Lecture-45 (Part-2)

EE5325 Power Management Integrated Circuits

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Power Aware Design Techniques

- **Dynamic Voltage Scaling (DVS):** Supply is dynamically changed depending upon operating conditions (data rate power demand, process, temperature)
- **Dynamic Frequency Scaling (DFS):** Clock frequency is dynamically changed depending upon data load
- **DVFS:** Combines both DVS and DFS

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Dynamic Voltage Scaling (DVS)

- DVS is a technique to improve system efficiency by dynamically varying the supply voltage
- Supply voltage is reduced when load demand is low
- Can be used for envelope tracking or compensate for the process and temperature variations in devices

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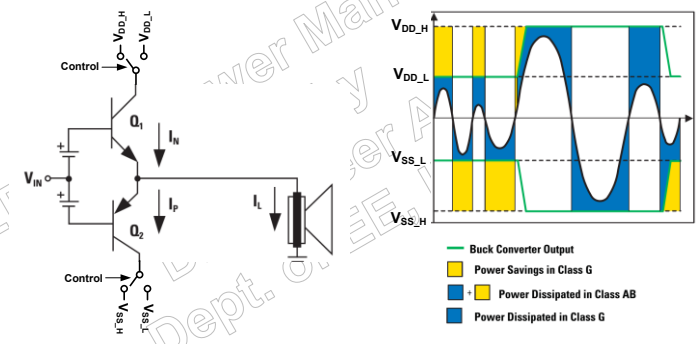
DVS in Class-G Amplifier

- Class-G = Class-AB with variable supply voltage
- Uses discrete levels of supply voltage
- Supply level is proportional to the signal level (power)



PowerWise® Class G versus Class AB. Headphone Amplifiers. — By *Richard Gomez, Audio Product Engineer, Texas Instruments*

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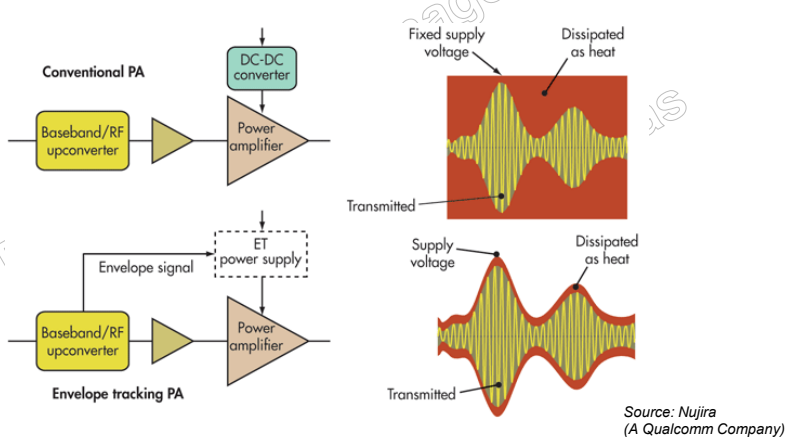
DVS in Class-H or Envelope Tracking PA

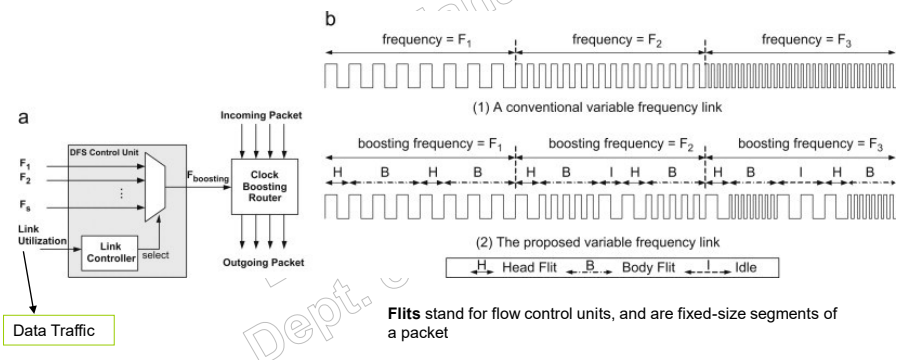
- Class-H = Continuous version of Class-G
- Supply voltage continuously tracks signal level
- Used in audio amplifier (low BW tracking) and RF PA (high BW tracking)



Source: Nujira (A Qualcomm Company)

Dynamic Frequency Scaling (DFS)

- Dynamic Frequency Scaling (DFS): Clock frequency is dynamically changed depending upon data load
- History based algorithm could be used to predict the data traffic

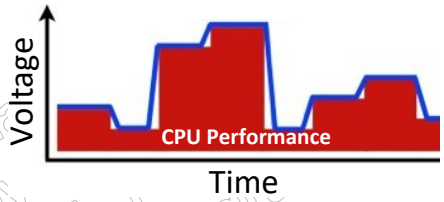


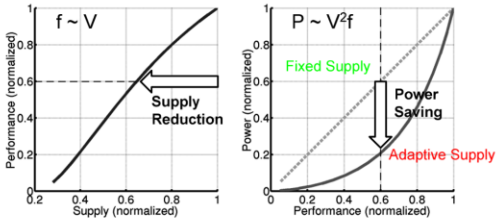
Flits stand for flow control units, and are fixed-size segments of a packet

Seung Eun Lee and Nader Bagherzadeh, A variable frequency link for a power-aware network-on-chip (NoC), Integration, the VLSI Journal Volume 42 Issue 4, September, 2009.

Dynamic Voltage Frequency Scaling (DVFS)

- DVFS = DVS + DFS
- Mostly used in processors and high speed serial links
- Processor performance is mainly controlled by clock speed. Transistors running at lower clock frequency does not require higher voltage
- Scaling voltage with frequency provides power saving by a factor of cube

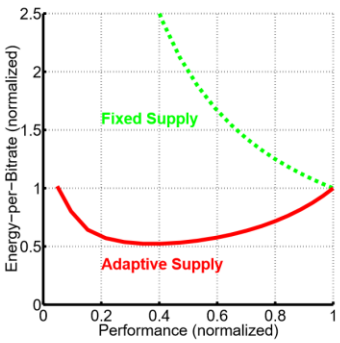




J. Kim, Design of CMOS adaptive supply serial links, PhD thesis, Stanford University, Dec 2002.

DVFS in High Speed Serial Links

- Most of the serial links are designed at slowest corner in order to meet the required performance – more power consumption if circuit is operated at other corners
- For a different data rates, operating the serial links at fixed power supply reduces the performance (bit rate/W)
- Adaptive Supply of serial link ensures min supply voltage required to operate the circuit at desired operating point thereby consuming min power



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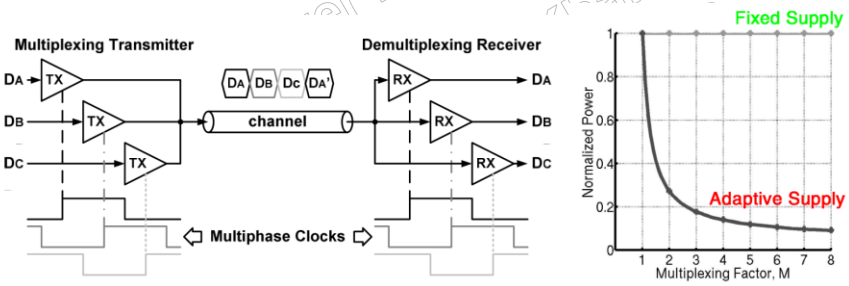
DVS with Parallel Serial Links

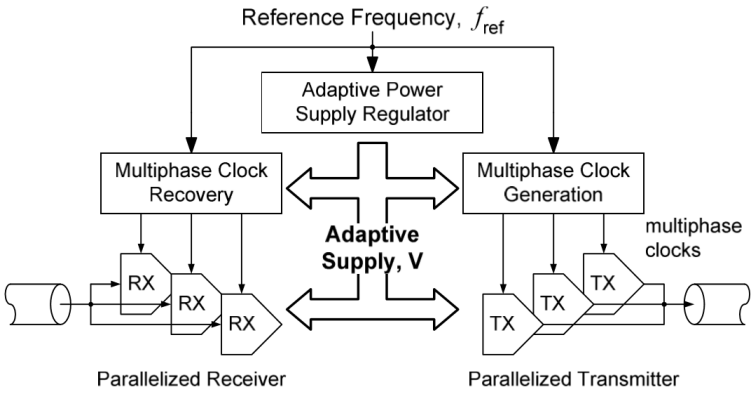
- Parallelizing the architecture provides significant power saving as supply voltage is scaled with frequency
- Instead of single link operating at frequency f, M number of parallel links are used and operated at f/M frequency
- The links are multiplexed in time to transmit the data on single line



J. Kim, Design of CMOS adaptive supply serial links, PhD thesis, Stanford University, Dec 2002.

Architecture of Adaptive Supply Serial Links

- Supply of Tx and Rx is varied with reference frequency
- Requires a dc-dc power converter which can be programmed with fref



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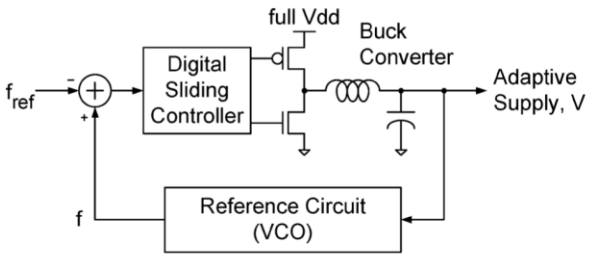
DC-DC Converter for DVFS

- **A sliding mode control is preferred it's switching frequency varies with output voltage and provide high efficiency over wide range of output**
- **Sliding mode control is non-linear like hysteretic (bang-bang) which has robust stability and fast transient response as compared to it's PWM counterpart**
- **Suitable for the application where ripple frequency is not a concerned**



- J. Kim and M. A. Horowitz, "An efficient digital sliding controller for adaptive power-supply regulation," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 639-647, May 2002.
- J. Kim and M. A. Horowitz, "Adaptive supply serial links with sub-1-V operation and per-pin clock recovery," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 11, pp. 1403-1413, Nov 2002.