Lecture-45 (part-1)

EE5325 Power Management Integrated Circuits

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Time-Based Low Drop-Out Regulator (LDO)

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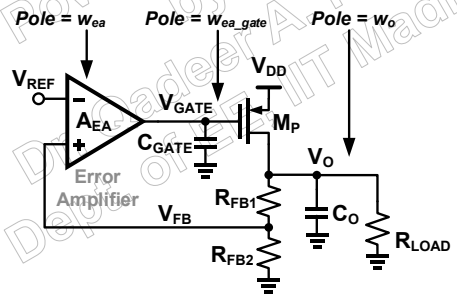
Low Drop-Out Regulator

- A conventional low drop-out regulator (LDO) suffers from trade-off between power and area.
- Pole, w_o, worsens the situation particularly under light-load condition due to high output resistance.
- Most of state-of-the art LDOs either consume high quiescent current, large on-chip capacitance or achieve limited bandwidth.
- Reduced bandwidth degrades power supply rejection (PSR) and transient response.



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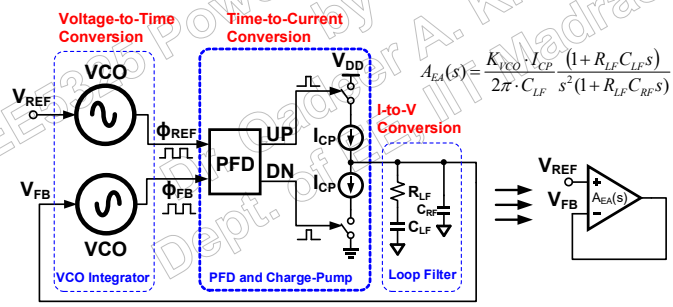
Time-Based Error Amplifier

- Concept of time-based error amplifier is derived from type-II phase locked loop (PLL).
- A voltage-controlled oscillator (VCO) is used for voltage-to-time/phase conversion which also acts as a phase integrator.
- Under lock condition, $F_{FB}=F_{REF} \rightarrow V_{FB}=V_{REF}$, assuming two VCOs are identical.



$$A_{EA}(s) \simeq \frac{K_{VCO} \cdot I_{CP}}{2\pi \cdot C_{LF}} \frac{(1+R_{LF}C_{LF}s)}{s^2(1+R_{LF}C_{RF}s)}$$

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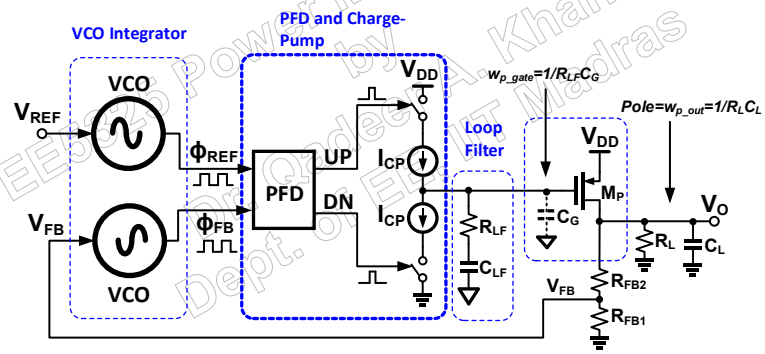
Time-Based LDO

- Concept of time-based error amplifier can be extended to LDO by adding a pass element, M_P to drive the output load R_L and C_L.

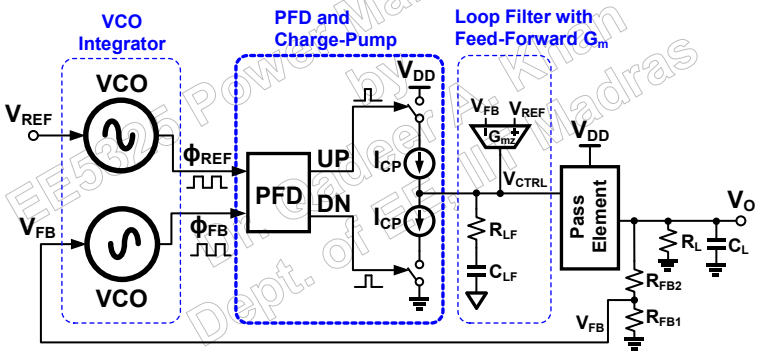
$$H_{LG}(s) = \frac{A_{PE} \cdot \beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot C_{LF}} \cdot \frac{(1 + w_{z_LF})}{s^2(1 + w_{p_gate})(1 + w_{p_out})}$$



Time-Based LDO with FF Compensation

- Feed-forward compensation cancels one of the poles (w_{p_gate} and w_{p_out}) and stabilizes the loop

$$H_{LG}(s) = \frac{A_{PE} \cdot \beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot C_{LF}} \cdot \frac{(1 + w_{z_LF})(1 + w_{z_FF})}{s^2(1 + w_{p_out})} \qquad w_{z_FF} = \frac{\beta \cdot K_{VCO} \cdot I_{CP}}{2\pi \cdot G_{mz}}$$



Area and Current Efficient Capacitor-Less Low Drop-Out Regulator Using Time-Based Error Amplifier, ISCAS-2018, Florence, Italy, May, 2018.

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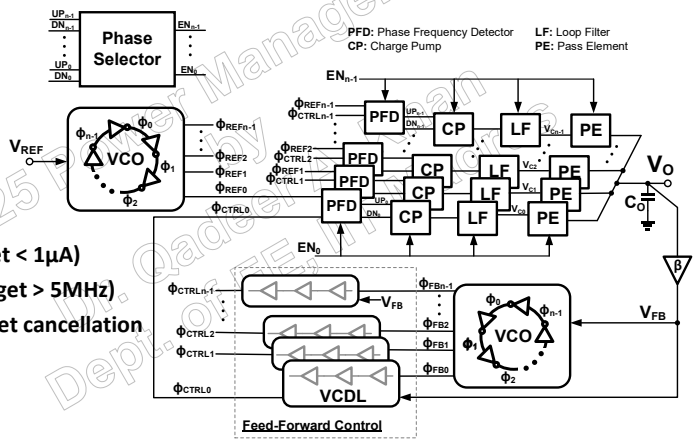
Multi-Phase Time-Based LDO

- Auto-Reconfigurable → numbers of phases are turned on/off based on load currents
- Seamless transition between number of phases



- Low IQ (target < 1µA)
- High BW (target > 5MHz)
- Dynamic offset cancellation

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Issues with Time-Based Controller

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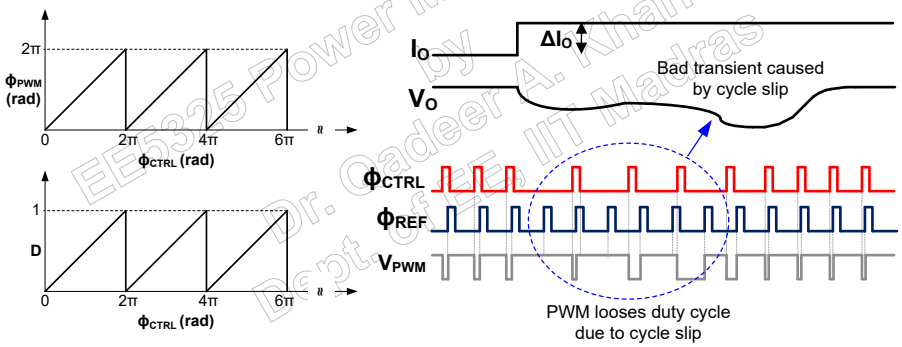
Problem-1: Cycle Slipping

- Since VCO phase folds back after every 2π, it causes duty cycle to reset and losing the duty cycle lock
- Duty cycle slipping may cause instability in the output before it acquires the phase lock again



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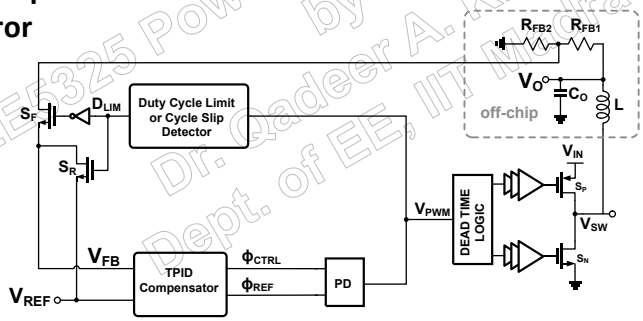
Solution: How to Avoid Duty Cycle Slip

- A cycle slip or min/max duty cycle detector can be used
- Once cycle slip is detected, error current to VCOs is made zero by applying V_{REF} to V_{FB}
- VCO phase will not accumulate further when there is no error



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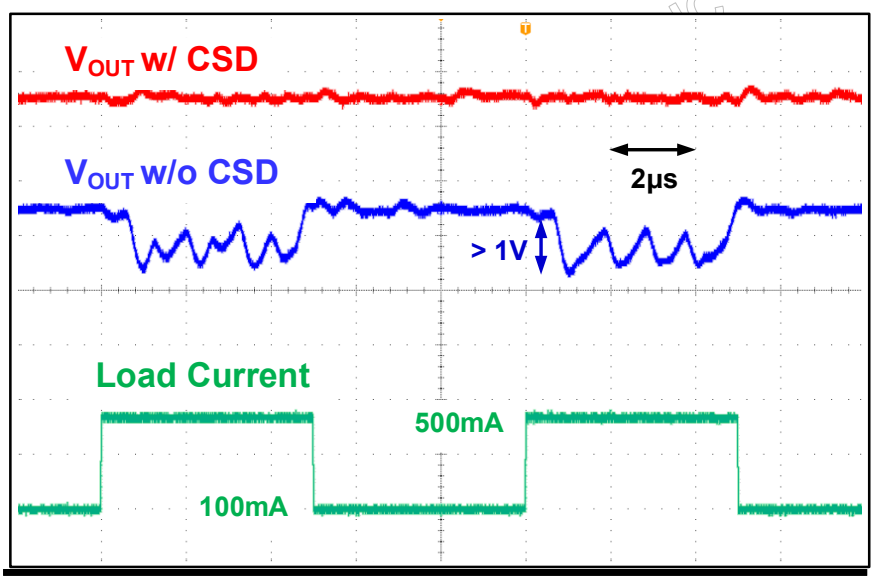
CSD Operation



Problem-2: Offset Due to VCO Mismatch

- Since any error between frequencies of two VCOs is integrated in phase, mismatch in VCOs will cause offset in input voltage
- Considering 10MHz frequency and K_{VCO} of 1MHz/V, 1% mismatch in VCO will introduce 100KHz offset in frequency
- Assuming offset frequency due to mismatch is Δf_{VCO}, absolute input referred offset voltage can be represented as:

$$V_{OS} = \frac{\Delta f_{VCO}}{K_{VCO}}$$

- 1% between VCOs causes 100mV offset which is 16.67% for V_{REF}=600mV.

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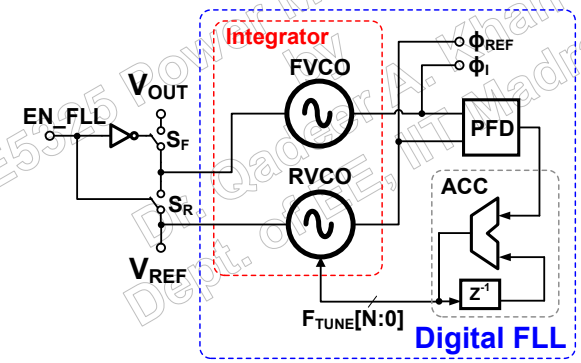
Solution: Offset Cancellation

- Mismatch between VCOs can be corrected by locking two VCOs to same frequency during startup
- Digital FLL is used for frequency locking
- Any offset in Gm also gets corrected during the calibration



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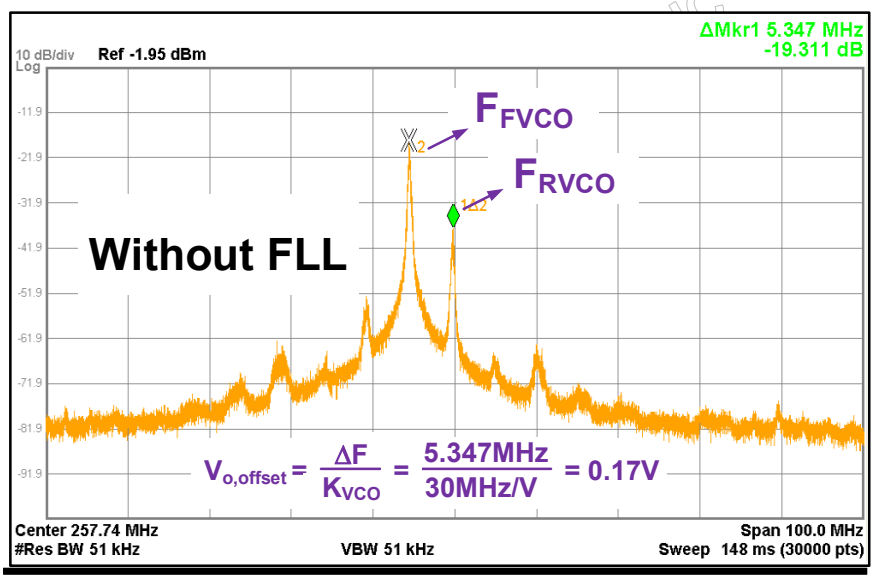
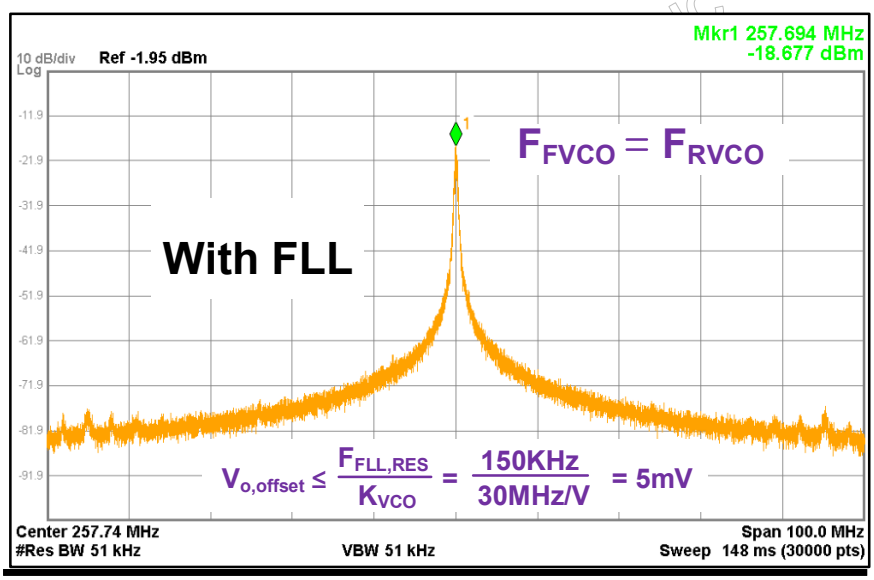
Oscillator Frequency Spectra



Oscillator Frequency Spectra