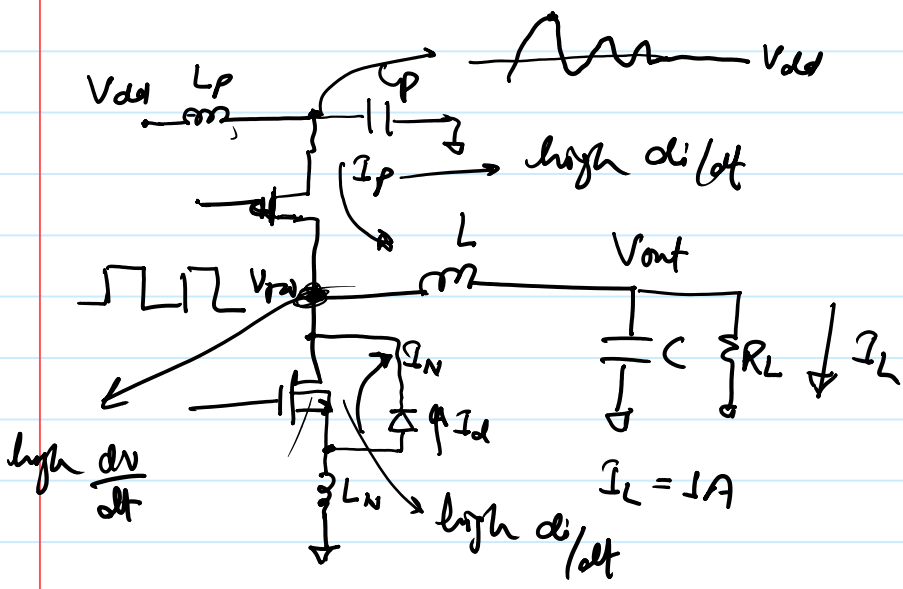
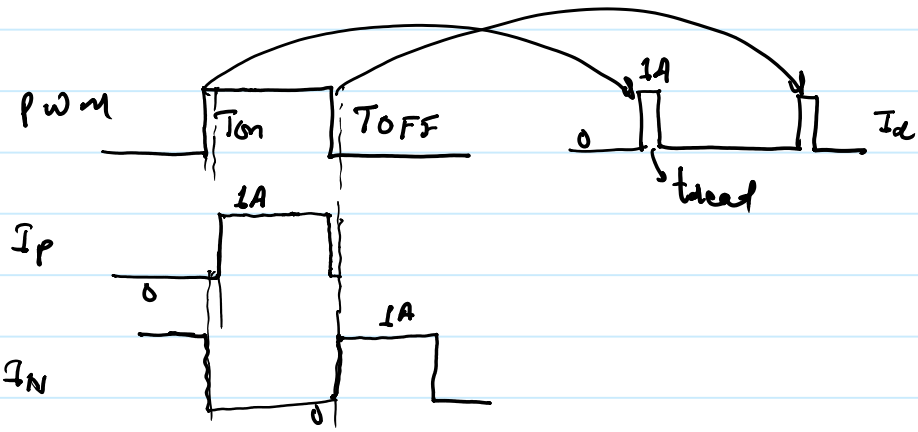
Noise in DC-DC





$$V_L = L\frac{di}{dt}$$

$L = 1nH$, $dt = 1ns$

$V_L = 1V$ $\quad di = 1A$

High di/dt Path ⟶ minimize palasitic L

High dv/dt ⟶ reduce palasitic C

Layout Guidelines