Lecture-42

EE5325 Power Management Integrated Circuits

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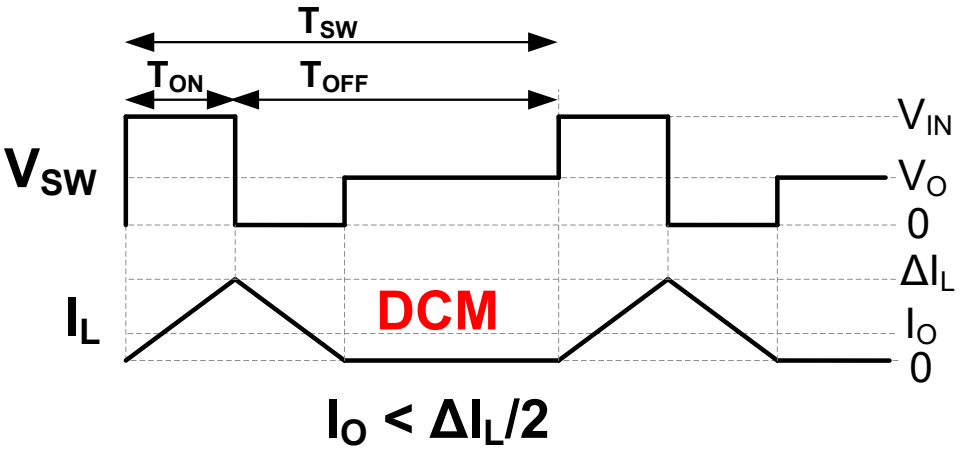
How to Enable PSM Mode

PSM mode is usually enabled when converter hits min or max duty cycle

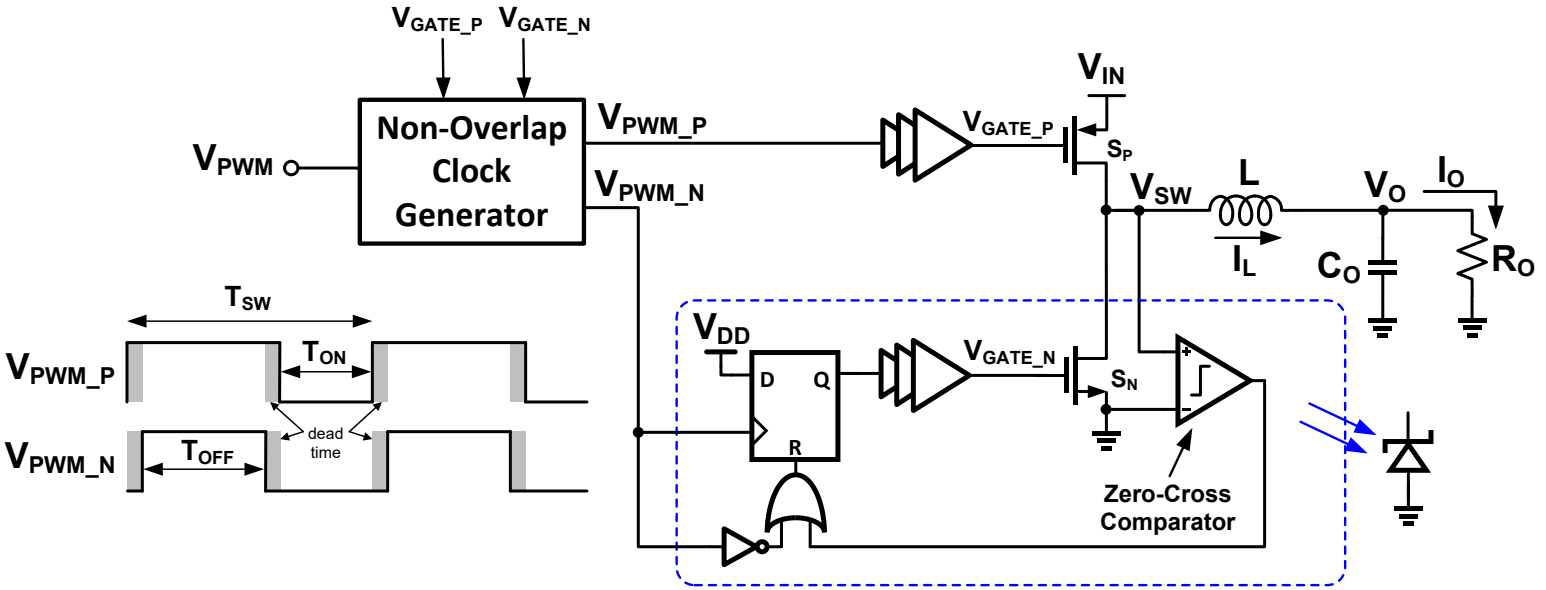
- **For a buck converter:**
  - **Minimum duty cycle can hit either under light load or when Vo/Vin ratio is quite low**
  - **Maximum duty can hit when Vo/Vin≈1 (close to 100% duty cycle)**
- **For a boost converter:**
  - **Minimum duty cycle can hit either under light load or when Vo/Vin≈1 (close to 0% duty cycle)**
  - **Maximum duty is very rare case in boost (>10x boost ratio in CCM)**

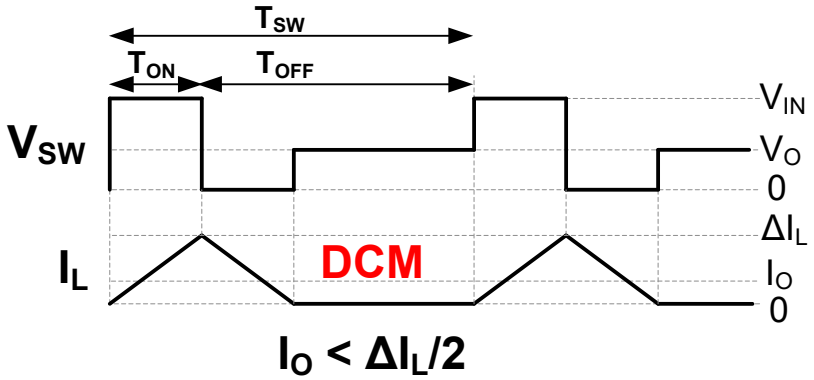
Detecting CCM-DCM Boundary

- Converter is operated in DCM by turning OFF low side FET (S_N) as soon as inductor current goes zero
- Zero current can be detected using zero-cross comparator as V_{SW} goes from negative to positive
- Can be used to switch from PWM to PFM mode
- Usually CCM-DCM detector output is de-bounced before entering/existing DCM mode to filter out any transient (momentarily) condition



Implementing DCM Operation





$I_O < \Delta I_L/2$

Zero-Cross Comparator Requirement

- **Since voltage drop across NFET is low (due to low R_{ds_on}), a very high gain and low offset comparator is required to detect the inductor reverse current**
  - **Assuming 100mOhm Rds_on, 1mV error may cause error of 10mA in zero current detection.**

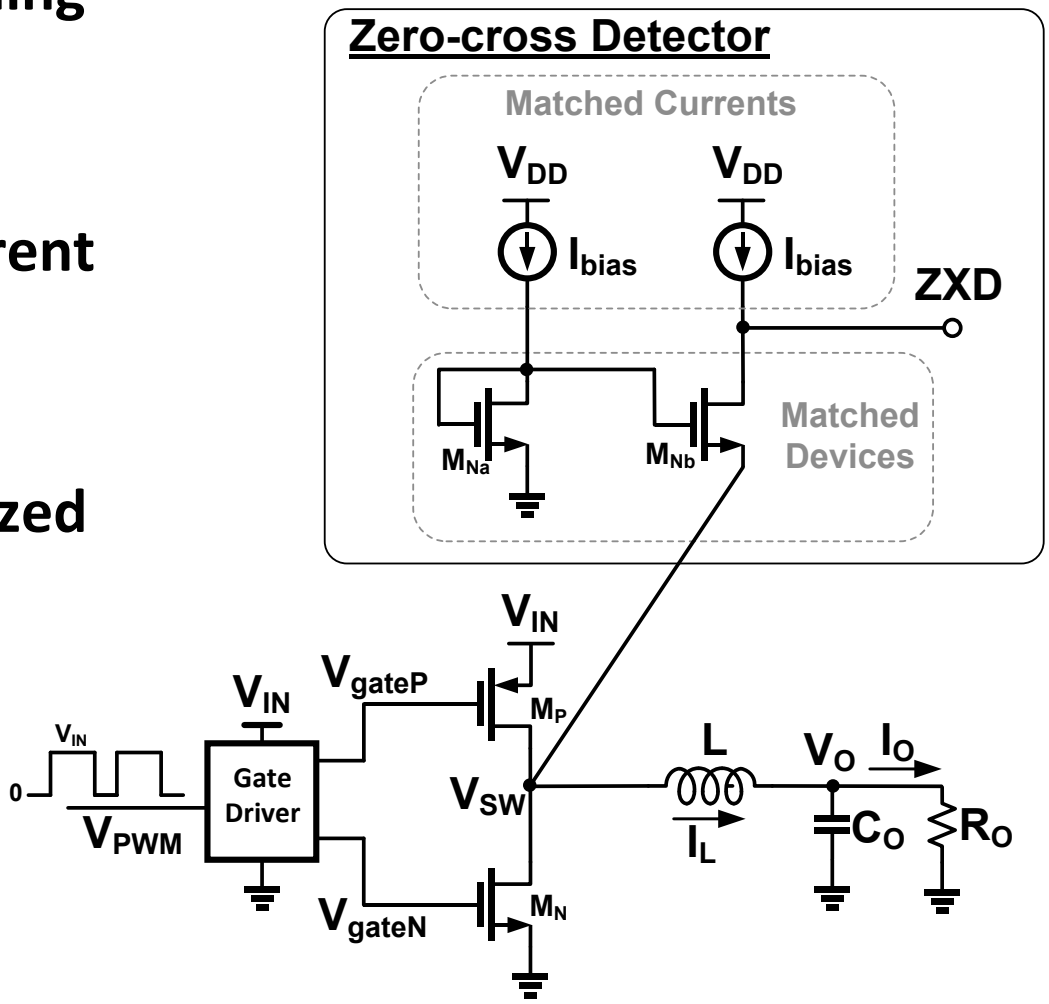
- **Comparator delay should be minimized as it may also introduce error**
  - **Assuming 1MHz and 10% duty cycle, with Vout=1.2V, L=1uH, inductor current slope is 1.2A/us → 10ns delay can cause an error of 12mA in the zero current detection**
  - **This becomes even more challenging when switching at higher frequencies (10MHz and above).**

Zero-Cross Comparator Topologies

- Conventional two stage comparator is not suitable of zero current detection mainly due to large delay
- High speed comparator with offset cancellation is usually required to minimize the error
- Current comparator can also be used to minimize the delay

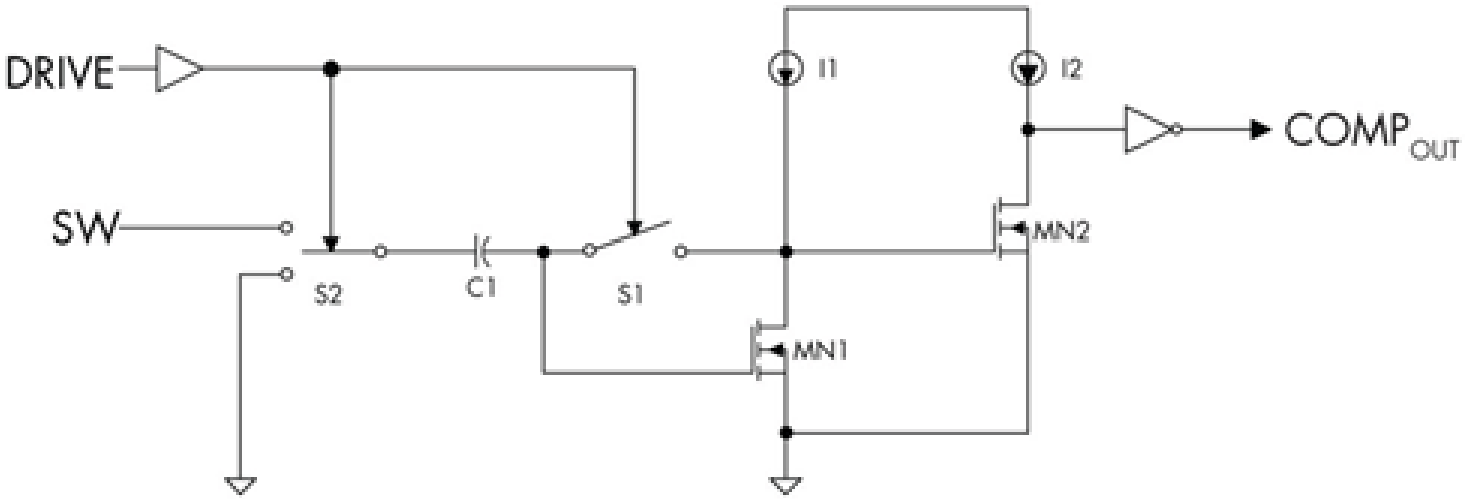
Current Based Zero-Cross Detector

- Requires good matching between devices
- Any mismatch in current will introduce offset
- Offset can be minimized by good layout and cascaded devices



Inverter Based Auto-Zeroed Comparator

- When DRIVE=1, C1 is pre-charged to Vgs of MN1
- When DRIVE=0, C1 samples V_{SW} node
- COM_{OUT}=1 if $V_{SW} < 0$
- Offset is automatically cancelled



Stephen W. Bryson , Using auto-zero comparator techniques to improve PWM performance, *eetimes article, 2008*