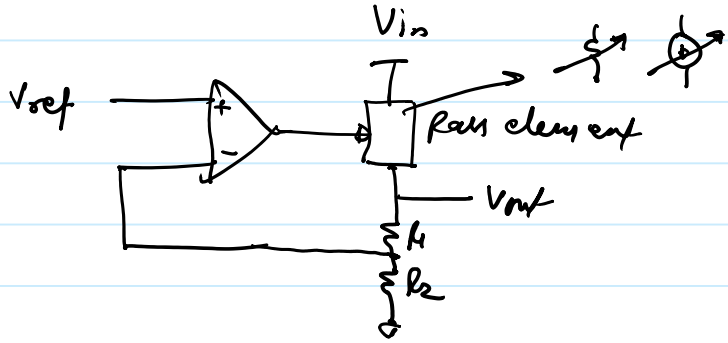
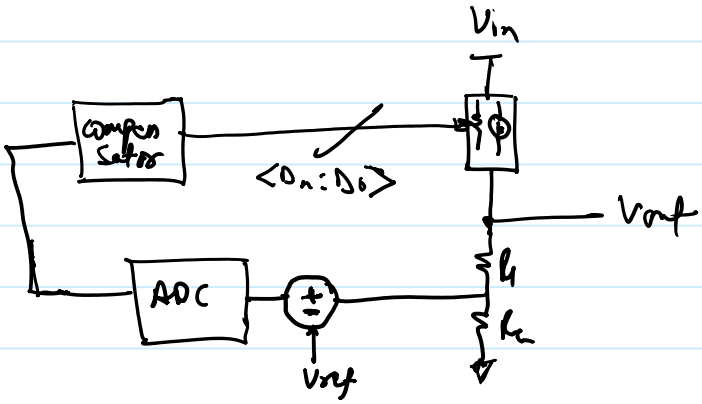
Digital LDO

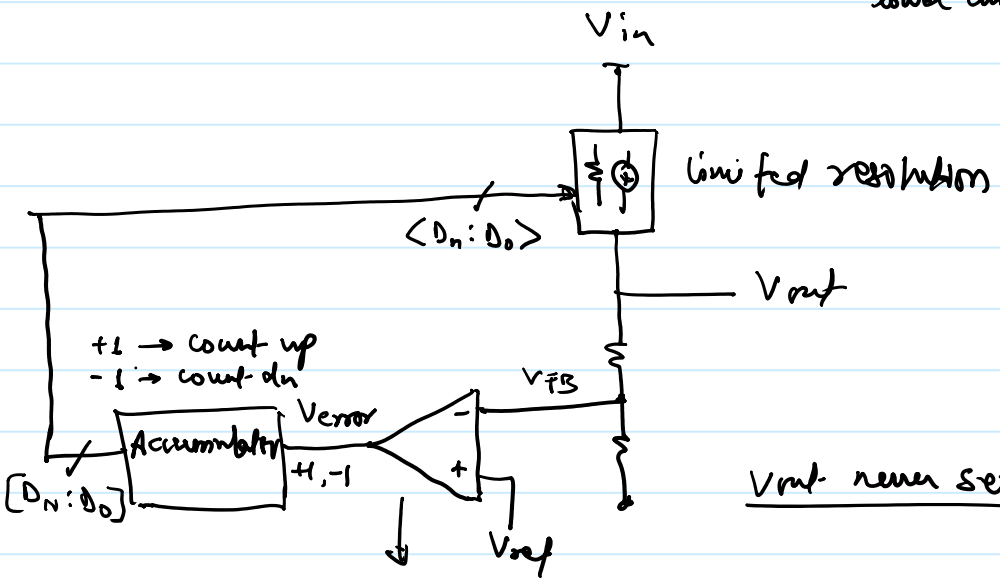




Advantages:

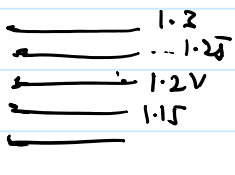
Smaller area
- no error amp
- no compensation capacitor

Low IQ
- ADC can be built using 1 or 2 comparators with much lower current.



Vout never settles → limit cycle oscillations

Single bit ADC (output never settles)

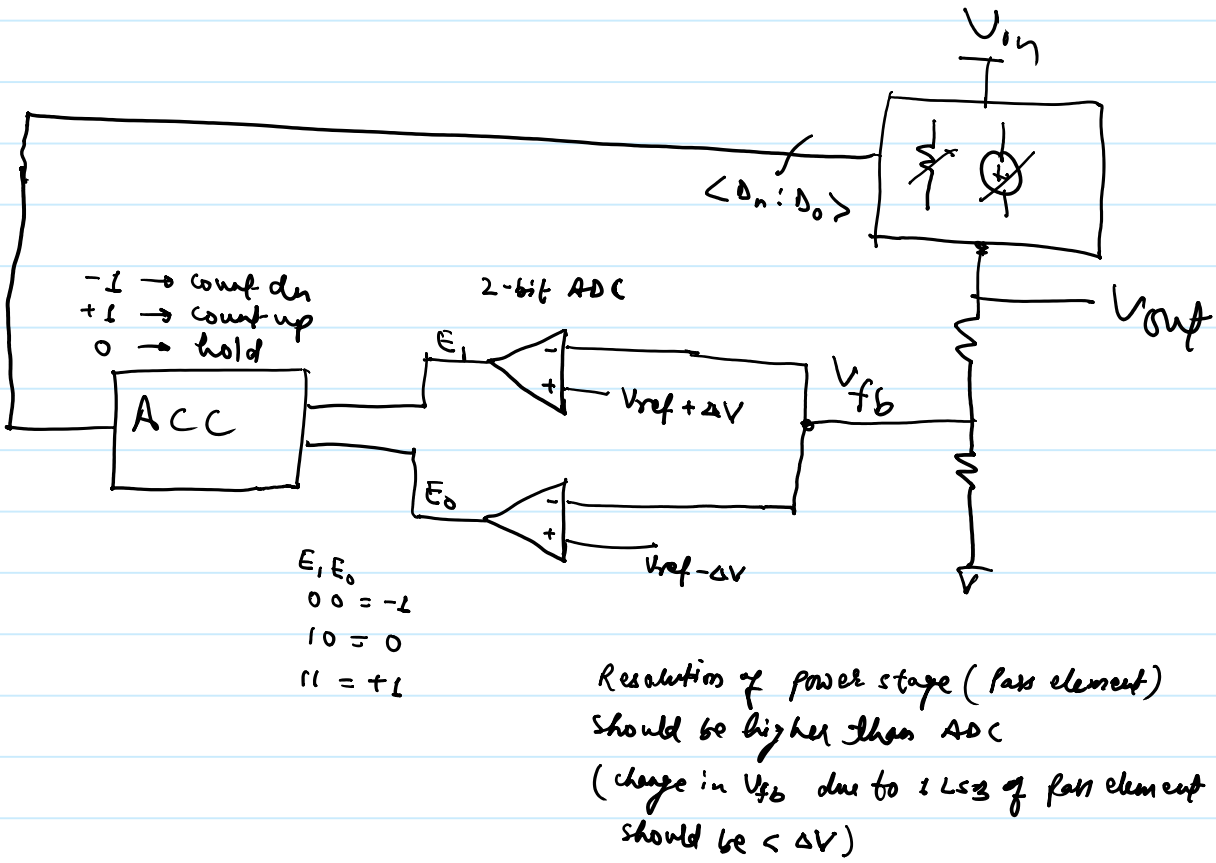


$$y(n) = y(n-1) + x(n)$$

Limit Cycle

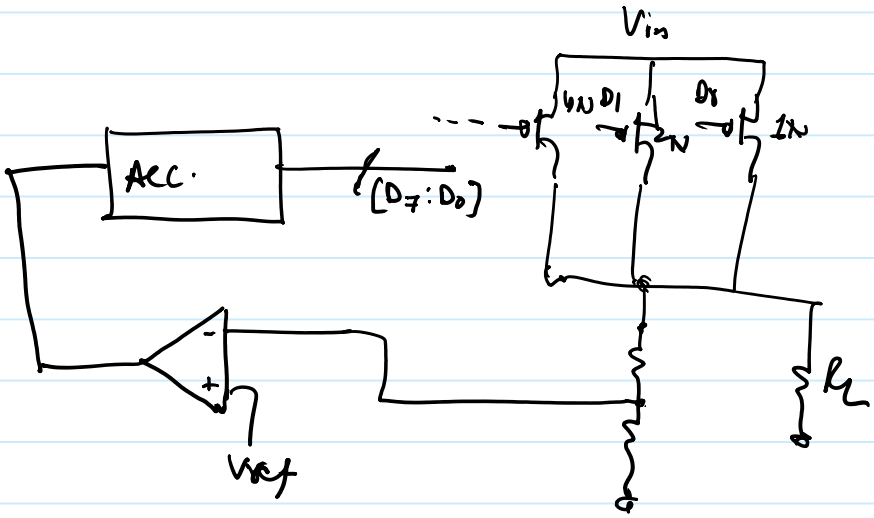
Limit cycle oscillation can be reduced by ensuring small loop delay ⇒ RC time constant at output should be $\frac{1}{5}$ th or smaller than update rate of accumulator.

oscillation around Vref (± LSB) can be removed by using more than 2 levels in ADC.

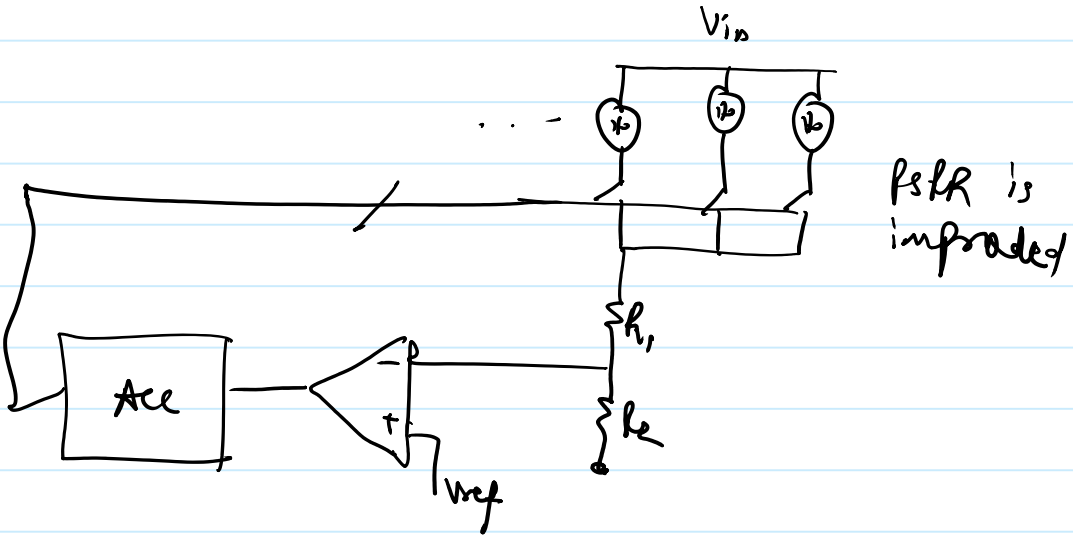


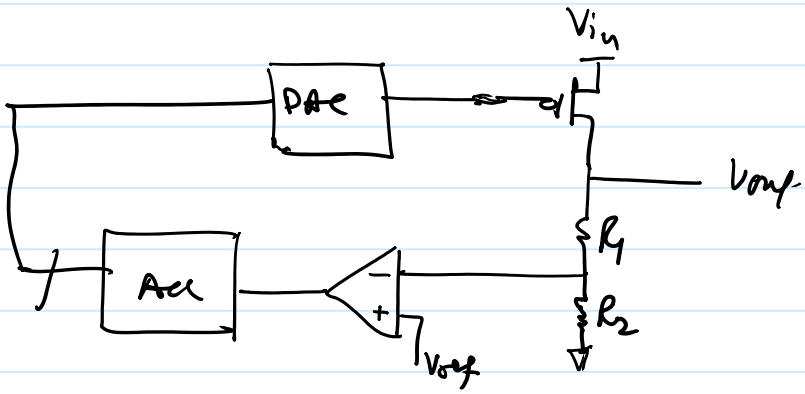
Resolution of power stage (pass element) should be higher than ADC
(change in V_{fb} due to 1 LSB of pass element should be < ΔV)

Using D/A Converter

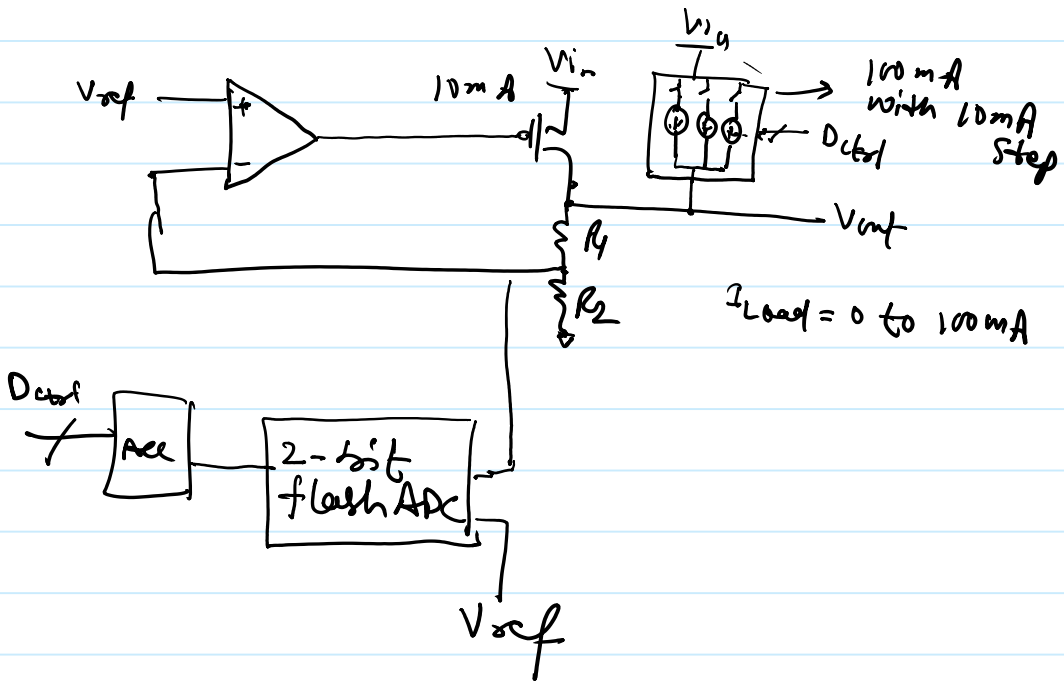


PSRR is not good.





Hybrid LDO


Vref
10mA
Vin
Vin
100mA
with 10mA
Step
Dctrl
Vout
R1
R2
ILoad = 0 to 100mA
Dcorf
Acc
2-bit
flash ADC
Vref