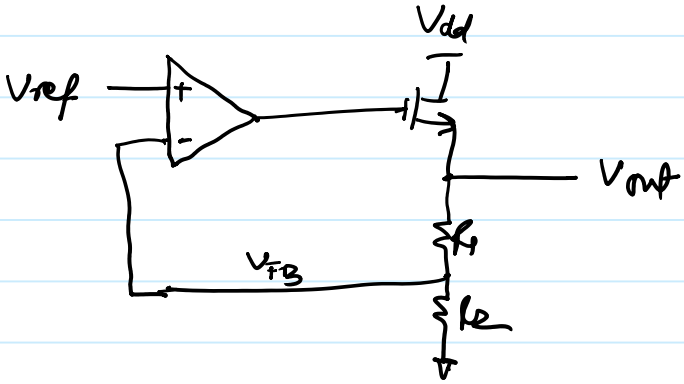
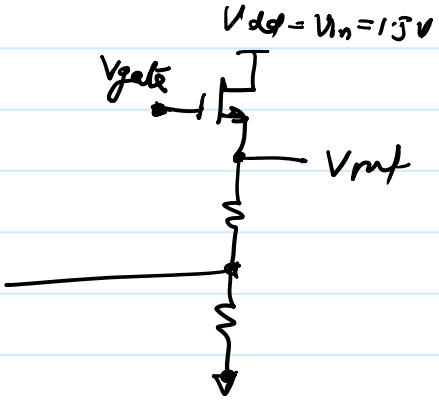
PMOS vs NMOS LDOs



$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

Increased drop-out - bad
Reduced Rout - good
PSRR is good - good
Lower loop gain = AEA
Smaller area

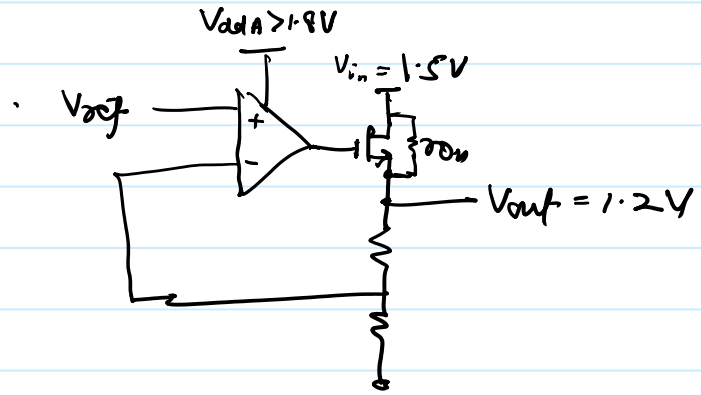
Increased drop-out



$V_{in} = 1.5V$
$V_{out} = 1.2V$
$V_{th} = 500mV$
$V_{od} = 100mV$

$V_{gate} = V_{out} + V_{gs}$
$= V_{out} + V_{th} + V_{od}$
$= 1.2 + 500mV + 100mV$
$= 1.8V$

PMOS vs NMOS LDOs



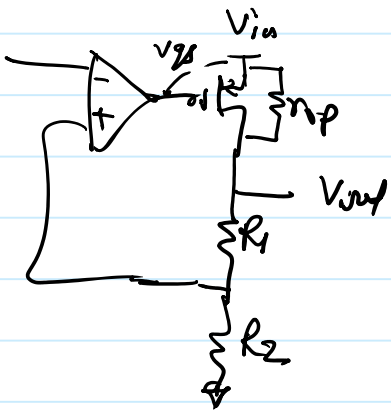
$$V_{out} = \frac{R_L}{r_{on}+R_L} V_{in}$$

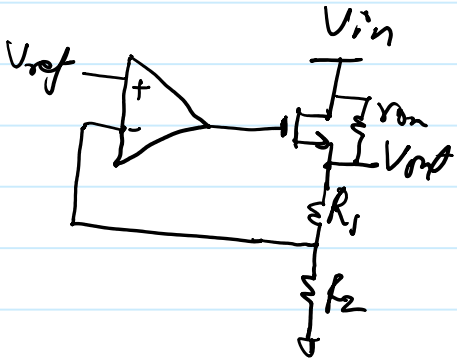
$\mu_n > \mu_p \quad \simeq 2\times$

Better PSRR

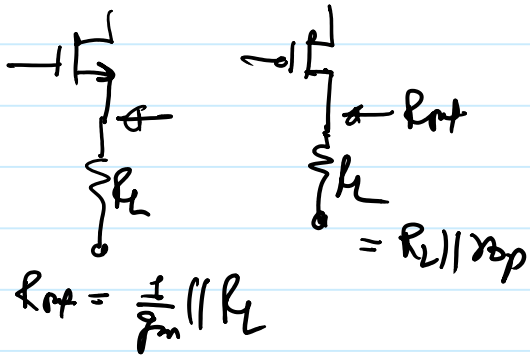
PMOS LDO has $g_m \cdot V_{in}$ path due to V_{gs} and r_{op} path.

NMOS LDO has only r_{on} path.





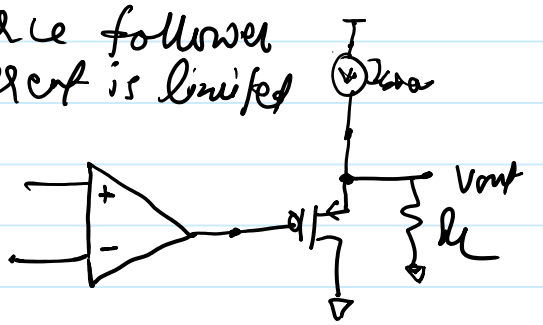
Reduced R_{out}



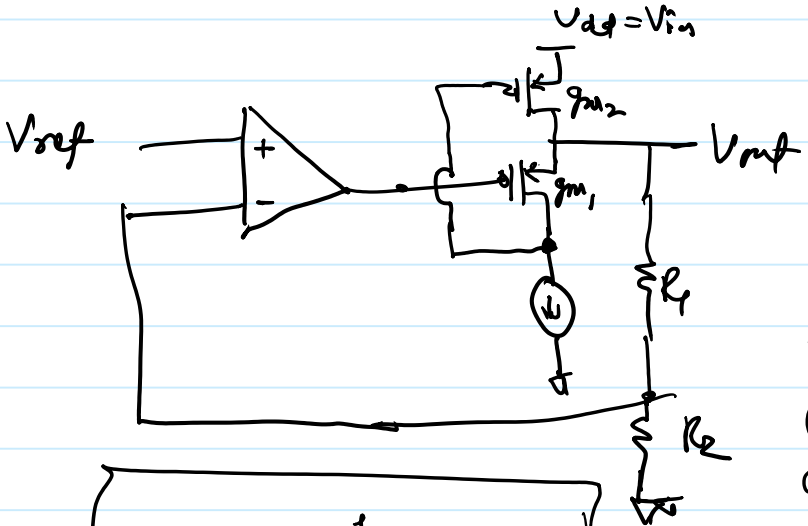
$$R_{out} = \frac{1}{g_m} \| R_L$$

LDO with Flipped Source Follower

pmos source follower
⇒ output current is limited to I_{bias}.



good for current sink not source.



Flipped source Follower

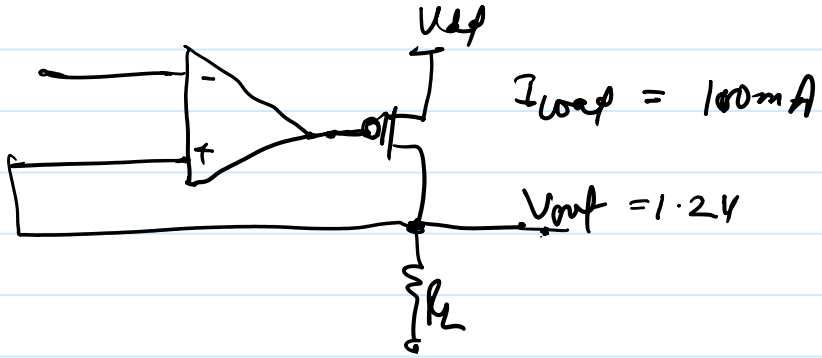
Good for sourcing current.

$$R_{out} = \frac{1}{g_{m_1} \times g_{m_2} r_{o_1}}$$

Similar characteristics as pmos LDO with much lower Rout

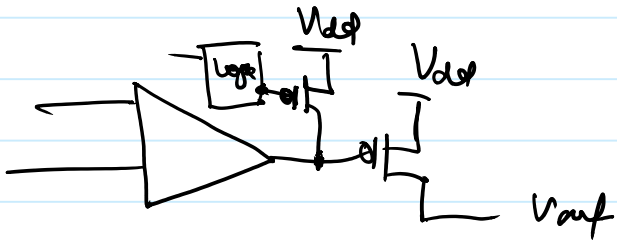
current limit

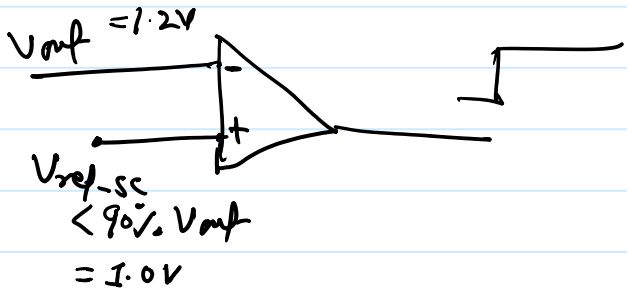
protection from high current
short circuit protection



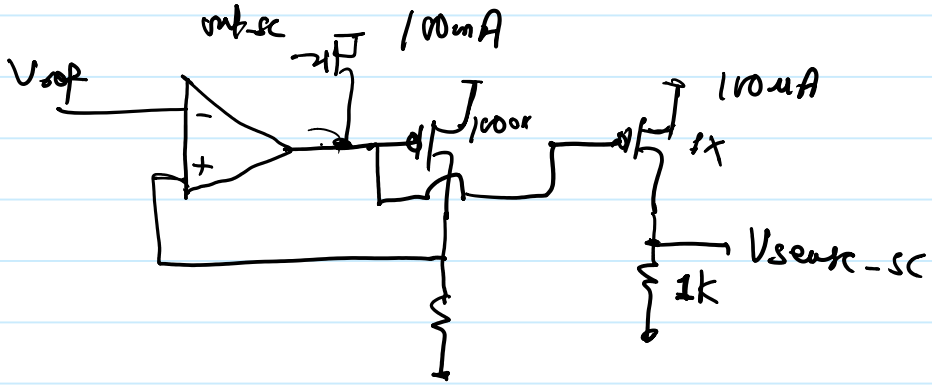
short circuit protection

① Turn OFF PMOS

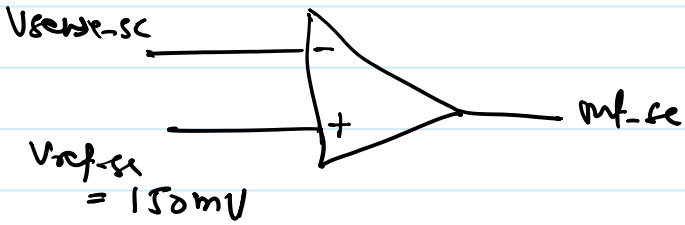




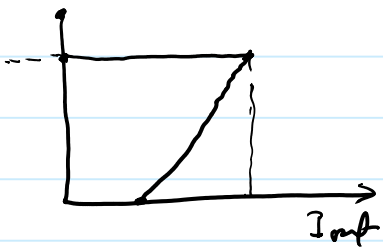
Current Limit and Short Circuit Protection



I_{limit} = 25-30% of max I_{load}



Foldback current limit



Power dissipation in PMOS

$= (V_{in} - V_{out}) I_{out}$

$V_{out} = 0$ when SC

Current Limit and Short Circuit Protection