ADVANCED ELECTRICAL NETWORKS : PROBLEM SET 4

Problem 1

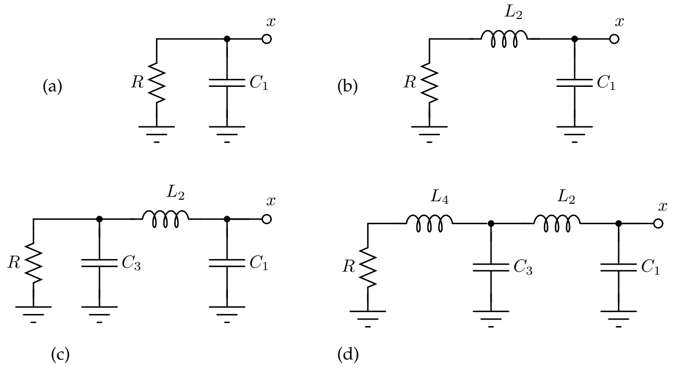

Figure 1: Networks for Problem 1(a).

(a) Fig. 1 shows four passive impedances. In the last tutorial, most of you plodded through the algebra to determine the mean square noise across node x and ground. It should have intrigued you that the mean square noise in all cases turned out to be kT/C_1. In this tutorial, use contour integration to determine the integral of the noise spectral density. You should integrate over an infinite semicircle enclosing the right-half s-plane. You may want to use the fact that the noise voltage spectral density of a passive impedance is $4kT\,\mathrm{Re}[Z(f)]$.

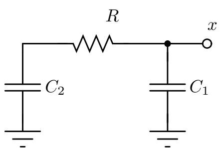

Figure 2: Networks for Problem 1(b).

(b) Now, evaluate the mean square noise voltage on C_1 in Fig.2, both by the contour integration method and through brute-force. Explain the results.

Problem 2

Fig.3 shows a resistive sheet, with thickness t, length l, width w and resistivity ρ. Four capacitors $C_1 \cdots C_4$ are soldered on to the sheet at arbitrary locations, as shown in the figure. Evaluate the mean squared energy stored on each capacitor.

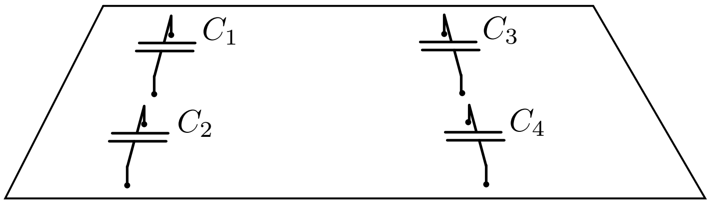

Figure 3: Network for Problem 2.

Problem 3

Consider an active network consisting of inductors, capacitors, resistors and ideal opamps. The circuit is such that

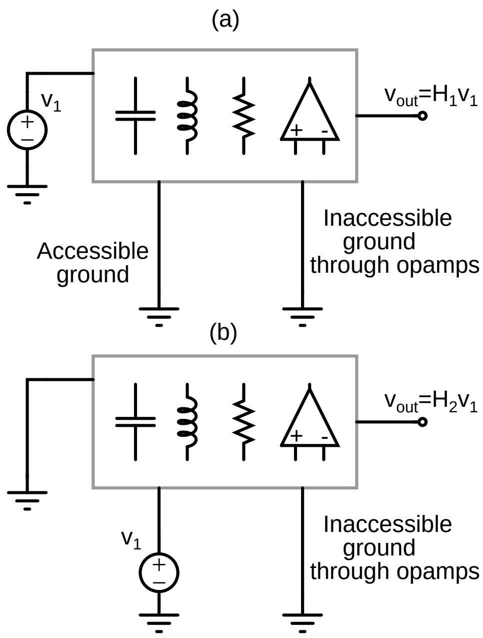

Figure 4: Opamps are ideal. One of the terminals of the output source of the opamp goes to ground, which is inaccessible.

there is negative feedback around all the opamps, so that their input terminals can be considered a virtual short. As you know, the opamp can be modeled as any one of the four controlled sources with transfer parameter (gain, transconductance set to infinity). Further, as you know, one of the terminals of the output source of the opamp goes to ground, which is inaccessible. So, the network can be represented as a box as shown in Fig. 4, where the accessible and inaccessible grounds are shown. Let $H_1(s)$ denote the transfer function from the v_1 to the output v_{out}, as shown in Fig. 4(a). Now, the input is grounded, and *the accessible ground is lifted off ground and connected to* v_1, as shown in Fig. 4(b). The resulting transfer function is $H_2(s)$. Determine $H_1(s) + H_2(s)$. It may help for you to consider a few opamp circuits you know, and see what happens in specific cases before applying it to the general case.

Problem 4

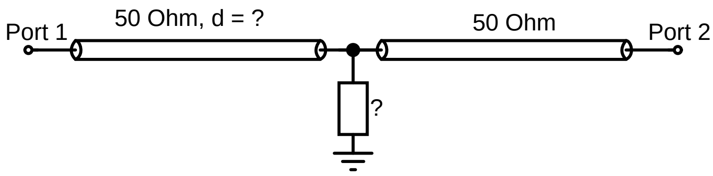

Figure 5: Figure for problem 4.

A two port network analyzer was used to characterize the two port shown in Fig. 9. The transmission line is ideal and lossless, and is 15 cm long - but has an unknown discontinuity at a distance d from port 1. The S_{11} of the two port was found to be

$$S_{11} = -\exp(-j2\omega \times 10^{-10}) \frac{\frac{j\omega}{\omega_o}}{2 + \frac{j\omega}{\omega_o}} \tag{1}$$

where $\omega_o = 20 \times 10^9$ rad/s. The transmission line has a dielectric with $\mu_r = 1$ and $\epsilon_r = 4$. Determine d and the element at the discontinuity.

Problem 5

Fig. 10 shows a periodically switched circuit, operating at 1 Hz. The two clocks ϕ_1 and ϕ_2 are 50% duty cycle, and do not overlap. The voltage controlled current source has a transconductance of G_m and is much greater than 1 S. Its output is connected to the switched capacitor using an ideal VCVS of gain 1, as shown in the figure. $v[n]$ denotes the voltage sampled on the capacitor at the end of ϕ_1. Determine $v[n]$ in steady state.

The 1 V DC source is now replaced by a sinusoidal source $\cos(2\pi t)$. Determine $v[n]$ now.

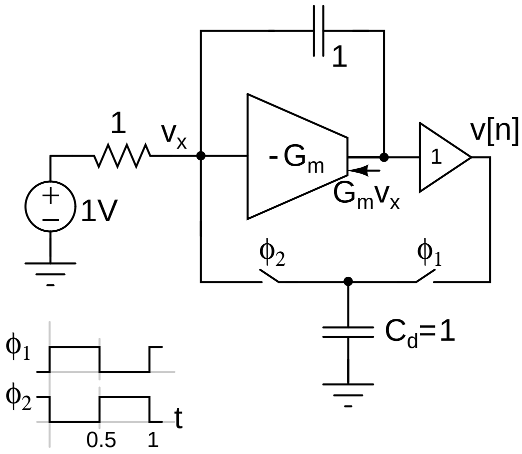

Figure 6: Figure for problem 5.

Problem 6

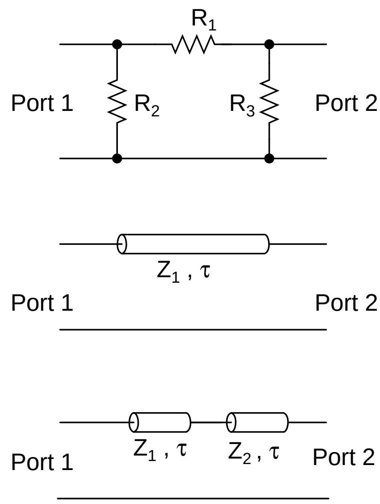

Figure 7: Problem 6

Determine the S-parameters of the two ports shown above. Assume the reference impedance to be Z_o.

Problem 7

Two 2-port networks with individual scattering matrices $[S^A]$ and $[S^B]$ are cascaded. What is the S_{21} of the cascade ? What is the intuition behind this answer ?

Problem 8

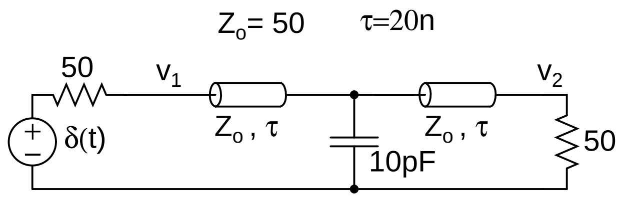

Figure 8: Problem 8

Determine $v_1(t)$ and $v_2(t)$ analytically and verify by SPICE simulation.

Problem 9

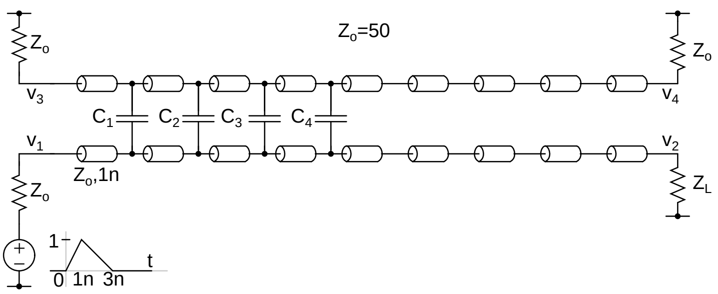

Figure 9: Problem 9

Fig. 9 shows two transmission lines. The input to the lower line is a triangular pulse, as shown.

a. For this part, assume $C_1, \cdots, C_4 = 0$ and $Z_L = 0$. Determine analytically and plot $v_1(t)$. Verify with SPICE by plotting what you get from simulation.

b. For this part, assume $C_1 = 10\,\text{fF}$, $C_2, \cdots, C_4 = 0$ and $Z_L = Z_o$. Determine analytically and plot $v_3(t)$ and $v_4(t)$. Verify with SPICE by plotting what you get from simulation.

c. For this part, assume $C_1, C_2, \cdots, C_4 = 10\,\text{fF}$ and $Z_L = Z_o$. Determine analytically and plot $v_3(t)$ and $v_4(t)$. Verify with SPICE by plotting what you get from simulation.

d. For this part, assume $C_1, C_2, \cdots, C_4 = 10\,\text{fF}$ and $Z_L = 0$. Determine analytically and plot $v_3(t)$ and $v_4(t)$. Verify with SPICE by plotting what you get from simulation.

Problem 10

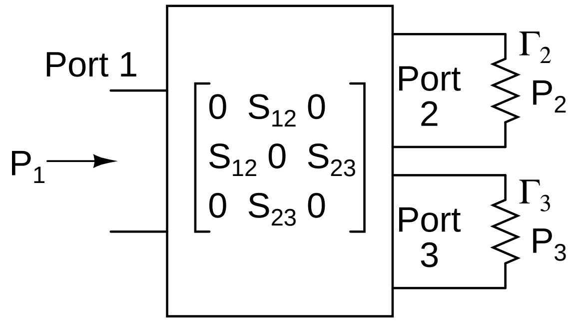

Figure 10: Problem 10

The S matrix of the 3-port is given. The reflection coefficients of the resistive loads at ports 2 and 3 are Γ_2 and Γ_3 respectively. Determine the power delivered into these loads (P_2 and P_3) if the power incident on port 1 is P_1.

Problem 11

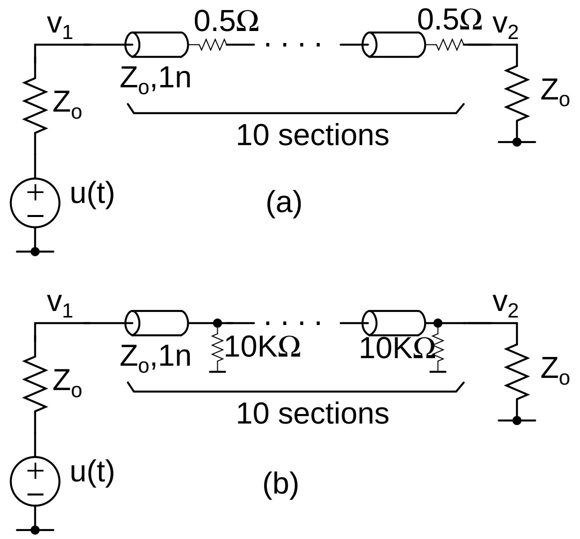

Figure 11: Problem 11

Fig.11(a) and (b) show transmission lines with series and shunt loss respectively. Determine and plot $v_1(t)$ and $v_2(t)$ for a step input. Verify with SPICE.

Problem 12

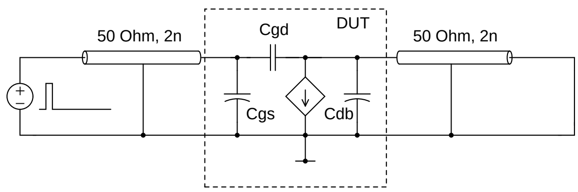

Figure 12: Problem 12

Fig.12 shows the equivalent incremental circuit for a test setup to measure y-parameters of a MOSFET biased in saturation. The cables conecting the signal generators (at both ports) can be modeled as transmission lines as shown in the figure.

a. For this part, assume $C_{gd} = 0$, $C_{gs} = C_{db} = 500\,\text{fF}$ and g_m=10 mS. Simulate the stability of the circuit in SPICE by impressing a small voltage pulse as shown. If the system is stable, the waveforms everywhere should eventually reach steady state.

b. Repeat part (a), but with $C_{gd} = 25\,\text{fF}$. What do you notice ? Why ?

c. Repeat part (b), but with a source impedance of 50 Ohms and the load end terminated by 50 Ohms instead of the short circuit. What do you notice ? Why ?