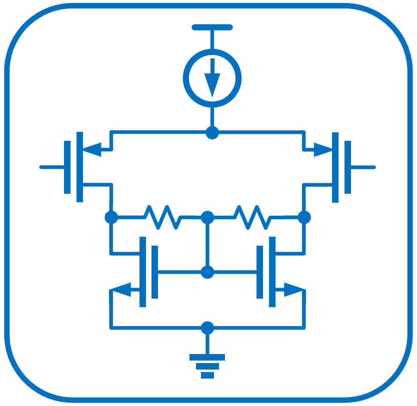
EE5320: Analog IC Design

Handout 3: MOSFETs



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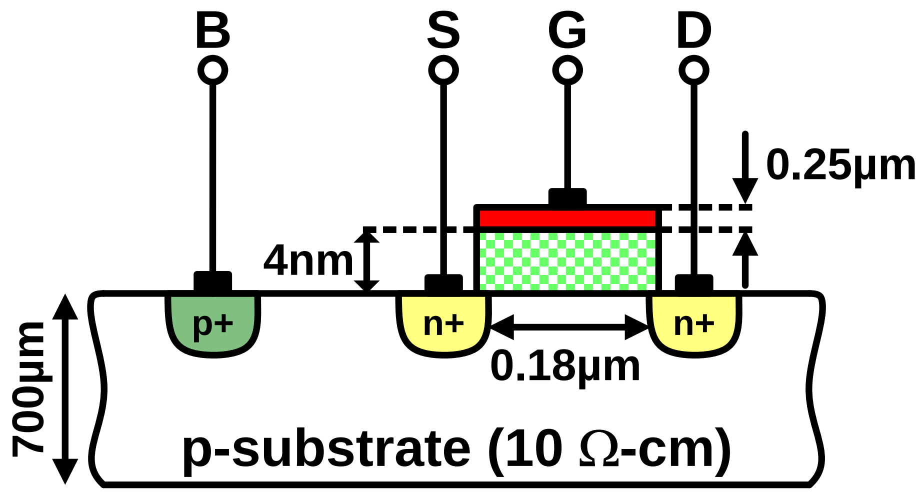
Overview

- Transistors in CMOS technology
  - Focus on NMOS and PMOS
  - Derive I/V characteristics
  - Regions of operation
  - Small-signal model
  - Secondary effects: channel-length modulation, body effect
  - Extrinsic capacitors

References

1. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Oxford University Press, 2006

Contact Terminals in NMOS Transistor

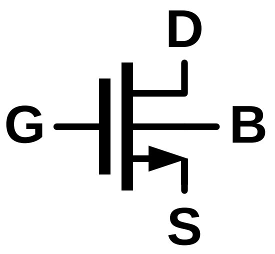


D: Drain

G: Gate

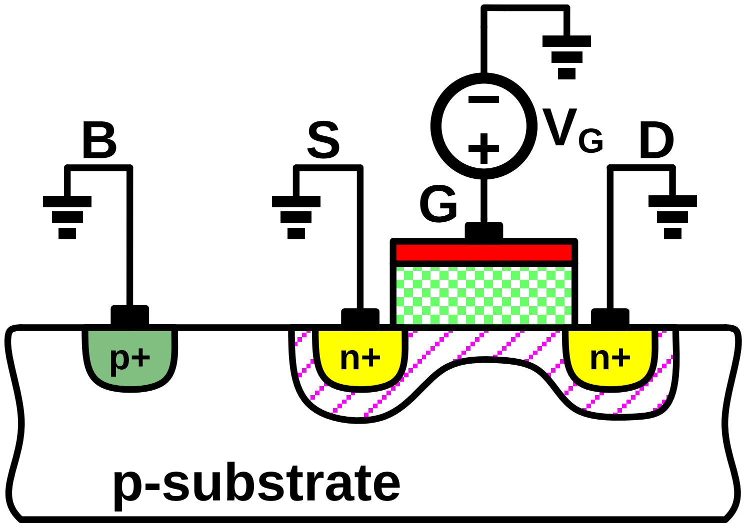
S: Source

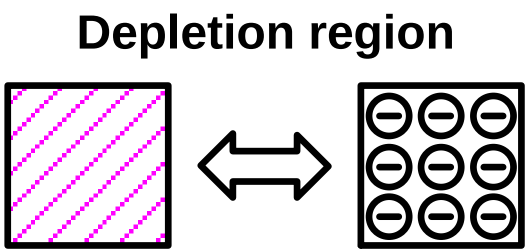
B: Bulk/substrate



- No current with zero bias voltages for G/D/S/B

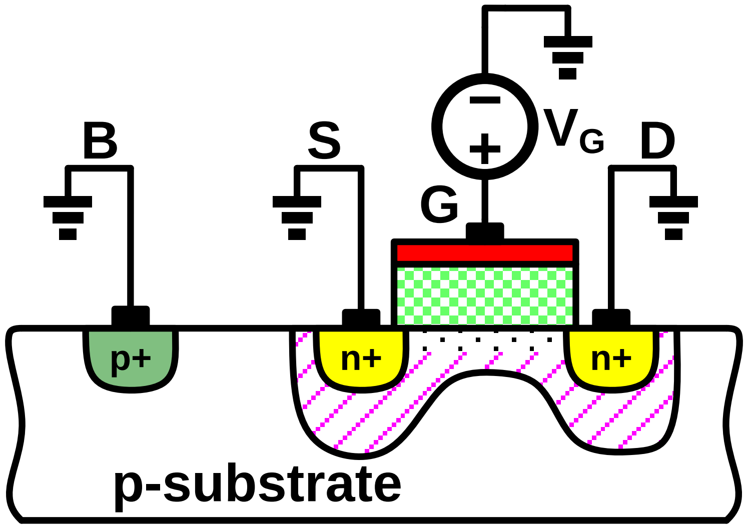
Channel Formation: Depletion

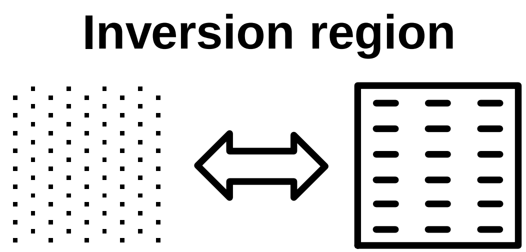




- Small positive voltage on the gate terminal introduces electric field in the p-substrate
- Holes in the p-substrate are repelled leaving negative ions
  - Forming depletion region
- Larger gate voltage increases depletion width

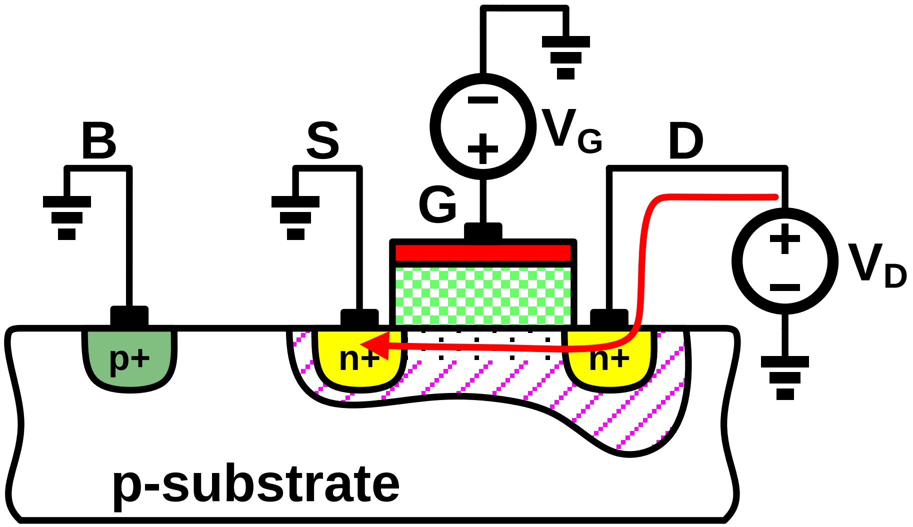
Channel Formation: Inversion





- Larger gate voltage pulls electrons from *electron-rich* source/drain region *inverting* majority carriers near gate
- Electron rich source (n+), drain (n+), & inverted substrate near gate forms a channel of free electron carriers

Channel Conduction

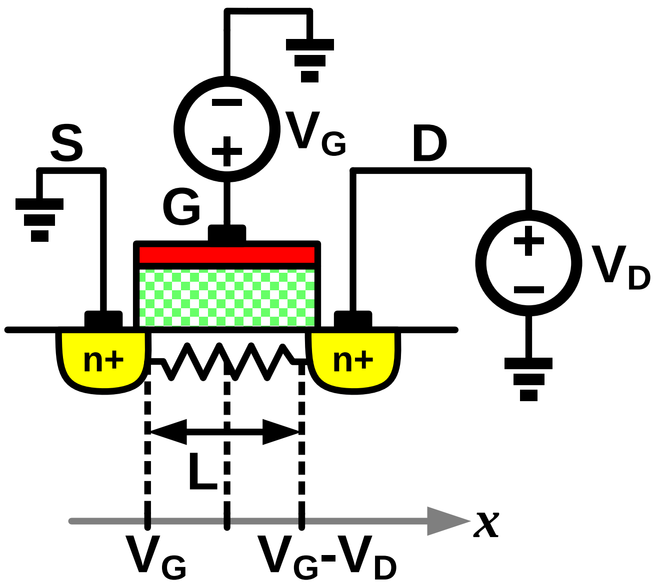


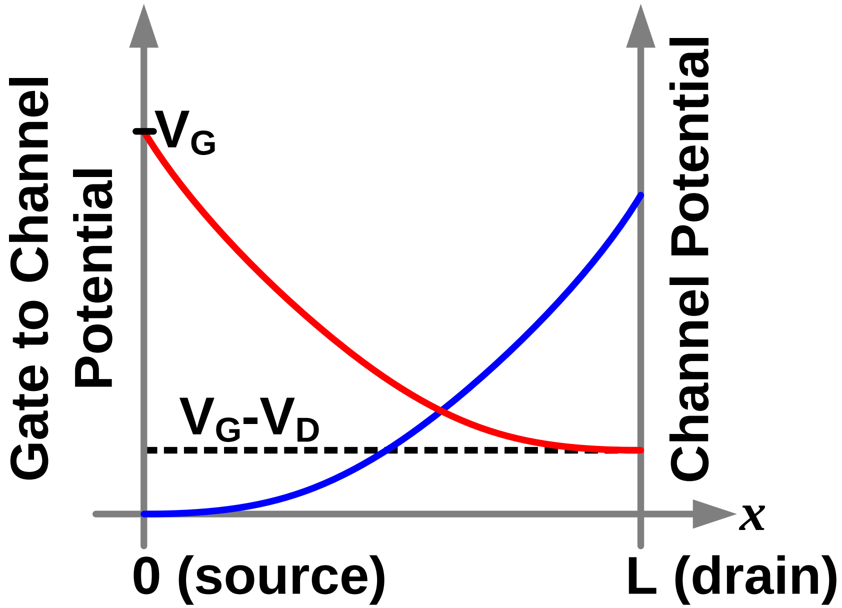
- Apply positive voltage on the drain terminal creating potential difference between drain and source
- Electrons flow from source to drain
  - Current flows form drain to source
- Larger gate voltage increases drain-to-source current

Threshold Voltage

- Formation of a channel (inversion layer) is gradual
- Need "a voltage" to indicate channel formation
- Threshold voltage: *Gate-to-source voltage to invert the surface of the substrate with same doping density*
- For an NMOS, it is the voltage to make the surface *n-type* as much as the substrate is *p-type*
- $V_{TH} \approx 0.5V$ in $0.18\mu m$ process

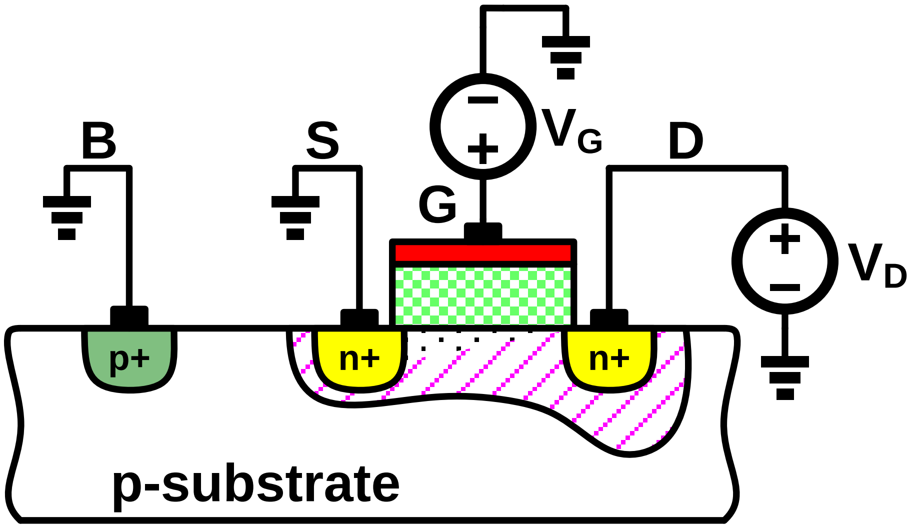
Channel Resistance





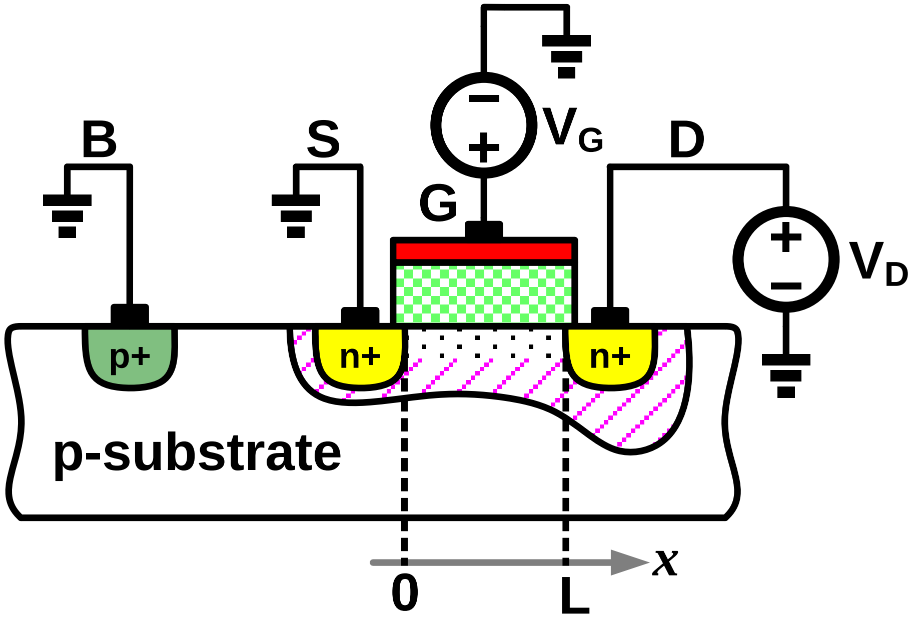
- Channel can be modeled as a resistor
- For positive drain voltage:
  - Channel potential decreases from drain to source (IR drop)
  - Gate-to-channel potential increases from drain to source

Channel *Pinch-off*



- If $V_{TH} > V_G - V_D$ → inversion layer stops at $x < L$
- Channel is said to be *pinched-off*
  - Carriers *drift* as opposed to diffusion
- Channel current saturates
  - Increasing V_{DS} does not increase I_{DS} provided $V_G < V_D + V_{TH}$
- Channel length modulated by V_{DS}
  - Large V_{DS} → Smaller channel length

NMOS Channel Current Equation(1)



$$\mathrm{Q(x)} = \text{Channel charge density}$$

$$\mathrm{Q_d} = \text{Charge per unit length}$$

$$\mathrm{V(x)} = \text{Channel potential}$$

$$v = \text{Carrier velocity}$$

$$\mathrm{Q(x) = C_{ox}[V_{GS} - V(x) - V_{TH}]}$$

$$\mathrm{Q_d(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}]}$$

$$\mathrm{I_{DS}} = \frac{\mathrm{Q_d(x) \cdot dx}}{\mathrm{dt}}$$

$$\mathrm{I_{DS}} = \mathrm{Q_d(x)}v = -\mathrm{Q_d(x)}\mu_n E = \mathrm{Q_d(x)}\mu_n \frac{\mathrm{dV(x)}}{\mathrm{dx}}$$

NMOS Channel Current Equation(2)

$$\mathbf{I_{DS} = W\mu C_{ox}[V_{GS} - V(x) - V_{TH}]\frac{dV(x)}{dx}}$$

$$\mathbf{Boundary\ conditions : V(0) = 0\ and\ V(L) = V_{DS}}$$

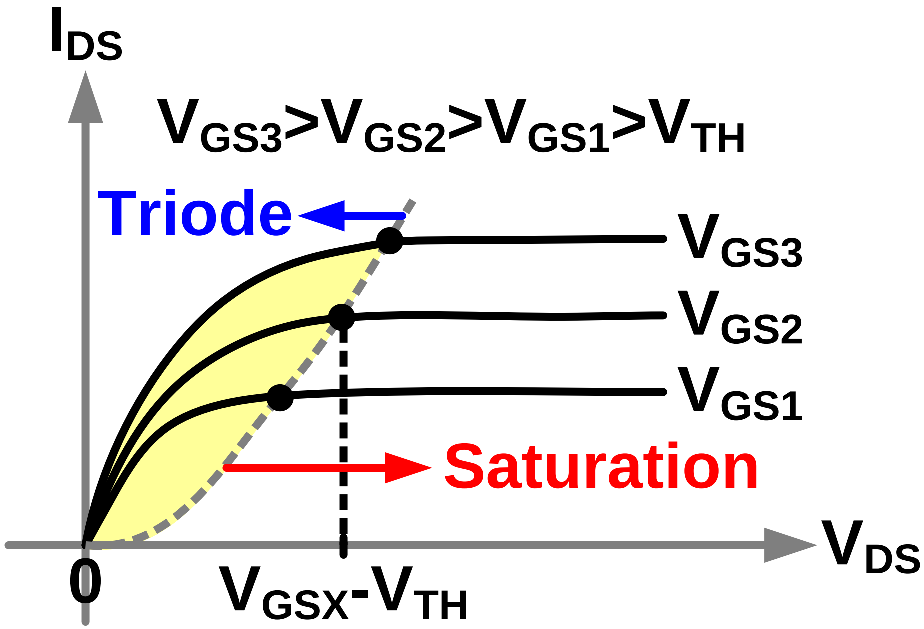
$$\mathbf{\int_0^L I_{DS}dx = W\mu_n C_{ox} \int_0^{V_{DS}} [V_{GS} - V(x) - V_{TH}]dV}$$

$$\mathbf{I_{DS} = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$

- During pinch-off, channel ceases to exist at drain
- At pinch-off point, V_{DS}=V_{GS}-V_{TH}

$$\mathbf{I_{DS,max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2}$$

NMOS I/V Characteristics



- For conduction, $V_{GS} > V_{TH}$
- In triode region, drain current is dependent on V_{DS}
- In saturation region, drain current is independent on V_{DS}

NMOS Regions of Operation

Cut-off

$$\mathbf{V_{GS} - V_{TH} < 0}$$

$$\mathbf{I_{DS} \approx 0}$$

Triode

$$\mathbf{V_{GS} - V_{TH} > 0 \text{ and } V_{GS} - V_{TH} > V_{DS}}$$

$$\mathbf{I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$

Saturation

$$\mathbf{V_{GS} - V_{TH} > 0 \text{ and } V_{GS} - V_{TH} < V_{DS}}$$

$$\mathbf{I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2}$$

Notation : $V_{GS} - V_{TH} = V_{OV}$ = Overdrive voltage