Analog Integrated Circuit Design

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Assignment 5

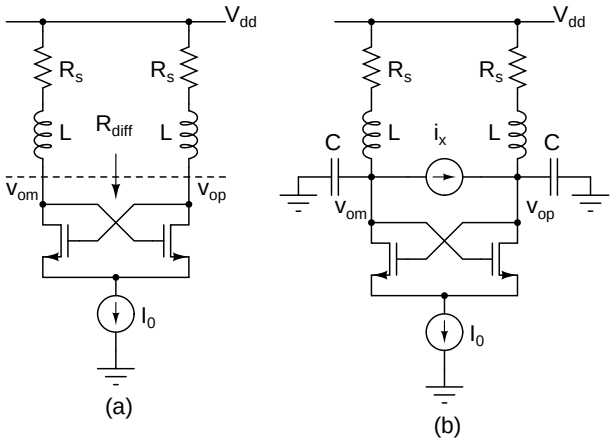

Figure 1: Problem 1

1. Calculate the current flowing in each transistor in Fig. 1(a) in the quiescent condition. Calculate the small signal differential resistance R_{out} looking into the drains of the two transistors.

   In Fig. 1(b), calculate $(v_{op} - v_{om})/i_x$. What is the condition for this to be infinity? What is the frequency at which this happens?

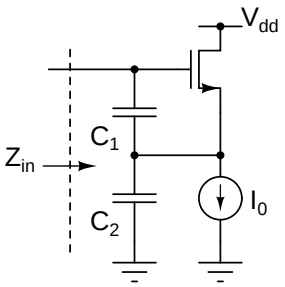

Figure 2: Problem 2

2. Calculate the input impedance Z_{in} in Fig. 2. Is there anything special about it? Model the transistor using only its g_m.

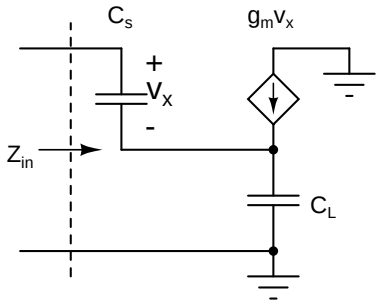

Figure 3: Problem 3

3. Calculate the input impedance $Z_{in}(s)$ in Fig. 3. Do you see anything special? What is the input impedance with $g_m = 0$?

   Express $Z_{in}(s)|_{g_m \neq 0}$ as a parallel combination of $Z_{in}(s)|_{g_m=0}$ and another branch $Z_1(s)$. What does $Z_1(s)$ consist of?

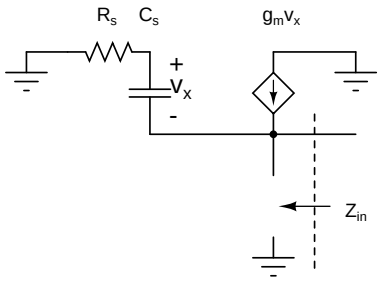

Figure 4: Problem 4

4. Calculate the input impedance $Z_{in}(s)$ in Fig. 4. Do you see anything special? Derive an equivalent circuit with passive elements that has an impedance Z_{in}.

5. Calculate the small signal impedance v_x/i_x. What is the condition for this to be infinity? What is the frequency at which this happens? Model the transistor

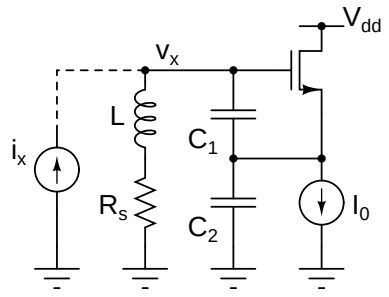

Figure 5: Problem 5

using only its g_m.

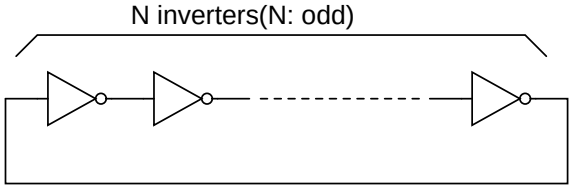

Figure 6: Problem 6

6. In Fig. 6, assume that all nodes are at the self bias voltage of the inverter. Model the small signal gain of each inverter as $A_0/(1+s/p_1)$ and calculate the condition for instability (i.e. when the loop gain becomes -1). Hint: Among the roots of -1, pick the one which satisfies the above for the lowest value of A_0.

7. What is the function of the circuits in Fig. 1(b), Fig. 5, and Fig. 6?

8. Fig. 7(a) shows a phase-locked loop which multiplies a 10 MHz reference up to 1 GHz. The charge pump details are shown in Fig. 7(b). $K_{VCO} = 100$ MHz/V; $I_{CP} = 100\mu$A; $R = 10\,\text{k}\Omega$; $C_1 = 10$ nF; $C_2 = 0$;

   Determine the loop bandwidth and the location of the loop-gain zero.

   Determine C_2 such that the phase margin is degraded by no more than 5° compared to the original. Determine the extra attenuation (in $\phi_{out}(s)/\phi_{ref}(s)$) at the reference frequency due to the addition of this value of C_2.

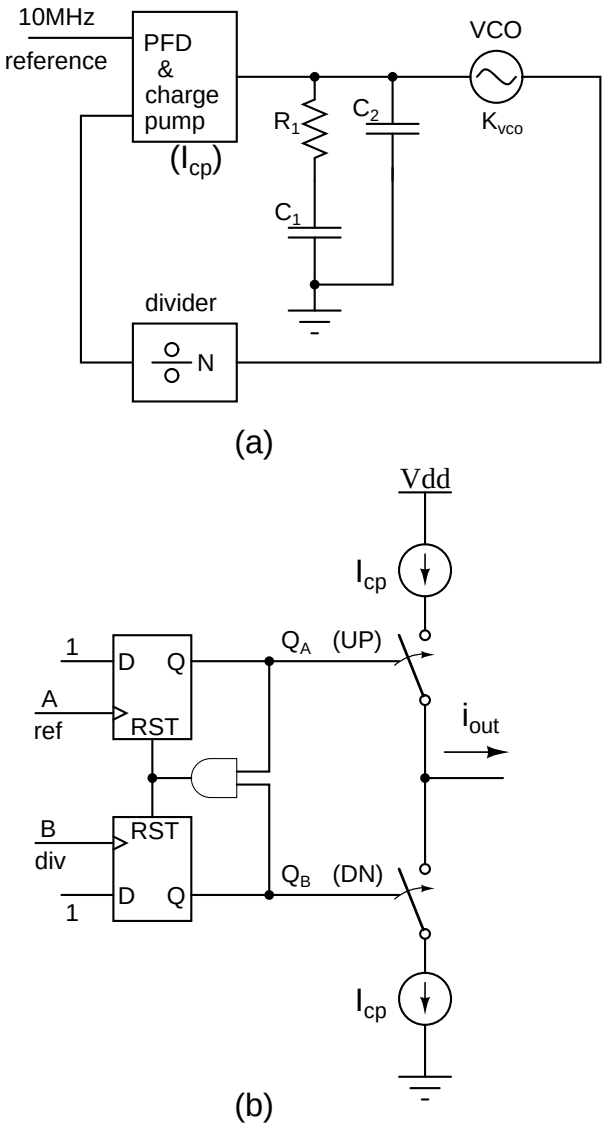

Figure 7: Problem 1