EE5320: Analog Integrated Circuit Design; Assignment 5

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 22 April 2015

Submit all solutions by email as a single pdf file; Present the solutions in the same order as the problems below.

$0.18\,\mu$m technology parameters: $V_{Tn} = 0.5$ V; $V_{Tp} = 0.5$ V; $K_n = 300\ \mu A/V^2$; $K_p = 75\ \mu A/V^2$; $A_{VT} = 3.5\,mV\ \mu$m; $A_\beta = 1\%\,\mu$m; $V_{dd} = 1.8$ V; $L_{min} = 0.18\ \mu$m, $W_{min} = 0.24\ \mu$m; Ignore body effect unless mentioned otherwise. (These for estimates by hand calculations. This assignment requires simulation results with real MOS models).

For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$ in simulations.

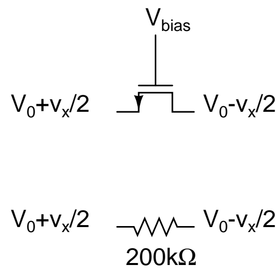

Figure 1:

1. (For this problem, The minimum usable dimension is $0.3\,\mu$m.) A MOSFET is used as a $200\,k\Omega$ resistor (Fig. 1) $V_0 = 0.5\,V$ and v_x is restricted to 0.25 V. The nonlinear part of the current (Difference between the actual current in the resistor and its linear approximation) in the resistor should be at most 5%.

   Simulate the MOS transistor with differential inputs as shown in the figure and adjust the gate bias V_{bias} and the dimensions of the transistor to obtain the above resistance with the required linearity.

   If a linear resistive material with a sheet resistance of $10\,\Omega$/sq. is available, what would be its dimensions? What is the motivation for using a transistor instead of a resistive material?

2. Design a 2 pF capacitor using A square nMOS device (drain/source shorted). Plot its capacitance as a function of voltage (0 to 1.8 V). What is the usable voltage range of this capacitor? (For this problem use the process information given in the cadinfo page).

   Repeat the above for a square pMOS device.

   A square Metal1-Metal2 structure.

   A square sandwiched structure with poly, M2, M4 tied together and M1, M3, M5 tied together.

   For the last two structures, determine the bottom plate parasitic capacitance.

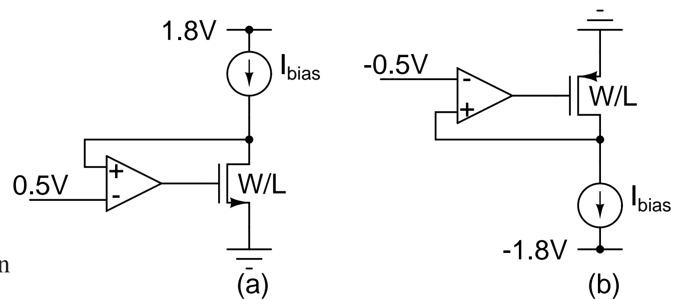

Figure 2:

3. This exercise is intended to give you an idea of where to bias your transistors to get the desired g_m, dc gain, transit frequency (f_T, which gives you an estimate of the intrinsic speed of the device).

   Fig. 2(a) shows an nMOS transistor biased at I_{bias} with an opamp to set the V_{DS} precisely. Fig. 2(b) shows the exact same circuit with pMOS. Use an

ideal VCVS of gain 100 in your simulations. Use $W = 10\,\mu$m. Pick the transistor as given below (you have to repeat the simulations with the two length values given).

Roll no.	Transistor	Lengths
4N	pMOS	$L = 0.18\,\mu\text{m},\ 0.36\,\mu\text{m}$
4N+1	pMOS	$L = 0.18\,\mu\text{m},\ 0.72\,\mu\text{m}$
4N+2	nMOS	$L = 0.18\,\mu\text{m},\ 0.36\,\mu\text{m}$
4N+3	nMOS	$L = 0.18\,\mu\text{m},\ 0.72\,\mu\text{m}$

(integer N of course!)

Vary I_{bias} from a small value (say 10 μA) to a value that drives the transistors to the edge of saturation (as V_{GS} increases). At each value, do a dc operating point analysis (this can be done conveniently with sweep or equivalent commands without having to manually carry out the simulations). Print the operating point of the MOS transistor. Plot the following versus *current density* (I_{bias}/W).

- Transconductance per unit width g_m/W
- Transit frequency $f_T = g_m/2\pi C_{gs}$ (C_{gs} is reported as `cgg` in simulators).
- Intrinsic dc gain g_m/g_{ds}
- V_{DSAT} of the transistor as reported by the simulator

4. Plot (log-log) I_D vs. V_{GS} (18 mV to 1.8 V) for $V_{DS} = 1$ V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment (very briefly) on the results. Calculate the subthreshold slope η. The current in a MOS transistor in the subthreshold region is proportional to $\exp(V_{GS}/\eta V_t)$ where $V_t = kT/q$ is the thermal voltage.

5. Plot (log-log) I_D vs. V_{BS} (-1.5 V to -15 mV) for $V_{DS} = 1$ V and $V_{GS} = 1$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment (very briefly) on the results.

(Don't submit the following, but you can do them to further your understanding)

1. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{GS} from 0 to 1.5 V in steps of 0.25 V and $V_{BS} = 0$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment on the results.

2. Plot I_D vs. V_{DS} (0 to 1.8 V) for V_{BS} from -1 V to 0 V in steps of 0.25 V and $V_{GS} = 1.5$ V. Overlay the plots for $W/L = 3.6\,\mu\text{m}/0.36\,\mu\text{m}$ and $W/L = 36\,\mu\text{m}/3.6\,\mu\text{m}$. Comment on the results.

3. Repeat the simulation of MOS characteristics (last 5 problems above) at temperatures of $\{0, 27, 100\}^\circ$ C. What do you observe?