EE5320: Analog Integrated Circuit Design; Assignment 4

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 7 April 2015

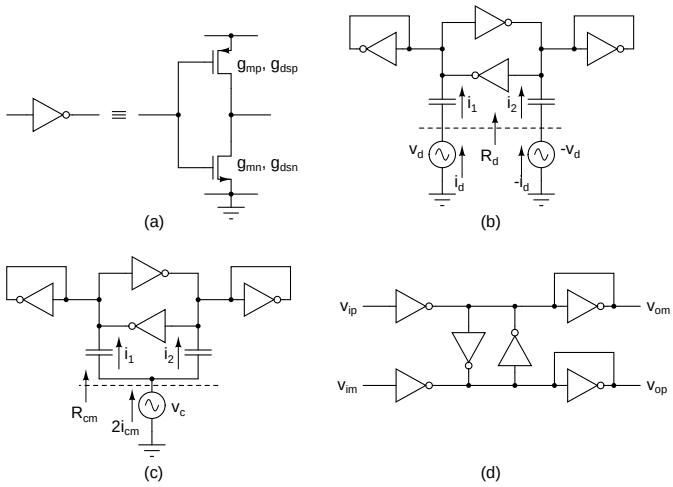

Figure 1: Problem 1

1. All inverters in Fig. 1 are identical and shown in Fig. 1(a). Model each transistor by its g_m and g_{ds} as shown. Answer the following:

   - Fig. 1(b, c) show a circuit driven by out of phase and in phase (small) signals. Calculate(symbolically) the small signal currents i_1 and i_2 in in the two cases. Comment on the magnitude of the currents in the two cases.
   - Determine $R_{cm} = v_c/i_{cm}$ and $R_d = 2v_d/i_d$ in Fig. 1(b, c).
   - Determine the common mode rejection ratio in Fig. 1(d). $A_d = (v_{op} - v_{om})/(v_{ip} - v_{im})$ and $A_{cm} = (v_{op} + v_{om})/(v_{ip} + v_{im})$.
   - If a single ended input is applied ($v_{ip} = v_i$, $v_{im} = 0$), calculate the output differential and common mode components.

2. The common mode gain of a differential amplifier is measured by applying a small signal common mode input v_{cm} as shown in Fig. 2. Fig. 2(a) has a current mirror load and Fig. 2(b) has a current source load which is independently biased. What is the common mode gain of these two configurations? Express the answer in terms of the small signal parameters of: M_0 (g_{m0}, g_{ds0}), $M_{1,2}$ (g_{m0}, $g_{ds1} = \infty$), $M_{3,4}$ (g_{m3}, g_{ds3})

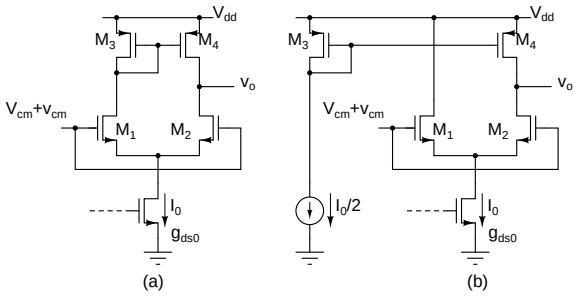

Figure 2: Problem 2

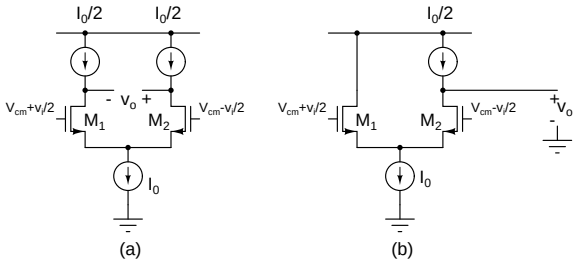

Figure 3: Problem 3

3. Determine the small signal dc gains of the two amplifiers in Fig. 3. The transistors can be modeled using g_m and g_{ds}. Explain the results.

4. Calculate the small signal tail node voltage v_x in Fig. 4. v_i is a small signal increment. The transistors can be modeled using g_m and g_{ds}.

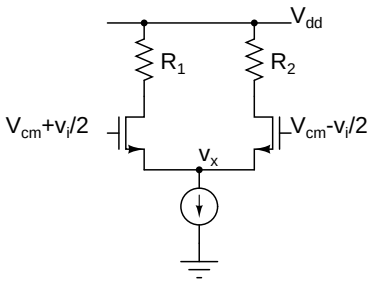

Figure 4: Problem 4

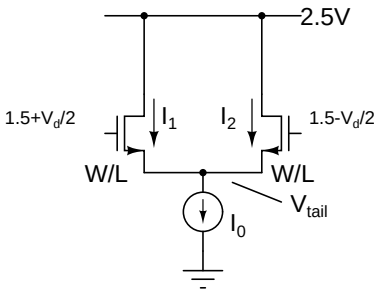

Figure 5: Problem 5

5. Assuming square law models without body effect, calculate and sketch the *large signal* I_1 and I_2 (on the same graph) versus V_d, and *large signal* V_{tail} versus V_d. Mark the axes cleanly with the correct numerical values. What is the differential input voltage at which all of the tail current is switched to one transistor? What whould be this voltage if the transistor behaved as a linear VCCS with the transconductance value at the quiescent point? Use the numerical values given below.

Roll. no.	W/L	I_0 (μA)
$4n$	10	60
$4n+1$	8	75
$4n+2$	10	135
$4n+3$	20	480

6. Determine the loop gain $L_{cm}(s)$ of the common mode feedback loop in the fingle-stage fully differential opamp shown in Fig. 6(a). The relevant capacitors are shown on the figure. To do this, draw the common mode half circuit, identify the common mode feedback loop, break it at an appropriate point, and calculate the loop gain. Sketch the magnitude and phase assuming that R_{cm} is large (as you would choose to maximize the differential gain) and $C_L > C_{gs3}$. e.g. say $R_{cm} \sim 100/g_{m3}$ and $C_L \sim 10C_{gs3}$. $g_{ds} = 0$ for all transistors. Comment on the stability of the loop.

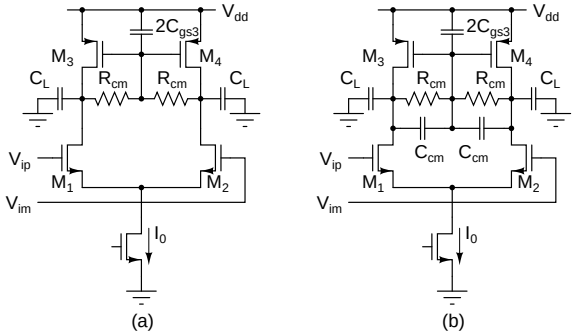

Figure 6: Problem 6

7. A suggestion is made to add C_{cm} in parallel with R_{cm} to improve the stability characteristics. Again, determine the loop gain function and sketch the loop gain. What would be a good choice for C_{cm}?