EE5320: Analog Integrated Circuit Design; Assignment 3

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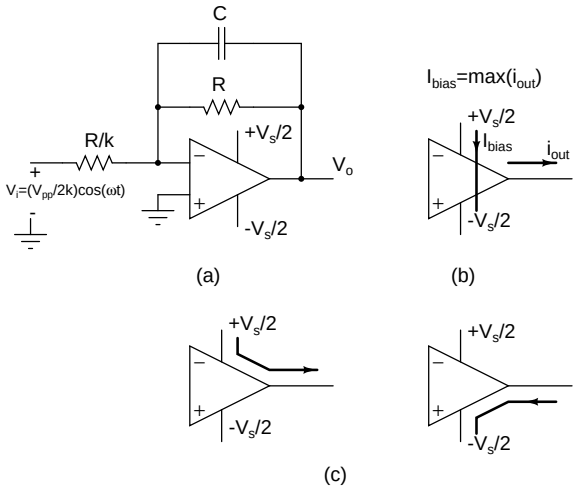

Figure 1:

1. Determine the rms signal, rms noise, signal to noise ratio (as a ratio of mean squared quantities) at the output of Fig. 1. Assume an low frequency input. What is the amplifier's transfer function? The opamp can be either (i) class A (Fig. 1(b)): In this case a constant current I_{bias}, equal to the highest possible output current) is drawn from the amplifier; or (ii) class B (Fig. 1(c)): In this case, currents out of the opamp are drawn from the positive supply and currents into the opamp are pushed into the negative supply. In each case, calculate the power dissipation. Relate the power dissipation to amplifier specifications: gain, bandwidth, and signal to noise ratio.

2. Determine the output current in Fig. 2. Determine the output noise current in terms of small signal parameters of M_3 and M_4. Which of the devices primarily contribute to the noise? Determine the output current error due to current factor and threshold mismatches ($\Delta\beta_{13}, \Delta V_{T13}$ between M_1 and M_3, and $\Delta\beta_{24}, \Delta V_{T24}$ between M_2 and M_4). Which of the mismatches is more critical?

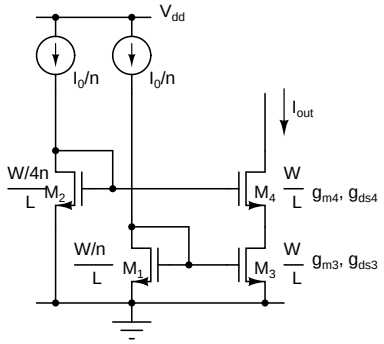

Figure 2:

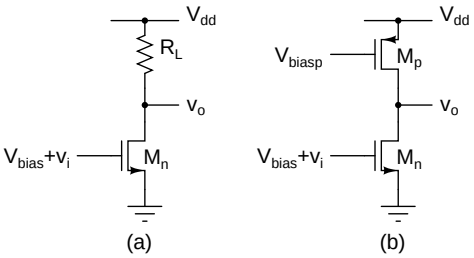

Figure 3: Problem 4

3. Fig. 3 shows two common source amplifiers designed for the same small signal gain. Determine the output noise of the two amplifiers in terms of the small signal parameters of M_p and M_n and comment on the results. Assume that the transistors are biased correctly in saturation region.

4. Fig. 4 shows a single-stage opamp which is driven by a common mode increment v_{cm} in addition a differential increment v_d. Determine the incremental output v_o. Assume that M_0, $M_{1,2}$, and $M_{3,4}$ have small signal parameters of g_{m0}, g_{ds0}, g_{m1}, g_{ds1},

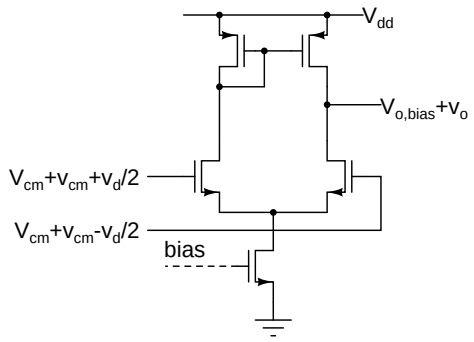

Figure 4: Problem 5

and g_{m3}, g_{ds3} respectively. Determine the common mode rejection ratio A_d/A_{cm} where $A_d = v_o/v_d$ and $A_{cm} = v_o/v_{cm}$.

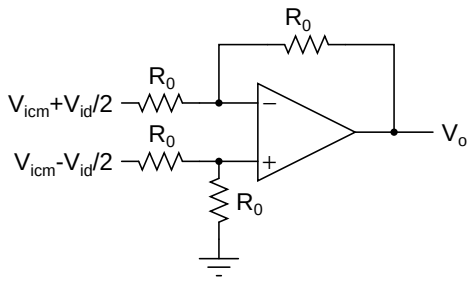

Figure 5: Problem 6

5. Fig. 5 shows a possible arrangement for converting differential signal to single ended signal. One of the applications of such a circuit is to determine small differences between two large voltages. For our application let us assume that a 10 mV difference around an input common mode voltage of 10 V (i.e. the inputs to the circuit are $10\,\mathrm{V} \pm 5\,\mathrm{mV}$) has to be determined "correctly". For the following, first find the outputs in general terms (input common mode and differential voltages of V_{icm} and V_{id}) and then calculate the numerical answers.

   - Determine the output voltage V_o with an ideal opamp
   - Determine the output voltage V_o when the opamp has a differential gain A_d and a common mode gain A_{cm}.
   - What is the common mode rejection ratio A_d/A_{cm} required such that the output error due to non-zero common mode gain is 10% of the ideal output value when the inputs are $10\,\mathrm{V} \pm 5\,\mathrm{mV}$.
   - Determine the output voltage V_o with an ideal opamp when the resistors have a relative mismatch standard deviation of $\sigma_R = \sigma(\Delta R/R_o)$ where R_o is the ideal value.
   - What is σ_R such that the standard deviation of the output voltage is 5% of the ideal output value when the inputs are $10\,\mathrm{V} \pm 5\,\mathrm{mV}$.

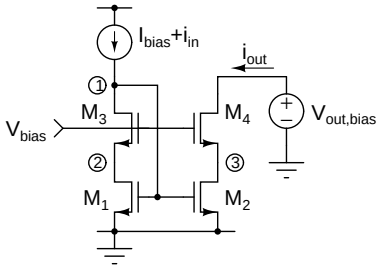

Figure 6:

6. In Fig. 6, determine the transfer function $I_{out}(s)/I_{in}(s)$ when a parasitic capacitor C_p is present from node 1, 2, or 3 to ground (only one at a time). V_{bias} and $V_{out,bias}$ are such that all transistors are in saturation.

   (not for credit, just to be tried out): Include parasitic capacitors at all three nodes and evaluate the frequency response $I_{out}(s)/I_{in}(s)$. Comment.