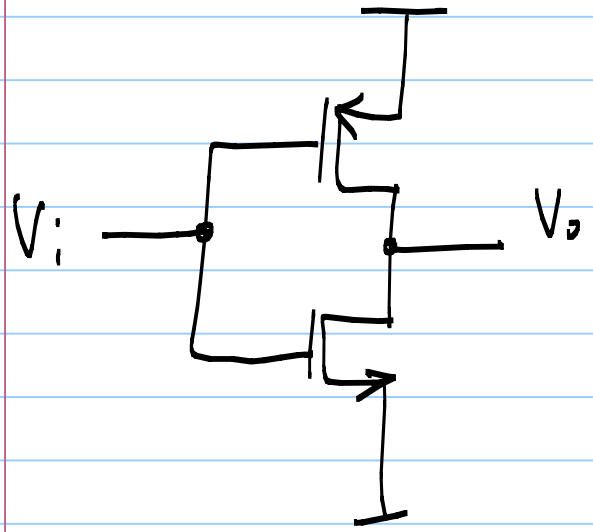
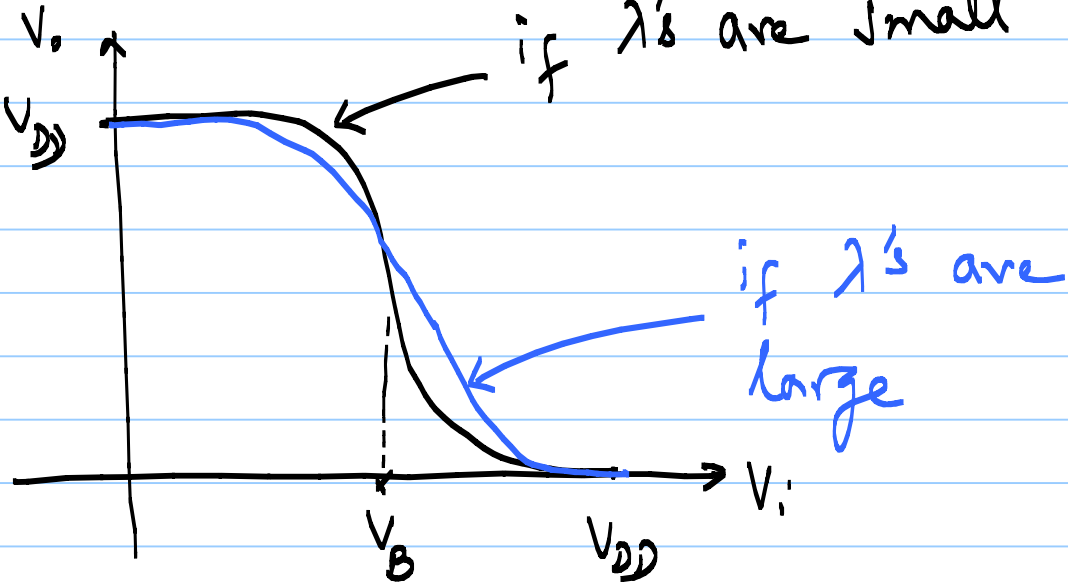
23|9|2020

Lecture 29

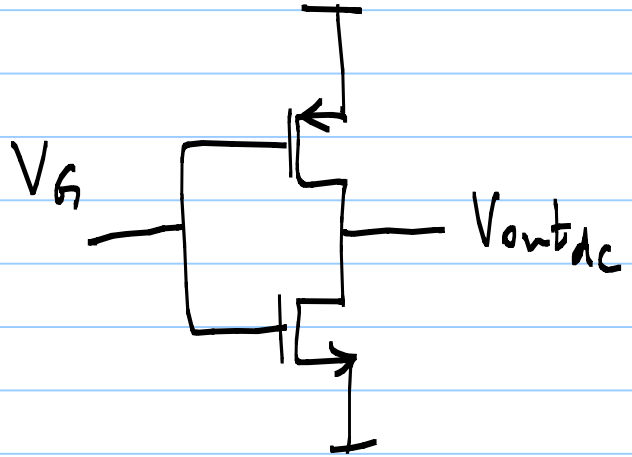


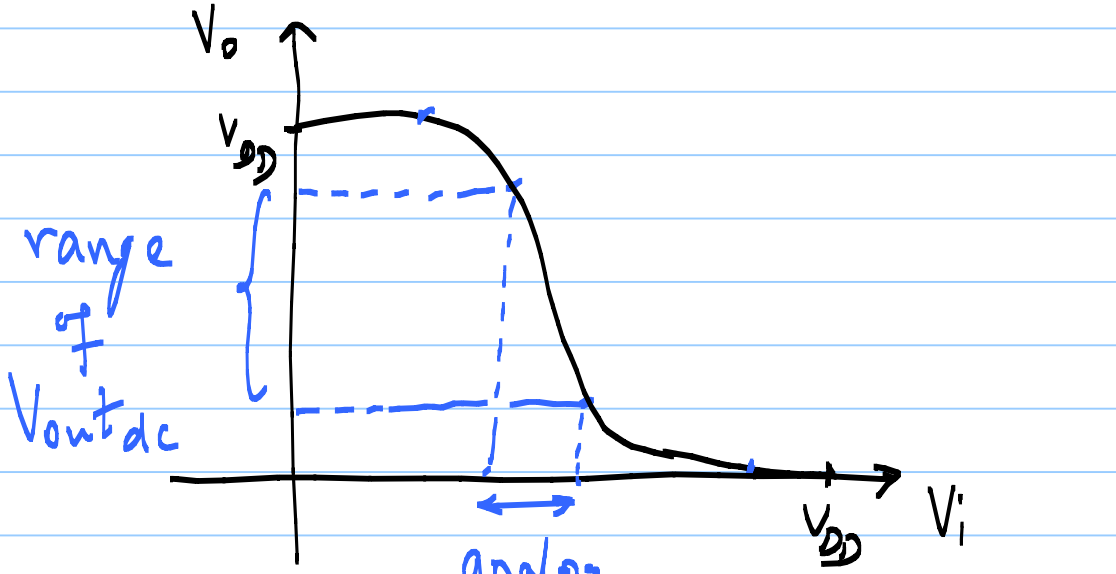


Small signal gain $\frac{v_o}{v_i} = \frac{-(g_{m_1} + g_{m_2})}{g_{ds_1} + g_{ds_2}}$

$= -(g_{m_1} + g_{m_2})(r_{ds_1} \| r_{ds_2})$

Biasing of CMOS inv.





* Assume $V_B \sim V_{DD}/2$

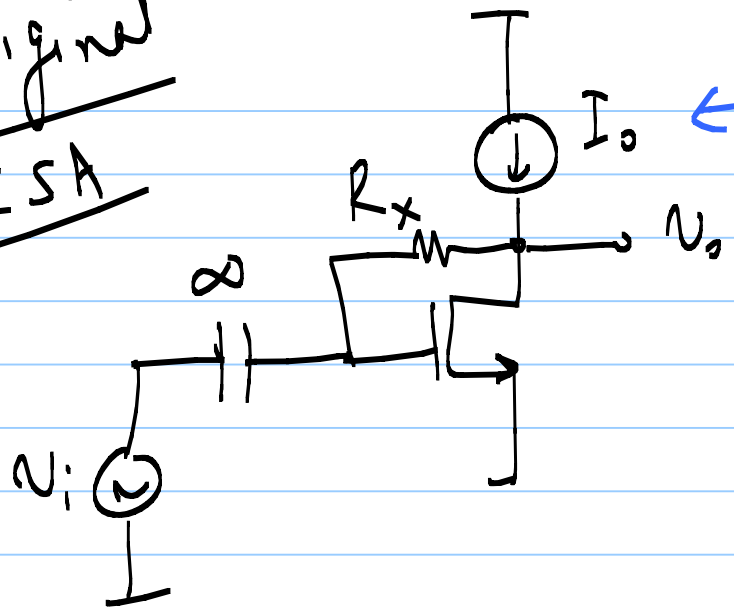
i.e. PMOS ~ NMOS except for $\mu_p \sim 3\mu_n$

$$\left(\frac{W}{L}\right)_p \sim 3\left(\frac{W}{L}\right)_n$$

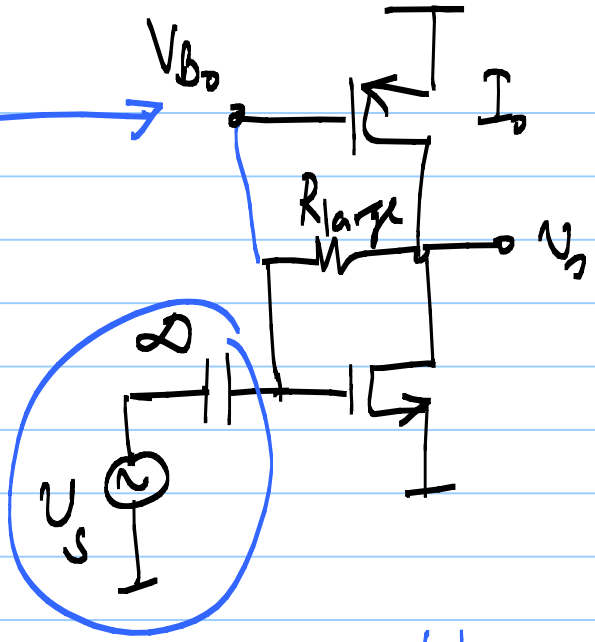
* Negative f.b. biasing

→ Drain to Gate f.b. using a current source & resistor

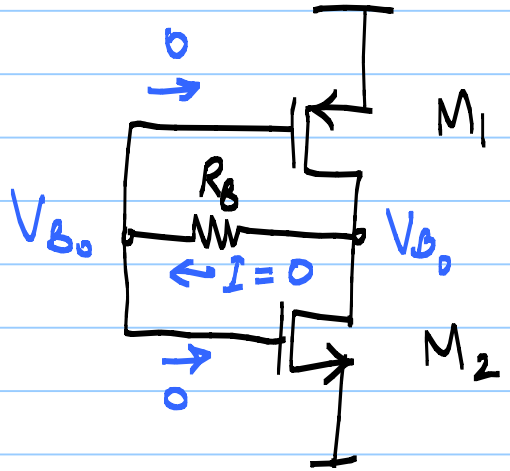
Original CSA

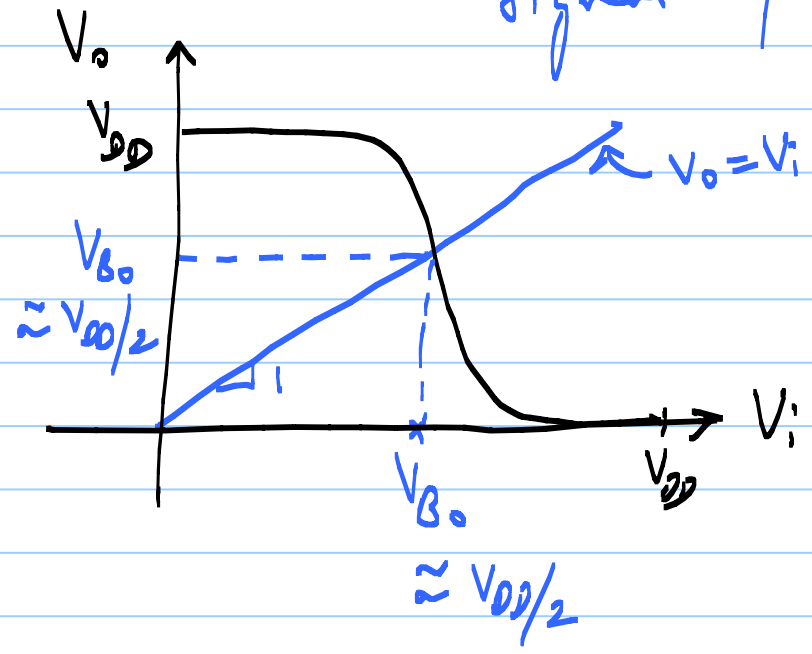


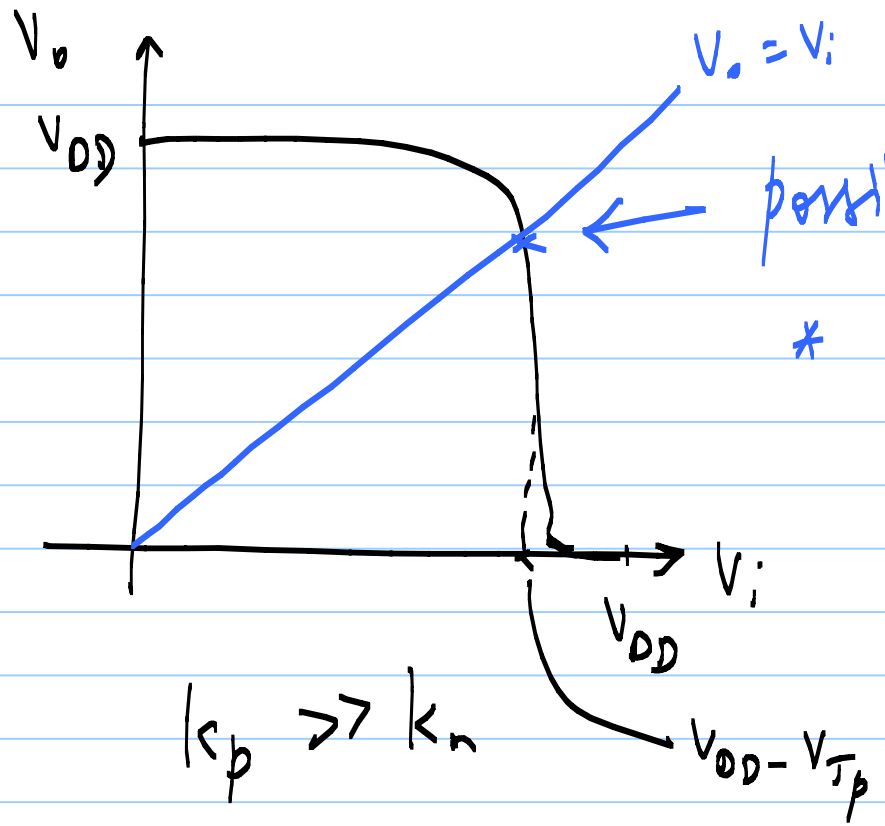
← get gain from this device →



signal portion



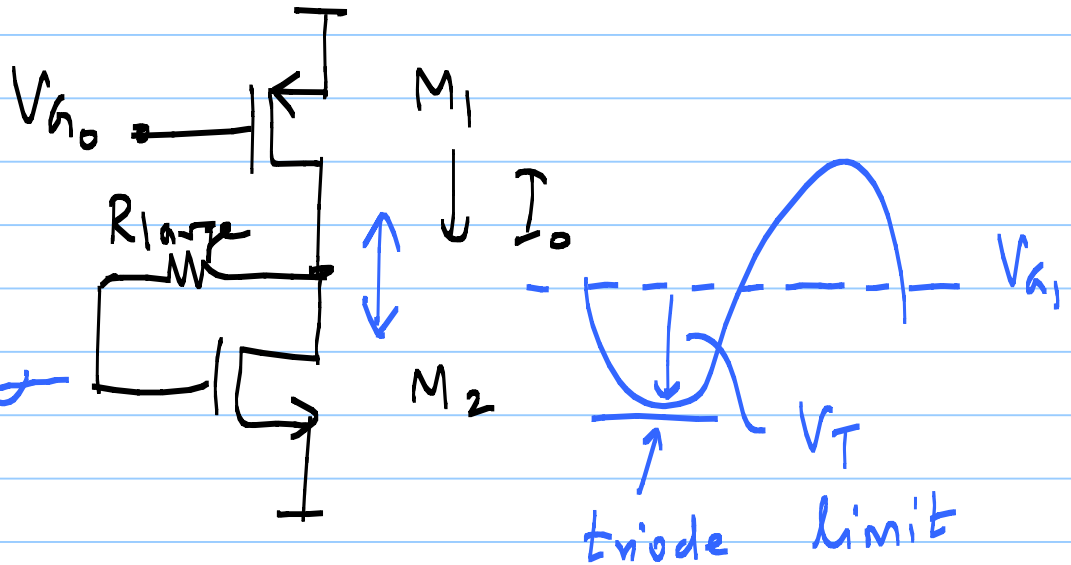




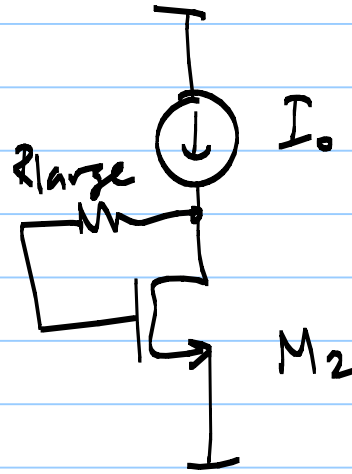
close to

possible to end up in region (D)

* any small voltage swing will push PMOS into triode



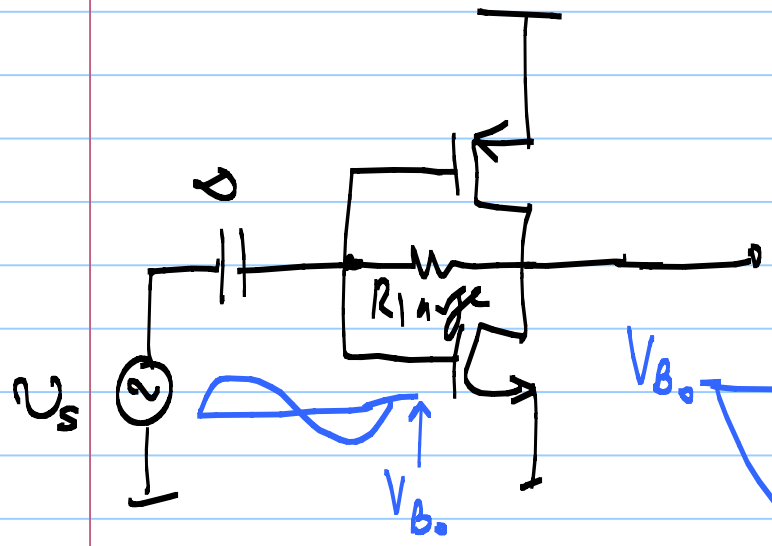
$\equiv$

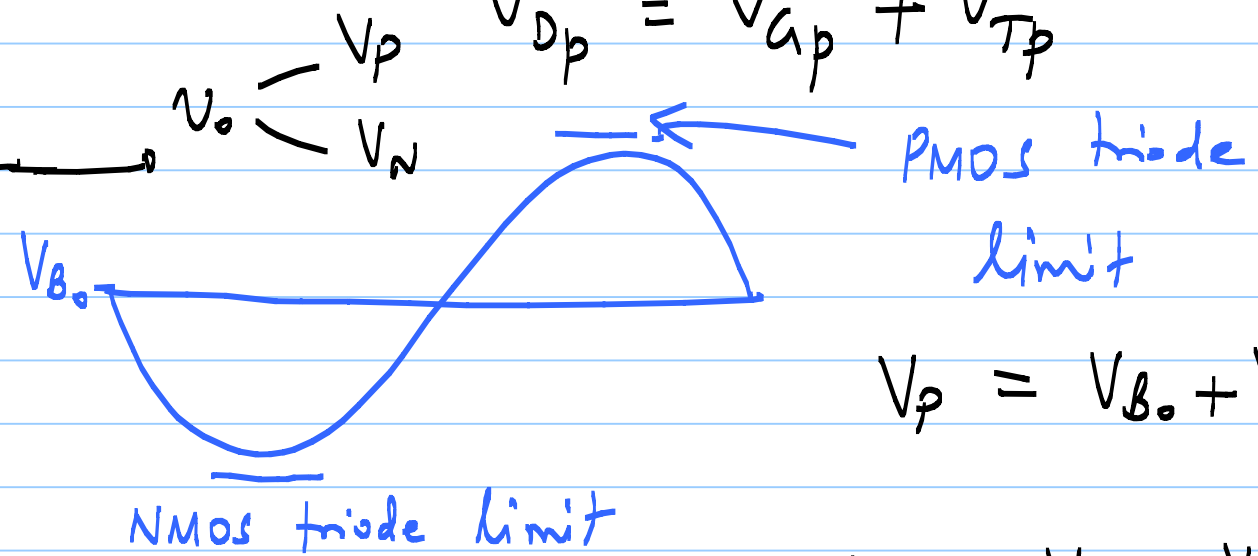


HW

swing limit calc.

Swing limits of CMOS Inv.





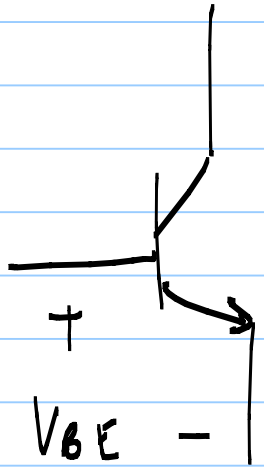
PMOS triode limit:

$$V_{DP} = V_{GP} + V_{TP}$$

$$V_P = V_{B_0} + V_{TP}$$

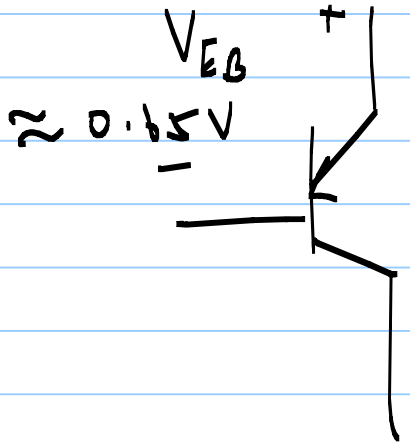
$$V_{DN} = V_{GN} - V_{TN} \Rightarrow V_N = V_{B_0} - V_{TN}$$

HW – accurate swing limit calculation for inv.



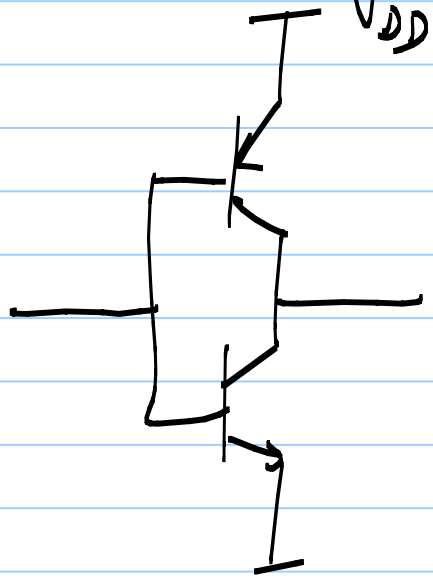
$\approx 0.65V$

npn BJT



$\approx 0.65V$

pnp BJT



$V_{DD} \approx V_{BE_n} + V_{EB_p} \approx 1.3V$