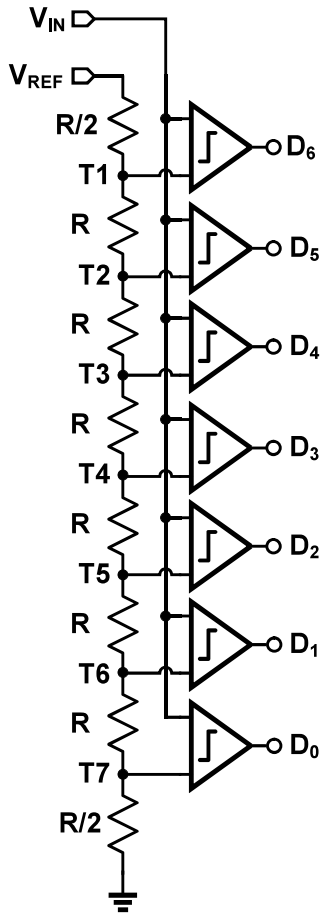


Problem Set # 8

Question-1

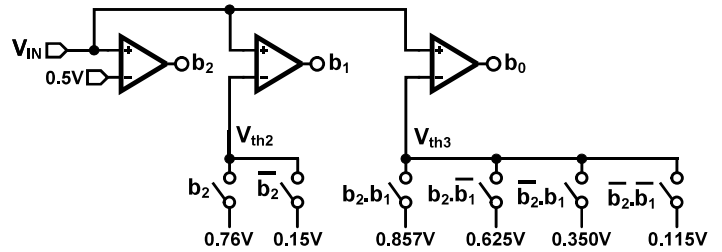
Consider a 3-bit flash ADC shown below. The comparators are ideal. Bits D_0, \dots, D_6 are combined to give a digital output, D . Outputs of comparators are 0 or 1. $V_{REF} = 1V$ and $V_{IN} = 0.37V$.

- Find the digital output for the given input.
- Sketch the digital output versus input voltage ($[0, 1V]$) for the flash ADC.
- Sketch the DNL profile of the ADC.
- Let T1 and T2 be shorted, T3 and T5 be shorted, and T6 and T7 be shorted together. Sketch the digital output versus input voltage ($[0, 1V]$) for the new flash ADC with shorted input reference voltage nodes.
- Find the digital output for input $V_{IN} = 0.37V$ with ADC described in (d).



Question-2

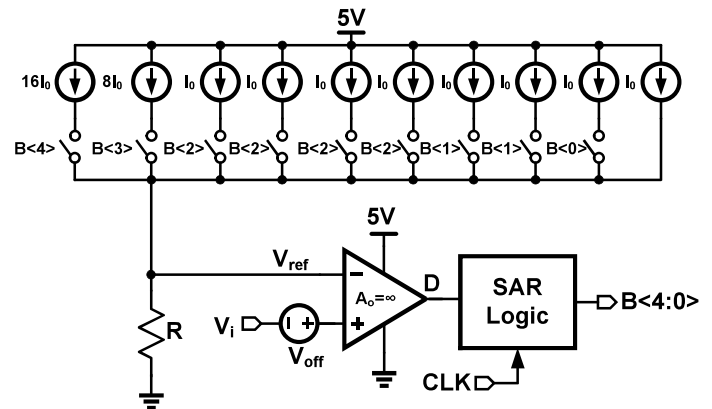
A 3-step flash ADC is shown below. Comparator outputs $b_{1,2,3}$ are 1 or 0. Switches are ideal with zero resistance for control voltage 1V. Switches are open with control voltage 0V.



- Find ADC's output ($b_2 b_1 b_0$) if V_{IN} is 0.715 V.
- Find comparator threshold voltages V_{th2} and V_{th3} .

Question-3

In the circuit shown below, switched current sources are used with a resistor R to generate the reference voltage V_{ref} for comparison. The switches are ideal with zero ON resistance when control signal is high. The switch is turned OFF when control signal as 0V. The comparator has an input referred offset voltage V_{off} . V_i is the sampled input available for comparison. SAR logic is clocked using clock signal, CLK with time period T . SAR's outputs i.e., $B_{<4:0>}$ change every clock (CLK) period. Let $B_{<4:0>}$ has 5V has high voltage and 0V as low voltage. Also, $I_0 = 31.25\mu A$ and $R = 1k\Omega$. Let $D=0$ and $B_{<4:0>}=0$ at $t=0$.



- If $V_i = 0.743V$ and $V_{off} = 0V$, find D and $B_{<4:0>}$ every clock period till a final digital equivalent is found for the input.
- If $V_i = 0.743V$ and $V_{off} = -31.25\mu V$, suggest a method to generate a correct digital equivalent of the analog input with available components in the circuit and without adding any extra circuit components.