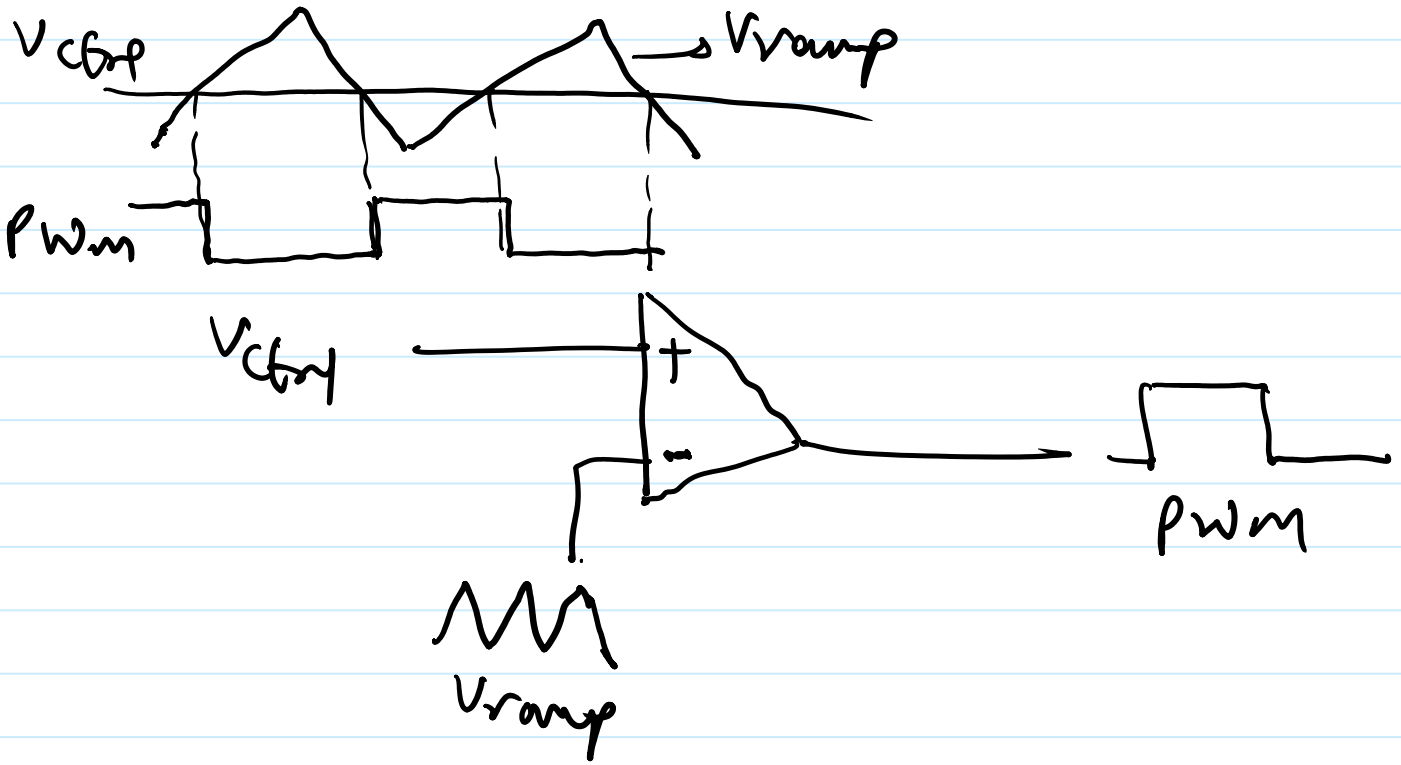
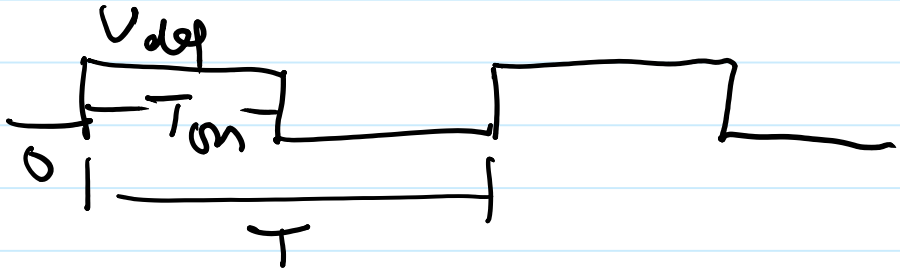
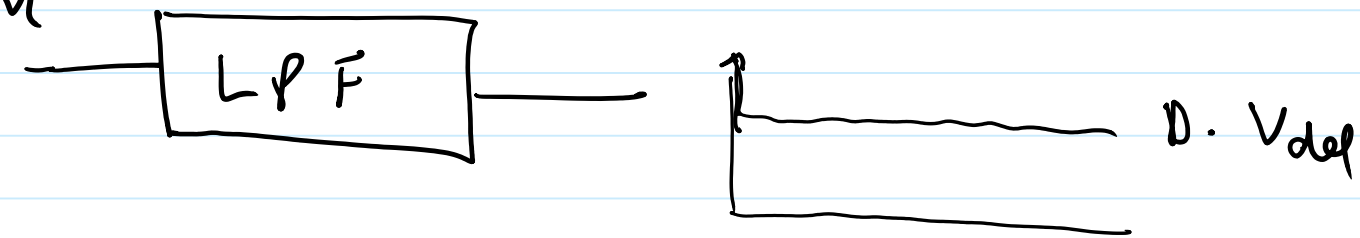
PWM Signal

PWM → Pulse Width Modulation





PWM



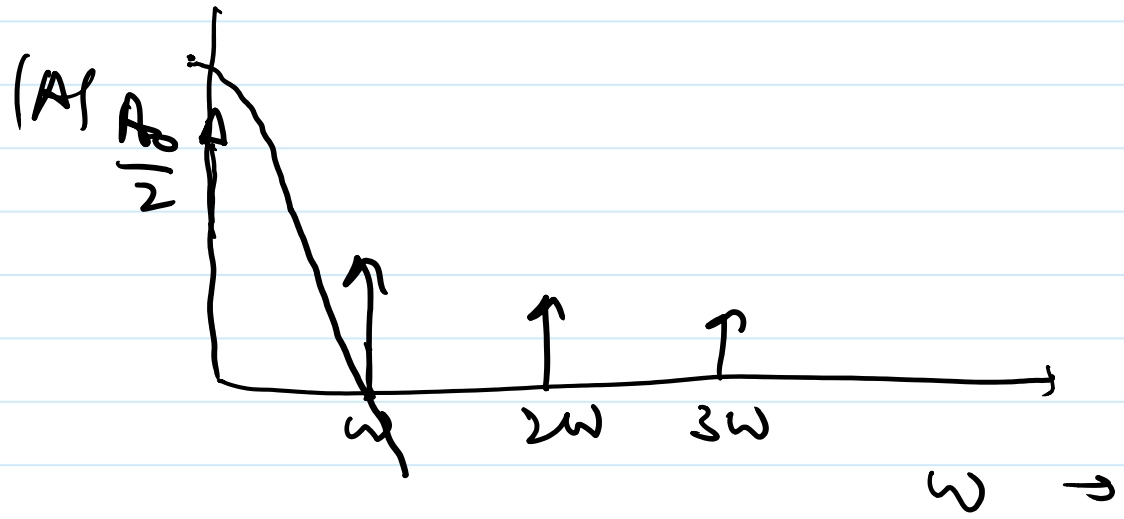
$$D = \frac{T_{on}}{T} = \text{Duty cycle}$$

Fourier Series

$$\frac{A_0}{2} + \sum_{n=1}^{\infty} \left[a_n \cos n\omega t + b_n \sin n\omega t \right]$$

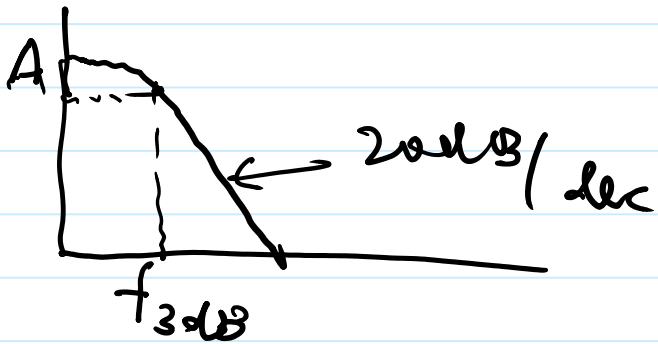
$\frac{A_0}{2}$ → dc component

$\sum_{n=1}^{\infty} \left[a_n \cos n\omega t + b_n \sin n\omega t \right]$ → AC component

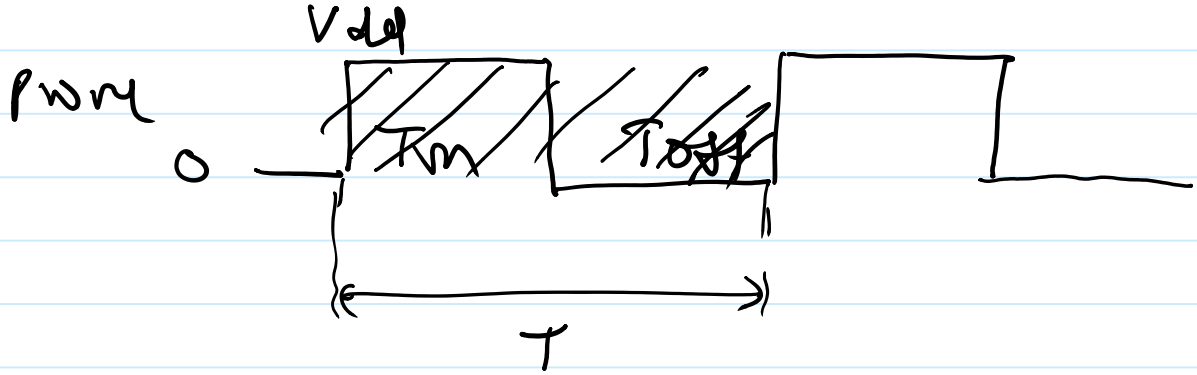


if T is period of PWM

Then LPF BW should be $<< \frac{1}{T}$



$f_{3db} << \frac{1}{T}$

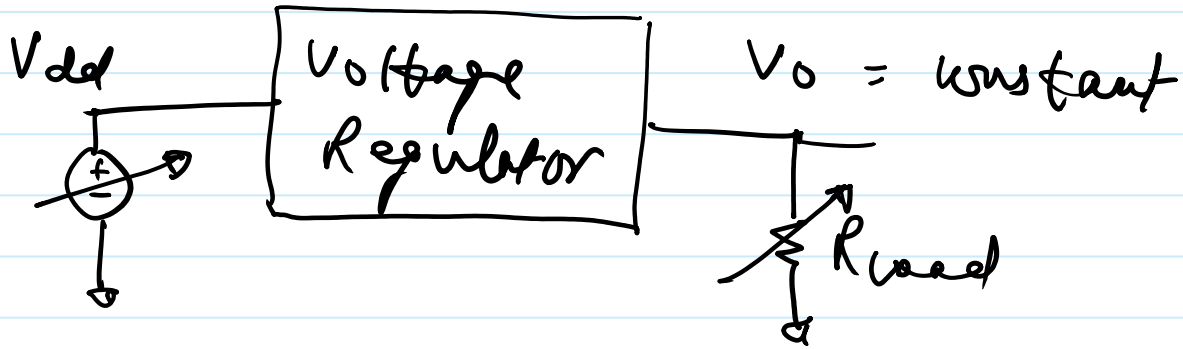


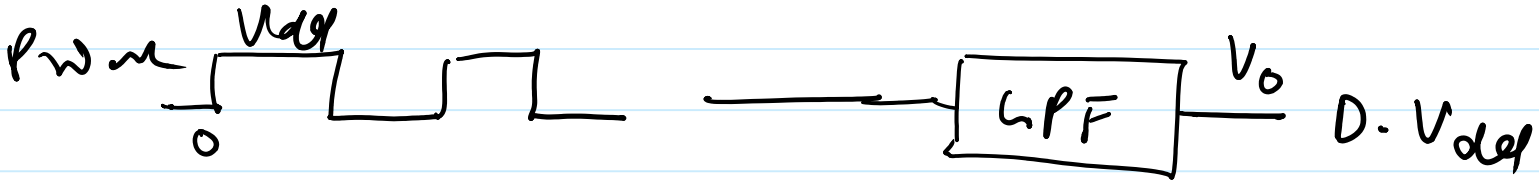
$$Avg(PWM) = \frac{1}{T}\int_0^T f(t)\,dt$$

$$= \frac{1}{T} \times V_{dd} \times T_{on}$$

$$= \frac{T_{on}}{T} V_{dd} = D \cdot V_{dd}$$

PWM is used to implement voltage regulator





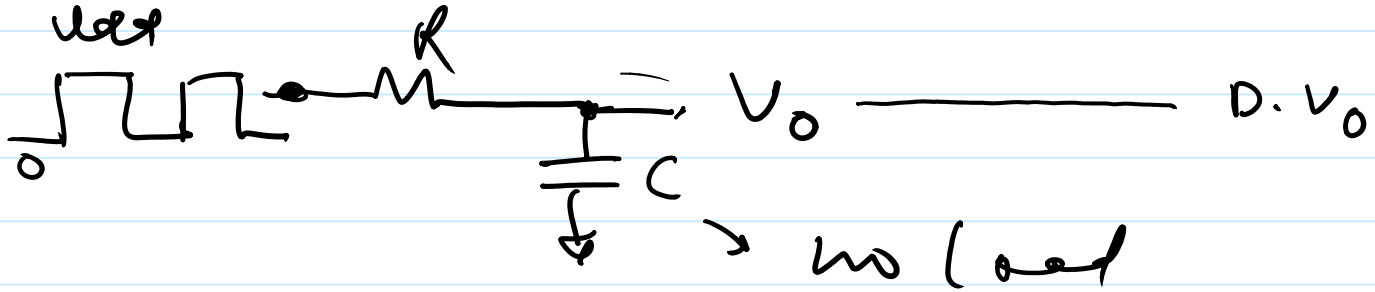
$V_{dd} = 5\,V$, $V_o = 2.5\,V$

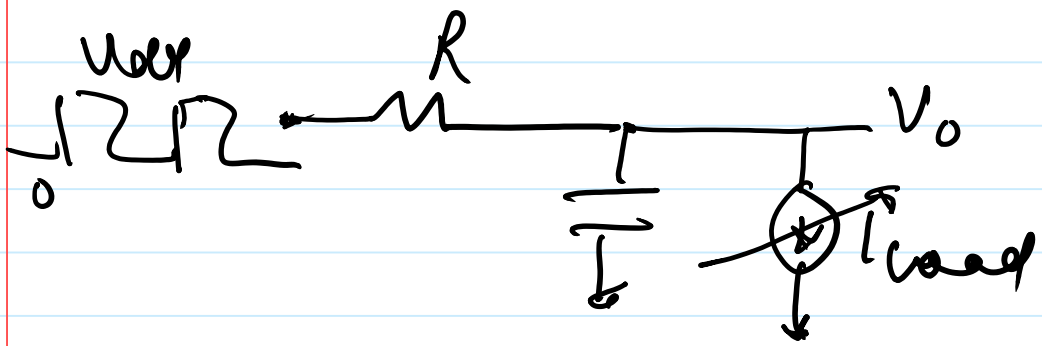
$V_o = D \cdot V_{dd} \Rightarrow D = \frac{V_o}{V_{dd}} = \frac{2.5}{5} = 0.5$

$V_{dd} = 10\,V$

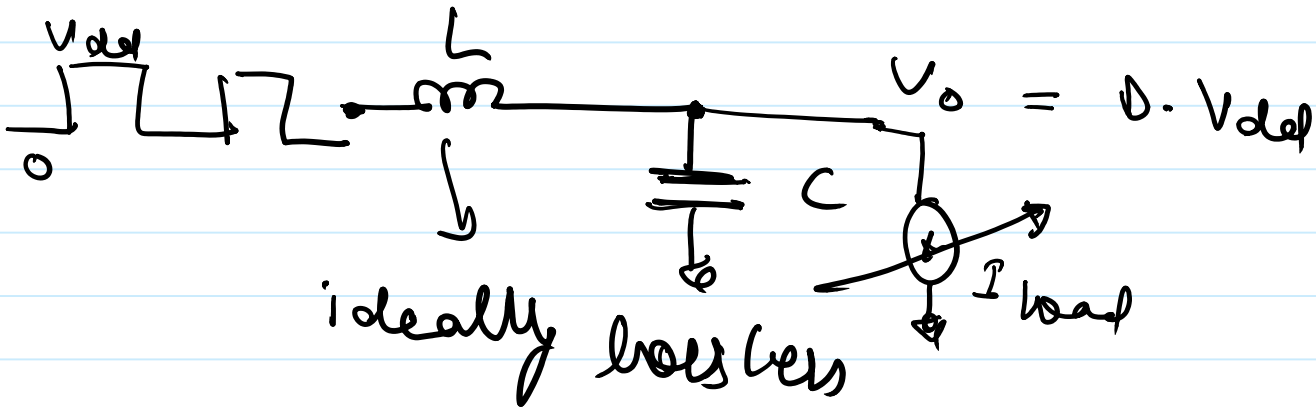
$D = \frac{2.5}{10} = 0.25$

which means under varying V_{dd} we need to vary D to keep V_o constant

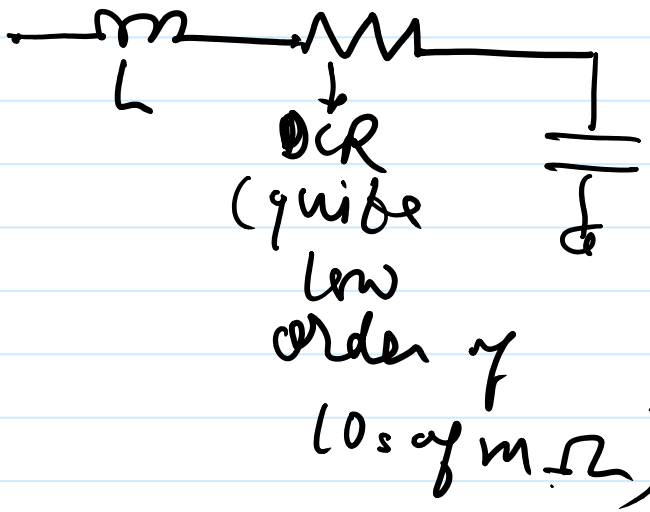


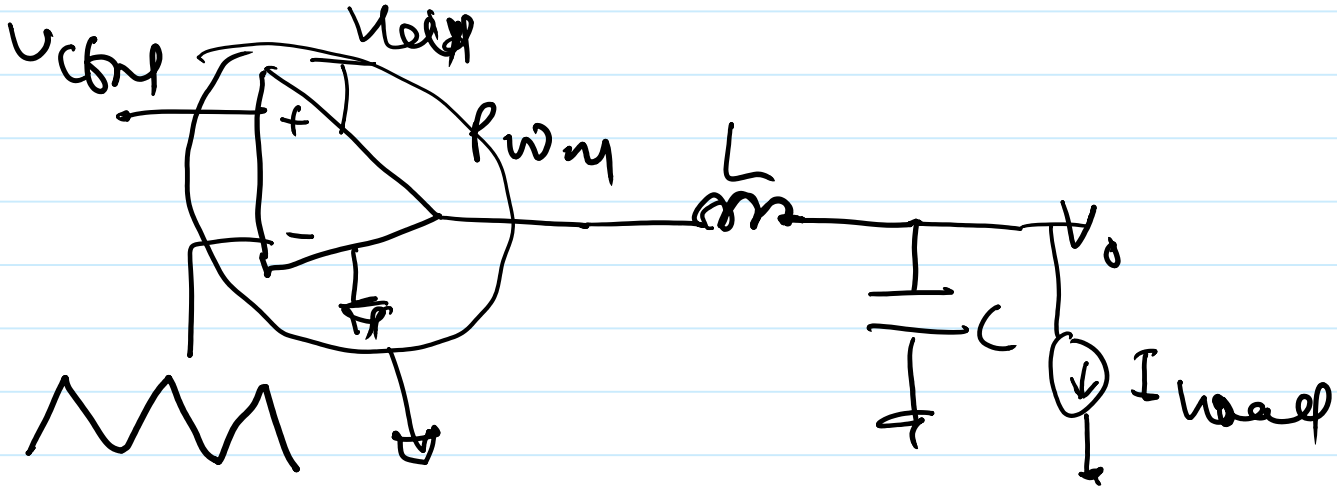


we can't use RC filter for regulator due to IR drop

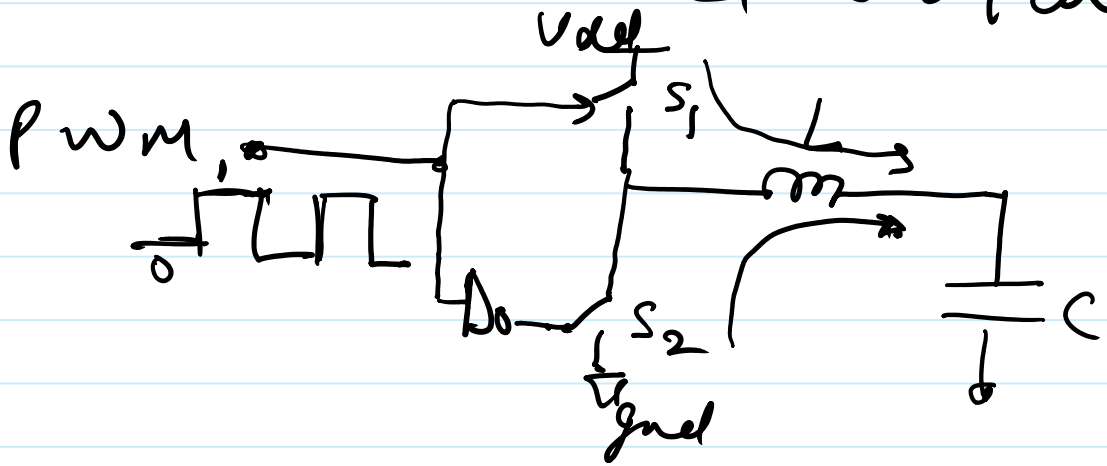

V_{dd}
L
$V_o = D \cdot V_{dd}$
C
I_{load}
ideally lossless

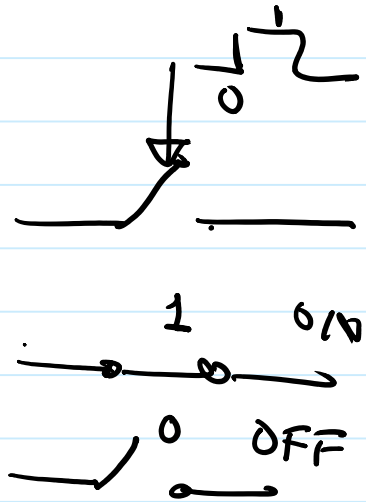
$V_o = D \cdot V_{dd}$

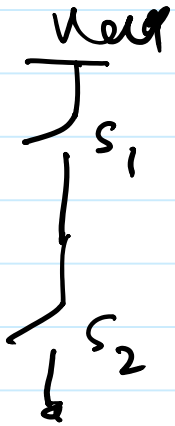

L
DCR
(quite
low
order of
10s of mΩ)



comparator
can't drive large current
so we need switches



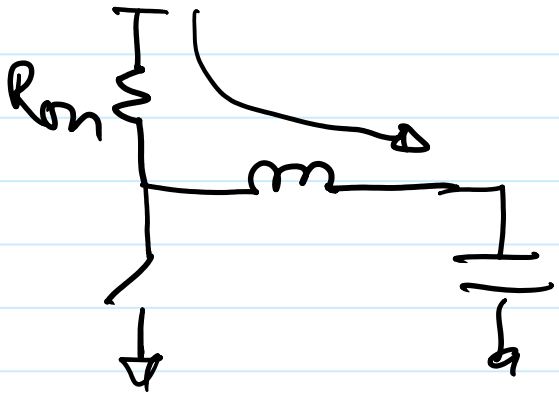




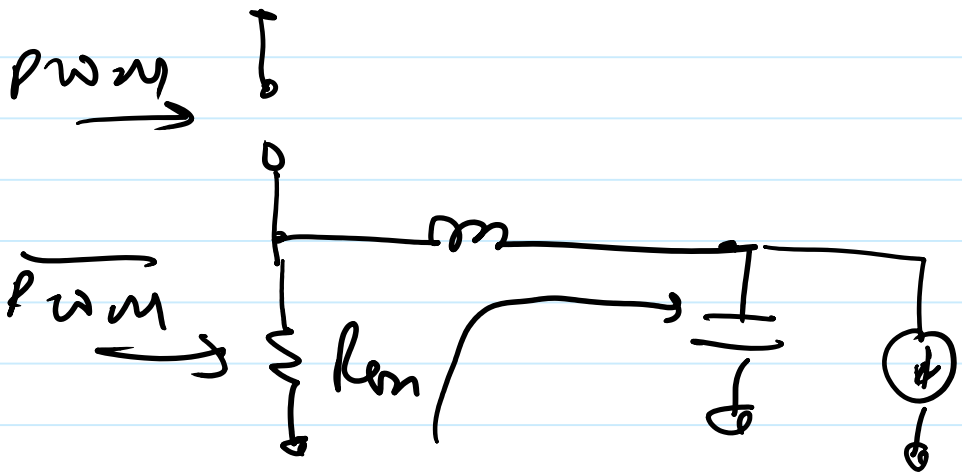
S_1 & S_2 are low resistance switches

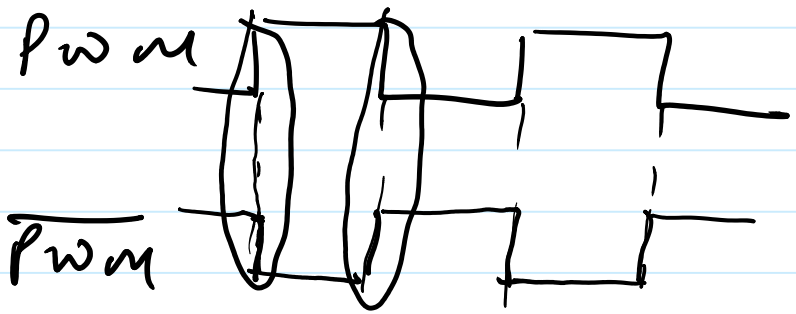
S_1 is ON & S_2 is OFF

R_{on} is order of 10s mΩ



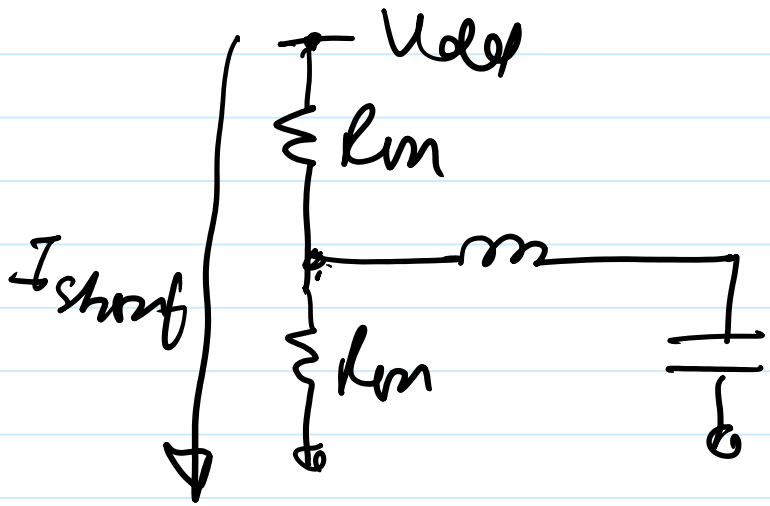
S_2 is ON & S_1 is OFF





There is a possibility that both S_1 & S_2 may turn ON simultaneously during transition

Both S_1 & S_2 are ON



direct path from Vdd to gnd through Rm

$$I_{short} = \frac{V_{dd}}{2R_m}$$

assume $R_m = 10m\Omega$, $V_{dd} = 5V$

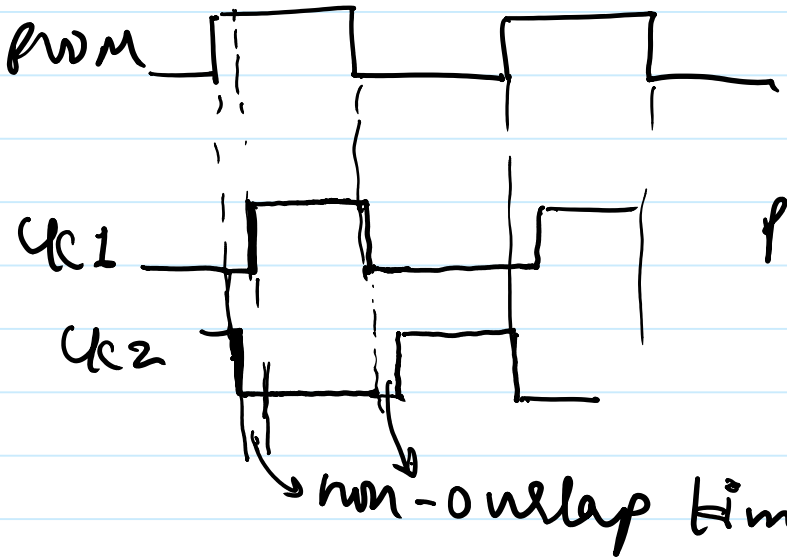
$$I_{short} = \frac{5}{20m\Omega} = 250A$$

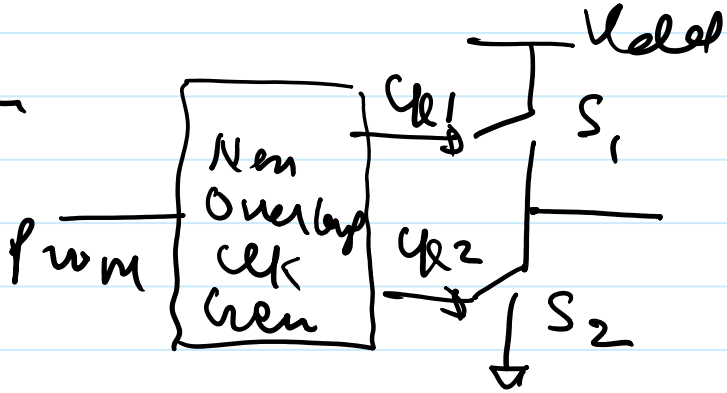
We need to ensure that both switches never turn ON simultaneously.

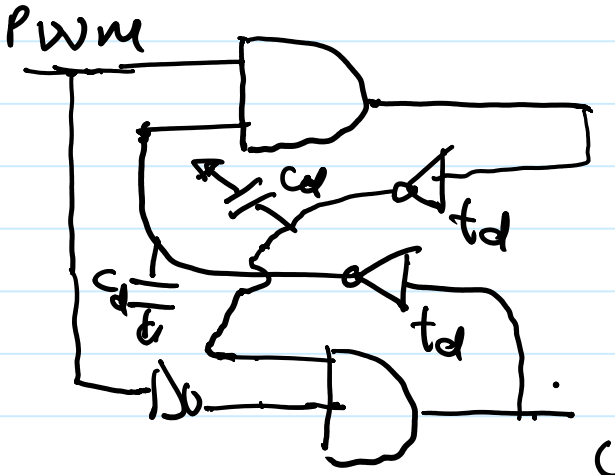
⇒ Break before make

or

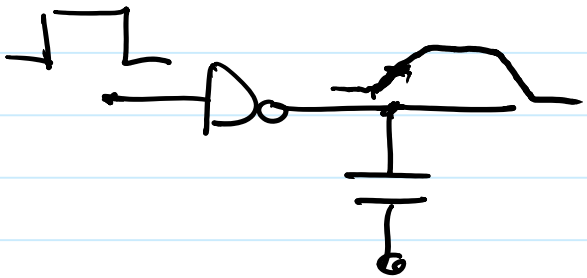
non-overlap clock generator

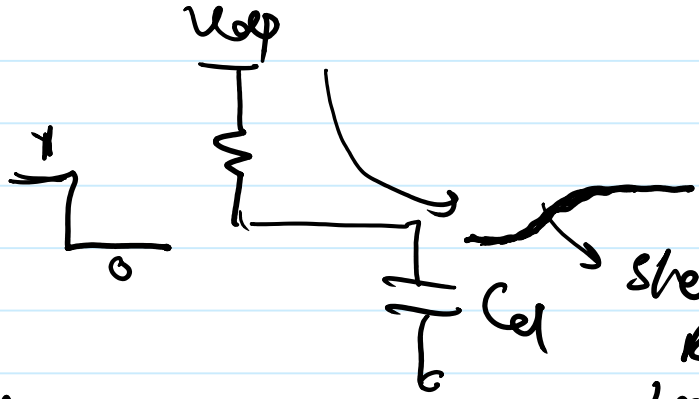


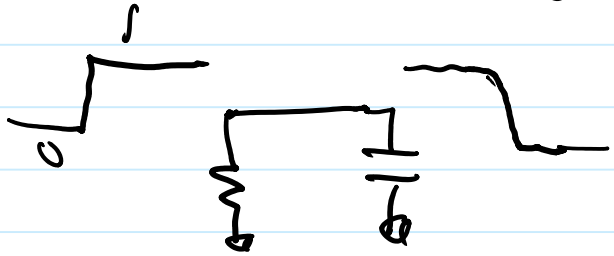




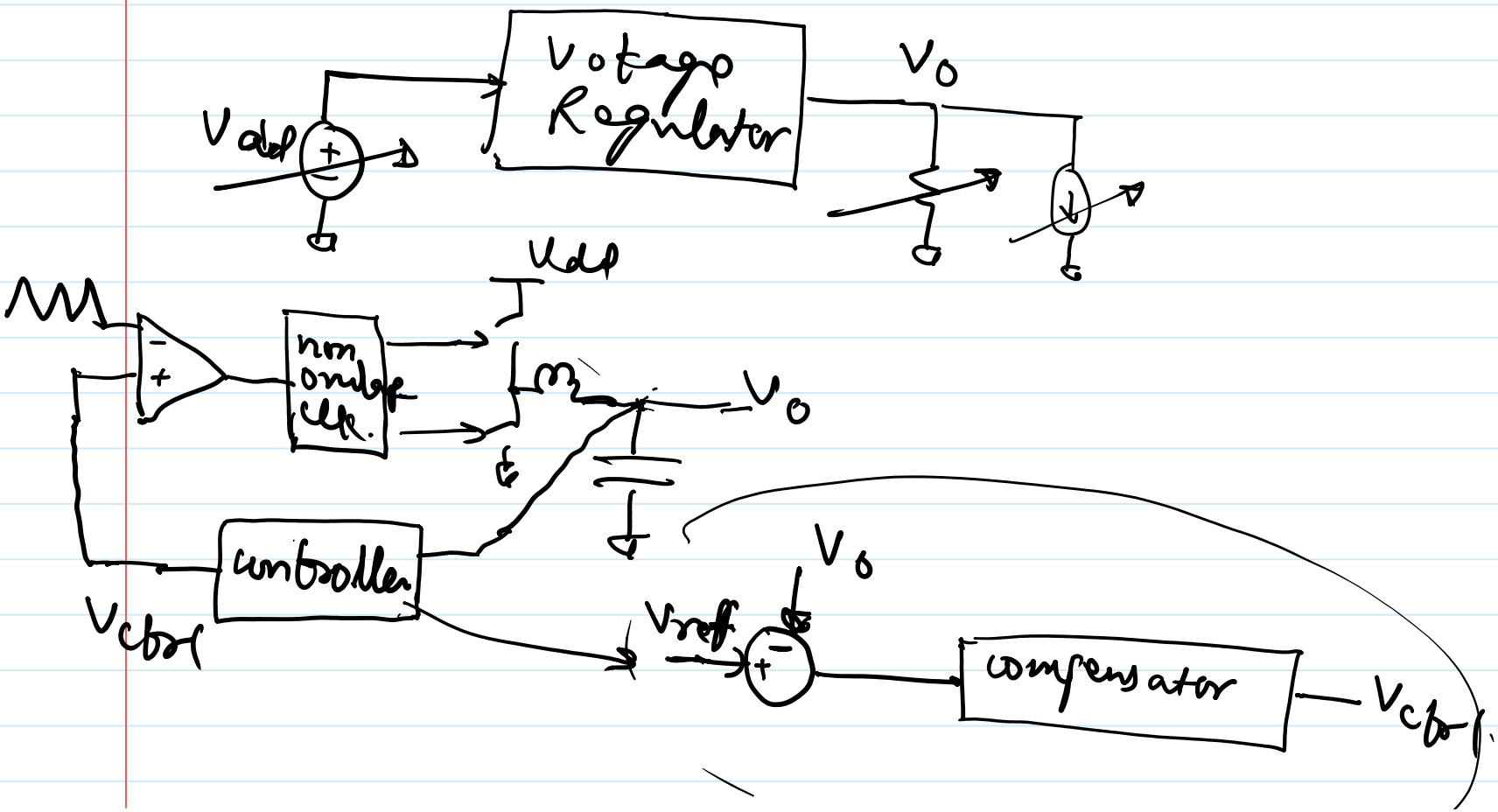
Cd can be used to control non-overlap time

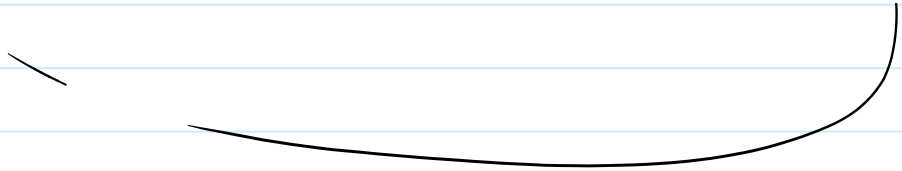


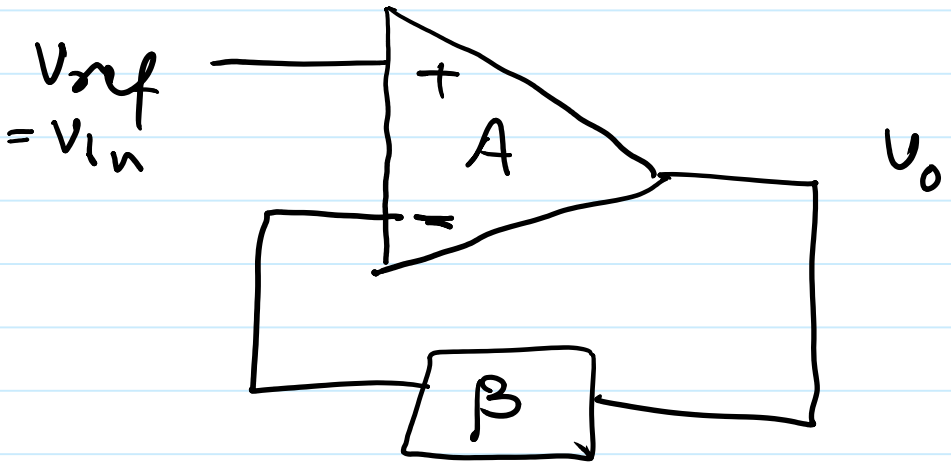




Regulator


Voltage Regulator
V_{dd}
V_o
V_{dd}
non overlap clk.
V_o
controller
V_{cbr}
V_o
V_{ref}
compensator
V_{cb}



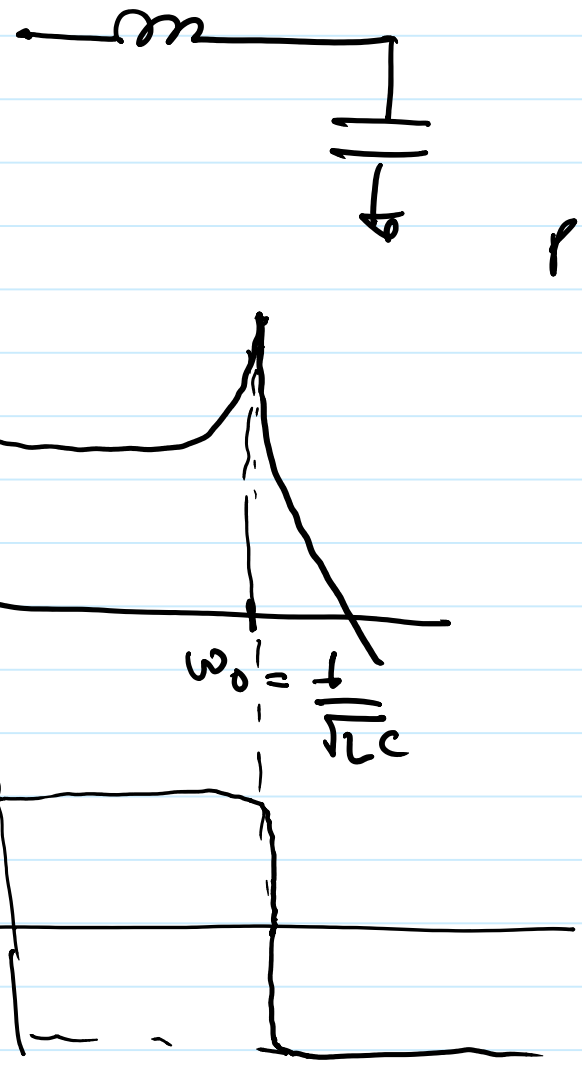


$$\frac{V_o}{V_{in}} = \frac{A}{1 + A\beta}$$

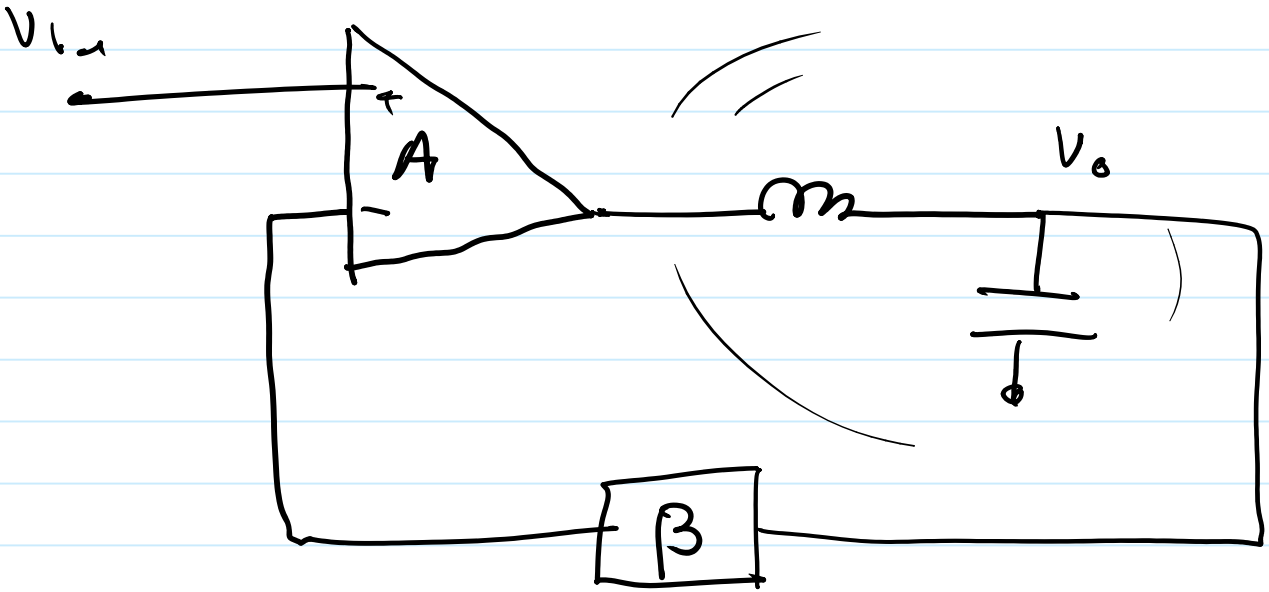
→ Loop gain $= A\beta$

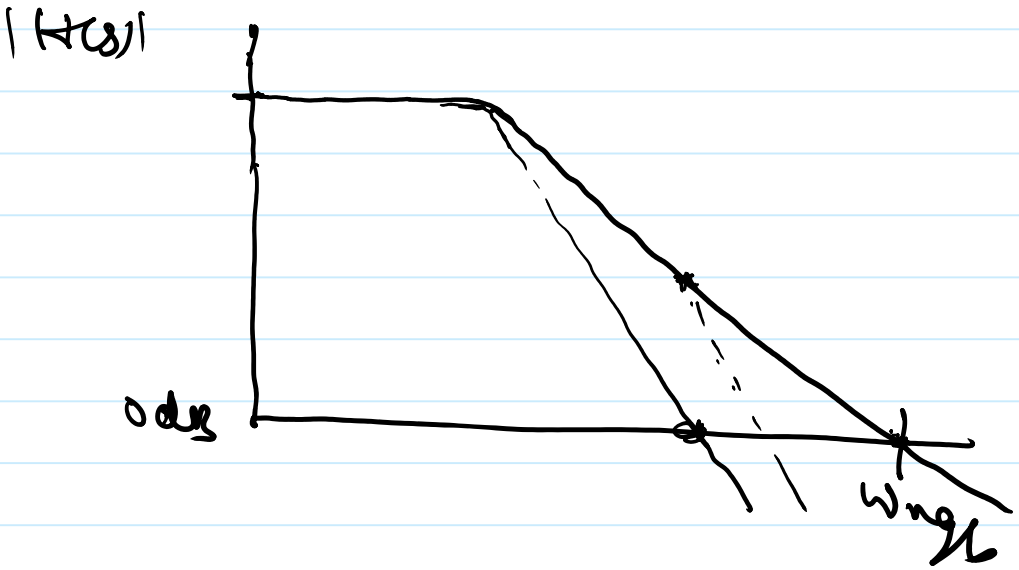
if $A\beta = -1$

$\frac{V_o}{V_{in}} = \infty$ → −ve feedback becomes +ve



$$\text{Poles} = \frac{1}{\sqrt{LC}}$$


V_{in}
+
A
−
V_o
β


$|H(s)|$
0dB
ω_{n_2}