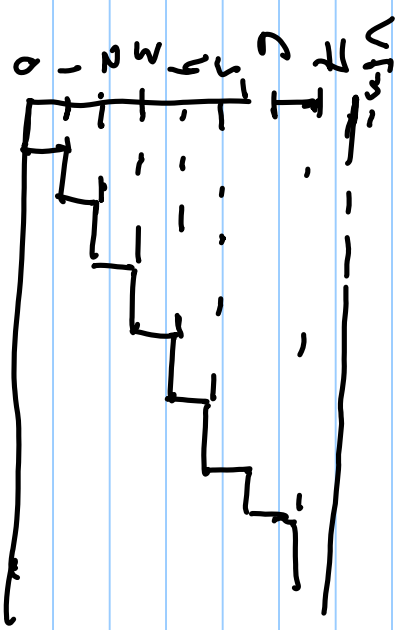
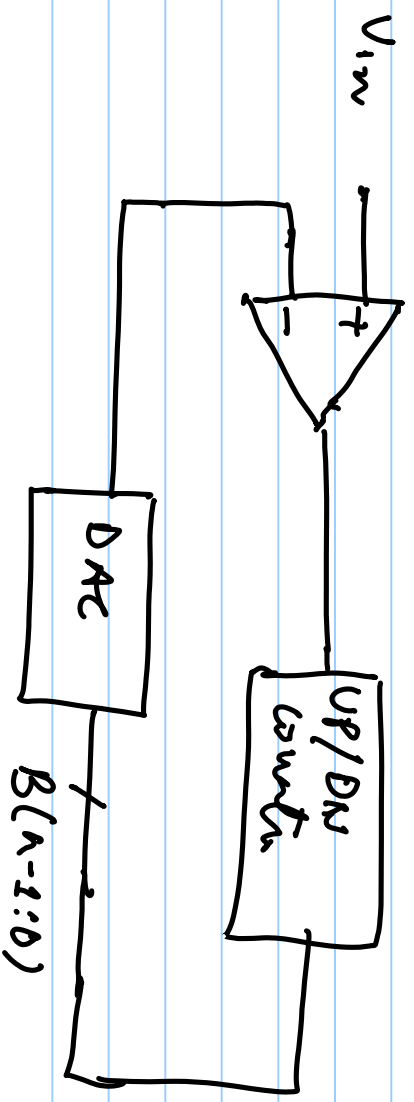


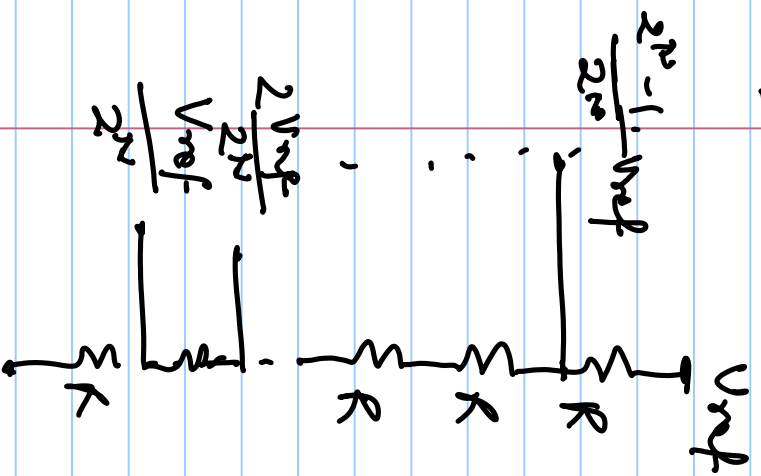
# EE2019

Note Title

4/23/2019



## D/A converters

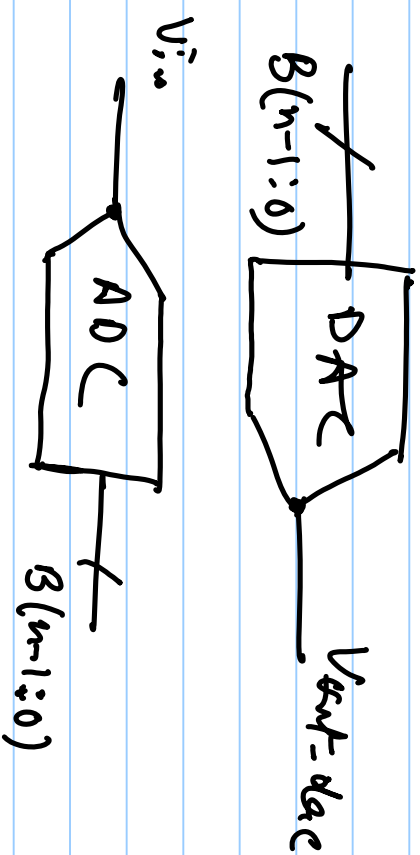


Linearly weighted D/A

$2^N R$  are needed  $\rightarrow$  quite large for higher no. of bits

# Binary weighted D/A Converter

Analog output-

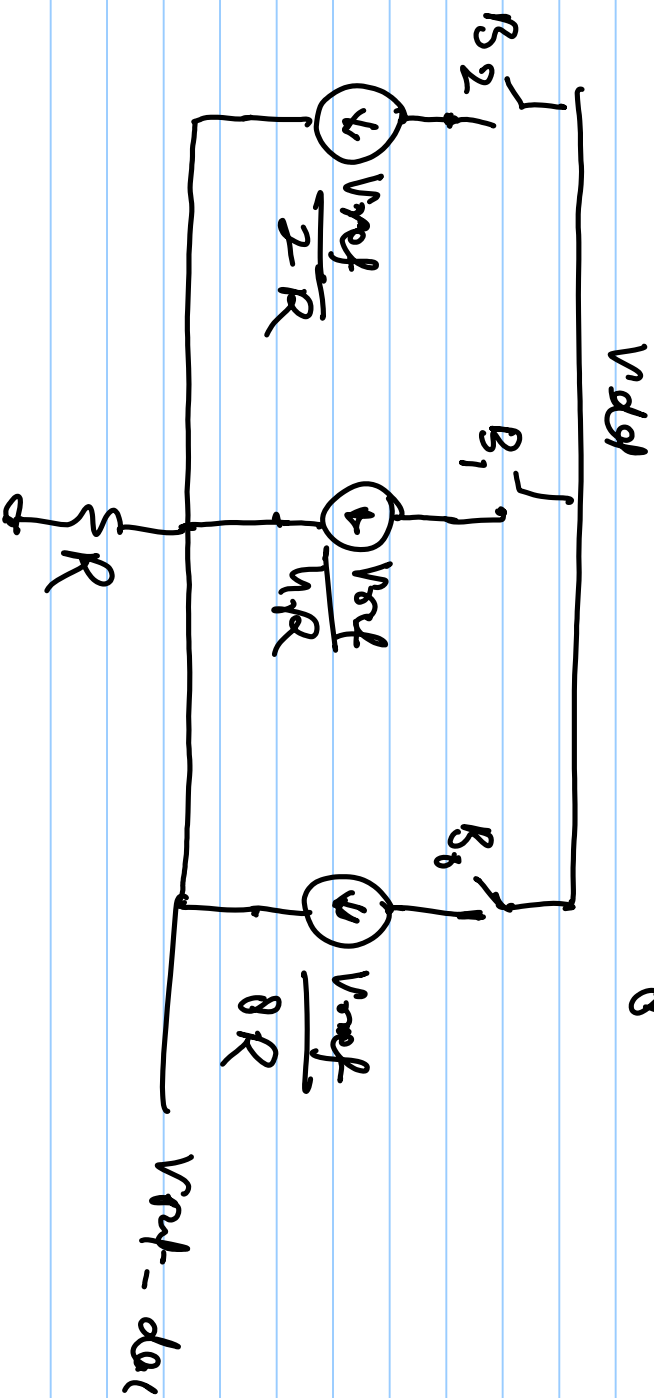


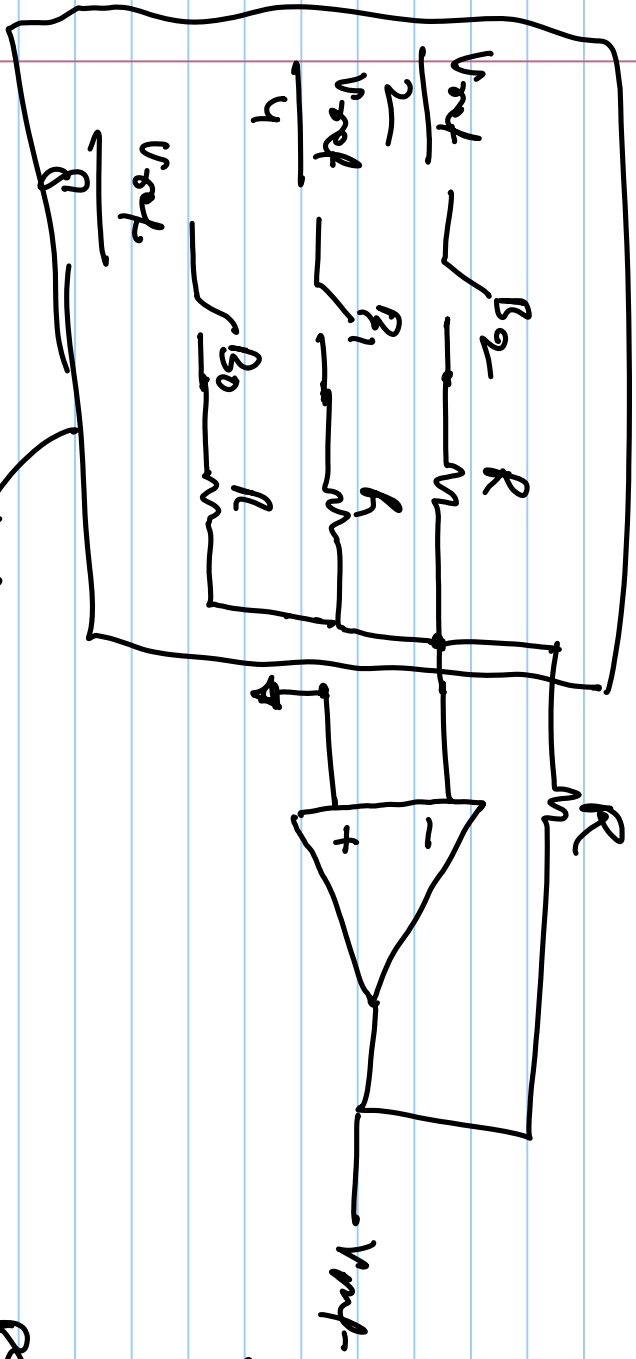
$$V_{out-dac} = \frac{V_{ref}}{2^n} \left[ B_{n-1} 2^{n-1} + B_{n-2} 2^{n-2} + \dots + B_1 2^1 + B_0 2^0 \right]$$

$$= \left[ B_{n-1} \frac{V_{ref}}{2} + B_{n-2} \frac{V_{ref}}{4} + \dots + B_1 \frac{V_{ref}}{2^{n-1}} + B_0 \frac{V_{ref}}{2^n} \right]$$

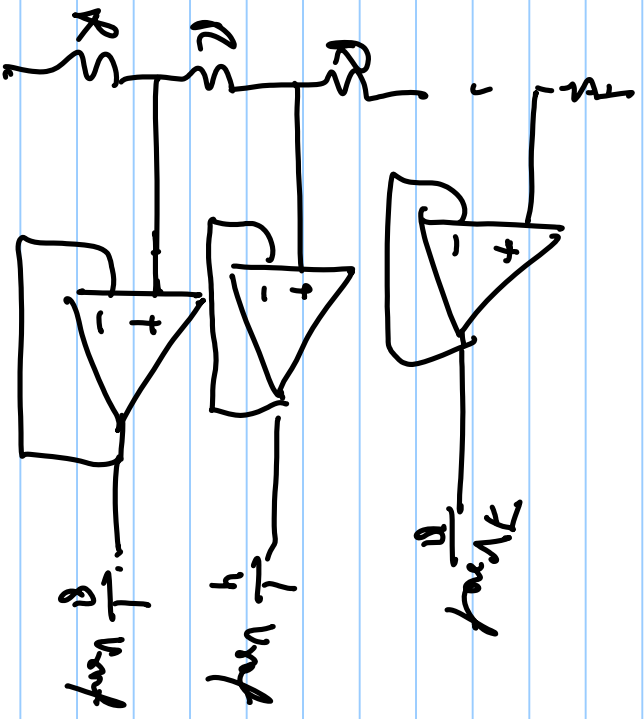
3-bit binary weighted D/A

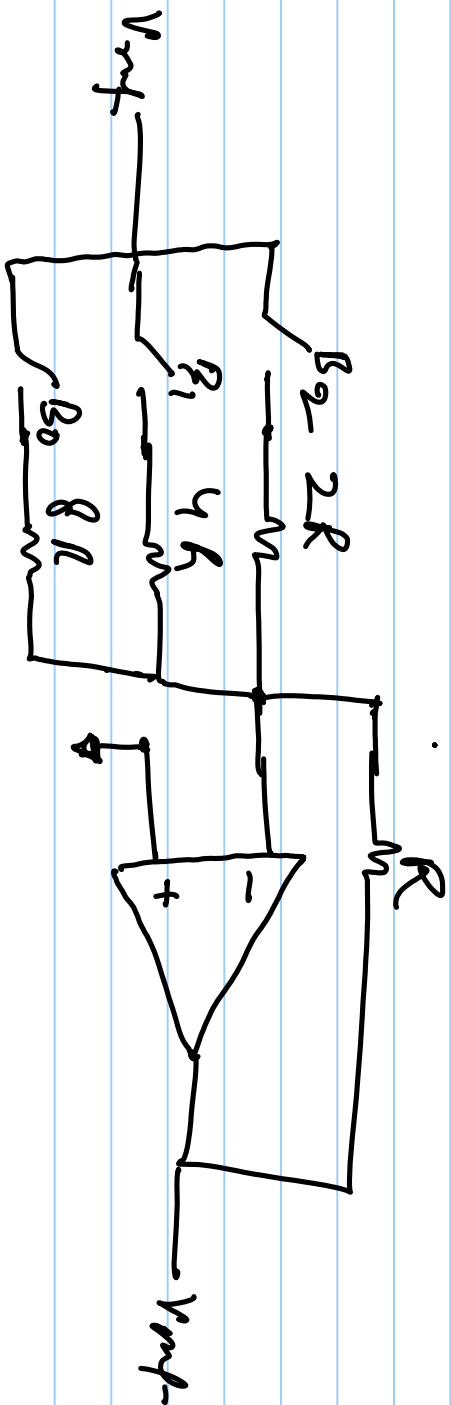
$$LSB = \frac{V_{ref}}{8}$$





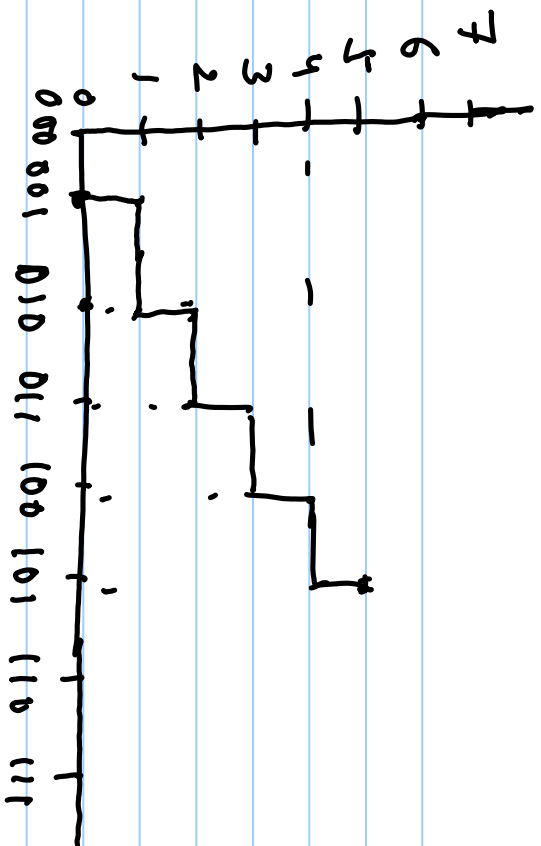
U-I conversion





## Errors in A/D and D/A conversion

1. Quantization error
2. Error in LSB or transition steps
3. Offset  $\rightarrow$  comparator offset or Vref offset



max. tolerable error to ensure  
 Proper operation (no missing code)

$$= \frac{I V_{DS}}{2}$$

