EE2019 Analog Systems Lab

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Chapter 1 Analog Systems Lab Overview

Objective

Design of a composite analog system for synchronized light and sound.

Learning Outcome

At the end of this lab, students should be understand following topics with their application in real world.

- Feedback theory
- Open and closed loop system
- Stability of a closed loop system
- Compensating an unstable system
- Voltage and Current regulation
- Opamp-RC Integrator
- Schmitt Trigger and Oscillator
- Active-RC Filters
- Summing Amplifier (Adder)
- Peak Detector
- Audio Amplifier

Brief Description

The system consists of following three main modules

1. DC-DC Converter based LED Driver
2. Bandpass Filters
3. Adder
4. Peak Detector
5. Class-D Audio Amplifier

When these 3 modules are connected together, it can synchronized light with sound by changing the brightness of LED (Light Emitting Diode) with sound level. Sound can be heard over speaker driven by class-D amplifier. Typically, heart beat and lung sound is used as an input which is derived from stethoscope and processed in electronic stethoscope module. However, alternate audio signal such as fixed frequency tone from audio source or functional generator can also be used.

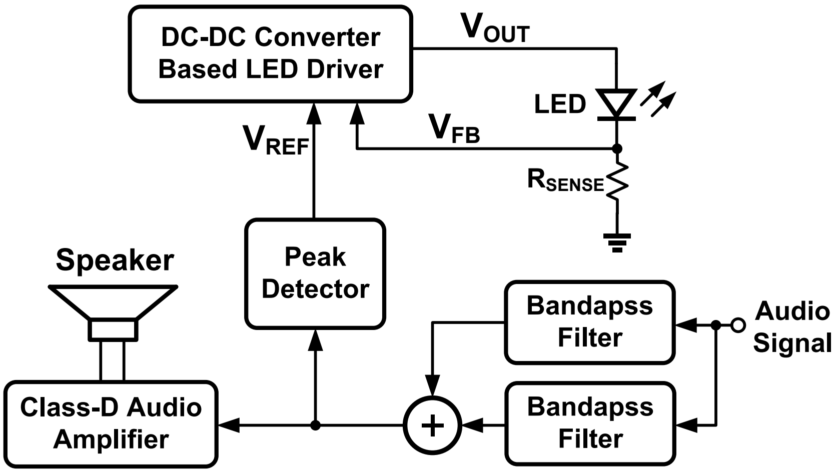

Figure 1-1 System Block diagram of the synchronized light and sound system

Evaluation

- Weekly pre-lab exercise, schematic and simulation: 25%
- Weekly module demo: 25%
- Final system demo: 25%
- Final exam: 25%

Important Instruction

- Pre-lab exercise and simulation results must be demonstrated and submitted before starting the lab experiment.

- Use LTSpice for pre-lab simulations. Information about cad tools can be found at http://www.ee.iitm.ac.in/~nagendra/cadinfo.html

- All lab experiments are carried in a group of two but pre-lab exercises, schematic design and simulations should be performed individually.

Chapter 2 DC-DC Converter Based LED Driver

Introduction

LEDs are designed to operate with a constant current and brightness is usually proportional to the current. Since the V-I characteristic of LED as shown in Figure is exponential, a small change in voltage can cause a significant change in LED current. Since current higher than rated LED current may damage LED, it requires constant voltage over varying operation conditions. Accurate and constant voltage is achieved by voltage regulation (linear or switching). Switching regulator or dc-dc converter is often preferred over linear regulator due to higher efficiency.

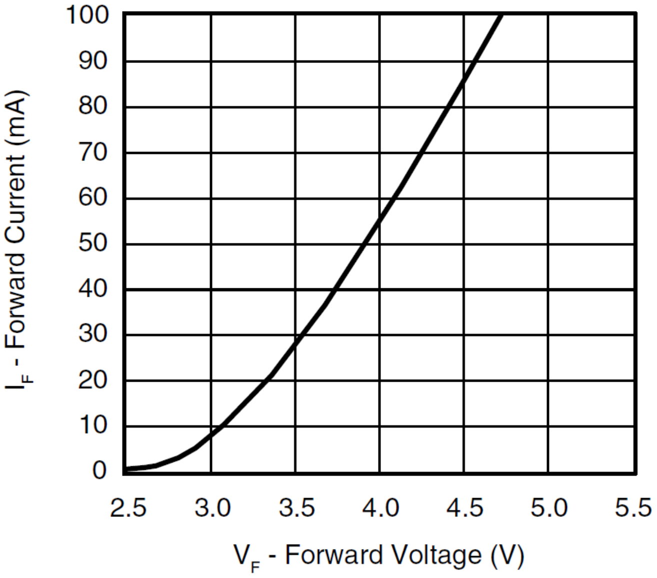

Figure 2-1 Voltage Vs Current Characteristic of LED

Figure 2-2 shows the block diagram of a switching dc-dc converter.

Working Principle

Switching regulator works on the principle of Pulse Width Modulation (PWM) and output voltage, V_{OUT} is expressed as:

Equation 2-1 $V_{OUT} = D \cdot V_{IN}$

Where D is the duty cycle of PWM signal expressed as ratio of ON time over Time Period ($D=T_{ON}/T_{SW}$), V_{IN} is the voltage level of PWM signal.

If V_{IN} remains constant then desired VOUT can be achieved by simply generating a PWM signal with duty cycle $D=V_{OUT}/V_{IN}$ in an open loop system. However, in the real world, V_{IN} varies depending upon the source. For instance if VIN is supplied from battery then voltage may be higher when battery is fully charge compared to when charge is low. Similarly if power source is solar panel voltage may vary based on the light. Therefore an open loop system may fail to work and closed loop system with negative feedback is required to regulate the output voltage with variable V_{IN}.

As shown in Figure 2-2, the feedback voltage, VFB which is scaled version of VOUT is compared with constant reference VREF to generate error signal VERR. Error signal is processed through compensator to generate the control signal VCTRL which is converted to PWM signal by PWM modulator. Since PWM modulator cannot supply high current, it requires a power stage to drive the large current. The switching PWM signal V_{SW} is then passed through a low-pass filter which suppresses all the switching harmonics and converts the PWM signal into desired DC voltage (with small ripple content). V_{OUT} is actually the average of the V_{SW} (which is expressed by Equation 2-1) with small ripple content. The negative feedback automatically adjusts duty cycle D in case of varying V_{IN} to ensure constant V_{OUT}.

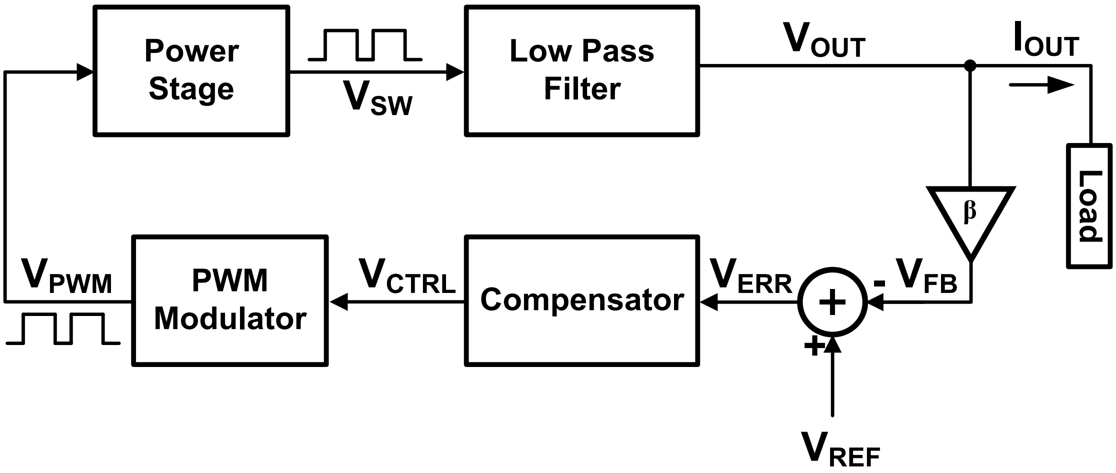

Figure 2-2 Block diagram of a switching regulator

The output voltage VOUT can be programmed either by changing feedback factor β or reference voltage V_{REF} which can expressed as:

Equation 2-2 $V_{OUT} = \frac{V_{REF}}{\beta}$

Building Blocks

As shown in Figure 2-2, a switching regulator consists of following blocks:

1. Low Pass Filter

Since filter has to supply the high load current, a very low loss filter is required. An ideal inductor has zero loss (zero impedance) at dc, hence LC low-pass filter makes an ideal choice for dc-dc converter.

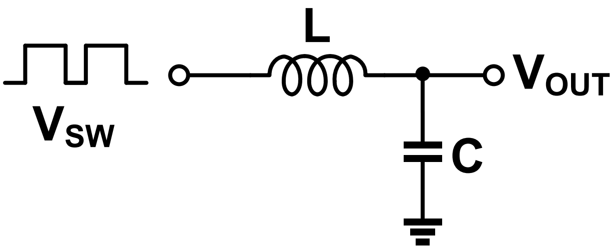

Figure 2-3 An ideal LC Low-pass Filter

In reality, inductor has a small series resistance call DCR and LC Low-pass filter in Figure 2-3 becomes a RLC filter as shown in Figure 2-4 which further modifies as Figure 2-5 with presence of resistive load R_{OUT}.

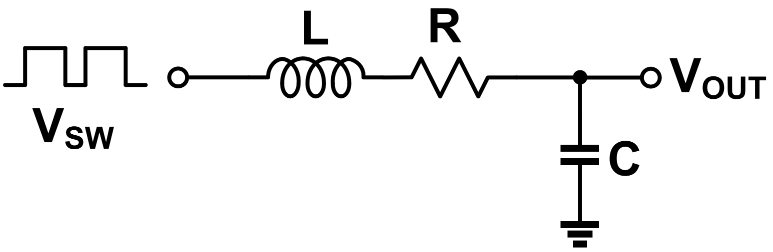

Figure 2-4 A non-ideal LC Low-pass Filter

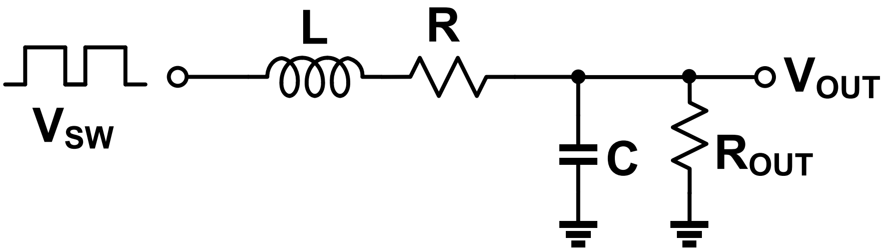

Figure 2-5 A non-ideal LC Low-pass Filter with resistive load R_{OUT}

Exercise 2-1 *Derive the AC transfer function of LC low-pass filters shown in Figure 2-3, Figure 2-4 and Figure 2-5. Find expressions for centre frequency W_o and quality factor Q_o for all the three filters. Study the effect of R and R_{OUT} on W_o and Q_o.*

Selecting L and C

The values and inductor L and capacitor C is selected based on two factors (1) Switching frequency (2) Inductor ripple current. The cut-off frequency of LC filter is selected 50-100 times lower than switching frequency to minimize the output voltage ripple. Value of inductor is selected to minimize the inductor ripple current for reduced RMS losses and also prevent the inductor from getting saturated. Since larger inductor value comes at the cost of bigger area, there is always a trade-off between inductor size and efficiency. The minimum value of an inductor is quite often chosen such that peak-to-peak ripple current of inductor does not exceed 1.5-2 time of the maximum load current while maximum value depends upon the required light load efficiency.

The peak-to-peak inductor ripple current can be expressed as:

Equation 2-3 $$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot \frac{D}{F_{SW}}$$

Where D is the duty cycle and F_{SW} is the switching frequency of the PWM signal V_{SW}. The output ripple voltage can be derived by integrating the inductor ripple current and expressed as:

Equation 2-4 $\Delta V_O = \frac{V_{IN} - V_{OUT}}{L} \cdot \frac{D}{8 \cdot C \cdot F_{SW}{}^2}$

The behaviour of inductor ripple current and output ripple voltage is shown in Figure 2-6.

There might be inductors with different dc and saturation current ratings for the same value and one should be careful in choosing the inductor to ensure that peak inductor current does not exceed the inductor saturation current under any operating conditions.

Exercise 2-2 *For a constant V_{OUT}, derive the duty cycle D for which ΔI_L is maximum. Plot the characteristic of ΔI_L Vs. D for D=0 to 1 for V_{IN}=5V, L=10uH and F_{SW}=500KHz.*

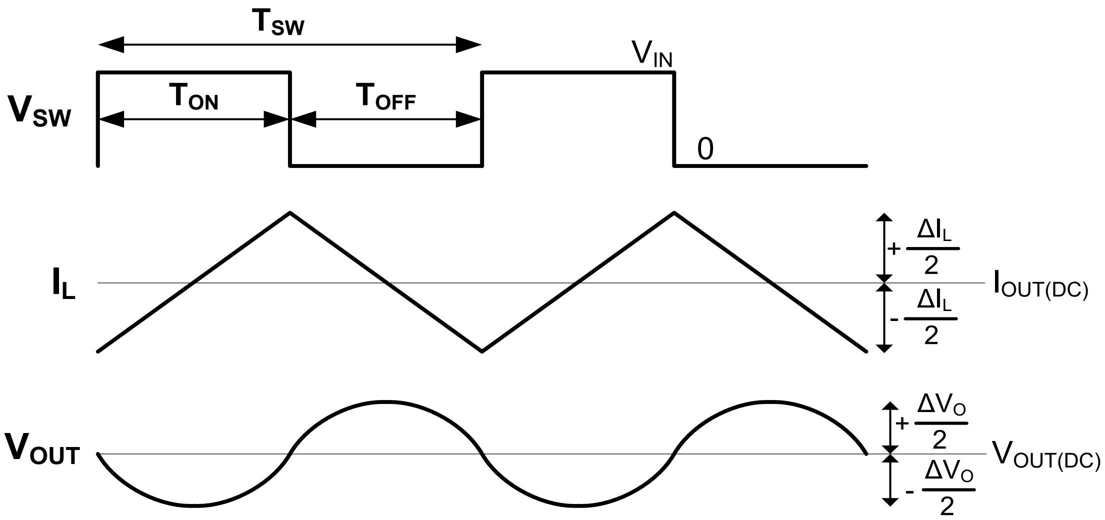

Figure 2-6 Inductor ripple current and output ripple voltage of LC Low-pass Filter with PWM input

2. Compensator

The RLC filter possesses double poles which are complex in nature hence causing 180 Degree phase shift. Negative feedback with 180 Degree phase shift makes the system unstable hence need to be compensated. As per the rule, in order to have a stable system, there could be only one dominant pole in a closed loop system with negative feedback. The compensator in a dc-dc converter can be used to either cancel one of the poles of LCR filter by using type-3 compensation or push both the poles outside unity gain bandwidth by using type-1 compensation.

Type-1 Compensation

Type-1 compensation uses a single pole low pass filter or integrator such that the UGB of the loop is much less (5-10 times) of the double pole frequency of LC filter. Figure 2-7 shows a first order opamp-RC filter used as type-1 compensator.

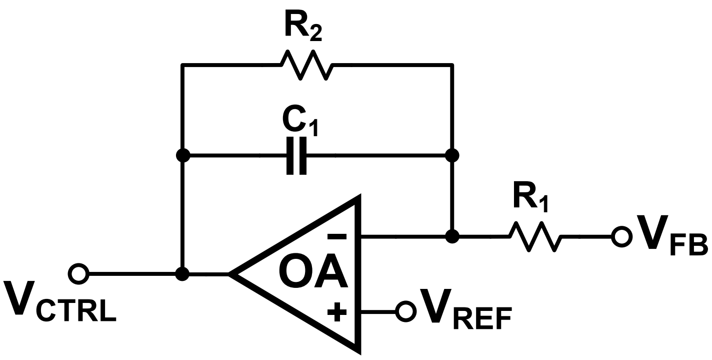

Figure 2-7 Fist order opamp-RC filter as type-1 compensator

Connecting positive terminal of opamp to VREF performs the function of subtraction (V_{ERR}=V_{REF}-V_{FB}) and low pass filter processes the error signal to get V_{CTRL}. Ideally, we desire zero dc error between VFB and VREF which can only be achieved by having infinite gain at dc. The feedback resistor R2 in the low pass filter limits the dc gain hence an opamp-RC integrator is preferred over lowpass filter as type-1 compensator.

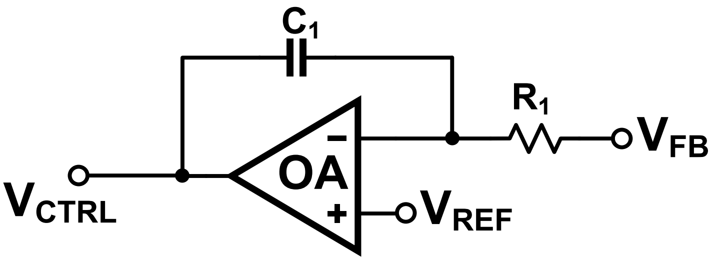

Figure 2-8 Opamp-RC integrator as type-1 compensator

Type-1 compensation can only be used with slower system where fast transient response or tracking speed is not needed as low bandwidth of the loop makes the system very slow.

Exercise 2-3 *Draw the bode plots of lowpass filter and integrator shown in Figure 2-7 and Figure 2-8, respectively. Find the expression for unity gain bandwidth (UGB) for the two circuits.*

Type-3 Compensation

Unlike type-1 compensator which pushes the double LC poles out of UGB by reducing the loop bandwidth, type-3 compensator cancels one of LC poles and extends the loop bandwidth. Type-3 compensator offers fast transient response and tracking speed due to higher bandwidth. The compensator is also known as PID as it possesses Proportional (P), Integral (I) and Derivative (D) components. Circuit diagram of a type-3 compensator is shown in

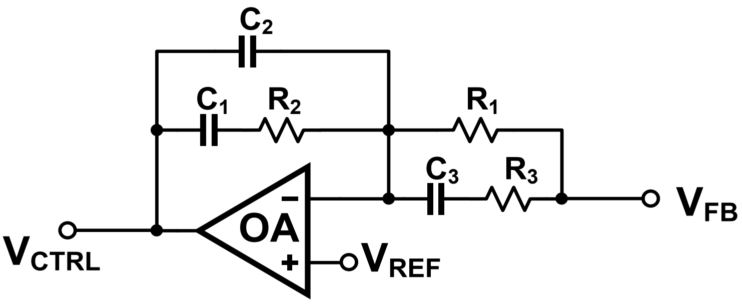

Figure 2-9 Opamp-RC integrator as type-1 compensator

3. PWM Modulator

PWM modulator is used to convert the control voltage, V_{CTRL} to PWM signal by comparing V_{CRTL} with a fixed frequency ramp signal as shown in Figure 2-10. Duty cycle of the PWM signal is proportional to V_{CTRL} and can be expressed as:

Equation 2-5 $$D = \frac{T_{ON}}{T_{SW}} = \frac{V_{CTRL}}{V_M}$$

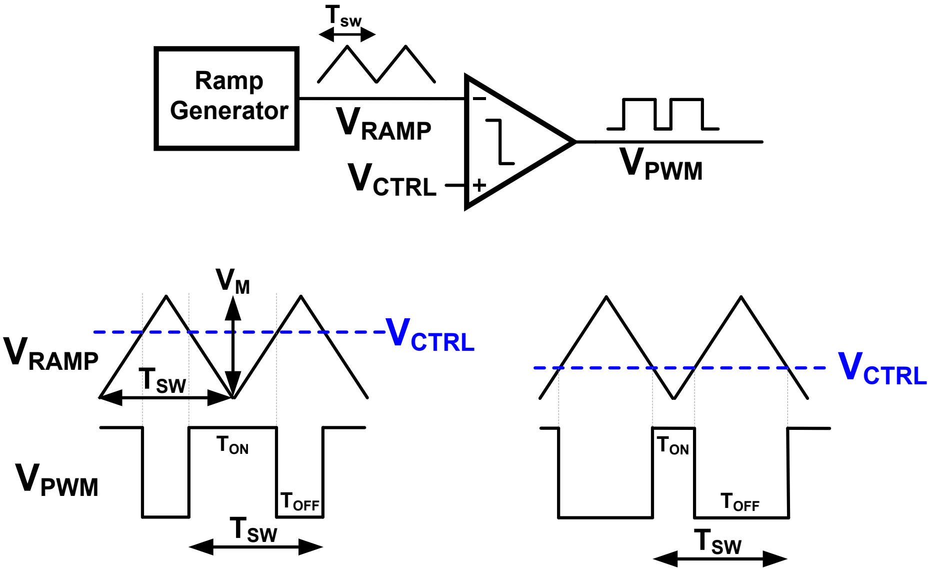

Figure 2-10 PWM Modulator

4. Power Stage

Since PWM comparator is not strong enough to drive high current, it requires high current complementary switches M_P and M_N. These switches are usually power MOSFETs with high gate capacitance hence also require gate drivers to ensure small rise/fall times. Non-overlap clock generator is used to avoid any circuit current between VIN-GND via M_P-M_N which may damage the circuitry. Non-overlap time can be adjusted by changing values if capacitors C_P and C_N.

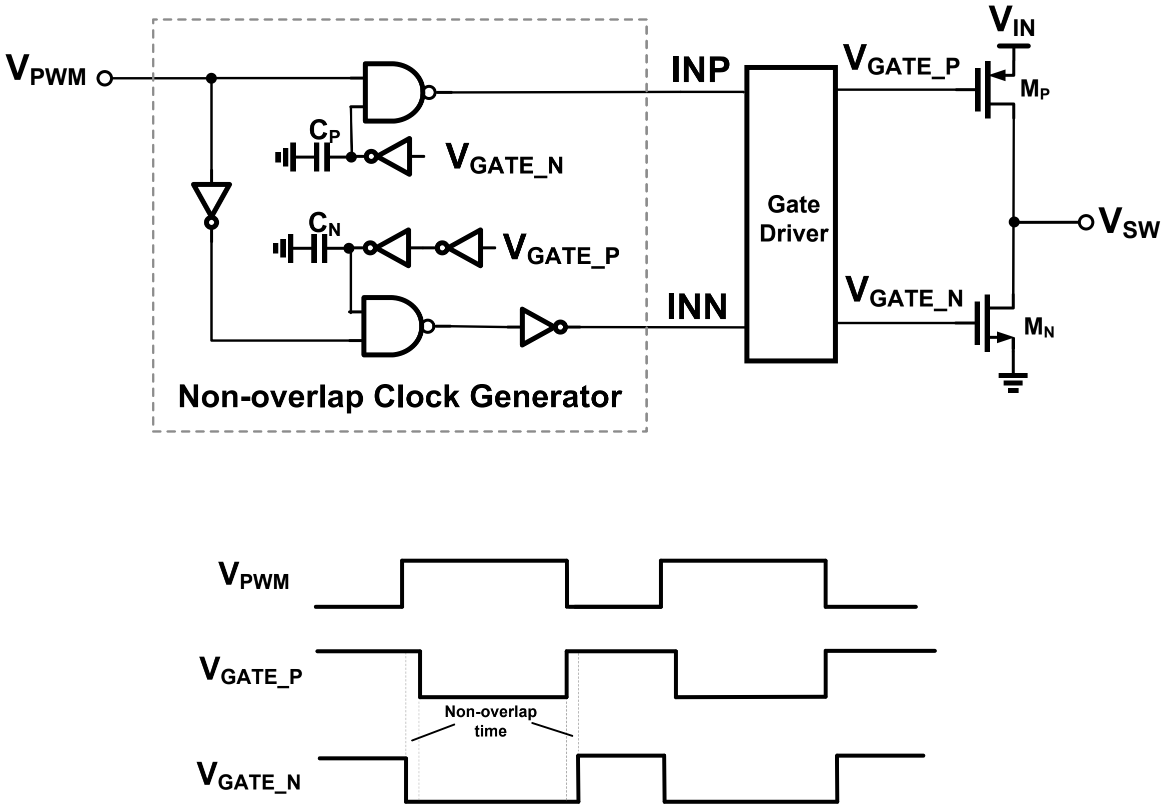

Figure 2-11 Power Stage with Non-overlap Clock Generator and Gate Driver

The complete LED driver using Type-I and Type-III compensator are shown in Figure 2-12 and Figure 2-13, respectively. Open loop or loop gain transfer function of the LED driver can be expressed as:

Equation 2-6
$$H(s) = \beta \cdot H_{comp}(s) \cdot \frac{1}{V_M} \cdot V_{IN} \cdot H_{LS}(s)$$

Where,

V_M is the peak-to-peak amplitude of ramp signal (V_{RAMP}), V_{IN} is the input supply of power stage and β is the feedback factor and can be derived from Equation 2-2 as:

Equation 2-7
$$\beta = \frac{V_{REF}}{V_{OUT}} = \frac{V_{REF}}{V_{REF}+V_{F\_LED}}$$

Where V_{F_LED} is the LED forward voltage, V_M is the amplitude of the ramp signal and V_{IN} is the power stage input supply voltage.

$H_{COMP}(s)$ is the transfer function of compensator and $H_{LS}(s)$ is the transfer function of LC low-pass filter.

Current into LED (I_{OUT}) can be expressed as:

Equation 2-8
$$I_{OUT} = \frac{V_{REF}}{R_{SENSE}}$$

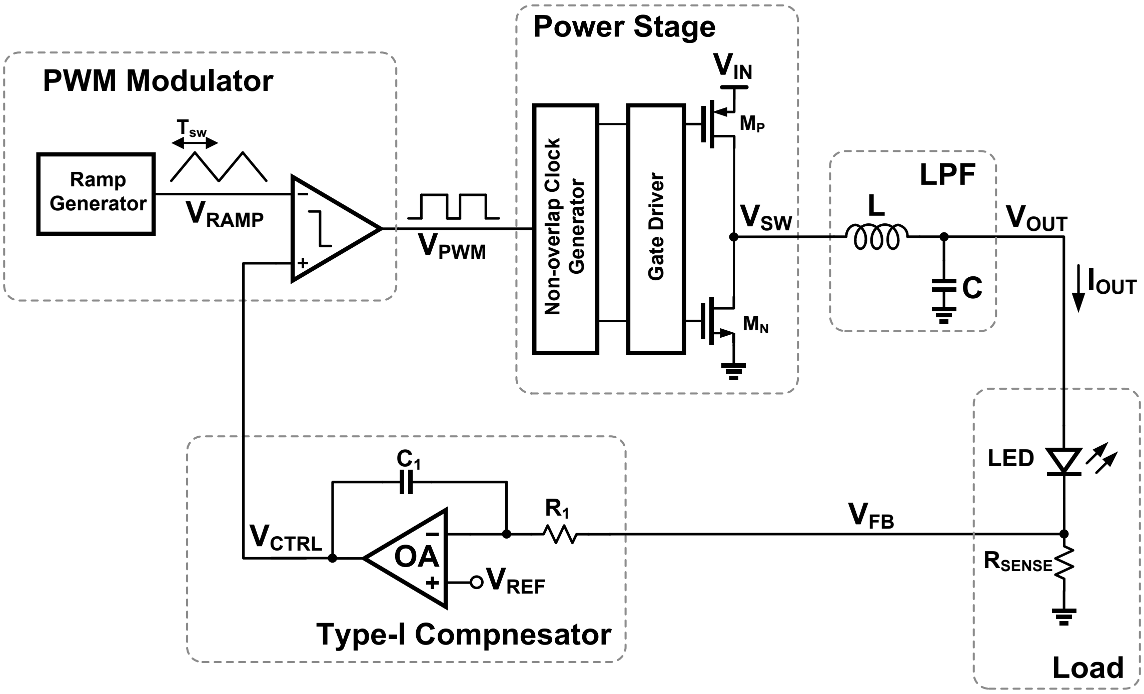

Figure 2-12 Circuit diagram of a dc-dc converter based LED driver using Type-I compensator

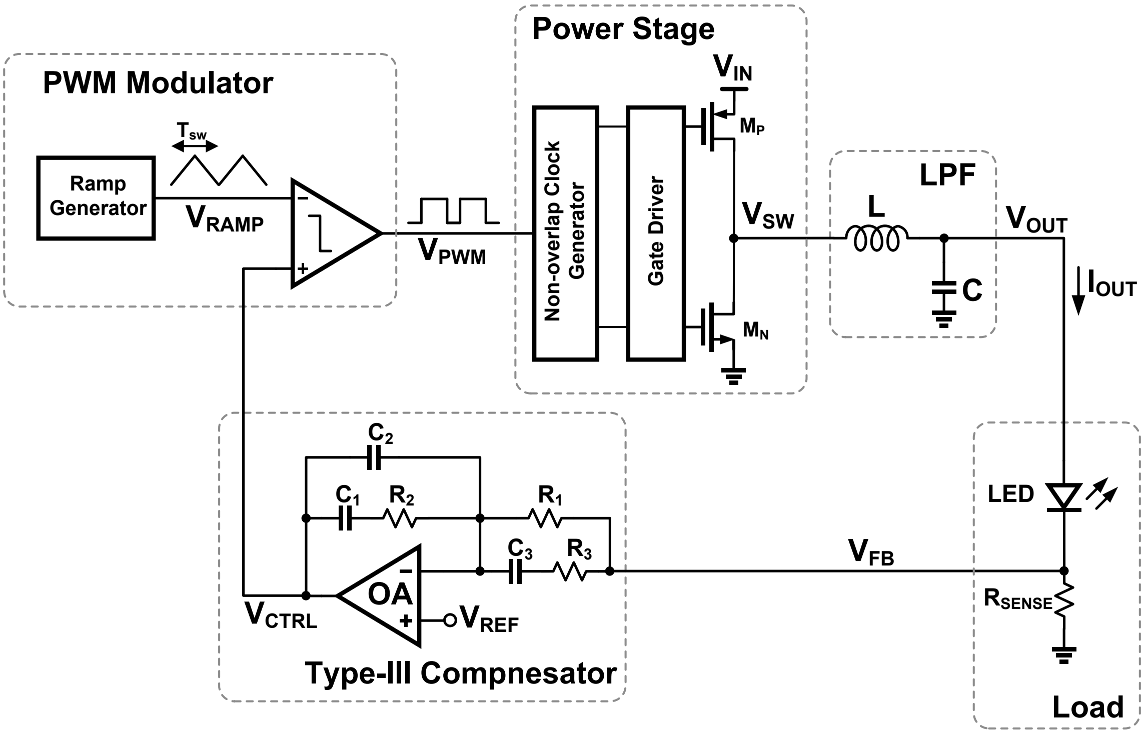

Figure 2-13 Circuit diagram of a dc-dc converter based LED driver using Type-III Compensator

References:

1. http://www.electronics-tutorials.ws/opamp/opamp_6.html
2. https://www.allaboutcircuits.com/textbook/semiconductors/chpt-8/differentiator-integrator-circuits/
3. http://fab.cba.mit.edu/classes/961.04/topics/pwm.pdf
4. http://www.ti.com/lit/an/sloa020a/sloa020a.pdf
5. https://en.wikipedia.org/wiki/Phase_margin
6. http://www.mit.edu/afs.new/athena/course/2/2.010/www_f00/psets/hw3_dir/tutor3_dir/tut3_g.html
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9. https://www.allaboutcircuits.com/technical-articles/negative-feedback-part-5-gain-margin-and-phase-margin/
10. https://www.allaboutcircuits.com/technical-articles/negative-feedback-part-6-new-and-improved-stability-analysis/
11. https://www.allaboutcircuits.com/technical-articles/negative-feedback-part-9-breaking-the-loop/

EXPERIMENT-1: RAMP GENERATOR AND PWM MODULATOR

Circuit Diagram

Ramp or triangle wave generator is actually an oscillator which is designed using opamp-RC integrator and Schmitt trigger. PWM is generated by comparing the ramp signal (V_{RAMP}) with control signal (V_{CTRL}). Common mode voltage of ramp signal should be around $V_{DD}/2$ hence might require to decouple the dc voltage and set common mode at V_{BIAS} (around $V_{DD}/2$). In case common mode of V_{RAMP} is $V_{DD}/2$, C_{BIAS} and R_{BIAS} may not be needed and V_{RAMP} can be directly connected to comparator input (V_{RAMP_B}).

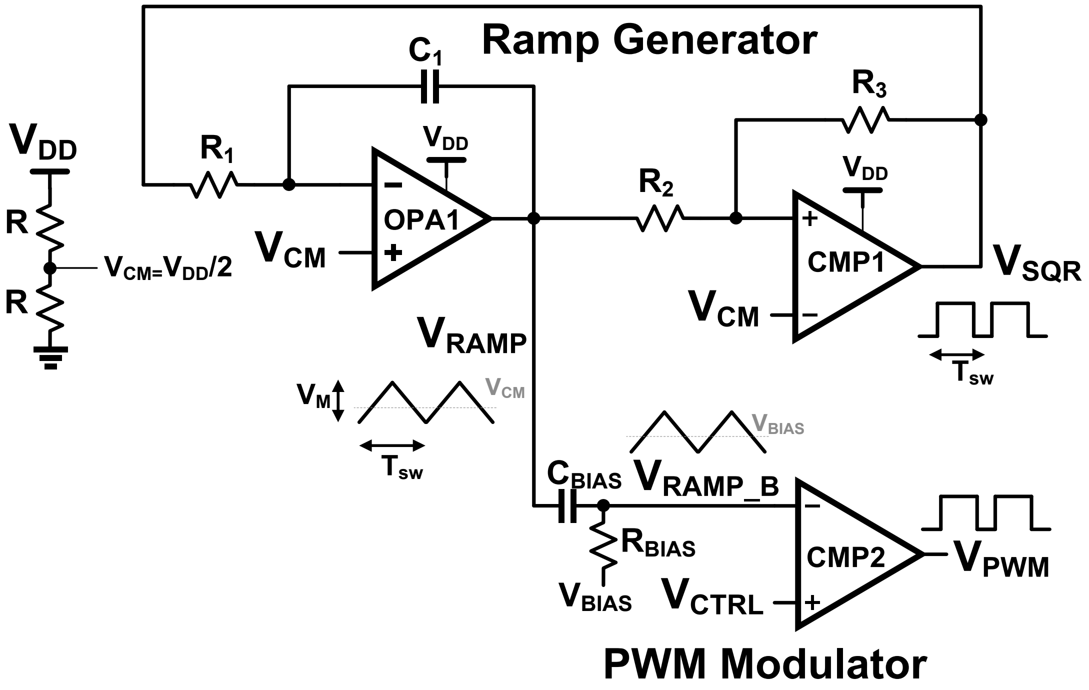


Figure 2-14 Ramp Generator Circuit

The peak-peak amplitude of the ramp is defined by the equation:

Equation 2-9 $$V_M = 2 \cdot \frac{R_2}{R_3} \cdot V_{CM}$$

The oscillation frequency of the ramp is given by equation:

Equation 2-10 $$F_{SW} \text{ or } 1/T_{SW} = \frac{R_3}{4 \cdot R_2 \cdot R_1 \cdot C_1}$$

Specifications

- Supply voltage (V_{DD}) = 5V
- Frequency ($1/T_{SW}$) = 100KHz
- Peak-peak ramp amplitude (V_M) = 1V

List of Components

- OPA1: MCP6004 or equivalent
- CMP1 and CMP2: LM339 (open collector – requires a pullup resistor between V_{DD} and V_{OUT})

List of Measurements

1. Set V_{IN}=5V, $V_{CM} = V_{BIAS} = V_{IN}/2$, $V_{CTRL} = V_{DD}/2$
2. Capture integrator output (V_{RAMP}) and Schmitt trigger output (square wave)
3. Measure and record frequency of V_{RAMP} and square wave
4. Measure amplitude of V_{RAMP}
5. Capture the ramp waveform V_{RAMP_B} and measure the amplitude and dc bias
6. Measure and record frequency of V_{RAMP_B}
7. Capture V_{PWM}, measure frequency and duty cycle
8. Capture and measure
9. Sweep V_{CTRL} between 0 to 1V to get duty cycles of 0%, 25%, 50%, 75% and 100%. Measure and record value of V_{CTRL} and V_{PWM} duty cycle.

Pre-Lab Exercises

1. For the ramp generator circuit in Figure 2-14, derive the expression for ramp amplitude (Equation 2-9) and frequency (Equation 2-10).
2. Simulate the ramp generator circuit shown in Figure 2-14 and verify the expressions in Equation 2-9 and Equation 2-10. Observe the effect of variation in R1, R2, R3 and C1 on ramp amplitude and frequency.
3. Plot the waveforms and perform measurements 1-9 using simulation.

EXPERIMENT-2: POWER STAGE AND LPF

Circuit Diagram

Power stage uses V_{PWM} from PWM modulator as input and drives LC LPF through power MOSFETs M_P and M_N. V_{GATE_P} and V_{GATE_N} must be non-overlapped (break before make) to avoid short circuit condition which may damage bread board and circuitry. Non-overlap time of the power stage can be adjusted by varying C_P and C_N. It is recommended to disconnect power supply (V_{IN}) from M_P for testing the non-overlap time. Once non-overlap time is verified, VIN can be connected back.

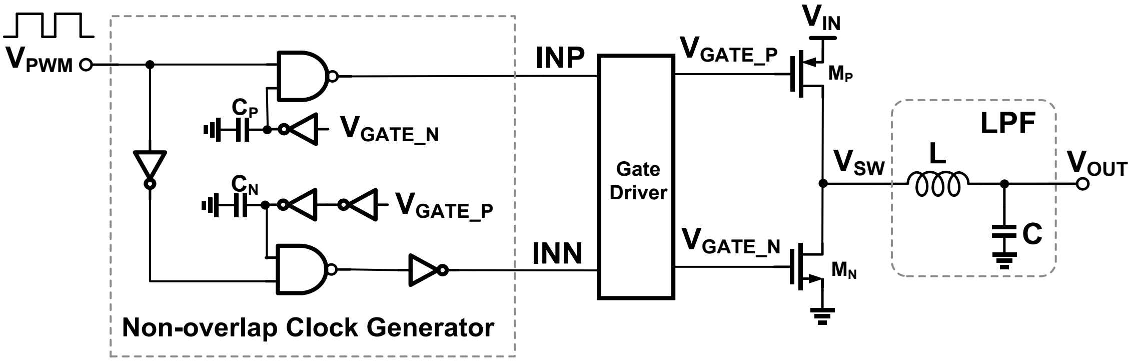


Figure 2-15 Power stage and LPF

Specifications

- Supply voltage (V_{IN}=V_{DD}) = 5V
- PWM Frequency ($1/T_{SW}$) = 100KHz

List of Components

- NAND Gates: SN74AHC00N or equivalent
- Inverters: CD4069UBE or equivalent
- Gate Driver: TC427EPA
- Power MOSFETs: IPP45P03P4L-11 (PMOS) and NTD3055L104-1G (NMOS)
- Inductor (L): RCH875NP-101K
- Capacitor (C): 47µF

List of Measurements

1. Set V_{DD}=V_{IN}=5V, PWM duty cycle (D)=50%
2. disconnect V_{IN} from M_P and input V_{PWM} from Experiment-1
3. Capture V_{GATE_P} and V_{GATE_N}, measure non-overlap time
4. Connect V_{IN} back to M_P
5. Capture V_{SW} and measure dead time, duty cycle and frequency. Observe the difference between V_{PWM} and V_{SW}
6. Plot V_{OUT}, measure average value, ripple amplitude and frequency
7. Vary PWM duty cycle (D) from 0 to 100% with 25% step by adjusting V_{CTRL} and repeat 6. Verify relationship, D = V_{OUT}/V_{IN}
8. Set D=50% and apply resistive load to draw 50mA from V_{OUT}

9. Observe difference in V_{OUT} with and without load. What could be the possible reasons for differences?

Pre-Lab Exercises

1. Design the power stage shown in Figure 2-15 in LTSpice and verify the functionality through simulation.
2. Perform measurements 1-9 using simulation. Capture all the graphs.

EXPERIMENT-3: COMPENSATOR AND MDODULE INTEGRATION

Circuit Diagram

For simplicity, type-I (integrator) compensator is used for loop compensation.

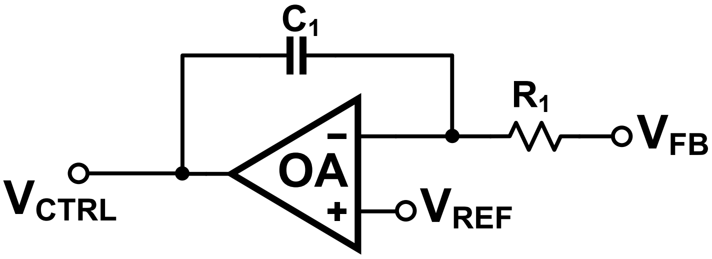


Figure 2-16 Type-I (Integral) Compensator

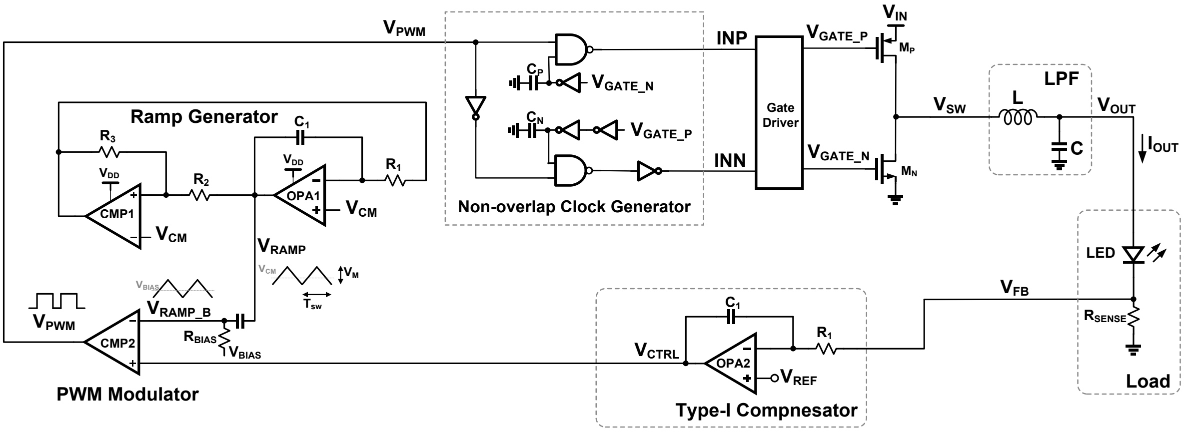


Figure 2-17 Complete LED Driver

Generating V_{REF}

V_{REF} applied at positive terminal of OPA2 determines the current into LED (see Equation 2-8). For standalone LED driver, V_{REF} can be supplied from the power supply.

Stability Analysis

Stability analysis of the complete LED driver (is done by modelling the circuit in continuous domain to get the open loop transfer function of Equation 2-6 so that bode plot can be used to analyse the transfer function.

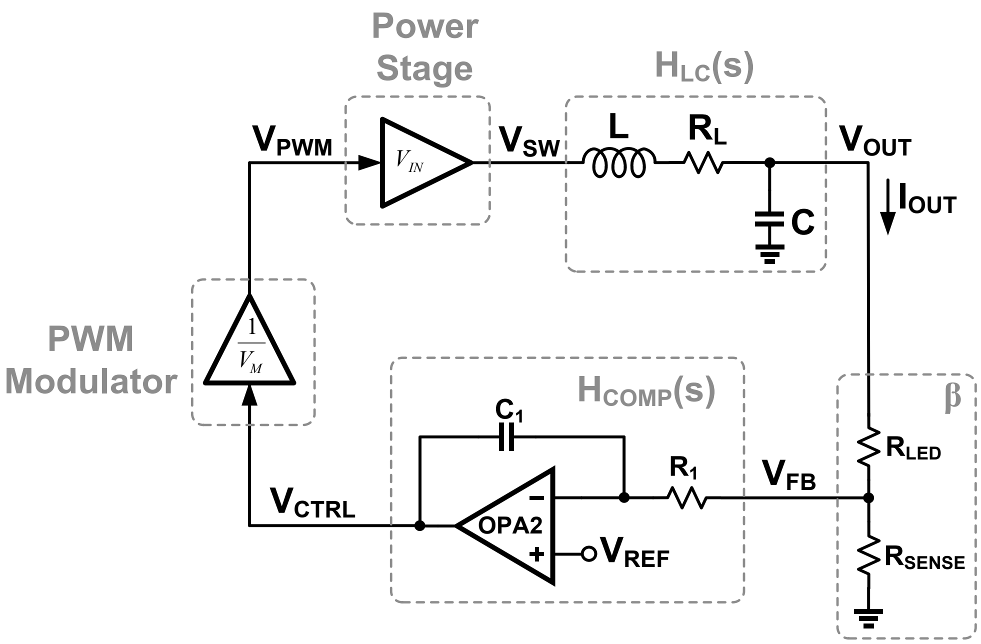


Figure 2-18 Continuous time model of siwtching LED driver with Type-I compensator

LED can be replaced by an equivalent resistor R_{LED} and V_{FB} can be expressed as:

Equation 2-11 $$V_{FB} = \frac{R_{SENSE}}{R_{SENSE}+R_{LED}} V_{OUT}$$

Since $V_{FB}=V_{REF}$

Equation 2-12 $$\beta = \frac{V_{REF}}{V_{OUT}} = \frac{R_{SENSE}}{R_{SENSE}+R_{LED}}$$

Using Equation 2-7 and Equation 2-12, R_{LED} can be calculated as:

Equation 2-13 $$R_{LED} = R_{SENSE} \cdot \frac{V_{F\_LED}}{V_{REF}}$$

Forward voltage of LED (V_{F_LED}) can be found the datasheet and is usually in the range of 2V to 3.3V depending upon the current capacity and colour.

For PWM modulator and power stage gains can be implemented using voltage controlled voltage source (VCVS) or a simple ideal gain element if available in the simulator’s ideal component library.

Once circuit is modelled, stability analysis can be performed by breaking the loop (to get the open loop transfer function). In, the loop is broken at output and should be at the output ac input of amplitude 1 is applied at v_{in_ac}.

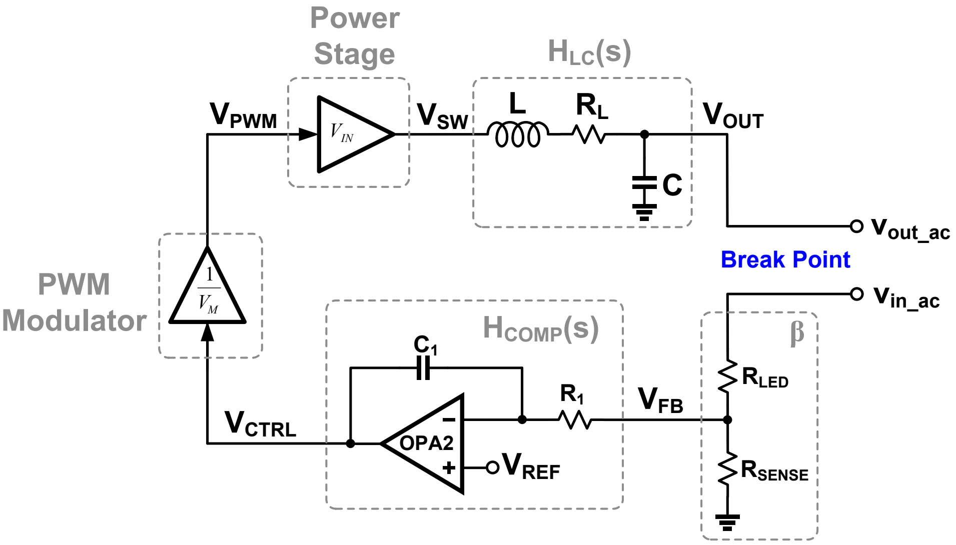


Figure 2-19 Breaking the loop for stability analysis

Since open loop transfer function is needed only for ac and dc operating points of the circuit should not be disturbed after opening the loop. In order to preserve the dc operating point of the circuit, loop is broken in such a way that it should behave like closed loop for dc but open loop for ac. This can be achieved by breaking the loop using inductor and capacitor as shown in Figure 2-20. Since inductor behaves like a short circuit at dc and capacitor as open circuit, loop will remain closed at dc. While for ac inductor behaves as open and capacitor as short, loop will open for ac.

Values L_{break} and C_{break} should be large (order of Mega Henry and Mega Farad) so that they don't interference with actual ac response of the circuit.

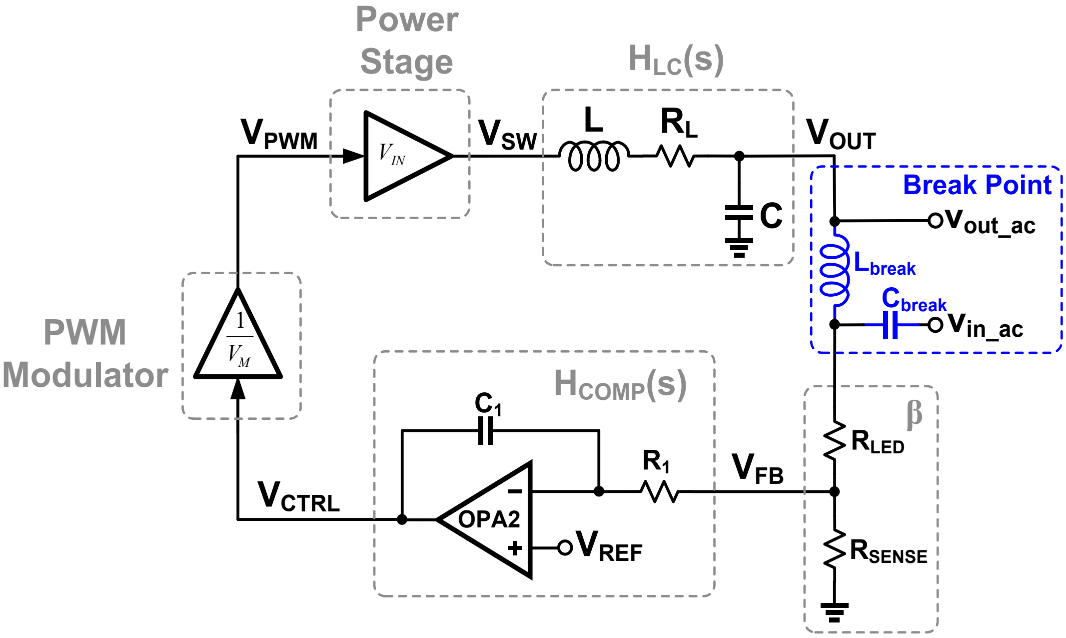


Figure 2-20 Breaking the loop using L and C

Stability of the circuit is checked by looking at the phase margin. Phase margin is defined as (phase difference of total loop phase shift from 0 or 360 degrees at unity gain (0dB). The frequency at unity gain is called unity gain bandwidth (F_{UGB}). Even though a system with > 0 degree phase margin is theoretically stable, in phase margin of a stable system should be greater than 45 degrees. However, it is recommended to have the phase margin ≥ 60 degrees and gain margin < -20dB for better transient response (without any ringing in the output).

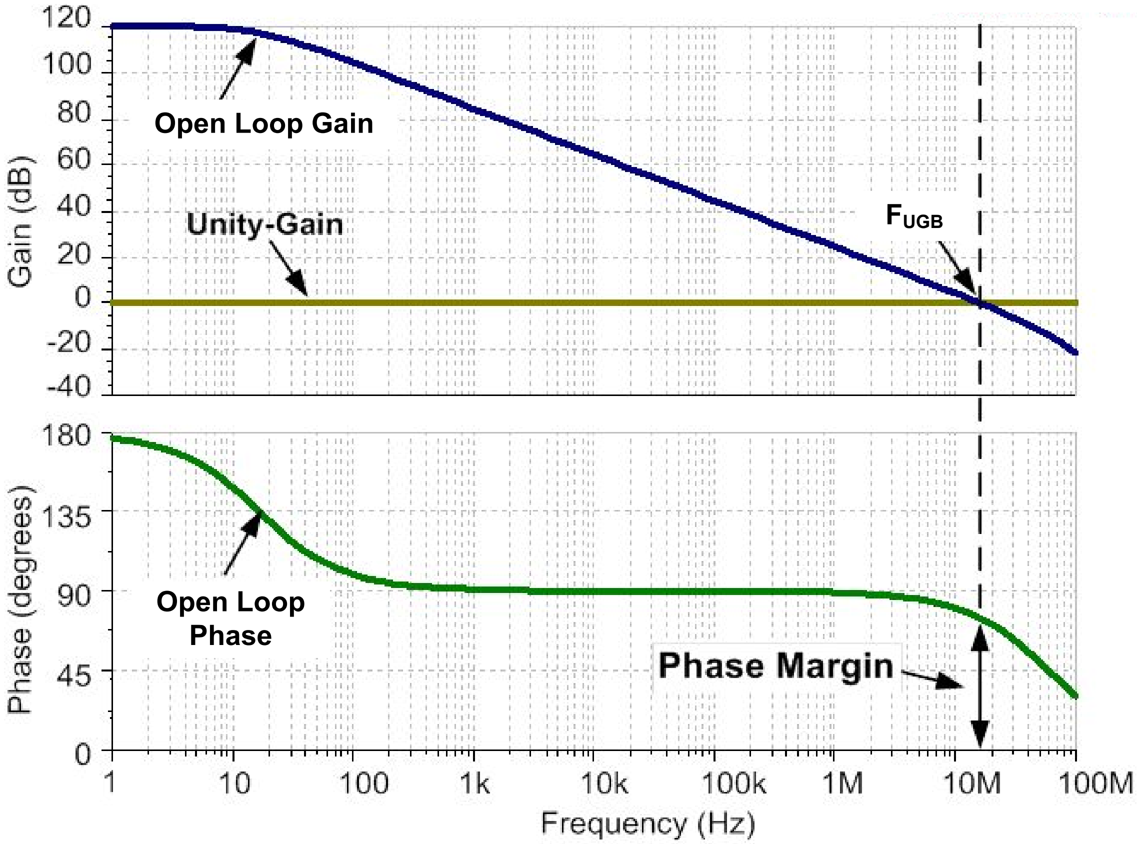


Figure 2-21 Phase Margin of a feedback system

Specifications

- Supply voltage (V_{IN}=V_{DD}) = 5V
- Phase Margin > 60 Degree
- I_{OUT} (I_{LED}) = 50mA
- R_{SENSE} = 5 Ohm

List of Components

- Op-Amp (OPA2): MCP6004 or equivalent
- Inductor (L=100uH): RCH875NP-101K
- LED: 151053YS04500
- Sense Resistor (R_{SENSE}=5Ω): MOSX1CT52R5R1J

List of Measurements

1. Set V_{DD}=V_{IN}=5V, connect V_{REF} to power supply and set V_{REF}=0V
2. Verify that V_{OUT}=0V, LED is OFF (I_{OUT}=0) and there is no switching i.e., V_{PWM}=V_{SW}=0. Measure V_{CTRL}.
3. Slowly increase V_{REF} to a value (few mV) where LED starts turning ON. Measure and plot V_{OUT}, V_{FB}, V_{RAMP}, V_{CTRL}, V_{PWM} and V_{SW}. Verify that PWM duty cycle, D = (V_{CTRL}-V_{RAMP_MIN})/V_M = V_{OUT}/V_{IN}
4. Repeat step 3 for V_{REF} = 0V, 50mV, 100mV, 150mV, 200mV and 250mV. Measure the LED current and observe change in LED brightness.
5. Turn OFF V_{REF} first and then V_{IN}.
6. Use function generator to supply V_{REF}. Select square wave of amplitude 250mV (with low level=0V and high level=250mV), frequency = 1Hz, duty cycle = 25%
7. Set V_{IN}=5V and turn on V_{IN} power supply first and then V_{REF} from function generator. Observe blinking LED light. Increase duty cycle if LED does not blink. Measure and capture V_{OUT}, V_{FB}, V_{RAMP}, V_{CTRL}, V_{PWM} and V_{SW}.
8. Now turn OFF V_{REF} from function generator and set it to sinusoid with frequency 1Hz and pk-pk amplitude 250mV (Vmin=0V, Vmax=250mV).
9. Turn ON V_{REF} and observe LED light. It should follow the sinusoid pattern. Capture voltages V_{OUT}, V_{FB}, V_{CTRL}, V_{PWM} and V_{SW} for one cycle of sinusoid.
10. Sweep the sinusoid frequency from 1 Hz to 1KHz and observe LED light. Does LED stop blinking at higher frequency? What is that frequency?

Pre-Lab Exercise

1. For the LED driver in Figure 2-17, Find the loop gain transfer function with and without type-I compensator. Calculate the values of R_1 and C_1 of the compensator for phase margin > 60 degrees and gain margin = -20dB. Use continuous time model (Equation 2-6, Equation 2-7, Equation 2-11, Equation 2-12, Equation 2-13 and Figure 2-18).
2.
3. Calculate V_{REF} for LED current of 10mA, 25mA and 50mA. If V_{REF} is fixed at 250mV, how will you program the LED current to 10mA, 25mA and 50mA?
4. Design switching LED driver shown in Figure 2-17 and perform the AC or stability analysis using simulation (see Figure 2-19, Figure 2-20 and Figure 2-21). Capture AC magnitude and phase response with and without compensator.
5. Perform measurements 1-10 on simulation. Observe LED current. Capture all the graphs. In case LED model is not available in LTSpice then use multiple PN junction diodes connected in series to get the LED forward voltage.

Chapter 3 Class-D Audio Amplifier

Class-D amplifier module is same as EE3703: Analog Circuits Lab with few minor changes. Details about class-d amplifier can be found at:

http://www.ee.iitm.ac.in/vlsi/courses/ec330_2011/finalproject/classdamp

References:

1. Wikipedia article
2. Notes on Class D amplifier from Georgia Institute of Technology
3. Notes from Elliott Sound Products
4. Brett Forejt, Vijay Rentala, Jose Duilio Arteaga, and Gangadhar Burra, "A 700+-mW Class D Design With Direct Battery Hookup in a 90-nm Process," *IEEE Journal of Solid-State Circuits*, Volume 40, Issue 9, Sep. 2005, pp. 1880-1887.
5. Varona et al., "A Low-Voltage Fully-Monolithic ΔΣ-Based Class-D Audio Amplifier," *Proceedings of the 1999 European Solid State Circuits Conference*, pp. 545-548. (This has an example of switch sizing. This is not the type of class D amplifier you are required to design)
6. Putzeys B., "Digital audio's final frontier," *IEEE Spectrum* vol. 40, no. 3, Mar. 2008. pp. 34-41.
7. Berkhout M., "Audio at low and high power," *Proceedings of the 2008 European Solid State Circuits Conference* pp. 40-49.
8. Application notes from companies
    a. Texas Instruments: http://www.ti.com/audio/ (e.g. Class-D LC Filter Design, 07 Jan 2008; TPA3101D2 Mono Amplifier Configuration, 16 Apr 2007)
    b. Maxim Integrated Circuits: http://www.maxim-ic.com/appnotes.cfm/appnote_number/3977 (The bridged three level topology shown here may be a bit confusing. See the TI datasheet for a simpler topology-logically they are the same)
    c. Analog Devices: http://www.analog.com/library/analogDialogue/archives/40-06/class_d.html
    d. International Rectifier: http://www.irf.com/product-info/audio/classdtutorial.pdf
    e. http://www.infineon.com/dgdl/an-1071.pdf?fileId=5546d462533600a40153559538eb0ff1

List of Difference between EE3703 and EE2019 Class-d Amplifier:

Parameters	**EE2019 Class-d**	**EE3703 Class-d**
PWM Frequency	100KHz	300KHz
Ramp Generator	Op-Amp and Comparator based (used from experiment-1)	BJT based

EXPERIMENT-4: SINGLE ENDED-TO-DIFFERENTIAL INPUT CONVERTER AND PWM MODULATOR

Circuit Diagram:

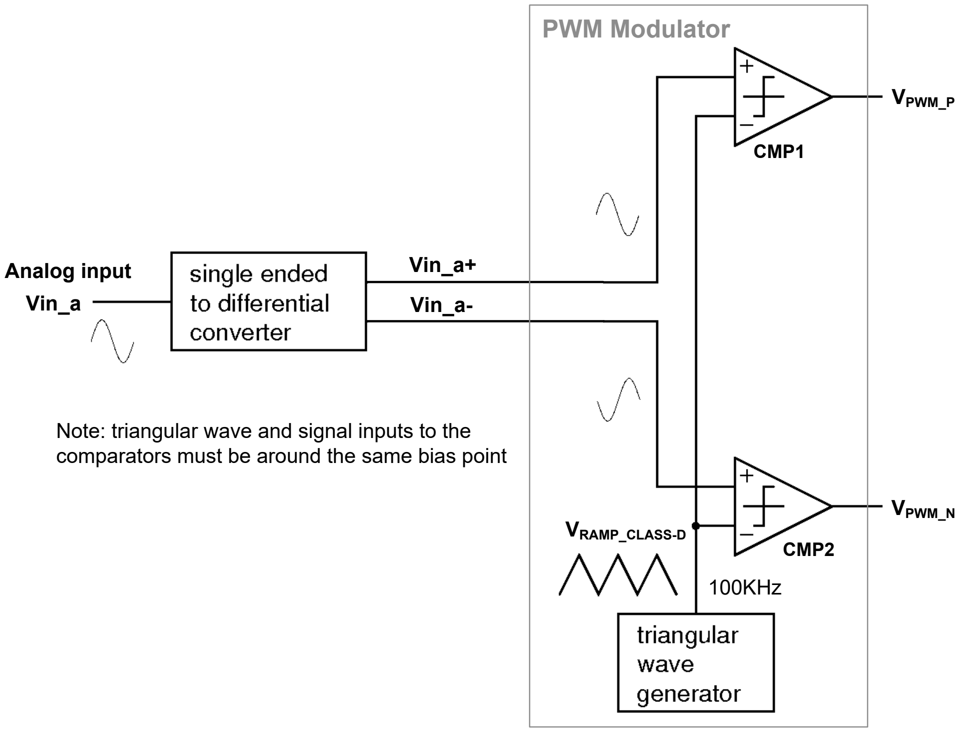


Figure 3-1 Block diagram of single ended-to-differential converter and PWM modulator

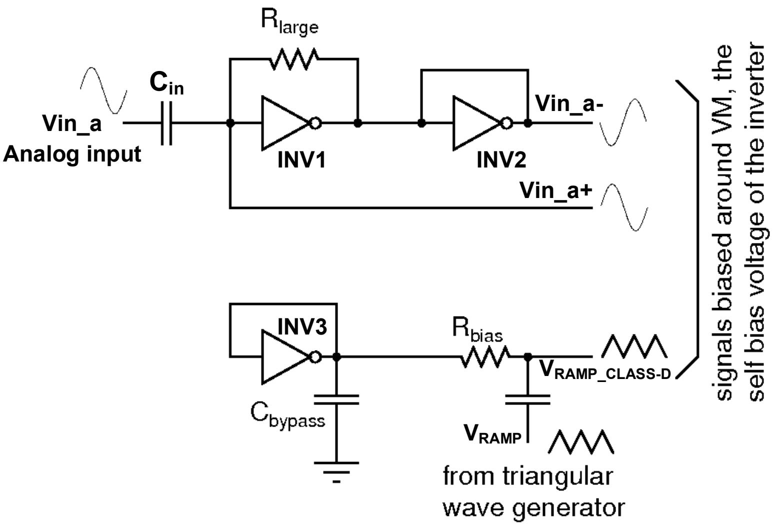


Figure 3-2 Circuit diagram of single ended-to-differential converter

Single ended-to-differential converter can also be designed using op-amp based inverting amplifier as shown in Figure 3-3.

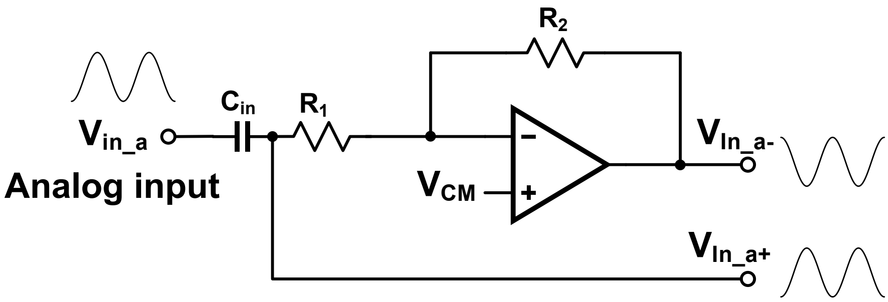


Figure 3-3 Circuit diagram of single ended-to-differential converter using op-amp

Input capacitor in both Figure 3-2 and Figure 3-3 should be large enough to make sure input audio signal is not attenuated.

For R_1=R_2:

$$V_{in\_a+} = V_{in\_a}\,(ac) + V_{CM}$$

$$V_{in\_a-} = -V_{in\_a}(ac) + V_{CM}$$

Since outputs (V_{in_a+} and V_{in_a-}) and V_{RAMP} are biased around V_{CM}, common mode shifting of VRAMP is not needed. Therefore $V_{RAMP\_CLASS\text{-}D}$ can be directly connected to V_{RAMP}. In case common mode of V_{RAMP} is not V_{CM} then it must be shifted to V_{CM} by using a coupling capacitor and resistor as it was done in Experiment-1 (Figure 2-14) to generate V_{RAMP_B}.

Specifications

- Supply voltage (V_{IN}=V_{DD}) = 5V
- PWM Frequency = 100KHz

List of Components

- CMP1 and CMP2: LM339 (open collector – requires a pullup resistor between V_{DD} and V_{OUT})
- INV1, INV2 and INV3: MC14069

List of Measurements

1. Set V_{DD}=V_{IN}=5V
2. From function generator, set sinusoid wave of 1kHz and use as input to single ended-to-differential converter. Peak-to-peak amplitude of the sinusoid should be same as peak-to-peak amplitude of the triangular wave.
3. Measure amplitude and frequency of waveforms at input, Vin+ and Vin-. Capture oscilloscope waveform and verify that Vin+ and Vin- are 180 degrees out of phase and have same amplitude as input.
4. Measure and capture duty cycle at V_{PWM_P} and V_{PWM_N}. Duty cycle should follow the same pattern as Vin_a+ and Vin_a-. Verify that V_{PWM_N} has inverter duty cycle (1-D) of V_{PWM_P} (D).
5. Add an RC filter at V_{PWM_P} and V_{PWM_N} with 3dB cut-off frequency of 10-20KHz and observe the output. Verify that output has the same shape as Vin_a+ and Vin_a-.

Pre-Lab Exercise

1. Drive the expression for Vin+ and Vin- in terms of input and prove that Vin+ and Vin- have sane amplitude but of opposite polarity.
2. Find the expression for differential PWM signal, V_{PWM_P}-V_{PWM-N} and prove that average output is amplified version of analog input to single ended to differential converter. Find the gain of amplifier.
3. Build the complete circuit shown in Figure 3-1 and Figure 3-2 in LTSpice. Verify the functionality in simulation with measurements 1-5.

EXPERIMENT-5: H-BRIDGE DRIVER AND INTEGRATION

Circuit Diagram:

Figure 3-7 shows the circuit diagram of half-bridge driver. The driver is the output stage of class-D amplifier and is the key to obtaining good efficiency. The switches (Qp and Qn) of the half-bridge driver are implemented using NPN and PNP transistors and driven with CMOS inverter buffers. Use a base resistance (bases of Q_p and Q_n) of a few kilohms to limit the base current. If you find that the drive is insufficient (i.e. the transistors don't saturate with a heavy load), reduce the base resistances so that they saturate. If you find that the drive is still not sufficient, you can omit the base resistor, and connect two inverters in parallel to drive the base of the transistors. The non-overlap generator can be designed using the circuit in experiment-2 or the one shown in Figure 3-5.

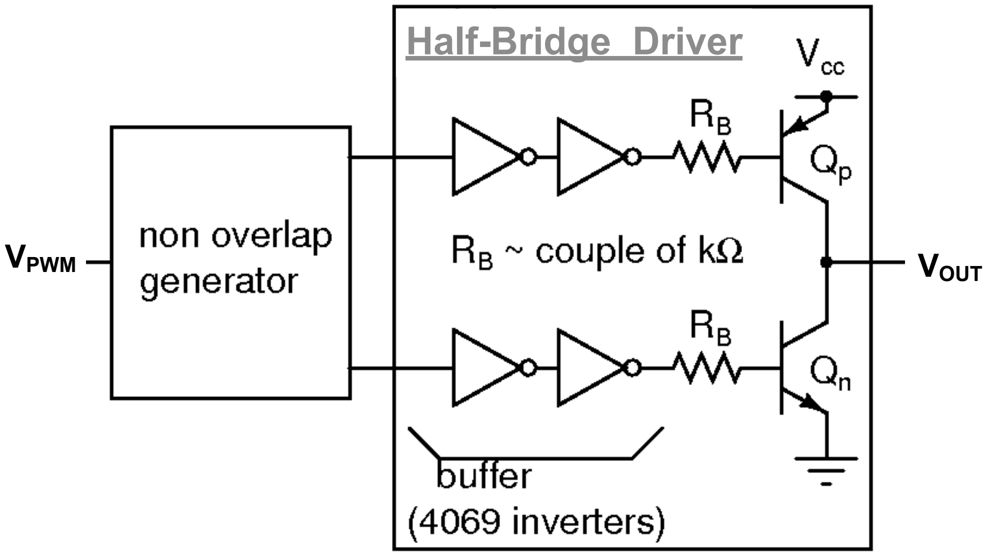
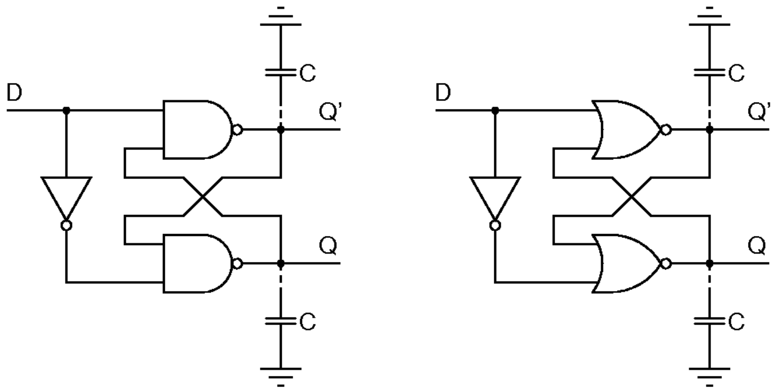


Figure 3-4 Half-bridge speaker driver



Non overlap generator-an additional inversion is necessary on one of the inputs to drive the p and n switches

Figure 3-5 Non-overlap clock generator

In order to test the half-bridge circuit, V_{PWM} from one of the PWM modulators (V_{PWM_P} or V_{PWM_N}) of experiment-4 can be used as input. VOUT can be initially tested without load and then 32Ω resistive load is applied.

For simulation, actual electrical model of speaker can be used as shown in Figure 3-6. L is the coil inductance which is usually within the range of few 100s to a 1000 uH depending upon the size of coil. R_L is coil resistance which depends upon power rating of the speaker.

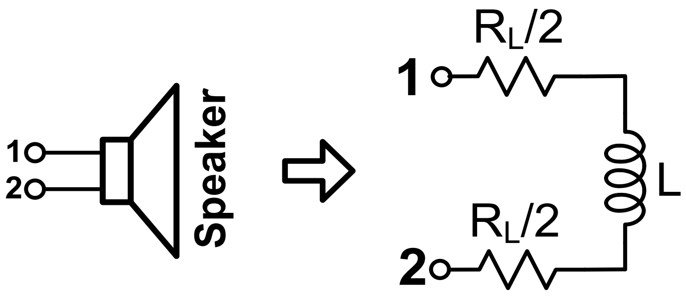
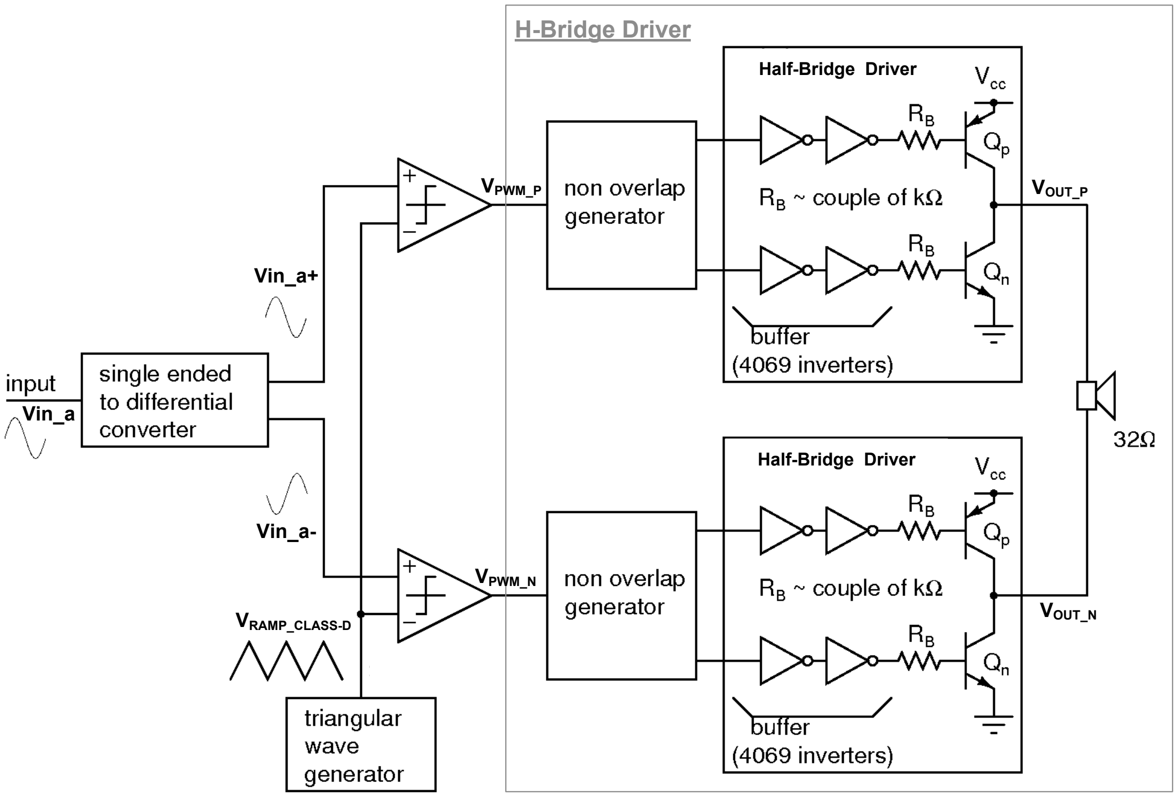


Figure 3-6 Electrical model of a speaker

Figure 3-7 shows the circuit diagram of complete class-d amplifier. The PWM output from single ended to differential converter and PWM modulator designed in experiment-4 is fed to H-Bridge driver which drives the speaker load. H-bridge driver consist of two identical half-bridge drivers. The complete class-D amplifier should be tested with resistive load first and then actual speaker.



Note: triangular wave and signal inputs to the comparator must be around the same bias point

Figure 3-7 Circuit diagram of the complete class-d amplifier

Specifications

- Supply voltage (V_{IN}=V_{DD}) = 5V
- PWM Frequency = 100KHz
- Load Resistance (R_L) = 32Ω

List of Components

- CMP1 and CMP2: LM339 (open collector – requires a pullup resistor between V_{DD} and V_{OUT})
- Inverters: MC14069 or CD4069
- NAND Gates: SN74AHC00N
- BJTs: 2NXXXX series or alternate parts

List of Measurements

1. Set V_{DD}=V_{IN}=5V, R_L=32 Ω
2. From function generator, set sinusoid wave of 1KHz and use as input to single ended-to-differential converter. Peak-to-peak amplitude of the sinusoid should be same as peak-to-peak amplitude of the triangular wave.
3. Measure and capture duty cycle at V_{OUT+} and V_{OUT-}. Duty cycle should follow the same pattern as Vin_a+ and Vin_a-. Verify that V_{OUT-} has inverter duty cycle (1-D) of V_{OUT+} (D).
4. Add an RC filter at V_{OUT+} and V_{OUT-} with 3dB cut-off frequency of 10-20KHz and observe the output. Verify that output has the same shape as Vin_a+ and Vin_a-. RC filter is only to observe the average value of output hence should not be in the load path (i.e. load should be connected directly between V_{OUT+} and V_{OUT-}).
5. Verify 2-4 with speaker and do hearing test. Reduce the amplitude of input sinusoid and observe the change in sound level. Repeat hearing test for 5 different frequency tones between 0.5KHz to 5KHz and observe the sound.

NOTE: capture oscilloscope waveform only for one condition to show the functionality of circuit.

Pre-Lab Exercise

1. Build the complete circuit shown in Figure 3-1 and Figure 3-2 in LTSpice. Verify the functionality by simulation with measurements 1-5. Use speaker model from Figure 3-6 as load and plot current through inductor. Inductor current should be average of differential output voltage (V_{OUT_P}-V_{OUT_N}) divided by R_L.

Chapter 4 Analog Filter, Adder and Peak Detector

Introduction and Circuit Diagrams

Analog filters are used to pass desired frequency signals and reject other frequencies. The objective of this module is to design a second order high-Q bandpass filter which will pass only a fixed frequency audio tone. Output of the filter is used as input signal to LED driver and class-D amplifier at later stage when we integrate all the modules and build complete system.

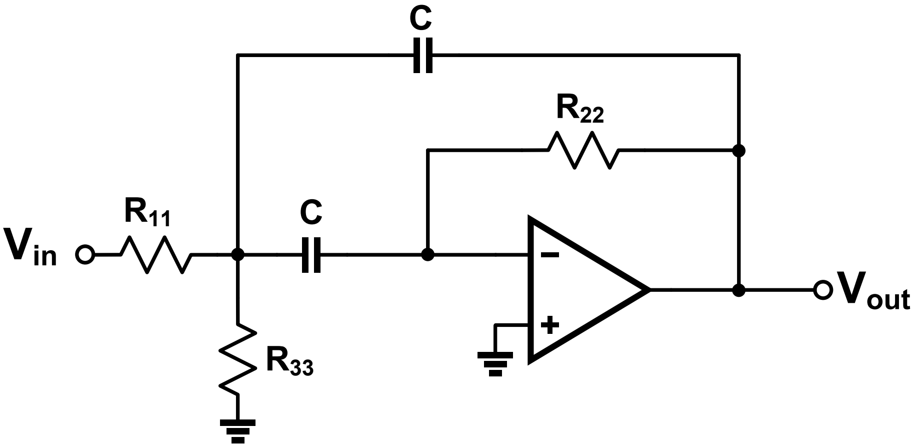


Figure 4-1 A second order bandpass filter

For basic theory and different types of filter, refer to the following documents:

- http://www.ti.com/lit/an/sbfa001c/sbfa001c.pdf
- https://focus.ti.com/lit/ml/sloa088/sloa088.pdf

For multiple frequency tones, multiple filters, centred at different frequencies, can be used. Filter outputs can be added using an inverting adder shown in Figure 4-2.

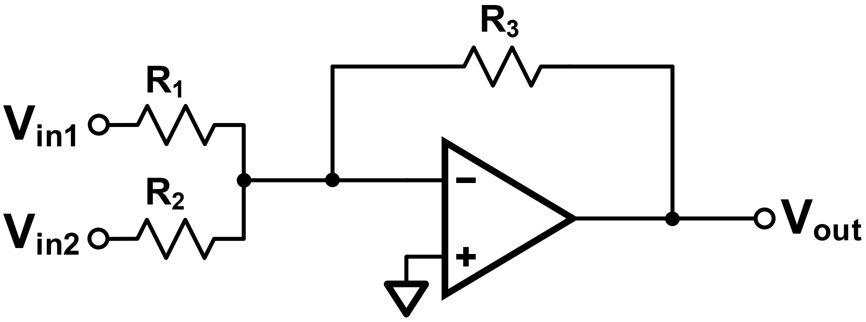


Figure 4-2 An opamp based adder

The output voltage of adder can be expressed as:

Equation 4-1 $$V_{out} = -\left(\frac{R_3}{R_1}V_{in1} + \frac{R_3}{R_2}V_{in2}\right)$$

If $R_1=R_2=R_3$ then:

Equation 4-2 $$V_{out} = -(V_{in1} + V_{in2})$$

Since, reference voltage to LED driver is dc, the ac output signal of the above bandpass filter must be converter to dc using a peak detector. Following document provides detailed description about the peak detector circuit.

- http://ww1.microchip.com/downloads/en/AppNotes/01353A.pdf

Figure 4-3 shows the circuit of a basic peak detector. It is based on a half-wave rectifier (AC-to-DC converter). Since V_{IN} must be greater than forward voltage of diode (D1) for conduction, the circuit does not work for input voltages lower than diode forward voltage (~0.7V).

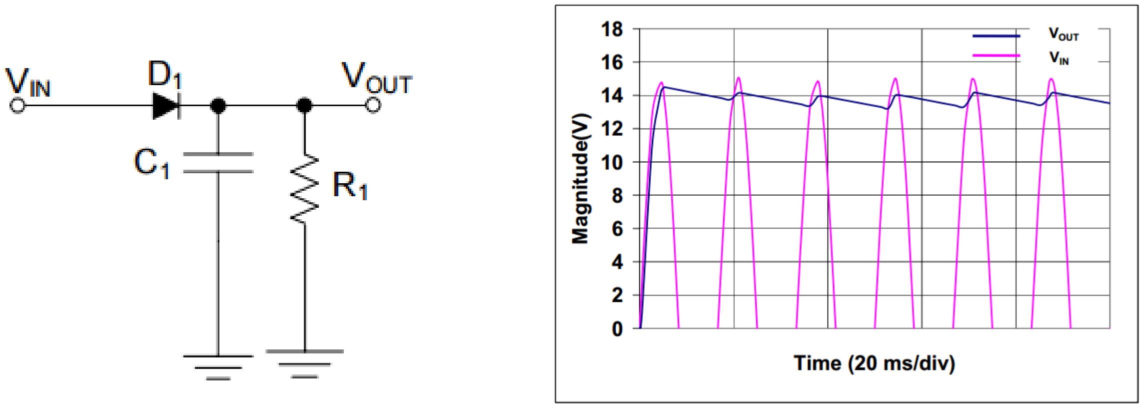


Figure 4-3 A basic peak detector curcuit

An op-amp based peak detector shown in Figure 4-5 is used in this module. First order high pass filter (R1-C1) is used to de-couple any dc bias of the input Vin. Feedback from Vpeak to op-amp inverting input ensures that D1 is always conducting for positive voltage of Vin_ac. Since diode remains reverse biased for negative voltage, capacitor (C2) holds the peak value of Vin_ac at Vpeak.

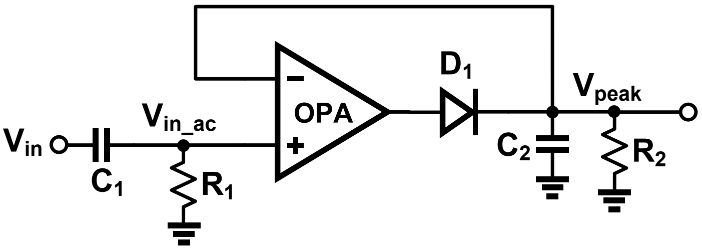


Figure 4-4 Op-amp based peak detector curcuit

Resistors R2 provides the discharge path to Vpeak so that output voltage can be reduced if amplitude of the input is reducing. The discharge rate of Vpeak depends upon the RC time constant defined as: $\tau = R2 \cdot C2$ and must be chosen high enough to ensure low ripple at Vpeak and low enough so that Vpeak can track any slow changes in the input signal amplitude. Generally, time constant (τ) is kept around 10 times of the time period of input signal.

The dc voltage obtained at Vpeak may have higher voltage than the maximum specified value of V_{REF} in the LED driver. Peak detector circuit of Figure 4-4 can be modified by splitting R2 into R2-R3 to form a voltage divider. The desired level of V_{REF} can be achieved by adjusting the values of R2 and R3. The values of R2+R3 should be order of 10s of KOhms or higher as lower values may cause current drawn from op-amp output higher than its drive capability. Maximum output current of the op-amp can be checked from the datasheet before selecting the values of R2 and R3.

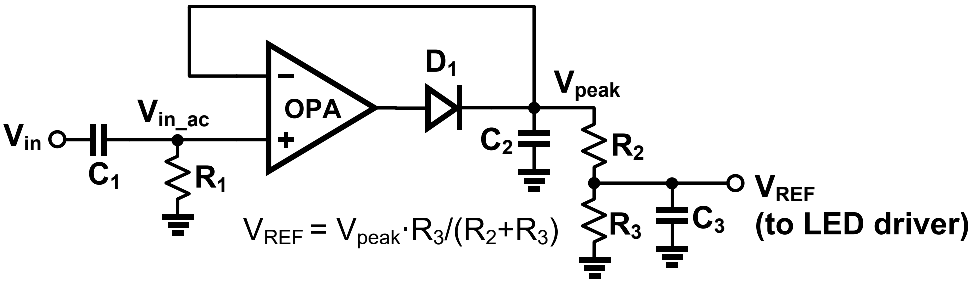


Figure 4-5 Modified op-amp based peak detector curcuit

Capacitor (C3) can also be added at V_{REF} to filters out the ripple further and get a cleaner dc voltage.

EXPERIMENT-6: BANDPASS FILTER

The objective of experiment-6 is to design two different bandpass filters in Figure 4-6. Audio input (Vin_audio), which is a fixed frequency sinusoid tone, is used as input to the bandpass filter. Each bandpass filter is designed to respond to a desired frequency tone and reject other frequencies.

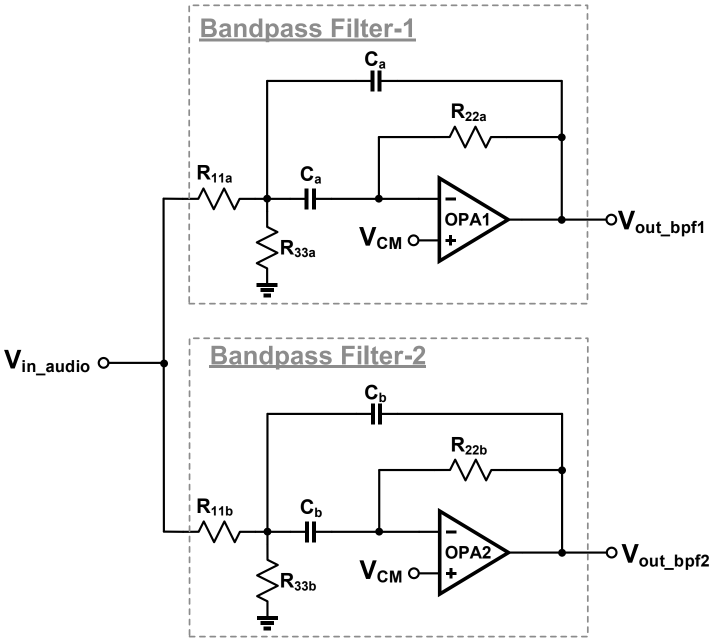


Figure 4-6 Bandpass Filters

Specifications

- Supply voltage: V_{DD}=5V
- $V_{CM}=V_{DD}/2$=2.5V
- Bandpass filter Gain (Ao1=Ao2)=1 (0 dB)
- Bandpass filter Q-factor (Qo1=Qo2) = 10
- Bandpass Filter-1 center frequency (fo1) = 1kHz, Bandpass Filter-2 center frequency (fo2) = 3kHz

List of Components

- OPA1 and OPA2: MCP6004 (Op Amps Quad 1.8V 1MHz)

List of Measurements

1. Set V_{DD}=5V, V_{CM}=2.5V
2. Tune Bandpass Filter-1 center frequency (f_{o1}) = 1kHz, Bandpass Filter-2 center frequency (f_{o2}) = 3KHz, gain (Ao1=Ao2)=1 and Qo1=Qo2=10.
3. From function generator, set sinusoid wave of 1kHz and use as input to bandapss filters (Vin_audio). Peak-to-peak amplitude of the sinusoid should be 0.9 times of peak-to-peak amplitude of the ramp signal of experiment-1.
4. Measure and capture the output of bandpass filters (Vout_bpf1 and Vout_bpf2) and verify the amplitude as per the filter response. Reduce the amplitude of Vin_audio and verify that

Vout_bpf1 follow the change in amplitude. Set the amplitude back to its maximum value (0.9xVm)

5. Change the frequency of Vin_audio to 3kHz and repeat 4.
6. Now sweep the frequency of Vin_audio from 100Hz to 5kHz) and verify that Vout_bpf1 and Vout_bpf2 do not respond to any other frequencies except their respective center frequencies (fo1=1kHz and fo2=3kHz)

Pre-Lab Exercise

1. Derive the transfer function of bandpass filter shown in Figure 4-1 and prove that it is a second order bandpass filter having transfer function equivalent to: $\mathrm{H}(s) = \frac{A_o \cdot \frac{w_o}{Q_o} \cdot s}{s^2 + \frac{w_o}{Q_o} s + w_o^2}$. Find the values of resistors and capacitors for BPF-1 and BPF-2 based on values (Ao, fo and Qo) provided in the Specifications.
2. Simulate and perform measurement 3-6. Capture all the plots and mark values.

NOTE:

- Center frequencies (fo1 and fo2) may be slightly off from simulation results when implemented on breadboard. This is mainly due to the tolerance in resistors and capacitors. In that case, you can tune the frequency of Vin_audio to match the center frequency of the bandpass filter. Exact center frequency of BPF-1 (fo1) can be found by sweeping the frequency of Vin_audio around 1kHz and look for the maximum amplitude of Vout_bpf1. Similarly , Exact center frequency of BPF-2 (fo2) can be found by sweeping the frequency of Vin_audio around 3kHz and look for the maximum amplitude of Vout_bpf2.

EXPERIMENT-7: ADDER and PEAK DETECTOR

The objective of experiment-7 is to add the band pass filtered signals (V_{out_bpf1} and V_{out_bpf2}) from experiment-6 and converter the added signal into a dc voltage (V_{REF}) using peak detector.

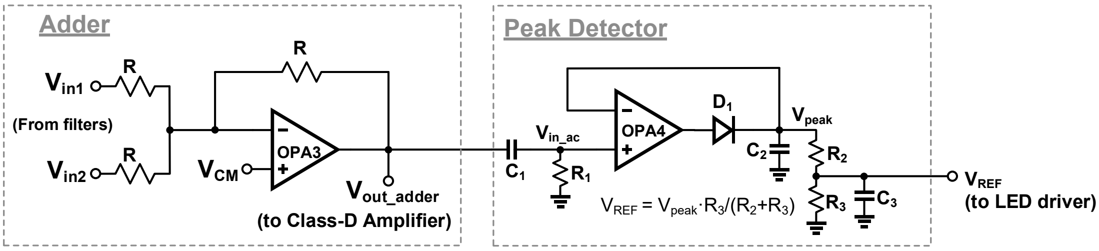


Figure 4-7 Adder and Peak Detector

Specifications

- Maximum peak-to-peak ripple at Vpeak = 100mV
- Maximum peak-to-peak ripple at V_{REF} = 10mV
- Maximum peak to peak amplitude of Vin1 and Vin2 = 0.9xVm (Vm is the peak-to-peak amplitude of the ramp signal obtained from experiment-1 at V_{DD}=5V)
- Maximum value of V_{REF} (for maximum amplitude of Vin1 and Vin2) = 250mV

List of Components

- OPA3 and OPA4: MCP6004 (Op Amps Quad 1.8V 1MHz)
- D1: 1N4148TR (Diodes - General Purpose)

List of Measurements

1. Set V_{DD}=5V, V_{CM}=2.5V
2. From function generator, apply sinusoid wave of amplitude=0.9xVm, frequency=1kHz at Vin1 and Vin2 with common mode (dc offset) set at 2.5V.
3. Measure and capture the output of adder (Vout_add) and verify that:

$$V_{out\_add} - (V_{in1} + V_{in2})$$

4. Plot Vin_ac and verify that signal is biased around 0V.
5. Change the frequency of input sinusoid to 3kHz and repeat 3 and 4.
6. Measure and plot Vpeak average and peak to peak ripple. Verify that average is approximately same as peak level of Vin_ac and prak-to-peak ripple is within the specification (100mV).
7. Measure and plot V_{REF} and verify the average value is 250mV and ripple is within 10mV.
8. Reduce the amplitude of Vin1 and Vin2 and verify that Vout_add and V_{REF} follow the change in amplitude.
9. Now connect Vin1 to the output of Bandpass Filter-1 (Vout_bpf1) and Vin2 to Bandpass Filter-2 output (Vout_bpf2). From function generator, apply sinusoid wave of 1kHz as input to bandapss filters (Vin_audio). Peak-to-peak amplitude of the sinusoid should be 0.9 times of peak-to-peak amplitude of the ramp signal of experiment-1. Repeat measurement 6 and 7. Reduce the amplitude of Vin_audio and verify that Vout_add and V_{REF} follow the change in amplitude.
10. Change the frequency of input sinusoid to 3kHz and repeat 9.

11. Now sweep the frequency of Vin_audio from 100Hz to 5kHz) and verify that Vout_ac amplitude is 0.9xVm and V_{REF} is 250mV at frequencies 1kHz and 3kHz but remain very low (~0V) at other frequencies.

Pre-Lab Exercise

1. Calculate the values of R, R1, R2, R3, C1, C2 and C3 for the frequency and ripple provided in the Specifications.
2. Design and simulate the entire circuit shown in Figure 4-7 with above calculated values. Verify the operation with measurements 1 to 11.

NOTE:

- The gain of the bandpass filter at center frequency should be unity. If not then adjust the value of R_{11}. Alternatively, the gain can be changed by selecting proper values of values of R1, R2 and R3 in the adder (Figure 4-2).

- The center frequencies (fo1 and fo2) may be slightly off from simulation results when implemented on breadboard. This is mainly due to the tolerance in resistors and capacitors. In that case, you can tune the frequency of Vin_audio to match the center frequency of the bandpass filter. Exact center frequency can be found by sweeping the frequency of Vin_audio around 1KHz and look for the maximum amplitude of Vout_bpf.

EXPERIMENT-8: SINGLE ENDED-TO-DIFFERENTIAL INPUT CONVERTER USING OP-AMP

Replace inverter based single ended-to-differential converter (Figure 3-2) in Experiment-4 with opamp (MCP6004) based on single ended-to-differential converter (Figure 3-3) and repeat Experiment-4 & 5.

Chapter 5 Top Level Integration

Top level integration combines all the four modules (LED Driver, Class-D Amplifier, Filtes and Adder+Peak Detector designed during experiments 1-7) to build the complete system. Figure 5-1 shows the block diagram of the complete system after integrating all the modules.

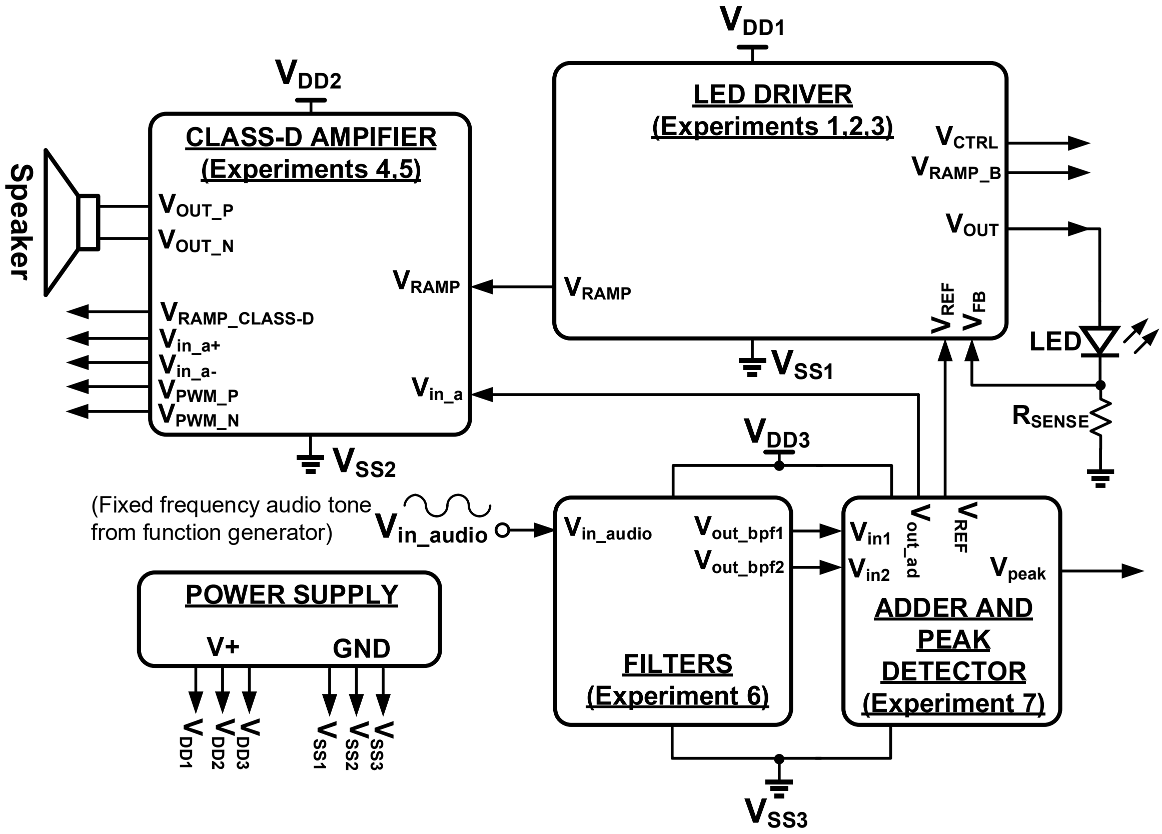


Figure 5-1 Block diagram of the complete system after integration

Vin_audio is a fixed frequency audio tone generated from function generated as it was used in experiment-6 and 7. All the interface signals going from one module to other should be connected properly. In order to prevent noise coupling from one module to other, V_{DD} and GND (V_{SS}) of each module should be connected directly to power supply and not shorted locally on the breadboard. If required, decoupling capacitors of few µF can be connected locally between VDD and GND of each module. If analog modules (non-switching) within the modules are affected from switching noise then VDD and GND of each analog module can be separated as well and connected directly to the power supply.

Integration Guidelines

1. Makes sure all the individual modules are working before integrating them together.
2. Before starting board level integration, integrate all the modules together on LTSpice and verify the functionality.
3. Label all the signals shown in the block diagram of Figure 5-1 using a small piece of paper and tape. Wires connecting to these labelled signals should be brought to for measurement. Rest of the signals can left inside the board.
4. Try to use different colour wires for VDD, GND and signals. For example, red can be used for VDD, black from GND and other colours for signals.
5. Putting tape around the circuits may help in keeping the connections intact. Signal wires which are brought out for measurement can also be fastened locally on board using tape to protect from popping out of the holes.
6. V_{DD} and GND (V_{SS}) of each module should be connected directly to power supply and not shorted locally on the breadboard. If required, decoupling capacitors of few µF can be connected locally between VDD and GND of each module.
7. Check the short between VDD, GND and signals before turning the power supply ON.
8. Limit the power supply current to prevent the circuit from damaging in case of accidental short. Usually current limit is set slightly higher (1.5x or so) than the maximum total current drawn by the circuits.

Final Demo

Final demo will be based on both LTSpice and board level design. Students will not be given extra time to work on circuits on the day of final demo hence all students should have their modules ready before start of the demo. Students will be asked to demonstrate following:

1. LTSpice simulation results. Must be implemented individually by each group mate.
2. Hardware functionality demo (in group).
3. Probe signals listed in Figure 5-1.
4. Capability of operating instruments used in EE2019 lab (oscilloscope, power supplies, function generator etc.)
5. Answering questions related to circuits designed in EE2019 lab experiments.