Design of a High Speed High Resolution Continuous-Time Delta Sigma Modulator

A THESIS

submitted by

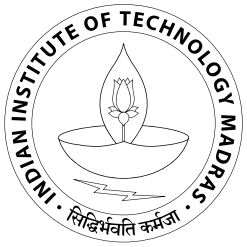
VIKAS SINGH

for the award of the degree

of

MASTER OF SCIENCE

(by Research)



Department Of Electrical Engineering

Indian Institute of Technology Madras, India

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CERTIFICATE

This is to certify that the thesis titled **Design of a High Speed High Resolution Continuous-Time Delta Sigma Modulator** , submitted by **Vikas Singh**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Data converters are key components of almost any electronic system. Since the real world is inherently analog and the trend in telecommunication, voice, video, computer and many other applications is to get a digital form of the analog signal to make use of robust, flexible and reliable signal processing, the analog-digital interfaces become critical paths. The most interesting class of data converters is Delta-Sigma ($\Delta\Sigma$) modulators (DSM), which are oversampled noised shaped analog-to-digital converters (ADC). They are closed loop negative feedback converters wherein the quantization noise is high pass filtered by the loop without affecting the input signal strength. They are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators. There are several advantages of implementing the modulator loop-filter with continuous time circuitry such as inherent anti-aliasing property, lower power consumption, higher maximum speed in a given technology. The bandwidth over which a given resolution can be achieved in a DSM is limited by the sampling frequency. For a CTDSM this sampling frequency is limited by the excess loop delay (ELD), which is one of the major concerns in high speed continuous time (CT) $\Delta\Sigma$ modulators. Conventional techniques address the problem of ELD by compensating the modulator only upto half clock cycle delay [1] [2], which limits the sampling rate. Our focus in this work was to come up with various circuit techniques that reduce the delay in the CTDSM loop. For example, to enable modulator operation with greater than a clock cycle delay in the quantizer, we analyze extensively the use of a parallel analog feedback path that bypasses the (slow) quantizer and enables stable modulators with quantizer delay in excess of a clock cycle [3]. Sampling rates hitherto not possible can therefore be achieved. Additionally, a new calibration

technique is introduced that removes the effect of mismatch between DAC cells without adding any extra delay in the loop. The above techniques have been applied to the design of a fourth order CTDSM with a 4 bit quantizer in 0.18 μm CMOS process. Test results of the fabricated chip show 80 dB of dynamic range for a bandwidth of 11 MHz. The modulator has a sampling rate of 600 MHz compared to previously reported maximum of 300 MHz [4]. The power dissipation is 45 mW from 1.8 V supply and occupies an active area of 1mm X 1mm. Measured anti-alias suppression is over 55 dB for input signals in the alias band from 589 MHz to 611 MHz. Since the technique presented here can tolerate quantizer delays of more than one clock cycle, it enables the use of multi-step quantizers, such as subranging or pipelined ADC converters, in $\Delta\Sigma$ modulators.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CMRR	Common Mode Rejection Ratio
CT	Continuous Time
CTDSM	Continuous Time $\Delta\Sigma$ Modulator
DAC	Digital to Analog Converter
DR	Dynamic Range
DSM	$\Delta\Sigma$ Modulator
DT	Discrete Time
ETF	Error Transfer Function
HRZ	Half-Return to Zero
MSA	Maximum Stable Amplitude
NRZ	Non-Return to Zero
NTF	Noise Transfer Function
OBG	Out of Band Gain
OSR	Oversampling Ratio
PSD	Power Spectral Density
RZ	Return to Zero
SFNR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
V_{ppd}	Volts, Peak to Peak Differential
UGF	Unity Gain Frequency

CHAPTER 1

Introduction

1.1 Motivation

In the last ten years there is an immense growth in wireless connectively. For every specific application in communication, a new wireless standard have arisen, which is categorized by the data rate and the range of communication (Fig.1.1). Supporting this multitude of wireless standards has become a significant design challenge in current and future wireless devices.

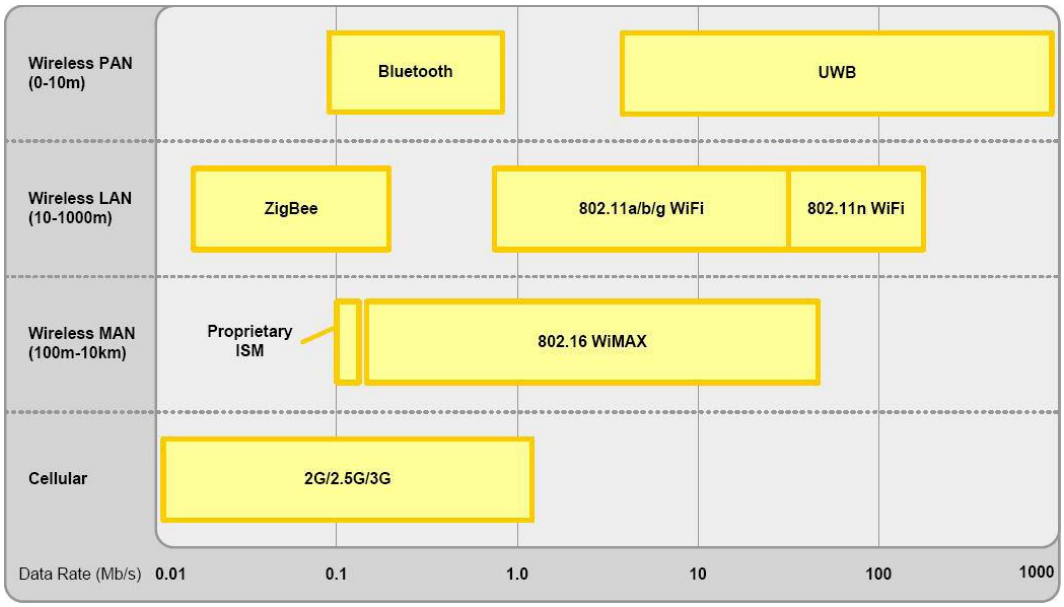

Figure 1.1: Comparison of wireless technologies [5].

An attractive architecture to achieve these goals on the receiver side is shown in Fig. 1.2, which comprises an LNA and IQ Mixer feeding into a wide bandwidth, high resolution analog-to-digital converter (ADC) that has minimal antialias filtering requirements. Channel selective filtering can then be performed in the digital domain, which greatly simplifies multi-standard support. To achieve good receiver

sensitivity and blocking performance with minimal antialias filtering, the ADC must have wide dynamic range and excellent SNDR characteristics. A promising ADC structure to fulfill the above requirements topology is the $\Delta\Sigma$ modulator with multi-bit quantizer.

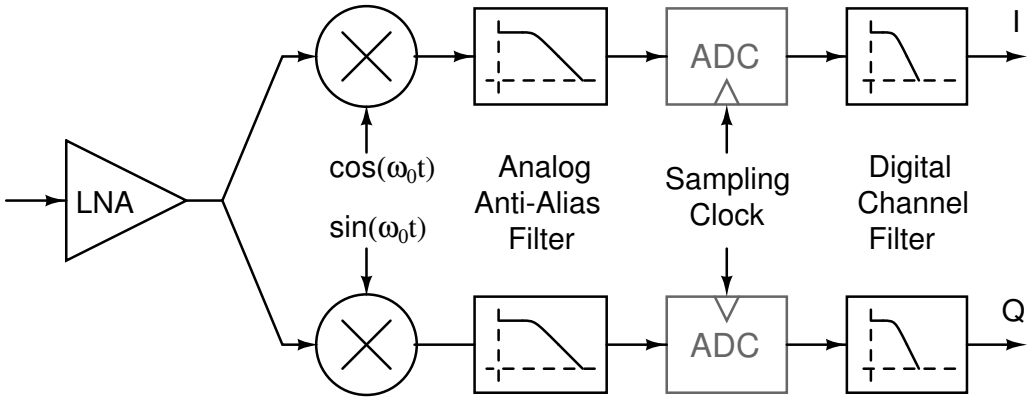

Figure 1.2: A wideband wireless transceiver utilizing a wideband ADC to achieve multi-mode operation.

Delta Sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs) are widely used in wireless applications [9][10] due to their oversampling, high dynamic range, and low power consumption characteristics. They are closed loop converters wherein the quantization noise is high pass filtered by the loop characteristics. Compared with the traditional discrete-time (DT) counterparts, the ADCs that employ continuous-time (CT) technique behave even better in terms of power consumption and allowable input bandwidth [11]-[2]. Continuous-time $\Delta\Sigma$ modulator (CTDSM) does not require high order anti-alias filters, thus further saving power and area. In CTDSMs, the maximum signal bandwidth that can be achieved for a given resolution is limited by the maximum sampling frequency ($f_{s,max}$). In a given technology, $f_{s,max}$ is limited by the excess loop delay (ELD). This prompted us to explore the effect of ELD. In previous works, the effect of ELD is mostly analyzed for ELD $<$ 1 clock cycle [16, 17]. In this work, the effect of ELD for delay $\geq$ 1 clock cycle is analyzed. This forms the major part of this thesis. A new circuit technique to compensate the modulator with ELD $\geq$ 1 clock cycles is investigated [3]. As an extension of the theoretical study, a fourth order modulator intended

for wide-band application and compensated by the new technique to accommodate 1≤ELD<2 clock cycles, has been designed. It operates at 630 MHz and has a signal bandwidth of 11 MHz. The design was implemented in a 0.18 μm CMOS process. Its occupies an active area of 1 mm^2 and the total chip area including 48 pads is 1.5 mm X 1.5 mm. The design consumes a power of 45 mW from a 1.8 V supply and the obtained ENOB is 12 bits with a peak SNR of 72 dB. The dynamic range measured is 80 dB.

1.2 Overview of the thesis

The rest of the thesis is organized as follows.

Chapter 2 provides some basic background knowledge and the challenges in CTDSMs to help understand the rest of the thesis.

Chapter 3 analyzes the effect of excess loop delay on the performance of the modulator and discusses about the conventional methods to compensate this delay. It also describes the proposed CTDSM that can compensate upto two clock cycles of ELD.

Chapter 4 discusses the fourth order loop filter and the topologies of opamps used in the modulator.

Chapter 5 deals with the design of the sample and hold (S/H) and the transconductance cell used to implement the fast loop in the modulator.

Chapter 6 discusses the need of current mode logic (CML) latch in the compara-

tor along with the design of the 4-bit flash ADC.

Chapter 7 deals with the design of 4-bit DAC with the new calibration technique to remove the mismatches in the internal DAC cells.

Chapter 8 Summarizes the design shows the simulation results.

Chapter 9 discusses the floorplan of the modulator and covers the test setup and the measurement results of the test chip.

Chapter 10 concludes the thesis and discusses possible future work.

CHAPTER 2

$\Delta\Sigma$ Modulator fundamentals

The Nyquist theorem states that a signal must be sampled at least twice as fast as the bandwidth of the signal (f_B) to accurately reconstruct the waveform; otherwise, the high-frequency content will alias at a frequency inside the spectrum of interest (passband). The minimum required sampling frequency, in accordance to the Nyquist Theorem, is the Nyquist Frequency ($f_{s,nyqt}$). Fig. 2.1.a shows the multibit ADC which convert analog input signal $y(t)$ to digital output bit stream $v[n]$. Fig. 2.1.b shows the equivalent quantization noise model. The quantization noise power σ_q^2 added by an ADC sampling at $f_s \geq f_{s,nyqt}$ with V_{lsb} as the level spacing, is given by $V_{lsb}^2/12$. The quantization noise is assumed to be white and has a *Power Spectral Density* (PSD) of $\dfrac{\sigma_q^2}{f_s/2}\ V^2/Hz$ and is shown in Fig. 2.2(a). Now if the sampling rate is doubled keeping the f_B same, then the noise PSD will reduce to half (Fig. 2.2(b)), as the total noise power is constant. For every dou-

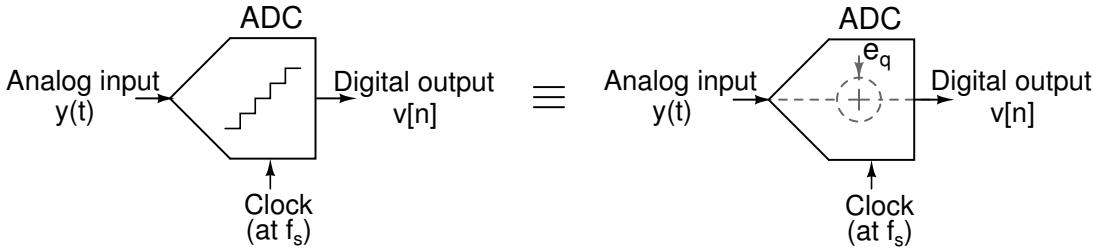

Figure 2.1: (a) ADC (b) Additive quantization noise model.

bling of the sampling rate, the noise reduces by a factor of 3 dB (3 dB/octave). The ratio of sampling frequency f_s to the nyquist rate $2f_B$ is called the *Oversampling Ratio* (OSR) which is one of the most important parameters used to characterize oversampling data converters. For an N bit ADC with OSR as the oversampling ratio, *Signal to Quantization Noise Ratio* (SQNR) is given by Eq. 2.1.

$$SQNR_{max}\,[dB] = 6.02N + 1.76 + 10log_{10}OSR \tag{2.1}$$

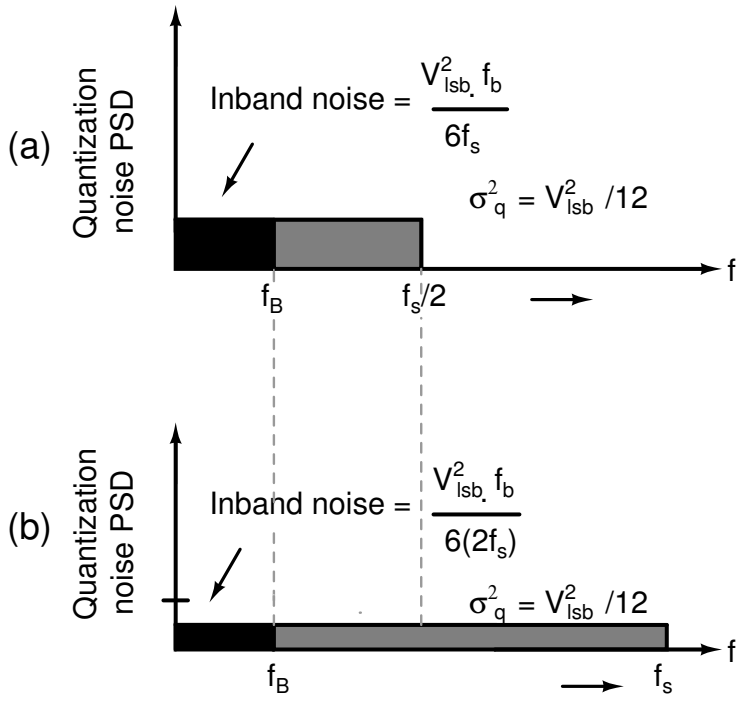

Figure 2.2: Quantization noise spectrum of ADC. (a) Sampling at f_s (b) Sampling at $2f_s$.

The oversamping can be used to trade speed for resolution of ADC. However, the rate of this trading is only 3 dB/octave with plain oversampling. A better way of utilizing this advantage of oversampling is to filter away the noise in the signal bandwidth to higher frequencies, and this what the $\Delta\Sigma$ modulator accomplishes. The block diagram of a discrete time $\Delta\Sigma$ modulator is shown in Fig. 2.3.a and Fig. 2.3.b shows the discrete time $\Delta\Sigma$ modulator with additive noise model for the quantizer. A discrete time modulator is shown for ease of explaining the operation of the modulator. The closed loop architecture can be linearized by modeling the quantization noise as an additive noise. Again, it is assumed that the quantization noise is uniformly distributed and not dependent on the input signal u. This system has two inputs, u and e_q, and one output, v. The transfer function from u to v, which is called *Signal Transfer Function* (STF), is given by:

$$STF(z) = \frac{V(z)}{U(z)} = \frac{L(z)}{1 + L(z)} \tag{2.2}$$

The *Noise Transfer Function* (NTF) which is defined as the transfer function

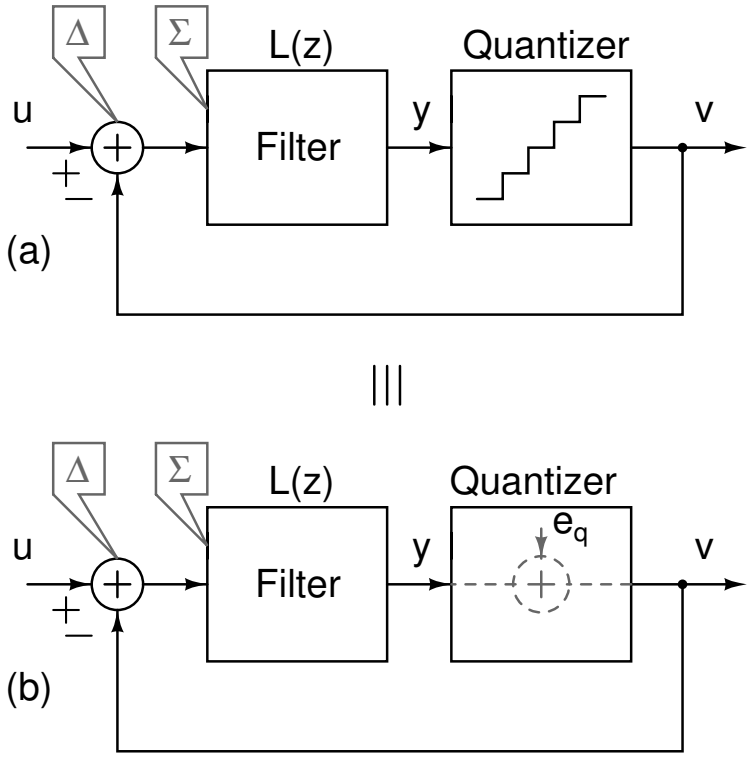

Figure 2.3: $\Delta\,\Sigma$ modulator.

from e_q to v, is given by:

$$NTF(z) = \frac{V(z)}{E_q(z)} = \frac{1}{1 + L(z)} \tag{2.3}$$

If the filter $L(z)$ is a low-pass filter with a high DC inband gain, then STF would be unity in signal band and NTF would be a high-pass filter. This high-pass NTF helps in filtering out the in-band quantization noise to out of band region as shown in Fig 2.4. Inside the signal bandwidth, the quantization noise is attenuated approximately by the large gain of the filter $L(z)$. The output spectrum of the modulator is given by,

$$V(z) = STF(z)U(z) + NTF(z)E_q(z) \tag{2.4}$$

As an example, if $L(z) = 1/(z-1)$, then from Eq. 2.4, we get

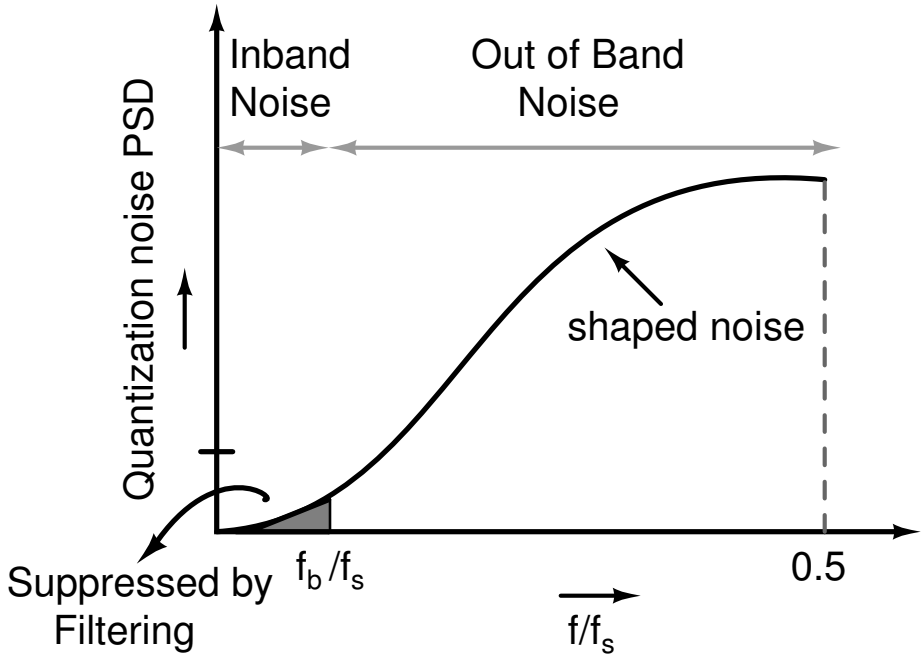

Figure 2.4: Spectrum of the shaped quantization noise.

$$STF(z) = z^{-1} \tag{2.5}$$

$$NTF(z) = 1 - z^{-1} \tag{2.6}$$

From Eq. 2.5, we see that $STF(z)$ is just a delay while $NTF(z)$ has a high pass response. If we want to achieve a very high in-band SQNR, we must choose a sampling rate f_s much higher than the Nyquist rate so that the total quantization noise within the signal band is reduced.

2.1 Continuous-time vs discrete-time

Switched-capacitor (SC) circuits form the building blocks of DT $\Delta\Sigma$ Modulators. SC filters used to be the choice of design for $\Delta\Sigma$ Modulators as they provide high accuracy and linearity. SC filters are unattractive for use in very high speed designs as the settling time and power requirements of opamps used in SC filters pose a

serious limitation. Moreover, the need for an anti-aliasing filter before converting the continuous-time input to a discrete-time input has led to an increase in the usage of CT modulators.

The block diagram of a Continuous-time $\Delta\Sigma$ Modulator is shown in Fig. 2.5. A

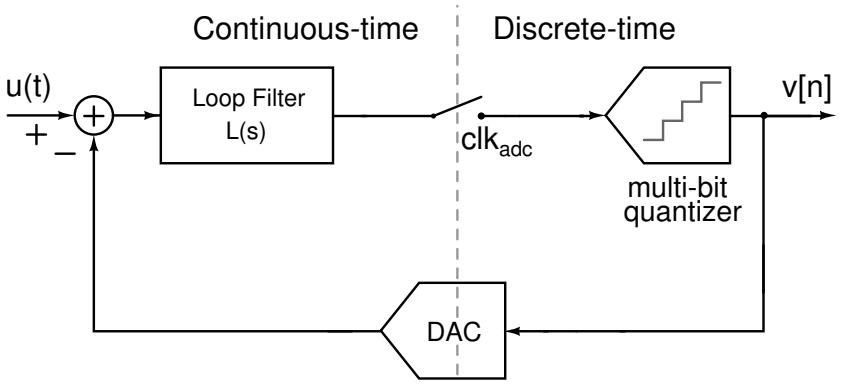

Figure 2.5: Block diagram of a continuous-time modulator.

CT modulator is derived from its DT counterpart by pushing the sampler from outside the loop to within the loop. A *Digital to Analog* (DAC) is used in the feedback path to convert the digital output $v[n]$ to an analog signal, which feeds to the input of the loop filter. CT modulators obviate the need for anti-aliasing filters because the loop filter does inherent anti-aliasing [18]. The maximum frequency of operation in CT modulators is limited by the delay in the quantizer and the feedback DAC while DT modulators are limited by the settling time of the opamps. In general, CT modulators can be operated at a higher frequency than a DT modulator in a given technology.

2.2 Basic components of the CTDSM

2.2.1 Loop filter

The basic circuit blocks of which a CT loop filter consists are the CT integrators. Many kinds of CT integrators are available but the most commonly used ones are active RC integrators and G_m-C integrators. The integrators used in this work

are active RC integrators and are described in Chapter 4.

2.2.2 ADC

The ADC quantizes the output of the loop filter to produce the output of the modulator. Any circuit level nonlinearities in the ADC are shaped out of the signal band. Hence the design constraints on the ADC are very relaxed. The only constraint is the regeneration time of the latch in the ADC, which limits the maximum sampling rate. Hence the flash architecture, which implements the fastest ADC, is the common choice for implementing this internal ADC of the modulator and is described in Chapter 6.

2.2.3 DAC

The DAC converts the output to analog and feeds back to the input. Hence, any nonidealities in the DAC are expected to appear at the input and hence at the output of the modulator, as the transfer function from input to output is unity in the signal band. The DAC elements are bound to have mismatch, which affects the inband performance of the modulator. Standard practices like data weighted averaging (DWA) mitigate this problem. But at high speeds delay from the DWA block becomes significant. This delay has to be accommodated by appropriately delaying the DAC clock, leading to increase in ELD in the loop.

2.3 Non-idealities in the CTDSM

Various non-idealities that appear in practical implementation of a CTDSM are discussed below.

2.3.1 Clock jitter

Clock jitter influences the sampling instant of the flash quantizer, as well as the width of the feedback DAC pulse. The error due to the variation of the sampling instant of the quantizer is noise shaped due to the high loop gain preceeding the quantizer. Hence, the in-band noise power will not be dominated by this noise. However, the error in the DAC feedback pulse width adds directly at the input of the modulator and is not noise shaped. Fig. 2.6 shows the DAC output in a CTDSM (see Fig. 2.5). A timing error of ΔT_s causes an error which can be represented by an impulse of area proportional to error Δq_c . This become more significant as $\frac{\Delta T_s}{T_s}$ increases.

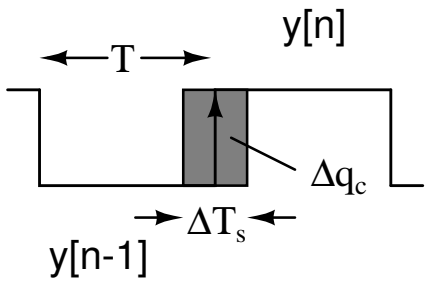

Figure 2.6: Clock jitter effect in a CTDSM.

The effect of clock jitter can be modeled as an additive sequence at the input of a jitter-free modulator [7]. For the case of NRZ feedback DACs considered in this work, the error sequence is given by:

$$e_j(n) = [y(n) - y(n-1)]\frac{\Delta T_s(n)}{T_s} \tag{2.7}$$

Here $y(n)$ and $y(n-1)$ are the n^{th} and $(n-1)^{th}$ samples of the modulator output, T is the sampling time period and $\Delta T_s(n)$ is the clocking uncertainty of the n^{th} edge of the DAC. If $\Delta T_s(n)$ are assumed to be independent identically distributed (i.i.d) random variables [19], the spectral density of e_j is white and has a variance σ_{ej}^2 given by [7]

$$\sigma_{ej}^2 = \sigma_{dy}^2 \frac{\sigma_{\Delta T_s}^2}{T^2} \tag{2.8}$$

Where σ_{ej}^2 is the variance of the clock jitter. Clearly σ_{ej}^2 is dependent on the signal through $y(n)$ and $y(n-1)$. σ_{dy}^2 is the variance of $[y(n)-y(n-1)]$, and is given by

$$\sigma_{dy}^2 = \frac{\sigma_{lsb}^2}{\pi} \int_0^{\pi} |(1-e^{-j\omega})NTF(e^{j\omega})|^2 \, d\omega \tag{2.9}$$

σ_{lsb}^2 is the variance of the quantization noise of the internal quantizer used in the modulator.

2.3.2 Mismatch between DAC cells of the multi-bit quantizer

In a wideband modulator, the oversampling ratio is usually limited by the circuit speed and power consumption. At the same time, the order and the aggressiveness of the noise shaping are also limited by the stability issue. So, in order to decrease the in-band noise power, an effective way is to use a multi-bit quantizer to reduce the quantization noise in the modulator. In a CTDSM, an extra bonus

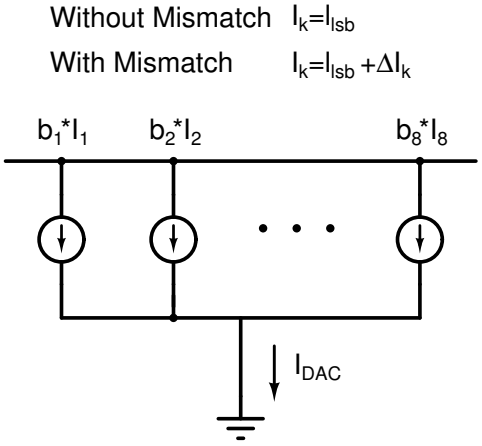

Figure 2.7: Current steering digital to analog converter.

of using a multi-bit quantizer is the reduction of the jitter sensitivity. However,

the use of a multi-bit quantizer leads to a multi-bit DAC in the feedback path. The nonlinearity of this DAC severely limits the performance of the modulator [20]. The Fig. 2.7 shows the current DAC, that give output current depending on the thermometer input code. Fig. 2.8 shows the transfer characteristic with and without mismatch in DAC cells. Each current source value is deviated from its mean value by a small amount.

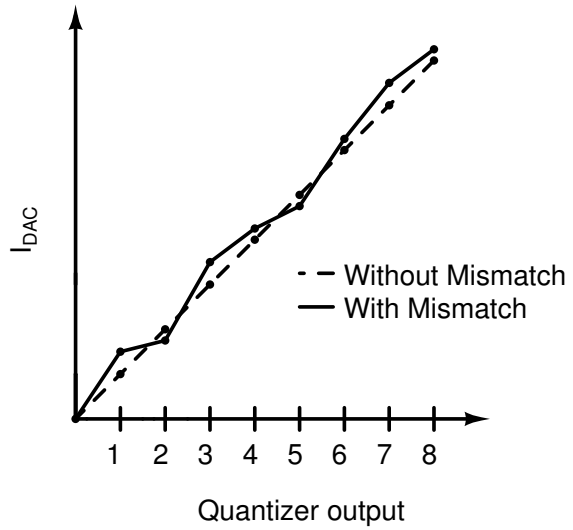

Figure 2.8: Transfer curve of a 3 bit DAC.

The nonlinearity due to this mismatch, can be modeled as additive error $e(n)$ at output of ideal DAC as shown in Fig. 2.9. The *Error Transfer Function* (ETF)

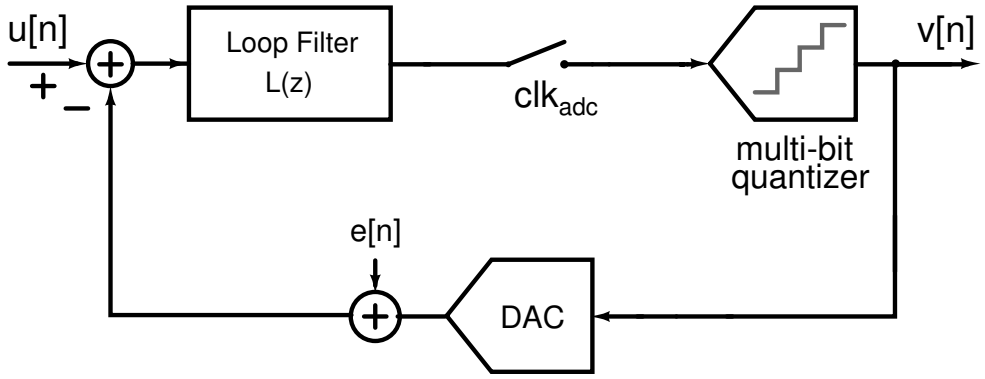

Figure 2.9: Modelling of DAC Error in $\Delta\Sigma$ modulator. A DT $\Delta\Sigma$ modulator is shown.

from DAC error to the modulator output is given by:

$$ETF = \frac{-L}{1+L} \tag{2.10}$$

Because the loop filter has very gain in the signal band, the inband magnitude of ETF is almost equal to one, which means that the power of the DAC error will be directly added to the modulator output without any attenuation. So the linearity of the modulator cannot be higher than that of the DAC.

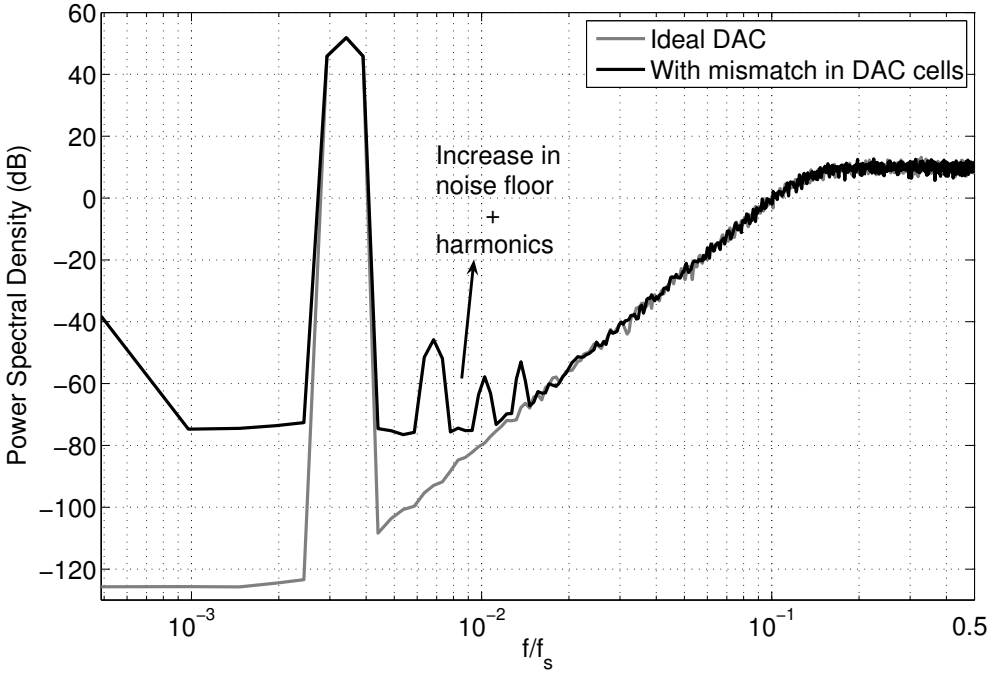

Figure 2.10: PSD due to DAC nonlinearity in a multibit $\Delta\Sigma$ modulator.

Fig. 2.10 shows the effect of this nonlinearity on the output of a fourth order modulator. As it can be seen that DAC nonlinearity has increased the in-band noise floor along with harmonics in the in-band region. The methods to mitigate the effects of mismatch are discussed in Chapter 7.

2.3.3 Non idealities of the loop filter

The loop filter is realized using active-RC integrators. Following are the non-idealities of the RC integrators that effect the modulator performance.

2.3.3.1 Finite gain of the opamp

The amplitude of the in-band shaped quantization noise depends inversely on the DC gain of the opamps [21] and causes *leaky integration* by the integrators of loop filter. Due to the finite opamp gain, the NTF zeros are moved off the unit circle towards $z = 0$, which reduces the amount of attenuation of the quantization in the in-band signal and therefore worse SNR. Fig 2.11 shows the output of a fourth order CTDSM, where the in-band noise is flat due to the finite gain of the opamp.

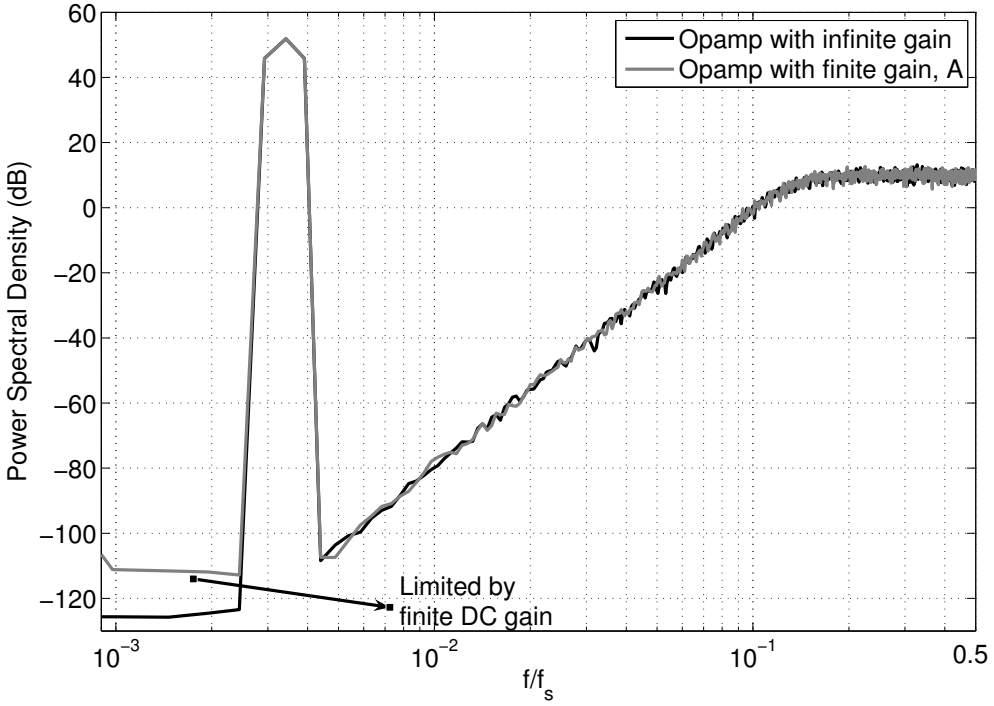

Figure 2.11: PSD due to finite gain of the opamps in the loop filter.

2.3.3.2 Finite unity gain frequency of the opamp

Fig 2.12 shows the an integrator having an opamp of gain $A(s)$. Due to the finite unity gain frequency (UGF) ω_u, opamp gain is characterized by:

$$A(s) = \frac{V_0(s)}{V_i(s)} = \frac{\omega_u}{s} \tag{2.11}$$

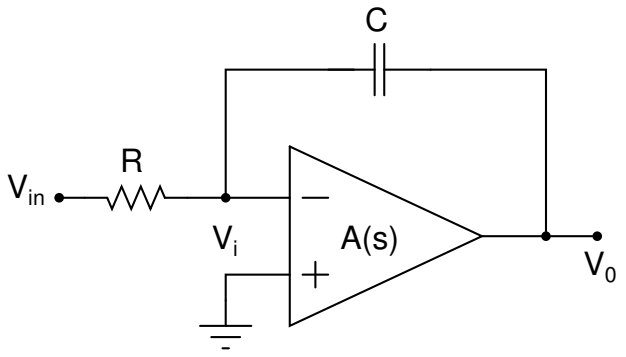

Figure 2.12: A first order active RC integrator.

Then the integrator transfer function from $V_{in}(s)$ to $V_0(s)$ is given by:

$$\frac{V_0(s)}{V_{in}(s)} = \frac{-1}{sRC\left(1 + \frac{1}{\omega_u RC} + \frac{s}{\omega_u}\right)} \tag{2.12}$$

or,

$$\frac{V_0(s)}{V_{in}(s)} = \frac{-1}{sRC(1+k_1)\left(1 + \frac{s}{\omega_u(1+k_1)}\right)} \tag{2.13}$$

Where, $k_1 = \dfrac{1/RC}{\omega_u} = \dfrac{\text{UGF of integrator}}{\text{UGF of opamp}}$.

Eq. 2.13 shows that due to the finite UGF of opamp, integrator gain is changed from $\dfrac{1}{sRC}$ to $\dfrac{1}{sRC(1+k_1)}$ and the second pole introduces an additional delay of $1/\omega_u(1+k_1)$. This is shown in Fig 2.13.

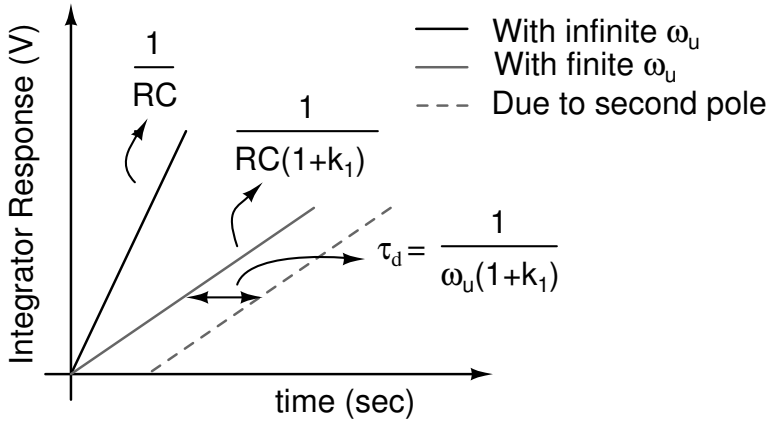

Figure 2.13: Integrator response due to finite UGF of the opamps in the loop filter.

Hence finite UGF of the opamp has two effects:

(a) Apparent UGF of the integrator is modified.

(b) There is delay due to the second extra pole.

2.3.3.3 Variation of RC time constants.

The accuracy of the integrator transfer function is related to that of the RC time constants. In modern semiconductor process, the absolute values of resistors and capacitors can vary by as large as ±15% independently due to the change of process, supply voltage and temperature (PVT), so it is reasonable to believe that the RC product and hence the integrator gain can vary by ±30%.

2.3.4 Excess loop delay

Excess loop delay (ELD) is well known for its detrimental effect on the performance and stability of continuous-time $\Delta\Sigma$ modulators. A detailed analysis on the ELD and methods to mitigate this issue is done in Chapter 3.

CHAPTER 3

Compensating excess loop delay of more than one clock cycle

3.1 Introduction

The CT loop filter is realized from a DT loop filter using $d2c$ command in the *Matlab*. Here, it is assumed that the delay between the sampling instant of the loop filter output and the generation of the new output is zero. However, in real circuits, this delay, known as excess loop delay (ELD), is non-zero due to the finite speed of transistors. The ELD usually consists of delays introduced by the regeneration time of the latch in the quantizer (including the dynamic element matching (DEM) logic if necessary), switching time of the DAC, and due to parasitics poles in the loop filter.

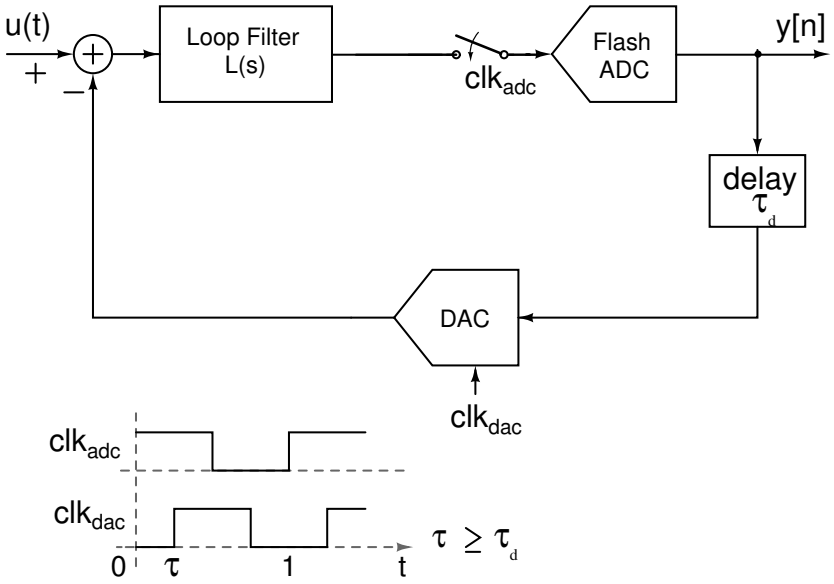

Figure 3.1: Block diagram of CTDSM with ELD.

Fig. 3.1 shows the block diagram of a standard single-loop CTDSM. Because of

the delay τ_d in the loop shown in Fig. 3.1, the DAC will have to be clocked at a time $\tau \geq \tau_d$ delayed from the sampling instant of the ADC. Here, an NRZ DAC pulse is shown so as to be consistent with the DAC used in this work.

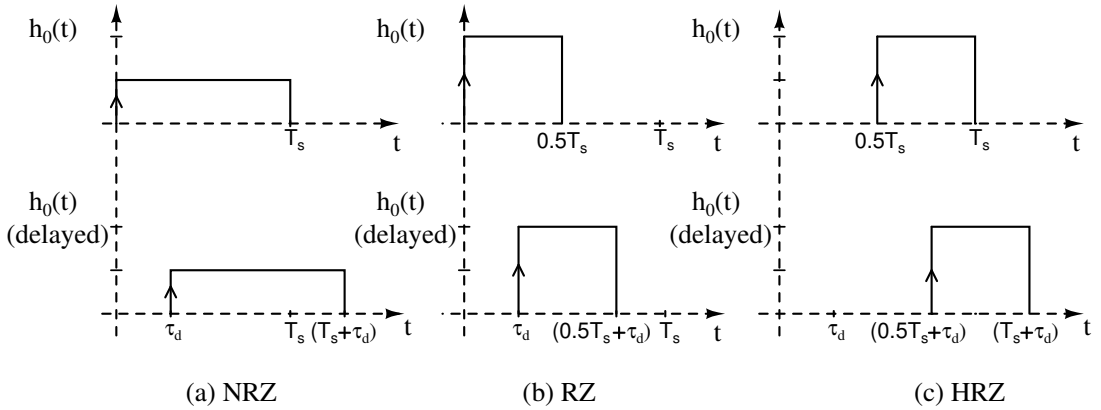

Figure 3.2: Impulse responses of the rectangular NRZ, RZ and HRZ DAC pulses for, (a) Top row: no delay, (b) bottom row: a delay of τ_d.

Fig 3.2 shows three possible rectangular DAC pulses. For NRZ and RZ pulse case, the entire delay τ_d has to be compensated by some ELD compensation technique. However, if a HRZ DAC pulse is used, then half the clock cycle delay can be absorbed by the explicit half clock delay of the DAC pulse.

As analyzed in [16], if the falling edge of the DAC pulse exceeds the time instant T_s, the order of the equivalent DT loop filter increases by one. The excess loop delay degrades the dynamic range of the modulator by reducing the effectiveness of the noise shaping as well as the maximum stable input signal swing. If the excess loop delay is too large compared to the clock period, the CT modulator will be unstable.

Fig. 3.3 shows the output PSD of an feedforward CTDSM with four different excess loop delays τ_d. It can be seen that with increase in τ_d, the in-band SNR reduces and the out-of-band region shows peaking. For $\tau_d = 0.3\,T_s$, the modulator becomes unstable showing the impact of ELD on the modulator performance. In the next section, conventional ELD compensation techniques are discussed.

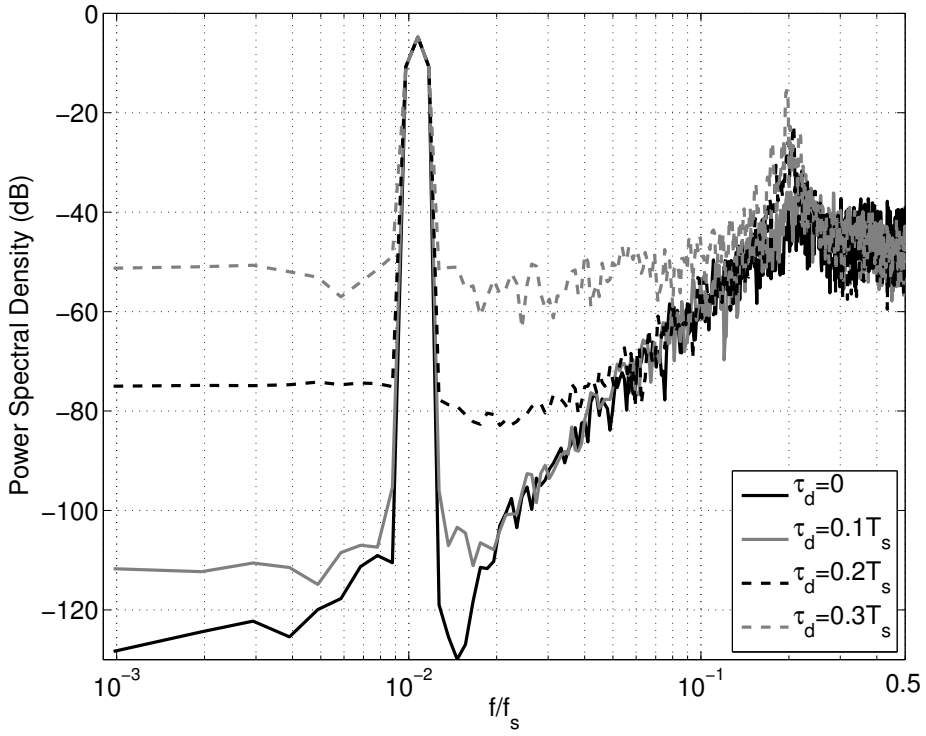

Figure 3.3: The effect of the excess loop delay on the CTDSM output spectrum.

3.2 Classical compensation techniques

Following are the two widely used compensation techniques to compensate ELD in CTDSM.

3.2.1 Compensation using an extra DAC

In this method, a full clock cycle delay is introduced in the feedback having NRZ DAC_1 (see Fig. 3.4), to absorb the varying quantizer delay as well as the other delays caused by the possible digital circuits like DEM and latches between the flash ADC and the DAC. However due to this full clock cycle delay, the impulse response of the CT loop at the sampling instant T_s is zero. To compensate this response sample, an extra feedback branch is added directly to the quantizer input to make the total impulse response equivalent to the ideal DT response [15], This feedback loop is marked as compensating loop in Fig. 3.4.

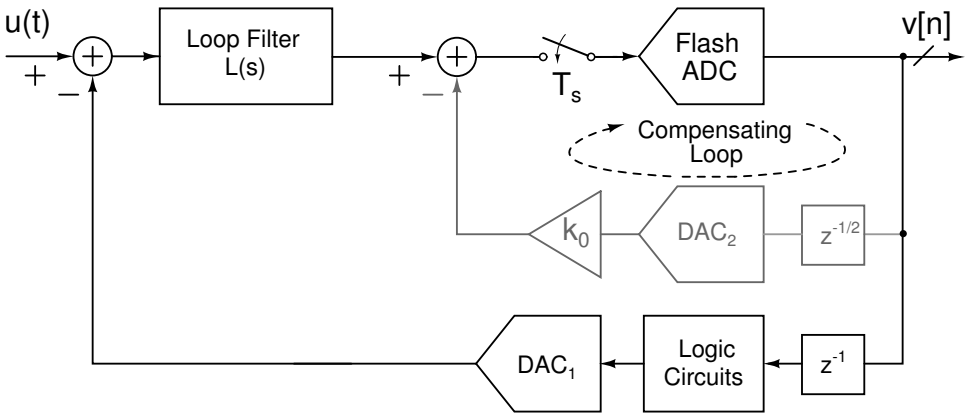

Figure 3.4: Block diagram of CTDSM with ELD compensation that is obtained by bypassing z^{-1} delay block of the main loop.

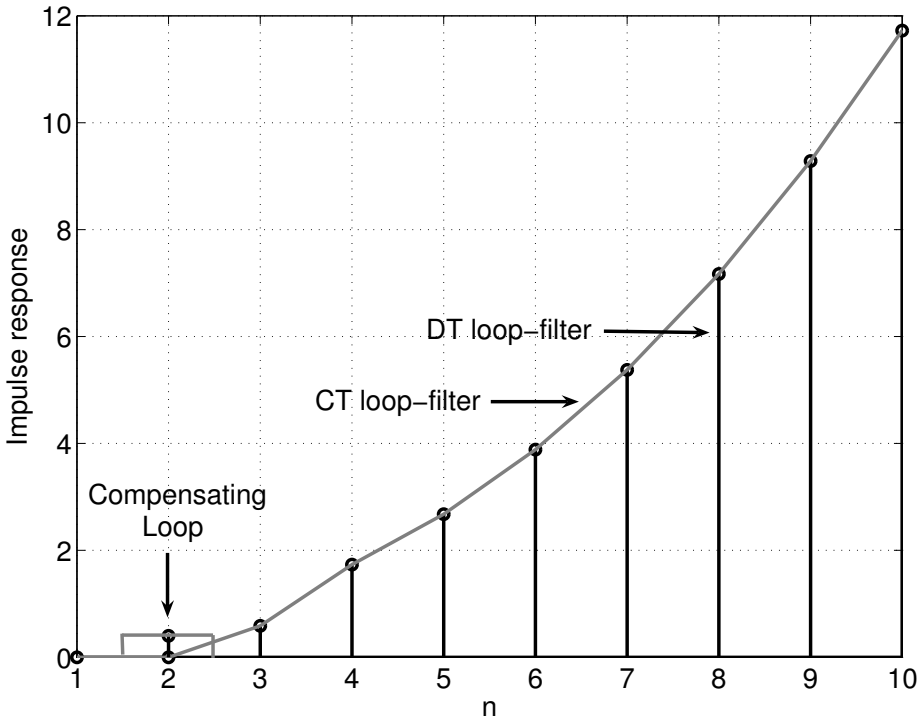

Figure 3.5: Impulse response of a CTDSM and its equivalent DT response with ELD compensation.

The resulting impulse response of the loop filter $L(s)$ is shown in Fig. 3.5. Here, the compensating loop provide the second sample and does not effect any other samples of the impulse response. Although a half clock delay is used in the direct feedback path to compensate the quantizer delay in this example, the real delay of the quantizer can be any value between 0 and T_s, which greatly relaxes the speed requirement of the quantizer. However to accommodate the delay of DAC_1 and equivalent delay caused by the finite opamp UGF in the loop filter, z^{-1} is replaced by $z^{-1/2}$ in high speed circuits [4].

3.2.2 Compensation using a differentiating path in the loop filter

The problem with the previous compensation technique is that it requires an extra DAC (DAC_2 in Fig. 3.4). This DAC loads the quantizer and occupies a large area. In this second technique above problem is removed by using an analog direct path from the output of the DAC_1 (see Fig. 3.4). Fig. 3.6 shows this technique. The direct path k_0 provides the second sample. Gain coefficient k_0 is realized using a

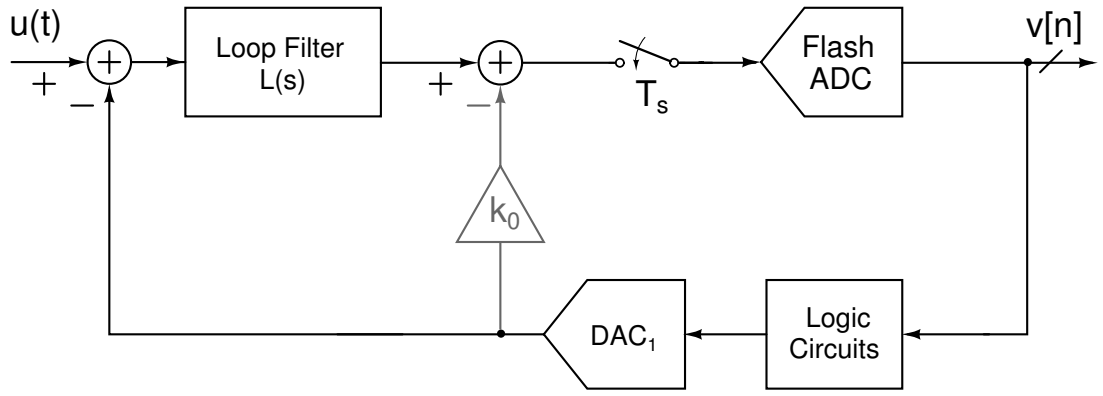

Figure 3.6: Block diagram of CTDSM with ELD compensation that is obtained by bypassing loop filter.

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differentiator following the first integrator in the loop filter. The differentiator is realized by passing output of the first integrator to virtual node of the summing opamp using a capacitor [2]. The drawback of this technique is that the loop delay

includes the delay of the main DAC (DAC_1 in Fig. 3.4) and the loop filter.

3.3 Fundamental limitations of classical compensation techniques

Both the methods described in the last section are effective only if the quantizer delay is less than one clock cycle. To understand this, Fig. 3.6 is modified by moving the sampler before summation as shown in Fig. 3.7. Here, the feedback path DAC is shown as an NRZ DAC pulse which is followed by a delay block. The

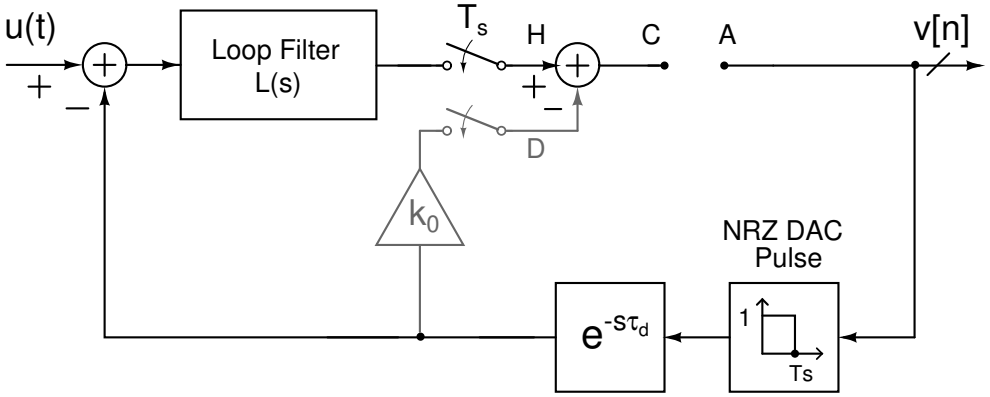

Figure 3.7: Fig. 3.6 modified to show the sampled outputs of $L(s)$ and direct path separately. The loop broken at the input of flash ADC.

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sampled impulse response at the output of the loop filter $L(s)$, the direct path k_0, the resulting NTF impulse response and the NTF magnitude response are shown in Fig. 3.8 for different values of ELD. A fourth order modulator with an Out of Band Gain (OBG) of two and a sampling rate of 1 Hz is used as a prototype.

The top row of Fig. 3.8 corresponds to the delay free case. In this case, the contribution of the direct path is zero to make the sampled impulse response at C equal to the ideal value in Fig. 3.7. The second row corresponds to a half period delay. The second and subsequent samples of the output of the loop filter $L(s)$ are reduced compared to the delay free case. Compensation is achieved by adding an appropriately scaled contribution from the direct path and adjusting coefficients

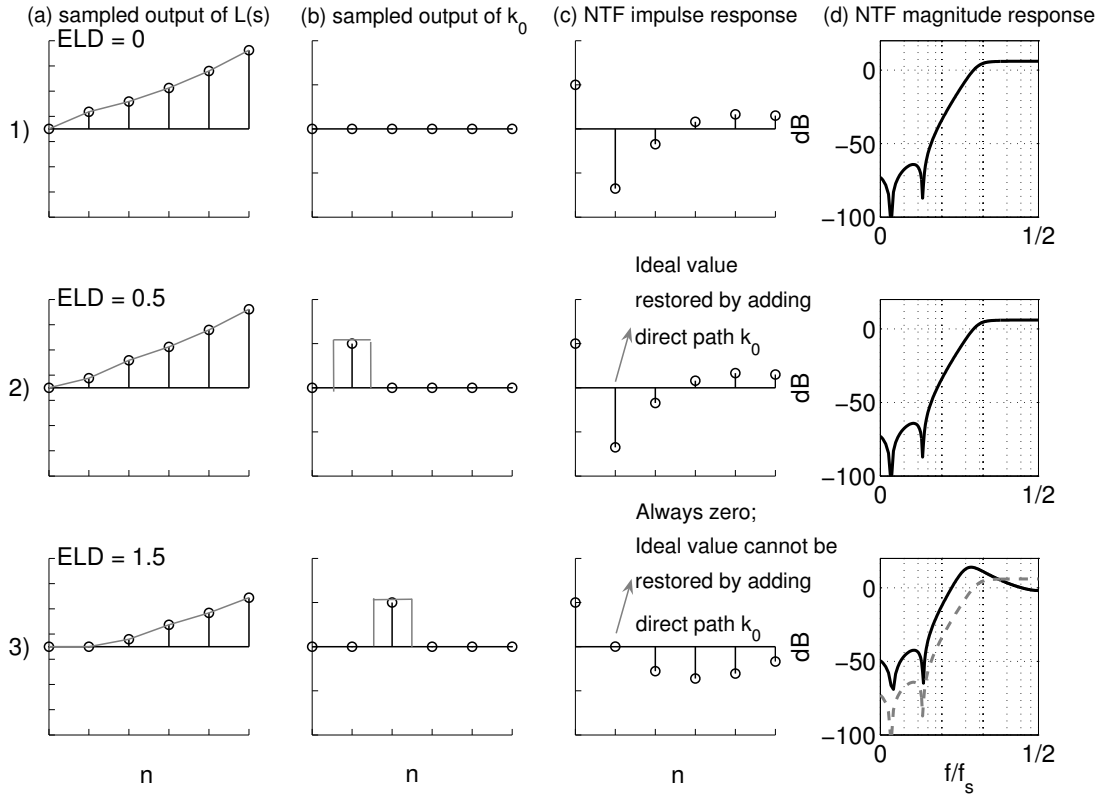

Figure 3.8: Limitation of conventional ELD compensation with $\tau_d > 1$; Each row shows the discrete time equivalent impulse response of the loop filter $L(s)$ and the direct path k_0 (with the continuous time waveforms in gray) and the NTF impulse response that results from the combination. For ELD > 1, the second sample of the NTF is always zero and results in a poor NTF. The Sampling rate is 1 Hz. For clarity, columns (a), (b), and (c) are shown to different scales.

k_{1-4} in the loop filter $L(s)$ to make the sampled impulse response at C in Fig. 3.7 the same as in the delay free case [17]. The resulting NTF (Fig. 3.8 (2c)) is exactly the same as in the ideal case (Fig. 3.8(1c)). As ELD increases, the second sample decreases further, and the contribution required from the direct path increases.

The third row corresponds to an ELD of one and a half clock cycles. The second sample of the output of the loop filter $L(s)$ is zero. In this case however, the contribution of the direct path is also zero and the second sample cannot be restored to its ideal value regardless of the choice of k_0. Therefore, the second sample of the impulse response at C in Fig. 3.7 is zero. This results in an NTF whose second sample is always zero (Fig. 3.8 (3c)). As shown in [22] (Appendix I), good lowpass $NTFs$ cannot be realized with stable minimum phase transfer functions having a zero valued second sample in their impulse responses. An example of the magnitude response of a stable NTF optimized for noise suppression at low frequencies, with second NTF sample being zero is shown in Fig. 3.8 (3d). Compared to the ideal case (Fig. 3.8 (1d)), the quantization noise suppression is worse and there is a greater peaking, indicating that conventional compensation techniques are not effective for ELD exceeding a clock cycle.

The only way to obtain a non zero second sample in the impulse response from A to C in Fig. 3.7 is to have an additional feedback path which does not depend on the quantizer. The delay of this path has to be less than a clock cycle. This is detailed in the next section.

3.4 Compensation technique for ELD≥ 1

A method of compensating more than a clock cycle by using a feedback loop that does not contain the quantizer is given in [23], where the authors evaluated the NTF and concluded that the resolution reduces due to increased NTF magnitude in the signal band. In this work, we thoroughly evaluate the technique of placing

a local feedback for a lowpass modulator and show that a much higher sampling rate can be achieved leading to a correspondingly higher oversampling ratio (OSR) and a significantly higher resolution.

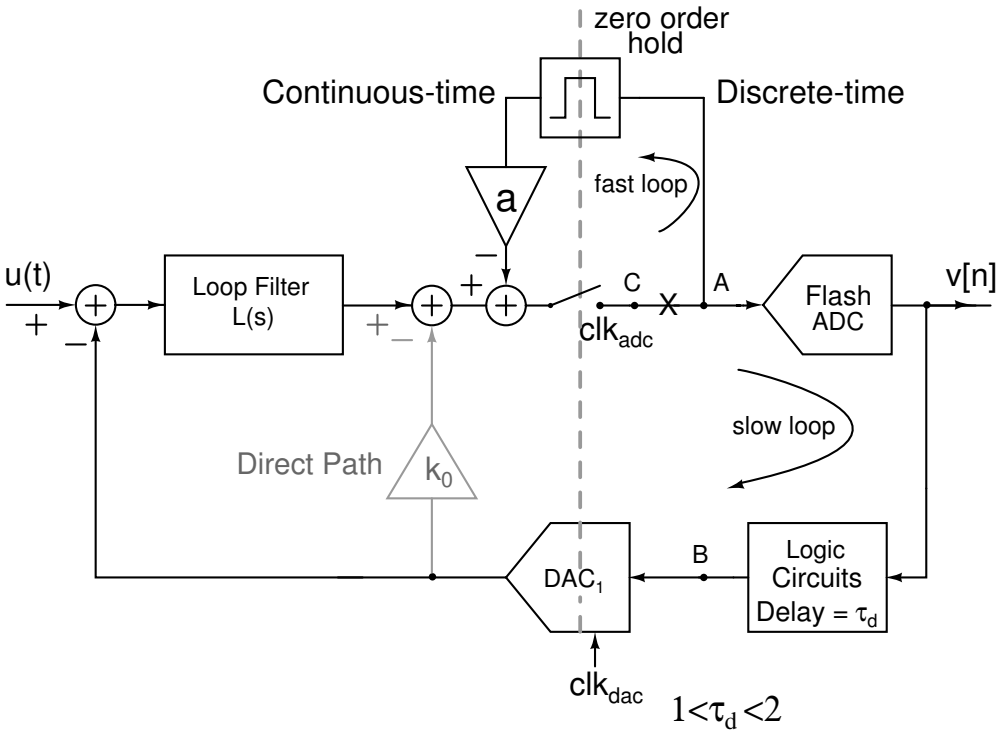

Figure 3.9: Block diagram of a $\Delta\Sigma$ ADC with ELD compensation obtained by bypassing the flash ADC using an S/H.

Fig. 3.9 shows the modulator of Fig. 3.6 with an additional feedback loop around the sampler. A zero-order-hold converts the discrete-time signal into a continuous-time signal. In practice, the zero-order-hold is realized using a separate sample-and-hold circuit (S/H). Since the new loop requires only a S/H, its delay is much smaller than that of the quantizer[2] and the digital logic, and can be designed to have a delay less than a clock cycle from A to C. As before, the loop is broken at the point marked X and the discrete time impulse response from A to C is adjusted to be that of the ideal loop filter.

Here, the second sample of the original loop filter impulse response from A to C is obtained by adjusting the coefficient a in the fast loop. After getting the second

[2]High speed quantizers usually need more than one latching stage to minimize errors due to metastability.

sample accurately from the fast loop, coefficients k_{0-4} are adjusted to match the rest of the samples to their ideal values.

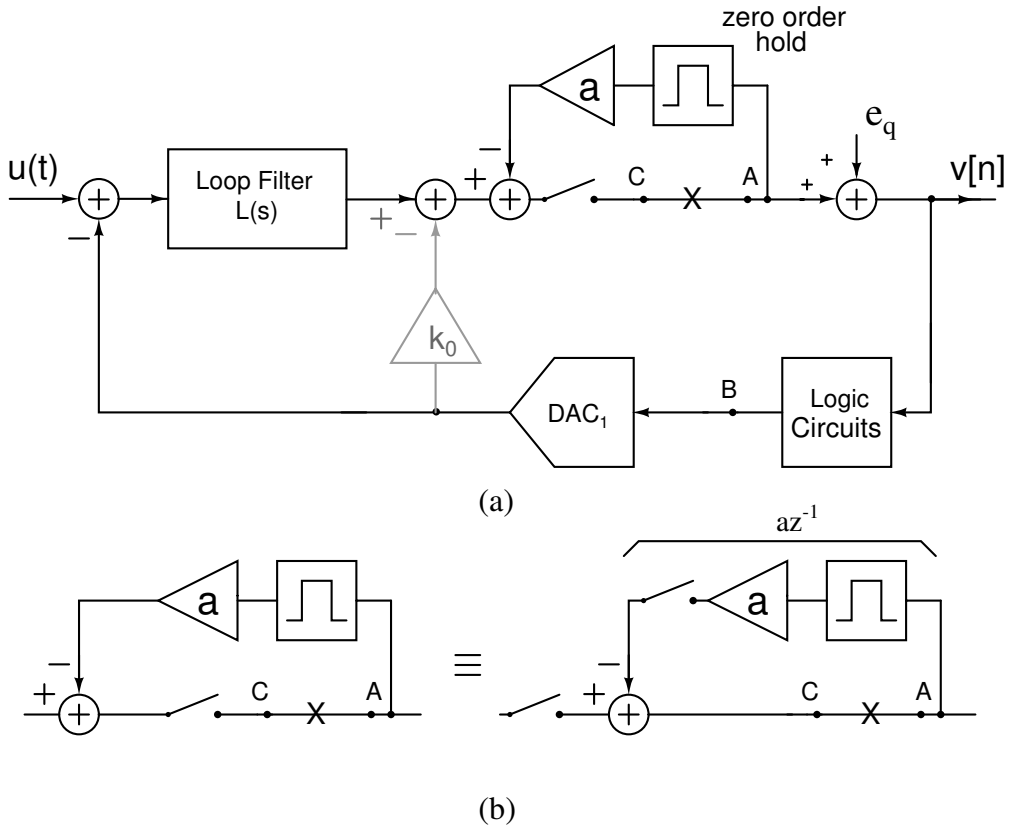

Figure 3.10: (a) Proposed $\Delta\Sigma$ modulator with additive quantization noise e_q and (b) calculating the transfer function of the fast loop.

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Fig. 3.10(a) shows the proposed structure with additive quantization error e_q. The transfer function before the quantizer consists of the sampled outputs of $L(s)$ and k_0 cascaded with the fast loop. From Fig. 3.10(b) it is seen that the transfer function of the fast loop is $1/(1+az^{-1})$. The transfer function from the quantization error E_q to the output V is then calculated as follows:

$$E_q(z) - V(z)\left[L_d(z)z^{-2} + k_0 z^{-2}\right]\frac{1}{1+az^{-1}} = V(z) \tag{3.1}$$

$$\frac{V(z)}{E_q(z)} = \frac{1+az^{-1}}{1+az^{-1}+(k_0+L_d(z))z^{-2}} \tag{3.2}$$

Where $L_d(z)$ corresponds to the sampled output of $L(s)$. As mentioned in the

previous section, the denominator is adjusted to be the same as that in the ideal NTF. Therefore,

$$NTF = (1 + az^{-1})NTF_{ideal}(z) \tag{3.3}$$

An additional zero appears in the noise transfer function, reducing the in-band signal to quantization noise ratio SQNR to some extent. These effects are studied in the next section, where a fourth order NTF is used for illustration.

3.5 Simulation results

The NTF of a conventional fourth-order $\Delta\Sigma$ modulator with optimized zeros is of the form

$$NTF_{ideal} = \frac{(1 - 2\cos\omega_1\, z^{-1} + z^{-2})(1 - 2\cos\omega_2\, z^{-1} + z^{-2})}{\sum_{m=0}^{4} b_m z^{-m}}$$

Where ω_1 and ω_2 are the frequencies of the optimized zeros. As shown in the previous section, the NTF of the modulator with the new compensation technique is of the form,

$$NTF_{prop} = (1 + az^{-1})\frac{(1 - 2\cos\omega_1 z^{-1} + z^{-2})(1 - 2\cos\omega_2 z^{-1} + z^{-2})}{\sum_{m=0}^{4} b_m z^{-m}} \tag{3.4}$$

Here, the ideal NTF is modified[3] due to the zero at $z = -a$.

Table 3.1 shows the values of b_m, optimized zeros ω_{1-2}, the continuous-time loop filter coefficients k_{0-4} and the fast loop coefficient a for ELD = 0, ELD = 0.5 (conventionally compensated) and ELD = 1.5 (compensated using a S/H.).

Fig. 3.11 shows the NTF magnitudes of the ideal and the analyzed modulator structures. There is an increase of 7.5 dB in the in-band quantization noise *for a*

[3]In this case, $\int_0^{\pi} \log\left|NTF\left(e^{j\omega}\right)\right| d\omega \neq 0$, because the zero at $z = -a$ is outside the unit circle.

Table 3.1: Coefficients of a fourth order butterworth NTF with $OBG = 2$ and optimized zeros. (OSR= 25)

b_0	b_1	b_2	b_3	b_4	ω_1	ω_2
1	-2.634	2.757	-1.332	0.248	0.0447	0.109

ELD	k_0	k_1	k_2	k_3	k_4	a	NTF
0	0	1.017	0.568	0.209	0.033	N/A	$NTF_{ideal}(z)$
0.5	0.588	1.343	0.705	0.225	0.031	N/A	$NTF_{ideal}(z)$
1.5	0.966	2.164	0.943	0.255	0.028	1.352	$(1+az^{-1})NTF_{ideal}(z)$

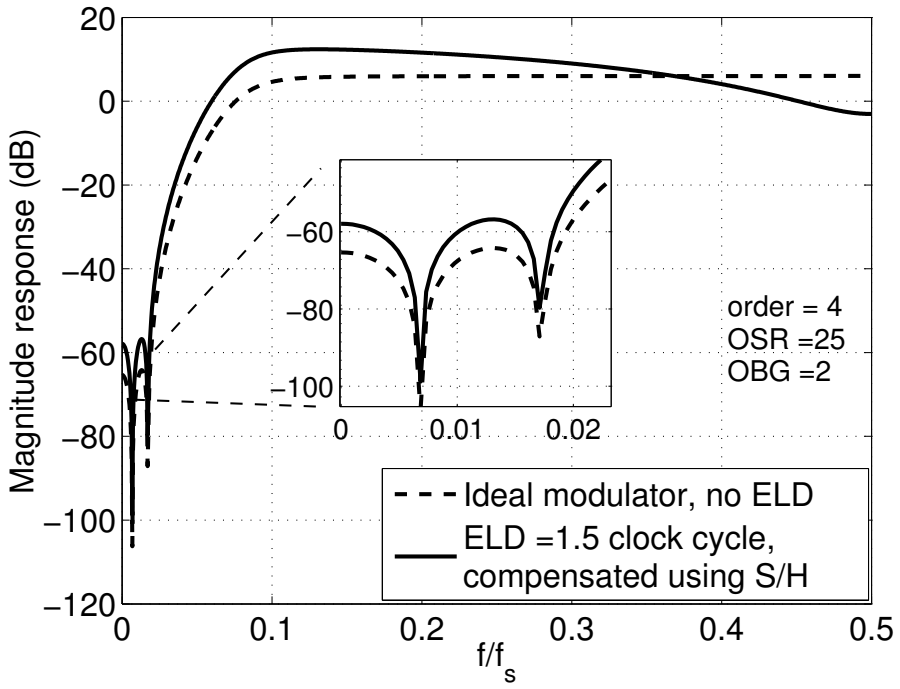

Figure 3.11: $|NTF|$ showing the effect of $(1 + az^{-1})$ in the analyzed modulator.

given OSR. The maximum stable amplitude (normalized to the quantizer range) with a 4 bit quantizer is 0.87 for the conventional case and 0.75 for the modulator with a S/H. However, ELD =1.5 represents a 3 times increase in sampling rate for a given quantizer in a given process technology compared to conventional case (where ELD is usually limited to 0.5). The resulting increase in OSR for a given signal bandwidth results in a much higher SQNR.

Fig. 3.12 shows the effect of the zero at $z = -a$ on the performance of the $\Delta\Sigma$ modulator. As OBG increases, it is seen that the difference in the peak SQNR of an ideal modulator and the one compensated using the analyzed technique

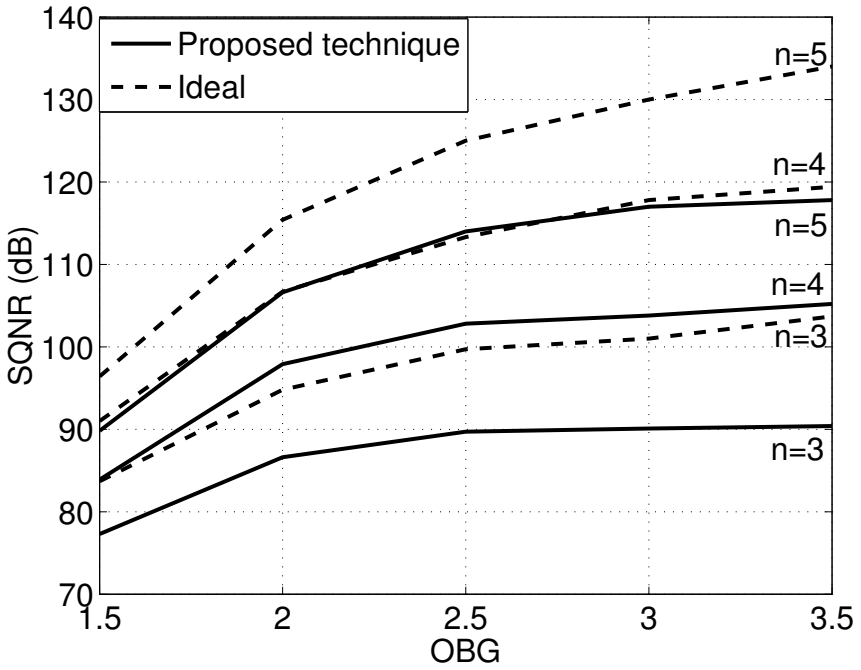

Figure 3.12: Peak SQNR versus OBG for various orders. An ELD =1.5 is compensated using the proposed technique. A 4 bit quantizer is assumed. (OSR = 25)

increases. However, the performance is better than that of a third order modulator. Similarly, the fifth order compensated modulator approaches the behavior of an ideal fourth order modulator. Thus, compensation technique demands an increase in order by one to get the same peak SQNR as from the ideal modulator for a given oversampling ratio.

Fig. 3.13 shows that for the same sampling frequency (f_s), a higher SQNR is obtained from a conventionally compensated modulator compared to the modulator with a S/H. Since $f_{s,max}$ is limited by ELD = 2 in the proposed technique, the sampling rate of the CTDSM can be increased by a factor of 2. In practice sensitivity considerations limit the ELD to 0.5 in the conventional case and 1.5 in the proposed technique. So, the sampling rate can be increased by an factor of three. Hence, as shown in Fig. 3.13, in a given technology we can obtain a higher SQNR (or bandwidth) with the proposed architecture compared to conventionally compensated modulators.

From the simulation results shown in Fig. 3.14, it is seen that the sensitivity of the

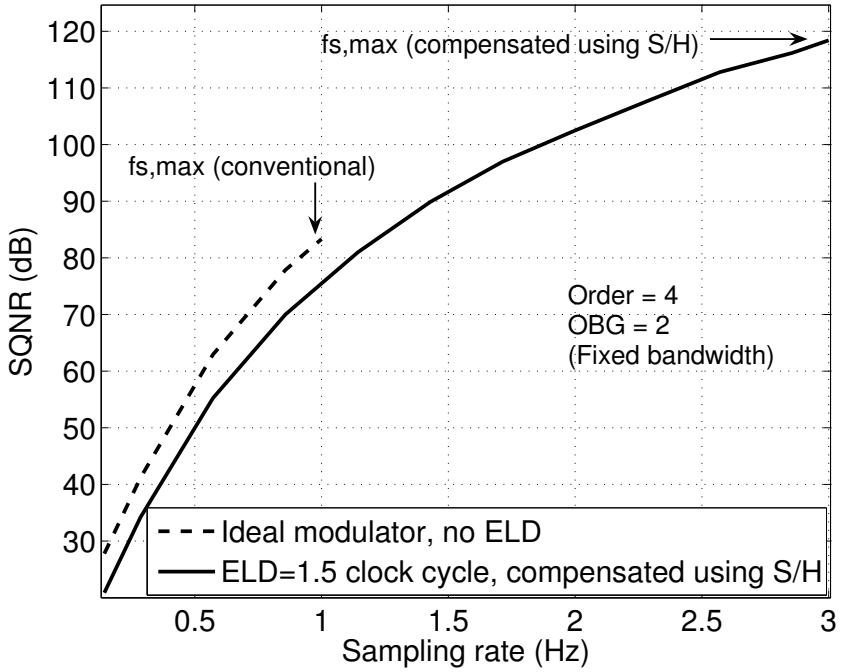

Figure 3.13: Variation of SQNR with sampling frequency (f_s). f_s is normalized to $f_{s,max}$ of a conventionally compensated modulator. The signal bandwidth is 1/50.

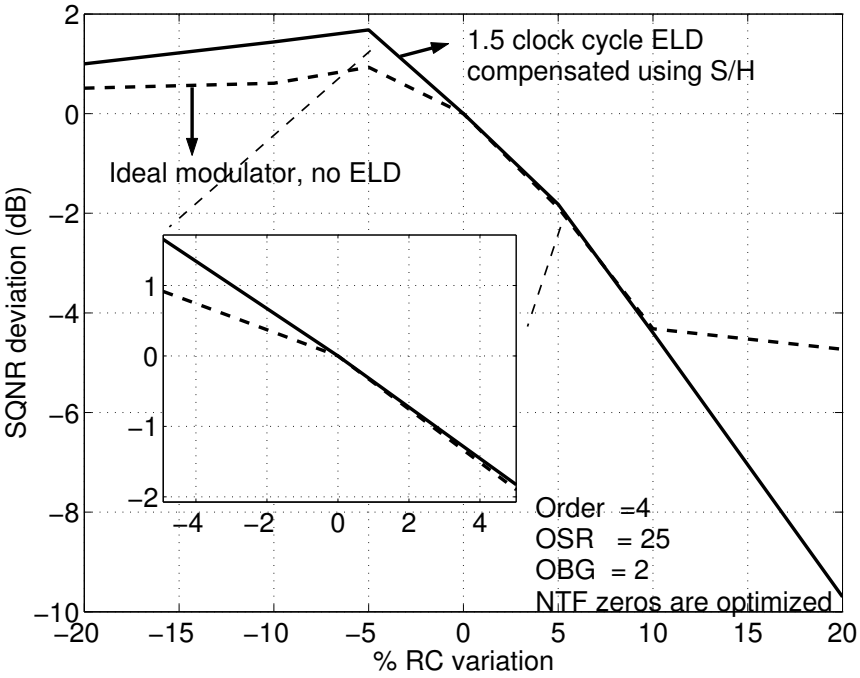

Figure 3.14: Peak SQNR deviation from its ideal value versus time constant variations of the loop filter.

conventional and proposed architecture is virtually the same for ±5% variations in filter time constants. The sensitivity of the NTF magnitude response with

respect to the coefficient a of S/H is shown in Fig. 3.15. The inband SNR changes by $\pm 0.5\,\mathrm{dB}$ for $\pm 10\%$ variation in the coefficient a, attesting to the robustness of the technique.

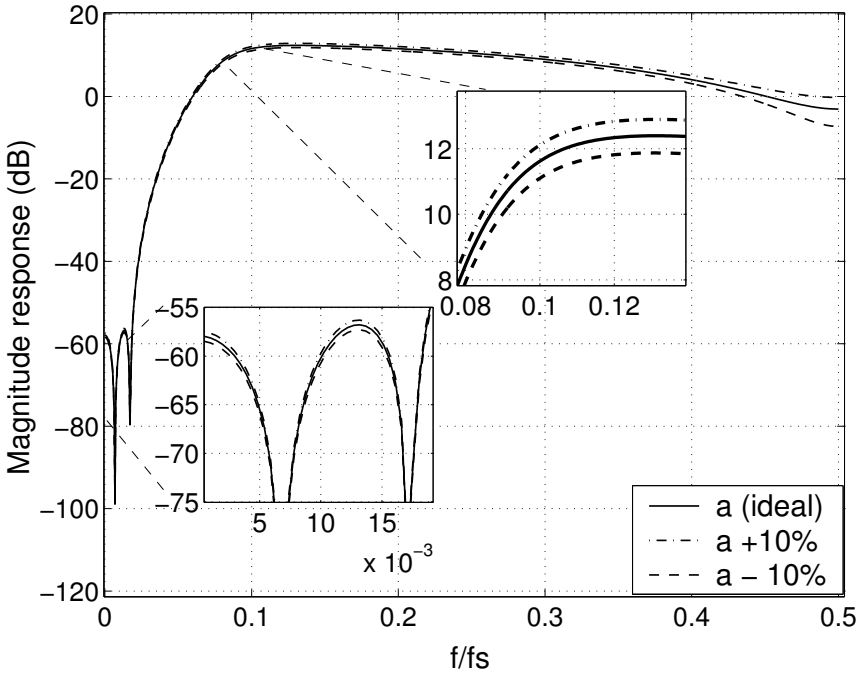

Figure 3.15: Magnitude response of noise transfer function (NTF) for different values of gain coefficient a.

3.6 Architecture of the Modulator

Fig 3.16 shows the final architecture of CTDSM implemented in this work. A fourth order modulator with OBG of 2 and OSR of 25 is designed. A 4 bit quantizer is chosen. Calibration is used to remove the mismatch in DAC elements. Each of these blocks will be discussed in detail in subsequent chapters. Table 3.2 shows the design specifications.

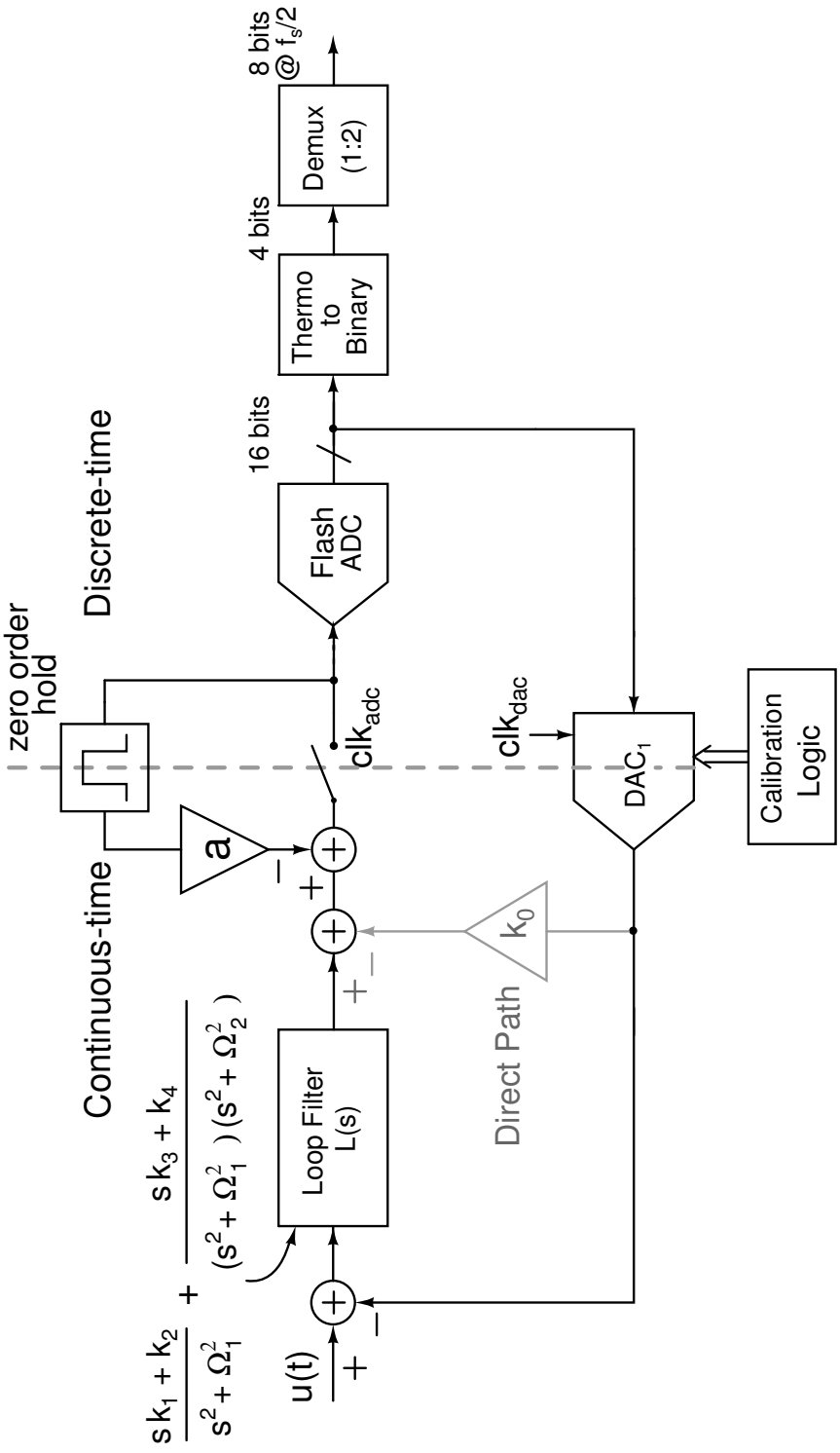

Figure 3.16: Block diagram of the designed CTDSM.

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Signal Bandwidth	16 MHz
Resolution	13 bits
Signal to Noise Ratio(SNR)	82 dB
Sampling Rate	800 MHz
Supply voltage	1.8 V
Full Scale(FS) of quantizer	$3\,V_{pp,d}$

Table 3.2: Design Specifications

CHAPTER 4

Fourth order loop filter

4.1 Architecture

In the previous chapter, we have seen that a fourth order loop filter with optimized zeros (for an OSR of 25) is used for the current design. Loop filter architecture was chosen to be cascade of integrator with feedforward summation (CIFF) as shown in Fig. 4.1(a). The main advantage of CIFF over cascade of integrator with distributive feedback (CIFB) is that the signal component at the integrator

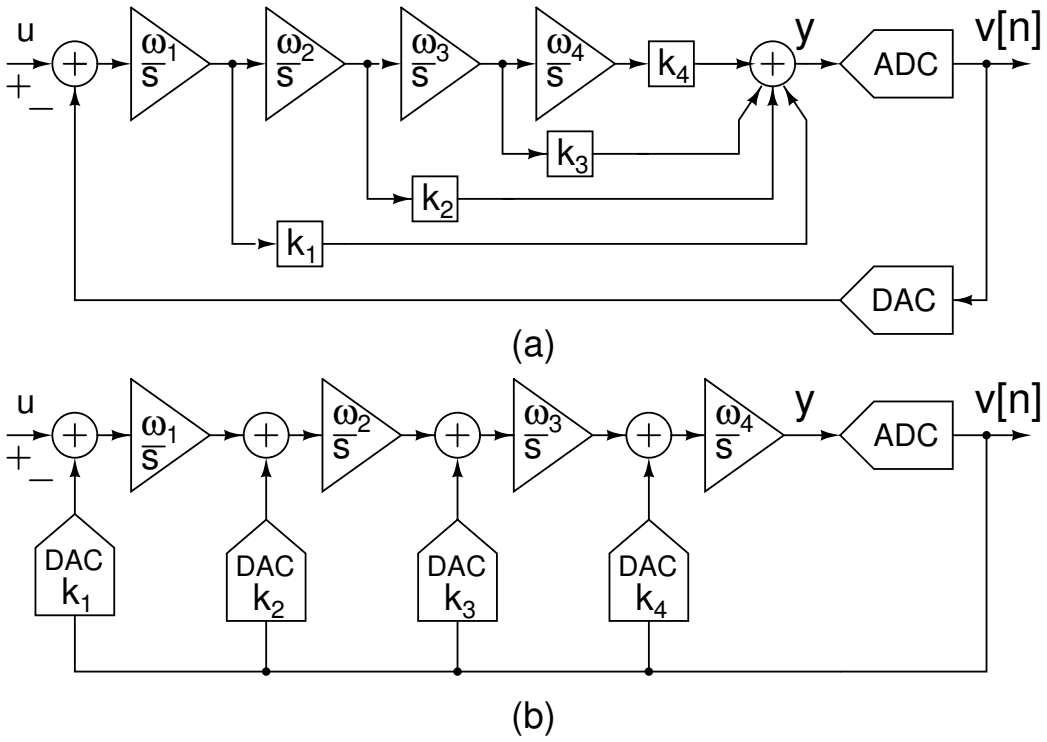


Figure 4.1: Lowpass fourth order CTDSM (a) CIFF and (b) CIFB topology.

outputs is a lot smaller. This enables a lower distortion.

Secondly, a 4-bit quantizer is used in the present implementation. A CIFB loopfilter would need four such DACs compared to a single DAC in case of CIFF. Hence,

using a CIFF loop-filter results in a smaller area. Also due to multiple feedback in the CIFB, load on the quantizer is higher. This increases the quantizer's power dissipation.

4.2 Active-RC vs G_m-C integrators

The basic circuit blocks in a CT loop-filter are the CT integrators. Many kinds of CT integrators are available but the most commonly used ones are active-RC integrators and G_m-C integrators (see Fig. 4.1). The comparison between active-

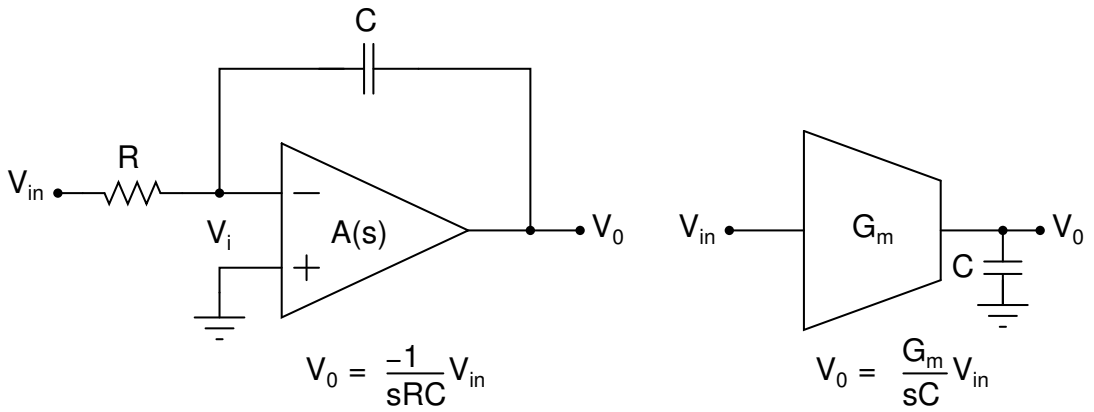


Figure 4.2: (a) Active-RC and (b) G_m-C integrators.

RC integrators and G_m-C is as follows :

- Active-RC integrators are closed loop applications of the opamps, whereas G_m-C integrators have transconductors in open loop.
- Because of this, active-RC integrators have high linearity, which allows a larger signal swing.
- G_m-C integrators can work at higher speeds then active-RC integrators due to their open-loop architecture.
- In a loop filter with active-RC integrators, the virtual ground termination provided by the first opamp will also greatly improve the linearity of the feedback DAC whose outputs are connected to the inputs of the opamp.

Because of the above reasons, active-RC integrators are used in our prototype CT $\Delta\Sigma$ modulator.

4.3 Discrete-time (DT) loop filter and its continuous-time (CT) equivalent

4.3.1 Discrete-time loop filter

A fourth order modulator with optimized zeros and an OSR of 25 is used for the current design. The NTF that is to be realized is derived from the $\Delta\Sigma$ *Toolbox* [24] in MATLAB and is given by:

$$NTF_{ideal}(z) = \frac{(z^2 - 1.998z + 1)(z^2 - 1.988z + 1)}{(z^2 - 1.204z + 0.3771)(z^2 - 1.43z + 0.6585)} \tag{4.1}$$

From the NTF_{ideal}, the loop filter response $L(z)_{ideal}$ can be determined by:

$$L_{ideal}(z) = \frac{1 - NTF_{ideal}(z)}{NTF_{ideal}(z)} \tag{4.2}$$

With the ELD compensation technique described in the previous chapter the NTF realized will be:

$$NTF(z) = (1 + az^{-1})NTF_{ideal}(z) \tag{4.3}$$

The modulator with the NTF given in Eq. 4.3, was simulated in MATLAB. The peak SNR obtained is 96 dB.

4.3.2 Continuous-time loop filter realization

If we want to realize the above discrete-time loop filter response in a CT modulator with an NRZ DAC, the sampled value of the pulse response of the CT loop filter should be the same as the impulse response of the DT loop filter. In our case, since the second sample of the NTF is obtained from the parallel path, the sampled

response at the output of the CT loop filter must corresponds to :

$$L(z) = L_{ideal}(z) - az^{-1} \tag{4.4}$$

Fig. 4.3 shows the DT and the CT implementations of the loop filter.

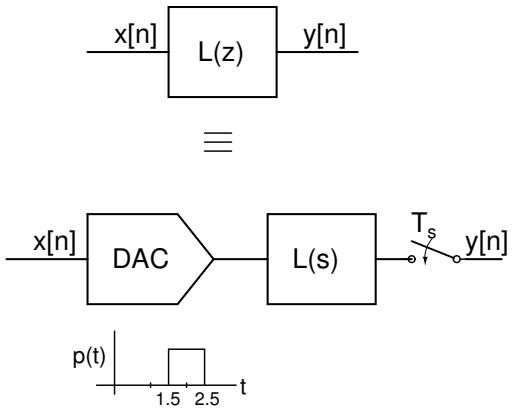


Figure 4.3: Equivalence of CT and DT loop filters

The two systems shown in Fig. 4.3 are identical if:

$$Z^{-1}\{L(z)\} = L^{-1}\{P(s)L(s)\}|_{t=nT_s} \tag{4.5}$$

where $P(s)$ represents the pulse response of the DAC. This transformation of the DT response to the CT response is called as the impulse invariance transform. Using MATLAB, for a CT modulator with an NRZ DAC, one can drive the CT loop filter response including ELD compensation as:

$$H(s) = \frac{0.9695(s + 1.758)(s + 0.2436)(s^2 + 0.2311s + 0.095)}{(s^2 + 0.001823)(s^2 + 0.01171)} \tag{4.6}$$

This forms the prototype CT loop filter for our design. The prototype loop filter response in Eq. 4.6 when driven by an NRZ DAC with a delay (ELD) of 1.5 clock cycles sampled at the output, corresponds to Eq. 4.4. A fourth order CT loop filter in CIFF architecture can be realized using a cascade of four integrators. Fig. 4.4 show the prototype loop filter for ELD of 1.5 clock cycle in the loop. The

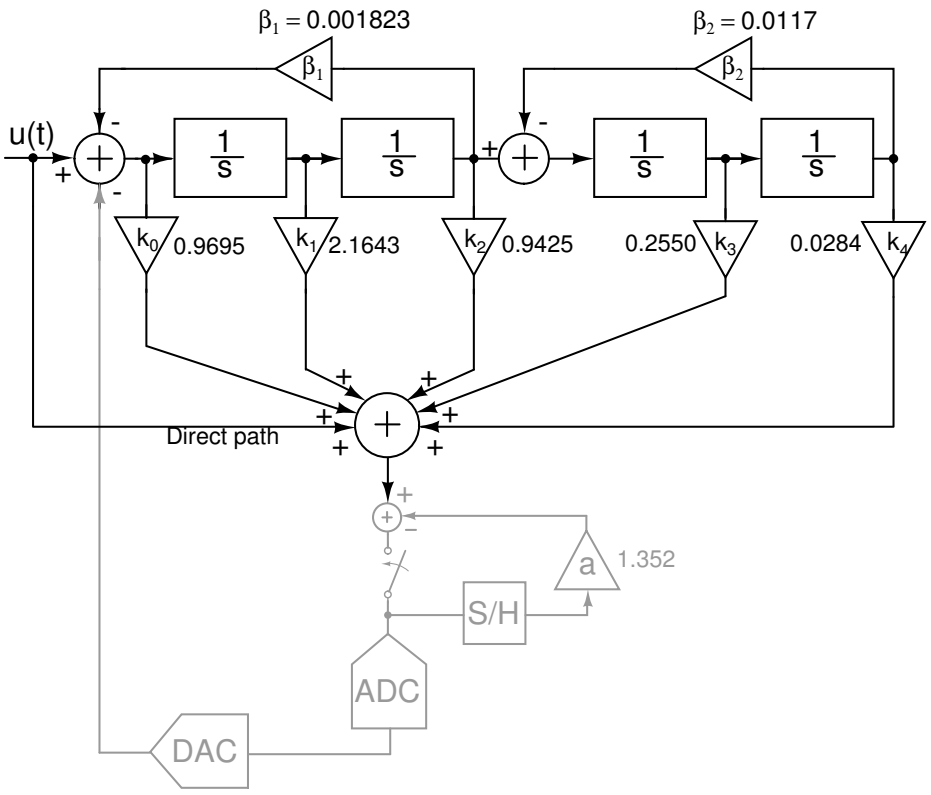


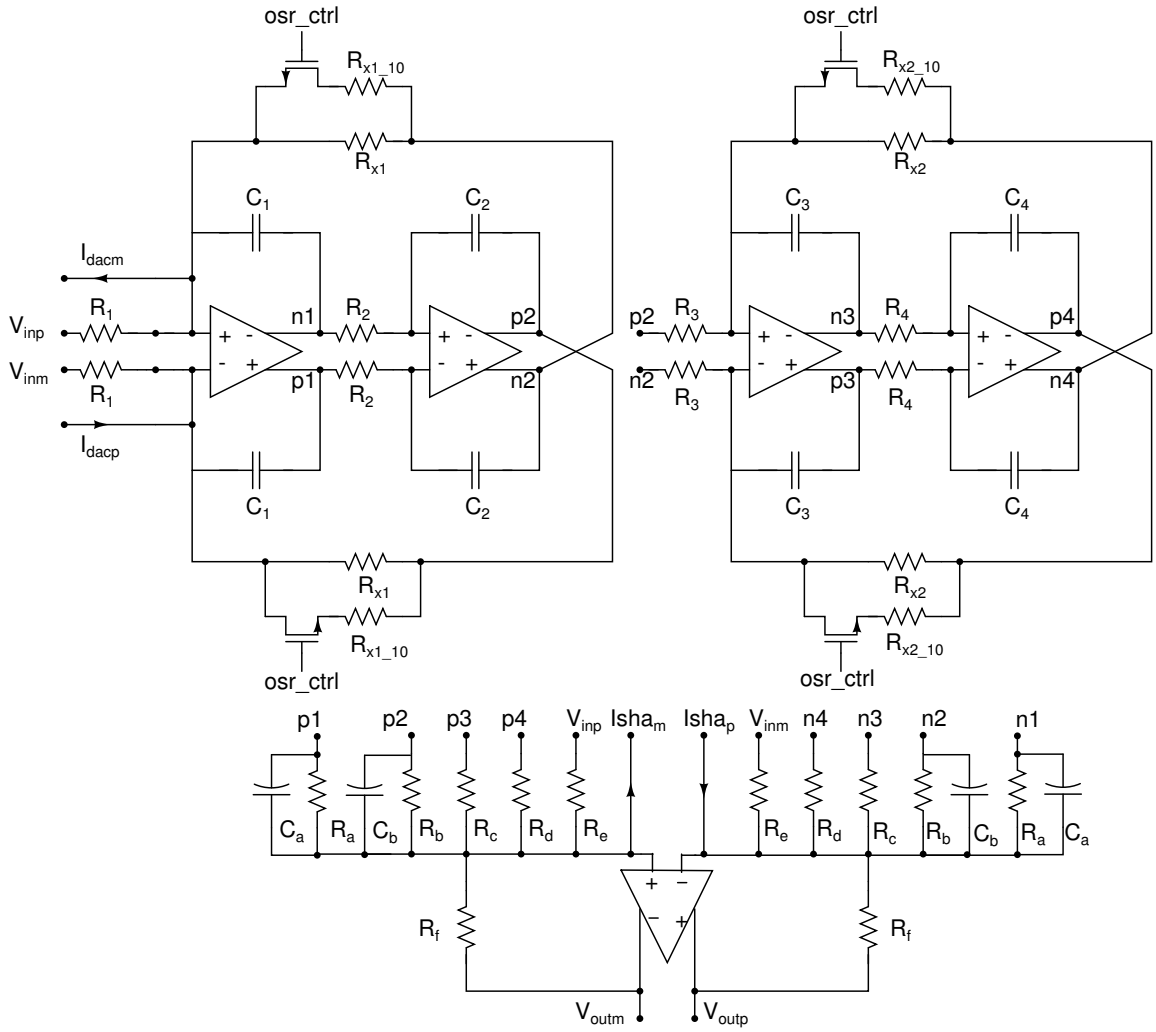
Figure 4.4: Prototype fourth order loop filter (ELD =1.5 clock cyle).

optimization zeros of the NTF are realized using the feedback factors β_1 and β_2. Direct path is added from the modulator input to the loop filter output to reduce the swing at the output of third and fourth integrators. In our design, we use a sampling frequency f_s of 800 MHz. So, we have to frequency scale our prototype loop filter by replacing s by s/f_s in Eq. 4.6. In other words, $H(s/f_s)$ gives the loop filter response to be operated at a sampling rate of f_s.

Nodes are scaled such that that all nodes have a peak-to-peak differential swing of approximately 800 $\mathrm{mV_{pp,d}}$, except for the summing amplifier which has a peak-to-peak differential swing of 3 $\mathrm{V_{pp,d}}$. Node scaling ensures that the outputs of the opamps do not saturate for input voltages within the quantizer range.

4.4 Loop filter component specifications

The loop-filter is a fourth order filter implemented using active-RC integrators shown in Fig. 4.5. The loop-filter is a cascade of integrators with feedforward



R_1	2 kΩ	C_1	625 fF
R_2	20 kΩ	C_2	93.75 fF
R_3	40 kΩ	C_3	104.16 fF
R_4	40 kΩ	C_4	375 fF
R_a	3.47 kΩ	C_a	242.37 fF
R_b	5.31 kΩ	C_b	25 fF
R_c	5.87kΩ	R_d	4.4 kΩ
R_e	7.5 kΩ	R_{x1}	731.2 kΩ
R_{x2}	61 kΩ	R_{x1_10}	116.7 kΩ
R_{x2_10}	9.75 kΩ	R_f	7.5 kΩ

Figure 4.5: Loop-filter block diagram.

summation. The output current of the DAC, $I_{dacp,n}$ feeds the input of the first integrator. The NTF determines the integrator time constants (RC). The factors which determine the absolute values of R and C are:

1) input referred noise of the system

2) node voltage swings

The input resistor R_1 is the major contributor to the input referred noise. Therefore, noise specifications determine R_1. The noise from succeeding integrators is is negligible. Therefore their impedance levels are increased to minimize power dissipation. The parasitic capacitances limit the extent to which impedance level can be increased. R or C values in individual stages are then adjusted for node scaling while preserving the transfer function.

The resistors and capacitors have process variations and the RC product varies by around 50% over the corners. This variation was overcome by having a bank of capacitors. Appropriate capacitor values are selected depending on the corner. The bank of capacitors reduces the maximum RC variation to around 5%.

By increasing the frequency of the optimized zeros, $\Delta\Sigma$ modulator can be operated with a higher bandwidth (lower OSR). The osr_ctrl signal in Fig. 4.5 controls the OSR of the modulator by increasing the frequency of optimized zeros by placing resistors $R_{x1\_10,2\_10}$ in parallel with $R_{x1,2}$.

- If osr_ctrl = 0, then OSR =25
- If osr_ctrl = 1, then OSR =10

The feed-in-capacitor C_a in Fig. 4.5 is used to provide a direct path k_0 (Fig. 3.9) across the loop filter. k_0 is given by $R_f C_a / R_1 C_1$ (with ideal opamps) [2]. C_b is used to bypass the delay introduced by the parasitics of R_b at higher frequency.

A direct path is added from the modulator input to the loop filter output through R_e [25]. The benefit of using the direct path is the reduction in the swing at the output of the third and the fourth integrators, which in turn helps in improving the

feedback factor of the summing amplifier. The direct path does not compromise the antialiasing property of the modulator as shown in [25]. The degradation in the alias rejection around f_s is given by:

$$\frac{\hat{L}_o}{L_o} = \frac{2\pi C_1 R_1 R_a}{R_e} \tag{4.7}$$

Where, $\hat{L}_o$and L_o denote the transfer function from the DSM input to the quantizer input for no direct path and with direct path respectively (from $V_{inp,m}$ to $V_{outp,m}$ in Fig. 4.5).

4.5 First opamp

The first opamp is the most critical opamp in the design of the loop-filter. The noise of the first opamp reflects directly at the input. The first opamp also the contributes to the distortion. A two stage opamp is required to provide the desired gain while driving the resistive load.

Two stage Miller compensated architectures provide high DC gain and high output swings. But the drawback is that they require a large amount of power for getting a particular bandwidth [26]. Instead, one can use feedforward compensated architectures which give the same bandwidth at much lower power but at the cost of output swing. Since we can scale down the output swings such that the opamps do not saturate, while preserving the loop-filter's transfer function, feedforward architecture was the choice for this design.

Because of the multibit quantizer used in this design, the maximum current that has to be provided by this opamp at any time is 1/(num of level) times less than that in a single bit architecture. So opamp slewing and distortion requirements are relaxed in a multibit architecture compared to a single bit CT $\Delta\Sigma$ modulator.

4.5.0.1 Feedforward compensated opamp

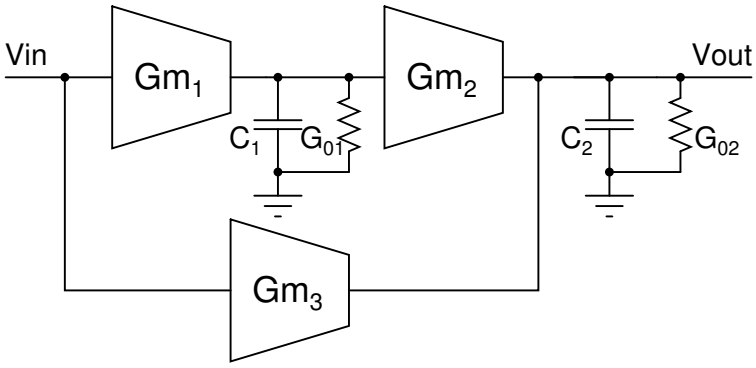


Figure 4.6: Feedforward architecture.

Figure 4.6 shows the block diagram of a feedforward compensated opamp. We can write the transfer function of the opamp as:

$$H(s) = \frac{Gm_1Gm_2 + Gm_3G_{01} + sC_1Gm_3}{(sC_1 + G_{01})(sC_2 + G_{02})} \tag{4.8}$$

The transfer function has two poles at $-G_{01}/C_1$ and $-G_{02}/C_2$ and a zero at approximately $-Gm_1Gm_2/C_1Gm_3$ [27]. The DC gain is

$$A_{DC} = \frac{Gm_1Gm_2 + Gm_3G_{01}}{G_{01}G_{02}}$$

If the zero is at a much lower frequency than the Unity Gain Frequency (UGF) of the opamp, then we get a first order (20 dB/dec) roll off at the UGF. We also get the high DC gain of a two stage opamp.

Fig. 4.7 shows the circuit diagram of the opamp used in the first integrator. The main contributor to the total noise is the first stage of the opamp. Flicker noise is not a serious issue in this design because the bandwidth of interest is assumed to be 1 MHz to 16 MHz. Yet, to reduce the flicker noise, the nMOS load transistors in first stage are chosen to have a length of 1 um. The total input referred thermal

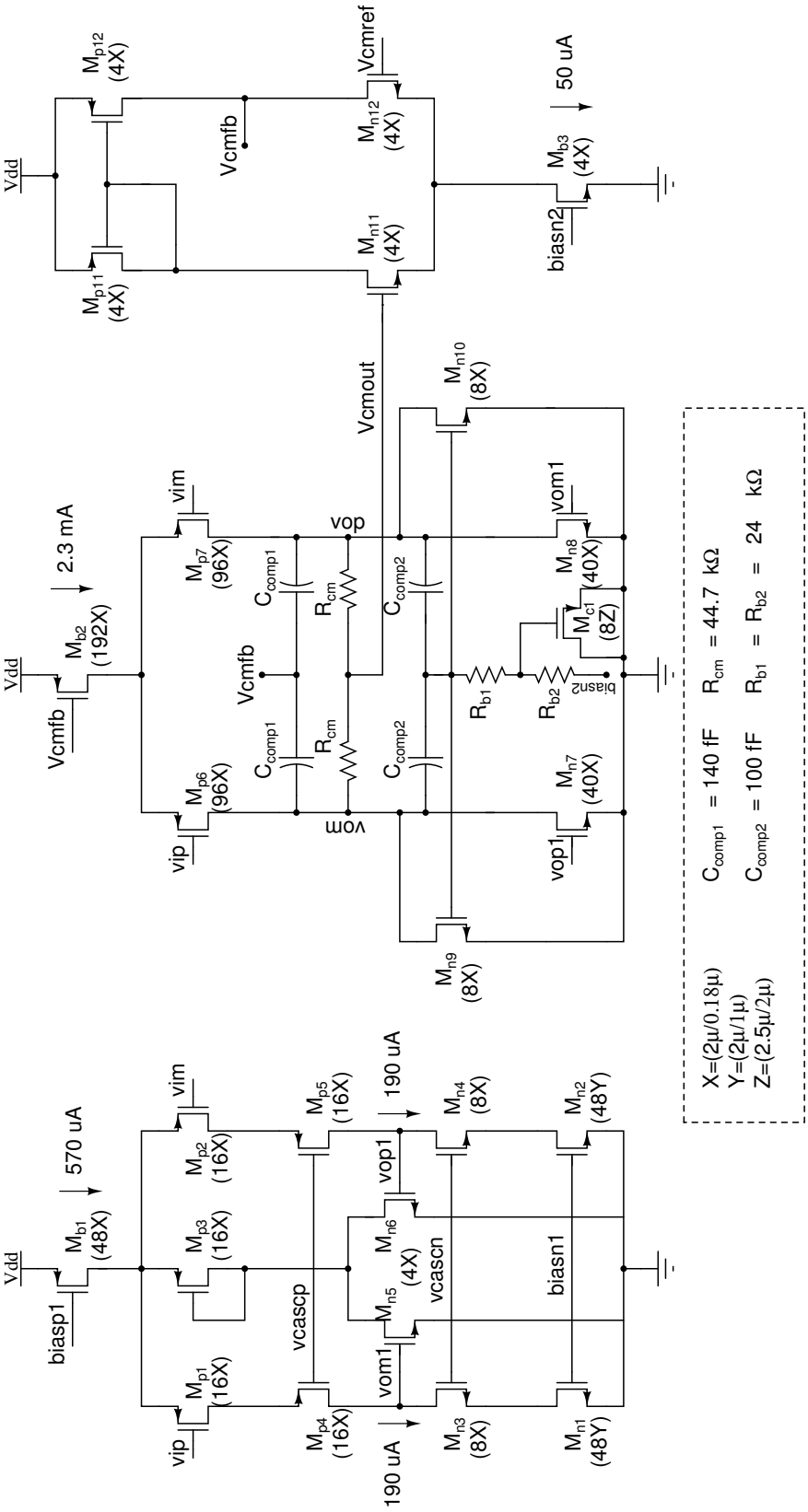


Figure 4.7: First opamp.

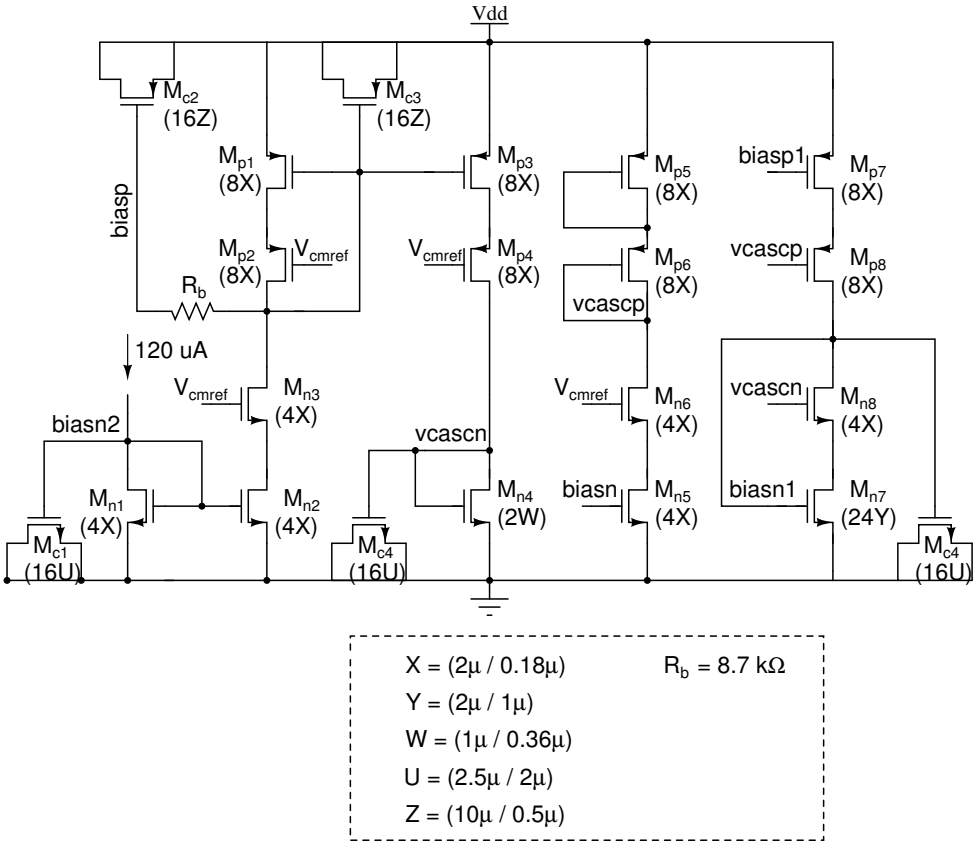


Figure 4.8: First opamp bias circuit.

noise voltage spectral density of the opamp can be roughly written as:

$$S_n(f) = \frac{16kT}{3G_{mp}}\left[1 + \frac{G_{mn}}{G_{mp}}\right] \tag{4.9}$$

where G_{mp} and G_{mn} are the transconductances of the transistors $M_{p1,2}$ and $M_{n1,2}$ respectively. Thus, to reduce the input referred noise, we need to have a large G_{mp} and a small G_{mn}. The second stage is designed such that it carries enough current to achieve the desired bandwidth. It should have enough current to supply the integrating capacitor, and the load resistors (the input resistor of second integrator, the input resistor of the summing amplifier used to realize the coefficient k_1, and the common mode sensing resistor). Transistors $M_{n7,8}$ are a scaled version of $M_{n5,6}$, used in the first stage common mode feedback circuit. $M_{p6,7}$ form the feedforward stage (Gm_3 in Fig.4.6)

4.5.0.2 CMFB circuitry

The feedforward opamp has two stages of common mode feedback. The first stage CMFB loop consists of the transistors M_{p3}, $M_{n5,6}$, $M_{p4,5}$ and $M_{p1,2}$. If the common mode level of v_{om1} and v_{op1} increases, the currents in $M_{n5,6}$ will increase which in turn will increase the current in M_{p3}. Since the total tail current is constant, this will result in an decrease in the currents in $M_{p1,2}$, thus bringing down the common mode output level of the first stage.

The second stage CMFB circuit has two loops. The first loop has the common mode sensing resistors R_{cm} and the feedback loop ensures that the dc common mode level is fixed to V_{cmref}. Since the CMFB loop has two stages, we need to compensate it by adding a miller capacitance C_{comp1} to stabilize the loop. The second loop is active at high frequencies and has $M_{n9,10}$ and C_{comp2}. At high frequencies, C_{comp2} becomes a short making $M_{n9,10}$ diode connected. Thus the phase shift around the loop is reduced at higher frequencies and the loop is stabilized. M_{c1} is used as a capacitor that shorts biasn2 to ground through resistor R_{b2}. At low frequencies biasn2 is connected to the gates of $M_{n9,10}$ through R_{b1} and R_{b2}.

Fig. 4.9 shows the magnitude and phase responses of the first opamp. Table 4.1 summarizes the opamp characteristics.

Table 4.1: Performance summary of the first opamp in the loop-filter

DC Gain	69.5 dB
Unity-gain frequency	2.3 GHz
Phase Margin	78°
Input Referred Noise (in 16 MHz Bandwidth)	13.2 μV_{rms}
Power (Vdda=1.8 V)	5.5 mW

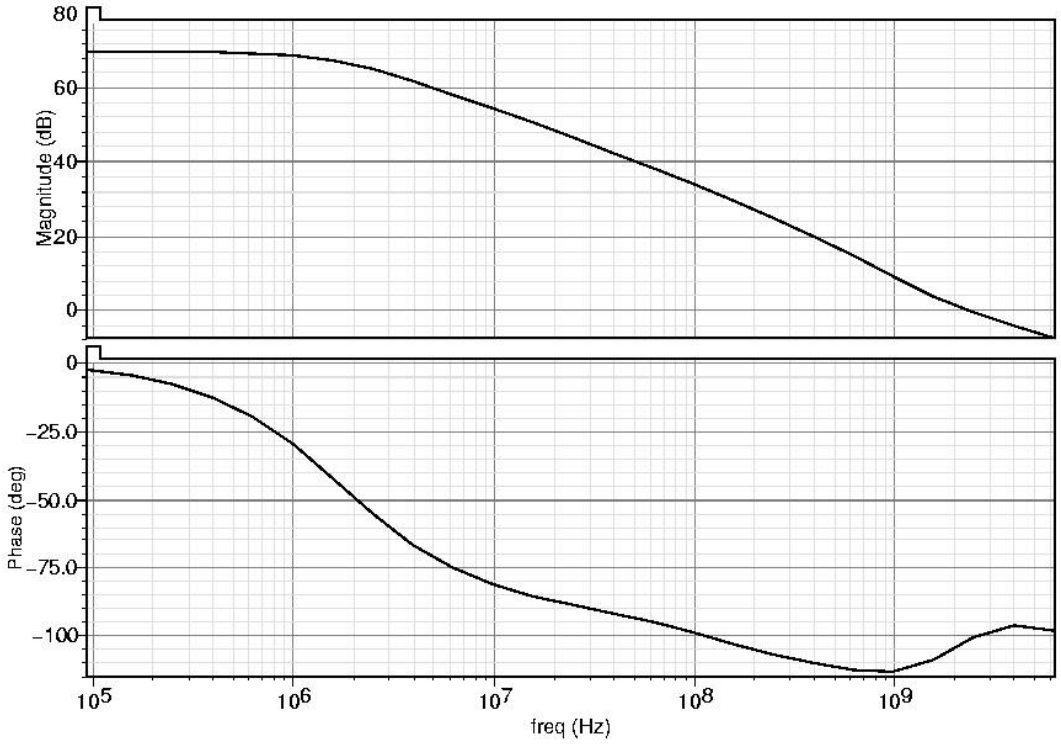


Figure 4.9: Frequency response of the first opamp.

4.6 Other integrating opamps

The noise and nonlinearities of other opamps get divided by the gain of their respective preceding stages. So the other integrating opamps have relaxed constraints on DC gain, input referred noise, unity gain frequency and slew rate specifications. Here we use nMOS input pair for the first stage to get a higher G_m for a given bias current. The only constraint is that the opamp has to supply enough current for its loads. Fig. 4.10 shows the circuit diagram of the other integrating opamps and Fig. 4.11 shows the corresponding bias circuitry. In these opamps, the additional CMFB loop ($M_{n9,n10}$ in Fig. 4.7) used in opamp1, is not required, as bandwidth requirement is relaxed in these opamps. Note that opamp1 needs to be fastest among all the four opamps used in the integrators, as it forms the fastest path (through k_1) of the loop filter.

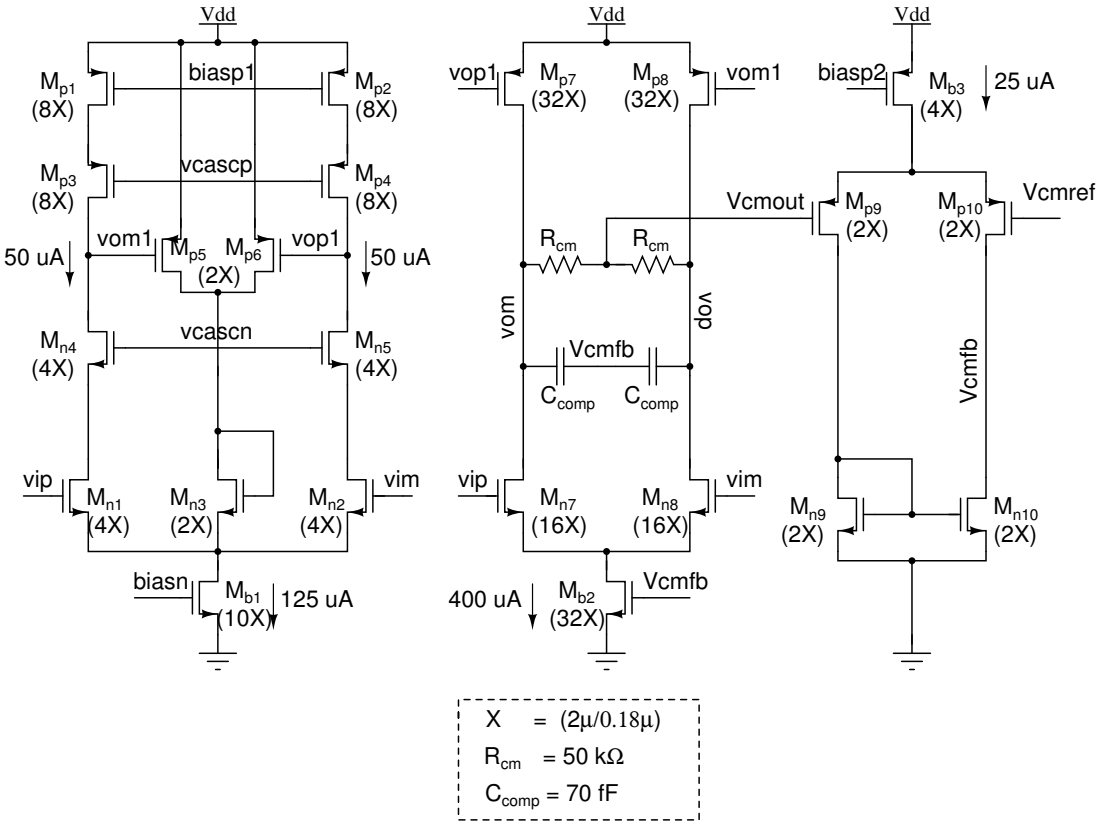


Figure 4.10: Opamp used in second, third and fourth integrators.

4.7 Summing opamp

The summing opamp has a huge capacitive load due to the 4-bit flash ADC. Also the feedback factor of the summing opamp is very small, as all the resistors realizing the feedforward coefficients of the loop filter are connected in parallel at its virtual ground node. Hence, the summing opamp has to satisfy very tight specifications on the UGF (to reduce delay), and the output swing. The bandwidth of the summing amplifier has to be greater than f_s to ensure that the pulse response of the summing amplifier settles within one clock period. The swing at the output of the opamp is $3V_{pp,d}$. So the headroom for the output stage is only $300mV_{pp}$. So we cannot use the feed-forward architecture that was used for the integrating opamps. Another option is to use the miller compensated two stage opamp. The miller opamp solves the swing problem, but it takes a lot of power to get the desired UGF. This motivated us to look for an architecture that combines the feedforward

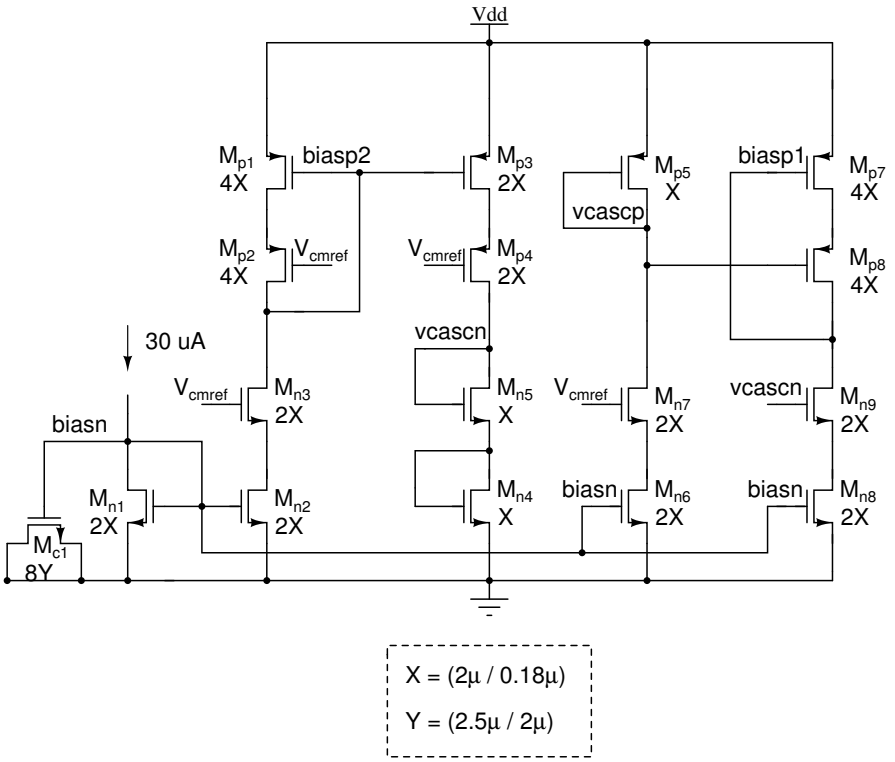


Figure 4.11: Bias circuit for the opamp shown in Fig. 4.10.

compensation which realizes a higher UGF for a given power consumption and a common source amplifier second stage which provides a high output swing. The swing limitation of the feedforward opamp architecture in Fig. 4.6 is due to the presence of Gm_3 directly between the input and output nodes. Gm_3 has to be a differential pair with a tail current source in order for the opamp to have common mode (CM) rejection. Therefore the only option to obtain large output swing is to split the feedforward stage into two stages as shown in Fig. 4.12. Gm_3' is a differential pair with high CM rejection and Gm_3 is a common source amplifier with high output swing. It has to be ensure that the pole at the output of Gm_3' is at a sufficiently high frequency.

The transfer function is given by:

$$H(s) = \frac{\frac{Gm_1Gm_2}{G_{01}G_{02}}\left(1+\frac{sC_3}{G_{03}}\right) + \frac{Gm_3Gm_3'}{G_{02}G_{03}}\left(1+\frac{sC_1}{G_{01}}\right)}{\left(1+\frac{sC_1}{G_{01}}\right)\left(1+\frac{sC_2}{G_{02}}\right)\left(1+\frac{sC_3}{G_{03}}\right)} \tag{4.10}$$

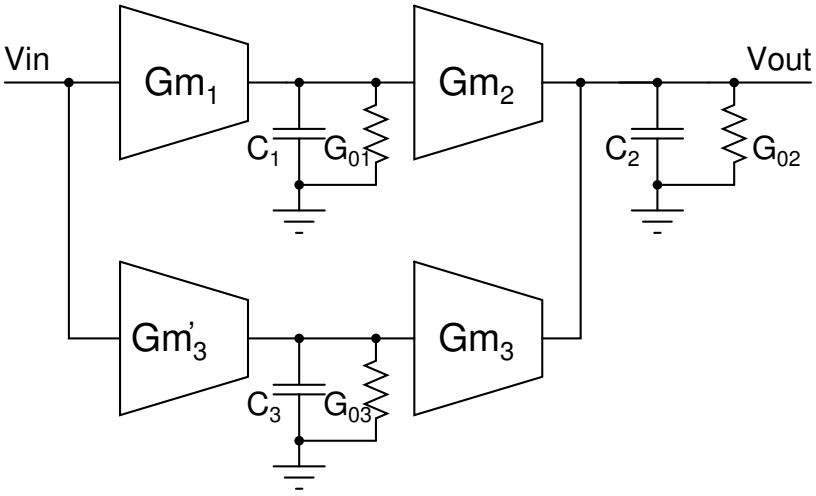


Figure 4.12: Summing opamp feedforward architecture.

G_{03} is equal to $Gm'_3/4$, to get a gain of four from this stage. Gm'_3 is chosen large enough such that the nondominant pole G_{03}/C_3 is much higher than the closed loop unity gain frequency. So, we can neglect the this pole and Eq. 4.10 can be modified as below

$$H(s) = \frac{\frac{Gm_1Gm_2}{G_{01}G_{02}} + \frac{Gm_3Gm'_3}{G_{02}G_{03}}\left(1+\frac{sC_1}{G_{01}}\right)}{\left(1+\frac{sC_1}{G_{01}}\right)\left(1+\frac{sC_2}{G_{02}}\right)} \tag{4.11}$$

The transfer function has two poles at $-G_{01}/C_1$ and $-G_{02}/C_2$ and a zero at approximately $-Gm_1Gm_2G_{03}/C_1Gm_3Gm'_3$. The DC gain is

$$\frac{Gm_1Gm_2G_{03} + Gm_3Gm'_3G_{01}}{G_{01}G_{02}G_{03}}$$

Recalling that the zero in the standard feedforward architecture is at $-Gm_1Gm_2/C_1Gm_3$, in this new architecture:

- The zero is brought to a lower frequency.
- The effective feedforward Gm is increased by as factor Gm'_3/G_{03}. So now, the open loop unity gain frequency is $Gm_3Gm'_3/C_2G_{03}$.

Circuit details of this feedforward opamp is shown in Fig 4.13. In the conventional

feedforward opamp (Fig 4.10), output swing is limited by the threshold voltage of nMOS ($M_{n7,8}$) because the input and the output of the opamp have the same common mode voltage. But in this architecture, the second stage input common mode voltage is independent of the output common mode voltage. For a higher output swing the output stage has to be a common source amplifier with its input biased at one V_{GS} above the ground. For this, G'_{m3} is ac coupled to G_{m3} through the capacitor C_b. G'_{m3} is implemented with the nMOS input pair and diode connected nMOS loads to have a gain of $\beta = 4$. An nMOS load is used instead of a pMOS load to have smaller parasitics and hence a larger ω_{p3}. CMFB of second stage is provided by sensing the common mode voltage through R_{cm} and feeding back the current through $M_{p11,12}$. CMFB through current feedback eliminates the tail current transistors in the second stage, and results in a larger swing. Table 4.2 summarizes the summing opamp characteristics.

Table 4.2: Performance summary of the summing opamp in the loop filter.

DC Gain	63 dB
Unity-gain frequency (Load capacitor is 600 fF)	4.3 GHz
Phase Margin	14°
Power (Vdda=1.8 V)	8.5 mW

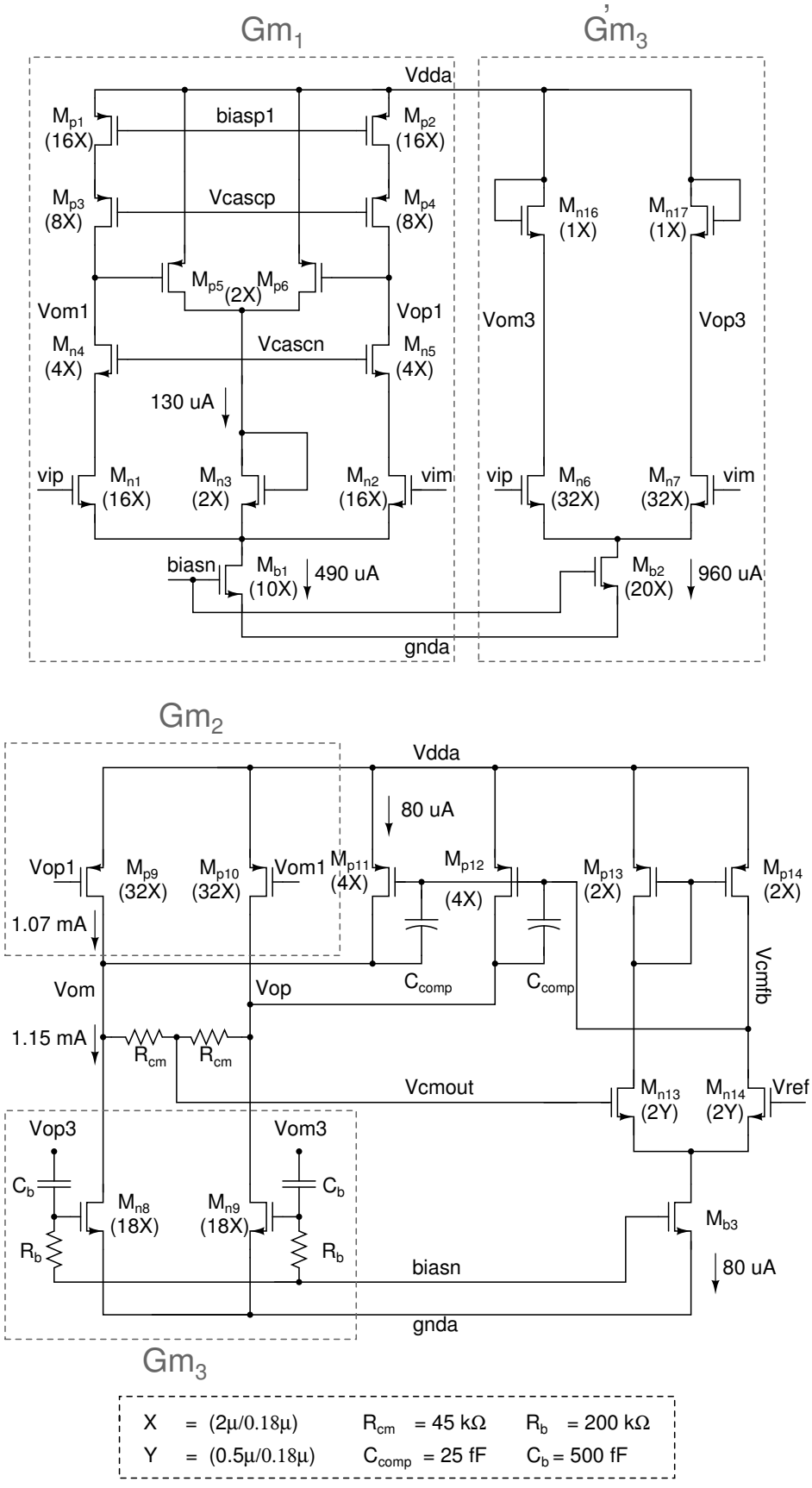


Figure 4.13: Summing opamp.

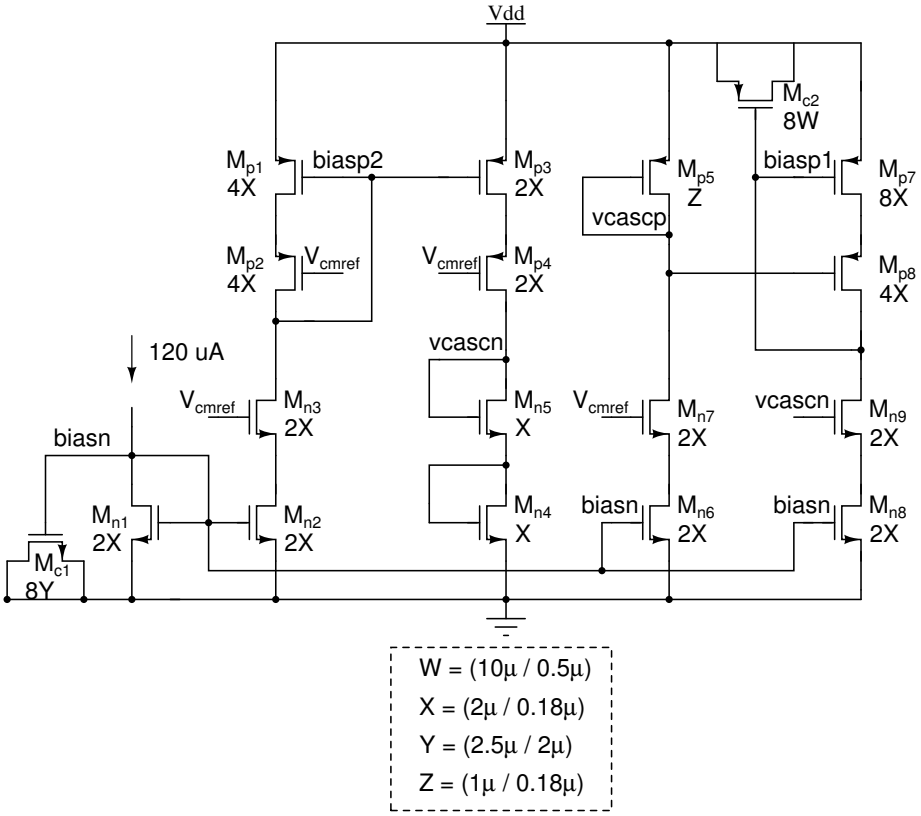


Figure 4.14: Summing opamp bias circuit.

CHAPTER 5

High speed parallel feedback path components

5.1 Architecture

We have seen in Chapter 3 that a fast loop excluding the quantizer is required to compensate for quantizer delay of more than one clock cycle. Fig. 5.1 (a) shows the block diagram of this fast loop, were a zero-order hold is cascaded with the gain stage. The gain coefficient a is the magnitude of the second sample of the NTF impulse response. The zero-order hold is realized using a S/H as shown in Fig. 5.1 (b). The gain stage is realized using a G_m cell whose output is connected to the virtual node of the summing opamp as shown in Fig. 5.1 (c). Transconductance of the G_m cell has to be a/R, for realizing the second sample of value a. In the following sections, we will discuss the circuit level details of the S/H and the G_m cell.

5.2 S/H

An open-loop architecture was chosen because of its ability to operate at higher speeds. The simplest open-loop S/H is constructed from an nMOS switch and holding capacitor. The nonlinearity of the S/H does not contribute to the ADC nonlinearity because of the high gain of the preceding loop filter.

Fig. 5.2 shows one half of the pseudo differential S/H circuit. The S/H is formed using a cascade of two track and hold stages operated by alternate clock phases Φ_1 and $\bar{\Phi}_1$. Source followers formed using transistors M_1 and M_2 act as input buffer for the two track and hold stages.

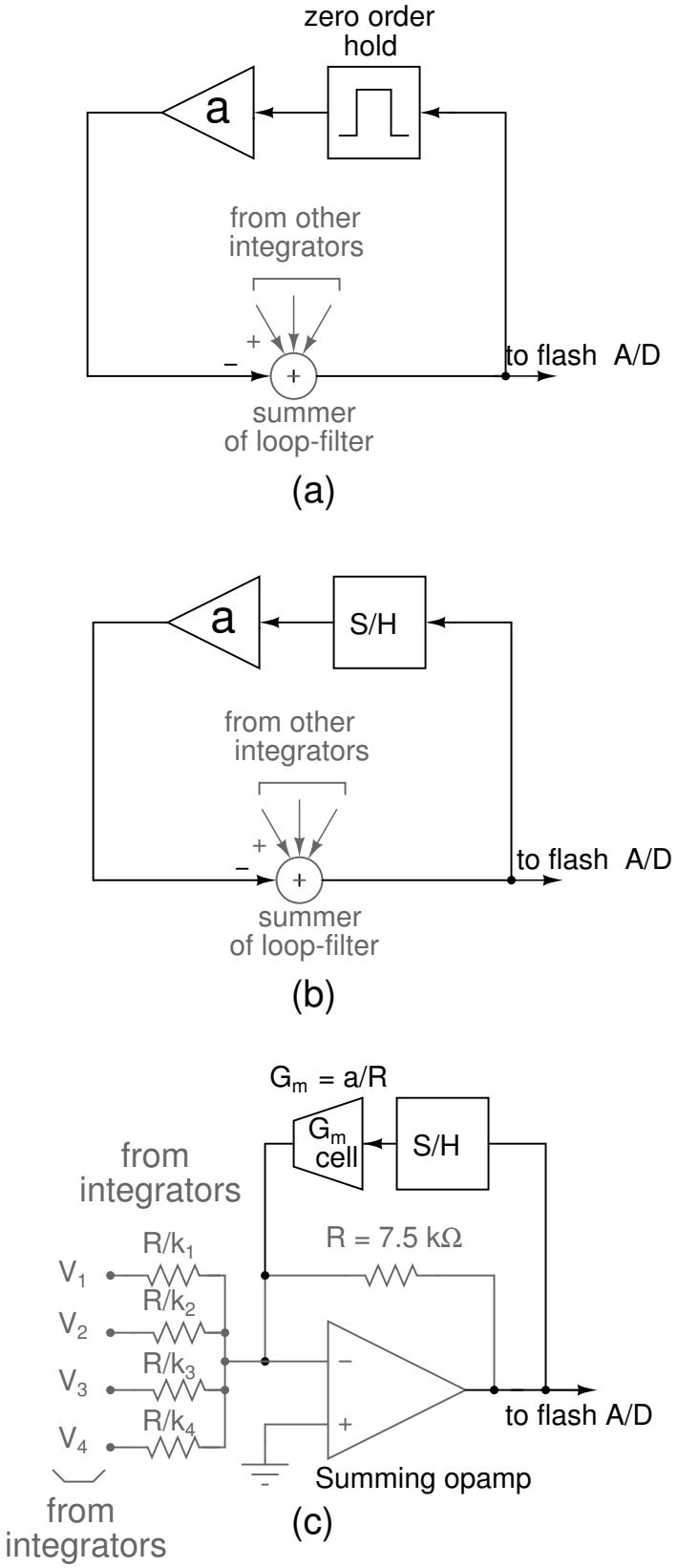


Figure 5.1: (a) Fast loop ELD compensation (see Fig. 3.16) (b) S/H as zero-order hold. (c) G_m cell as gain stage. (Single ended equivalent)

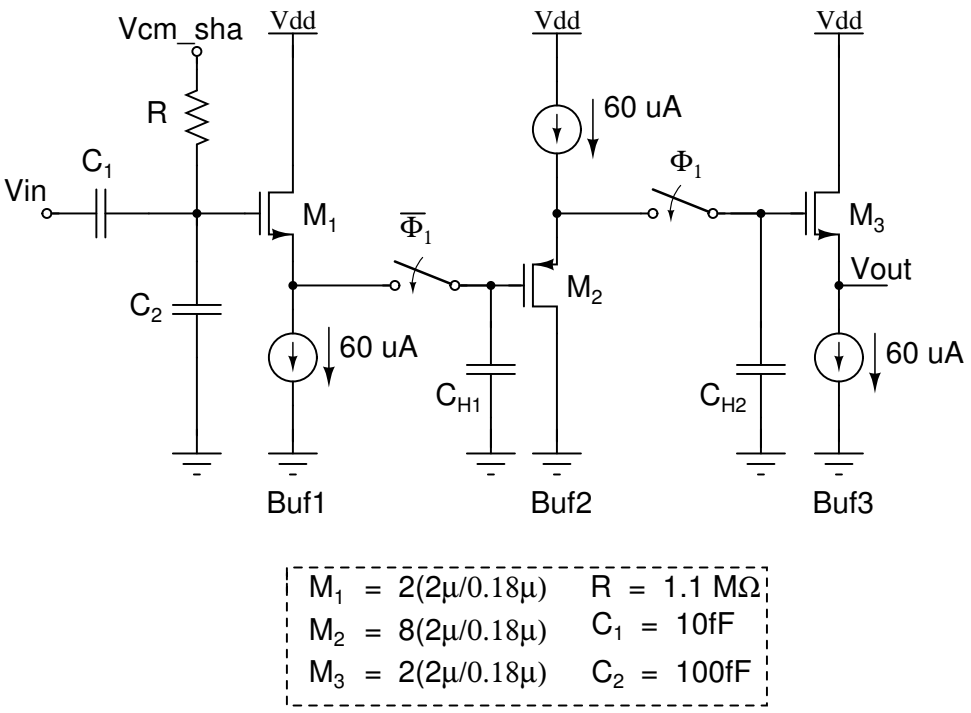


Figure 5.2: S/H circuit (One half of the pseudo differential structure.)

A capacitive attenuator with C_1 and C_2 is used at the input to reduce the signal swing ($C_1/(C_1+C_2)$) requirement of the buffers. The reduction in the input signal swing is compensated by providing a correspondingly higher gain in the G_m cell. A source follower M_3 serves as the output buffer to drive the G_m cell. The parasitic capacitances at the gates of M_2 and M_3 are sufficiently large and therefore, C_{H1} and C_{H2} are not explicitly realized. Resistor R is used to provide the DC bias point to the gate of M_1. The voltage Vcm_sha is derived from the analog supply voltage by means of a simple potential divider. The output of the attenuator is buffered by source follower M_1 before being fed into the first sampler having C_{H1}. The input buffer is needed so that the previous stage sees a constant load. The source follower M_1 isolates the input from switching activity of the sampler. $M_{1,2,3}$ have their body and source terminals are tied together to avoid distortion and attenuation due to body effect.

In order to reduce nonlinearity, the sampling switch is implemented as a"constant gate-overdrive" switch as shown in Fig. 5.3. Here the capacitor C_3 is charged to

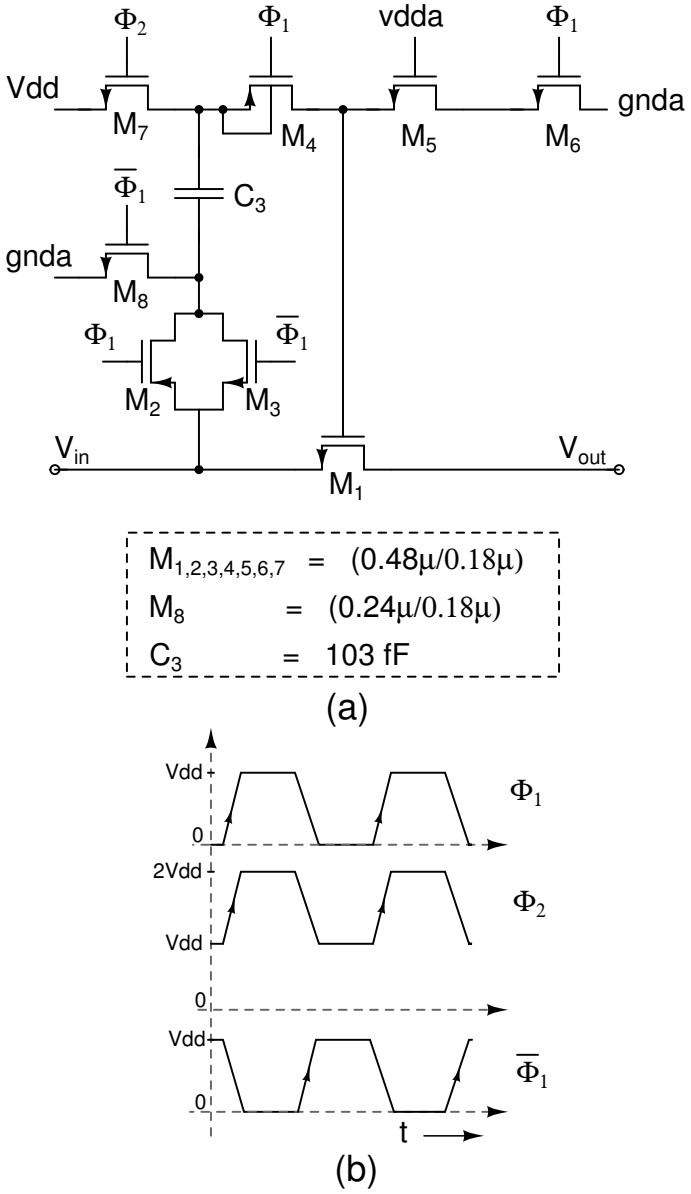


Figure 5.3: (a) Bootstrapped switch. (b) Clock waveforms for the bootstrapped switch.

the voltage Vdd during the hold phase (Φ_1 being high). During the track phase ($\bar{\Phi}_1$ being high), the bottom plate of C_3 is connected to the input signal whereas the top plate is connected to the gate of M_1 through M_4. Thus the gate-to-source voltage of M_1 during tracking mode is constant [28].

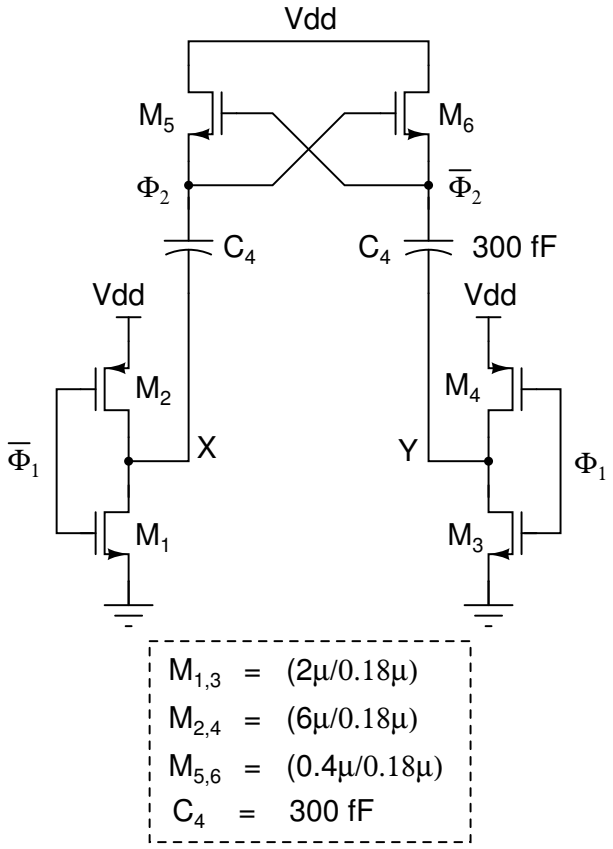


Figure 5.4: Charge pump to generate clock with levels 2Vdd and Vdd.

A charge pump is used to generate 2Vdd and Vdd for Φ_2. Fig. 5.4 shows the schematic of the charge pump. When the Φ_1 is high, bottom plate of C_4 is connected to gnda, through M_1 and top plate is charged to Vdd through M_5, which is acting as current source. When Φ_1 goes low, the bottom plate of C_4 sees a jump of Vdd and hence top plate of C_4 also jumps by Vdd to 2Vdd. So Φ_2 toggles between 2Vdd and Vdd following the Φ_1 signal [29].

5.3 G_m cell

The circuit schematic of the G_m cell used after the S/H is shown Fig. 5.5. The

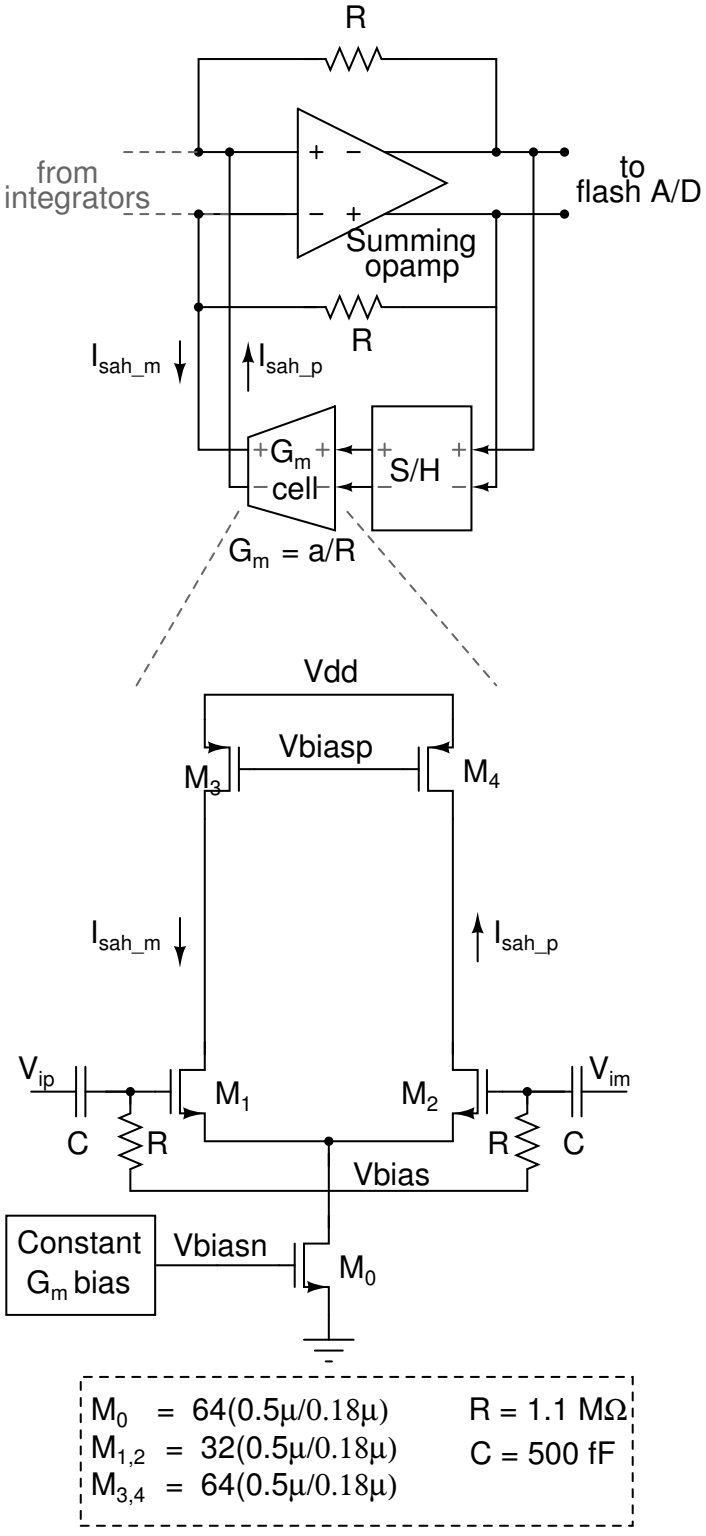


Figure 5.5: G_m cell.

output of the S/H is ac coupled to its input through the capacitor C. To realize the coefficient a, the transconductance G_m has to be:

$$G_m = \frac{a}{R_f}\left(\frac{C_1 + C_2}{C_1}\right) \tag{5.1}$$

where a is the second sample of the ideal NTF impuse response. R_f is the feedback resistor around the summing opamp used in the loop filter. The output of this G_m cell is fed back to the virtual node of the summing opamp to from the *fast loop* of the modulator.

The G_m cell is biased using a fixed G_m, so that the G_m of transconductor can track $1/R$ across all process corners and the second sample value remains unchanged across all process corners. The fixed transconductance bias used in this work is based on the design proposed in [6]. The circuit diagram is shown in Fig. 5.6.

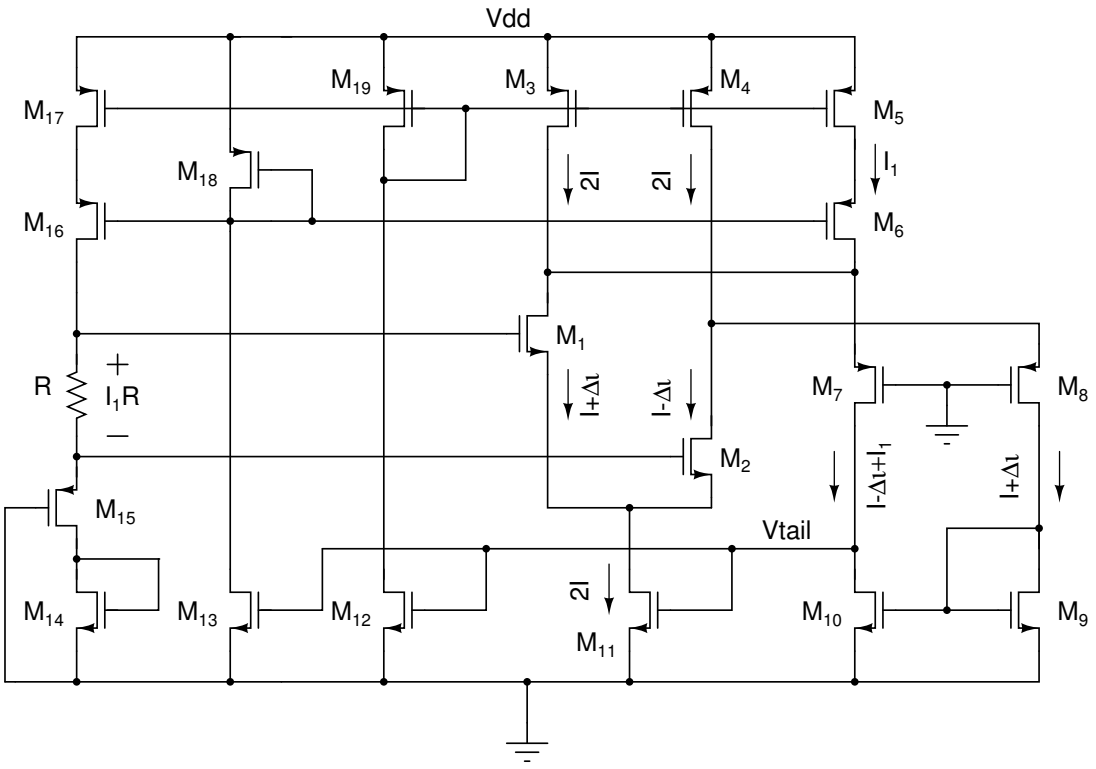


Figure 5.6: Fixed-G_m bias circuit [6].

The devices whose transconductance needs to be fixed are M_1 and M_2. In steady

state, the feedback in the circuit ensures that the currents in M_9 and M_{10} are equal. This gives:

$$I + I_1 - i_1 = I - i_2 \tag{5.2}$$

$$i_1 - i_2 = I_1 \tag{5.3}$$

The differential current $i_1 - i_2$ due to a small incremental voltage I_1R is given by the relation:

$$i_1 - i_2 = G_{m,M_1}.I_1R \tag{5.4}$$

Substituting 5.3 in 5.4, we have

$$G_{m,M_1} = \frac{1}{R} \tag{5.5}$$

The resistance R is the replica of the feedback resistor around the summing opamp of the loop filter. This design is robust in various aspects namely:

- It is not dependent on the MOSFET square law.
- It is independent of supply voltage and temperature variations.
- It is not affected by the output impedance of the transistors and back-gate effect [6].

The design details of the fixed transconductance bias used in this design is shown in Fig. 5.7.

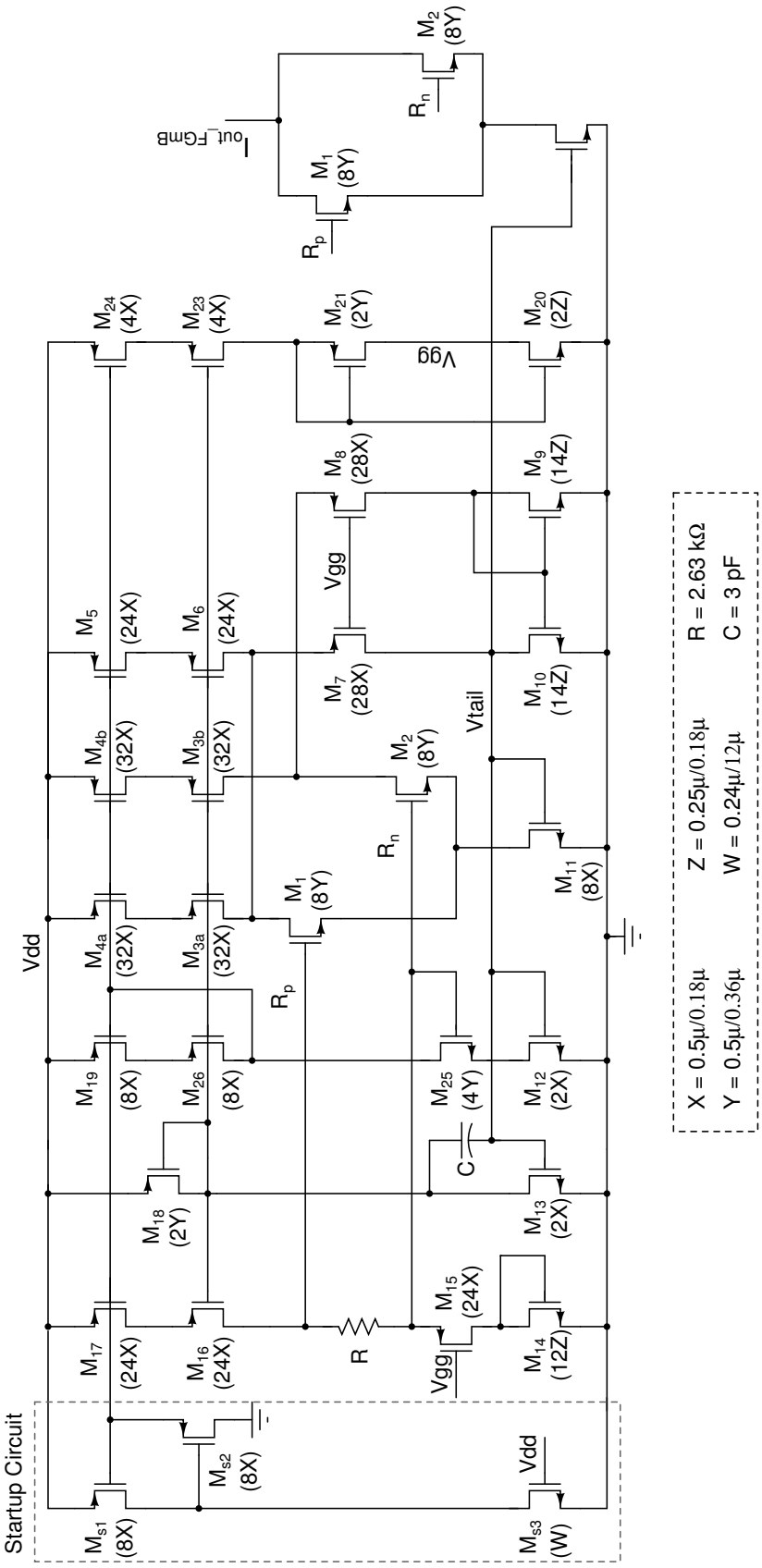


Figure 5.7: Fixed-G_m bias circuit used in this work.

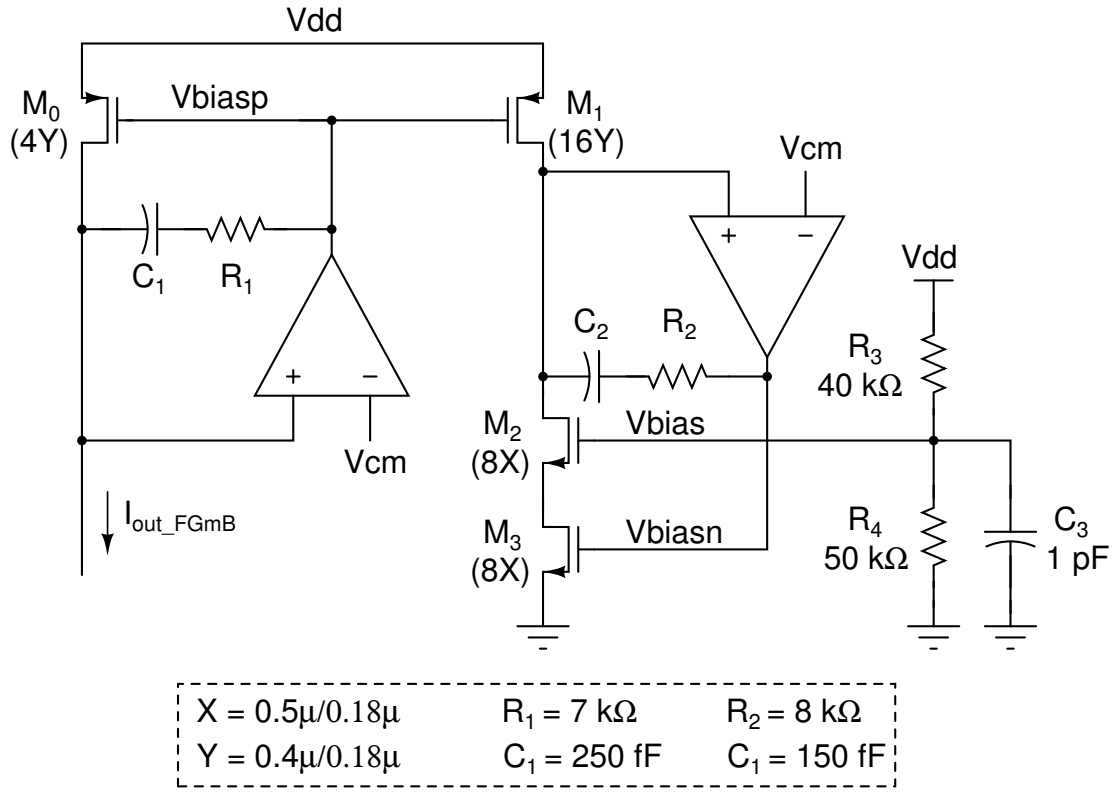


Figure 5.8: Biasing circuit for the G_m cell shown in Fig. 5.5. (The output from Fig. 5.7 is the input to this circuit.)

The circuit in Fig. 5.8 accepts the current from the constant G_m bias generator (Fig. 5.7) and provide the bias voltage V_{biasn} to the G_m cell in Fig. 5.5. It consists of a pMOS current mirror $M_{0,1}$ followed by an nMOS stack $M_{2,3}$ which are the replicas of $M_{1,2}$ and M_0 respectively in Fig. 5.5. Opamps are used to force equal V_{DS} across transistors in a mirror realize accurate current mirroring. Single stage opamps consisting of a differential pair and a current mirror are used in Fig. 5.8 [21].

CHAPTER 6

4-bit flash ADC

6.1 Introduction

The ADC used in this modulator is the 4-bit flash ADC. Flash architecture is a popular approach for designing high-speed low-to-medium resolution converters. Fig. 6.1 shows the block diagram of flash ADC, where the full scale of ADC is divided into $(2^n - 1)$ number of levels and the input is compared with each of this levels. The comparison is done using $(2^n - 1)$ comparators(one for each level) and is done in parallel. The result of the comparison is a $2^n - 1$ bit code and is always of the form of the string of $1's$ followed by a string of $0's$. Such a code is called thermometer code. This thermometer code is later converted to binary code as per the need of external circuitry. The drawback of this architecture is the exponential increase in comparators per increase increase in bit. The references for the comparators are generated using a resistive ladder running between fullscale voltages. Since the implementation is differential, a pair of differential references are required for each of the comparators. This is achieved by running two resistive ladders in parallel in an intertwined fashion and feeding the corresponding node voltages to each of the comparators.

The output of this ADC is a thermometer code which drives the feedback DAC and the thermometer-to-binary converter that follows it.

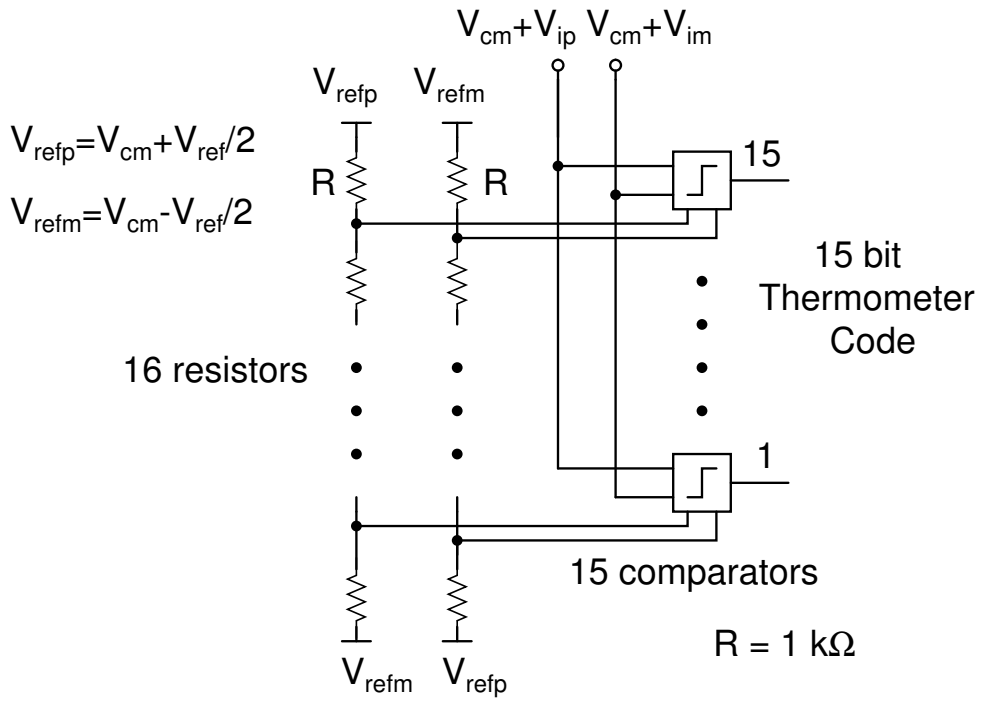


Figure 6.1: Block diagram of the 4 bit flash A/D.

6.2 Drawbacks of CMOS comparators

CMOS latch is used for 300 MHz operation in [7]. This section discusses the issues that were faced while extending this architecture to higher speeds.

The first problem that we faced while trying to increase the frequency of operation is the current drawn by the latch when we turn it on or off. Evidently, as we increase the frequency of operation, the reactive currents increase due to a reduction in the capacitive impedances. This would imply increased drops across the switches thereby resulting in subtraction errors. It was found that around 500 MHz, these drops were of the order of 25 mV differential as compared to the differential LSB of 187.5 mV . Tracing the currents drawn by the comparator showed that most of the current flowed into the latch indicating that this was the primary source of trouble. There are four issues with the operation of the CMOS latch shown in Fig. 6.2.

- Shared input and output of the latch
- Resetting the input nodes of the latch

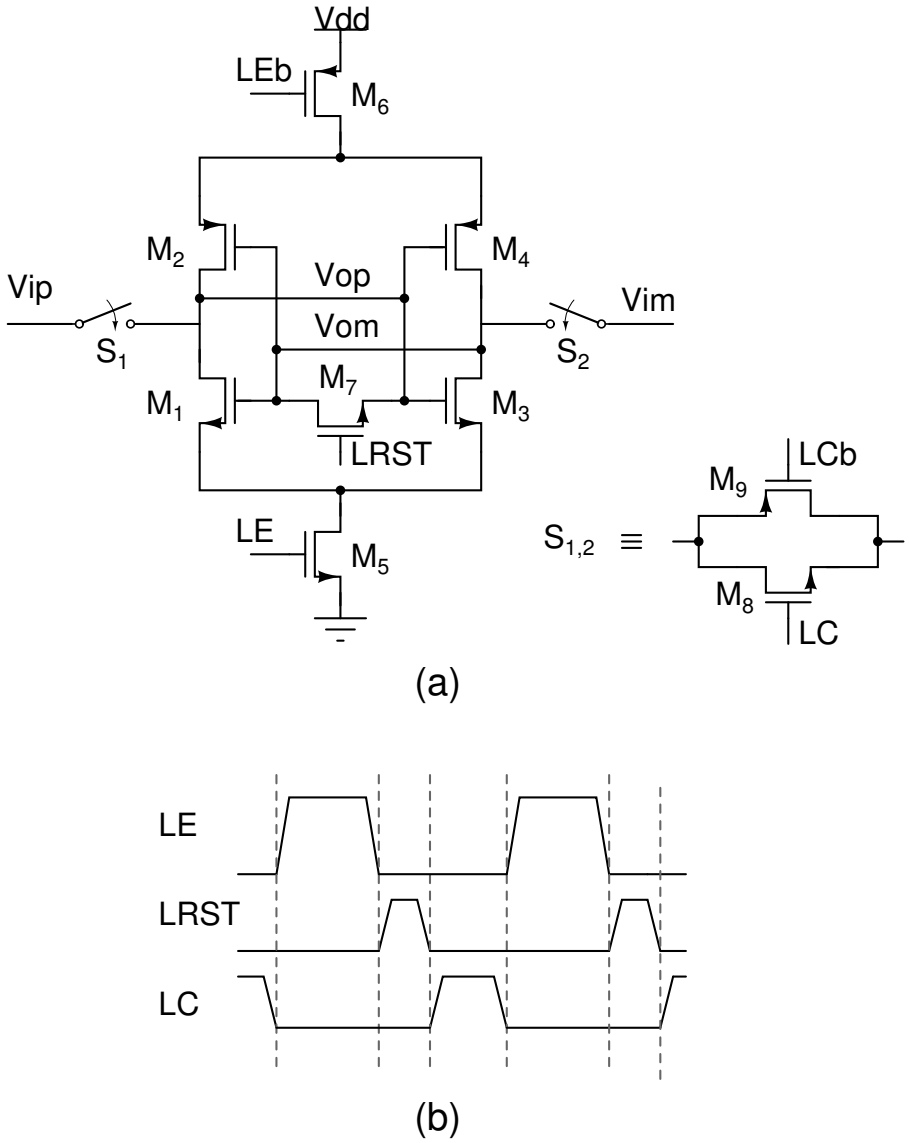


Figure 6.2: (a) Schematic of the CMOS latch used in [7] (b) Clock waveforms used for the latch.

- Common mode noise
- Clocking

These issues are described in detail in [30]. These issues can be overcome using a truly differential topology with isolated input and output for the latch. One such latch is the current mode logic (CML) latch and will be discussed in next section.

6.3 CML latch

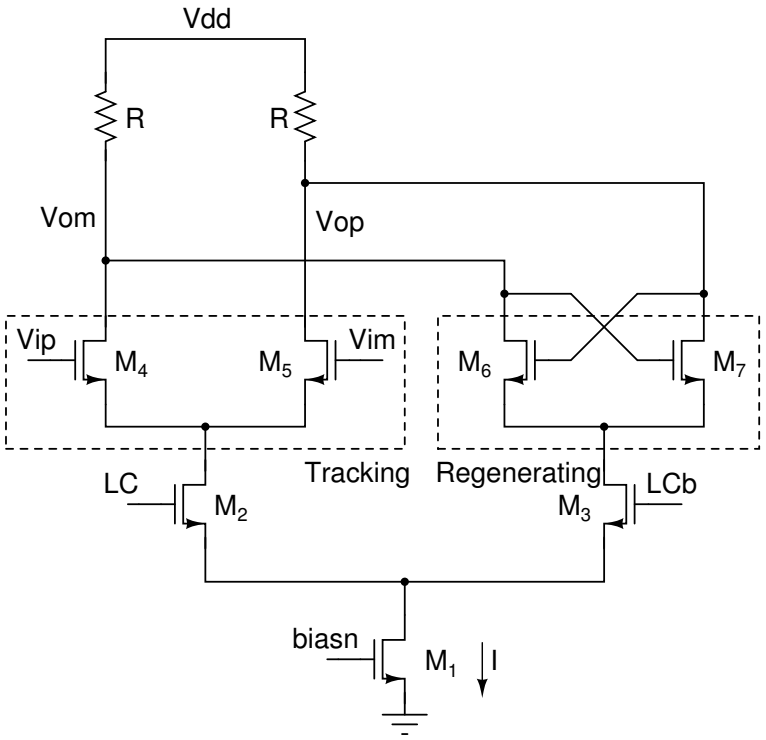


Figure 6.3: CML latch.

A standard CML latch is shown in the Fig. 6.3. This is constructed from a CML inverter/buffer which is a simple differential pair. The CML inverter has two outputs one being the exact complement of the other. As a result, to construct a latch we need only one CML inverter and connect its outputs back to the inputs in positive feedback. To separate the input and output of the latch and to supply the input of the latch to the regenerating section, we make use of another CML inverter whose outputs are connected to the regeneratively connected CML inverter.

During the phase when the latch is expected to track/amplify the input, the normal CML inverter branch is enabled by enabling LC. When it is expected to regenerate, the regeneratively connected CML inverter is enabled by enabling LCb. If we assume infinite output impedance for all transistors (as they are maintained in saturation), the input common mode does not affect the output common mode for the normal CML inverter block. Therefore the output common mode is $Vdd - IR/2$. The tail current in the tracking and regenerating phases are the same. Therefore there is no change in the output common mode voltage, when changing from one phase to another, and the dynamic offset of the latch is greatly reduced.

6.4 Comparator architecture

The block diagram of the comparator and the corresponding clock waveforms are shown in Fig. 6.4(a) and (b) respectively. The comparator operates as follows.

The node X and Y are connected to V_{ip} and V_{im} through two coupling capacitors C_c, which have been periodically charged two $V_{refp} - V_{cm}$ and $V_{refm} - V_{cm}$ respectively through the two capacitors C_b (When LC is high). The two capacitors C_b act as floating batteries of voltage $V_{refp} - V_{cm}$ and $V_{refm} - V_{cm}$ respectively which are generated using *single ended references* V_{refp}, V_{refm} and V_{cm} (When LE is high). The LC and LE are non-overlapped clocks that are operated at $f_s/4$ instead of f_s. This improves the performance considerably because there is 4 times more time for settling.

The input reference subtractor is cascaded with three latches to provide enough gain for complete regeneration and to reduce the metastability problem. A buffer is cascaded with the output of the Latch3 to clean-up the ripple in the waveform and to drive the feedback DAC and the digital backend. Latches and buffers are implemented using current mode logic (CML) and will be discussed in section.

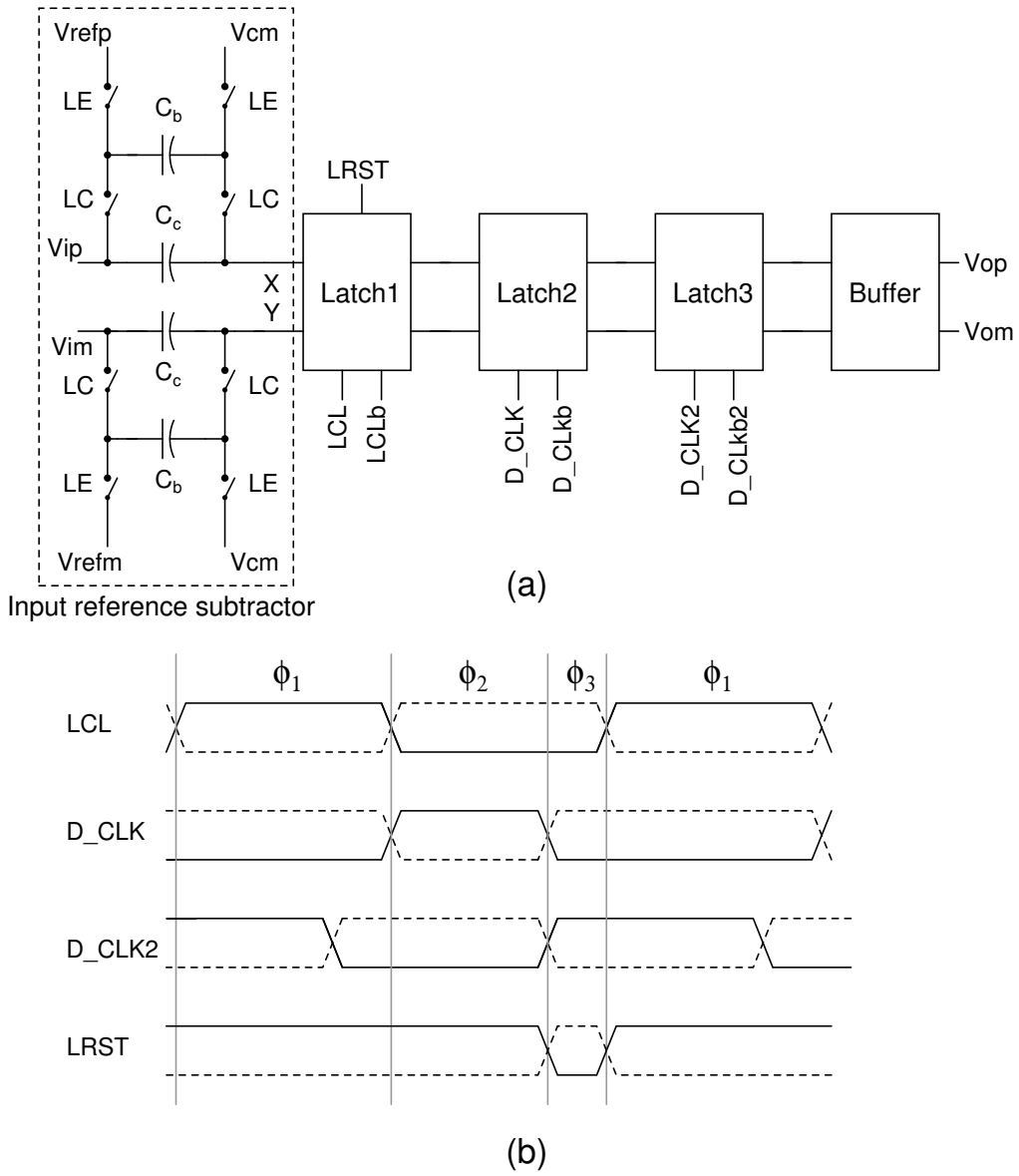


Figure 6.4: (a) Block diagram of the comparator. (b) Clock waveforms.

6.5 Design of latches

6.5.1 Latch1

A schematic of Latch1 which resolves the difference between the input and the reference voltage is shown in Fig. 6.5. The latch is driven by a pair of complementary clock LCL and LCLb. During the track phase, LCL is high and $M_{4,5}$ track/amplify the input. During regenerating phase, LCLb is high and $M_{6,7}$ regenerate the Vop and Vom to Vdd and $Vdd - IR$ or vice-versa. Here I is the tail current through

M_1. Resetting the latch is done towards the end of the regenerating phase of the Latch1 (by pulling down LRST).

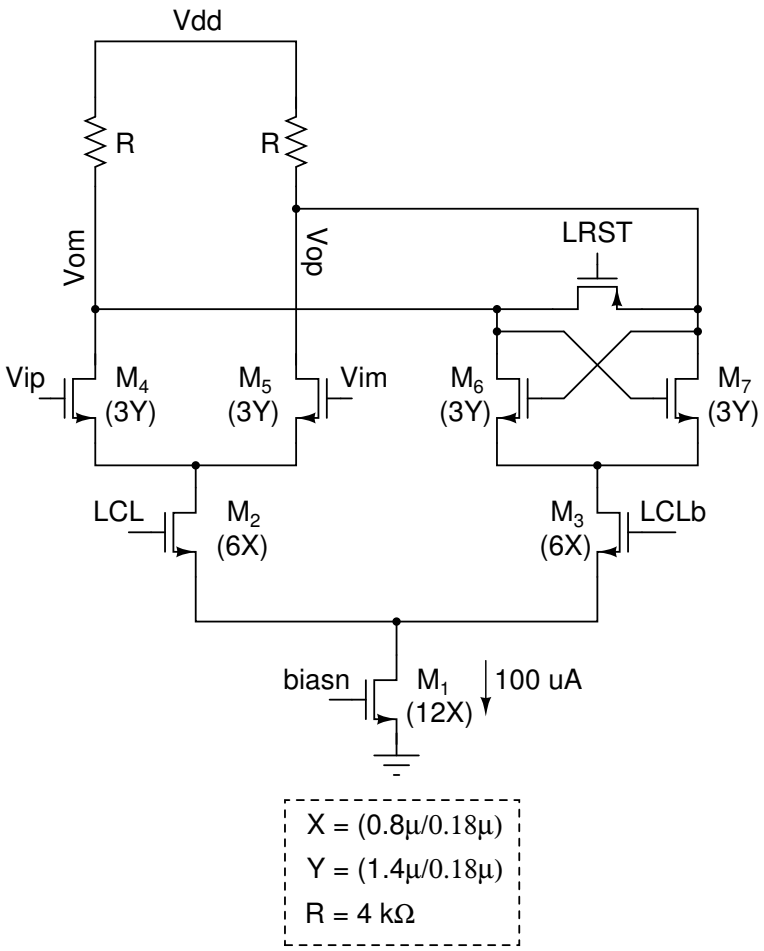


Figure 6.5: Latch1 in Fig. 6.4.

6.5.2 Latch2,3

Since the Latch1 is reset every clock cycle, Latch2 is needed to stored the desired logic level. A schematic of the Latch2 is shown in Fig. 6.6. This latch provides us with some more gain and holds the output for one full clock cycle. In order to save time however, this latch tracks the input when the first latch is regenerating. In other words, we do not wait for the first latch's output to regenerate to enable the second latch. It was found that the second latch was also not always able to resolve the input voltages and hence another CML latch, Latch3 is added at the output to make sure that waveform is completely regenerated. Latch3 is identical

to Latch2.

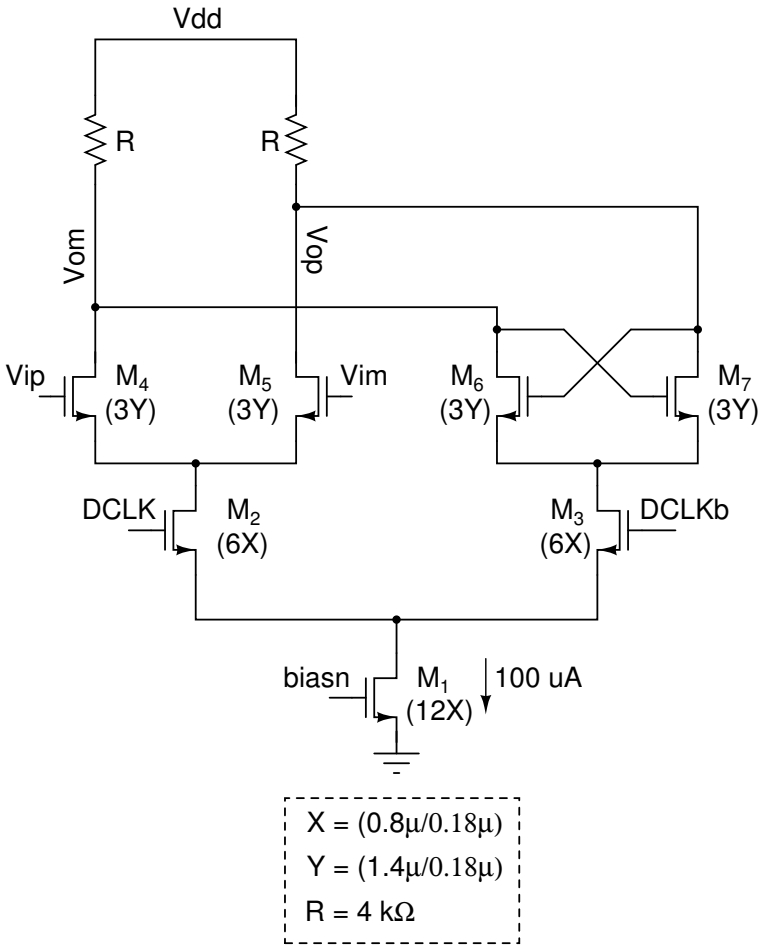


Figure 6.6: Latch2, 3 in Fig. 6.4.

6.5.3 Buffer

Due to the finite output impedance of the current sources in the latches, the tail node parasitic capacitance along with the dip in the output voltage when the current switches from one arm to the other cause a lot of ripple in the output voltage. An output buffer, shown in Fig. 6.7, is used to clean up this ripple.

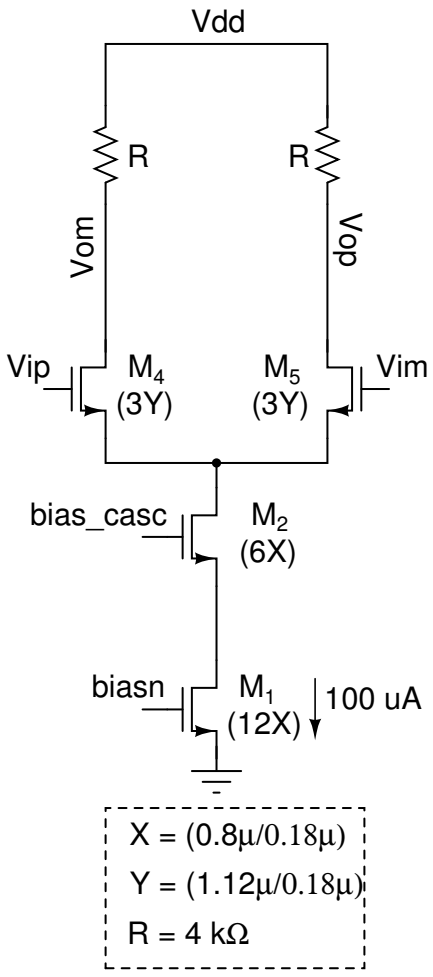


Figure 6.7: CML Buffer in Fig. 6.4.

6.6 Clocking

It can be seen from Fig. 6.4 (a), that following clocks are required: LC, LE, LCL, LCLb, D_CLK, D_CLKb, D_CLK2, D_CLKb2, LRST. Out of these, LC and LE are independent clocks and D_CLK2 and D_CLKb2 are the delayed version of LCL and LCLb respectively. So the available time period of $1/f_s = 1.25\,\text{ns}$ has to be now appropriately divided amongst the remaining clocks - LCL, LCLb, D_CLK, D_CLKb, LRST.

Here, LCL and LCLb are complementary and so are D_CLK and D_CLKb. The period for which LCL is ON controls the time available for the output of the first latch to start tracking the input waveform. Therefore, increasing the duty cycle of LCL would to a certain extent increase the tracking ability of the latch.

Unlike the CMOS latch, the CML latch need not be turned off when resetting it. We therefore reset the first latch towards the end of it's regeneration phase. We therefore, choose to use 50 % duty cycle clocks for LCL and LCLb while placing the reset towards the end of the regenerating cycle turning off along with the rise of LCL. Also, since the output of the first latch has to be stored on to the second latch before reset, D CLK has to turn off before LRST goes high. In order to save

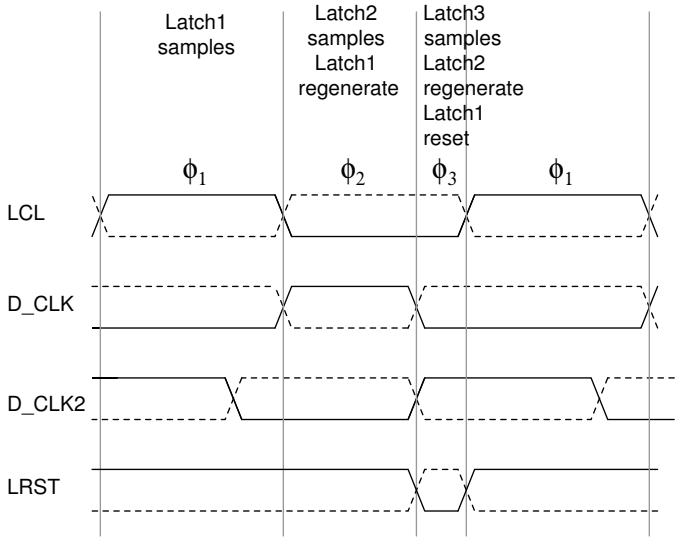


Figure 6.8: Timing diagram of the clocks used for the latches.

time, we let the second latch to be in tracking phase when the first latch is in it's regenerating phase. As soon as Latch2 switches to the regeneration phase, Latch3 goes to track phase for 50 % duty cycle providing higher gain for the regeneration. This however has the drawback that the output waveform of the third latch shows a lot of ripple even in a completely switched state. The purpose of the CML buffer which follows the second latch, is to clean up this ripple and add some gain to the signal path. The subtraction stage is asynchronous with the rest of the circuit. They are generated by using a $f_s/4 = 200\,MHz$ clock and a non-overlapping clock generator. Rising edge of LCLb is the sampling instant. Data is available at the output of comparator after rising edge of D_CLK2. The timing diagram of the clocks is redrawn in Fig. 6.8 for readability.

6.7 Flash reference level generation

The 4-bit flash ADC designed in this work operates with a full scale of $3V_{ppd}$. This implies that the flash operates with reference voltage levels as linear divisions of voltages 1.5 V apart and centrally located in the available voltage range $0 - 1.8\,V$. In other words, the reference voltages for the comparator array V_{refp} and V_{refm} are 1.65 V and 0.15 V. These voltage references should be able to supply

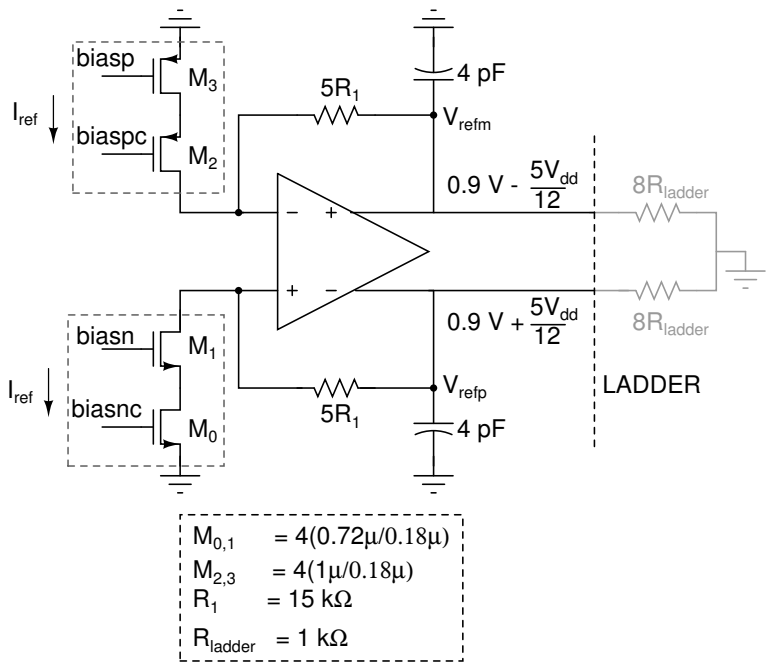


Figure 6.9: Circuit which generates the flash reference levels.

a current $\dfrac{1.5}{16R_{ladder}}$, where $R_{ladder} = 1k\,\Omega$ forms the equivalent ladder resistance between two consecutive reference levels. These voltages are therefore generated in a method similar to the CML voltage levels by producing a drop of 0.75 V across the feedback resistor and fixing the output common mode to 0.9 V (through the opamp's CMFB). This is shown in Fig. 6.9.

The circuit that generates the bias voltages for generating I_{ref} is shown in Fig. 6.10. To generate I_{ref}, external reference voltage V_{ref_flash} is fixed across $6R_1$. The current I_{ref} so obtained equals $\dfrac{V_{dd} - V_{ref\_flash}}{6R_1}$.

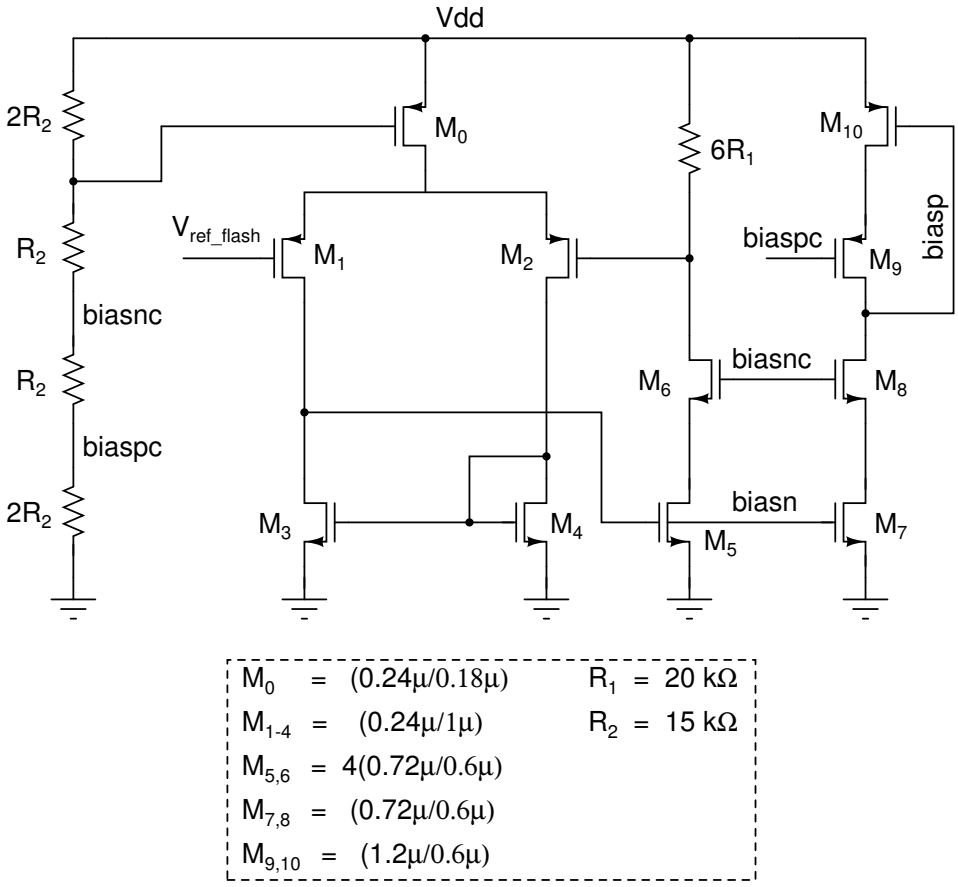


Figure 6.10: Biasing circuit for Fig. 6.9.

6.8 Effect of offset in the flash ADC

Many flash converters used in $\Delta\Sigma$ modulators use offset-cancelled preamplifiers [31] or calibration [11] to reduce the latch offset. This strategy increases area and power dissipation. In this work, we eliminated the pre-amplifier by using a large LSB size. The predominant nonideality in the flash converter is the deviation in quantizer thresholds from the ideal values due to device mismatch in the comparators. It is usually assumed that this is not a serious issue since nonidealities in the flash ADC are noise shaped by the loop. However, ADC threshold deviations increase the mean square error introduced by the quantizer, so it should be expected that the performance of the modulator will be degraded by comparator offsets. To study this effect, the modulator was simulated for various levels of Gaussian distributed offsets in the comparators. One thousand trials for each level of offset were run. Fig. 6.11 shows the results. The lines represent the mean, the

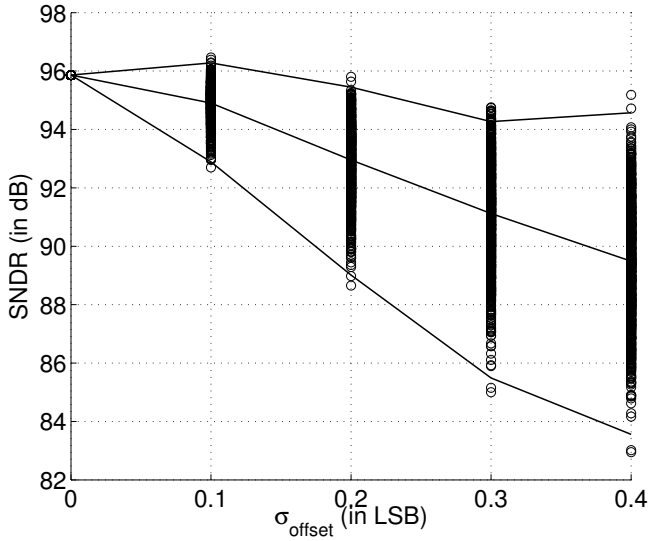


Figure 6.11: Effect of comparator random offset on in-band SNDR–for each level of offset, 1000 trials were simulated. The lines show the modulators with the best 1% SNDR, mean SNDR, and the worst 1% SNDR, respectively.

best, and the worst 1% of the SNDRs. It is thus seen that, to achieve a 13 bit performance from the modulator, random offsets in the comparator with a standard deviation of up to 0.35 LSB can easily be tolerated, as long as the characteristic of the quantizer is monotonic. The estimated 3σ random offset of the comparator is about 18 mV which is about 0.1 LSB and hence not an issue.

CHAPTER 7

4-bit calibrated DAC

7.1 Architecture

7.1.1 One-sided switching vs complementary switching

Current steering architecture is used to implement the DAC. The most common current steering DAC is using an nMOS current steering switch and pMOS common mode current sources, as shown in Fig. 7.1.

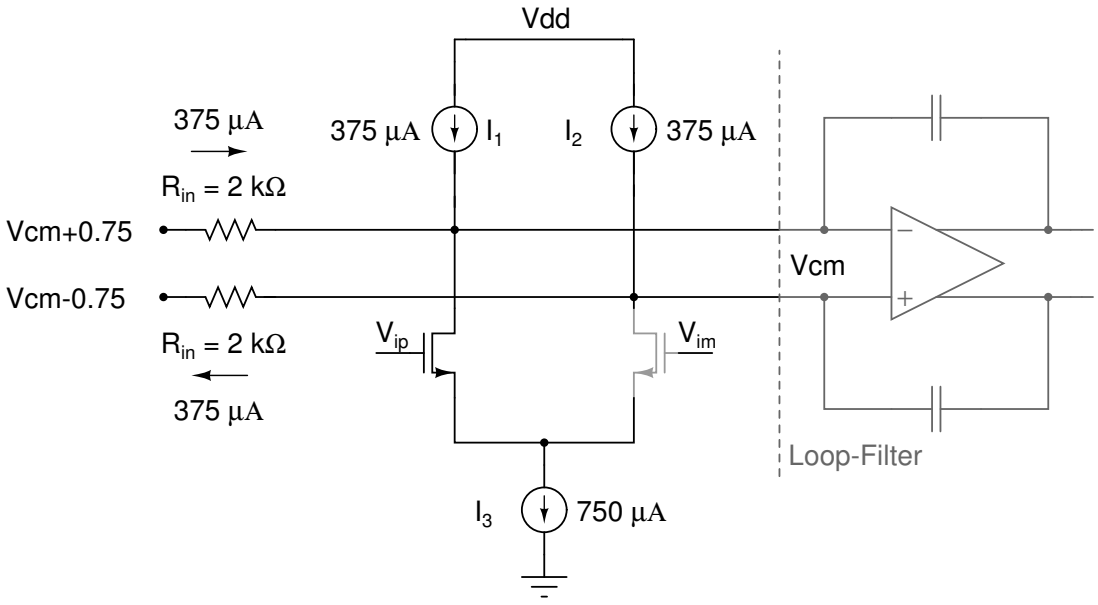


Figure 7.1: Circuit diagram of the NMOS current steering DAC feeding to the loop filter input. A single current steering switch carrying the total DAC current is shown for simplicity.

Here, the noise current I_{n_nmos} at the input of the first integrator, due to the DAC is :

$$I_{n\_nmos} = I_{n1} - I_{n2} - (-I_{n3}) \tag{7.1}$$

Where I_{ni} is the noise current corresponding to the current source I_i.

Also the input referred noise power spectral density (PSD) S_{n_nmos} is :

$$S_{n\_nmos} = R_{in}^2(S_{n1} + S_{n2} + S_{n3}) \tag{7.2}$$

or,

$$S_{n\_nmos} = 4.R_{in}^2.S_{n1,375uA} \tag{7.3}$$

Where S_{ni} is the noise current spectral density corresponding to the current source I_i[1].

Eq. 7.6 shows that the total noise PSD is 4 times that of the noise PSD due to the current source I_1. To reduce the input noise power, current steering DAC with complementary architecture is used as shown in Fig. 7.2.

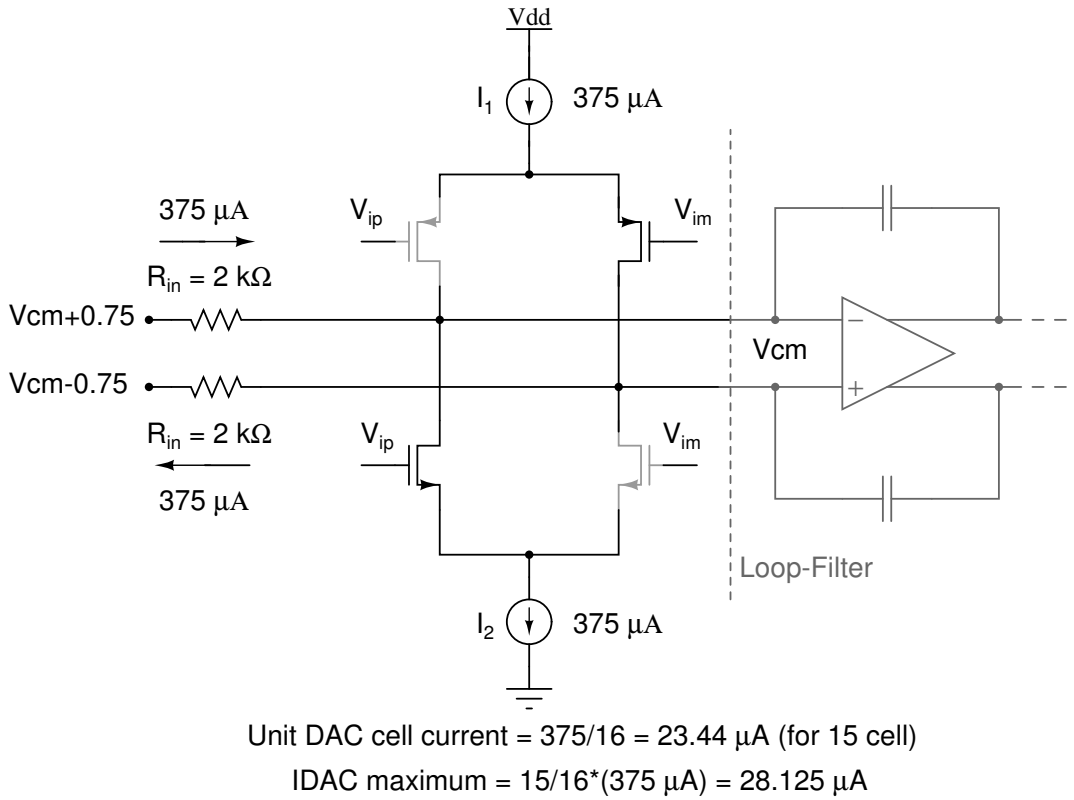


Figure 7.2: Circuit diagram of complementary current steering DAC feeding to loop filter input.

[1]It is assumed that I_1,I_2, and I_3 operate with the same overdrive voltage. Therefore, $g_{m3} = 2g_{m1,2}$ and $S_{n3} = 2S_{n1,2}$

Here, the noise current I_{n_comp} at the input of the first integrator, due to the DAC is :

$$I_{n\_comp} = I_{n1} - I_{n2} \tag{7.4}$$

and input referred noise power spectral density (PSD) S_{n_comp} is :

$$S_{n\_comp} = R_{in}^2(S_{n1} + S_{n2}) \tag{7.5}$$

or,

$$S_{n\_comp} = 2.R_{in}^2.S_{n1,375uA} \tag{7.6}$$

Eq. 7.6 shows that the total noise PSD is 2 times that of the noise PSD due to the current source I_1.

So, on comparing the two architectures, complementary switching has the following advantages over one-sided switching.

- Half the current consumption.
- 3 dB lesser noise.

This comes at a price of more complicated control layout.

7.1.2 Unit DAC cell

In this work, we choose the complementary architecture for the DAC due to the above advantages. The schematic of the DAC cell with clocking and the latch (to hold the input for one clock cycle), is shown in Fig 7.3. M_{n1} along with M_{n2} as cascode form the nMOS current source. Similarly, M_{p1} along with M_{p2} as cascode form the pMOS current source. $M_{n2,3}$ and $M_{p2,3}$ are the nMOS and pMOS switches respectively to steer current in one of the two paths. For simplicity, the DAC switches are operated using full rail signal swing. For this a *CML to*

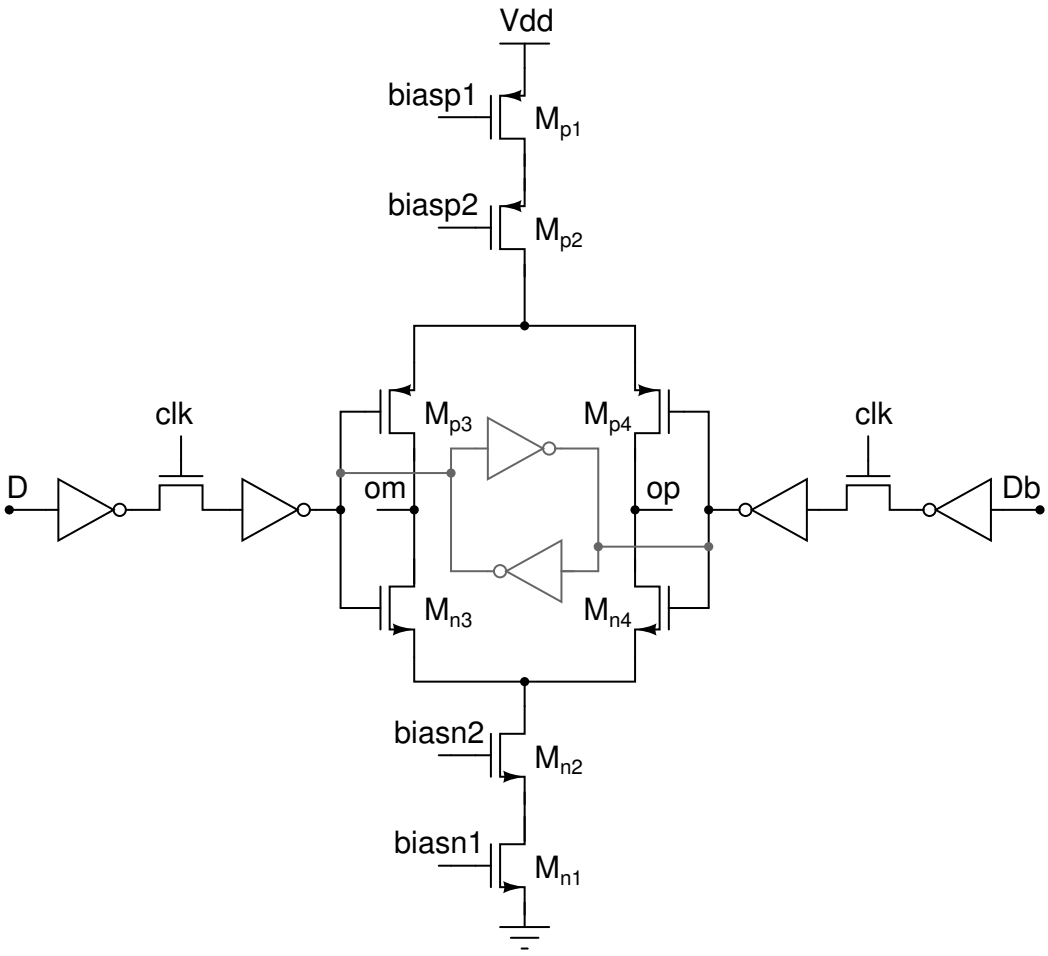


Figure 7.3: DAC unit-cell with drive circuitry.

CMOS converter is used, to convert CML logic of the flash ADC output to CMOS logic (D and Db complementary signals in Fig 7.3). *CML to CMOS converter* is implemented as an nMOS source follower cascaded with an inverter.

7.2 Methods to reduce the effect of mismatch in the DAC cells

In Chapter 2, we had seen the effect of mismatch in DAC cells on the performance of the CTDSM. There are many methods to reduce the DAC nonlinearity. Following are the most commonly used methods.

7.2.1 Dynamic Element Matching (DEM)

Using DEM, the bits in the thermometer code output, of the quantizer are rearranged following certain rules by digital processing before they are applied to the DAC. The rearrangement does not affect the data value, but it changes the usage of the unit elements of the DAC, which can result in two effects. *First*, the DAC error becomes uncorrelated to the DAC input, eliminating the signal dependent tones that will appear at the modulator output otherwise. *Second*, the so called mismatch shaping will move the error power from lower frequencies to higher frequencies. There are many choices for the DEM. Data weighted averaging (DWA) which provides first order shaping using a simple element rotator algorithm is a very commonly used technique.

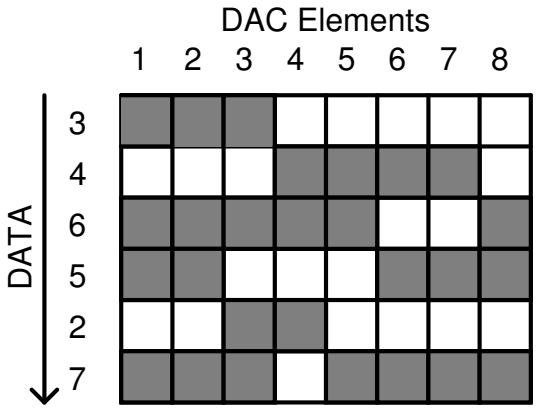


Figure 7.4: Illustration of DWA.

DWA is illustrated in an 8 level DAC shown in Fig. 7.4. The grey cells represent the currently used DAC cells while the white cells indicate those not used. The number of elements used to generate the new output is equal to the current input data value, and elements are selected in a circular way such that each element has equal probability of usage. Hence, mismatch between the unit elements are quickly averaged out and DAC error is first order shaped [18].

However the effect of mismatch shaping depends on the OSR. In wideband applications, where OSR is as low as 8, the error shaping from the DWA is too weak to

satisfy high resolution requirements. As for the CT modulator, the delay caused by the DEM logic will increase the ELD and hence affect the performance and stability of the modulators. ELD is quite significant for wideband high resolution converters as explained in Chapter 3. As reported in [7] this delay was 700 ps, which is 0.21 times sampling period in our case.

7.2.2 DAC calibration

Another method to tackle the DAC mismatch errors is self calibration [8]. The basic idea of this technique is to use a reference current as a standard to trim each current source. The calibration is done circularly so that calibration is continuous. The principle of calibrating a current source is shown in Fig. 7.5. During the calibration phase, switch S2 is on and switch S1 connects the reference current

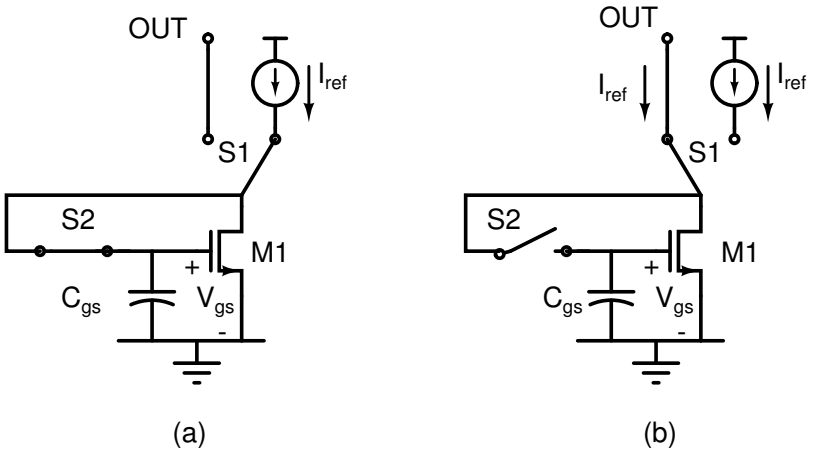


Figure 7.5: Current calibration principle during (a) Calibration. (b) Operation.[8]

source to the transistor M_1. The drain current of M_1 is I_{ref} and its V_{gs} settles to the appropriate value that results in a drain current I_{ref}. During the operation phase, S2 is off and S1 connects the drain of M_1 to the output node. Since the V_{gs} is held on the C_{gs} of M_1, the output current from M_1 will still be I_{ref}.

To be suitable for multibit current steering DAC, the calibration idea must be extended to the array of current sources as shown in Fig. 7.6. Here, $N+1$ current sources are used to generate N equal output currents. An extra current source

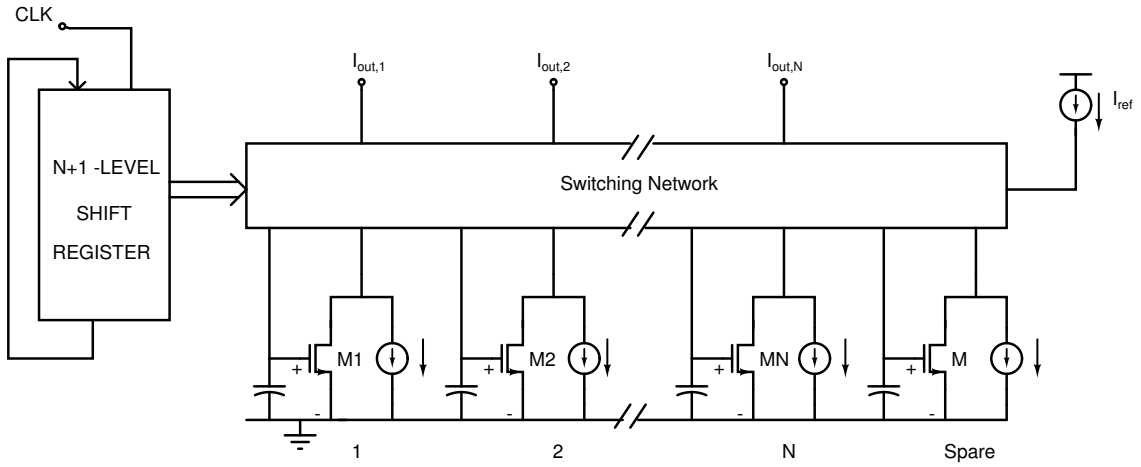


Figure 7.6: Block diagram of N element current steering DAC with Calibration.

takes the place of the current source being calibrated to ensure continuity of the DAC output. The $N + 1$ level digital shifter generates 1-of-n code to select the cell to be calibrated. All the cells are calibrated in sequence and the cycle repeats. The switching network connects the cell being calibrated to the reference current source and the other N cells to the corresponding input and output terminals.

Nonidealities such as charge injection, clock feedthrough and switch mismatch lead to nonlinear errors. [8] describes several design techniques to mitigate these nonidealities and achieve 16 bits linearity.

7.3 Modified calibration scheme

The drawback of the above circuit is that it has switches in the signal path, i.e. between the output of the flash ADC and the input of the feedback DAC. At high speeds, delay through these switches is a large fraction of clock period and significantly increase ELD. In this work, above problem is overcome by connecting two DAC cells to the output of each flash comparator. Out of these two DAC cells only one is going to contribute to the output at any instant. This logic can be implemented without switches in the signal path. So this technique reduces the ELD in the $\Delta\Sigma$ loop at the expense of having $2N$ current cells instead of N.

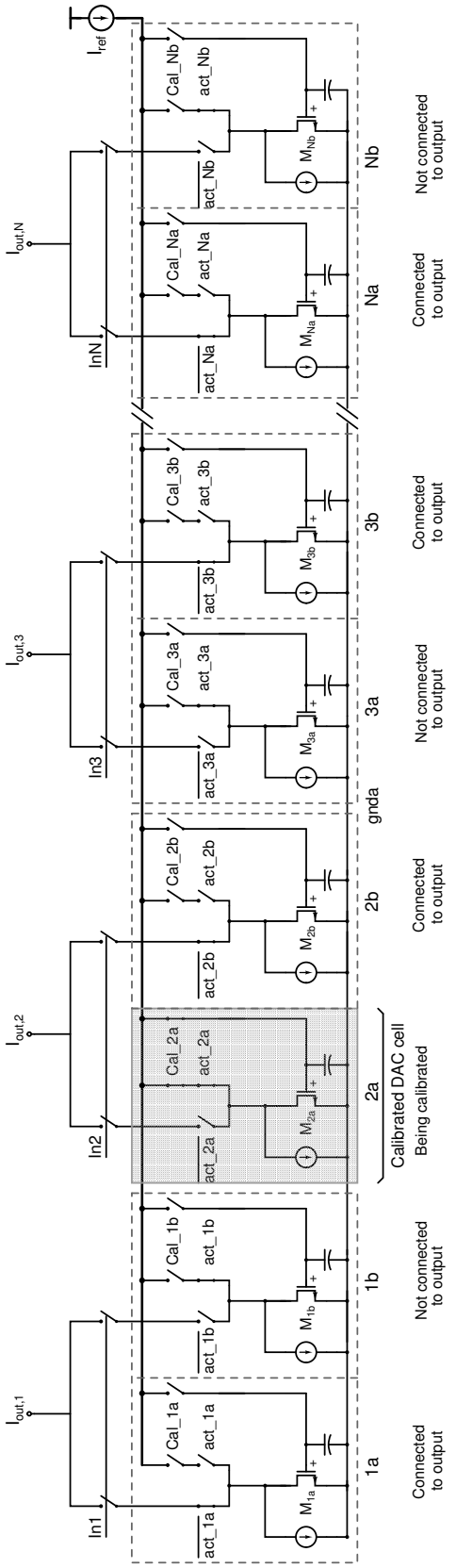


Figure 7.7: Block diagram of N level current steering DAC with 2N current source.

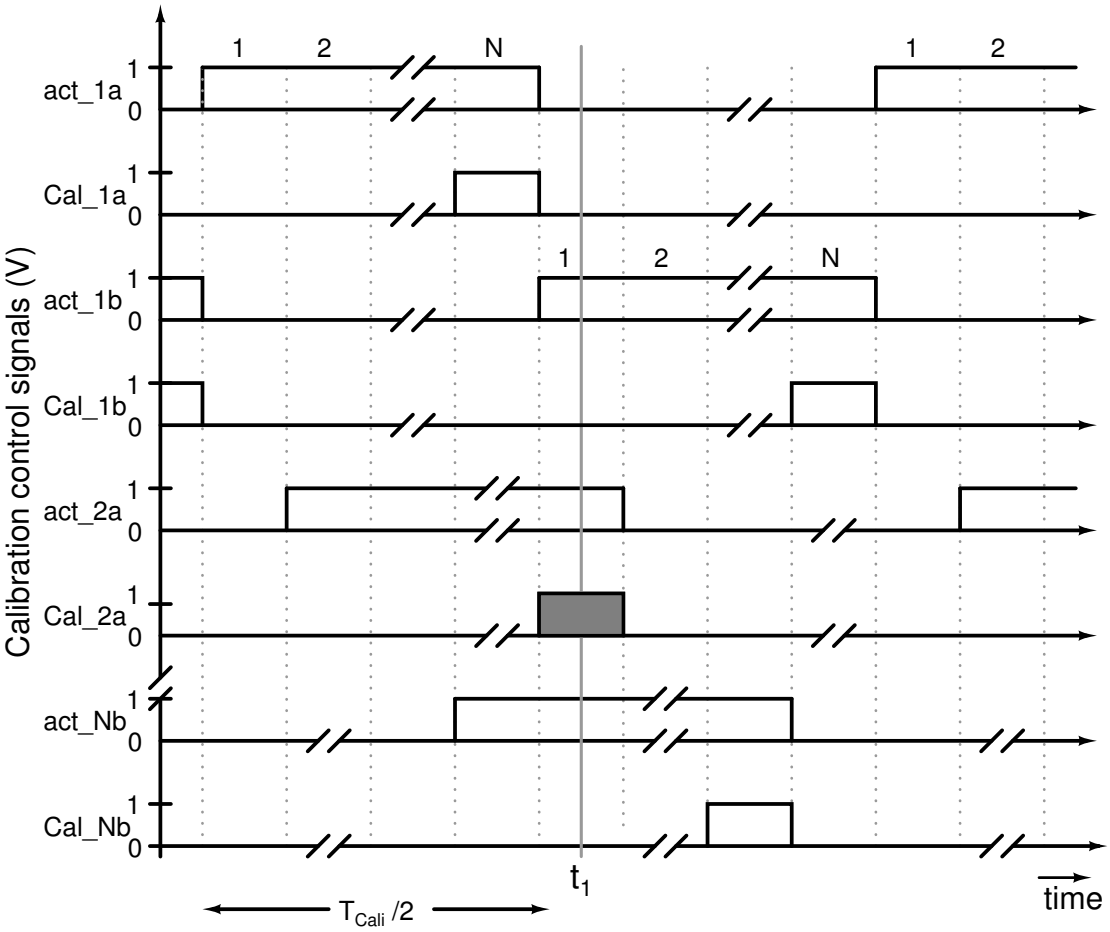


Figure 7.8: Logical waveforms of control signals for the calibration.

At any given time N cells contribute to the output and the remaining N cells are calibrated in a cyclic manner. The system level schematic[2] of the DAC with the calibration logic is shown in Fig. 7.7. The position of the switches is shown at time t_1 (marked in Fig.7.8). Here out of act_1a and act_1b, one will be on and the other will be off as shown in Fig.7.8. act_ia, b signals control the selection one DAC cell out of the two DAC cells. So at any time instant, N DAC cells will be on and contributing to output current and the remaining N current cells will be off. Reference current Iref shown in Fig. 7.7, will calibrate one of N DAC cells that are off. After calibration it becomes active (act_ia become high) and the other DAC cell of that pair turns off. The selection of DAC cell for calibration out of N cells is done by Cal signal (Fig.7.8) which is on for $T_{cal}/2N$. where T_{cal} is the

[2]This schematic is shown only to illustrate the calibration scheme. The actual current steering DAC cell will be shown in next section.

calibration time period.

7.4 DAC with calibration loop

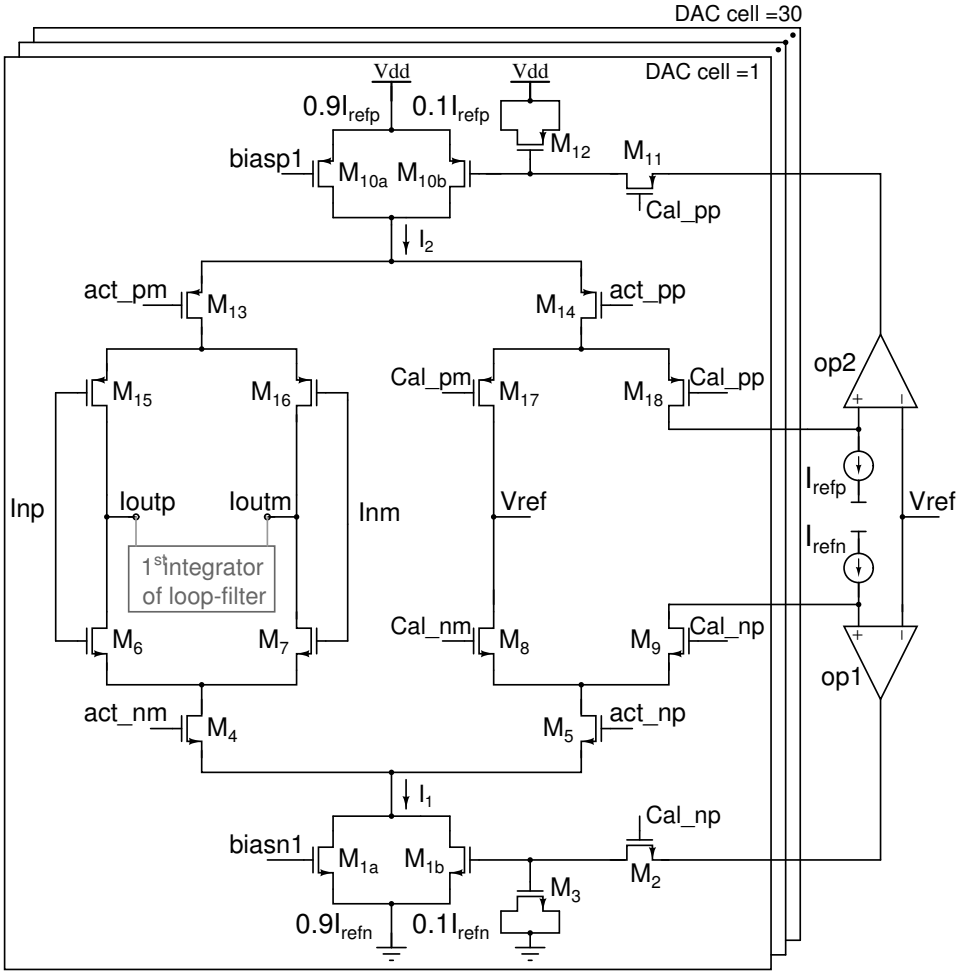
Circuit level schematic of the DAC cell with calibration is shown in Fig.7.9. For the 16 levels DAC used in this work, $N = 15$, and we need 30 DAC cells to implement the scheme in Fig. 7.7. Two current sources I_{refn} and I_{refp}, derived from a single master source, are used to calibrate nMOS (M_{1b}) and pMOS (M_{10b}) DAC cell respectively. Here, $M_{2,1b,5,9}$ and op1, and $M_{11,10b,14,18}$ and op2 form calibration loop for nMOS and pMOS respectively. At the end of the calibration of a DAC cell, $I_1 = I_{refn}$ and $I_2 = I_{refp}$ and DAC cell switches from calibration mode to the operational mode (act_nm, act_pm ON) and gets connected to the DAC output. In practice, the calibration circuit suffers mainly because of two issues, *charge injection* (due to switches $M_{2,11}$) and *leakage current* through reverse biased diode of $M_{2,11}$ (between their drain and the substrate). To remove these effects, following methods are used:

- Adding capacitance (MOS capacitance $M_{3,12}$ in Fig.7.9) to $M_{1b,10b}$ respectively [8].
- Current sources of DAC cells ($M_{n1,p1}$ in 7.3) are divided into two current sources of value $0.9I_{ref}$ ($M_{1a,10a}$) and $0.1I_{ref}$ ($M_{1b,10b}$). This reduces the affects of charge injection as explained in [8]. The current division is done on the basis of maximum deviation in current from its ideal value (I_{ref}), that we can expect due to mismatch in current cells.

7.5 Biasing

7.5.1 Generation of biasn1 and biasp1 in Fig. 7.9

Fig. 7.10 shows the circuit diagram for generating biasn1 and biasp1, which are used to bias M_{1a} and M_{10a} respectively in Fig. 7.9. This MOS acts as a current



M1a,b	=2(1.2u/4u)	M6,7,8,9	= (0.5/0.18)	M12	=(4.5u/4u)
M2	= (0.48u/0.18u)	M10a	=5(2.5u/2.5u)	M13,14	= (6u/0.18u)
M3	=2(4.3u/3u)	M10b	=3(2.5u/2.5u)	M15,16,17,18	= 3(0.5u/0.18u)
M4,5	= (2u/0.18u)	M11	= (1.2u/0.18u)		

Figure 7.9: Circuit diagram of the calibrated DAC. N=15.

source carrying 0.9 times unit DAC current. Large capacitors are used to filter out the noise contribution from this biasing circuit. V_{ref_dac} is the off chip control signal that can be used to adjust the DAC current (and hence the quantizer gain) for experimentation. biasn2 and biasp2 are generated using a resistor string. This resistor string also generate logic level voltages required by signals act_nm, act_np, act_pm, act_pp in Fig. 7.9.

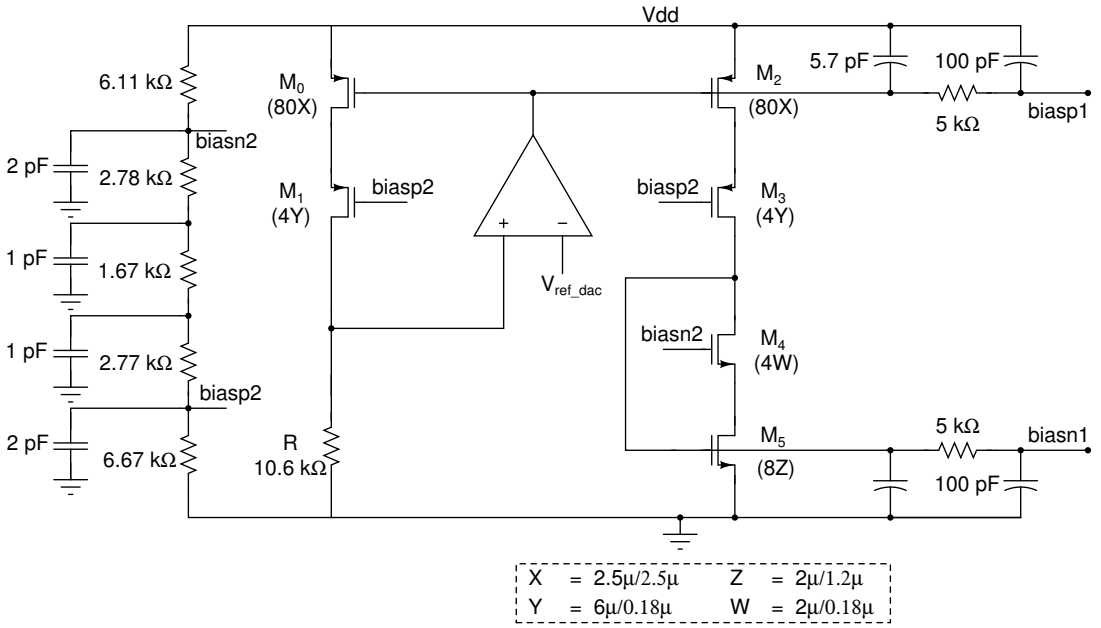


Figure 7.10: Bias circuit for generating biasn1 and biasp1 in Fig. 7.9.

7.5.2 Generation of reference currents for calibration

Fig. 7.11 shows the biasing circuit to generate reference currents I_{refn} and I_{refp} to calibrate the nMOS and pMOS current sources respectively. This current is generated using $1/R$ biasing.

$$I_{refn} = I_{refp} = \frac{V_{ref\_dac}}{5(R_1 + R_2)} = \frac{0.9}{5(7.67\,k\,\Omega)} = 23.46\,\mu A \tag{7.7}$$

The circuit is stabilized using miller compensation.

The modulator was simulated with the above calibration technique in the DAC. The mismatch standard deviation of each element is $\sigma_{\Delta I/I} = 0.01$. Fig. 7.12 shows the PSD of the modulator output, for with and without calibration. The obtained inband SNDR was 89 dB and inband SFDR was 101 dB with calibration, and inband SNDR was 74 dB and inband SFDR was 84 dB without calibration.

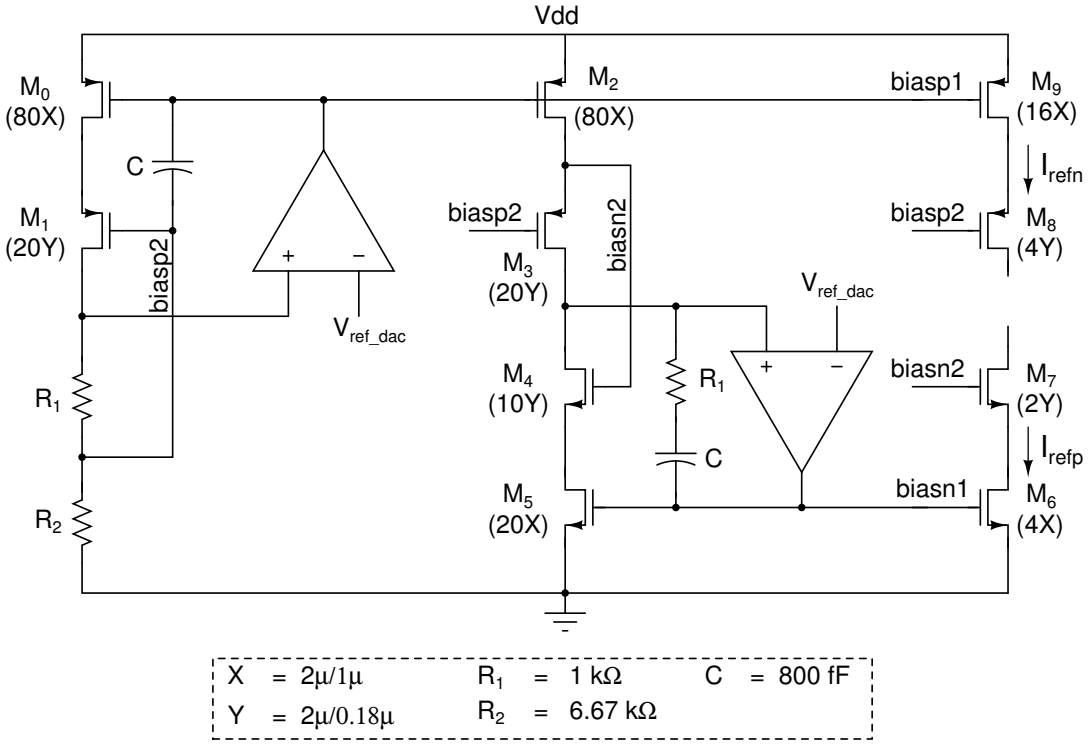


Figure 7.11: Bias circuit for generating I_{refp} and I_{refn} in Fig. 7.9.

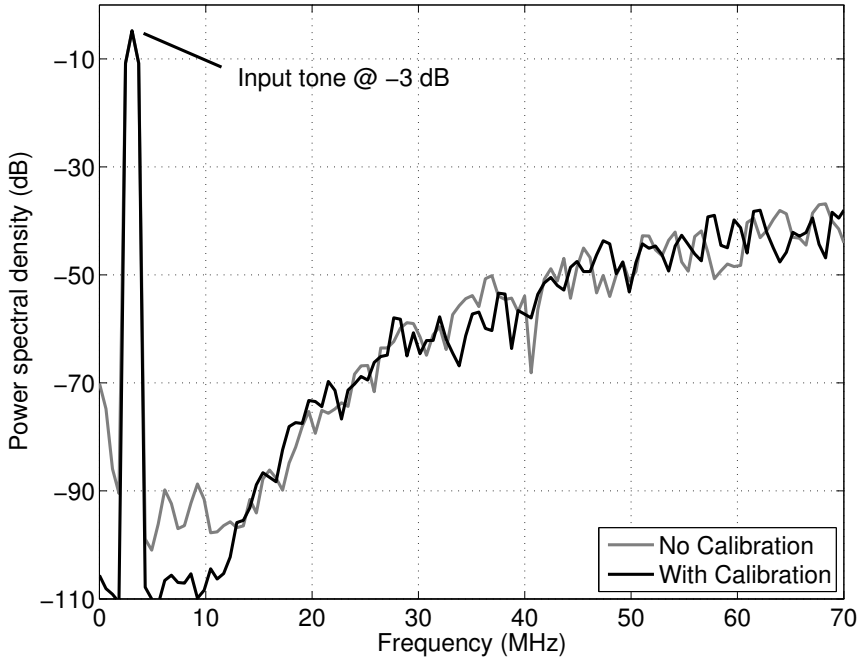


Figure 7.12: Output PSD of CTDSM with and without calibration ($\sigma_{\Delta I/I} = 0.01$).

CHAPTER 8

Design summary and simulation results

8.1 Architecture of the Modulator

Fig 8.1 shows the top level architecture of the modulator implemented in this work.

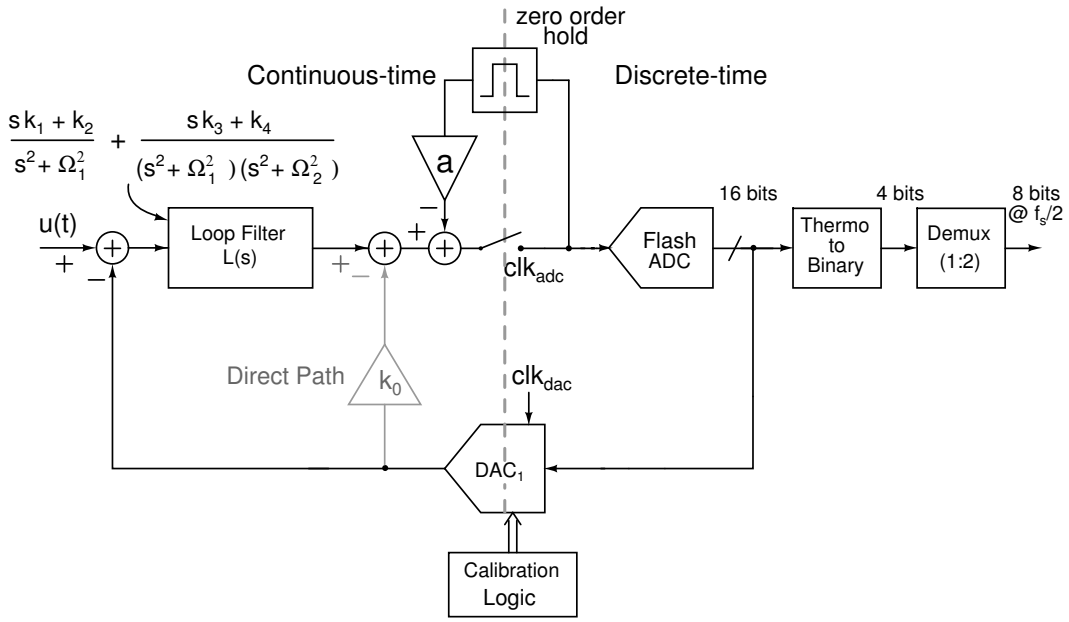


Figure 8.1: Block diagram of the designed CTDSM.

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8.2 Floorplan of the modulator

The floorplan of the layout of the modulator is shown in Fig. 8.2. Here, all the blocks discussed in previous chapters are placed in a optimal way to reduce the parasitic capacitance in the high speed paths. Empty area is filled up with supply bypass capacitors.

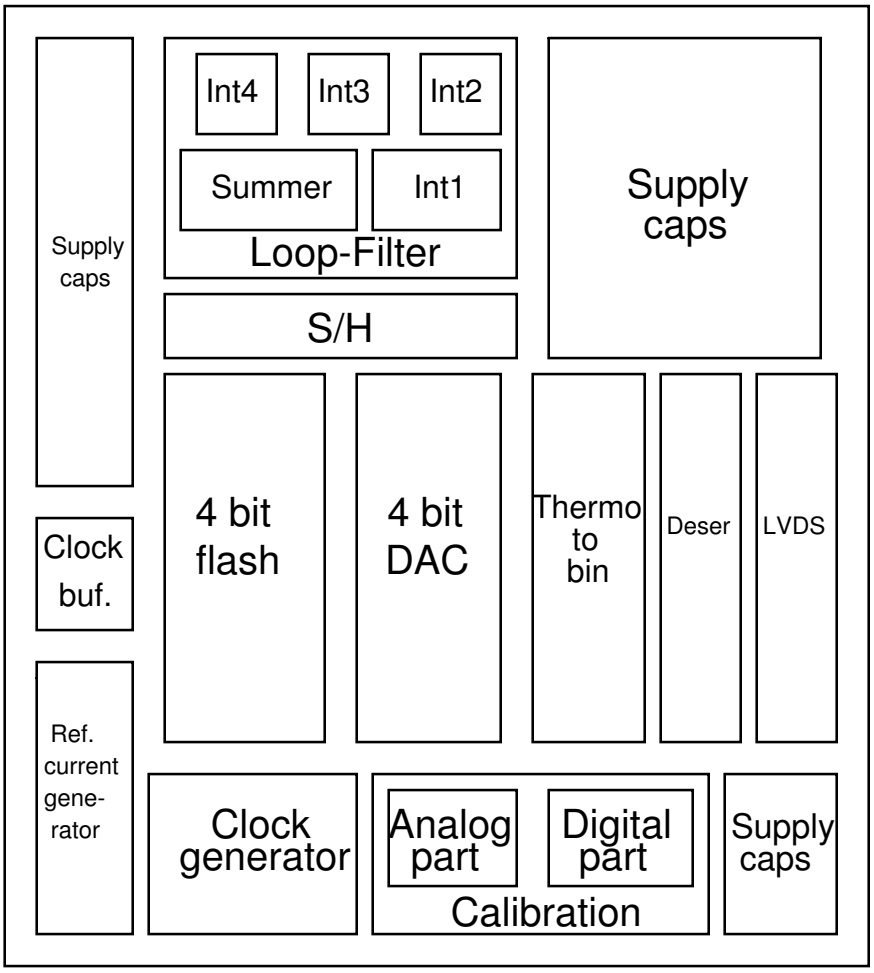

Figure 8.2: Floorplan of the designed CTDSM.

The flash and DAC are laid out as arrays with equal pitch. This minimizes the interconnect parasitics. Summing opamp of the loop-filter is placed close to flash ADC and first opamp1 is placed close to DAC to reduce the routing capacitances in the closed loop of the modulator. The remaining three integrators are placed at the corner (Fig. 8.2). S/H is placed between the summing opamp and the flash ADC to reduce parasitics in fast loop of the modulator. Input signal and input sampling clock are provided pads on different sides of the chip, so as to reduce the coupling between them. The two pads on either side of input signal pads are grounded to reduce the coupling from adjacent pads. The snapshot of the layout of the chip is shown in Fig. 8.3.

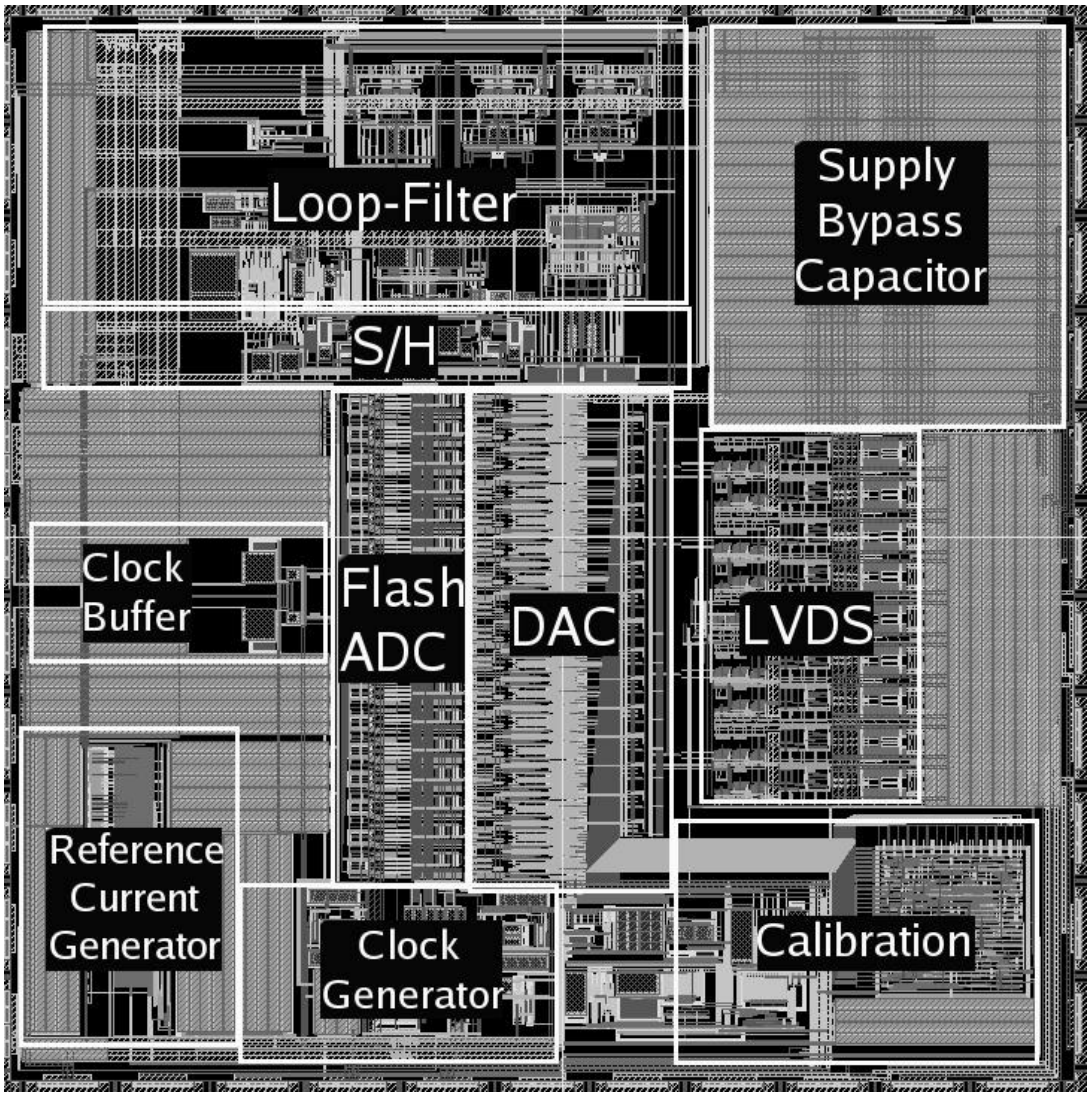

Figure 8.3: Snapshot of the layout of the designed CTDSM.

8.3 Circuit level simulation results

8.3.1 CTDSM loop with VerilogA model for each block

Simulations of the entire modulator was first carried out at verilog model level. Fig. 8.4 show the PSD at the output of the modulator. Obtained SNR at an input equal to MSA is 98 dB. MSA is 0.75 times quantizer range.

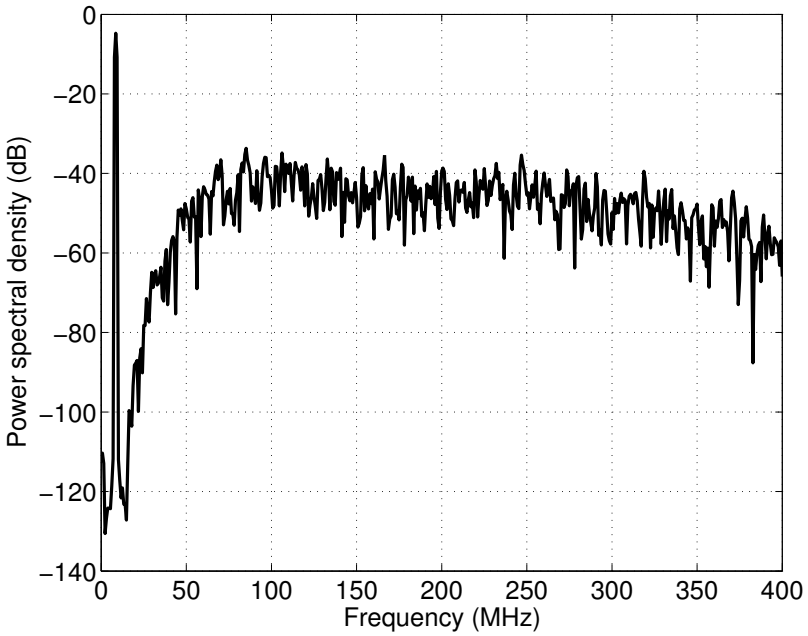

Figure 8.4: PSD of the modulator: VerilogA model

8.3.2 Transistor level simulation at the schematic level

Fig. 8.6 show the PSD at the output of the modulator with each verilog block replaced by its transistor level schematic (0.18 μm UMC CMOS models are used). Obtained SNR is at an input equal to MSA 93 dB. There was 3 dB variation in this SNR across various process corners.

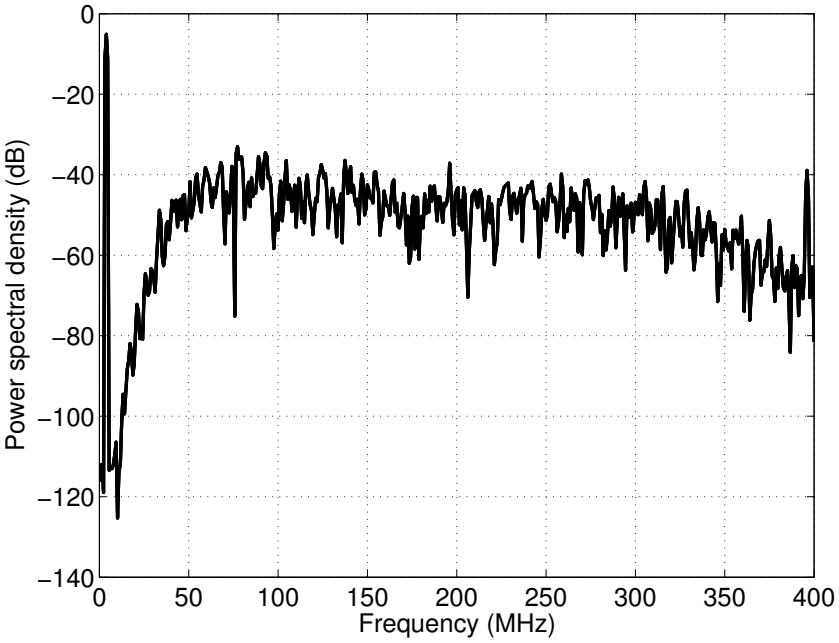

Figure 8.5: PSD of the modulator: Transistor level circuit.

8.3.3 Transistor level simulation with extracted view after layout

Fig. 8.6 shows the PSD at the output of the modulator with the extracted view including all the layout parasitics. Supply bypass capacitors are also included in this extracted view. Supply is provided to the modulator using an ideal voltage source connected in series with an inductor. This inductor is used to model bond wire inductance present in chip. Obtained SNR at an input equal to MSA is 88.5 dB. There was 2 dB variation in this SNR across various process corners.

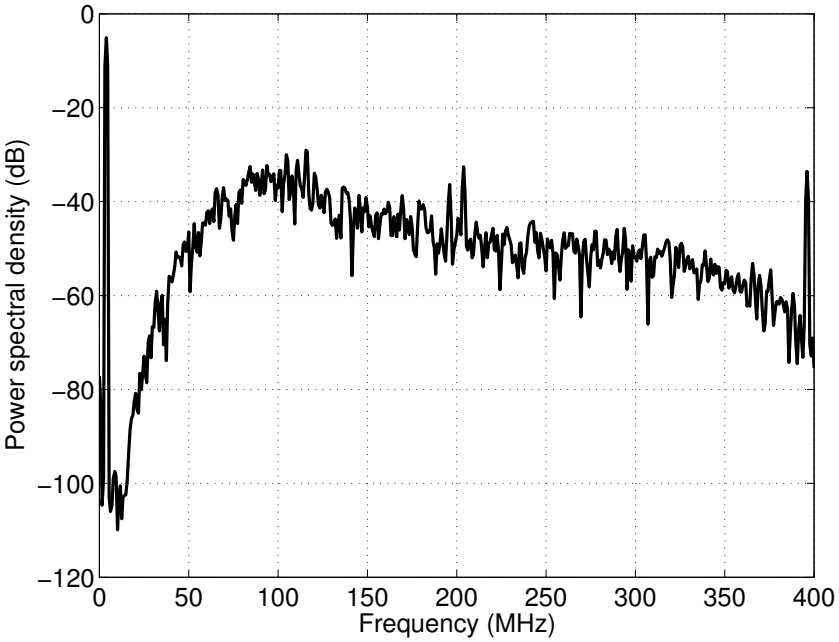

Figure 8.6: PSD of the modulator: Extracted view with layout parasitics.

8.3.4 Summary of the simulation results

Table 8.1: Simulation Results.

View	Corners				SNDR (dB)	SFDR (dB)
	MOS	Resistor	Capacitor	Temp (C)		
VerilogA model	-	-	-	-	98	-
Transistor level	tt	typ	typ	27	92	101
	ss	max	max	75	93	103
	ff	min	min	0	91	100.3
Capacitance extracted level	tt	typ	typ	27	88.2	93
	ss	max	max	75	88.5	95
	ff	min	min	0	88	92.6

8.3.5 Power dissipation in different blocks of the modulator

Table 8.2: Power dissipation.

	Blocks used in the designed modulator		Power (Vdd=1.8 V) mW
1.	Loop-filter	First integrator	6.3
		Second, third and fourth integrator	1 (each)
		Summing amplifier	7.4
2.	Flash ADC with clock generator		15.2
3.	DAC with level shifter		8.6
4.	Fast loop (S/H and G_m cell)		2.4
5.	Clock buffer		2.6
	Total		45.5

8.4 Final result

The worse case quantization noise in transistor level simulations with capacitance extracted view was -88 dB. Modulator was designed for thermal noise of -84 dB. So total noise (thermal noise + quantization noise) is -82.5 dB. Table 8.3 shows the summary of the simulated performance.

Table 8.3: Summary of the ADC simulated performance

Specification	Value
Sampling Frequency	800 MHz
Input Bandwidth	16 MHz
Quantizer Range	$3\,V_{pp,diff}$
SQNR	88 dB
Inband Thermal Noise	84 dB
Peak SNR	82.5 dB
Power	46 mW (1.8 V)
Active Area	$1\,mm \times 1\,mm$
Total Area	$1.5\,mm \times 1.5\,mm$
Technology	$0.18\,\mu m$ UMC CMOS

8.4.1 Inferences

- Quantization noise was mainly limited by the dynamic nonlinearity of the feedback DAC. This is due to the signal dependent sampling of the virtual ground voltages of the opamp on the tail node of the DAC cells. To reduce this, opamp1 was scaled up by a factor of 2. This reduces the signal swing at the output of the DAC and hence reduces the nonlinearty. On doubling current through opamp1, the SNDR increased from 82 dB to 88 dB.

- Dynamic nonlinearities can also be reduced by reducing the swing of the signal controlling the DAC switches and maintaining the switches in saturation. But its hard to generate these reduced supplies.

- Thermal noise is mainly contributed by the feedback DAC, input resistor of opamp1, and opamp1 itself. Out of these, the feedback DAC was the main contributor to thermal noise.

- 4-bit digital bit stream is taken at half the sampling rate for the sake of measurement. So it is a 8-bit digital bit stream (at $f_s/2$) coming out of the modulator along with a corresponding reference clock at $f_s/2$.

CHAPTER 9

Testing

9.1 Test chip

A snapshot of the fabricated test chip is shown in Fig. 9.1. It is in a Quad Flat No leads (QFN) package with 48 pins and an area of 36.7 mm^2.

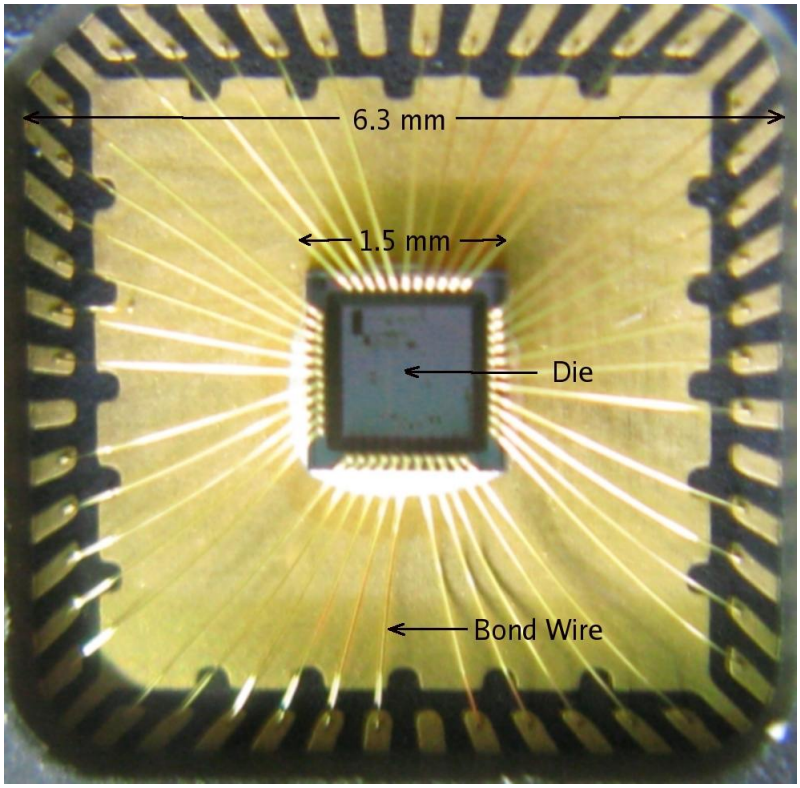

Figure 9.1: Test chip. (QFN 48 package)

Fig. 9.2 shows the pin details of the chip. Out of the 48 pins, 4 pins are not used and remaining 44 pins are allocated as shown in Table 9.1. Appendix B shows the description of each pin.

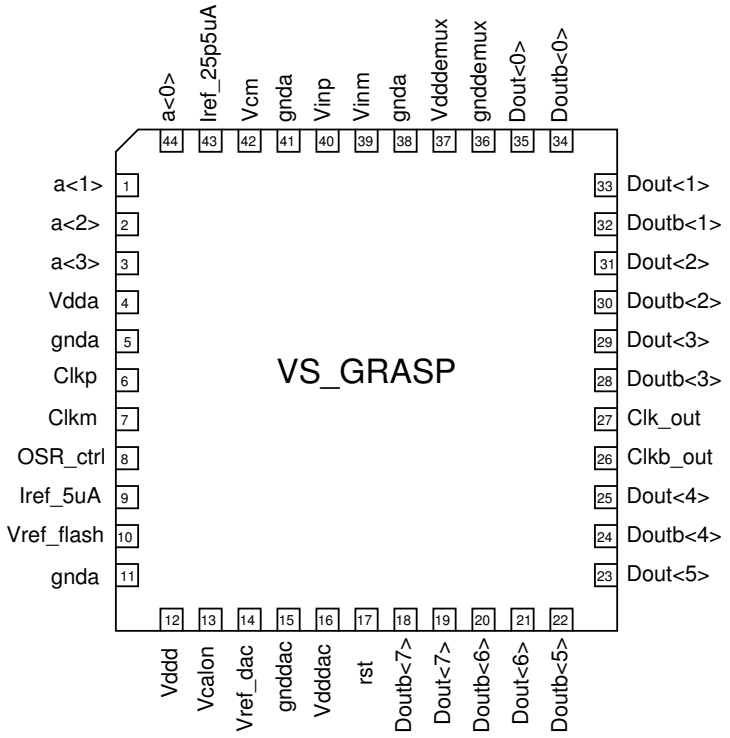

Figure 9.2: Pin details of the test chip.

Table 9.1: Pin allocation in the test chip.

Signal	Number of pins used
Input signal	2
Input clock	2
Output digital data	18
Power supplies	10
References	5
Control signals	7

9.2 Test setup

Fig. 9.3 shows the block diagram of the test setup used for the testing of the chip. Here, a signal source (Agilent 33250A) drives a 3.6 MHz tone into a passive band-pass filter (ICE-3.5M-4M), which suppresses the harmonics and the wideband noise of the signal source. An RF transformer (Mini-Circuits ADT1-1WT) converts this spectrally purified tone into a differential signal that serves as the input to the test chip. The clock signal is generated by a signal source (Agilent E4422B), which can generate low-jitter sine wave at 800 MHz. RF transformer (Mini-Circuits ADT1-

1WT) is used to convert this clock to differential clock, which is fed to the test chip. The 8 output digital bits at $f_s/2$ (400 MHz) are stored in a FIFO. This FIFO is implemented in an FPGA (Xilinx-Virtex-5). From the FPGA, the data is transfered to a logic analyzer (Agilent 1682-AD) at a lower rate. A FIFO is used between test chip and logic analyzer because the logic analyzer available to us can operate at a maximum speed of 200 MHz. So, the FPGA captures the data at a high speed and then transfers it at a lower speed to the logic analyzer. From the logic analyzer, deserialized data is transfered to a PC for post-processing.

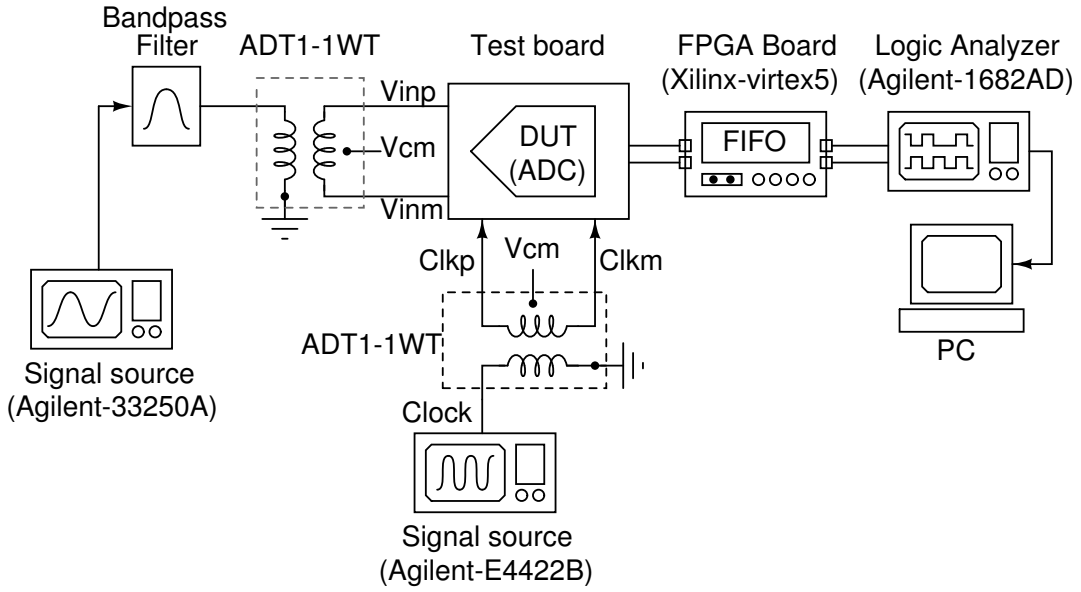

Figure 9.3: Test setup for evaluating the prototype modulator.

9.2.1 Test board

The printed circuit board to test the chip was designed in OrCAD. Schematics of the test board are shown in Appendix C. It is a two layer board measuring 3.4" × 3.7" and the material is FR4 glass epoxy. The thickness of the board is 0.8 mm. A snapshot of the testboard with all the components populated on it shown in Fig 9.4. Input single ended clock is converted to differential clock on-board using a center-tapped transformer. Input single-ended signal is converted to differential signal on a separate board and then fed to this board. The board has the provision

to provide either separate power supplies or a common power supply to the loop filter, DAC, flash ADC and deserializer used inside the chip.

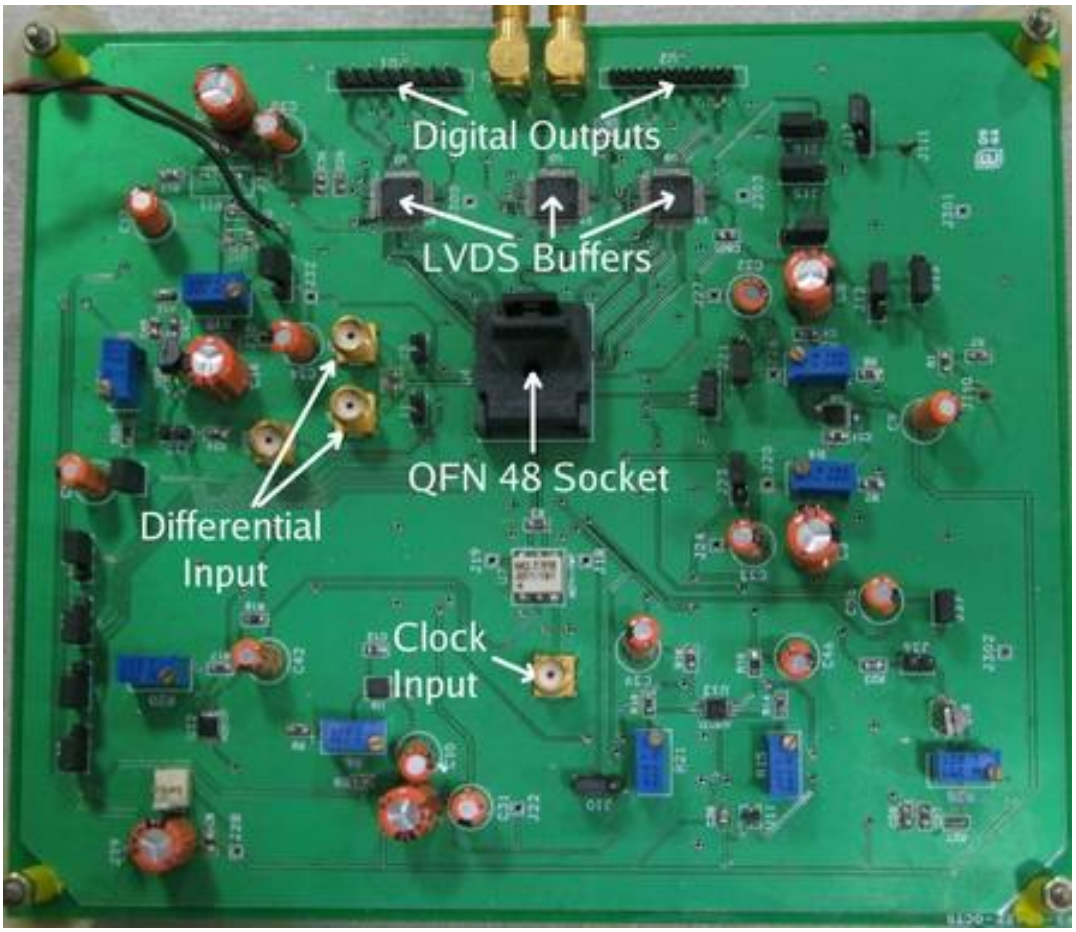

Figure 9.4: Test board. The test chip is inside the QFN 48 Socket.

The snapshot of the test setup is shown in Fig. 9.5.

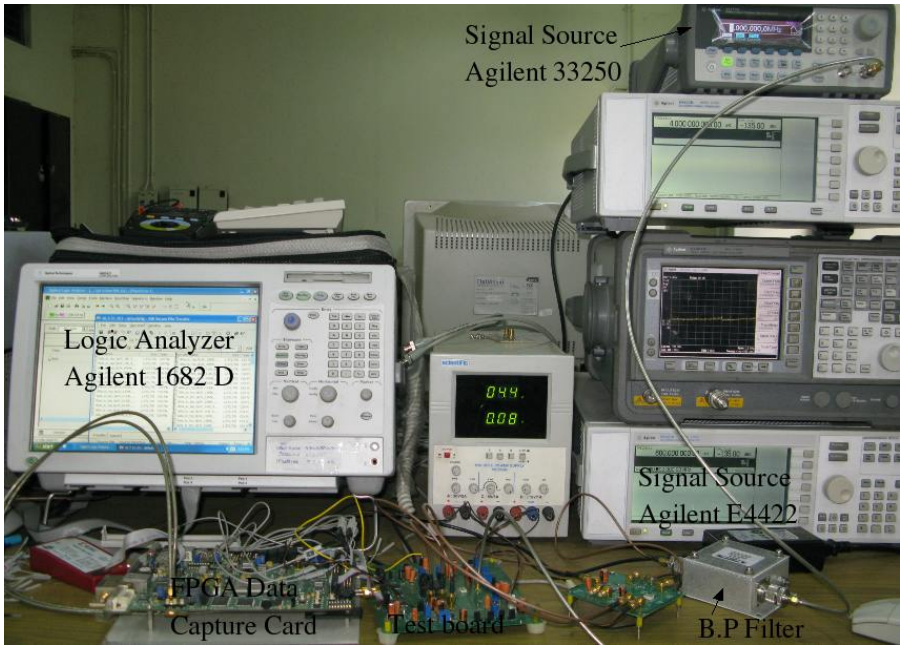

Figure 9.5: Measurement setup.

9.3 Measurement results

All the measurements are done at $f_s = 600\,MHz$ instead of 800 MHz, as the modulator was becoming unstable after 630 MHz. Fig. 9.6 shows the idle channel noise of the designed CTDSM. The inband idle channel noise is -80 dBFS with respect to quantizer full swing. The idle channel noise is higher because of low pMOS V_{th} (Appendix D). It has tones at $f_s/4$ due to the input reference substractor used in the flash, which is operating at $f_s/4$.

Fig 9.7 shows the measured SNR of the modulator. The peak SNR is 72 dB. Peak SNR is limited by the signal generator's SNR. The measured dynamic range of the modulator is 80 dB. Thanks to the 4 bit quantizer employed in the loop, the modulator is stable for signals as large as -1.6 dBFS. In this design the effect of clock jitter is completely dominated by the quantization noise and the circuit noise.

The inband spectrum when the modulator is excited by a 3.6 MHz tone at the maximum stable amplitude is shown in Fig. 9.8. It is seen that the harmonics

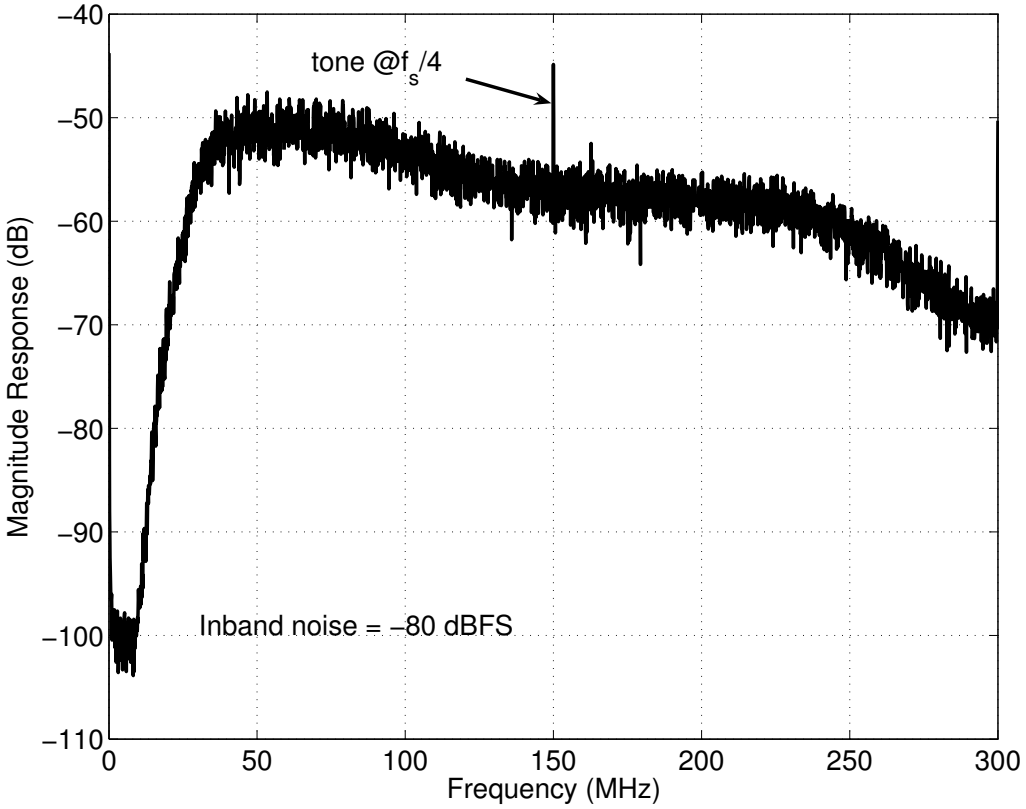

Figure 9.6: Idle channel noise of designed CTDSM.

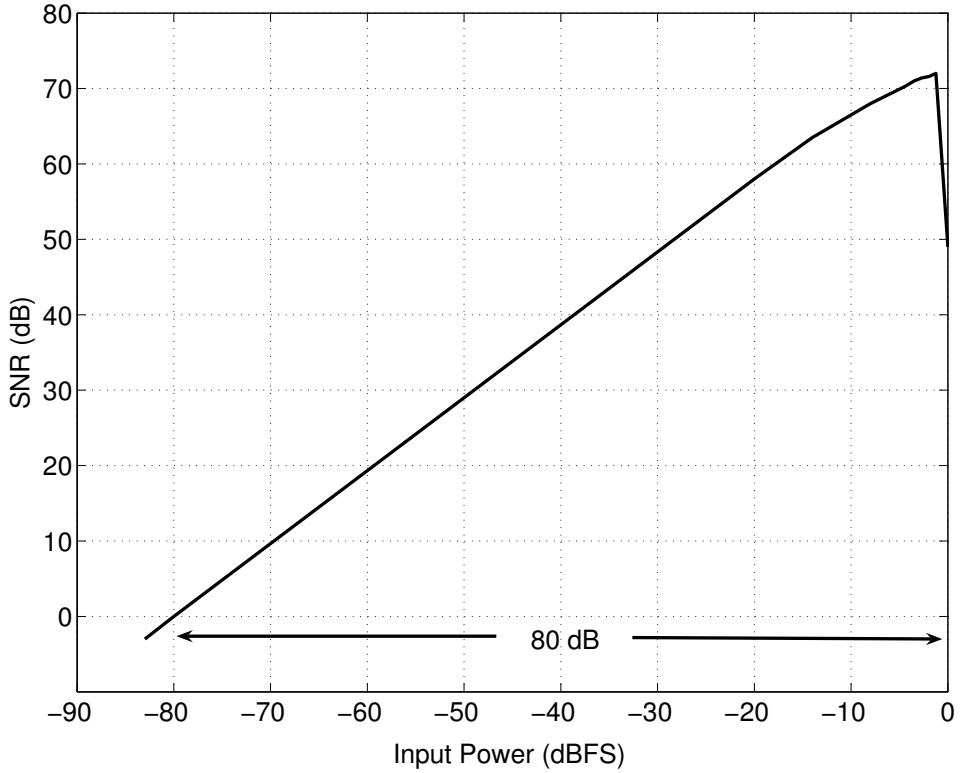

Figure 9.7: Measured SNR–the dynamic range is 80 dB.

are about 73 dB below the fundamental, and no nonharmonics tones are observed above the noise floor. Fig. 9.9 shows the complete spectrum.

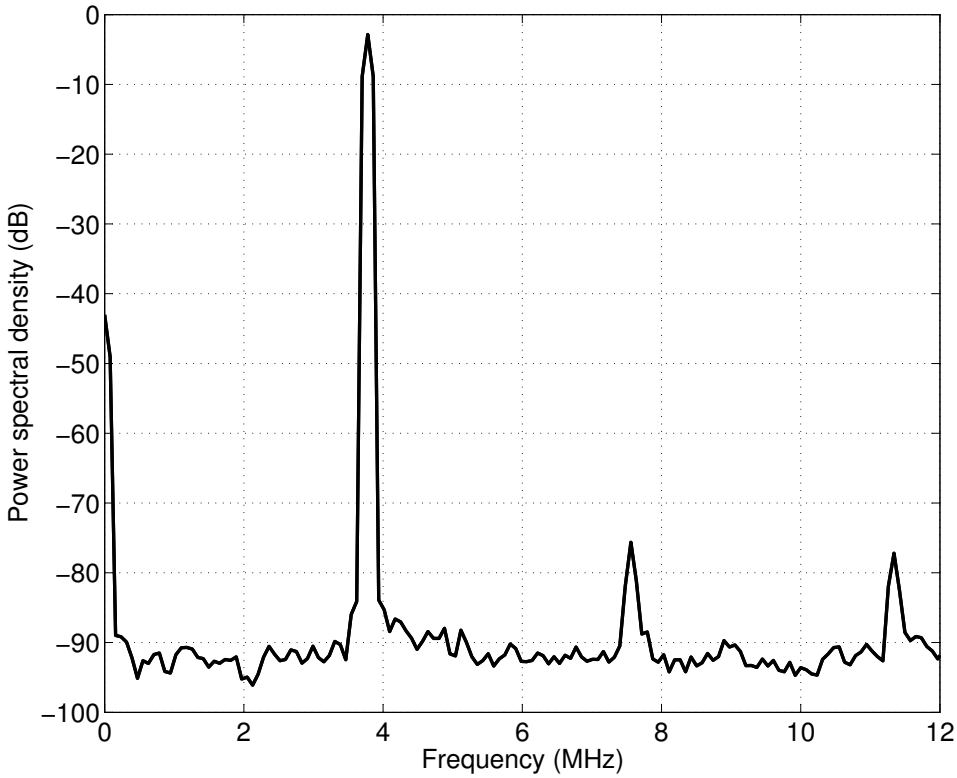

Figure 9.8: In-band spectrum for a 3.6 MHz input. The amplitude is that which results in the maximum SNR.

Fig. 9.10 shows the rejection of signals near $f_s \pm f_b$, demonstrating the inherent anti-aliasing property of continuous time $\Delta\Sigma$ modulator. In this test setup, a full swing signal ($1.25\,V_{p,diff}$) is applied at the input of the CTDSM and the frequency is swept from $f_s - f_b$ to $f_s + f_b$. There is more than 55 dB of anti-alias filtering for the signal in the band from 589 MHz to 611 MHz.

Summary of measured performance is given in Table 9.2. The figure of merit of the converter is determined as [32].

$$FOM_{DR} = \frac{P}{2 \times BW \times 2^{(DR-1.76)/6.02}} \tag{9.1}$$

where P, BW and DR denote the power dissipation, signal bandwidth and dynamic range (in dB) respectively. Our converter achieves 0.25 pJ/level, making it the most power efficient wideband modulator in $0.18\mu m$ to be reported.

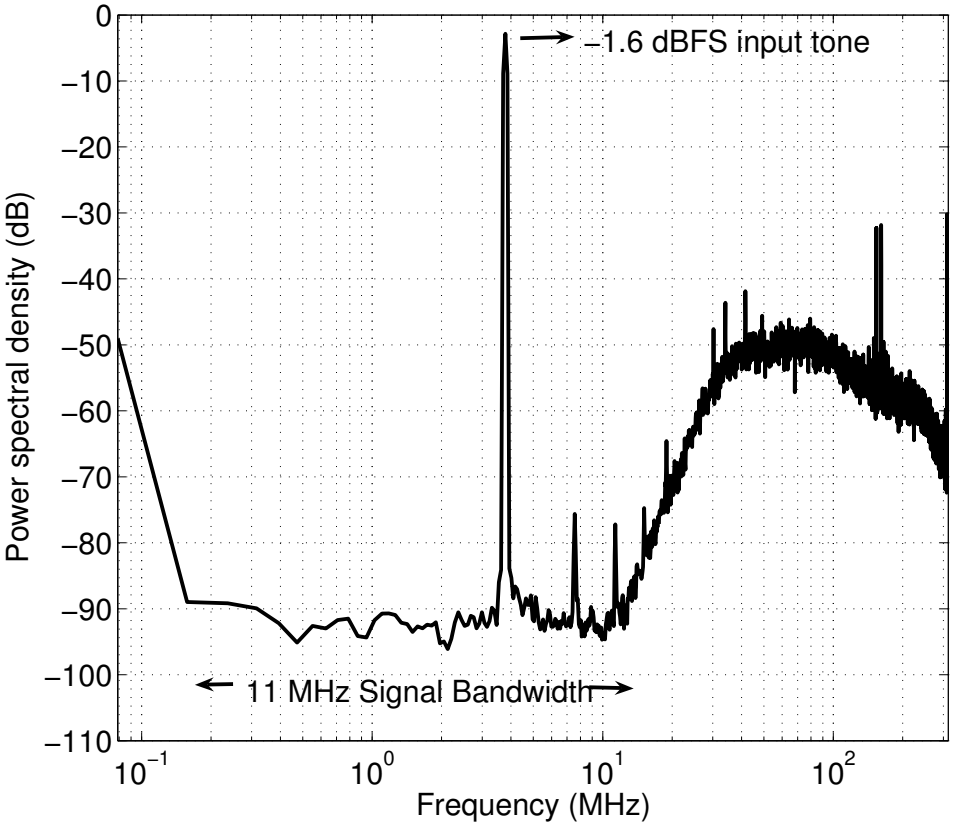

Figure 9.9: Complete spectrum for a 3.6 MHz input.

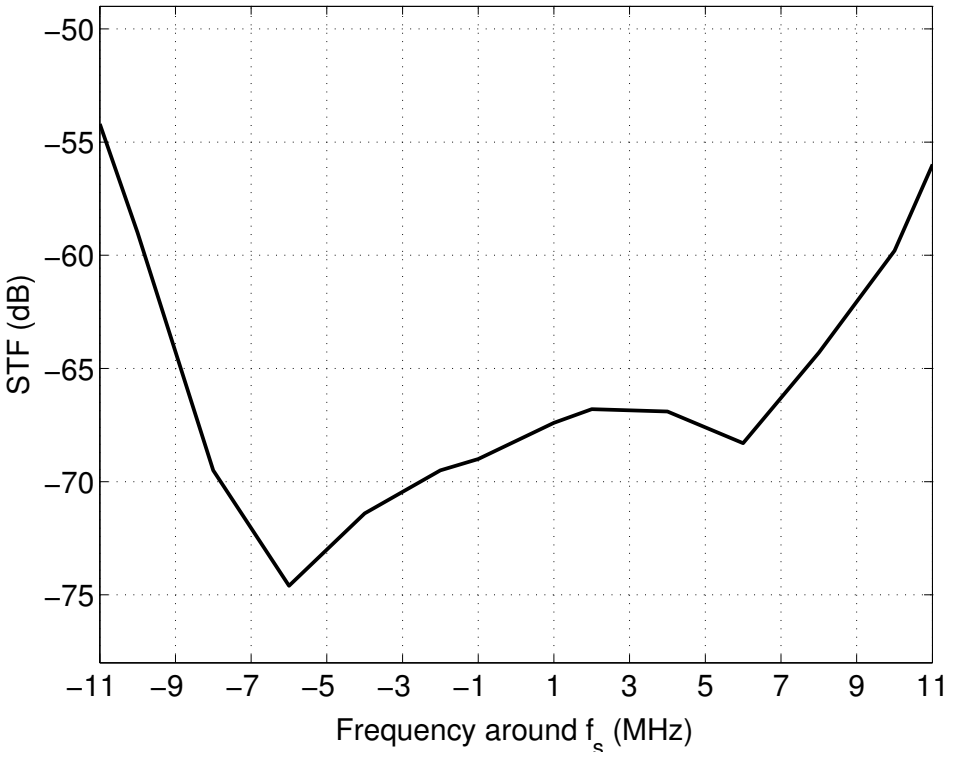

Figure 9.10: Anti-aliasing property: Signal transfer function (STF) magnitude response at the output of the CTDSM.

Table 9.2: Summary of measured ADC performance

Specification	Value
Sampling Frequency	600 MHz
Input Bandwidth	11 MHz
Quantizer Range	$3\,V_{pp,diff}$
DR	80 dB
Peak SNR	72 dB
Power	45 mW (1.8 V)
Figure of Merit	0.25 pJ/level
Active Area	$1\,mm \times 1\,mm$
Total Area	$1.5\,mm \times 1.5\,mm$
Technology	$0.18\,\mu m$ UMC CMOS

Table 9.3 compares the measured results of this work with other CT $\Delta\Sigma$ ADCs operating at a sampling rate of 250 MHz or above. They are designed in different technologies with varying supply voltage which makes a true comparison difficult, but we nevertheless use the FOM to assess power efficiency. The 80 dB DR and 72 dB SNR of this work shows that a fast loop in parallel with the slow quantizer can be utilized in high speed applications, $2X$ faster than what has been done in $0.18\,\mu m$ CMOS process.

Table 9.3: Comparison of CT $\Delta\Sigma$ ADCs with similar input bandwidths.

Ref.	f_s (MHz)	BW (MHz)	DR/SNR (dB)	Power (mW)	Process	$FOM_{DR/SNR}$ $pJ/level$
[12]	300	15	67/64.6	70	$0.13\mu m$	1.28/1.68
[33]	320	10	58/55.5	15.2	$0.25\mu m$	1.17/1.56
[34]	160	10	67/63	122.4	$0.18\mu m$	3.35/5.3
[35]	240	7.5	77/71	89	$0.18\mu m$	1.05/2.05
[4]	300	15	70/67.2	20.7	$0.18\mu m$	0.27/0.37
[11]	640	20	80/76	20	$0.13\mu m$	0.06/0.1
[36]	950	10	86/86	40	$0.13\mu m$	0.12/0.12
This Work	**630**	**11**	**80/72**	**45**	$0.18\mu m$	**0.25/0.63**

where, $FOM_{DR/SNR} = \dfrac{Power}{2 \times BW \times 2^{(DR/SNR-1.76)/6.02}}$ [2]

CHAPTER 10

Conclusion and Future Work

10.1 Conclusion

The effect of excess looop delay (ELD) in continuous time delta sigma modulators has been studied. We proposed a technique for compensating much higher values of ELD (normalized to the clock period) than previously published. Since the ELD due to the quantizer limits the sampling rate in a given process, the proposed technique enables significantly higher sampling rates. This can be used to achieve much higher resolutions by increasing the oversampling ratio, or to achieve higher signal bandwidths. Based on this, CT $\Delta\,\Sigma$ ADC has been designed. This operates at 600 MHz using a fast parallel feedback to compensate the delay of the slow quantizer.

Also a new DAC cell calibration technique, which reduces the ELD, is introduced. A new feedforward opamp is used to realize the summer of the loop filter that helps in getting high unity-gain frequency in presence of a large load capacitance. The efficiency of the proposed design techniques are verified through measurement results from test chip fabricated in a $0.18\,\mu m$ CMOS process. The design techniques helps in achieving 80 dB dynamic range in a 11 MHz bandwidth with $2X$ increase in speed. The power consumption of the chip is 45 mW at 1.8 V supply.

10.2 Future Work

The 4-bit flash quantizer used in this work was power hugry and loaded the summing opamp of loop filter. This is a big contributor to the power consumption.

Also the *CML to CMOS* level shifter between the flash ADC and the DAC introdues extra delay in the $\Delta\Sigma$ loop. Possible methods to reduce power consumption are lisited below.

10.2.1 Replacing 4-bit to 3-bit quantizer

This chops the load on the summing opamp to half. Also power of the flash ADC itself reduces. But on doing so, the quantization noise increases by 6 dB. But its OK because at present, noise is limited by the dynamic distortion and thermal noise.

10.2.2 New latch topology

The final CML latch (Latch3 in 6.4) can be replaced by a topology that tracks in CML mode and regenerates to CMOS levels. This eliminates the *CML to CMOS* converter and can reduce delay and power consumption.

APPENDIX A

NTFs for lowpass modulators

$NTFs$ with all zeros and poles inside the unit circle obey the Bode sensitivity integral relationship [22]:

$$\int_0^{\pi} \log \left| NTF\left(e^{j\omega}\right)\right| d\omega = 0 \tag{A.1}$$

For a lowpass NTF, the large negative $\log|NTF(e^{j\omega})|$ in a small region near $\omega = 0$ is balanced by a small positive $\log|NTF(e^{j\omega})|$ over a wide range. As seen in Fig. 3.8, for ELD ≥ 1, the second sample of the NTF impulse response is always zero. As shown in [22], when the second sample is zero,

$$\int_0^{\pi} \cos(\omega) \log \left| NTF\left(e^{j\omega}\right)\right| d\omega = 0 \tag{A.2}$$

A "good" NTF for a lowpass $\Delta\Sigma$ modulator cannot be realized while satisfying the above relationship due to the following:
Since $\cos(\omega)$ is positive from 0 to $\pi/2$ and negative from $\pi/2$ to π, to balance a large negative $\log|NTF(e^{j\omega})|$ in a small region near $\omega = 0$, we require a large positive $\log|NTF(e^{j\omega})|$ in a region before $\omega = \pi/2$. This implies either an NTF with very high peaking or one without much attenuation in the signal band near $\omega = 0$. Neither of these makes for a good lowpass $\Delta\Sigma$ modulator, indicating that good lowpass $\Delta\Sigma$ modulators cannot be built with an excess loop delay of more than a clock cycle. The proposed idea circumvents this problem by using an additional loop with a delay less than one clock cycle. The NTF in our case (Eq. A.3):

$$NTF_{prop} = (1 + az^{-1})\frac{(1 - z^{-1})^4}{\sum_{m=0}^{4} b_m z^{-m}} \tag{A.3}$$

does not obey (A.1) despite having a zero valued second sample because the zero at $z = -a$ is outside the unit circle.

APPENDIX B

Pin details of the $\Delta\Sigma$ modulator chip

Table B.1: Functionality of each pin.

Pin	**Name**	**Functionality**
1,2,3,44	$a < 1 >$, a< 2 >, a< 3 >, a< 4 >	Capacitor tuning bits
4	Vdda	1.8 V supply voltage for the loop filter and biasing
5, 11, 15, 36, 38, 41	gnda	Ground
6, 7	Clkp, Clkm	Differential input clocks
8	OSR_ctrl	Controll to chose between OSR =25 (low), OSR =10 (high)
9	Iref_5uA	Reference current source $5\mu A$(sinking current)
10	Vref_flash	Controll for changing input swing of flash ADC. Nominal value =0.9 V
12	Vddd	1.8 V supply voltage for the flash ADC
13	Vcalon	Controll for making calibration on (high) and off (low).
14	Vref_dac	Controll for DAC unit cell current. Nominal value =0.9 V
16	Vdddac	1.8 V supply voltage for the DAC
17	rst	Reset the digital calibration logic (Reset when high)
18-25 and 28-35	Doutb $< 7 >$ to Dout $< 0 >$	Deserialized differential output LVDS data stream
26, 27	Clk_out, Clkb_out	Differential output LVDS clocks
37	Vdd_demux	1.8 V supply voltage for the Demux and IO pads
39, 40	Vinm, Vinp	Differential input signals
42	Vcm	Common mode reference voltage of 0.9 V
43	Iref_25p25 μA	Reference current source of value $25.5\mu A$(source current)

APPENDIX C

Test board

The schematic of the board is split into three portions. The schematic of the board with the ADC and the input and output interfaces is shown in Fig. C.1. The schematic of the board with the reference part is shown in Fig. C.2. The schematic of the board with the power supply part is shown in Fig. C.3.

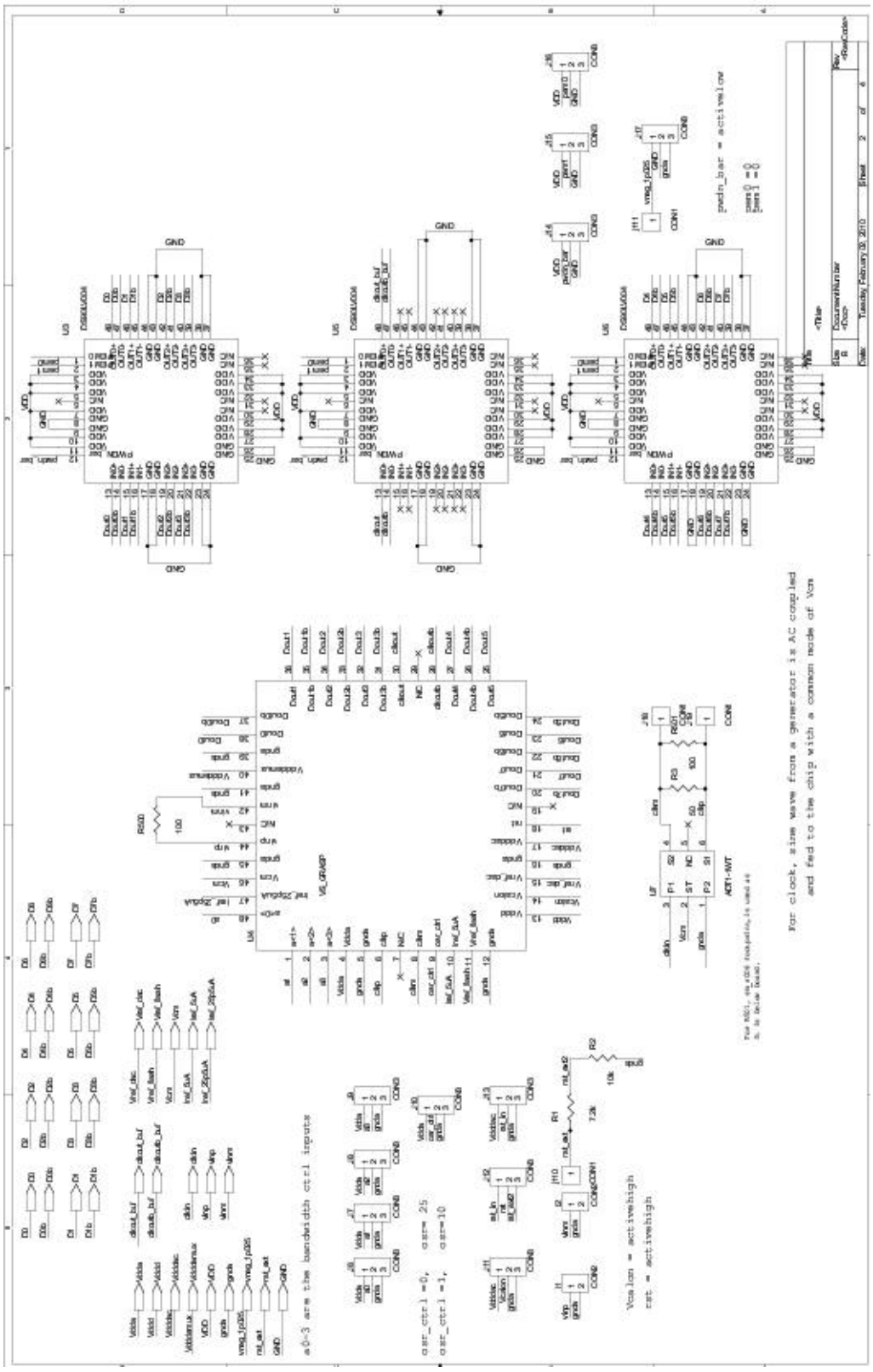

Figure C.1: ADC and its interfaces.

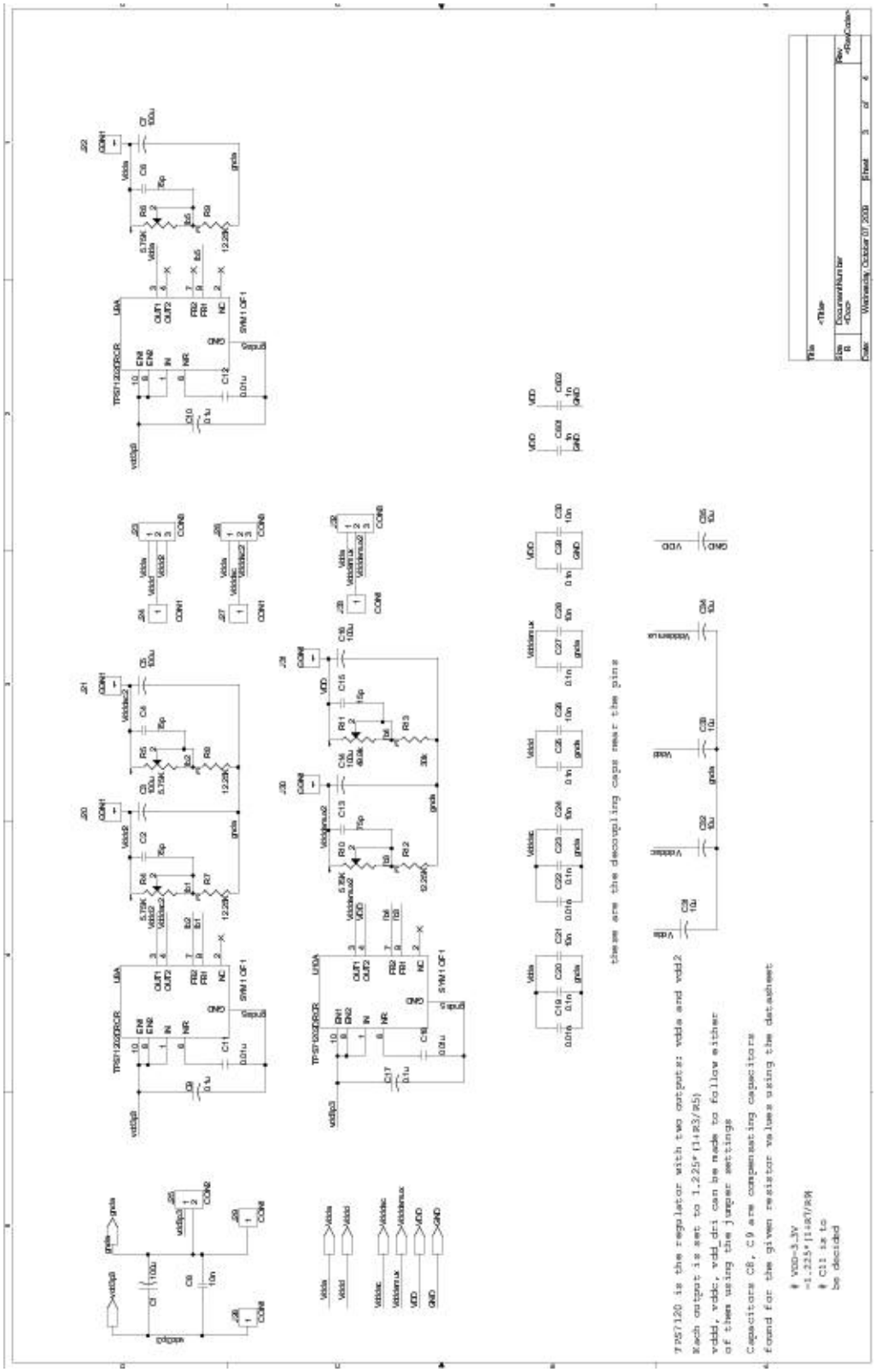

Figure C.2: Reference voltages and currents.

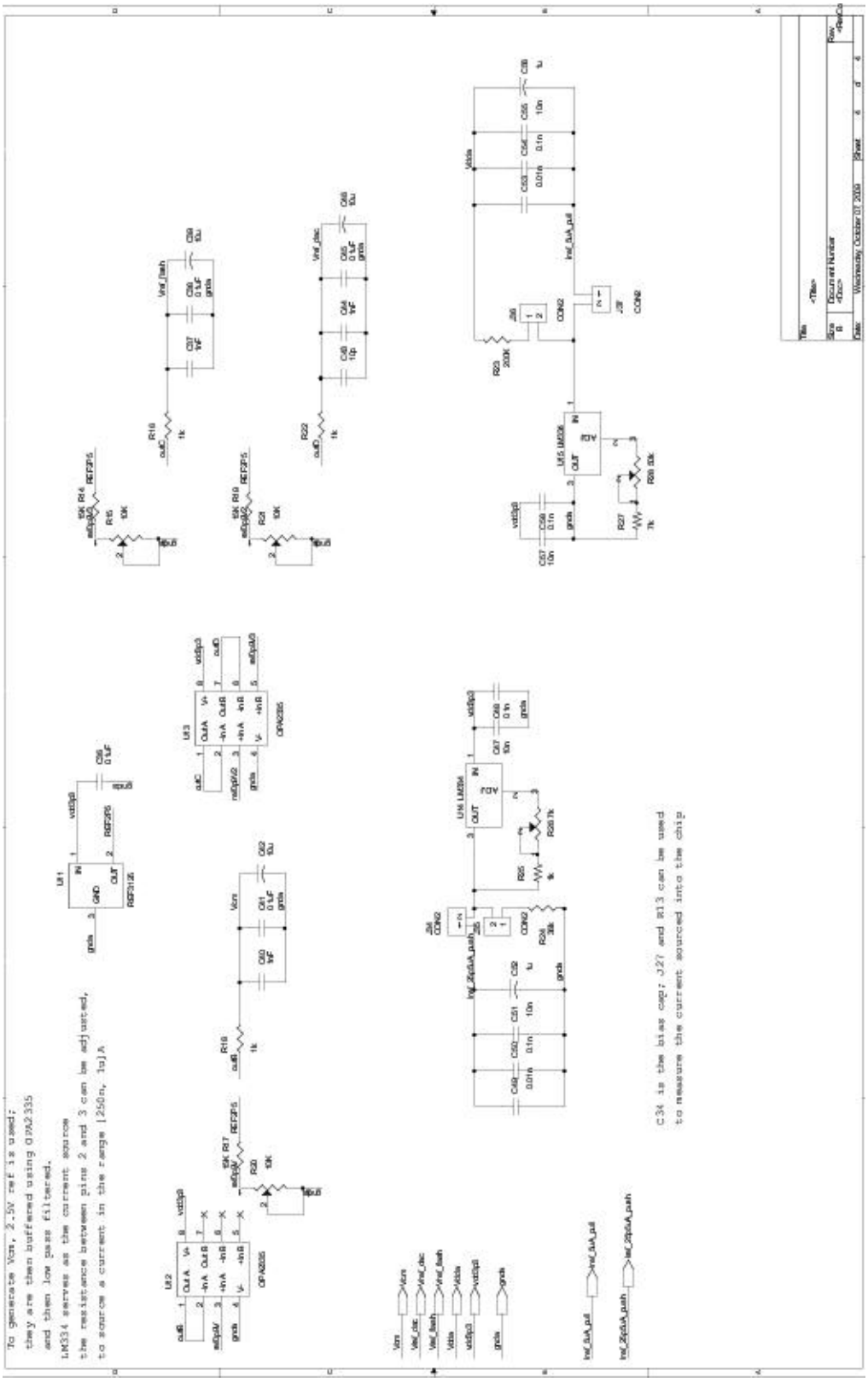

Figure C.3: Power supply.

APPENDIX D

Investigation of increase in the idle channel noise floor at the output of the modulator, due to low V_{th} of pMOS

The threshold voltage (V_{th}) of the pMOS in all the chips in this fabrication run was significantly lower than what is specified across process corners in 0.18 μm UMC CMOS. pMOS V_{th} was found to be around 0.2 V instead of 0.455 V. This low V_{th} affects the performance of the modulator, mainly due to the reduced DC gain of opamp1. Following is the reasoning done to prove this point.

- Fig. D.1 show that if V_{th} of pMOS reduced form 0.5 V to 0.3 V (the parameter V_{th} is reduced in the model file), the DC gain of opamp1 is reduces by 20 dB. This is because the input pair G_m ($M_{p1,p2}$ in Fig. 4.7) reduces with reduction in pMOS V_{th}, as they go into triode region (vcascp, derived from the current in Fig. 4.8, goes towards Vdd).
- If we increase the common mode voltage of input signal to 1.1 V from 0.9 V for this low V_{th} case, we can see that the DC gain increased by 15 dB (Fig. D.1), but the UGF reduces, because of reduction in G_{m3} ($M_{p6,p7}$ in 4.7). This is because, second stage bias current (current through M_{b2} in Fig. 4.7) depends on both, V_{ds} and V_{gs}. With increased input Vcm, V_{ds} reduces for the second stage current source (M_{b2}) and hence G_{m2} and G_{m3} also reduces.
- But, if Vcmref of CMFB circuit (Fig. 4.7) is also increased to 1.1 V, then gate voltage of the second stage current source reduces and hence increase in current (pMOS) through it. This increases the UGF along with DC gain of opamp1.
- Hence we should expect improvement in performance when overall Vcm of the loop filter is increased. This is what we get in the test chip when overall Vcm was increased. The next paragraph discusses the effect of reduced DC gain of opamp1 on the performance of the modulator.

Fig. D.2 shows the architecture of CTDSM implemented in this work. Following

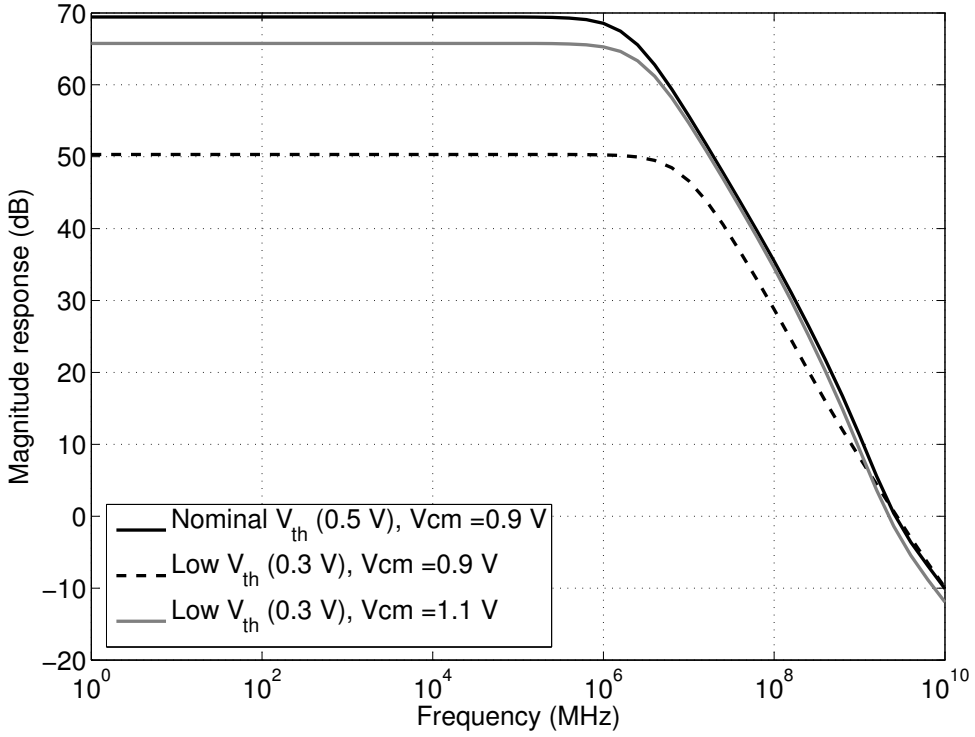

Figure D.1: AC response of the opamp1 of loop filter (circuit level simulation) for (a) Nominal V_{th} (0.5 V) of pMOS with input Vcm = 0.9 V (b) Low V_{th} (0.3V) of pMOS with input Vcm = 0.9 V (c) Low V_{th} of pMOS with input Vcm = 1.1 V.

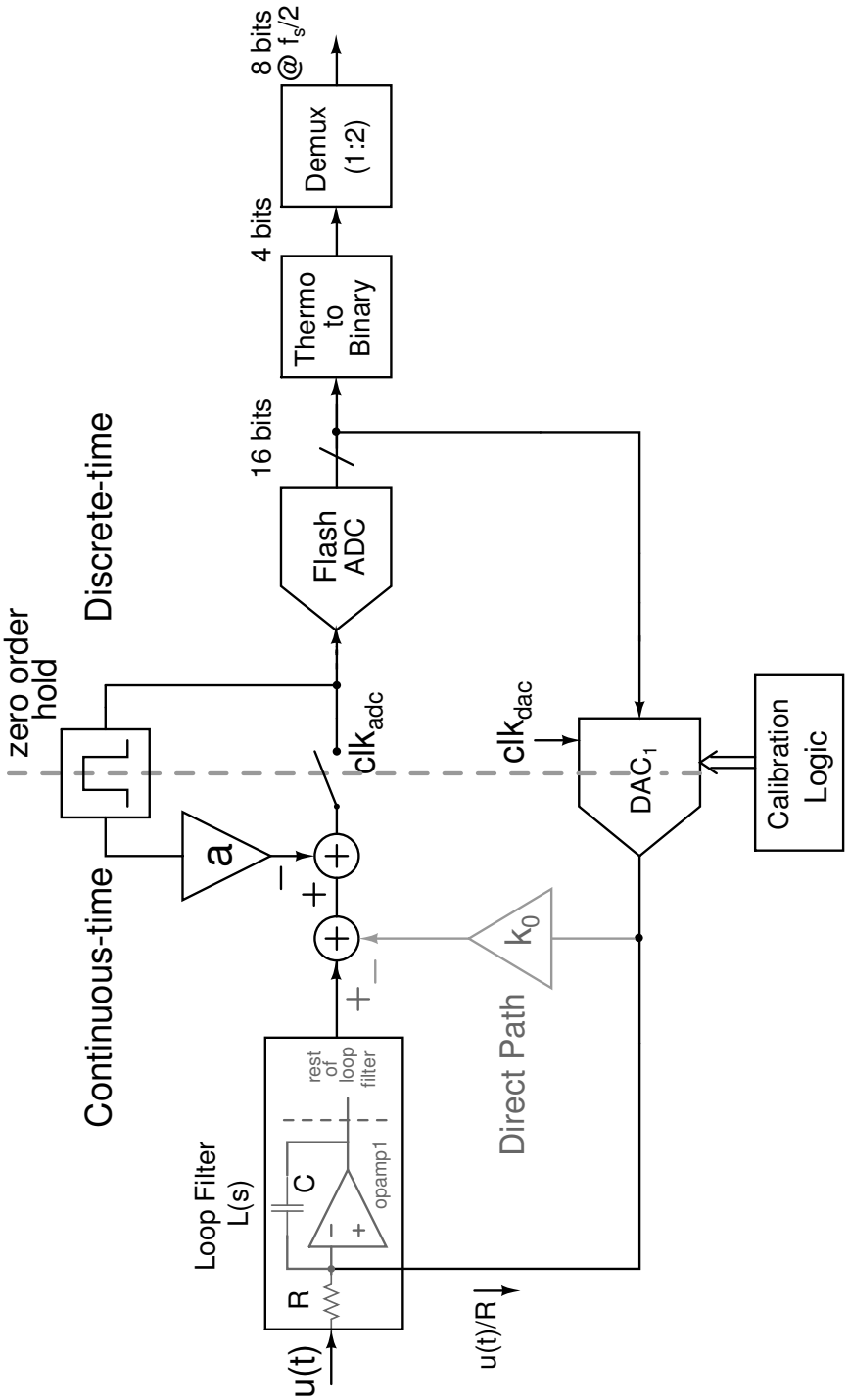

Figure D.2: Block diagram of the designed CTDSM.

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simulation and inferences were made while trying to analyze the effect of low V_{th} of pMOS (and hence low DC gain of opamp1). Simulation are done with pMOS $V_{th} = 0.3\,\mathrm{V}$.

- In Fig. D.2, when we used real opamp1 (schematic) and all other blocks as ideal for simulation, there was 2.5 dB reduction in SNR.
- Now with only real feedback DAC and all other blocks as ideal, there was almost no reduction in SNR.
- But with real opamp1 and real feedback DAC together, there was 7dB reduction compared to the case with nominal V_{th}. This is because now DAC sees more swing at its output (virtual node of opamp1 input in Fig. D.2). So the dynamic nonlinearty due to sampling of the virtual ground node voltage on the DAC cell tail nodes increases.
- To make sure that the above point is the culprit, the feedback DAC was terminated with ideal virtual ground and ideal current control current source (CCCS) is used to feed the DAC current to the virtual node of the opamp1. In this case, DAC sees a virtual node at its output. So we should not see any increase in the noise floor as DAC current is not modulated by opamp1 virtual mode swing. This indeed was the case, there was almost no reduction in the noise floor.
- The reason for increase in the signal swing at the virtual node of the opamp1, is due to the reduced DC gain of opamp1, which indeed is due to reduced V_{th} of pMOS, as explained before.
- In simulation, to reduce the signal swing at the virtual node, input Vcm was increased. But as explained before, this also reduces G_{m3} and hence the UGF. So there was not much improvement after increasing input common mode of signal u(t) (in Fig. D.2).
- When Vcmref of the CMFB loop is also increased, the UGF of the opamp1 increases along with the DC gain. This test setup shows 2 dB improvement in performance.

All the simulation and inferences where consistent with the silicon results that we got from the test chip, which is expected to have low V_{th} (around 0.2 V) for pMOS. Low V_{th} of pMOS is found by ploting I-V characterices of two diode connected pMOS transistors in series, in the reference current branch on the chip.

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