A Technique to Reduce Distortion in Active-RC Filters

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **A Technique to Reduce Distortion in Active-RC Filters**, submitted by **Siva Viswanathan T**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally, I would like to dedicate this thesis to my parents and my brother for their support and encouragement through my entire life.

ABSTRACT

In this project, we present a technique for reducing distortion in Active-RC filters using the method of current injection. The project involves the design of two fifth order lowpass Chebyshev filters with a passband ripple of 1 dB and a bandedge of 20 MHz in 0.18 μm CMOS process.

In the first design, the filter has been designed using a two-stage Miller compensated opamp for high output swings. The current injection technique in this case has been implemented using a replica biquad and experimental results on the test chip prove the efficacy of the technique. The filter with current injection gives a distortion improvement of around 9 dB near the bandedge and an IIP3 improvement by a factor of 1.9. The noise of the filter is unaffected with current injection. The power consumption of the filter without and with injection are 4.09 mW and 5.06 mW respectively. With 23% extra power, we get an improvement of 9 dB. The filter occupies an area of 0.33 mm^2.

In the second design, the filter has been implemented using a single-stage folded cascode opamp. The current injection is achieved using linear transconductor biased in their triode region. A circuit technique to fix the transconductance of these triode transistors has also been implemented. Simulation results show that the filter with current injection gives a distortion performance of around 14 dB near the bandedge and an improvement in IIP3 by 10 dB. The power consumption of the filter with/without injection are almost the same and is around 5.5 mW. The noise of the filter is unaffected with current injection. Each filter occupies an area of around 0.33 mm^2. The design has been sent for fabrication.

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ABBREVIATIONS

AC	Alternating current
ADC	Analog to Digital converter
BALUN	Balanced-Unbalanced
BQ1	Biquad 1
BQ2	Biquad 2
CMFB	Common mode feedback
CMOS	Complimentary Metal Oxide Semiconductor
CMRR	Common mode rejection ratio
DC	Direct current
DSL	Digital Susbcriber Loop
FOS	First order section
IEEE	Insititute of Electrical and Electronics Engineers
IF	Intermediate frequency
IIP3	Input Third Order Intercept Point
IMD	Intermodulation distortion
JLCC	J-leaded chip carrier
LAN	Local Area Network
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel MOSFET
OPAMP	Operational Amplifier
PMOS	p-channel MOSFET
TI	Texas Instruments®
UGF	unity gain frequency

CHAPTER 1

Introduction

1.1 Motivation

Continuous-time filters form an essential part of several systems today. They are mainly used as anti-aliasing filters in ADC applications and also for achieving communication in hard disk read channels. These filters act as channel selection filters in IEEE 802.11 Wireless LANs, in the direct end receiver architecture design. Several other applications include signal extraction in lock-in amplifiers, to separate telephone and digital signals in DSL lines, graphic equalizers in stereo systems and also in low IF Blue tooth receivers.

The important parameter which governs the performance of these filters for most of these applications is its dynamic range. The lower limit of the filter's dynamic range is decided by the generated noise and on the upper limit it is decided by its distortion. With the rapid scaling of CMOS technology in the last decade, the available supply voltage for analog designers has reduced considerably. In order to achieve high dynamic range with the low supply voltages in today's CMOS technology, the analog designer must make the best use of this available power supply (i.e. maximize the swings at the output of the filter). With increased signal swings, non-linearities in the filter dominate and this limits the maximum achievable dynamic range. Thus, any effective technique which can reduce distortion in a power efficient manner (resulting in a greater dynamic range for the filter) would be beneficial.

In this thesis, a new technique for reducing the distortion has been proposed. Two variations of the technique have been discussed and verified using simulation/experimental results. The theory and design of the building blocks of the

two filters has been discussed. Experimental results for one of the fabricated chips is also given.

1.2 Organisation of Thesis

Chapter 2 introduces the filter type, architecture and type of implementation used.

Chapter 3 explains the proposed technique of reducing distortion.

Chapter 4 discusses the design of a Fifth Order Active-RC Chebyshev filter using Replica Biquad Current Injection.

Chapter 5 discusses the macromodel simulations and Design simulation results.

Chapter 6 explains the measurement Techniques, the design of the testboard and measured experimental Results.

Chapter 7 explains the design of a Fifth Order Active-RC Chebyshev filter with Current Injection using Triode transconductors.

Chapter 8 discusses simulation Results for the Active-RC Chebyshev filter with Current Injection using Triode transconductors.

Chapter 9 gives the conclusions and scope for future work.

CHAPTER 2

Filter type, architecture and implementation

Continuous-time filters can be classified mainly into four categories namely the Butterworth, Chebyshev (Type I), Inverse Chebyshev (Type II) and the Elliptic filter. The response of these filters is shown in Fig. 2.1.

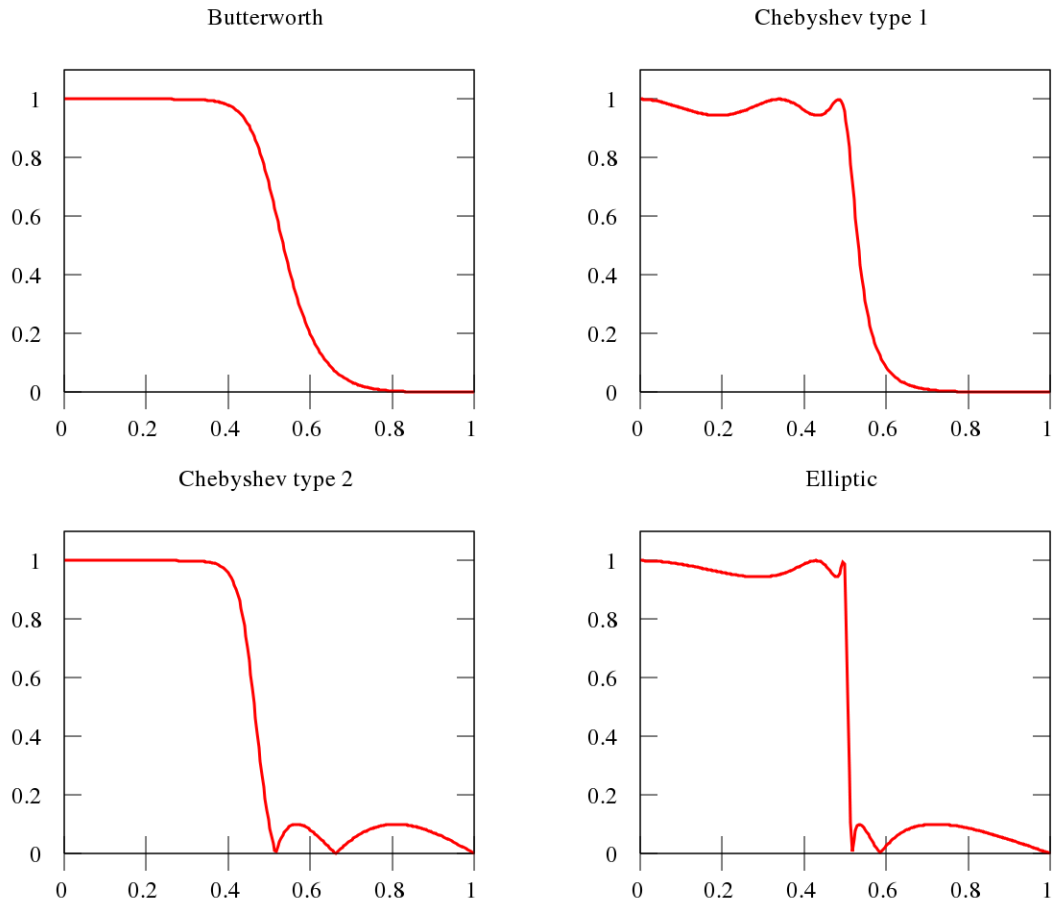


Figure 2.1: Respone of the various filter types [1]

Depending on the needs of the application, the appropriate filter type is chosen. The various steps involved while choosing a filter type is given in a flowchart in Fig. 2.2. In our design, we consider the design of a fifth order lowpass Chebyshev (Type I) filter with a passband ripple of 1 dB.

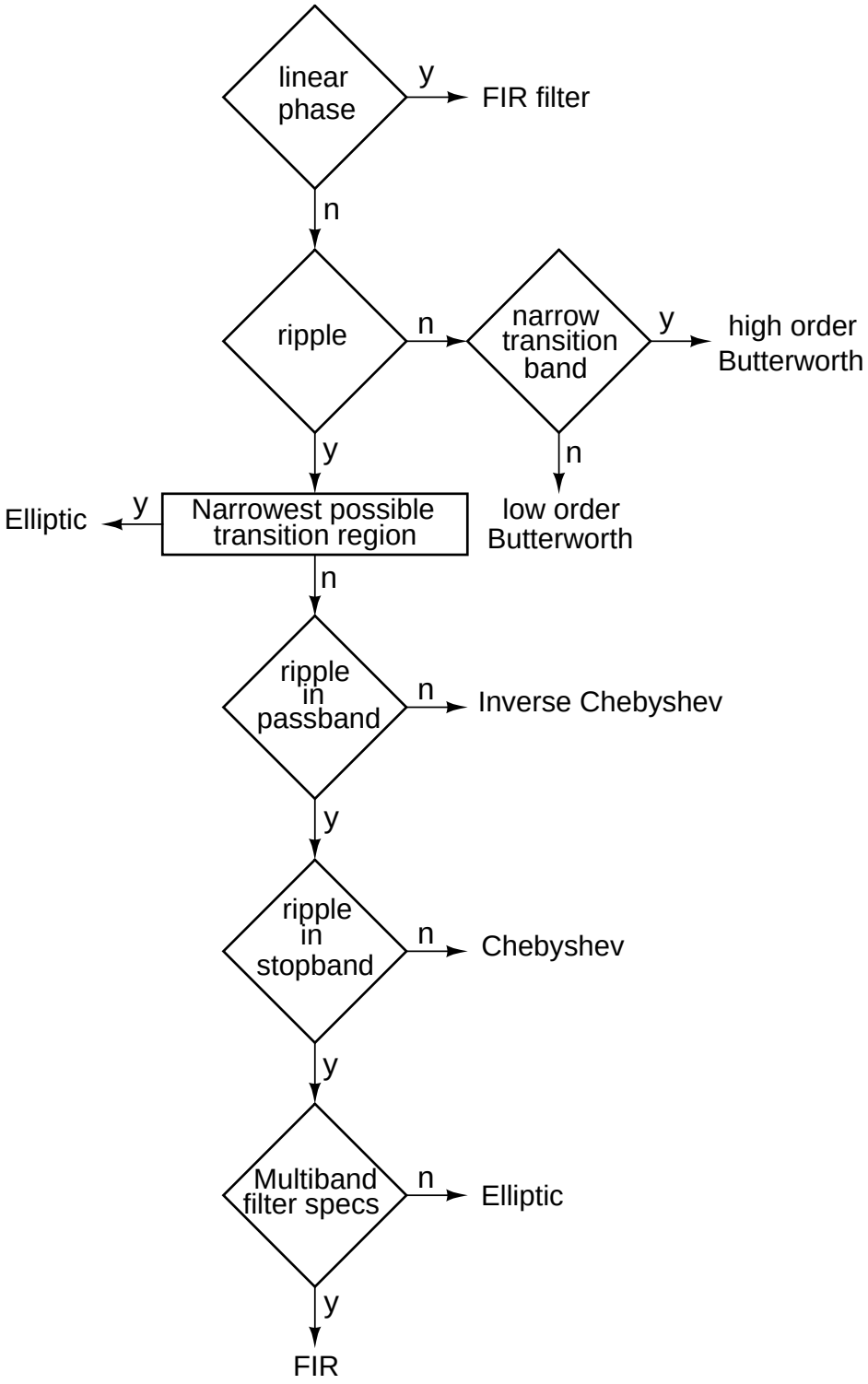


Figure 2.2: Flowchart for selecting the filter type [2]

2.0.1 Filter transfer function

The magnitude response $|H(j\omega)|$ of an n^{th} order lowpass Chebyshev filter is given as

$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2(c_n(\omega))^2} \tag{2.1}$$

where ϵ is a parameter to decide the passband ripple and $c_n(\omega)$ is the Chebyshev polynomial and is given as

$$\begin{aligned} c_n(\omega) &= \cos(n\cos^{-1}(\omega)) \qquad \omega < 1 \\ &= \cosh(n\cosh^{-1}(\omega)) \qquad \omega > 1 \end{aligned}$$

For our analysis $n = 5$. For a fifth order filter with a bandedge of 1 Hz we get the transfer function $H(s)$ as

$$H(s) = \frac{1}{1 + 0.7523s + 0.201s^2 + 0.0554s^3 + 0.0049s^4 + 0.0008s^5} \tag{2.2}$$

The transfer function can be split into a first order and two second order sections and implemented as a cascade. For the first order section, the pole is at -1.8189. For the second order systems the poles are at $-1.4716 \pm 3.8448j$ and $-0.5621 \pm 6.2210j$.

2.1 Implementation

Typical topologies of filter implementation include the G_m-C and Active-RC architectures. Filters implemented using the G_m-C architecture suffer from non-linearity at high signal swings. This is because the poles of the filter depend on the transconductance values which in turn is a non-linear function of the input. In comparison, Active-RC filters are more linear but at high frequencies, finite band-

width of the opamp affects their linearity. Compared to the G_m-C, the Active-RC architecture results in lesser distortion for the same amount of power consumption. Active-RC filters are also less noisier than their G_m-C counterparts. For these reasons, an Active-RC topology was chosen in the design of these filters.

2.1.1 First order section

The schematic of the first order section is shown in Fig. 2.3. The pole of this system occurs at $\frac{1}{RC}$.

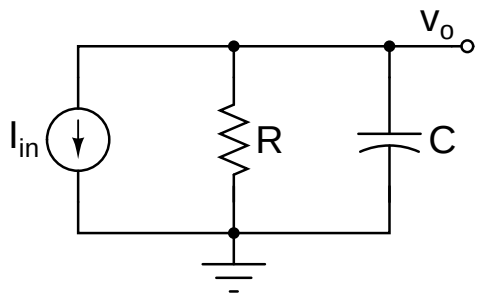


Figure 2.3: First order section

Fig. 2.4 shows the Active RC implementation of the first order section. The current $i_{in} = v_{in}/R$ and the transfer function $H(s)$ is given as

$$H(s) = \frac{1}{1 + sRC} \tag{2.3}$$

2.1.2 Second order section

The schematic of a bandpass second order section is shown in Fig. 2.5. The transfer function $H(s)$ of this filter can be shown to be of the form

$$H(s) = \frac{\frac{s}{\omega_p Q_p}}{1 + \frac{s}{\omega_p Q_p} + \left(\frac{s}{\omega_p}\right)^2} \tag{2.4}$$

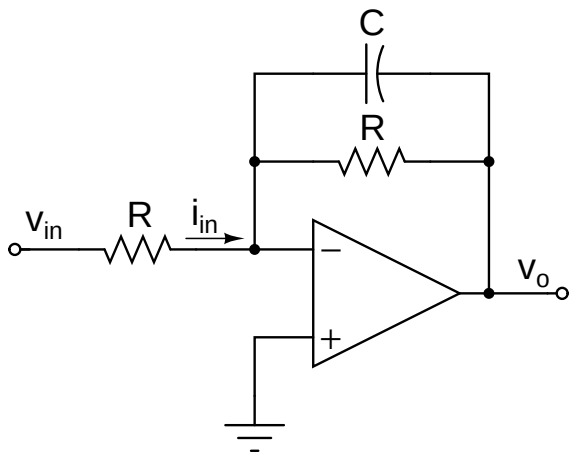


Figure 2.4: First order section Active RC implementation

where $Q_p = \frac{R}{\sqrt{\frac{L}{C_1}}}$ is the quality factor and $\omega_p = \frac{1}{\sqrt{LC_1}}$ is the cut-off frequency.

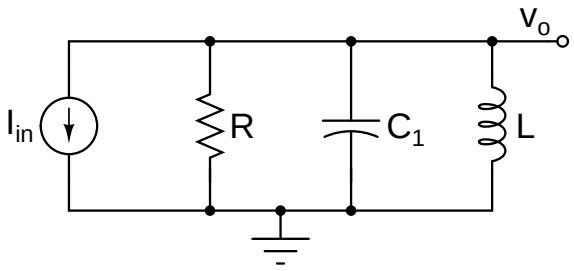


Figure 2.5: Second order section

Fig. 2.6 shows the Active RC implementation of the second order section. In order to implement the inductor, we discuss the steps shown in the Figure. If the inductor is replaced with a current source as shown, the circuit transfer function remains unaltered. We use the duality between the inductor and capacitor and generate this required current using opamps. The inductance value is thus given as $L = R^2C_2$ and $Q_p = R_1/R$. Using such a topology, also gives us the required low pass second order transfer function $v_{o,lp}$ to implement the filter.

2.1.3 Node scaling and ordering of the filter sections

From the circuit implementation, we observe that the number of design parameters available is much more than the constraints. The input resistor values can

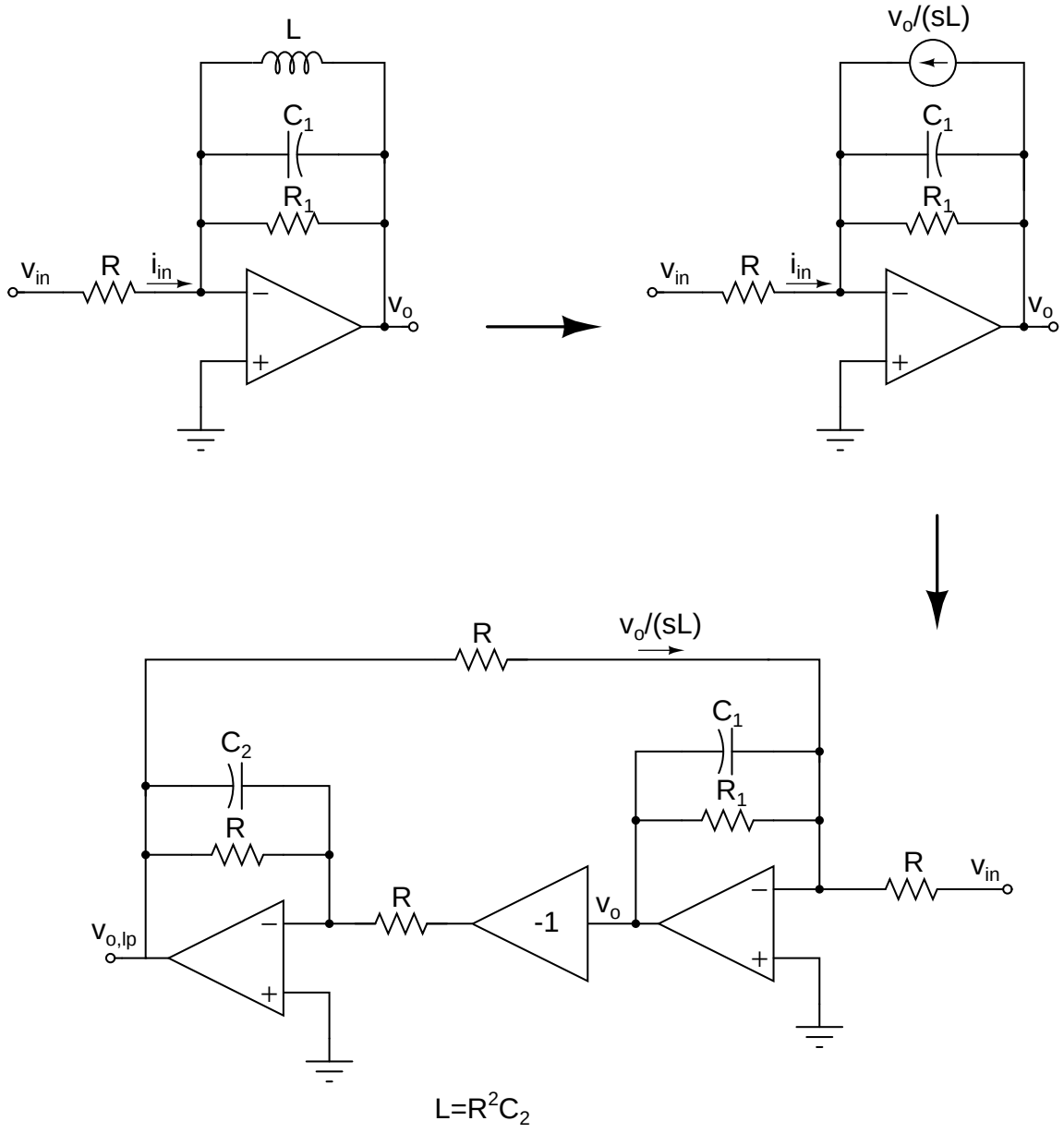


Figure 2.6: Second order section Active RC implementation

be decided based on the output noise specifications. In order to maximize the dynamic range at every intermediate node, the resistor and capacitor values are altered to ensure equal maximum swing at each of these nodes. The response at every intermediate node must also be made as flat as possible. Thus, we also need to consider the ordering of the filter sections. The first order section has a flat roll-off from dc and is thus chosen as the first section. Cascading BQ1 to the output of the FOS ensures that the intermediate nodes remain as flat as possible. The same is applicable for BQ2 which is implemented in cascade with BQ1.

2.2 Q enhancement

In the analysis carried out in the previous section, the opamps have been assumed to be ideal. In practice, the opamps have a finite gain and finite bandwidth. We now discuss the effect of Finite gain and Parasitic pole on the response of the filters.

2.2.1 Finite gain

The pole plot of the filter transfer function is shown in Fig. 2.7. The magnitude of the transfer function of the filter at the point shown ω_a is given as

$$|H(j\omega_a)| = \frac{1}{|j\omega_a - p_1|.|j\omega_a - p_2|.|j\omega_a - p_3|.|j\omega_a - p_4|.|j\omega_a - p_5|} \tag{2.5}$$

In other words, it is the inverse of the product of the distances of the each pole from the frequency point being considered i.e. ω_a. With finite gain of the opamp, the $j\omega$ axis shift to the right i.e. $H(j\omega) \rightarrow H(j\omega + k_0)$, where k_0 is a constant. Therefore, the distance of each pole from the frequency point considered increases. This causes the response of the filter to droop.

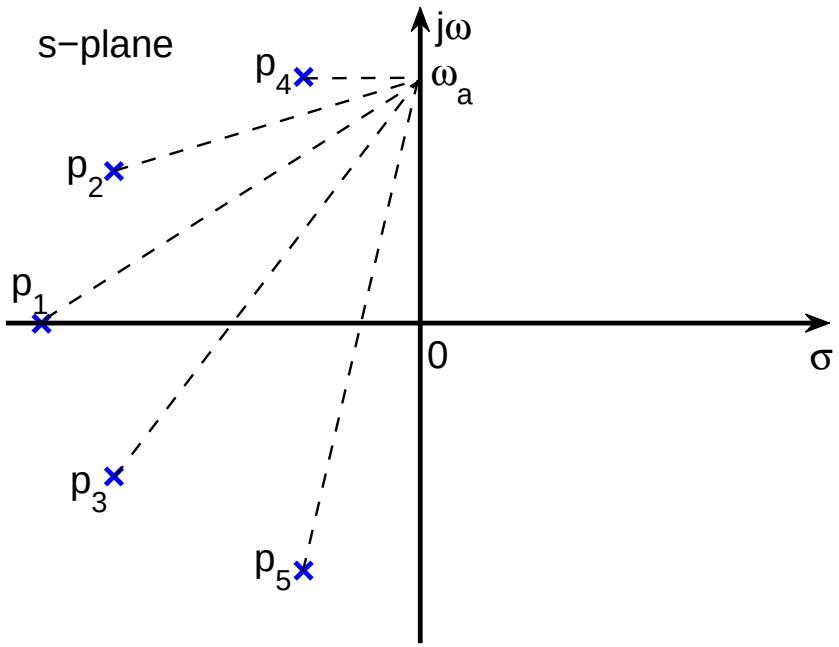


Figure 2.7: Pole-zero diagram for filter transfer function

2.2.2 Parasitic pole

With the introduction of a parasitic pole say ω_p in the opamp's transfer function, the filter transfer function transforms from $H(j\omega) \rightarrow H(j\omega - \frac{\omega^2}{\omega_p})$. Hence, the response is now evaluate over a parabolic curve as shown in Fig. 2.8. Since, the distance of each pole from the frequency point considered decreases and this decrease is maximum near the highest Q pole, we would see some Q enhancement for BQ1 and much more for BQ2. For a second order system as described in (2.4), the poles of the system in frequency (Hz) axis with $\omega_p = 1$ are at $p = -\frac{1}{2Q} \pm j\sqrt{1 - \frac{1}{4Q^2}}$. With a high Q biquad, the imaginary part of the pole is approximately equal to 1. The real part of the high Q pole is $1/(2Q)$. Hence, the new Quality factor Q' with an opamp parasitic pole is given as

$$2Q' = \frac{1}{\frac{1}{2Q} - \frac{1}{\omega_p}} \tag{2.6}$$

$$Q' = \frac{Q}{1 - \frac{2Q}{\omega_p}} \tag{2.7}$$

For a well-designed opamp, $\frac{1}{\omega_p} \ll \frac{1}{2Q}$. Therefore, as ω_p reduces the peaking increases.

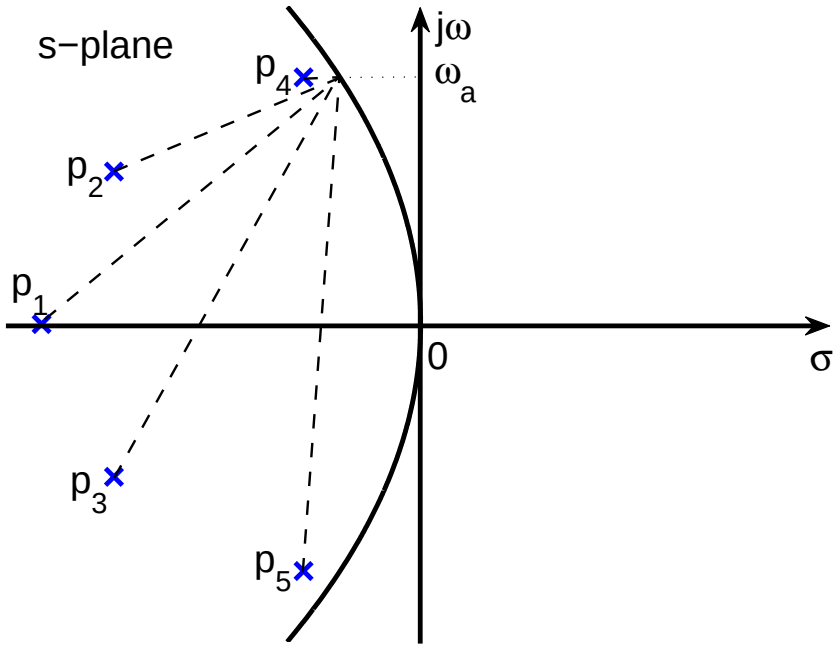


Figure 2.8: Pole-zero diagram for filter transfer function with parasitic pole

In order to account for the changes in frequency response due to these factors, the resistance and capacitance values are tweaked to get back the desired response. Hence, we would observe variations in the resistance and capacitance values for the filter without/with the implemented technique.

CHAPTER 3

Proposed Technique for reducing distortion

In this chapter, we propose a technique for reducing distortion. We consider the effects of using this technique on various performance measures such as power consumption, noise and distortion. This technique has been used in the design of filters using single and two-stage opamps. Hence, we restrict our discussion to these opamp topologies. Since the basic concept is the same, this technique can be extended to other architectures also.

3.1 Distortion in single, two-stage opamps

Distortion occurs due to the inherent non-linearity of the transistors which are the main building blocks of the opamp. In order to measure the distortion of a circuit to a sinusoidal input, several techniques have been proposed in literature. The analysis of distortion can be performed using a state space methodology as in [3] or using Volterra series based methods. In [3], the state space modeling of non-linearity in G_m-C filters has been discussed. A time domain approach has been used to describe the system using differential equations and this can be implemented easily in Matlab®. In our analysis, we employ the phasor method introduced in [4],[5] and used extensively in [6] to analyze the distortion in single, two and three stage opamps.

In order to illustrate the phasor method, we consider an RC integrator circuit using a single-stage opamp. The opamp can be modeled as a transconductor,

whose output current i_{out} is given as

$$\begin{aligned} i_{out} &= I_{max}\tanh(\frac{g_m v_i}{I_{max}}) \\ &\approx g_m v_i - \beta {v_i}^3 \end{aligned} \tag{3.1}$$

where $g_m v_i \gg \beta {v_i}^3$ (considering weak non-linearity) and $\beta = k_0(g_m/I_{max})^3$. Here, I_{max} is the maximum possible output current from the transconductor, g_m its transconductance, v_i its input voltage swing and k_0 is a constant. Only odd-order non-linearities are considered because the implementation is fully differential.

Fig. 3.1 shows the RC integrator circuit. Let us assume that the input to the integrator is a sinusoid with $v_i(t) = A_i \sin(2\pi f_i t)$. Assuming the transconductors to be linear as shown in Fig. 3.2, we find the fundamental phasor components (denoted with suffix $fund$) of the controlling voltages of the non-linear transconductor (namely $v_{x,fund}$ at frequency f_i). We get

$$v_{x,fund} = \frac{A_i}{1 + g_m R} \tag{3.2}$$

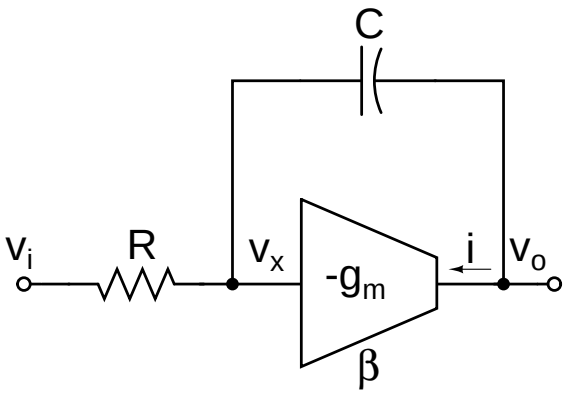


Figure 3.1: Model of an RC integrator using a single-stage opamp

In order to calculate the third harmonic distortion, we consider the linear circuit in Fig. 3.3. The circuit now is operating at the third harmonic frequency $3f_i$. The fundamental input source is grounded and the third harmonic distortion

source i_3 causes distortion at the output. The magnitude of i_3 is given as

$$i_3 = 0.25\beta {v_{x,fund}}^3 \tag{3.3}$$

where $v_{x,fund}$ is as calculated in (3.2).

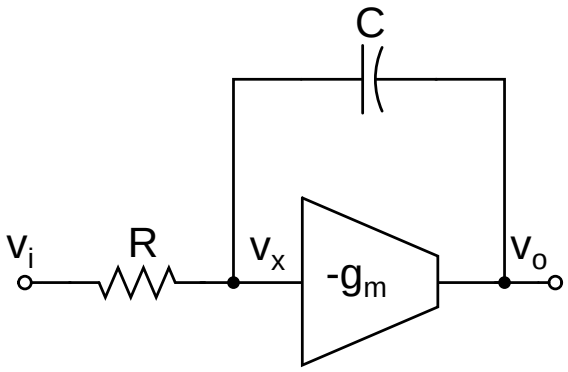


Figure 3.2: Model of an RC integrator using a single-stage opamp : Evaluating the fundamental component

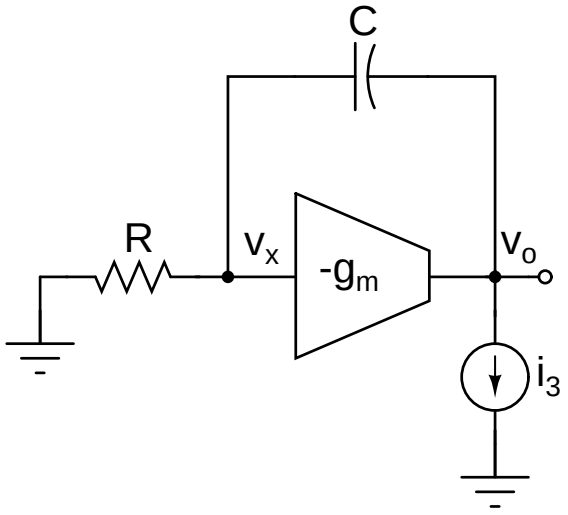


Figure 3.3: Model of an RC integrator using a single-stage opamp : Evaluating the distortion component

We thus find the third harmonic phasor component (denoted with suffix *dist*) of the controlling voltage of the transconductor (namely $v_{x,dist}$ at frequency $3f_i$)

as

$$v_{x,dist} = -\frac{0.25\beta R}{1+g_m R} {v_{x,fund}}^3 \tag{3.4}$$

$$= -\frac{0.25\beta R}{(1+g_m R)^4} {A_i}^3 \tag{3.5}$$

The distortion at the output $v_{o,dist}$ is thus given as

$$v_{o,dist} = \frac{1+j2\pi(3f_i)RC}{j2\pi(3f_i)RC} v_{x,dist} \tag{3.6}$$

We now proceed with the same technique for the discussion of distortion in a two-stage Miller compensated opamp. The integrator RC circuit is shown in Fig. 3.4.

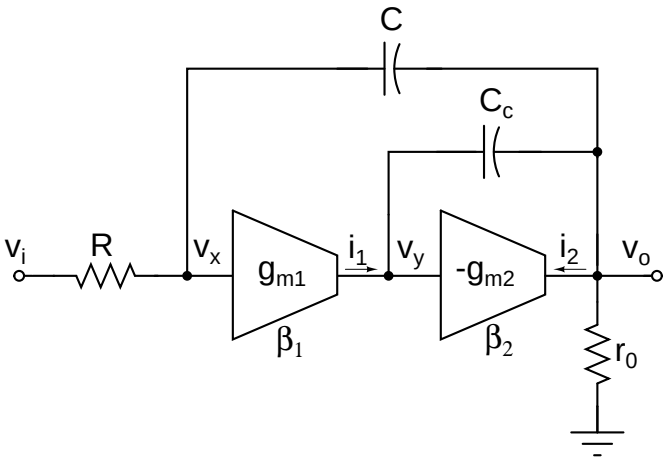


Figure 3.4: Model of an RC integrator using a two-stage Miller compensated opamp

As before, the input to the integrator is a sinusoid with $v_i(t) = A_i \sin(2\pi f_i t)$. Assuming the transconductors to be linear, we find the fundamental phasor components (denoted with suffix $fund$) of the controlling voltages of the non-linear transconductors (namely $v_{x,fund}$, $v_{y,fund}$, $i_{1,fund}$, $i_{2,fund}$ at frequency f_i).

We get

$$i_{2,fund} \approx \frac{A_i}{R}(1 + \frac{C_c + C}{C} - j\frac{1}{2\pi f_i r_0 C}) \tag{3.7}$$

$$i_{1,fund} \approx \frac{C_c}{C}\frac{A_i}{R} + j2\pi f_i C_c \frac{i_{2,fund}}{g_{m2}} \tag{3.8}$$

The control voltages are found as

$$v_{x,fund} = \frac{i_{1out,fund}}{g_{m1}} \tag{3.9}$$

$$v_{y,fund} = \frac{i_{2out,fund}}{g_{m2}} \tag{3.10}$$

In order to calculate the third harmonic distortion at the output, the linear circuit is excited using current sources (at the output of the transconductors) operating at the third harmonic frequency ($3f_i$). These current sources have a magnitude of $0.25\beta_1(v_{x,fund})^3$ and $0.25\beta_2(v_{y,fund})^3$ where $v_{x,fund}$ and $v_{y,fund}$ are as calculated in (3.9) and (3.10). We must note that the magnitude of this distortion current is proportional to the cube of the controlling voltage. We thus obtain the third harmonic component of distortion (denoted with suffix *dist*) at the output as

$$v_{o,dist} \approx -\frac{0.25\beta_1(v_{x,fund})^3}{g_{m1}(\frac{j2\pi(3f_i)RC}{1+j2\pi(3f_i)RC})} - \frac{0.25\beta_2(v_{y,fund})^3}{[\frac{g_{m1}g_{m2}}{j2\pi(3f_i)C_c}.(\frac{j2\pi(3f_i)RC}{1+j2\pi(3f_i)RC})]} \tag{3.11}$$

From (3.11), we notice that the distortion at the output of the integrator is a sum of the contributions from the first and the second stage of the opamp. The distortion component from the second stage is divided by a large factor because for a well-designed opamp $g_{m1}/(2\pi f C_c) \gg 1$. The relative contributions of each stage depends on the individual stage's non-linearity factor (β). As an example, for applications with high signal swings at the output, the distortion contribution from the second stage is significant.

3.2 Proposed technique of Current Injection

The technique of current injection is based on the gain-enhancement concept introduced in [7]. In this work, a replica is used to boost the output resistance of the main amplifier, thereby increasing its dc gain. The method described in this paper has severe noise penalty if applied to a single-stage or the first stage of a two-stage opamp. Several amplifier designs [8], [9], [10], that utilize this gain-enhancement technique have been reported in the literature. We use this concept in our filter design to reduce the distortion levels at the output. We show two methods of current injection and discuss the conditions under which these can be applied.

In order to understand the concept of current injection, we consider the circuit shown in Fig. 3.5. If the current source i_{inj} is not present, the distortion of the circuit is as given in (3.4). We note that the component of distortion is proportional to the cube of the fundamental component of the controlling voltage of the transconductor. The fundamental component of current supplied by the transconductor is given as $i = g_m.v_{x,fund}$. If we now inject a current $i_{inj} = g_m.v_{x,fund}$, the output current is no longer supplied by the transconductor. Due to the feedback in the circuit, the current supplied by the transconductor reduces and the magnitude of the controlling voltage $v_{x,fund}$ also decreases. This causes a reduction in the distortion contribution from the transconductor as is evident from (3.4). Hence, the distortion at the output of the circuit also decreases.

A similar procedure can be also applied for the two-stage opamp. Fig. 3.6 shows the circuit diagram of the injection technique. Here, two currents $i_{2,inj}$ and $i_{1,inj}$ with magnitudes as in (3.7) and (3.8) respectively, are injected as shown. This causes the net fundamental component of the currents from the transconductors, namely $i_{1,fund}$ and $i_{2,fund}$ to be negligible. Therefore, from (3.9) and (3.10), the input swing of the transconductors $v_{x,fund}$ and $v_{y,fund}$ reduces. This causes the distortion component at the output of the integrator to decrease, from (3.11).

We now consider the block level implementation of the current injection technique. We propose two ways of implementing the technique.

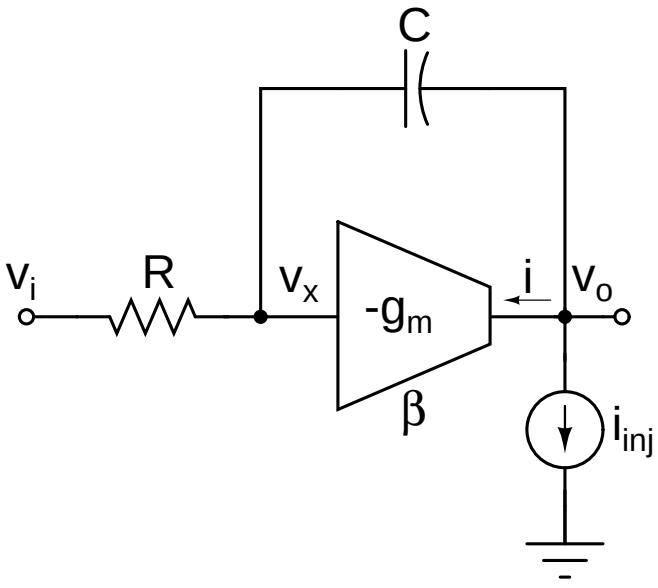


Figure 3.5: Model of an RC integrator using a single-stage opamp with Current Injection

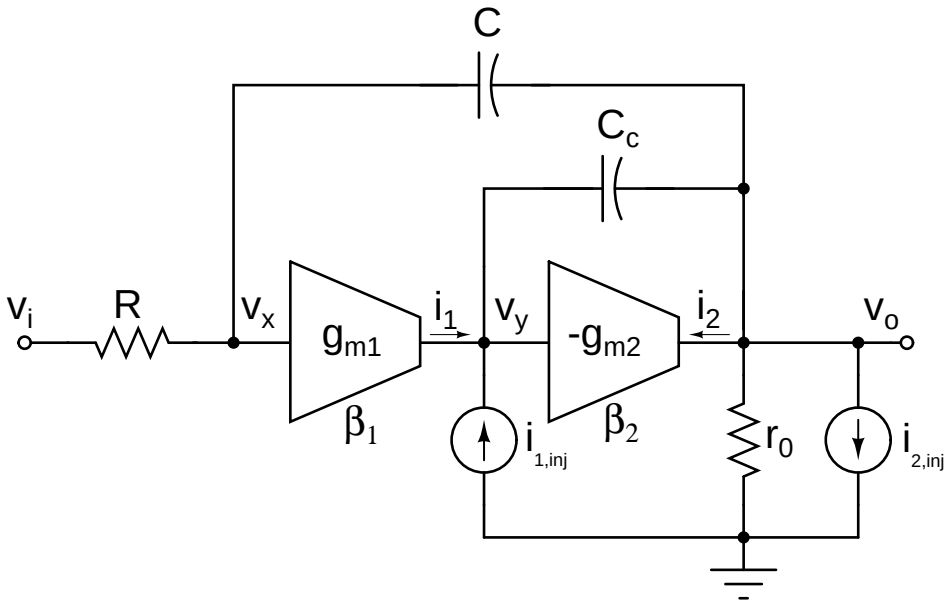


Figure 3.6: Model of an RC integrator using a two-stage Miller compensated opamp with Current Injection

3.2.1 Technique 1

Distortion

Fig. 3.7 shows the first implementation technique. In this method, a replica of the integrator circuit is used. The controlling voltage of the transconductor in the replica circuit is used to inject current into the main integrator using a similar g_m block. This helps in reducing the distortion at the output. Using the phasor method as before for solving the distortion of the circuit, we obtain the third harmonic distortion of the controlling voltage v_x as

$$v_{x,dist} = -\frac{0.25\beta R}{(1+g_m R)^5} {A_i}^3 \tag{3.12}$$

From (3.5) and (3.12), we observe that the distortion has reduced by a factor of $g_m R$. In general, for a well designed opamp, the loop gain is high and hence $g_m R \gg 1$.

Noise

The noise contributed by the transconductor can be modeled as a noise current source at its output with a current spectral density $S_i = \frac{8}{3} k_B T g_m$, where k_B is the Boltzmann constant, T the temperature and g_m the transconductance. From Fig. 3.7, we observe that the noise current source at the output of the circuit consists of three components. One due to the main transconductor itself, the other due to the injection transconductor and the third due to the replica transconductor. Hence, with this kind of injection scheme there is a heavy penalty in terms of noise.

Even though the above technique may not be effective for a single-stage opamp, it can still be implemented for a two-stage Miller compensated opamp. Here, we inject current only in the second stage of the opamp. Current injection at the output of the first stage of the opamp causes loading problems at the virtual ground

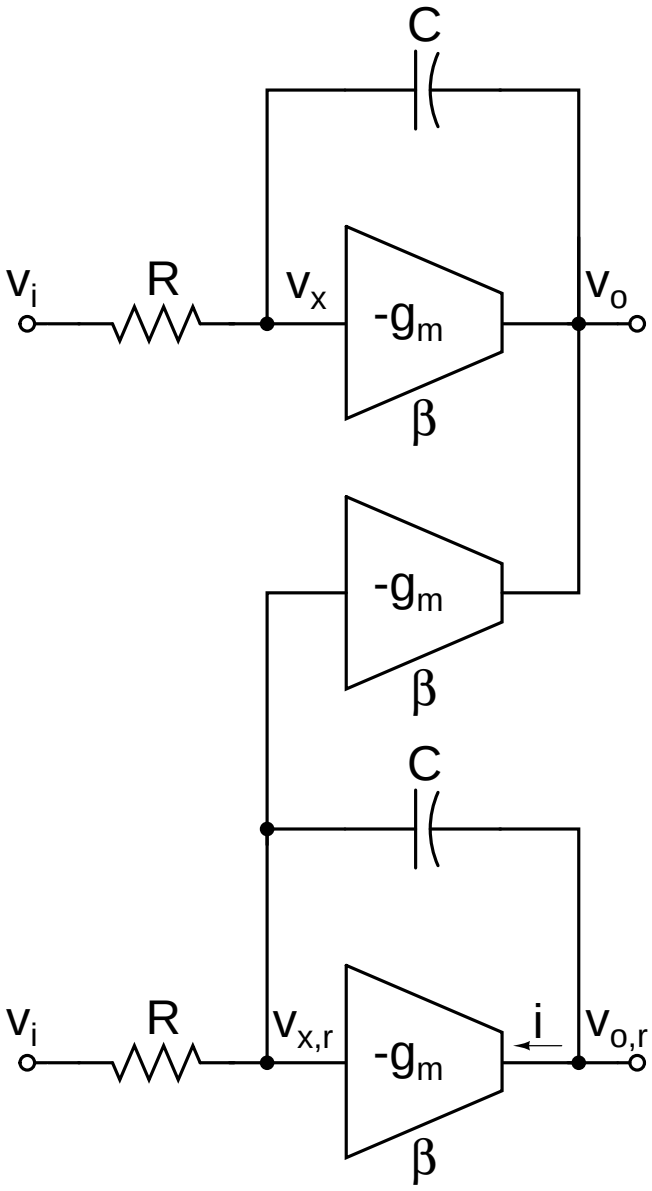


Figure 3.7: Model of an RC integrator using a single-stage opamp with Current Injection : Technique 1

node in the replica and leads to stability issues. Since the first stage in an opamp is typically a telescopic architecture with many transistors, the implementation is also complicated. Hence, we consider the injection technique for the second stage alone. In order to achieve high signal swings for the filter, cascode transistors cannot be used in the output stage of the opamp. This causes the output impedance of the opamp to be very low. Due to this low output impedance, the current requirement from the second stage and hence its contribution towards distortion, increases. Since there is no current injection in the first stage of the opamp, there is no penalty in terms of noise. We now show that current injection at the second stage doesnot alter the noise at the output of the filter.

To simplify the analysis, we consider the RC integrator circuit as before and neglect the output resistance r_0. Fig. 3.8 shows the circuit with current injection technique. The replica integrator circuit is impedance scaled by a factor k. We denote the feedback factor as $\eta = \frac{sRC}{1+sRC}$. Since the second stage of the opamp is used for driving the load, in general we have $g_{m2} \gg g_{m1}$. Also, for a well designed opamp, we have $g_{m1}/(2\pi f C_c) \gg 1$ and $C \gg C_c$. We use these to determine approximate analytical expressions for the noise spectral density.

For the case without current injection, the noise at the output is from three sources, namely the resistor R and the transconductors g_{m1} and g_{m2}. The noise voltage of the integrator referred to the input (denoted as $v_{ni,woinj}$) is evaluated as

$$v_{ni,woinj} \approx -[v_{nR} + \frac{i_{n1}}{g_{m1}(1-\eta)} + \frac{i_{n2}}{\frac{g_{m1}g_{m2}}{sC_c}(1-\eta)}] \tag{3.13}$$

Therefore, from (3.13), we get the input referred noise spectral density as

$$\begin{aligned} S_{vni,woinj} = S_{vnR} + \frac{(1+\omega^2R^2C^2)}{g_{m1}^2}.S_{in1} \\ +(\frac{\omega C_c}{g_{m2}})^2.\frac{(1+\omega^2R^2C^2)}{g_{m1}^2}.S_{in2} \end{aligned} \tag{3.14}$$

For the case with current injection, the noise at the output has additional

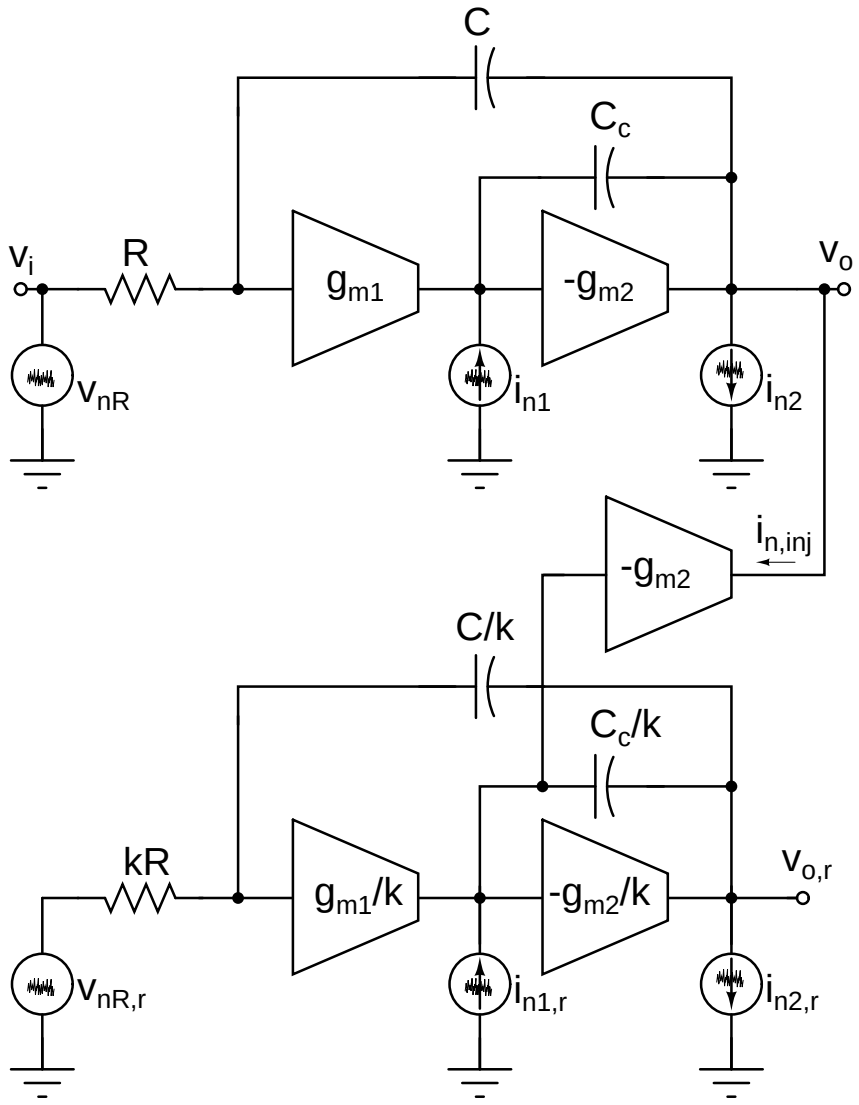


Figure 3.8: Noise analysis for an integrator circuit with current injection technique

components due to the injected noise current from the replica and the injection transconductor itself. The injected noise current into the main integrator is computed as

$$i_{n,inj} \approx \sqrt{k}.[\frac{1}{R}.(1+\frac{C_c}{C})v_{nR} + \frac{i_{n1}}{g_{m1}R} - i_{n2}] \tag{3.15}$$

Hence, adding this noise spectral density due to (3.15) to that obtained for the case without current injection, we get the input referred noise spectral density for the case with injection as

$$\begin{aligned} S_{vni,winj} = [1 + k.\frac{(1+\frac{C_c}{C})^2}{(\frac{g_{m1}}{\omega C_c})^2}.\frac{(1+\omega^2R^2C^2)}{(g_{m2}R)^2}].S_{vnR} \\ + \frac{(1+\omega^2R^2C^2)}{g_{m1}^2}[1 + k.\frac{1}{(g_{m1}R)^2(\frac{g_{m2}}{\omega C_c})^2}].S_{in1} \\ + \frac{(1+\omega^2R^2C^2)}{(\frac{g_{m1}g_{m2}}{\omega C_c})^2}[2+k].S_{in2} \end{aligned} \tag{3.16}$$

From (3.16), we observe that with current injection, an incremental noise is added to the expression obtained in (3.14). For the noise contributed by the resistor and the first transconductor, these incremental noise quantities are negligible. For the second transconductor, this incremental noise is significant and dependent on the scaling factor of the replica. Even though the noise contributed by the second transconductor is enhanced by injection, it is negligible in comparison to the noise added by the first transconductor because $g_{m2}/(2\pi f C_c) \gg 1$. Hence, the total noise without/with injection are approximately the same.

Power

The implementation of this technique requires an additional replica circuit in order to estimate the value of the controlling voltage. This causes the power consumption to be very high (100% extra). In order to save power, the replica circuit can be impedance scaled. The power consumed in the injection transconductor

is another factor which needs to be considered. In the design of the filter using this opamp architecture, we have proposed a new implementation technique, which saves power in the replica as well as the injection transconductor. This is discussed in Chapter 4.

3.2.2 Technique 2

Distortion

Fig. 3.9 shows the second implementation technique. In this method, no replica circuit is used. We notice that if the loop gain of the feedback circuit is high, the virtual ground node of the opamp i.e. v_x has almost zero magnitude. Hence, the current supplied by the transconductor $i \approx v_i/R$. Thus, to inject current into the output of the opamp, we use another transconductor with transconductance $g_{mx} \approx 1/R$ and control voltage v_i. This causes the swing at the virtual ground node of the opamp to reduce further and thus decreases the output distortion. The injection transconductor must have a good linearity to minimize its contribution towards distortion. This technique is particularly useful for single-stage opamps because there is only one stage which contributes to distortion.

Noise

The injection of current using this technique has little effect on the output noise of the filter. As we discussed earlier, the noise of the transconductor block can be modeled as a noise current source at its output. The ratio r of the spectral density of the main transconductor to the injection transconductor is given as

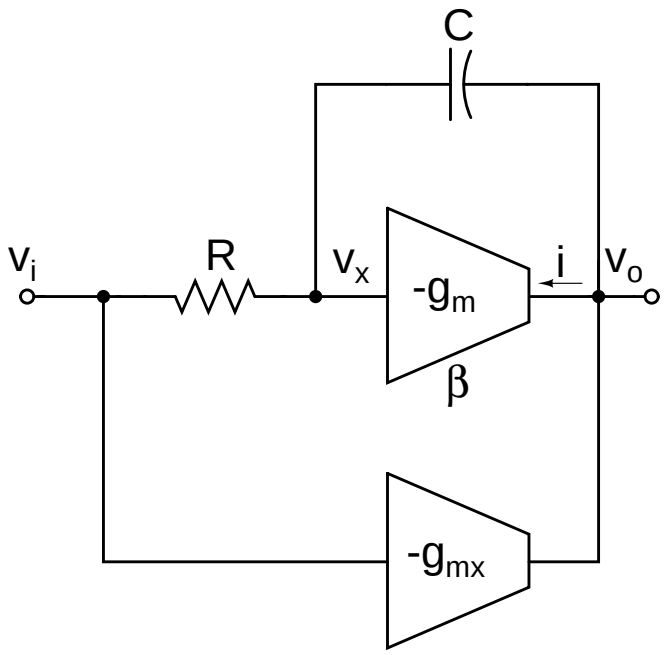


Figure 3.9: Model of an RC integrator using a single-stage opamp with Current Injection : Technique 2

$$r = \frac{\frac{8}{3}k_B T g_m}{\frac{8}{3}k_B T g_{mx}} = g_m R \gg 1 \tag{3.17}$$

Hence, the noise generated by the noise current source due to the main transconductor is much higher than that of the injection transconductor and thus the overall noise of the circuit does not change with injection.

Power

In this technique, no replica circuit is used for current injection. The extra power consumption in the injected circuit can be only due to the injection transconductor g_{mx}. In the design of the filter using a single-stage opamp architecture, we have proposed a new implementation scheme which has almost zero overhead in terms

of power. This is discussed in detail in Chapter 7.

CHAPTER 4

Design of a Fifth Order Active-RC Chebyshev filter using Replica Biquad Current Injection

In order to validate the proposed technique, a fifth order Active-RC low-pass Chebyshev filter is designed in 0.18 μm CMOS process with a supply voltage of 1.8 V. The bandwidth of the filter is 20 MHz and the passband ripple was chosen to be 1 dB. The filter is fully differential with a common mode equal to half the supply voltage. This filter first technique of implementation of the current injection scheme discussed in Chapter 3. In this chapter, we focus on the design details of each of the blocks which make up the filter. Fig. 4.1 shows the block diagram of the designed chip. The filter here is implemented as a cascade of FOS, BQ1 and BQ2 sections.

4.1 Opamp Design

Each of the sections in the filter i.e. first/second order are realized as a negative feedback system with the opamp as the active element. In order to achieve high output swings, a two-stage opamp is generally preferred as its gain is very high. Design of opamps with more than two-stages is difficult because of frequency compensation complications. For a two-stage opamp, frequency compensation can be achieved using the Feed forward technique or using Miller compensation. In the Feed forward technique, the opamp is stabilized by introducing a zero in its transfer function. This is done by adding a parallel path from the input to the output. This makes the opamp behave as a second order system at low frequencies and as a first order section near its unity gain frequency. In the Miller compensated technique, the opamp is stabilized by pole-splitting. The poles of the

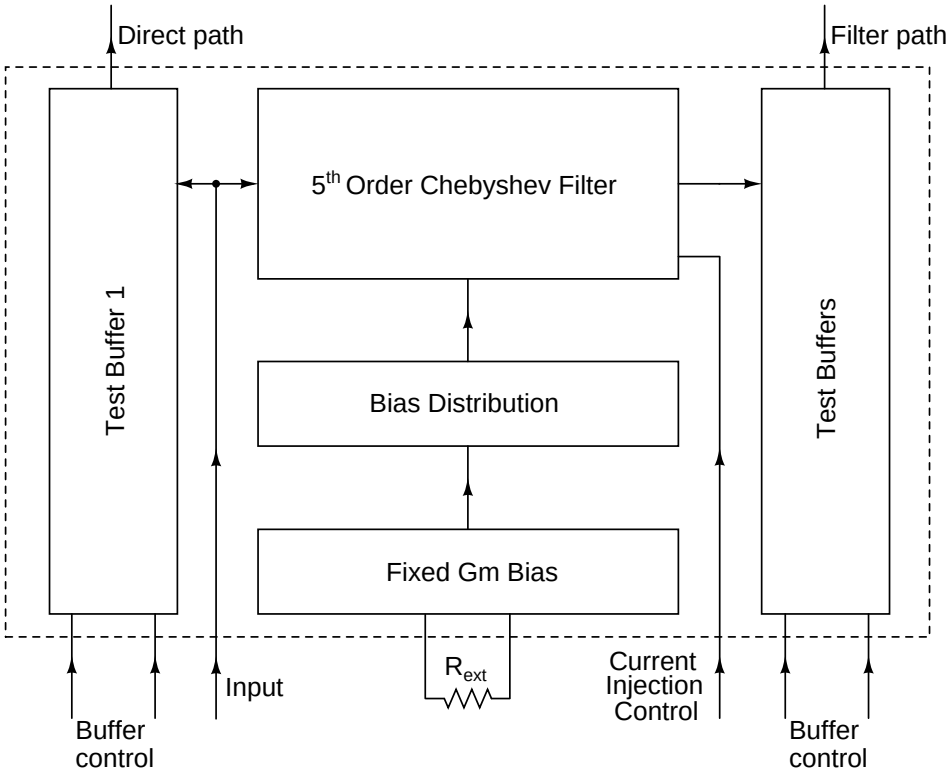


Figure 4.1: Block diagram of the chip

opamp are separated to make the opamp behave mainly as a first order system. This technique results in a greater bandwidth penalty compared to the former, but the output swings are limited in the feedforward architecture. In this design, we use the two-stage Miller compensated opamp to realize the filter.

4.1.1 First stage

The schematic of the first stage of the opamp is shown in Fig. 4.2. It is realized using a fully differential telescopic cascode stage. M1 is used to bias the transistors at a constant current provided by the fixed transconductance bias circuitry. The input differential pair comprises of M2a and M2b and transistors M5a and M5b act as active loads. Cascode transistors M3 and M4 are used to boost the first stage gain of the opamp. In order to maintain the output common mode voltage, the gates of M5a and M5b are controlled using a common mode feedback loop, discussed in Section 4.1.3. In order to reduce the flicker noise of the opamp, PMOS

transistors have been used as the input pair.

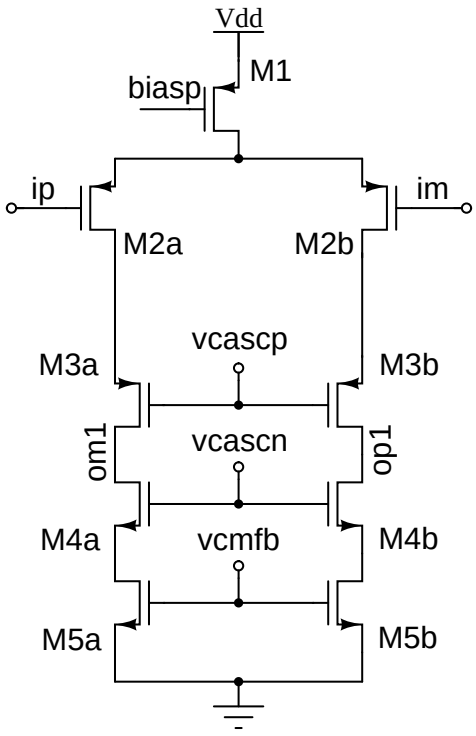


Figure 4.2: First stage of the Miller compensated opamp

4.1.2 Second stage

The schematic of the second stage of the opamp is shown in Fig. 4.3. The output of the first stage is applied as input to the NMOS differential pair M12a and M12b. Transistors M11a and M11b act as the active load. Since the output stage comprises only of PMOS and NMOS transistors, the output swing of the opamp is very high. Theoretically, the maximum peak-to-peak output differential swing possible possible is $2.(V_{sup} - V_{dsat,p} - V_{dsat,n})$, where V_{sup} is the supply voltage and $V_{dsat,p}$ and $V_{dsat,n}$ are the PMOS and NMOS saturation voltages. In order to reduce the capacitance at the output of the opamp, transistors M11 and M12 have minimum lengths. This causes the intrinsic output impedance of the opamp to be very low. Capacitor C_c is used as the Miller capacitor for stabilizing the opamp and its value is fixed depending on bandwidth and common-mode stability requirements.

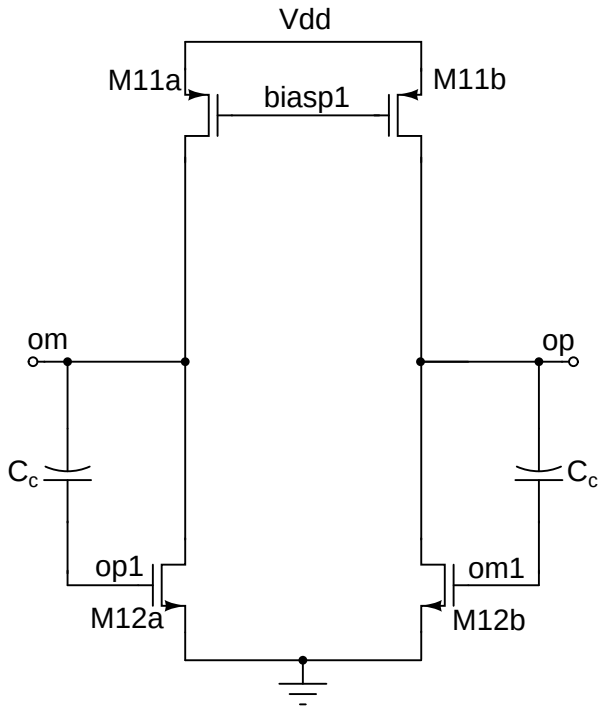


Figure 4.3: Second stage of the Miller compensated opamp

4.1.3 Common mode feedback loop

The common mode feedback loop circuitry is shown in Fig. 4.4. In order to fix the output common mode voltage of the opamp, a single common mode feedback loop is used. The output common mode is detected by the parallel combination of resistor R and capacitor C. The capacitor is used in order to enhance the bandwidth of the common mode loop. The measured output common mode is then fed to the error amplifier comprising of transistors M6-M10. In this implementation, one-half of the error amplifier is implemented as part of the first stage. This is done in order to avoid startup problems with the opamp. To avoid offset problems in the output common mode voltage, transistors M2a, M7a, M7b; M5, M10; M4 and M9; M3 and M8 must have the same current density. Any error in the common mode voltage results in a difference in the current between the two halves of the common mode feedback loop. The negative feedback loop corrects this by tweaking the current source M5a, M5b in the first stage of the opamp, thus fixing the output common mode voltage to the desired value.

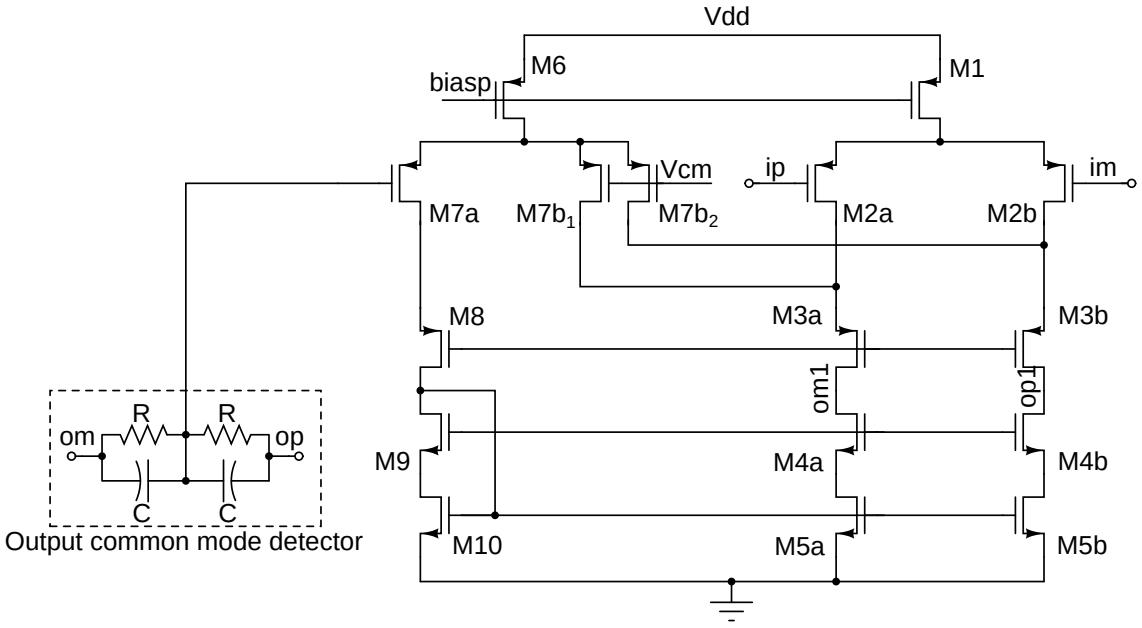
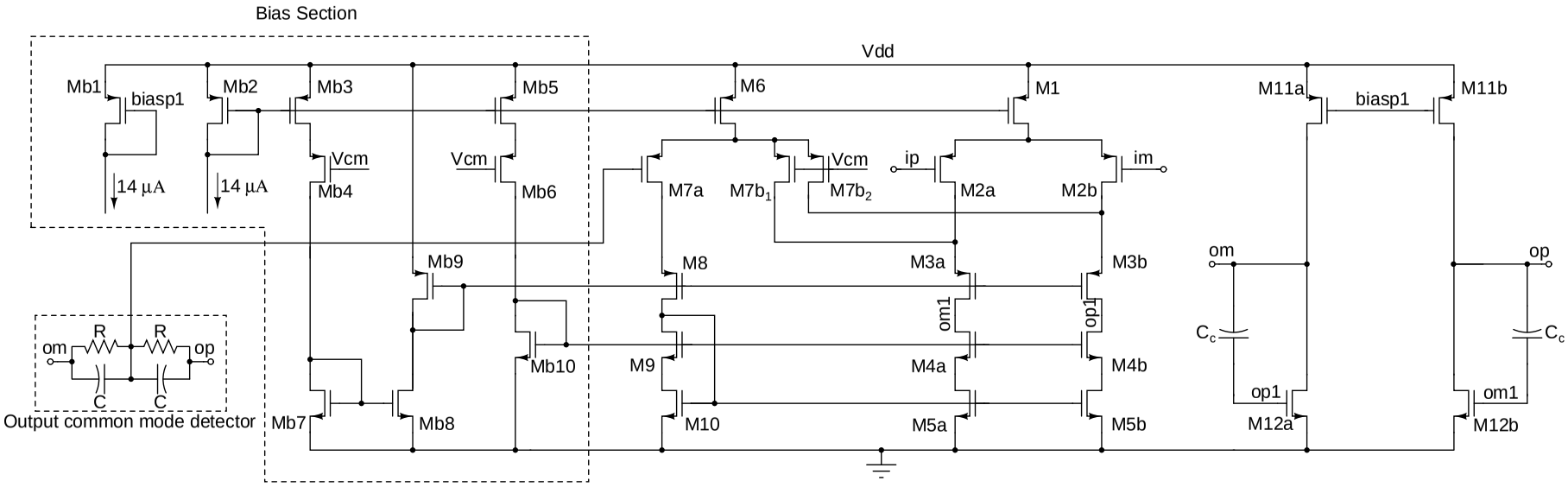


Figure 4.4: Common mode feedback loop of the Miller compensated opamp

The complete circuit diagram of the opamp with the sizes is shown in Fig. 4.5. The bias section of the opamp is also shown. The diode connected transistors Mb1 and Mb2 carry currents supplied from the fixed transconductance bias. Using a diode connected transistor helps in an easy layout and accurate biasing of transistors at the desired value of current.

4.2 Preliminary simulation results

Using the opamp design discussed in the previous section, a filter was implemented as a cascade of FOS, BQ1 and BQ2 sections as has been discussed in Chapter 2. In order to identify the contribution towards distortion from each section of the filter, IMD simulations were performed with only one section (either FOS or BQ1 or BQ2) implemented using transistor level circuitry and the other sections kept ideal. Fig. 4.6 shows the simulation results. It is seen that the contribution of distortion from the highest Q biquad (BQ2) is maximum. As BQ2 contributes to the high frequency part of the filter transfer function, it is affected the maximum



M1, M6 : 128 (0.5/0.18)	M7a, M8 : 8 (0.5/0.18)	M12 : 16 (0.5/0.18)	Mb4, Mb6 : 2 (0.5/0.18)	R = 100 kΩ
M2 : 8 (0.5/0.18)	M7b : 4 (0.5/0.18)	Mb1 : 4 (0.5/0.18)	Mb7, Mb8 : 2 (0.5/0.36)	C = 30 fF
M3 : 12 (0.5/0.18)	M9, M10 : 8 (0.5/0.36)	Mb2 : 32 (0.5/0.18)	Mb9 : 2 (0.24/0.9)	C_c = 120 fF
M4, M5 : 12 (0.5/0.36)	M11 : 32 (0.5/0.18)	Mb3, Mb5 : 16 (0.5/0.18)	Mb10 : 2 (0.24/1.6)	

Figure 4.5: Schematic of the Miller compensated opamp

near the filter bandedge, due to greater capacitive currents.

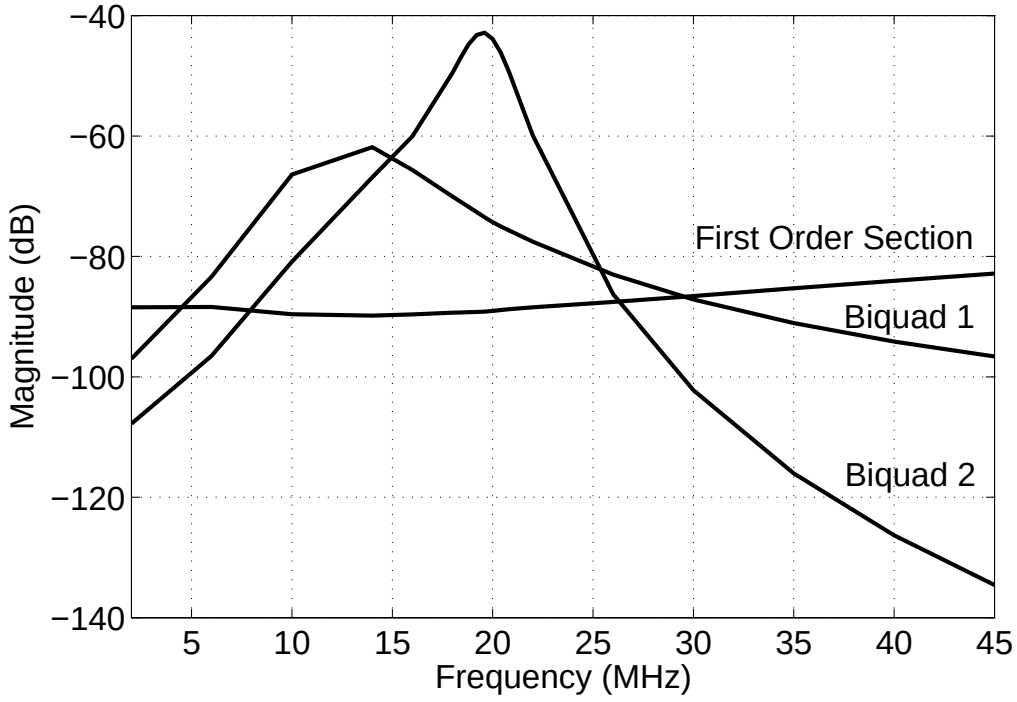


Figure 4.6: Contribution towards distortion from different sections of the filter with input differential amplitude 500 mV per tone

4.3 Current Injection circuit

The implementation of the current injection scheme in [7] mirrors the output stage of the opamp in the replica and injects the current into the output stage of the main opamp. The impedance matching between the main and replica opamps is achieved by adding a dummy output stage to the replica, biased at a dc voltage. For a given output bias current I and a fixed output swing (keeping the transistor overdrive the same), the transconductance achievable for the output stage MOSFET is one-half of what could have been achieved without using gain enhancement at all. This is because half the dc current $I/2$ is required for the current injection part. We now propose a new circuit technique that does not require the extra transconductor as in [7] and thus saves upto fifty percent power

in the second stage for the same specifications of the opamp.

From the circuit of the two stage opamp in Section 4.1.2, we notice that the current source at the output stage of the opamp is used only for biasing purposes. The idea therefore, is to utilize this current source in some possible manner. If we can implement the transconductor (used for injection) as part of this current source itself, the extra transconductor for injection will no longer be required. Hence, we design the opamps used in the replica opamp to be a flipped version of that in the main one. Fig. 4.7 shows the circuit implementation of the scheme. For the replica opamp, M9a, M9b forms the input transconductor stage. In the output stage, M13a, M13b serves as a constant current source and M14a, M14b implements the transconductor. For the main opamp, the input transconductor stage consists of M2a, M2b. The transconductor in the output stage is implemented by M6a, M6b whereas M7a, M7b forms the current source. Hence, in order to inject current into the main opamp, we modulate the PMOS current sources M7a, M7b using the voltage swings at the gate of M14a, M14b, in the replica opamp with the right phase. As the second stage in both the cases are just a flipped version of one another, with proper biasing, the bias voltages at the circuit nodes can be made nearly the same. Also, since the injection is carried out by varying the voltage at the gate of the MOSFETs, the replica can be a scaled version of the main opamp (in this case by a factor of two). By using this technique, no extra dc power is dissipated in biasing the injection transconductor and the output impedance matching of the main and replica opamps is exact.

The modified opamps used in the main and replica design are shown in Fig. 4.8 and 4.9. From Fig. 4.8, we notice that the transistors M11a and M11b at the output stage of the opamp are controlled by the bias section of the opamp when current injection is turned off. When the current injection is turned on, the gates of the transistors M11a and M11b are connected to the replica opamp shown in Fig. 4.9. The replica opamp is exactly identical to design of the main opamp, except the fact that it is impedance scale by a factor of two to save power.

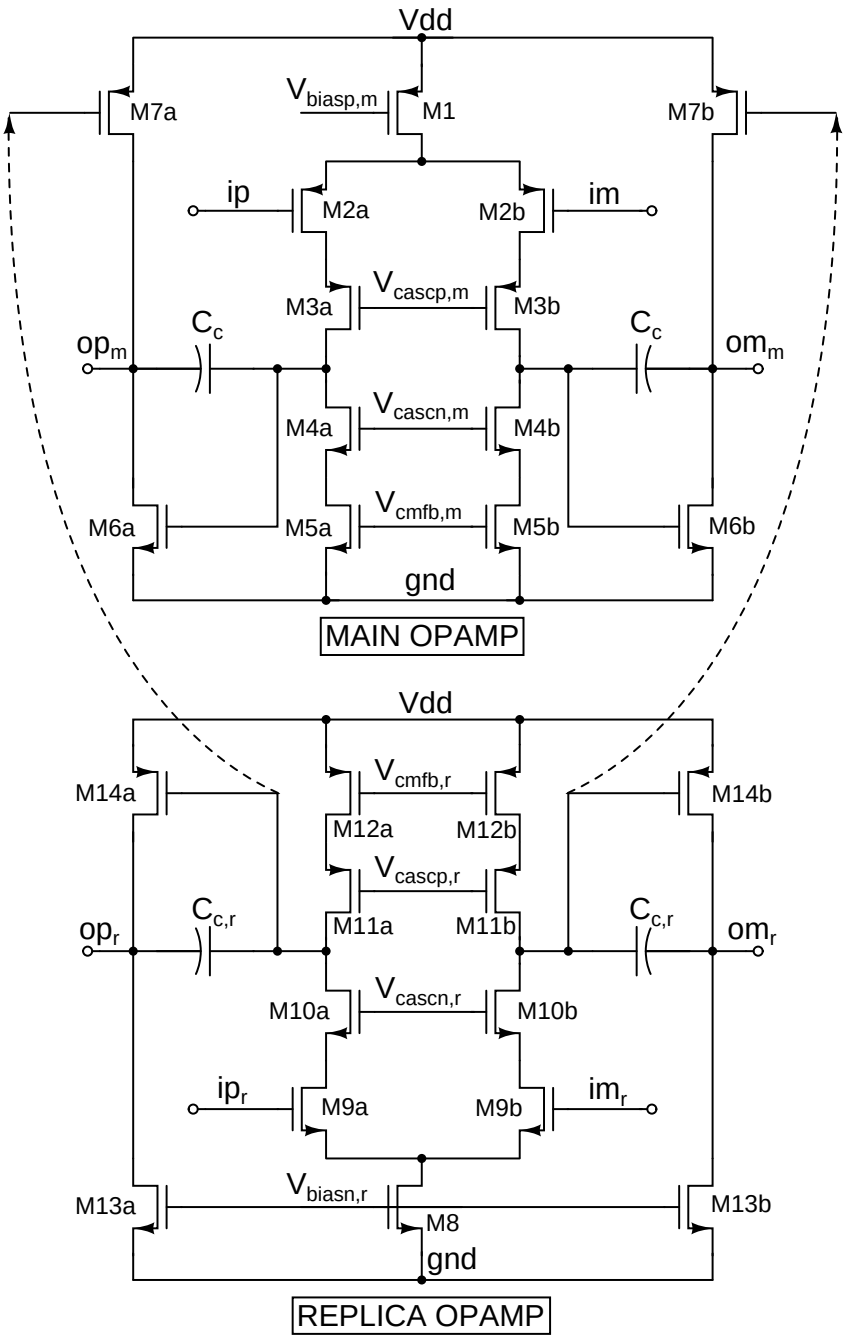
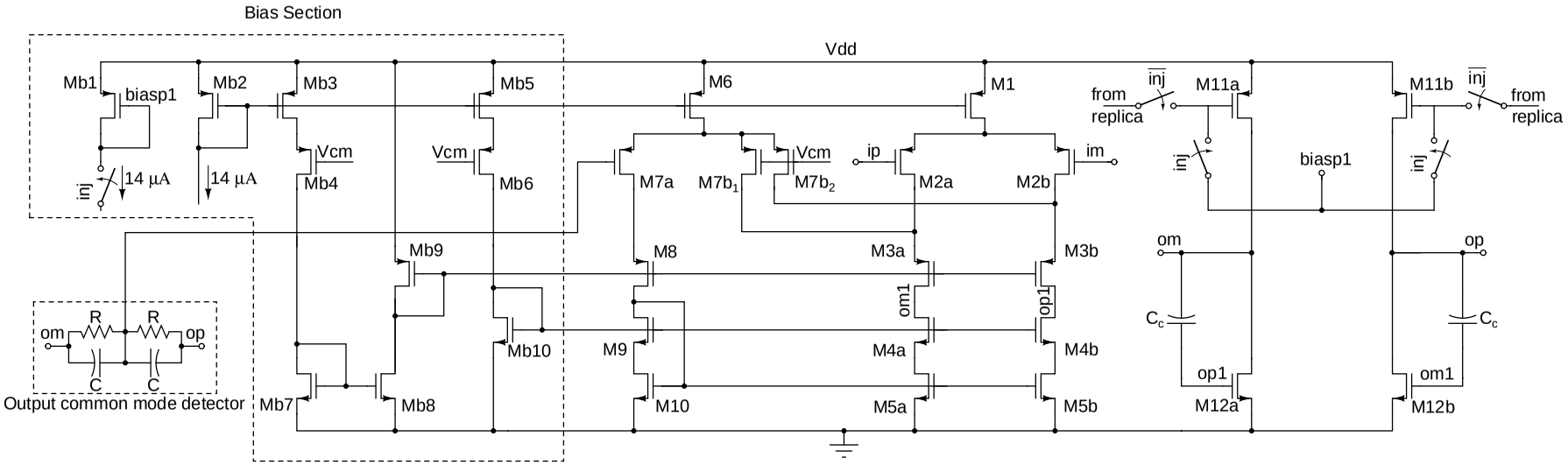
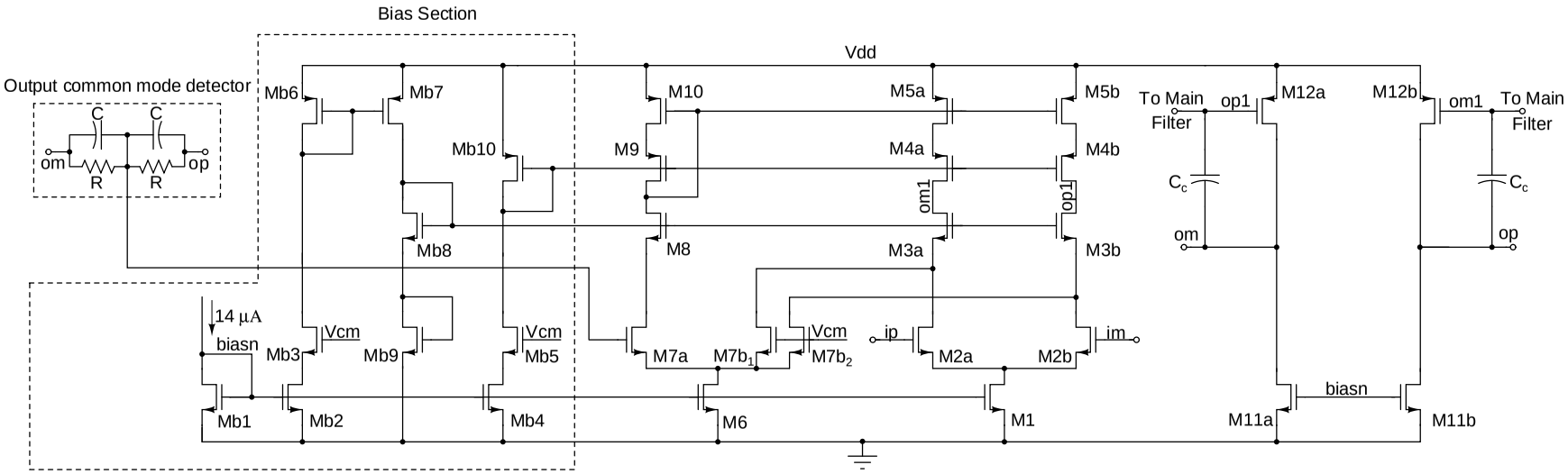


Figure 4.7: Circuit implementation of the current injection technique



M1, M6 : 128 (0.5/0.18)	M7a, M8 : 8 (0.5/0.18)	M12 : 16 (0.5/0.18)	Mb4, Mb6 : 2 (0.5/0.18)	R = 100 kΩ
M2 : 8 (0.5/0.18)	M7b : 4 (0.5/0.18)	Mb1 : 4 (0.5/0.18)	Mb7, Mb8 : 2 (0.5/0.36)	C = 30 fF
M3 : 12 (0.5/0.18)	M9, M10 : 8 (0.5/0.36)	Mb2 : 32 (0.5/0.18)	Mb9 : 2 (0.24/0.9)	C_c = 120 fF
M4, M5 : 12 (0.5/0.36)	M11 : 32 (0.5/0.18)	Mb3, Mb5 : 16 (0.5/0.18)	Mb10 : 2 (0.24/1.6)	Ms : 2 (0.5/0.18)

Figure 4.8: Schematic of the Miller compensated opamp in main BQ2



M1, M6 : 4 (0.5/0.18)	M7a, M8 : 4 (0.5/0.36)	M12 : 16 (0.5/0.18)	Mb6, Mb7 : 2 (0.5/0.18)	R = 200 kΩ
M2 : 4 (0.5/0.36)	M7b : 2 (0.5/0.36)	Mb1 : 2 (0.5/0.18)	Mb8 Mb9 : 2 (0.24/0.36)	C = 15 fF
M3 : 6 (0.5/0.36)	M9, M10 : 4 (0.5/0.18)	Mb2, Mb4 : 1 (0.5/0.18)	Mb10 : 2 (0.24/0.5)	C_c = 60 fF
M4, M5 : 6 (0.5/0.18)	M11 : 8 (0.5/0.18)	Mb3, Mb5 : 2 (0.5/0.36)		

Figure 4.9: Schematic of the Miller compensated opamp in replica BQ2

4.4 Filter Implementation

From the distortion analysis, we observe that the contribution of distortion from BQ2 in the main filter is maximum. The contributions from the FOS and BQ1 are relatively very small compared to that of BQ2. Hence, in this design we carry out current compensation for BQ2 alone. The compensation of BQ2 would require another replica filter to estimate the nominal values of current needed to be injected. Instead of using a replica filter, a replica BQ2 driven by BQ1 of the main filter is used. Since the distortion of BQ1 is relatively small, this doesnot affect the output distortion of the filter. This results in a block level implementation of the technique as shown in Fig. 4.10. The filter has a manual control which allows injection to be turned on/off. A one-bit manual capacitive tuning which accounts for 15% RC variation is incorporated in the design of the filter.

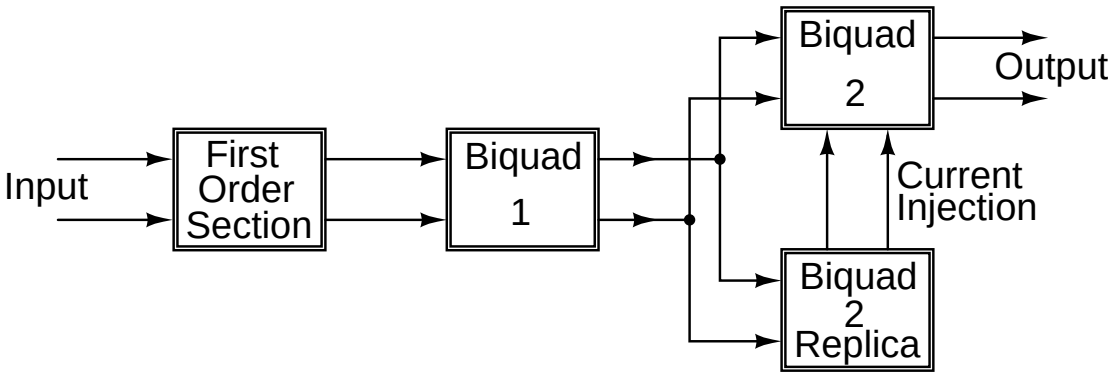


Figure 4.10: Block diagram of the filter

The complete filter including the replica biquad with the resistor and capacitor values are shown in Fig. 4.11 and 4.12. The opamps in the replica and main biquad are implemented as discussed before. The replica biquad is impedance scaled by a factor of two.

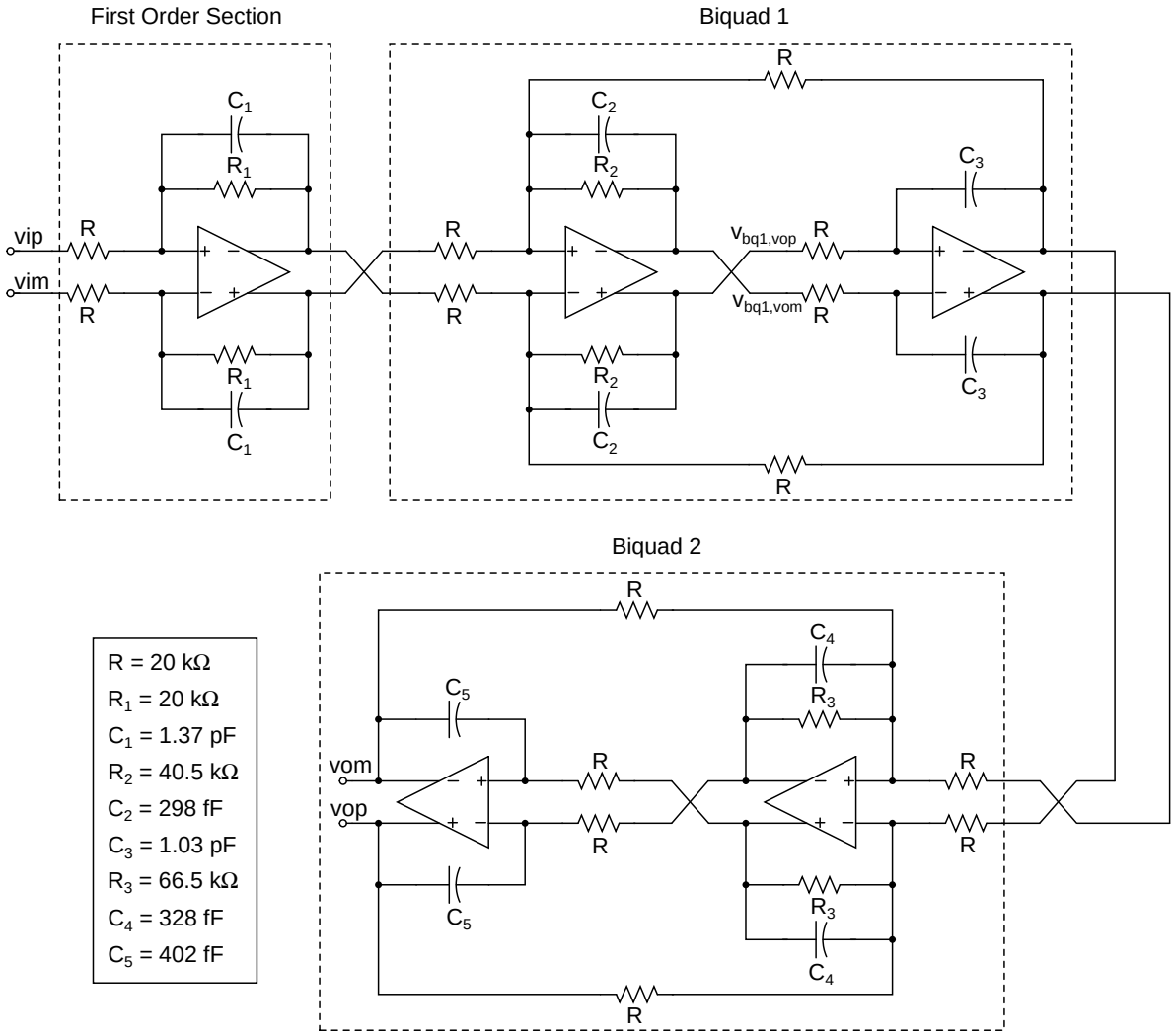


Figure 4.11: Circuit schematic of the filter showing the FOS, BQ1 and BQ2 sections

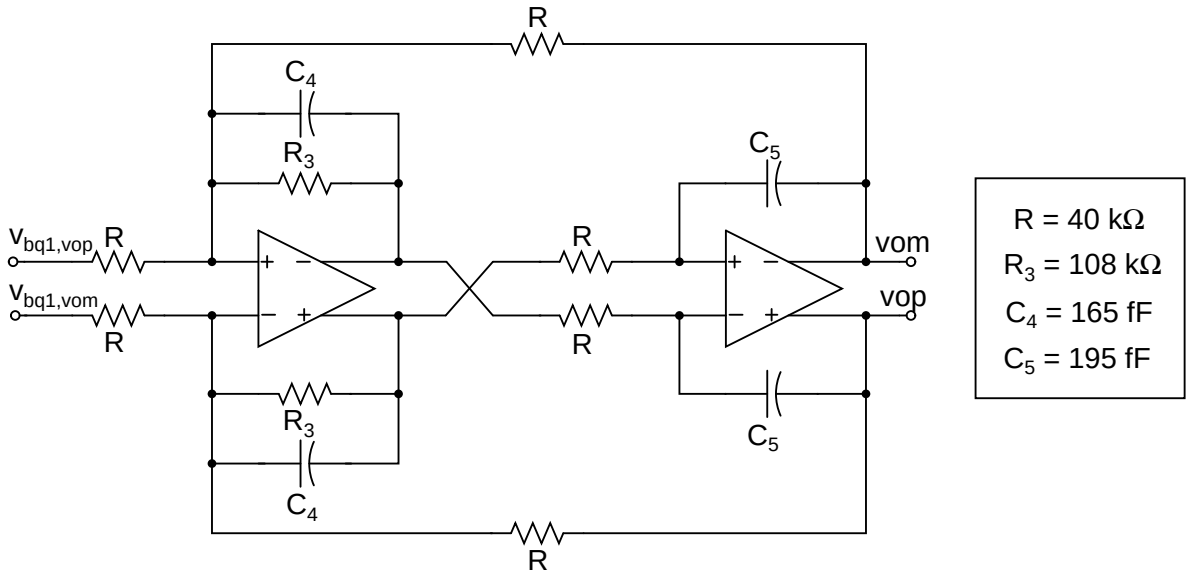


Figure 4.12: Circuit schematic of the replica BQ2

4.5 Fixed Transconductance Bias

In order to stabilize the design over process, temperature and power supply variations, a fixed transconductance bias circuit is required. The fixed transconductance bias used in this work is based on the design proposed in [11]. The circuit diagram is shown in Fig. 4.15.

The devices whose transconductance needs to be fixed are M2a and M2b. In steady state, the feedback in the circuit ensures that the currents in M9 and M10 are equal. This gives

$$2I + I_1 - i_1 = 2I - i_2 \tag{4.1}$$

$$i_1 - i_2 = I_1 \tag{4.2}$$

The differential current $i_1 - i_2$ due to a small incremental voltage $I_1 R$ is given

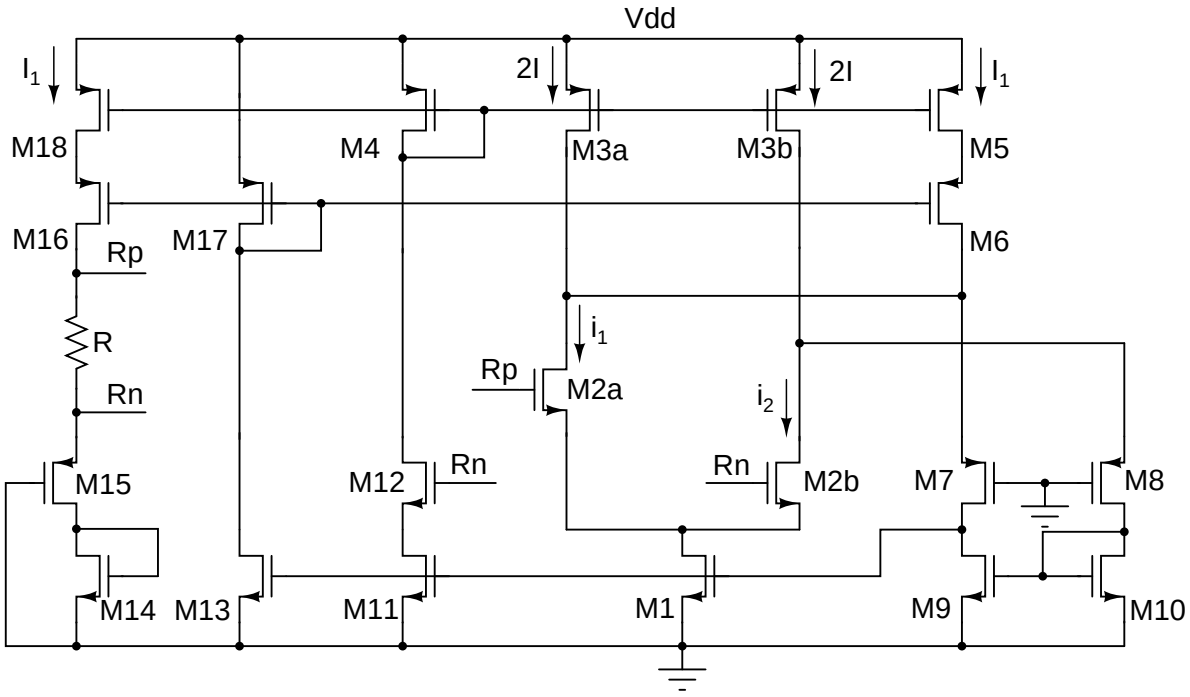


Figure 4.13: Fixed-Gm Bias circuit

by the relation

$$i_1 - i_2 = g_{m,M2}.I_1R \tag{4.3}$$

Substituting (4.2) in (4.3), we have

$$g_{m,M2} = \frac{1}{R} \tag{4.4}$$

The resistance R is determine by a stable off chip resistor. Hence, with process and temperature the variation in the transconductance of the transistors is minimized. This design is robust in various aspects namely

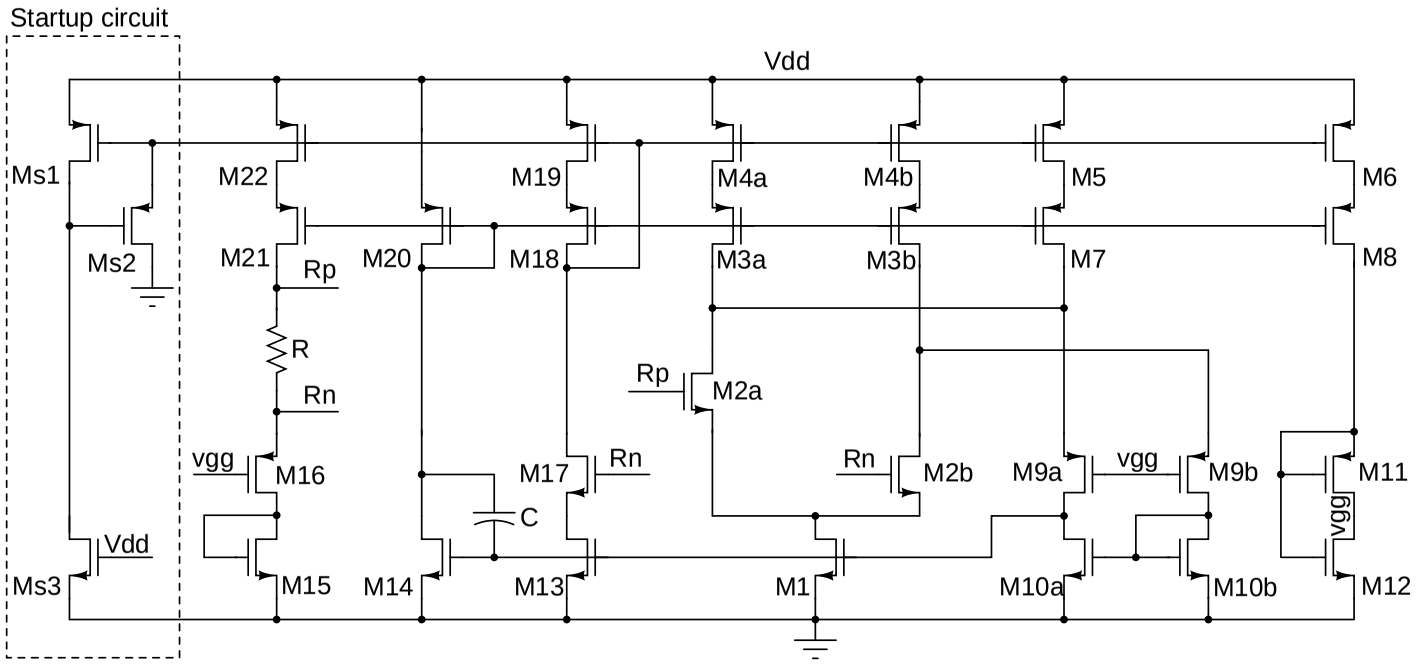
1. It is not dependent on the MOSFET square law compared to conventional techniques.
2. It is independent of power supply voltage and temperature variations.
3. It is not affected by the output impedance of the transistors and back-gate effect.

The design details of the fixed transconductance bias used in this design is shown in Fig. 4.14. In this design, the bias currents are modified so that $g_{m,M2} = \frac{2}{R}$. Simulation results are shown in Fig. 4.15. The variation of transconductance value with process and temperature is less than 2.5% of the average value.

4.6 Bias distribution

The fixed transconductance bias circuit discussed in the previous section is used to servo the transconductance of all the transistors in the filter to an external stable resistor. This is done by biasing all the transistors in the opamps to the biasing current I_{bias} of the fixed transconductance bias circuit. Fig. 4.16 shows the basic block of the bias distribution.

Typically, the bias network is implemented along with the fixed transconductance bias. The replicated bias currents are then distributed to the various opamps in the filter. In order to accurately replicate this biasing current in the local bias network of each opamp, cascode transistors will have to be used to avoid errors due to finite output impedance of the current sources. This results in designs which are difficult to layout. In this implementation, the transistors M3, M4, M5, M6 form a feedback loop. The loop ensures that the current in M3 is equal to I_{bias}. If the current in M5 is I_x and this current is fed into a transistor in the opamp with the same current density as M5, then with the appropriate mirroring, the current I_{bias} can be reproduced. The advantage with this method is that the layout is now much more easier and no other extra current source/transistors are required as in the case of using a cascode current source. The Capacitor C in the design is used to stabilize the feedback loop. The complete bias distribution network with the transistor size is shown in Fig. 4.17. The current I_{bias} is distributed to the filter and the three test buffers.



M1 : 8 (0.5/0.18)	M6, M8 : 4 (0.5/0.18)	M12 : 2 (0.25/0.18)	M18, M19, Ms1, Ms2 : 8 (0.5/0.18)
M2 : 8 (0.5/0.36)	M9 : 28 (0.5/0.18)	M13, M14 : 2 (0.5/0.18)	M20 : 2 (0.5/0.36)
M3, M4 : 32 (0.5/0.18)	M10 : 14 (0.25/0.18)	M15 : 12 (0.25/0.18)	Ms3 : 1 (0.24/12)
M5, M7, M21, M22 : 24 (0.5/0.18)	M11 : 2 (0.5/0.36)	M16 : 24 (0.5/0.18)	
R = 3.2 kΩ	C = 3 pF	M17 : 4 (0.5/0.36)	

Figure 4.14: Fixed-Gm Bias circuit used in the filter design

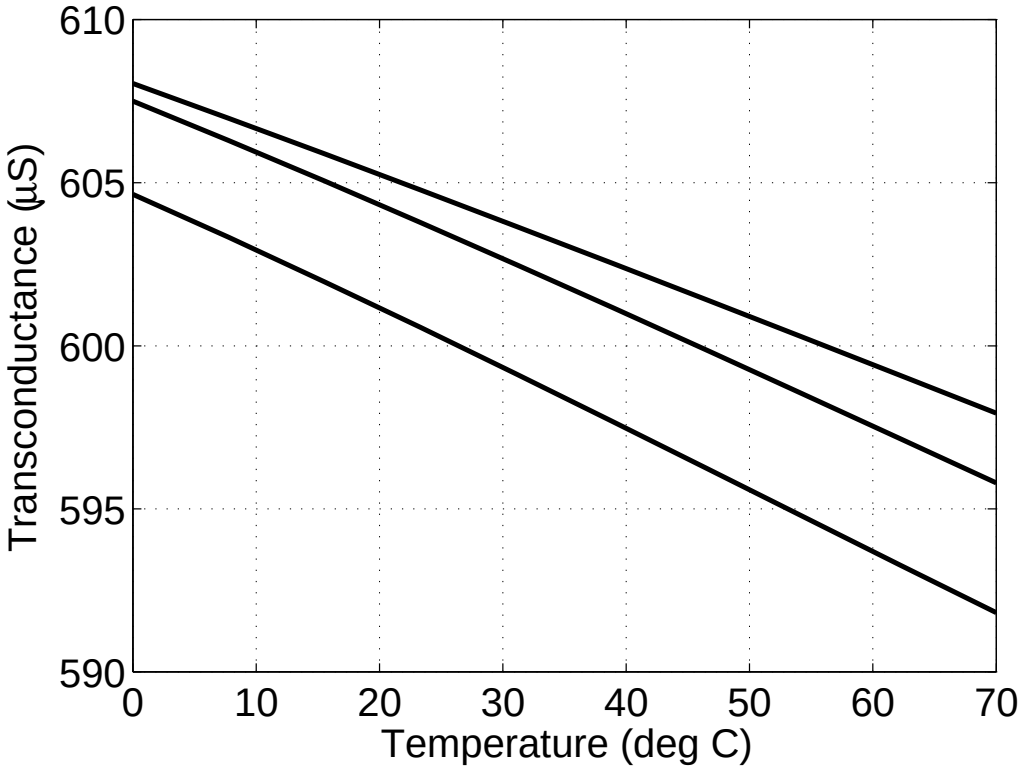


Figure 4.15: Variation of transconductance with process and temperature

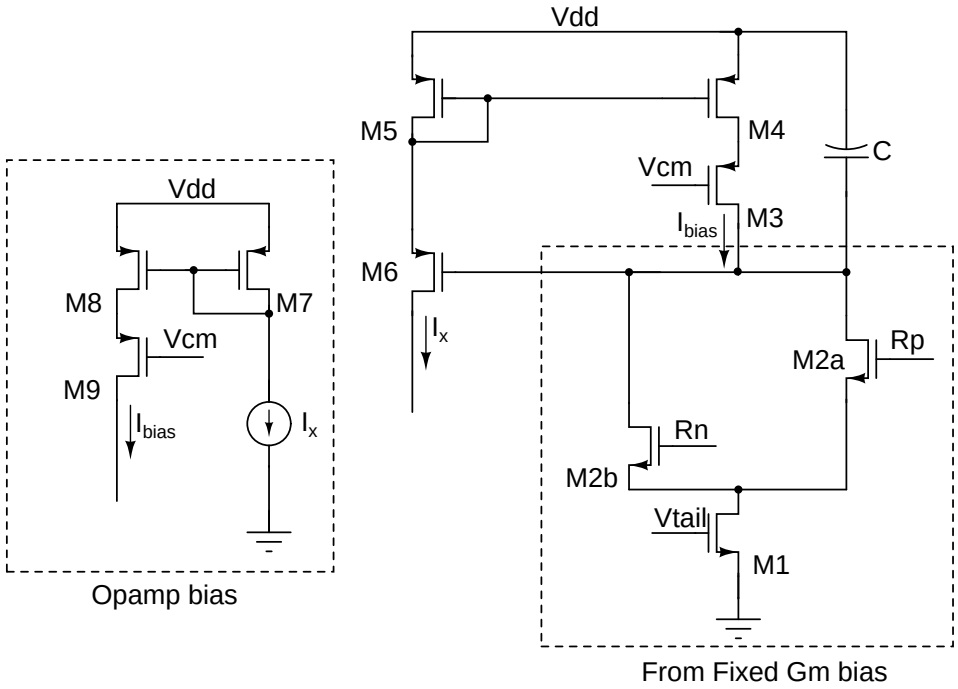
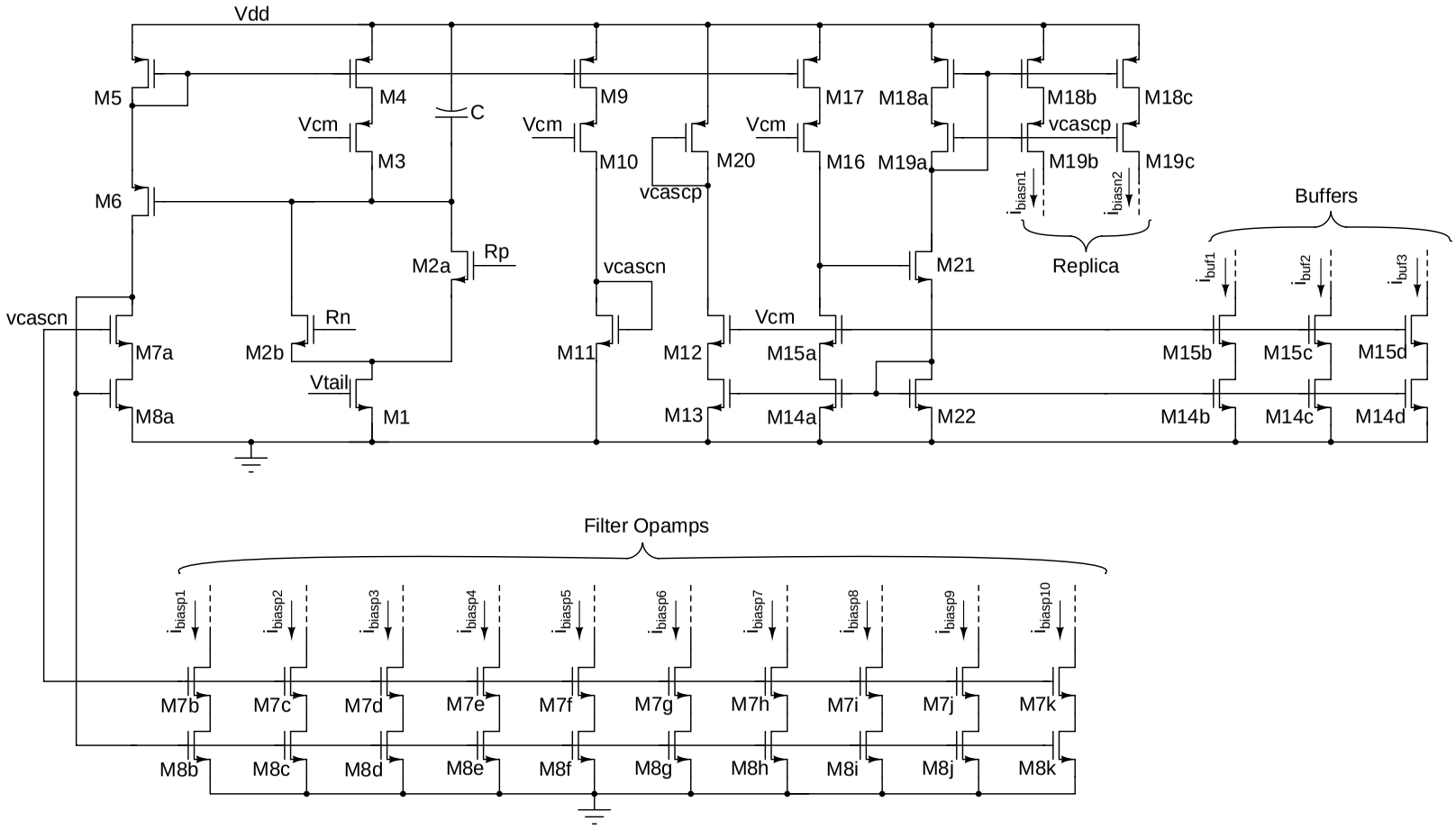


Figure 4.16: Basic block of bias distribution



M1 : 2 (0.5/0.18)	M7, M8, M10 : 2 (0.5/0.18)	M13 : 1 (0.5/0.18)	M17, M18 : 32 (0.5/0.18)
M2 : 2 (0.5/0.36)	M9 : 16 (0.5/0.18)	M14, M22 : 2 (0.5/0.18)	M20 : 1 (0.24/0.18)
M3 : 4 (0.5/0.18)	M11 : 1 (0.24/1.6)	M15, M21 : 4 (0.5/0.36)	C = 100 fF
M4, M5, M6 : 32 (0.5/0.18)	M12 : 2 (0.5/0.36)	M16, M19 : 4 (0.5/0.18)	

Figure 4.17: Bias distribution

4.7 Buffer Design

The filters discussed above are used in practice as part of a larger design and donot act as stand alone devices. In general, the filter is not designed to drive the huge capacitive loads offered by the package. In order to accurately characterize the filter, buffers are used to drive the package capacitances, thus preventing any loading of the filter. On the whole, three buffers have been used in the design of the chip. One buffer is used to measure the direct path transfer function. The other two buffers are driven by the output of the main and the replica filter. The outputs of these three buffers are multiplexed together.

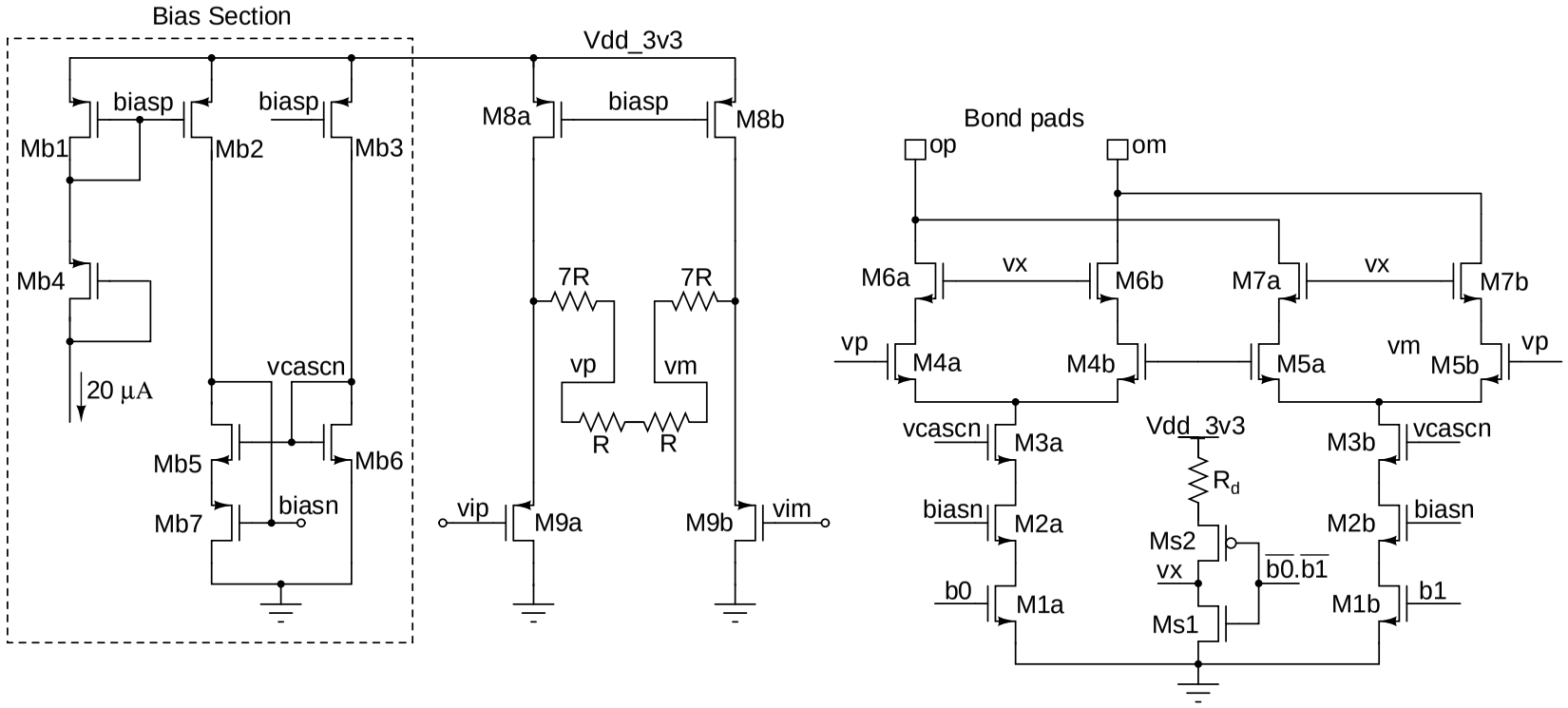
The design of the buffer is similar to the Active-RC filter discussed in [12]. The circuit schematic of the buffer is shown in Fig. 4.18. The buffer consists of a two simple transconductors implemented as a differential pair. In order to accurately characterize the filter, the gain of buffer can be negated using a switch control. Transistor M4 and M5 form the input positive and negative paths of the buffer respectively. An output current proportional to the voltage generated by the filter is achieved using this transconductor stage. M6 and M7 act as cascode transistors to enhance the output impedance of the transconductor. The drains of M6 and M7 are connected in opposite fashion, thus allowing the gain to be either ± 1. Transistor M2 and M3 act as cascode current sources. M1a and M1b act as switches to turn on/off either of the transconductor. The cascode transistors M6 and M7 are controlled using digital logic and pulled to logic level 0 when both the paths are off. When either of the paths are on, the cascode node is pulled to the supply rail of 3.3 V. Resistor R_d acts as a damping resistor for possible oscillations with the inductance due to the bond wires.

The design of the buffer must be such that the distortion generated by it must be much lesser than that of the filter. Hence, the transconductance of M4 and M5 must be as linear as possible. This can be achieved by using a 3.3 V supply, by reducing the voltage applied to the gates of M4 and M5 and by increasing their overdrives. This results in large sizes for these transistors. In order to prevent

loading effects on the filter due to this, the transconductors are driven using a common drain amplifier stage. The source follower stage is implemented using a PMOS input stage M9 with its bulk tied to the source and an active load M8. The output of the filter is given as input to M9a and M9b. An attenuation by a factor of eight is introduced between the source follower and the transconductance stage, to increase the buffer linearity. Transistors Mb1-Mb6 act as the local bias circuitry for the buffer. The current for the buffer is supplied by the bias distribution block.

4.8 Filter Layout

The layout of the filter is shown in Fig. 4.19. The filter core consists of the FOS, BQ1 and BQ2 sections in cascade. The bias block consists of the Fixed transconductance bias and the bias distribution section. The three buffers used in the chip are also shown. Fig. 4.20 shows the bonding diagram of the chip.



M1-M3 : 40 (2/0.34)	M8 : 32 (2/0.34)	Mb2, Mb3 : 8 (2/0.34)	R = 20 kΩ
M4-M5 : 4 (0.24/0.34)	M9 : 4 (0.5/0.34)	Mb5, Mb7 : 2 (2/0.34)	R_d = 110 Ω
M6-M7 : 16 (0.5/0.34)	Mb1, Mb4 : 16 (2/0.34)	Mb6 : 2 (0.5/0.78)	

Figure 4.18: Circuit implementation of the buffer

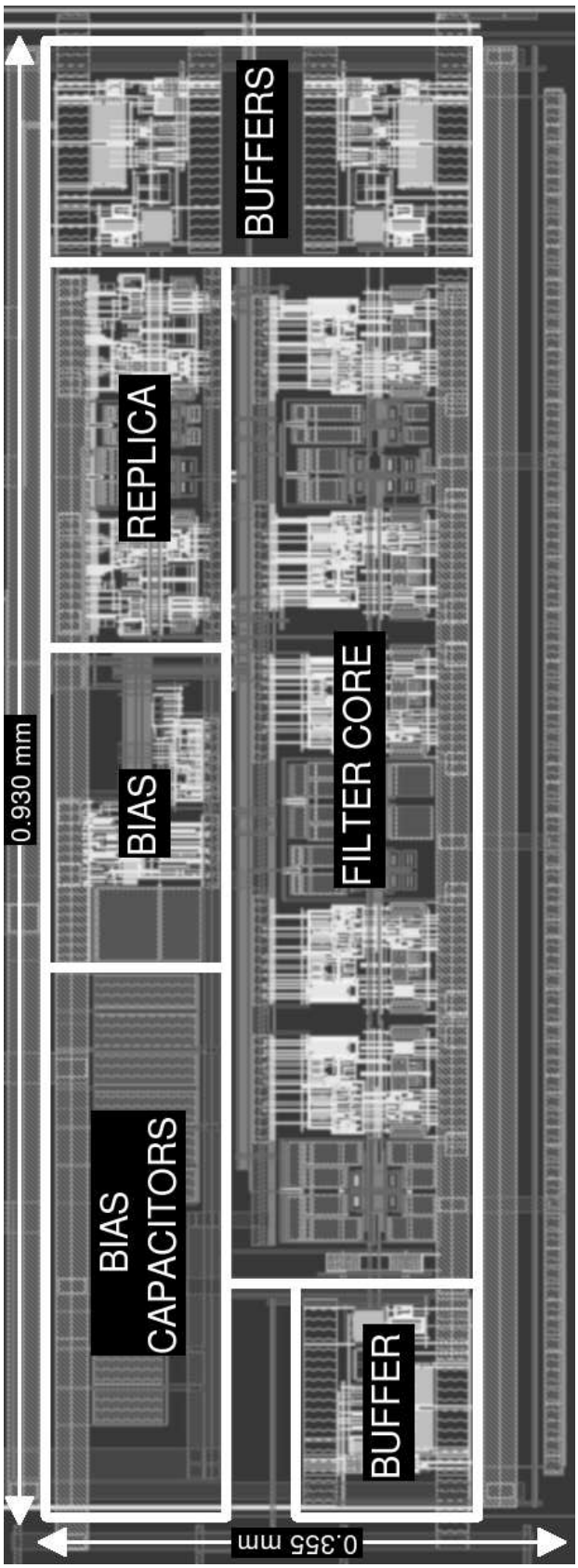


Figure 4.19: Layout of the designed filter

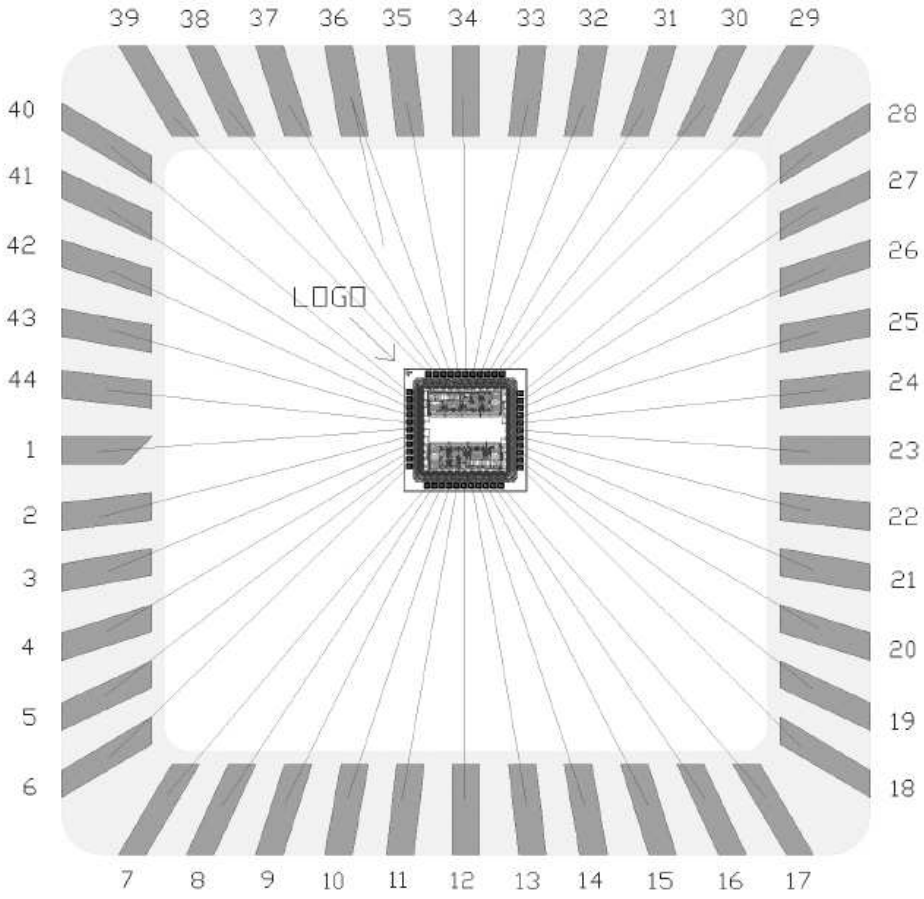


Figure 4.20: Bonding diagram of the designed filter

CHAPTER 5

Macromodel simulations and Design simulation results

5.1 Macromodel simulations

In order to understand distortion and the working of the injection technique, we carry out macromodel simulations of the designed filter. The two-stage Miller compensated opamp designed in 4 is modeled using two transconductors in cascade, with the Miller capacitor connected across the input and output of the second transconductor. The output capacitance and conductance values were obtained from the dc operating point of the actual opamp. In order to model the distortion of the opamp, the maximum current and transconductance value of each transconductor is obtained from the operating points and the non-linearity in each of them is incorporated. The model used for the transconductor is the same as discussed in (3.1). The model of the opamp is shown in Fig. 5.1.

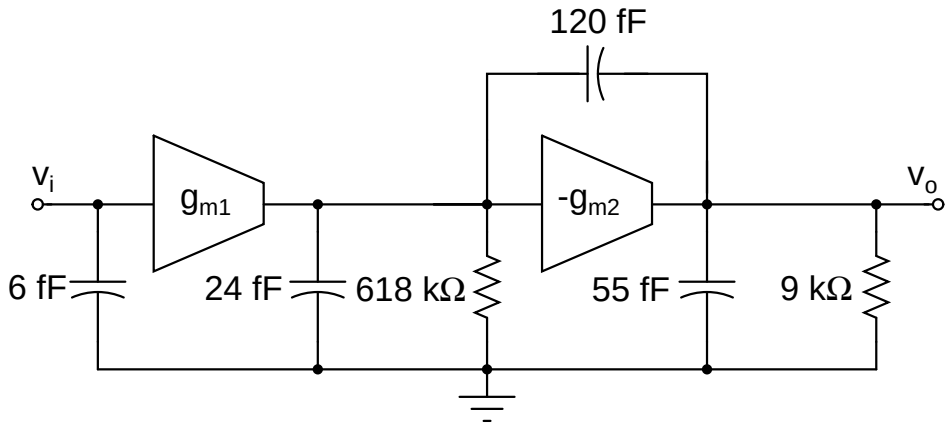


Figure 5.1: Model of the designed two-stage Miller compensated opamp. $g_{m1} = 255\,\mu\text{S}, I_{max1} = 31.67\,\mu\text{A}, g_{m2} = 1.524\,\text{mS}, I_{max2} = 163\,\mu\text{A}$

Fig. 5.2 shows the actual opamp response and the response of the model used for macromodel simulations.

We now discuss the macromodel simulations carried out for a fifth order Chebyshev filter of bandedge 20 MHz with a passband ripple of 1 dB. The filter is implemented as a cascade of FOS, BQ1 and BQ2 sections. The two-stage opamps used in the filter are modeled as above, as a cascade of two transconductors. Since in the main design, only the BQ2 is compensated, we keep the FOS and BQ1 sections ideal and compensate only for BQ2. The two opamps in BQ2 are compensated at the output using ideal current controlled current sources. IMD simulations with input differential amplitude of 500 mV per tone, is carried out for different cases as given below. The transconductors in each of the opamps is referred here. The cases considered are

1. Both transconductors non-linear - without and with injection
2. Second transconductor alone non-linear - without and with injection
3. First transconductor alone non-linear - without and with injection
4. First transconductor alone non-linear and second transconductor linear with high transconductance - without injection

Fig. 5.4 shows the IMD plots of the filter. Since we are more interested in the distortion near the bandedge we look at the magnified version of the plot shown in Fig. 5.1. Table 5.1 gives the IMD values near the bandedge.

Table 5.1: IMD values for macromodel simulations near bandedge

Simulation	Without Injection (dB)	With Injection (dB)
g_{m1}, g_{m2} non-linear	-39.79	-49.75
g_{m1} non-linear	-44.05	-48.79
g_{m2} non-linear	-48.79	-63.17
g_{m1} non-linear, high g_{m2}	-48	–

For case (1), with both transconductors non-linear, current injection at the output of the opamp results in improvement in distortion. In case (2), the improvement in distortion is considerably high. This is because the second transconductor is the only source of distortion in the filter and we are compensating for

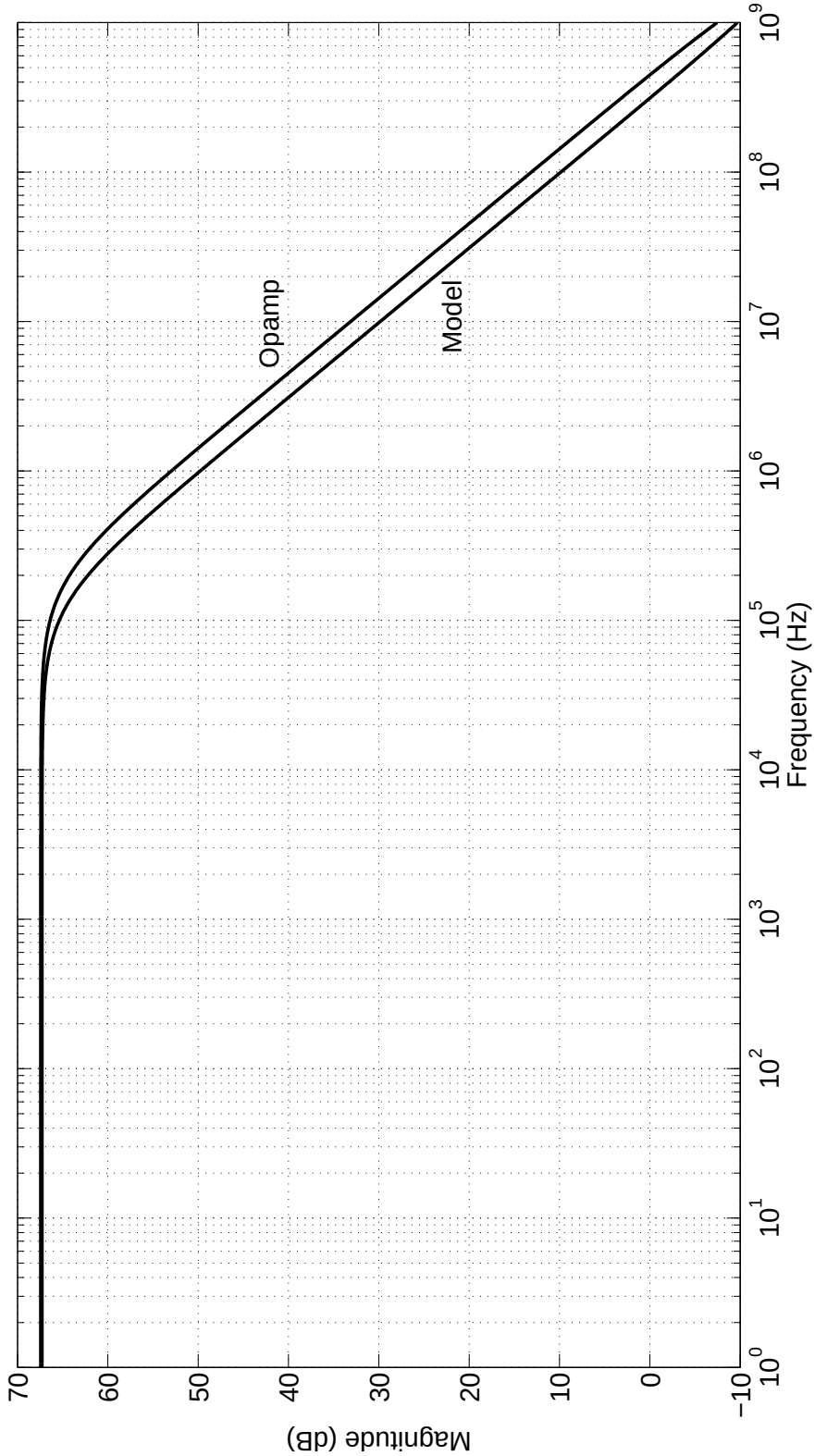


Figure 5.2: Comparison of Actual and Model response

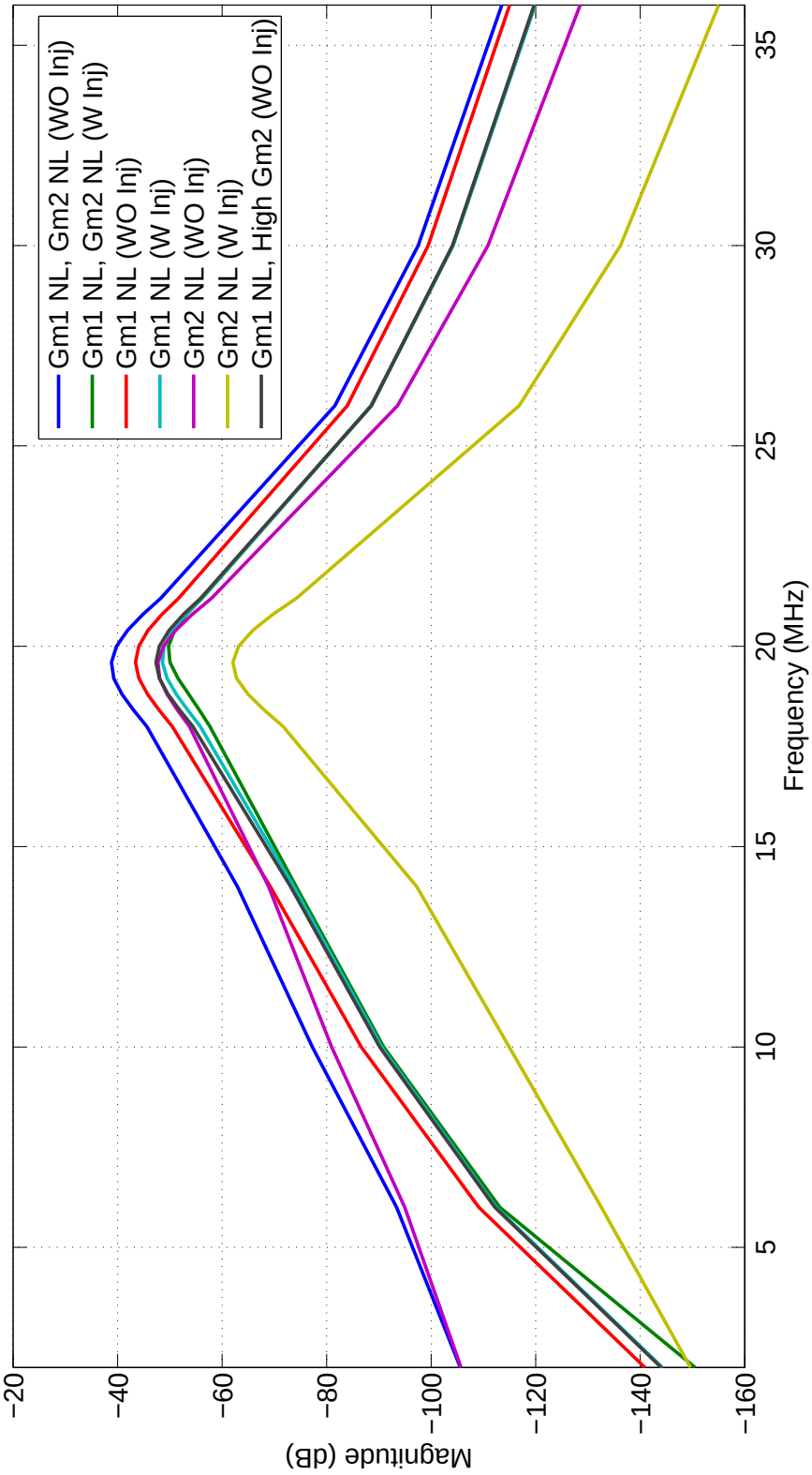


Figure 5.3: IMD plots for Macromodel simulations.

it by current injection. In the distortion analysis of the two-stage opamp, we observed that current injection at the output of the opamp must not only reduce the second stage distortion but also reduce the contribution of distortion from the first stage. This was evident from (3.8), (3.9) and (3.11). In case (3) the first transconductor alone is non-linear. With current injection, the swing at the input of the second transconductor reduces, which in turn reduces the compensating current supplied by the first stage. Thus, we see a reduction in the distortion even when the second stage non-linearity is not considered. This confirms the proposed theory. This fact is further confirmed by simulation results in case (4). By deliberately increasing the transconductance g_{m2}, we reduce the swing at the input of the second stage. We observe that as g_{m2} increases, the distortion curve in this case tends towards that of case (3) with injection, confirming the analytical calculations.

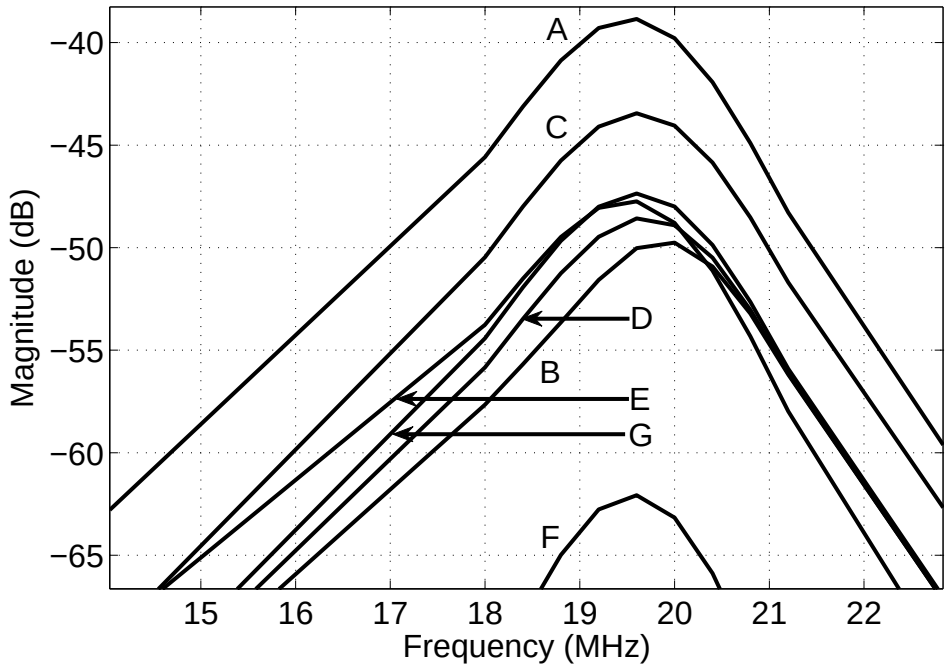


Figure 5.4: IMD plots for Macromodel simulations near bandedge. (A) g_{m1}, g_{m2} non-linear, without injection. (B) g_{m1}, g_{m2} non-linear, with injection. (C) g_{m1} alone non-linear, without injection. (D) g_{m1} alone non-linear, with injection. (E) g_{m2} alone non-linear, without injection. (F) g_{m2} alone non-linear, with injection. (G) g_{m1} alone non-linear, higher value of g_{m2}.

5.2 Design simulation results

A fifth order Chebyshev Active RC filter with a passband ripple of 1 dB and a bandedge of 20 MHz was implemented in a 0.18 μm CMOS process. The chip occupies an area of 0.33 mm^2.

5.2.1 Frequency Response

The simulated frequency response of the filter without/with current injection is shown in Fig. 5.5. The bandedge of the filter is 20 MHz. We observe peaking in the frequency reponse when the current injection is removed. This is because with current injection, the opamps in the filter tend towards ideal behaviour and the Q enhancement reduces.

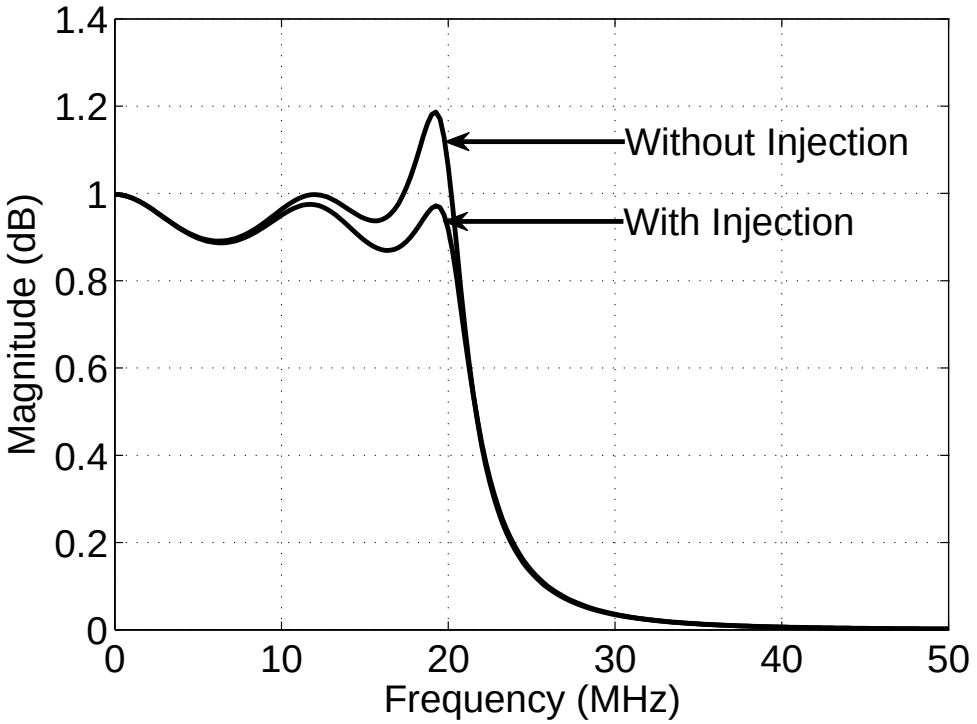


Figure 5.5: Simulated Frequency Response without/with current injection

5.2.2 Noise

Fig. 5.6 shows the simulated thermal output noise spectral density of the filter without/with current injection. We see that the noise without/with current injection are almost the same. The noise of the filter due to current injection is less than that without injection due to slight difference in the frequency response. The simulated thermal output noise of the filter without current injection is 1.286 Vrms and that with current injection is 1.262 Vrms.

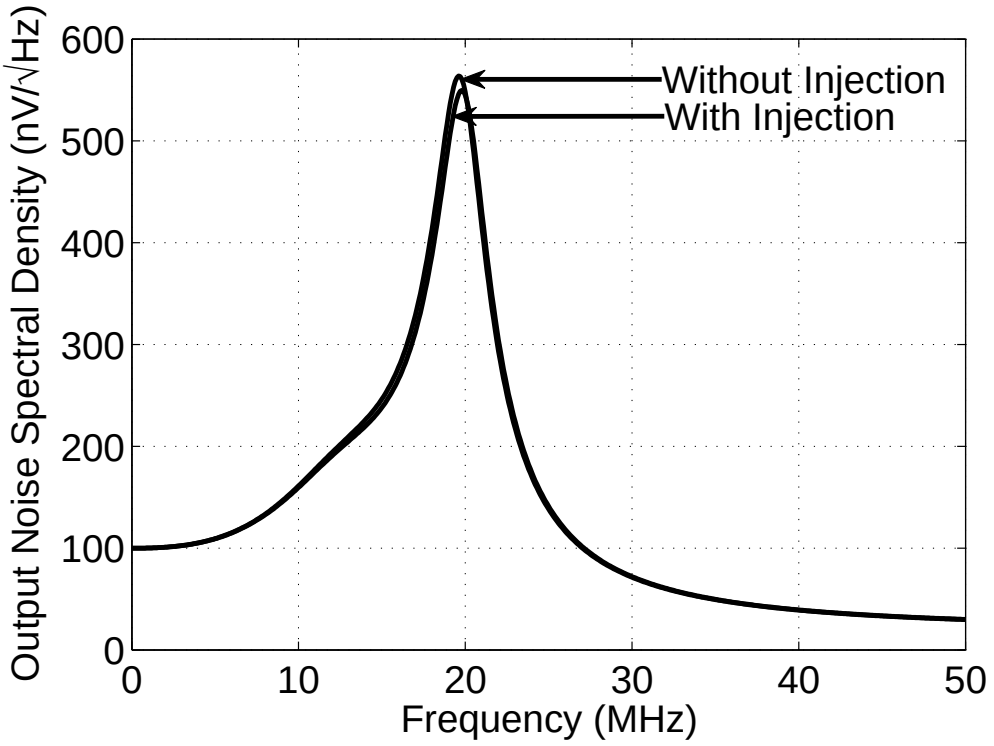


Figure 5.6: Simulated Thermal Output Noise Spectral density

5.2.3 Distortion

The distortion of the filter was simulated using IMD measurements. Two tones at $f_0 - 0.2$ MHz and $f_0 + 0.2$ MHz were given as input and f_0 was varied. Fig. 5.7 shows the IMD simulation for an input differential amplitude of 375 mV per tone. From the plots, we observe that the improvement near the filter bandedge due

to current compensation is significant. The improvement is around 12 dB at the point of maximum distortion.

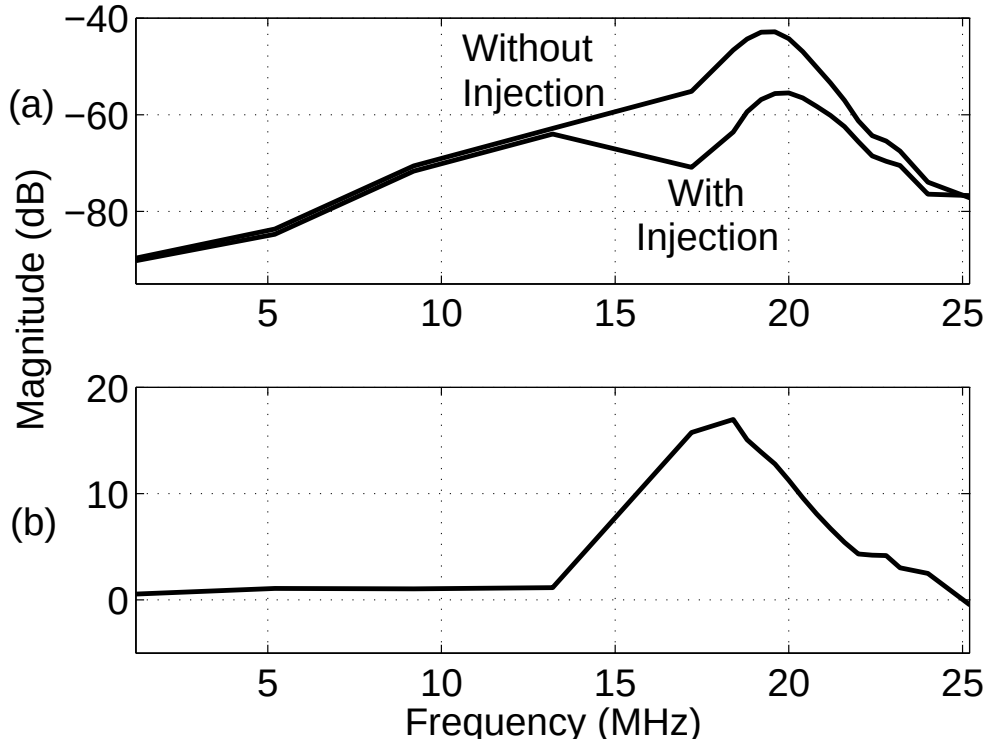


Figure 5.7: (a) IMD as a function of frequency for input differential amplitude 400 mV per tone (b) Improvement in IMD

CHAPTER 6

Measurement Techniques, Design of Testboard and Experimental Results

6.1 Measurement Techniques

In this section, we discuss techniques to accurately characterize the filter. These include the measurement of the filter's frequency response, noise and distortion. The accurate measurement of the filter characteristics has been discussed in great detail in [12]. For the measurement of frequency response, the characterization technique takes into account the spurious coupling through the package and the stop band measurement is two orders of magnitude better compared to conventional techniques.

6.1.1 Frequency Response

We state the method of frequency response technique discussed in [12], [13]. Fig. 6.1 shows the signal flow graph considering package and board feedthrough. The feedthrough coefficients k_1, k_2, k_3 are assumed to be symmetric with the output and input ports. Here, H_b is the response of the buffer and H_f the response of the filter. There are two paths used for measurement, one through the filter and buffer i.e. the filter path $V_{o,fil}$ and the other through the buffer alone i.e. buffer path $V_{o,dir}$.

Solving the signal flow graph and quoting the results from [13], we get

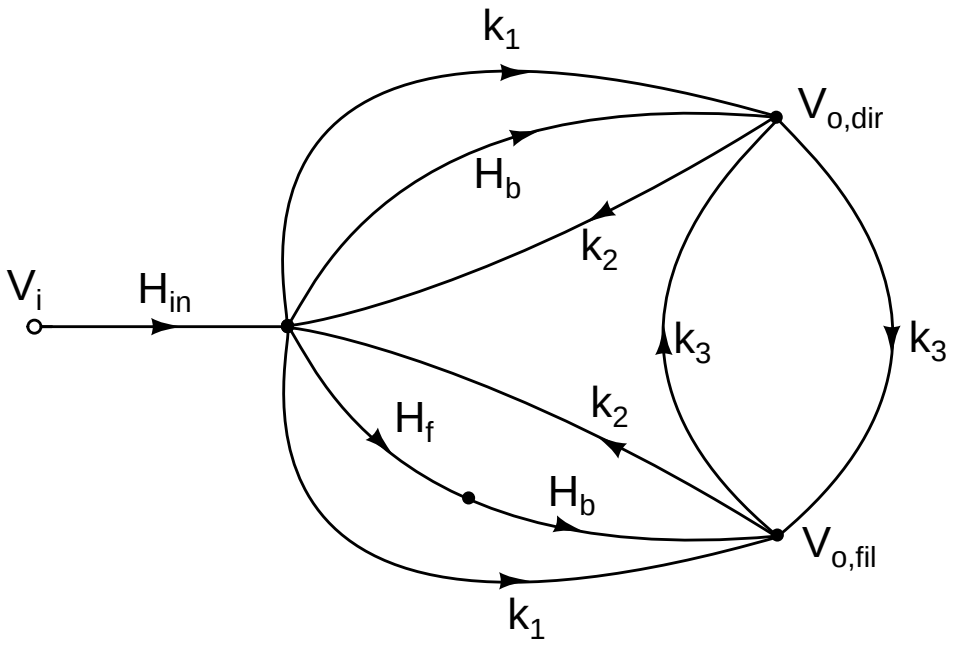


Figure 6.1: Signal flow graph consider package feedthrough

$$\frac{V_{o,fil}(f)}{V_i(f)} \approx H_{in}H_fH_b + k_1H_{in} + k_3H_{in}H_b + k_2(H_{in}{H_b}^2{H_f}^2 + H_{in}{H_b}^2H_f) \tag{6.1}$$

$$\frac{V_{o,dir}(f)}{V_i(f)} \approx H_{in}H_b + k_1H_{in} + k_3H_{in}H_fH_b + k_2(H_{in}{H_b}^2 + H_{in}{H_b}^2H_f) \tag{6.2}$$

The on chip measurement setup for the filter is shown in Fig. 6.2. The buffers have a gain control, which allows the gain to be either 0 or ± 1. Hence, referring back to (6.1), we measure the filter path by setting the gain to $+1$ ($H_{fil,p}$) and then to -1 ($H_{fil,n}$). Subtracting these two measurements and neglecting k_2, we

get

$$H_{fil,p} - H_{fil,n} \approx 2H_{in}H_fH_b \tag{6.3}$$

When we do the same for the buffer path, from (6.2) we get

$$H_{buf,p} - H_{buf,n} \approx 2H_{in}H_b \tag{6.4}$$

Dividing the results in (6.3) and (6.4), we can accurately calculate H_f. The measurement of frequency response is done using the Vector Network Analyzer (VNA) using the S parameters.

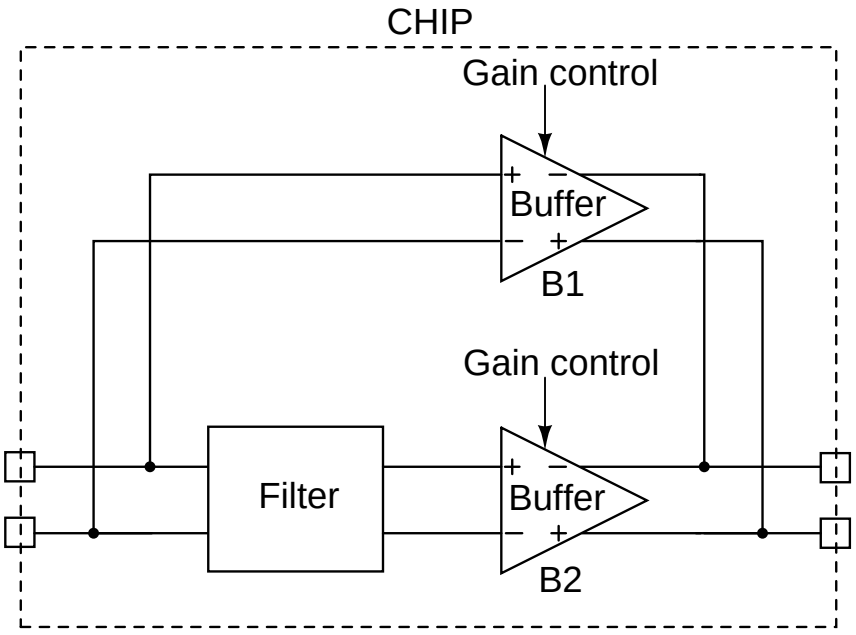


Figure 6.2: On chip measurement setup for the filter

6.1.2 Noise

The measurement of noise is done using a Spectrum Analyzer by turning off the inputs to the testboard. In order to measure the output noise of the filter, the noise contributions from the buffer and amplifiers must be subtracted to give accurate

results. The errors due to package response must also be taken into account. We now propose two methods to determine the output noise of the filter.

Method 1

We consider the block diagram shown in Fig. 6.3. The measured output noise comprises of noise contributions from the input stage, the filter, the buffers and the amplifier.

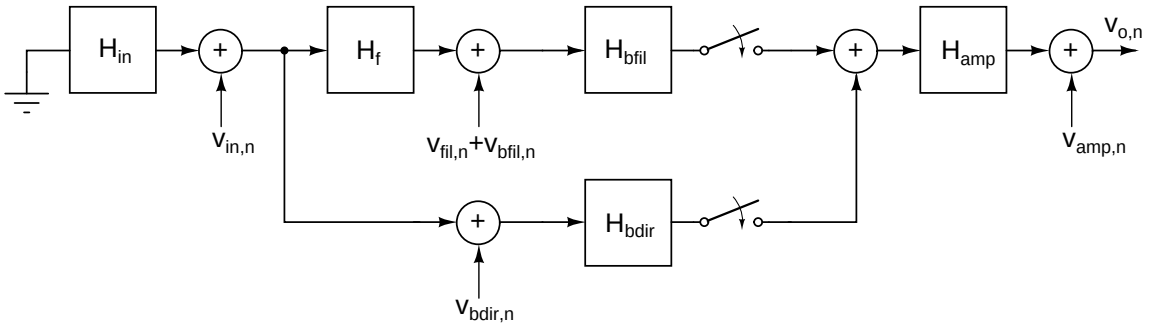


Figure 6.3: Block diagram for Noise measurement of the filter : Method 1

Considering the direct path noise measurement, we get the measured output noise spectral density S_{vo,n_dir} as

$$S_{vo,n\_dir} = S_{vamp,n} + (|H_{bdir}|.|H_{amp}|)^2.(S_{vbdir,n} + S_{vin,n}) \tag{6.5}$$

Considering the filter path noise measurement, we get the measured output noise spectral density S_{vo,n_fil} as

$$\begin{aligned} S_{vo,n\_fil} =& S_{vamp,n} + (|H_{bfil}|.|H_{amp}|)^2.(S_{vfil,n} + S_{vbfil,n}) \\ &+ (|H_f|.|H_{bfil}|.|H_{amp}|)^2.S_{vin,n} \end{aligned} \tag{6.6}$$

Subtracting (6.5) from (6.6), we get

$$\begin{aligned} S_{vo,n\_fil} - S_{vo,n\_dir} =& (|H_{bfil}|.|H_{amp}|)^2.S_{vfil,n} \\ &+ |H_{amp}|^2.(|H_{bfil}|^2.S_{vbfil,n} - |H_{bdir}|^2.S_{vbdir,n}) \\ &+ |H_{amp}|^2.((|H_{bfil}|.|H_f|)^2 - |H_{bdir}|^2).S_{vin,n} \end{aligned} \tag{6.7}$$

We have $H_{bfil} \approx H_{bdir} = H_b$ and we assume that the noise due to the direct path and filter path buffers are the same with the spectral density being equal to $S_{vb,n}$. We also assume that the noise contributed by the input stage is negligible. With these assumptions, from (6.7) we get

$$S_{vfil,n} = \frac{S_{vo,n\_fil} - S_{vo,n\_dir}}{(|H_b|.|H_{amp}|)^2} \tag{6.8}$$

The magnitude response $|H_b|.|H_{amp}|$ can be measured using frequency response measurements.

Method 2

In cases when the noise contributions from the direct and filter path buffer are unequal but the gains are almost the same, we propose another technique to measure the output noise of the filter. For this purpose, we need a provision in the buffer design to turn on both the paths (positive and negative) simultaneously. In this method, we donot make use of any direct path noise measurement. To explain the method, consider the block diagram in Fig. 6.4.

Considering the positive path measurement, which includes buffer with frequency response H_{b1} we have the output noise spectral density $S_{vfilpos,n}$ as

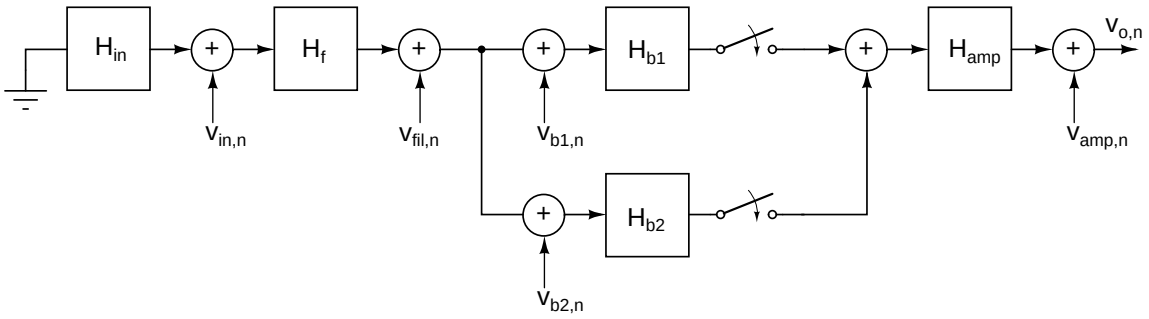


Figure 6.4: Block diagram for Noise measurement of the filter : Method 2

$$\begin{aligned} S_{vfilpos,n} =& S_{vamp,n} + (|H_{b1}|.|H_{amp}|)^2.(S_{vfil,n} + S_{vb1,n}) \\ &+ (|H_f|.|H_{b1}|.|H_{amp}|)^2.S_{vin,n} \end{aligned} \tag{6.9}$$

Considering the negative path measurement, we have the output noise spectral density $S_{vfilneg,n}$ as

$$\begin{aligned} S_{vfilneg,n} =& S_{vamp,n} + (|H_{b2}|.|H_{amp}|)^2.(S_{vfil,n} + S_{vb2,n}) \\ &+ (|H_f|.|H_{b2}|.|H_{amp}|)^2.S_{vin,n} \end{aligned} \tag{6.10}$$

When both the paths are turned on, we have the output noise spectral density $S_{vfilboth,n}$ as

$$\begin{aligned} S_{vfilboth,n} =& S_{vamp,n} + |H_{amp}|^2.((|H_{b1} + H_{b2}|)^2.S_{vfil,n} \\ &+ |H_{amp}|^2.(|H_{b1}|^2.S_{vb1,n} + |H_{b2}|^2.S_{vb2,n}) \\ &+ (|H_f|.(|H_{b1}| + |H_{b2}|).|H_{amp}|)^2.S_{vin,n} \end{aligned} \tag{6.11}$$

Assuming the input stage noise to be negligible and using the fact that $H_{b1} \approx -H_{b2} = H_b$, (6.9)+(6.10)-(6.11) gives

$$S_{vfilpos,n} + S_{vfilneg,n} - S_{vfilboth,n} = S_{vamp,n} + 2.(|H_b|.|H_{amp}|)^2.S_{vfil,n} \tag{6.12}$$

We can find $S_{vamp,n}$ by measuring the output noise spectral density when the buffers are turned off.

Hence, we get

$$S_{vfil,n} = \frac{S_{vfilpos,n} + S_{vfilneg,n} - S_{vfilboth,n} - S_{vamp,n}}{2.(|H_b|.|H_{amp}|)^2} \tag{6.13}$$

6.1.3 Distortion

In order to measure the distortion of the filter, the distortion added by the interfacing circuit must be low. Also, for IMD measurements the sources must be sufficiently isolated to have an input with low distortion. The measurement is done using a Spectrum Analyzer. While measuring the distortion, care must be taken to avoid distortion contribution from the analyzer itself.

6.2 Design of Testboard

In this section, we discuss about the design of the testboard used for characterizing the filter. Fig. 6.5 shows the block diagram of the testboard. Since the filter is implemented in a fully differential manner and the available sources are single-ended, we require a single-ended to differential converter. In a similar manner, since we can measure single-ended signals only, we use a differential to single-ended converter at the output of the filter. The power supply block is required to supply power to all the sections of the testboard.

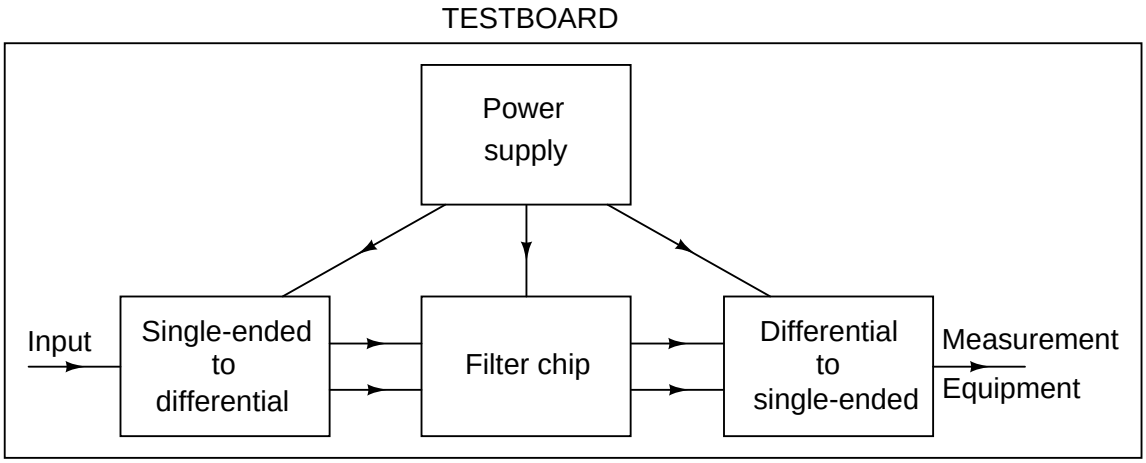


Figure 6.5: Block diagram of Testboard

6.2.1 Power supply

In order to minimize the number of independent sources required for the testboard and to stabilize the power supply to the filter block, voltage regulators are used. The input to the chips is a 5 V supply. Two regulators (TPS73601 from TI) are used to generate the 1.8 V and 3.3 V supply. Bias capacitors are added to stabilize these voltages.

6.2.2 Single-ended to differential converter

In order to convert the signal from single-ended to differential, two circuits were implemented. In Testboard 1, a fully differential opamp (THS4502 from TI) is used. Fig. 6.6 shows the circuit diagram. A single ended voltage source is applied to one input of the opamp, keeping the other grounded. Due to the high CMRR of the opamp, the common mode component of this input signal is rejected and a differential voltage of the input magnitude is generated at the output . The opamp has a provision to vary the output common mode voltage generated. A simple potential divider which is RC filtered, is used to generate this voltage. For measuring IMD, two sources v_{s1} and v_{s2} are added using the opamp summer circuit.

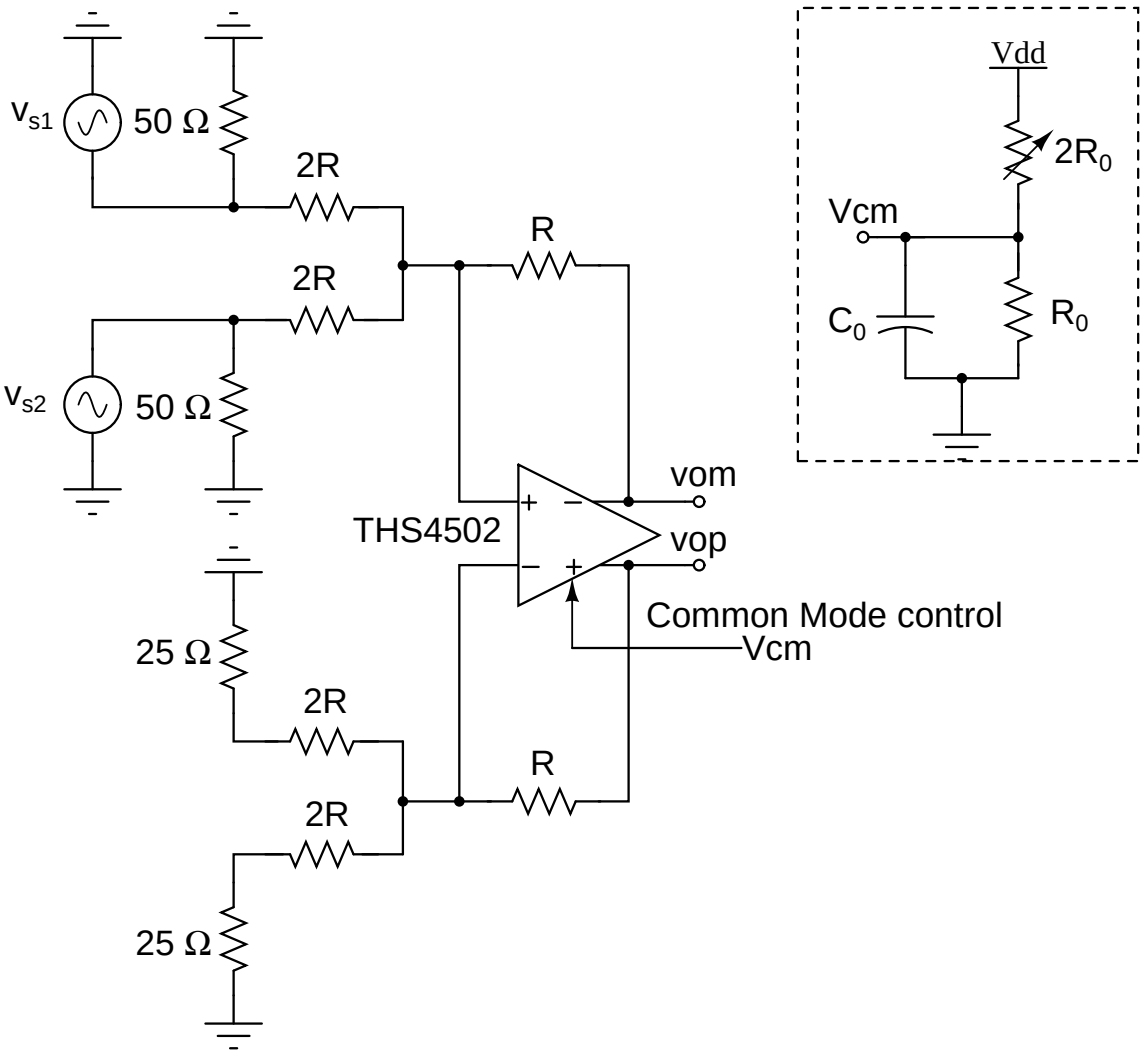


Figure 6.6: Single-ended to differential circuit in Testboard 1

In the implementation in Testboard 2, a BALUN is used to achieve the same. Fig. 6.7 shows the circuit diagram. The BALUN used is ADTW from Minicircuits® with a turns ratio of 1:1. For measuring IMD, the sources are added using a resistive attenuator circuit formed by the resistors (resistance equal to R) as shown. The output common mode is achieved by center tapping the transformer on the secondary side.

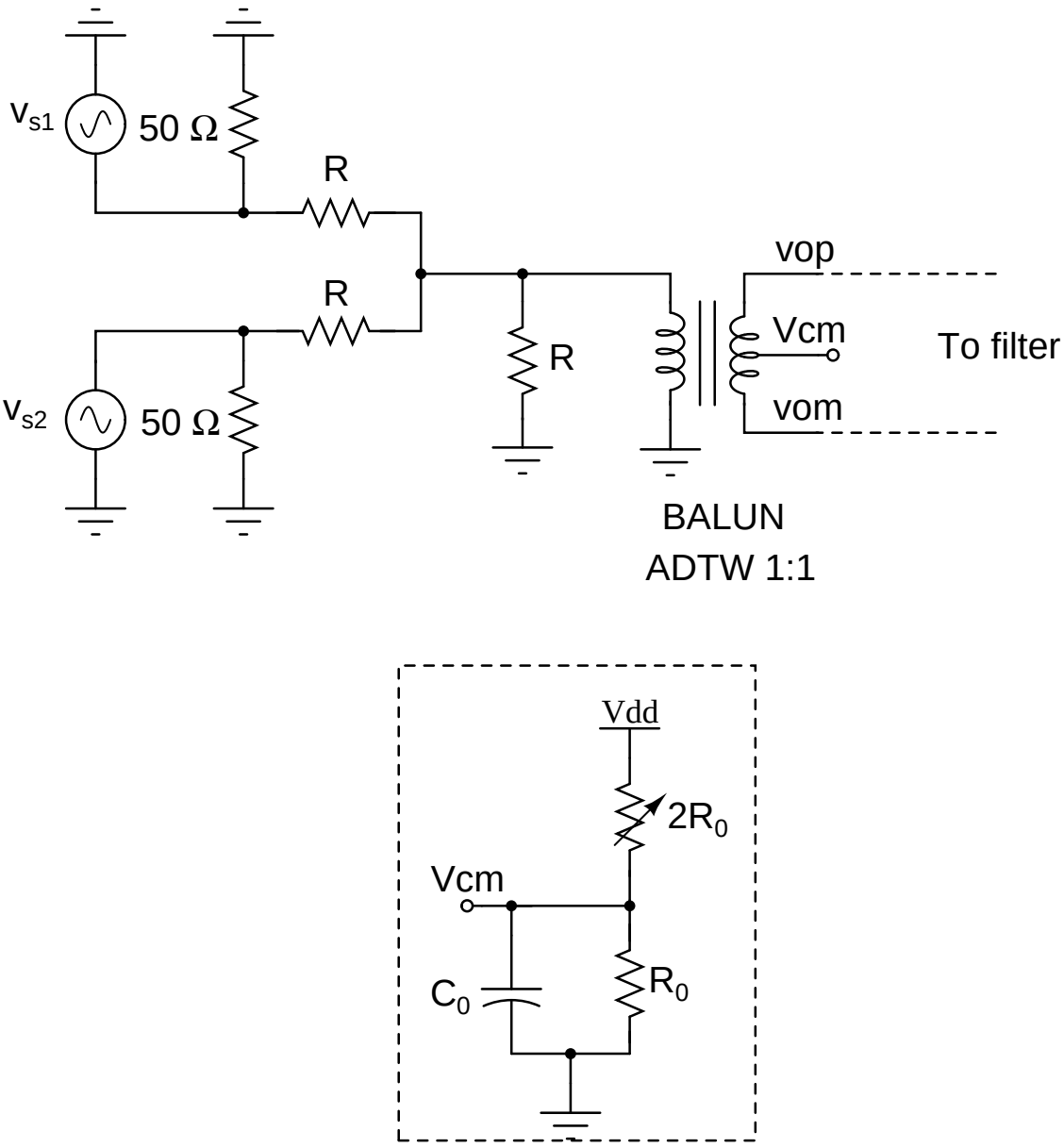


Figure 6.7: Single-ended to differential circuit in Testboard 2

Though both the circuits generate the appropriate differential voltage required,

experimental results show that the circuit in Testboard 1 is a better implementation for distortion measurements. In Testboard 2, since a resistive attenuator is used for summing the input signals, the sources itself get intermodulated and the generated signals are highly distorted. In other words, the isolation between the two sources is not enough. In Testboard 1, the summing of the sources is performed at the low impedance node of the opamp's virtual ground. Hence, the distortion generated due to self intermodulation between the sources is highly reduced. An even better design can be achieved in Testboard 1, by applying one source to the positive input of the opamp and the other to the negative input. In this way, the isolation between the sources is much better.

6.2.3 Filter chip

The interface circuitry is shown in Fig. 6.8. The 1.8 V and 3.3 V are given to the chip from the voltage regulators. The external resistor required for the filter fixed transconductance bias circuitry is implemented using a potentiometer as shown. The buffers are control using switches implemented using jumpers. The same is done for the injection and tuning control.

6.2.4 Differential to single-ended converter

In Testboard 1, two different converter circuits were implemented. Fig. 6.9 shows the first circuit implemented. The output current from the filter is first amplified using a transimpedance stage amplifier. This is implemented using opamp a high speed opamp OPA847 (from TI). The output bias of the filter is set by V_{bias}. Capacitor C_x acts as a high pass filter to filter out the dc component. The generated differential output is converter to a single ended voltage using the opamp OPA842. This kind of implementation requires a high ugf opamp with compensation in order to achieve a transimpedance amplifier to span the whole filter bandwidth. Hence, for stability reasons this circuit was not used during measurement.

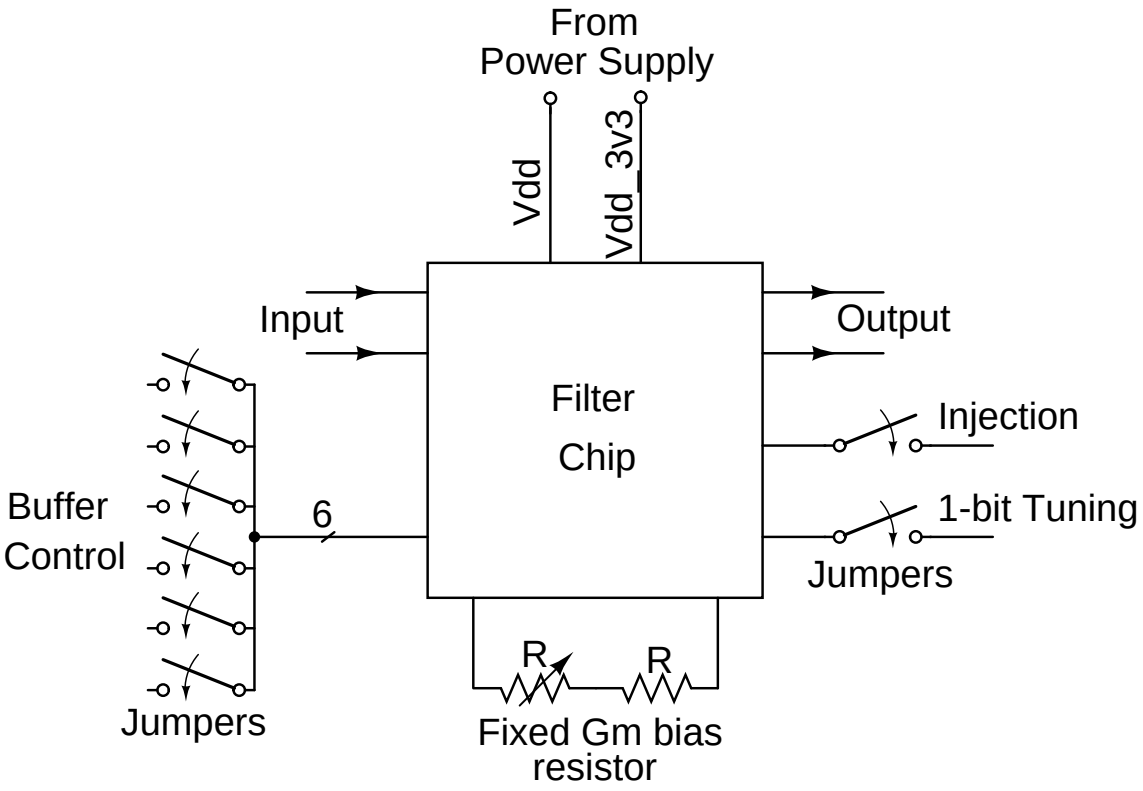


Figure 6.8: Circuit diagram for the filter chip block

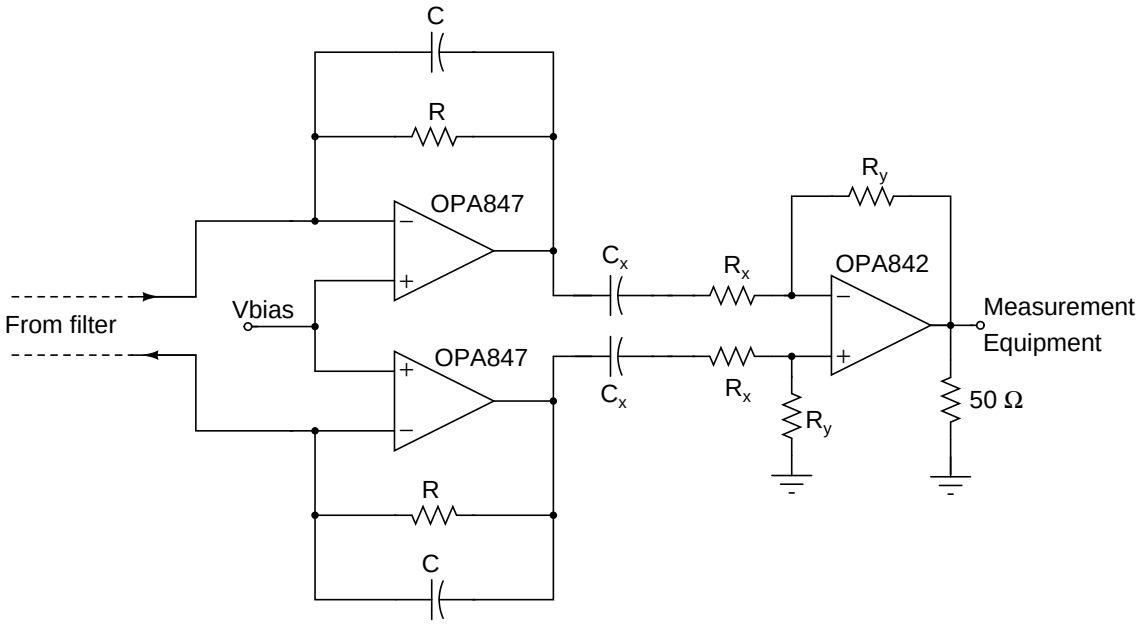


Figure 6.9: Differential to single-ended circuit in Testboard 1

The second circuit implemented is shown in Fig. 6.10. A BALUN has been used with a center tapping dc voltage of 3.3 V applied to the primary. The secondary is directly connected to the measuring equipment. For noise measurements, this is not enough because the noise figure of the spectrum analyzer is low. Hence, in the design in Testboard 2 shown in Fig. 6.11 the secondary is terminated with a large resistor taking into consideration the bandwidth requirements. This voltage is then amplified using a low-noise, low-distortion, high gain-bandwidth opamp in an inverting configuration. The opamp used is OPA843 from TI.

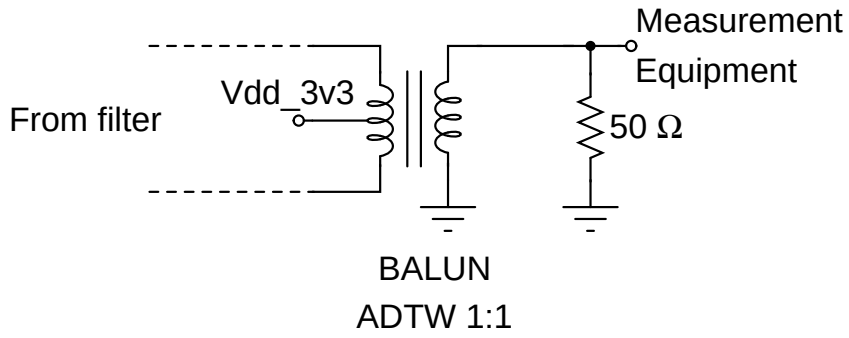


Figure 6.10: Differential to single-ended circuit in Testboard 1

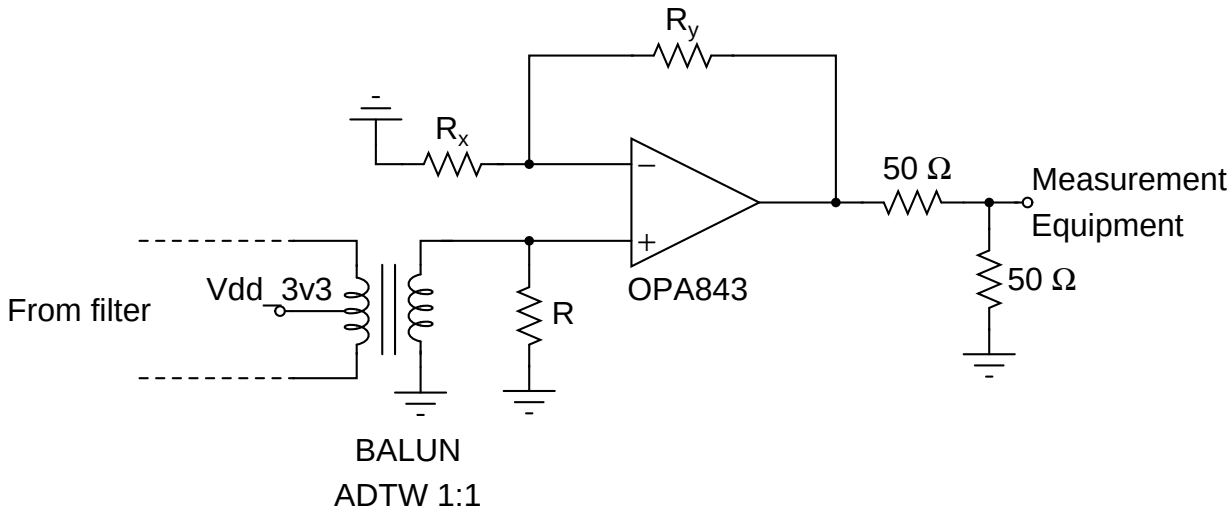


Figure 6.11: Differential to single-ended circuit in Testboard 2

The photograph of the populated testboards for the two designs are shown in Fig. 6.12 and 6.13. From the design of the testboards, it is concluded that for measurement of response, noise and distortion it is best to use an active BALUN at

the input side and a passive BALUN at the output followed by a high performance amplifier.

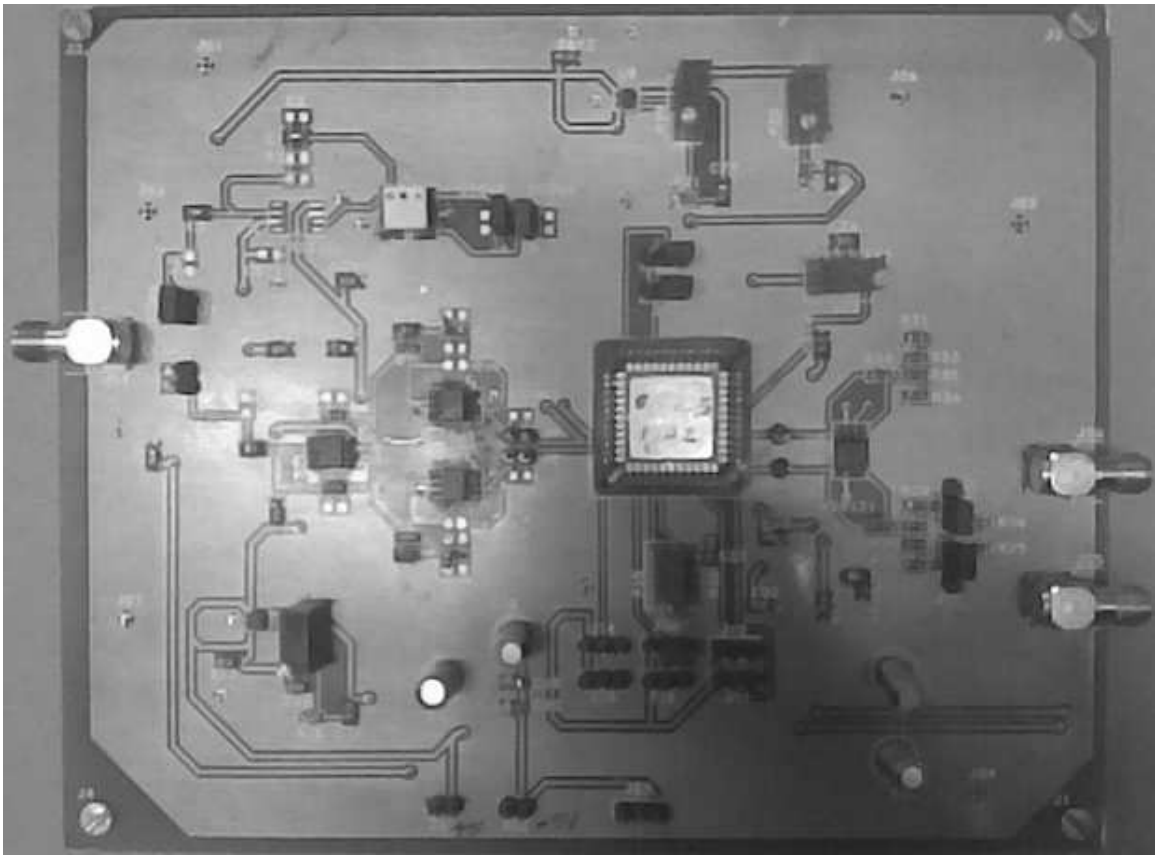


Figure 6.12: Photograph of the first testboard

6.3 Experimental Results

A fifth order Chebyshev Active-RC filter with design specification as in 4 was implemented and fabricated through Europractice program. A 44 pin JLCC was used for packaging the chip. The chip occupies an area of 0.33 mm^2.

6.3.1 Frequency Response

The measured frequency response of the filter without/with current injection is shown in Fig. 6.14. It is seen that the bandedge of the filter is 19 MHz. This is due

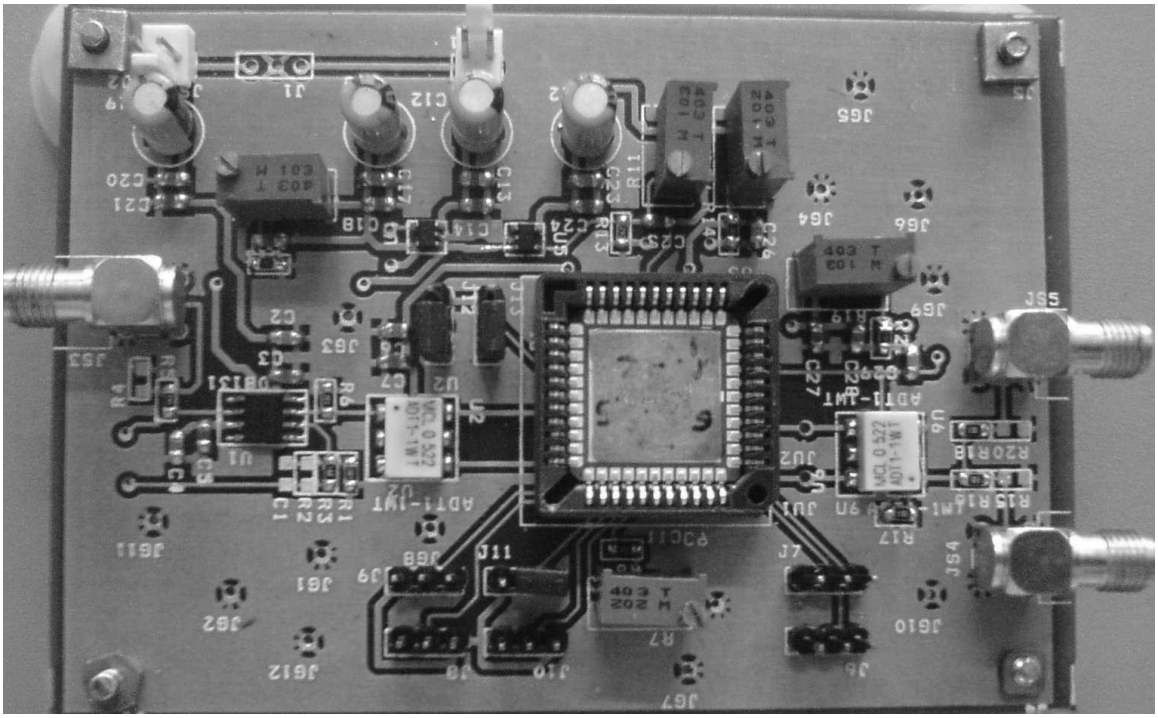


Figure 6.13: Photograph of the second testboard

to slight RC variations in the fabrication process. The other aspect to be noticed is that the response of the filter without injection peaks more than that with injection as we saw in the simulation results. This is to be expected because with current injection the opamps in the BQ2 section of the filter tend more towards ideal behaviour and the peaking reduces. This confirms the working of the current injection technique in the test chip.

Fig. 6.15 and Fig. 6.16 show the measured frequency response for 10 chips plotted on the same plot for the cases without and with current injection respectively. The robustness of the technique is indicated by the good repeatability seen in the frequency response plots.

6.3.2 Noise

Fig. 6.17 shows the measured output noise spectral density of the filter without/with current injection. For the case with current injection, the input referred

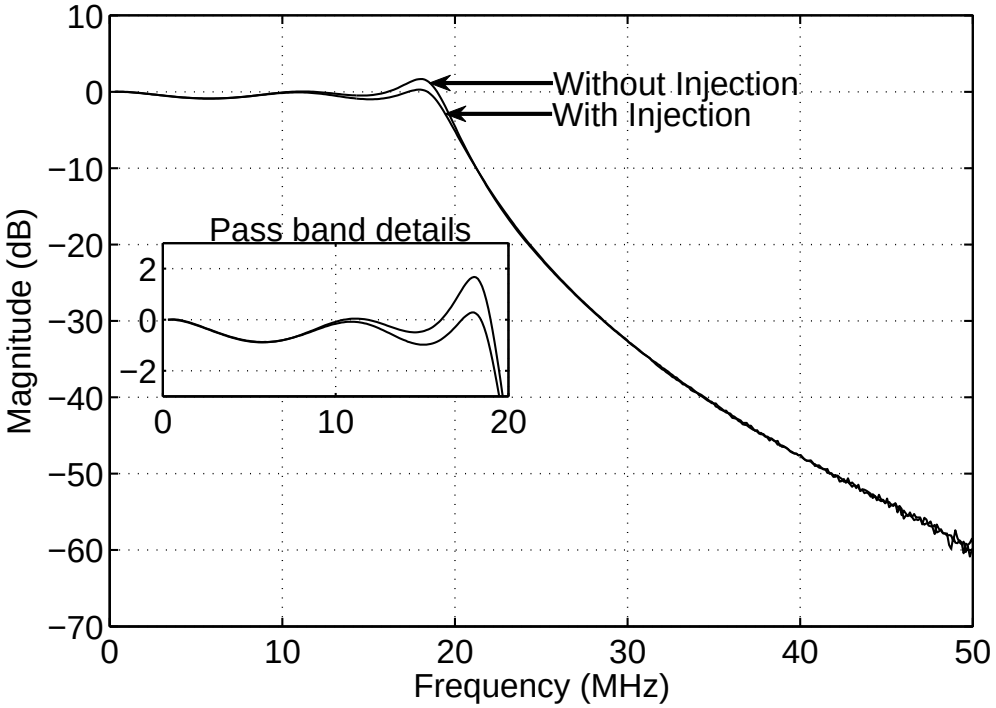


Figure 6.14: Measured Frequency Response without/with current injection

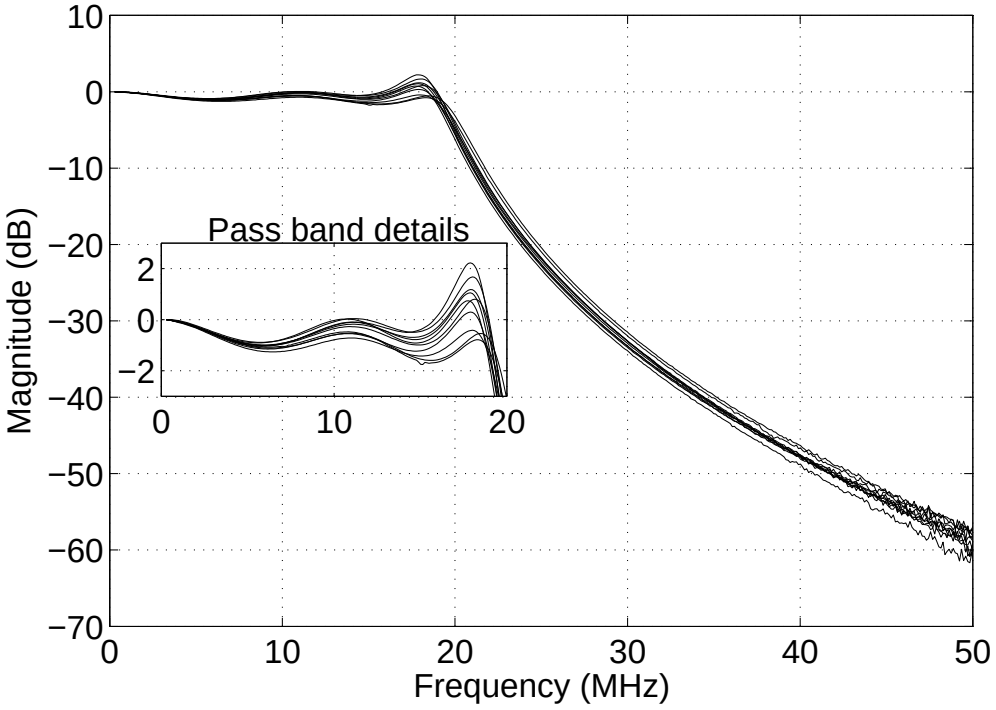


Figure 6.15: Measured Frequency Response of 10 chips without current injection

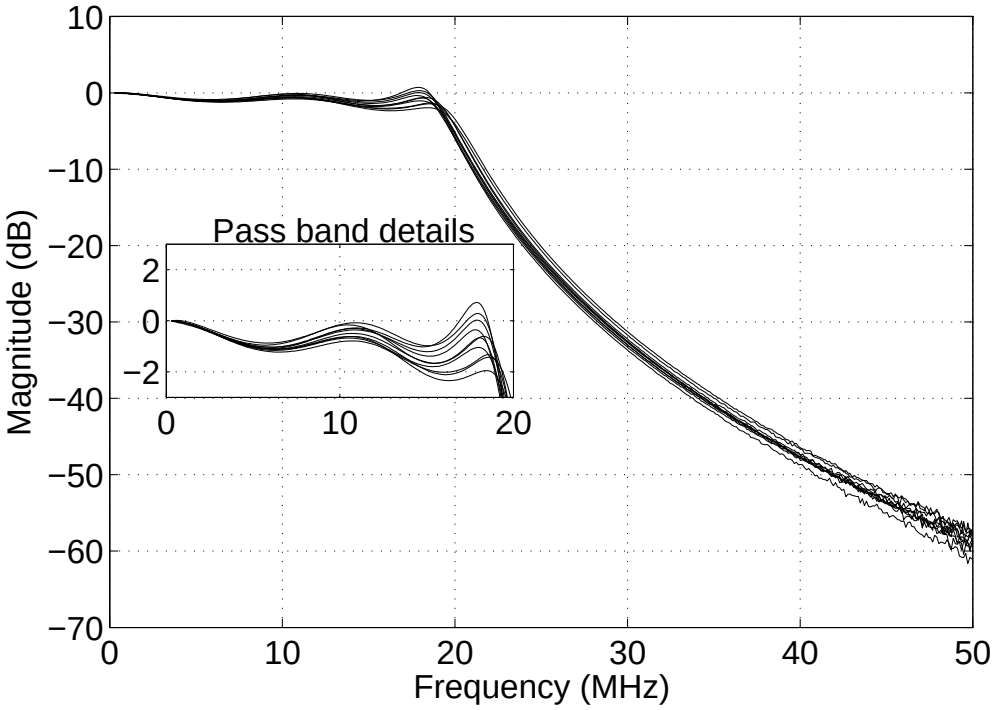


Figure 6.16: Measured Frequency Response of 10 chips with current injection

noise generated due to the injected noise current is much lesser than the inherent noise of the filter as had been discussed in Chapter 3, Section 3.2.1. Thus, it is seen that the measured noise is almost same in both the cases. The measured output noise of the filter without current injection is 2.01 Vrms and that with current injection is 1.93 Vrms. The noise is much more than the simulated value due to flicker noise contribution.

6.3.3 Distortion

The distortion of the filter was characterized using IMD measurements. Two tones at $f_0 - 0.1$ MHz and $f_0 + 0.1$ MHz were given as input, with f_0 varying from 2 MHz to 22 MHz with finer steps at the bandedge. Fig. 6.18 shows the IMD for an input differential amplitude of 400 mV per tone. At high frequencies near the bandedge where the filter distortion dominates, we can see an improvement of around 9.25 dB. At low frequencies, the buffer distortion dominates over that of

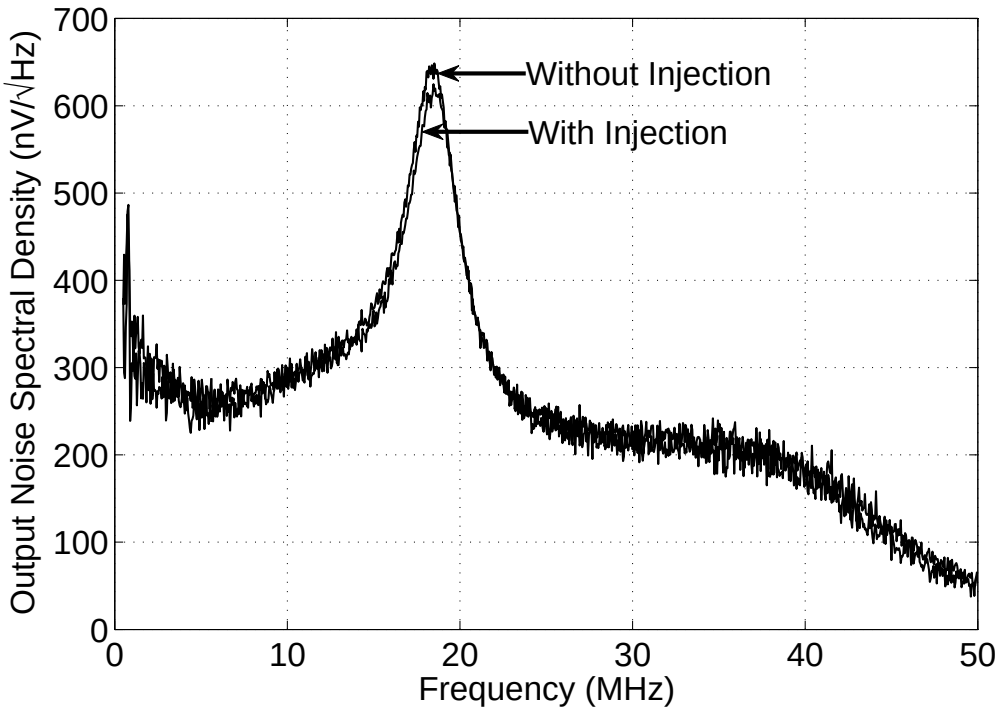


Figure 6.17: Measured Output Noise Spectral density

the filter and hence the distortion remains almost a constant. Fig. 6.19 shows the output spectrum without/with current injection for an input differential voltage of 625 mV per tone. We see the improvement in distortion even for high input amplitudes. The measured improvement may not be a good indicator of the efficacy of the technique because the output amplitudes in the two cases are slightly different. It must be noted that even by considering this factor, the improvement is significant. A better indicator, independent of the input and output amplitudes is the Input Third Order Intercept Point (IIP3).

Fig. 6.20 shows the IIP3 as a function of frequency. It is seen from the plots that the least IIP3 occurs at the bandedge as expected. With the current injection technique, we obtain an improvement in IIP3 by a factor of 1.9, thus indicating the efficacy of the technique. Table 6.1 summarizes the filter performance.

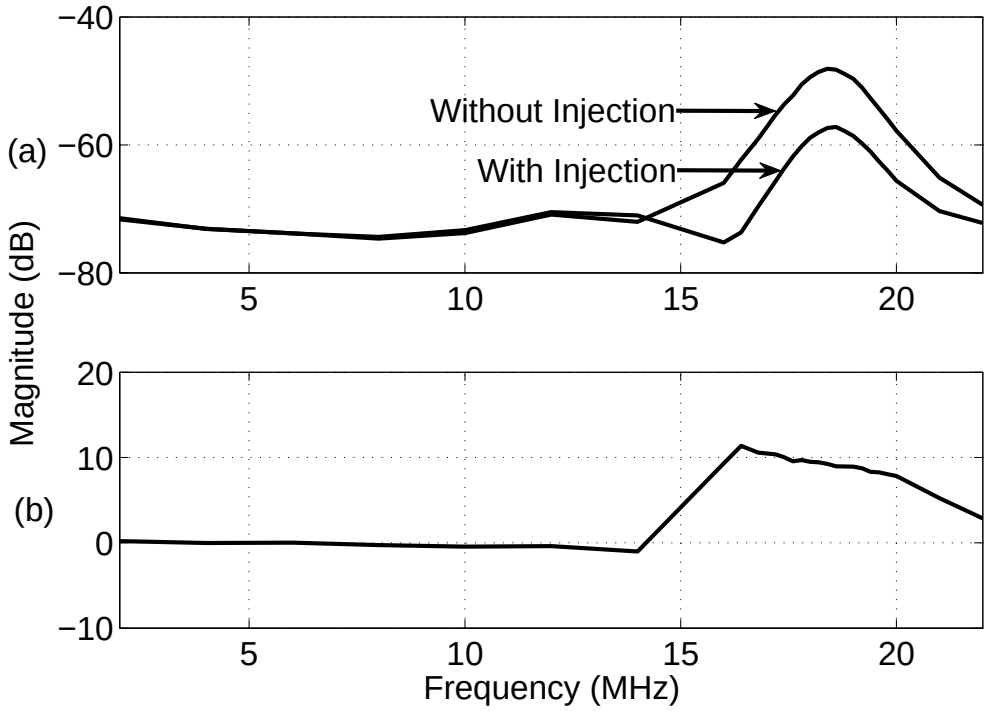


Figure 6.18: (a) IMD as a function of frequency for input differential amplitude 400 mV per tone (b) Improvement in IMD

Table 6.1: Summary of Measurement Results

	Without Injection	With Injection
Technology	0.18 μm CMOS	
Filter type	5^{th} order Chebyshev	
Supply voltage	1.8 V	
Bandwidth	19 MHz	
Active chip area	0.33 mm^2	
Power	4.09 W	5.06 W
Integrated output noise	2.01 mVrms	1.93 mVrms
IMD test tones at 18.3 MHz and 18.5 MHz with amplitude 400 mV differential per tone		
IMD @ 18.4 MHz	−48.09 dB	−57.34 dB
IIP3 @ 18.4 MHz	3.48 Vrms	6.65 Vrms

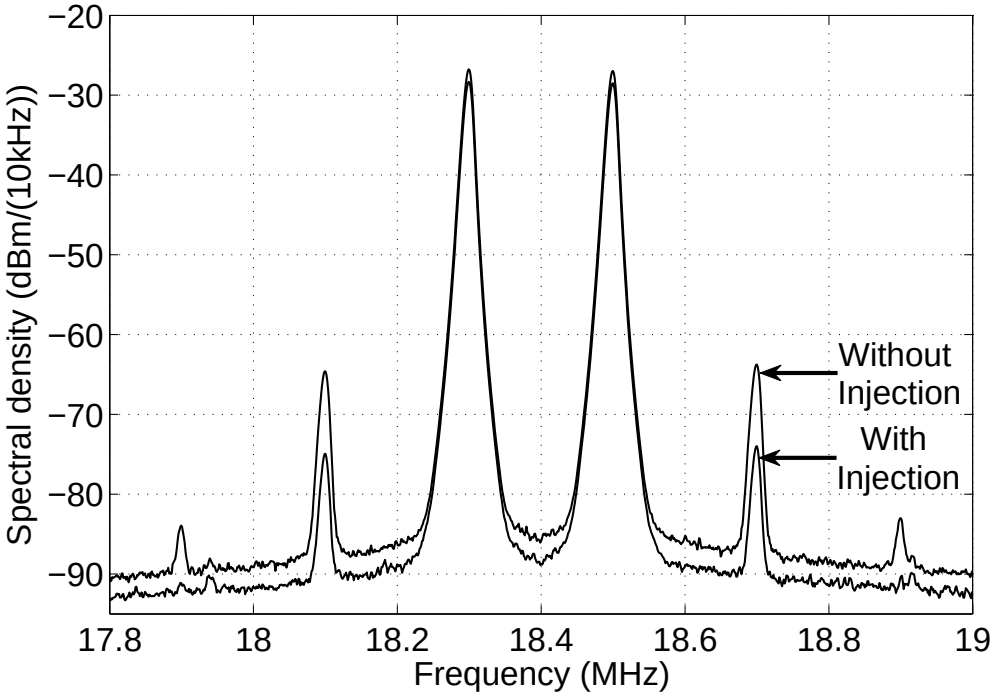


Figure 6.19: Output spectrum without/with current injection for an input differential voltage of 625 mV per tone near the filter bandedge

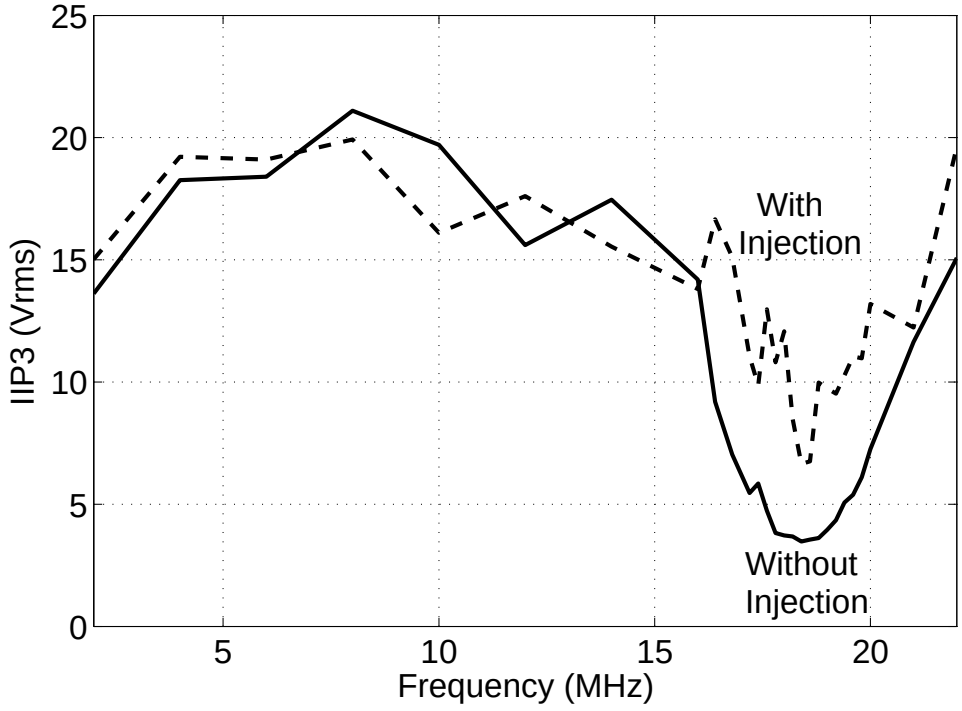


Figure 6.20: Measured IIP3 as a function of frequency

CHAPTER 7

Design of a Fifth Order Active-RC Chebyshev filter with Current Injection using Triode transconductors

In order to validate the second method in the proposed technique in Chapter 3, a fifth order Active-RC low-pass Chebyshev filter is designed in 0.18 μm CMOS process with a supply voltage of 1.8 V, having specifications similar to the previous design. The filter is fully differential with a common mode of half the supply voltage. In order to compare the performance of the filter without/with current injection, two separate designs are implemented with one of them using the proposed technique. In this chapter, we focus on the design details of each of the blocks which make up these filters. Fig. 7.1 and 7.2 show the block diagrams of the designed chips. The filters here are implemented as a cascade of FOS, BQ1 and BQ2 sections.

7.1 Opamp Design

As discussed in the previous design, the first/second order sections are realized as a negative feedback system with the opamp as the active element. For high gain requirements a two-stage opamp was used in that design. We use a single-stage opamp in the design of this filter. Single-stage opamps have several advantages than their two-stage counterparts. For the same power dissipation, the single stage architecture is much faster than the two-stage opamp. Since the number of stages is only one, the system is mainly first order in nature and hence is very stable with respect to common mode and differential mode stability. The disadvantage of using a single-stage opamp is that its gain is low, but with the

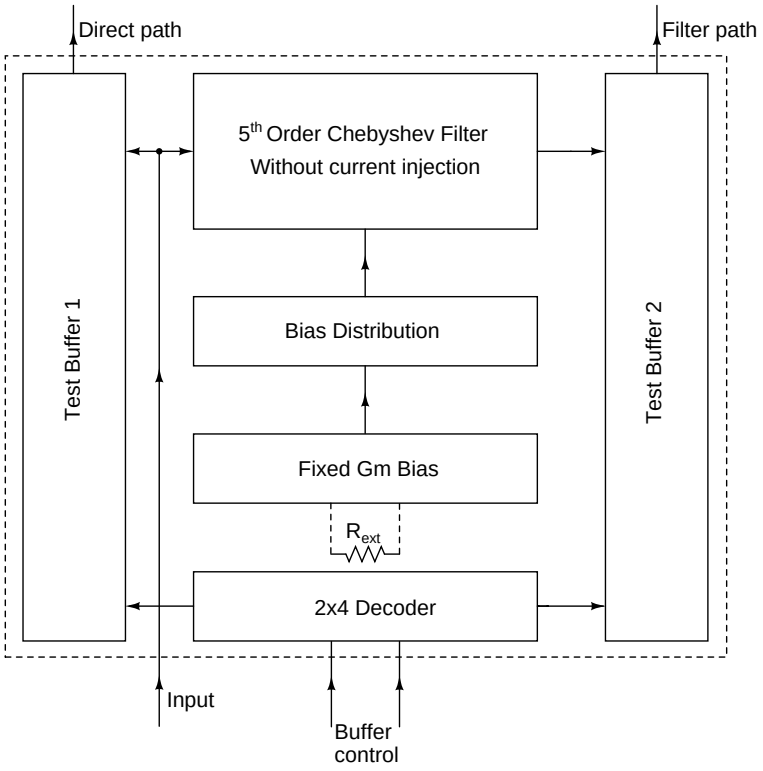


Figure 7.1: Block diagram of the chip without current injection

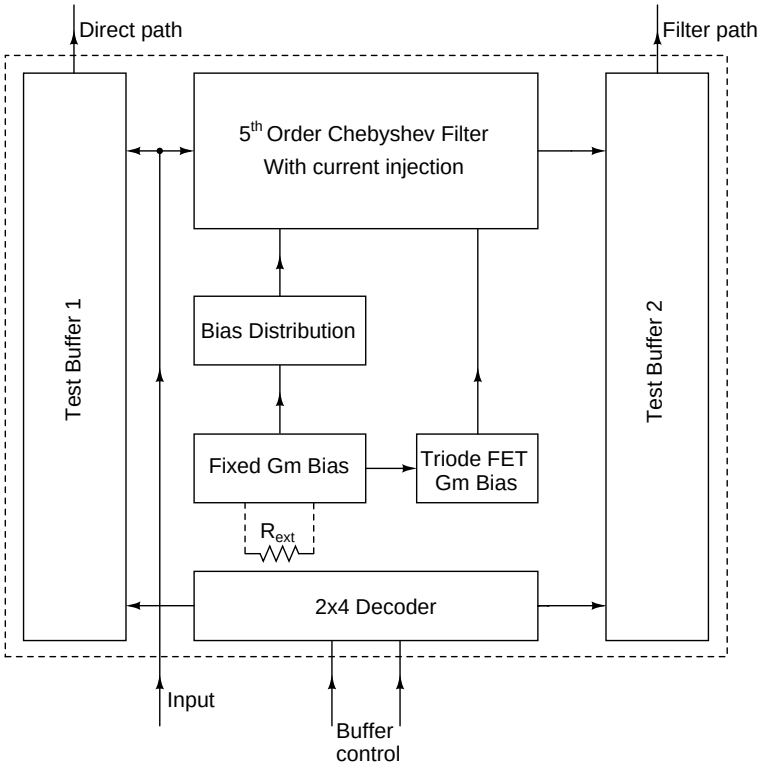


Figure 7.2: Block diagram of the chip with current injection

technique of current injection its gain is enhanced. In this design, we use a single-stage folded cascode opamp as the building block of our filter. Using such an opamp architecture provides a greater scope for the current injection technique. Since there are two independent current sources in the design, current injection can be implemented easily.

7.1.1 Folded cascode stage

The schematic of the opamp is shown in Fig. 7.3. Transistor M2 is used to bias the transistors at a constant current provided by the fixed transconductance bias. The input differential pair comprises of M4a and M4b. In order to reduce the flicker noise of the opamp, PMOS transistors have been used as the input pair. The differential current generated in the input pair is folded to the NMOS transistors M7a and M7b. Using an output stage with cascode transistors helps in improving the gain of the opamp but this limits the maximum achievable swing of the filter. In this design, M6 and M7 act as the output cascode transistors. The current source M5 is controlled by a common mode feedback loop to stabilize the output common mode voltage. The unity gain frequency of the opamp is determined by the transconductance of the input pairs M2 and the output load capacitance.

7.1.2 Common mode feedback loop

Referring back to Fig. 7.3, we now discuss the common mode feedback loop used in the opamp. In order to fix the output common mode voltage of the opamp, a single common mode feedback loop is used. The operation of the loop is similar to the one used in Design 1 in the two-stage Miller compensated opamp. The resistor R and capacitor C are used to detect the output common mode of the opamp. When the measured common mode voltage is different from V_{cm}, the currents in the branches M3a and M3b are unequal. This causes the current density in the branch comprising of transistor M9-M12 to be either greater/lesser than that in the opamp. This error in the current is corrected by the loop by adjusting the

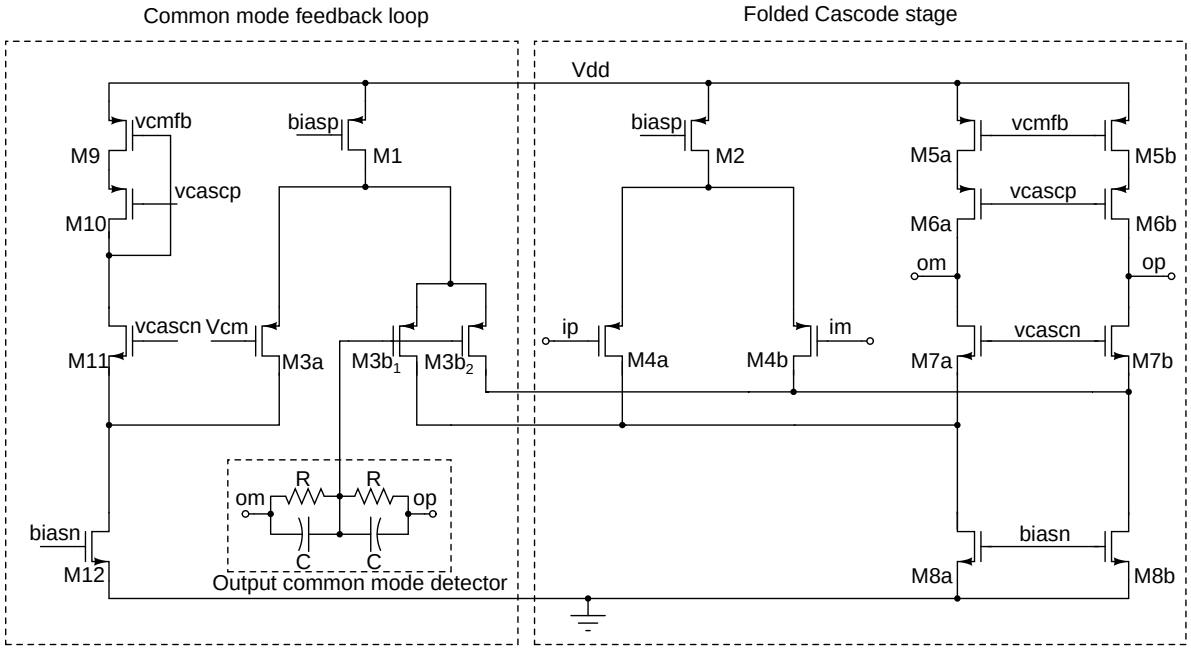


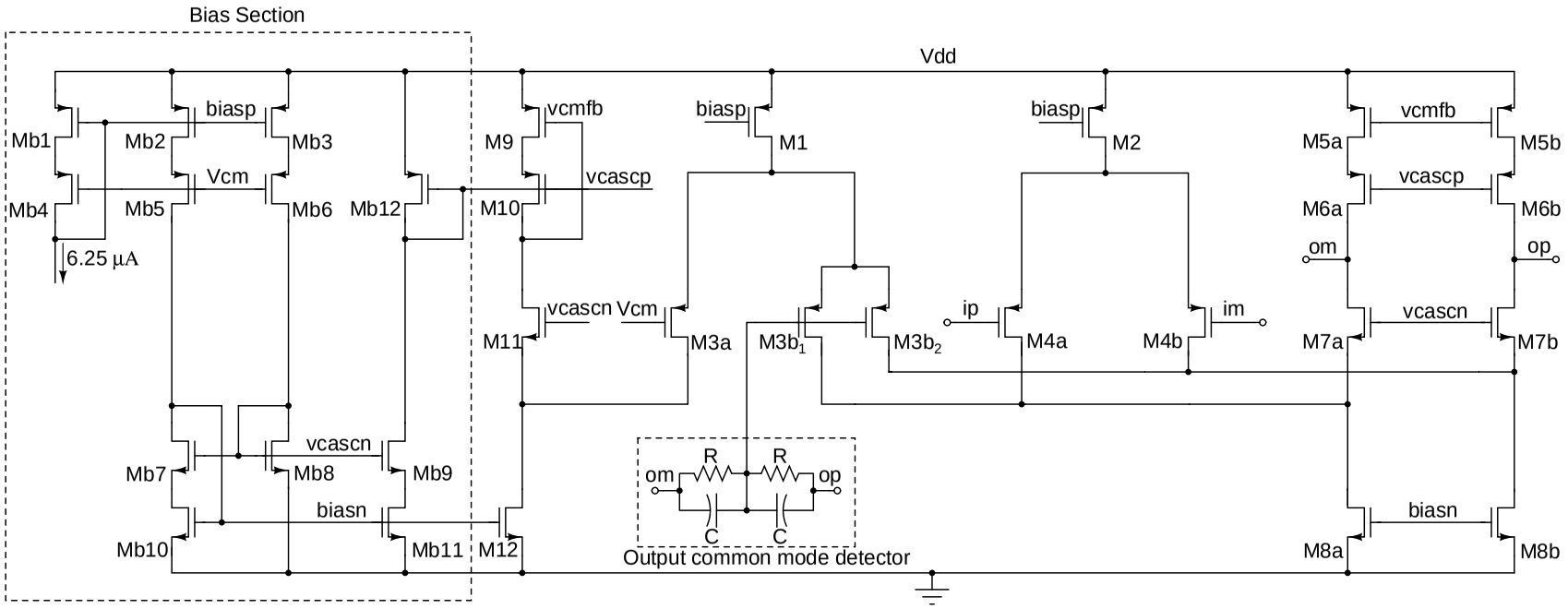
Figure 7.3: Circuit diagram of the folded cascode opamp with cmfb loop

current through M5a and M5b, till the current densities become equal. To avoid offset problems in the output common mode voltage, transistors M3a, M3b, M4a, M4b ; M6, M10; M5 and M9; M7 and M11 must have the same current density.

The complete circuit diagram of the opamp with the sizes is shown in Fig. 7.4. The bias section of the opamp is also shown. The transistors Mb1 and Mb4 carry currents supplied from the fixed transconductance bias. Using cascode transistors, the currents are replicated and fed to the opamp.

7.2 Triode transconductor

Before proceeding to the implementation of the current injection scheme, we discuss a transconductance circuit implemented using triode transistors. We are especially interested in this implementation because of linearity issues. Fig 7.5 shows the circuit diagram of the differential triode transconductor. Transistors M1a and M1b form the input pair and are biased in the triode region. Transistors M2a and M2b are used to maintain the drain source voltage across M1a and M1b



M1 : 16 (2/0.18)	M5 : 36 (2/0.18)	M10 : 4 (1/0.18)	Mb4, Mb6 : 2 (0.5/0.18)	Mb10 : 4 (2/0.72)
M2 : 64 (2/0.18)	M6 : 18 (1/0.18)	M11 : 8 (0.5/0.18)	Mb5 : 4 (0.5/0.18)	Mb11 : 2 (2/0.72)
M3a : 8 (0.5/0.18)	M7 : 36 (0.5/0.18)	M12 : 16 (2/0.72)	Mb7 : 4 (0.5/0.18)	Mb12 : 2 (0.5/1)
M3b : 4 (0.5/0.18)	M8 : 72 (2/0.72)	Mb1, Mb3: 2 (2/0.18)	Mb8 : 2 (0.24/2)	R = 500 kΩ
M4 : 32 (0.5/0.18)	M9 : 8 (2/0.18)	Mb2 : 4 (2/0.18)	Mb9 : 2 (0.5/0.18)	C = 20 fF

Figure 7.4: Circuit diagram of the folded cascode opamp with the sizes

respectively, to fix their transconductance. This is achieved by varying the gate control voltage V_{cont} of M2a and M2b. The transistors M1a and M1b carry a constant current I such that no dc current flows through the resistors R. This is done to ensure convergence in simulation.

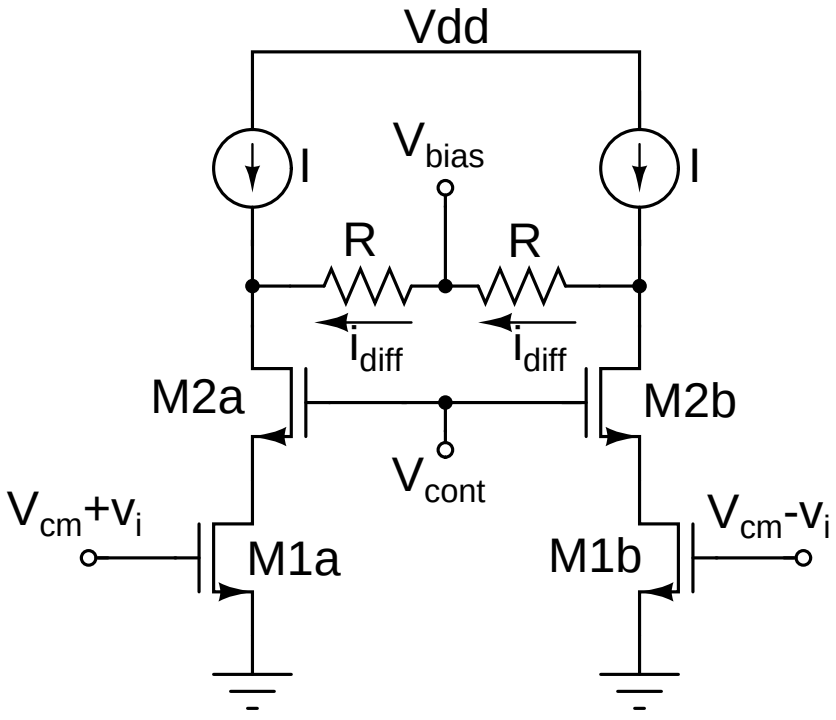


Figure 7.5: Circuit diagram of the triode transconductor

Using the simple Square law model for the MOSFETs, we have the quiescent current I through M1 as

$$\begin{aligned} I &= \mu_n C_{ox} \frac{W}{L}\Big|_{M1} .[(V_{cm} - V_t)V_{ds,M1} - \frac{{V_{ds,M1}}^2}{2}] \\ &\approx \mu_n C_{ox} \frac{W}{L}\Big|_{M1} (V_{cm} - V_t)V_{ds,M1} \end{aligned} \tag{7.1}$$

where μ_n is the mobility, C_{ox} the oxide capacitance, W and L are the sizes of the transistor M1, V_{cm} the input common mode voltage, V_t the threshold voltage of M1 and $V_{ds,M1}$ its drain source voltage. Thus, we see that the current varies linearly with the applied signal voltage at the gate.

Hence, the transconductance $g_{m,M1}$ is given as

$$g_{m,M1} = \mu_n C_{ox} \frac{W}{L}|_{M1} V_{ds,M1} \tag{7.2}$$

From (7.1) and (7.2) we observe that if we require a fixed transconductance from this circuit, the current I is automatically fixed. With a normal transistor, this current is generally not enough for high input swings. In order to overcome this limitation, M1 is implemented as a Low threshold voltage transistor. We now evaluate the differential input output characteristics for this transconductor.

We denote $\beta_{M1} = \mu_n C_{ox} \frac{W}{L}|_{M1}$ and $\beta_{M2} = \mu_n C_{ox} \frac{W}{L}|_{M2}$.

For M1a, assuming the large signal operation we have

$$I + i_{diff} = \beta_{M1}(V_{cm} + v_i)V_{ds,M1} \tag{7.3}$$

For transistor M2a in saturation,

$$I + i_{diff} = \beta_{M2}(V_{cont} - V_{t,M2} - V_{ds,M2})^2 \tag{7.4}$$

Solving (7.3) and (7.4), we get

$$I + i_{diff} = \beta_{M1}(V_{cm} + v_i)\Bigg[V_{cont} - V_{t,M2} + \frac{\beta_{M1}}{\beta_{M2}}\frac{V_{cm} + v_i}{2} - \sqrt{\left(\frac{\beta_{M1}}{2\beta_{M2}}\right)^2 (V_{cm} + v_i)^2 + \frac{\beta_{M1}}{\beta_{M2}}(V_{cont} - V_{t,M2})(V_{cm} + v_i)}\Bigg] \tag{7.5}$$

For evaluating $I - i_{diff}$ for transistor M1b, we replace v_i with $-v_i$. The input output characteristic of this transconductor is shown in Fig. 7.6. We note that the characteristics are of a expansive type compared to conventional compressive characteristics. This helps in further cancellation of distortion by the method of current injection.

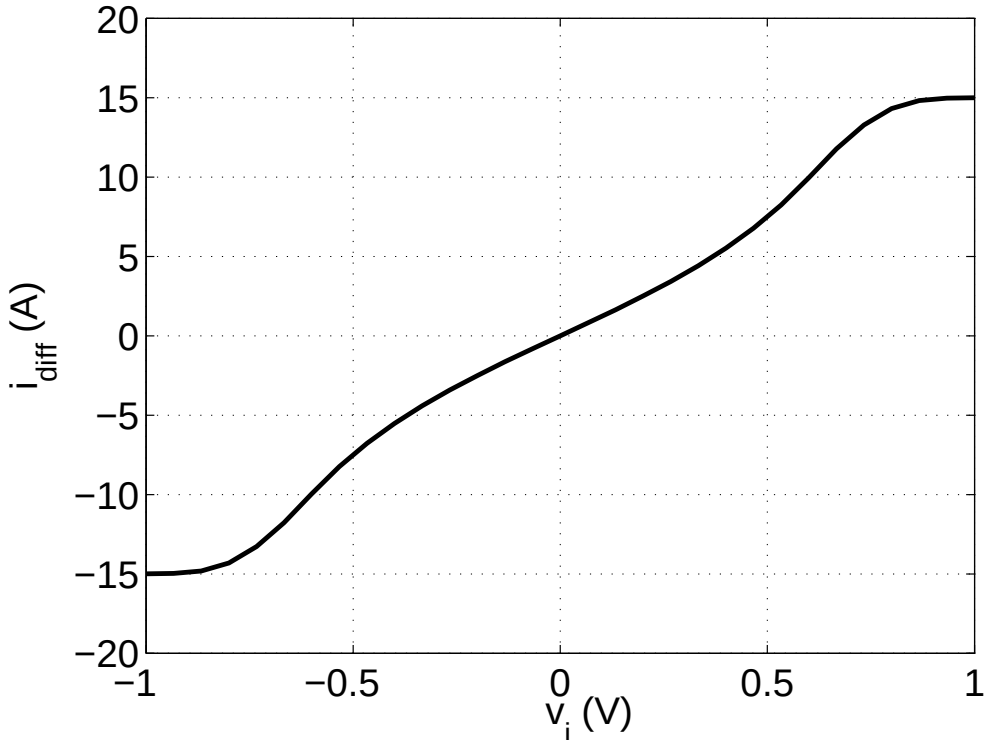


Figure 7.6: Characteristics of the triode transconductor

7.3 Opamp with current injection

The folded cascode opamp operation has been discussed in Section 7.1. In order to explain the current injection scheme using triode transistors consider Fig. 7.7. We observe that the current sources comprising of transistors M8a and M8b are used only for biasing purposes. The sizes of the transistors M8a and M8b are adjusted such that they implement only part of the actual current required. The remainder of the quiescent current is contributed by the triode transconductors. Hence, no extra power is consumed in implementing this technique.

In order to implement three transconductors for current injection, we add transistors Mt1-Mt3, Mx1-Mx3 in parallel to the current source M8. The control voltage to fix the transconductance is applied to transistors Mx1-Mx3. We could have also applied the control voltage to the gates of M7a and M7b without using the transistors Mx1-Mx3. Using an extra stage in between helps in isolating the low

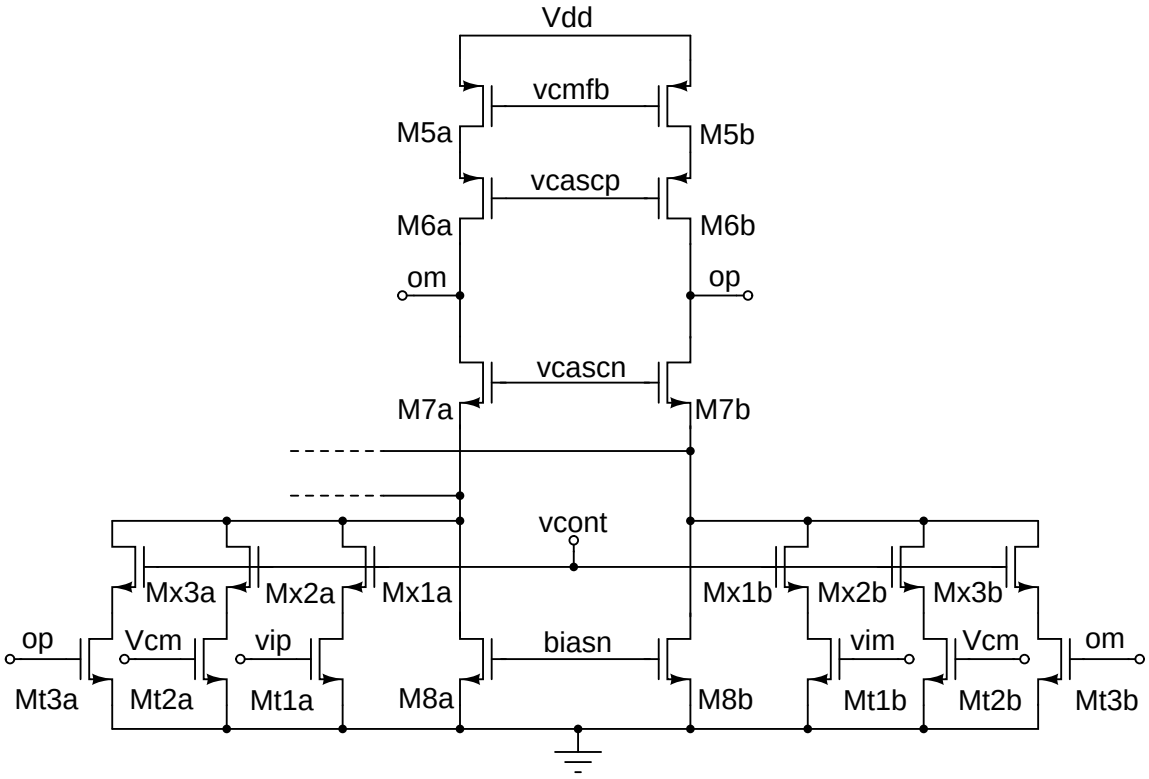
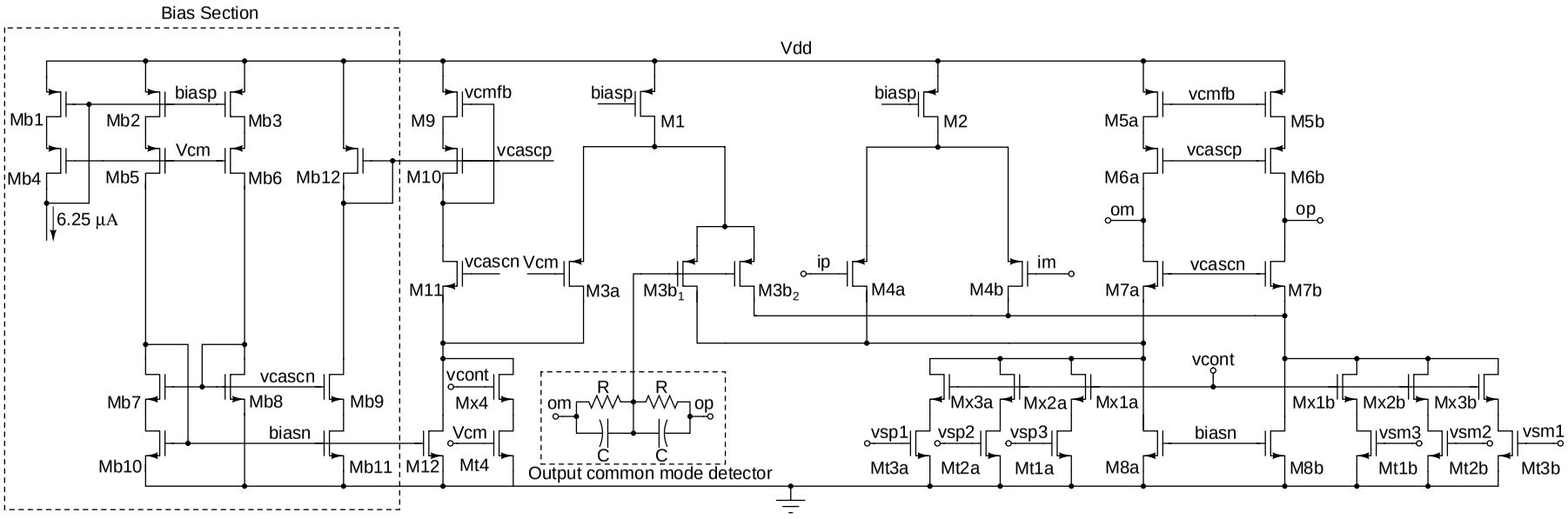


Figure 7.7: Proposed implementation of the current injection technique

threshold voltage transconductors further from the output node swings. Hence, the distortion added by this transconductor is further reduced. The complete circuit diagram of the opamp with current injection is shown in Fig. 7.8.

7.3.1 Implementation in a First order system

The circuit diagram showing the implementation in a FOS is shown in Fig. 7.9. The output current sunk in by the negative half of the opamp is approximately $\frac{vip}{R} + \frac{op}{R}$. The transconductance of the triode transistors is fixed to $\frac{1}{R}$. The current injection at the output is achieved by applying these voltages to the gates of the transistors Mt1a and Mt3a. A similar approach is followed for the positive half of the opamp. The drain of Mt1-Mt3 have been shorted together in order to decrease the looking in impedance at the drain of the triode transistors. Shorting the nodes increases the effective conductance at the drain and thus reduces the variation of



M1 : 16 (2/0.18)	M5 : 36 (2/0.18)	M10 : 4 (1/0.18)	Mb4, Mb6 : 2 (0.5/0.18)	Mb10 : 4 (2/0.72)	Mt1-Mt3 : 6 (0.24/1)
M2 : 64 (2/0.18)	M6 : 18 (1/0.18)	M11 : 8 (0.5/0.18)	Mb5 : 4 (0.5/0.18)	Mb11 : 2 (2/0.72)	Mt4 : 4 (0.24/1)
M3a : 8 (0.5/0.18)	M7 : 36 (0.5/0.18)	M12 : 8 (2/0.72)	Mb7 : 4 (0.5/0.18)	Mb12 : 2 (0.5/1)	R = 500 kΩ
M3b : 4 (0.5/0.18)	M8 : 36 (2/0.72)	Mb1, Mb3: 2 (2/0.18)	Mb8 : 2 (0.24/2)	Mx1-Mx3 : 12 (1/0.18)	C = 20 fF
M4 : 32 (0.5/0.18)	M9 : 8 (2/0.18)	Mb2 : 4 (2/0.18)	Mb9 : 2 (0.5/0.18)	Mx4 : 8 (1/0.18)	

Figure 7.8: Circuit diagram of the folded cascode opamp with current injection

the triode transistors' transconductance with the input signal.

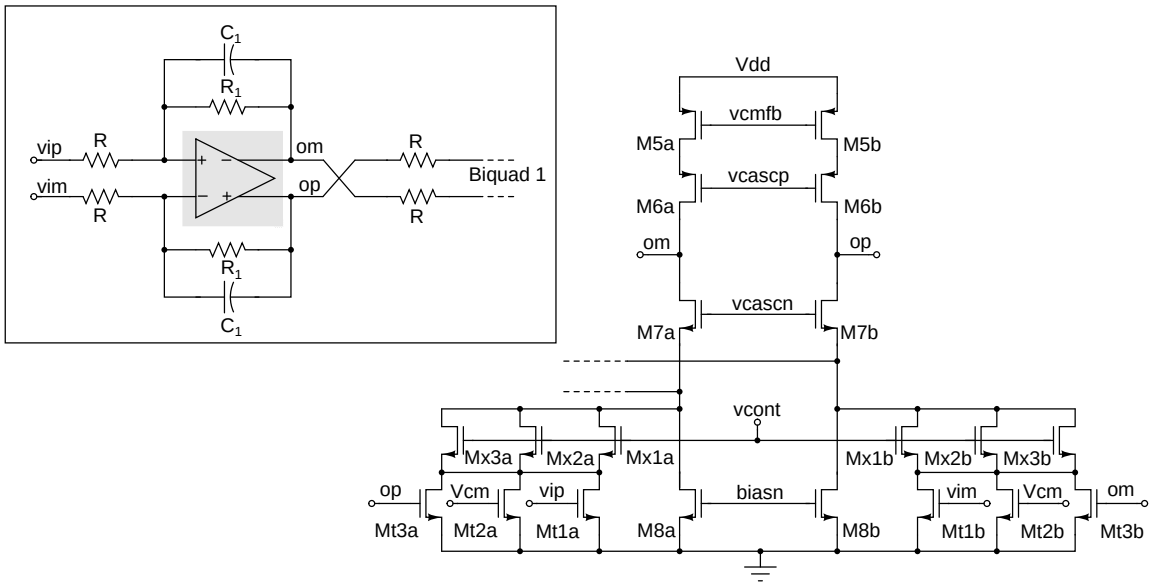


Figure 7.9: Circuit implementation of current injection in FOS

7.3.2 Implementation in Biquad 1

The circuit diagram showing the implementation for the first opamp in BQ1 is shown in Fig. 7.10. The output current sunk in by the negative half of the opamp comprises of three parts and is approximately $\frac{vip}{R}+\frac{op1}{R}+\frac{om}{R}$. The transconductance of the triode transistors is fixed to $\frac{1}{R}$. These signals are applied to the gates of the transconductors Mt1a-Mt3a as before. In this case we short the drains of two transconductors only, namely Mt2 and Mt3. This is more effective compared to the previous case for the biquad because the applied signal swing at the gates of these two transistors are out of phase with each other. The triode transconductor appears as a common source amplifer from the gate to the drain of Mt2, Mt3. Hence, the drain voltage swing is reduced considerably in this case.

Following a similar procedure as before, we find that the output current sunk in by the negative half of the second opamp in BQ1 comprises of three parts and is approximately $\frac{op1}{R}+\frac{op}{R}+\frac{op}{R}$. The circuit diagram is shown in Fig. 7.11.

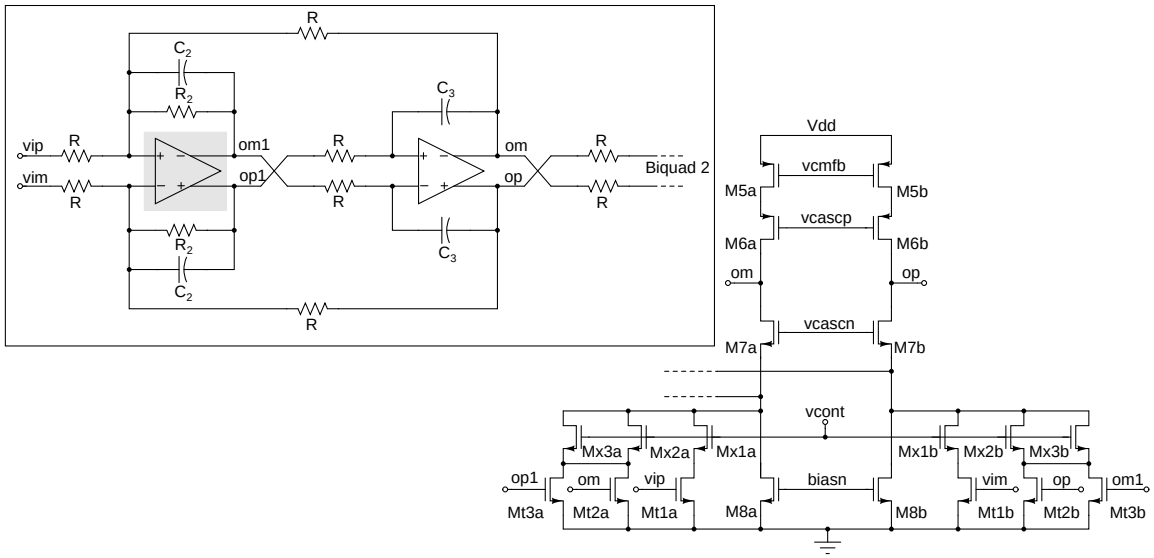


Figure 7.10: Circuit implementation of current injection in first opamp of BQ1

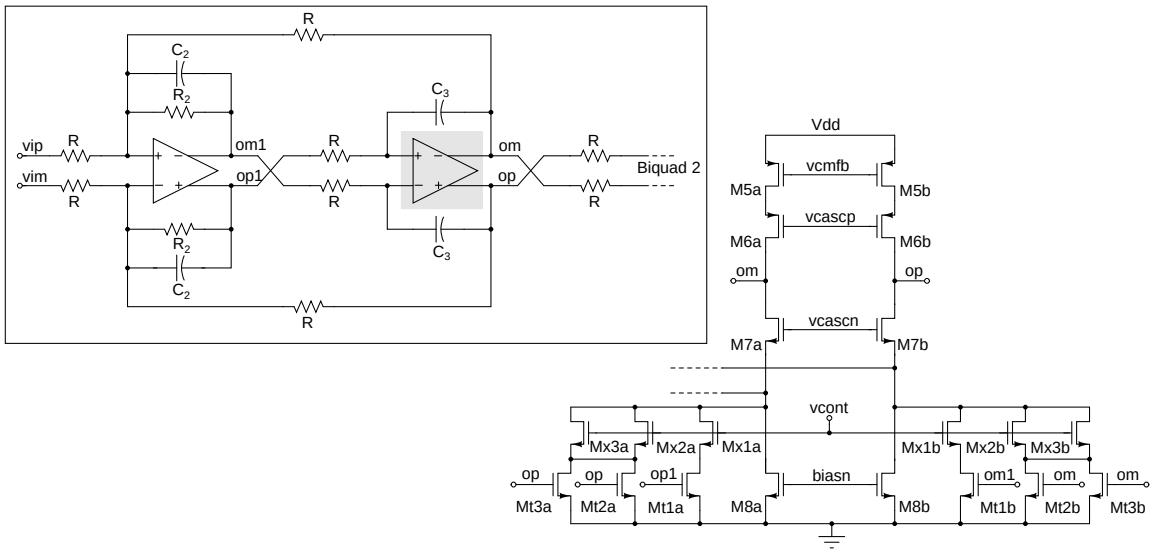


Figure 7.11: Circuit implementation of current injection in second opamp of BQ1

7.3.3 Implementation in Biquad 2

For circuit implementation of BQ2, we follow the same procedure as that for Biquad 1. The implementations for the two opamps in BQ2 are shown in Fig. 7.12 and 7.13.

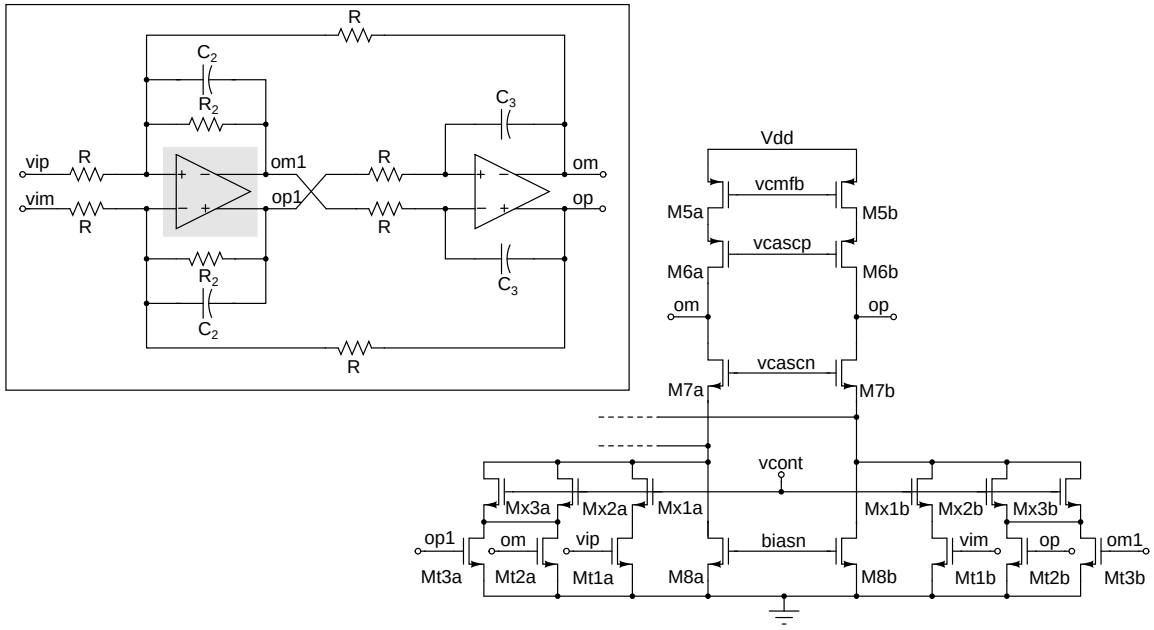


Figure 7.12: Circuit implementation of current injection in first opamp of BQ2

In the implementation above, the transconductance of all the triode transconductors is equal to $\frac{1}{R}$. Hence, the control voltage V_{cont} is the same for all of them. This voltage is generated from a fixed transconductance bias for the triode transconductors and distributed to all the opamps.

7.4 Filter implementation

The filters are implemented as a cascade of FOS, BQ1 and BQ2 sections. The filters are design centered to give the desired filter frequency response. For the filter with current injection, the compensation is done for all stages because the overhead in terms of power is zero. In order to account for RC variations, tuning scheme has been implemented for both filters. The implementation of the tuning

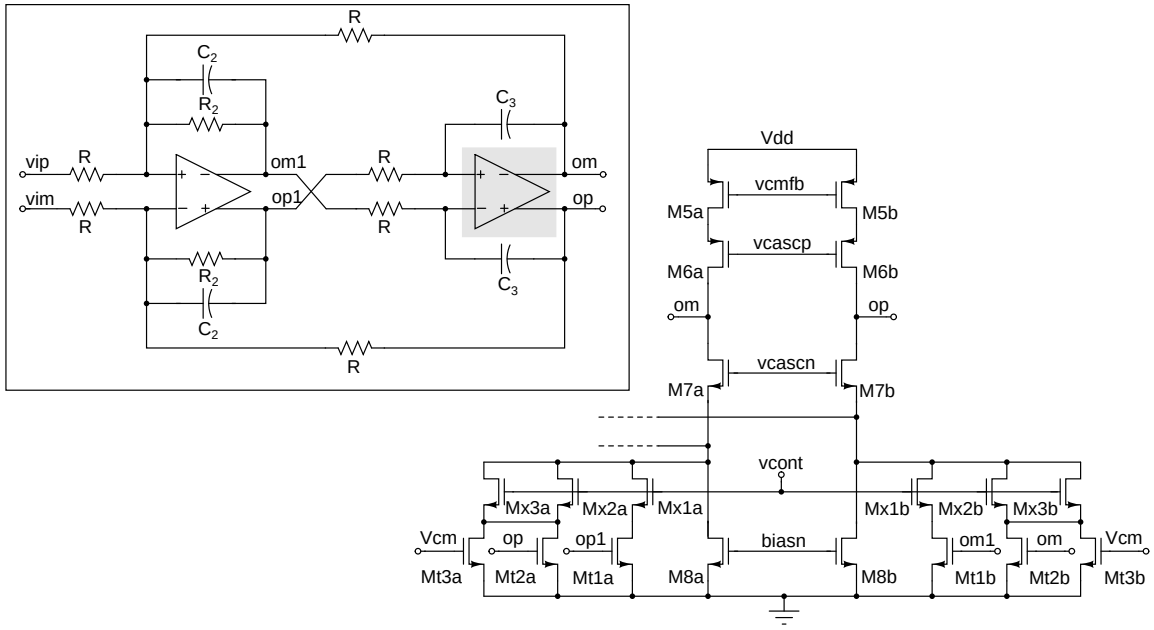


Figure 7.13: Circuit implementation of current injection in second opamp of BQ2

banks for resistors and capacitors is shown in Fig. 7.14. The tuning bank allows for 256 different RC levels spanning the whole process variations possible. The tuning control is manual and is common to both the filters.

The complete filter schematic showing the resistor and capacitor values for the cases without and with current injection is shown in Fig. 7.15. The opamp implementation in both the cases are different. The values of the resistors and capacitors for the filter after design centering are given.

7.5 Fixed transconductance bias

The fixed transconductance bias used in this filter is the same as before. The circuit schematic and design details have already been discussed in Chapter 4, Section 4.5.

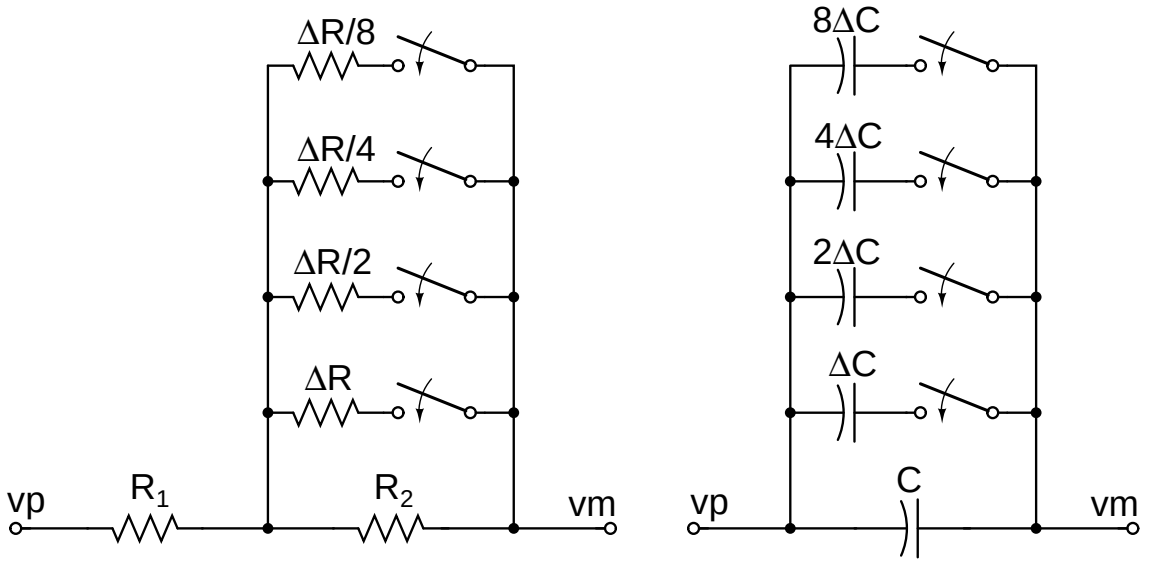
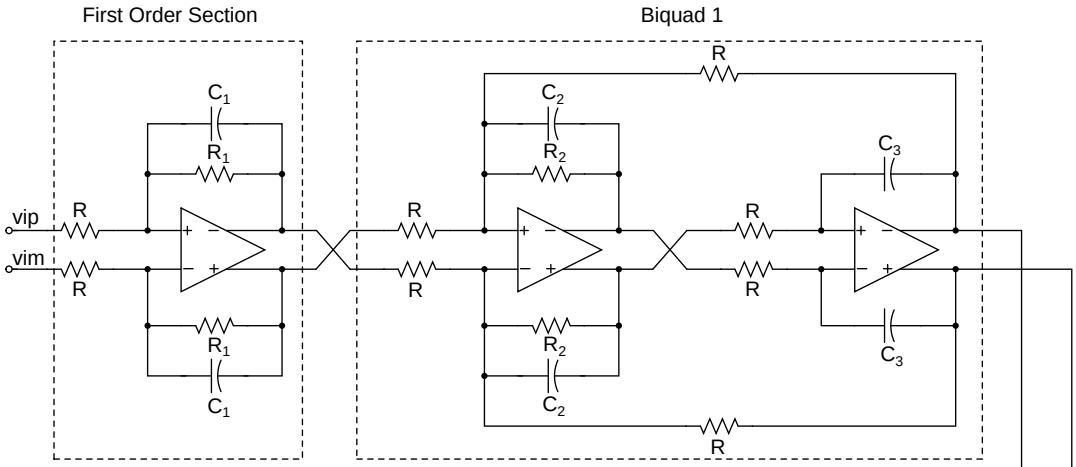


Figure 7.14: Implementation of resistor and capacitor tuning



Without Injection	With Injection
R = 24 kΩ	R = 24 kΩ
R_1 = 28 kΩ	R_1 = 24 kΩ
C_1 = 1 pF	C_1 = 1.1 pF
R_2 = 71 kΩ	R_2 = 56 kΩ
C_2 = 250 fF	C_2 = 271 fF
C_3 = 722 fF	C_3 = 822 fF
R_3 = 133 kΩ	R_3 = 101 kΩ
C_4 = 253 fF	C_4 = 297 fF
C_5 = 307 fF	C_5 = 316 fF

Figure 7.15: Circuit schematic of the filter showing the FOS, BQ1 and BQ2 sections

7.6 Fixed transconductance bias for triode transistors

In order to have a robust mechanism of current compensation, the transconductance of the triode transconductor must be constant with process and temperature variations. The transconductance value must also change with resistance variations of the input resistor R used in the design of the filter. For achieving a fixed transconductance bias, we cannot use the same circuit used for fixing the transconductance of the input differential pairs of the opamps. The circuit discussed before is effective only for fixing the transconductance of transistors operating in saturation. A small incremental input proportional to the required transconductance is applied and compared against a constant current source. For the triode transconductors, the transconductance value depends on the overdrive as well as the drain-source voltage of the transistors. By giving an incremental input to the differential pair in the fixed transconductance bias circuit, the drain-source voltage itself changes. This is because the circuit acts like a common source amplifier with the output at the drain node. Also, simulation results show that the variation with process and temperature is large due to variations in this drain-source voltage. Hence, we need to develop a fixed transconductance bias circuit which will fix the transconductance to the exact value of the resistor R.

We now discuss a new circuit implementation which fixes the transconductance of the triode transistors. Fig. 7.16 shows the circuit diagram of the fixed transconductance bias. To understand the operation, we consider the two halves of the circuit. The circuit on the left half comprising of Mt1 and Mx1 carries a current I in steady state. The circuit in the right half comprising of Mx2 (with similar sizes as Mt1 and Mx1) also carries a current I, but an incremental voltage I_1R is applied to the gate of Mt2. The total current I_y flowing through Mt2 is

$$I_y = f(V_{gs}, V_{ds}) \tag{7.6}$$

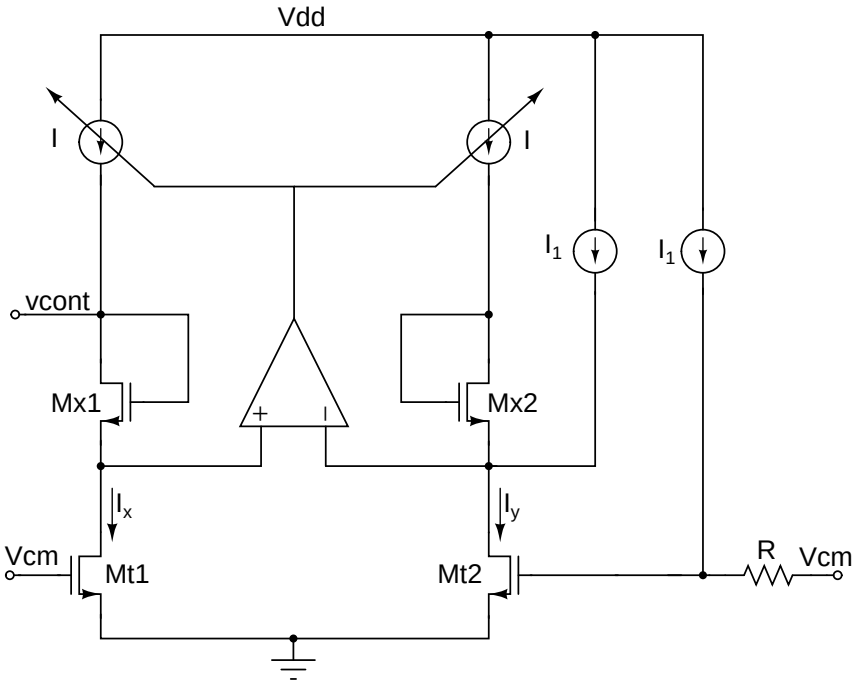


Figure 7.16: Fixed transconductance bias circuit for triode transistors

$$i_y = \frac{\partial I_y}{\partial V_{gs}}.v_{gs} + \frac{\partial I_y}{\partial V_{ds}}.v_{ds} \tag{7.7}$$

The opamp ensures that the drain-source voltages of Mt1 and Mt2 are identical by tweaking the current source I and thus generating the control voltage V_{cont} required for biasing. Hence, we have $v_{ds} = 0$. Hence, from (7.7). we get

$$i_y = \frac{\partial I_y}{\partial V_{gs}}.v_{gs} \tag{7.8}$$

$$= g_{m,Mt2}.v_{gs} \tag{7.9}$$

This incremental current i_y under steady state equals I_1 and $v_{gs} = I_1 R$. Thus, the transconductance of Mt2 ($g_{m,Mt2}$) gets fixed to $1/R$. Since the drain-source voltage of Mt1 and Mt2 are equal, the transconductance of Mt1 is also $1/R$. This R is implemented as an on-chip resistor bank and is connected to the tuning circuitry. As the input resistors of the opamp are tuned, this resistor also gets

changed appropriately.

The opamp used in the Fixed transconductance bias circuit is a folded cascode opamp. The input stage is a PMOS differential pair, so that a low common mode voltage at the gate can be supported. Using such an opamp topology also minimizes offset problems. The complete circuit is impedance scaled by a factor of 3 to save power. Fig. 7.17 shows the complete circuit diagram of the Fixed transconductance bias. The opamp comprises of the transistors M0-M5, M8. The transistors whose transconductance needs to be fixed are M7a and M7b. Capacitor C_b is used in the circuit in order to stabilize the loop. Resistor R and capacitor C serve as a low pass filter and distribute the required control voltage to the rest of the circuitry. Transistors Mb1-Mb6 forms the local bias of the circuit. Simulation results are shown in Fig. 7.18. The variation of transconductance value with process and temperature is less than 0.8% of the nominal value.

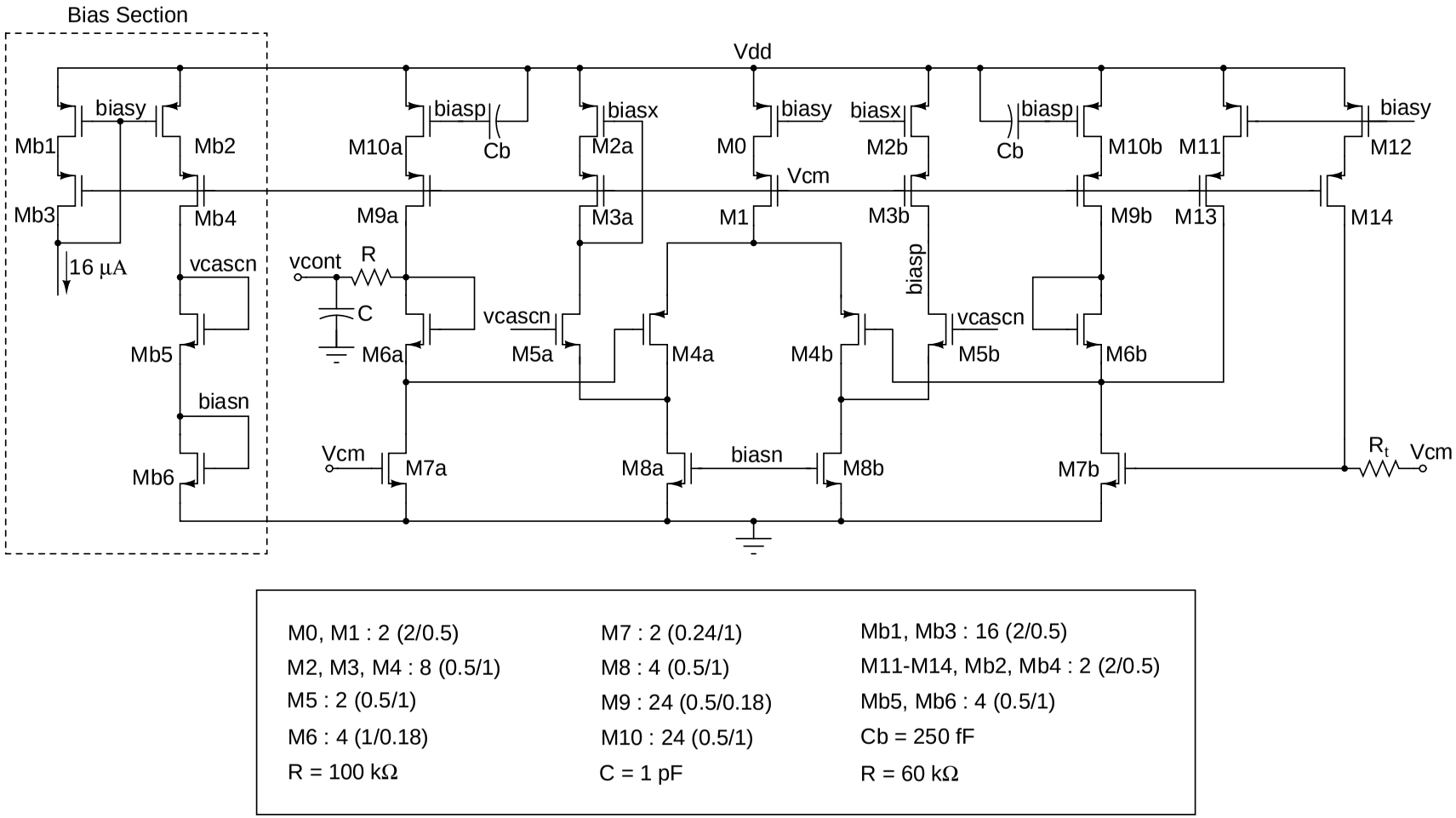
7.7 Bias distribution

The circuit schematic of the bias distribution network is shown in Fig. 7.19.

The current from the fixed transconductance bias circuit is used to bias all the blocks in the filter. Transistors M2a and M2b provide the required fixed transconductance bias current, which is mirrored, replicated and distributed to the different filter blocks using transistors M7 and M8. Transistors M9a and M9b are used to supply the bias current required for the fixed transconductance bias circuitry of triode transconductors.

7.8 Buffer design

The buffer design discussed in Chapter 4, Section 4.7 doesnot satisfy the distortion requirements for the implemented filter with current injection. This is because the improvement in this case is much larger than the filter designed previously.



M0, M1 : 2 (2/0.5)	M7 : 2 (0.24/1)	Mb1, Mb3 : 16 (2/0.5)
M2, M3, M4 : 8 (0.5/1)	M8 : 4 (0.5/1)	M11-M14, Mb2, Mb4 : 2 (2/0.5)
M5 : 2 (0.5/1)	M9 : 24 (0.5/0.18)	Mb5, Mb6 : 4 (0.5/1)
M6 : 4 (1/0.18)	M10 : 24 (0.5/1)	Cb = 250 fF
R = 100 kΩ	C = 1 pF	R = 60 kΩ

Figure 7.17: Complete circuit of the Fixed transconductance bias circuit for triode transistors

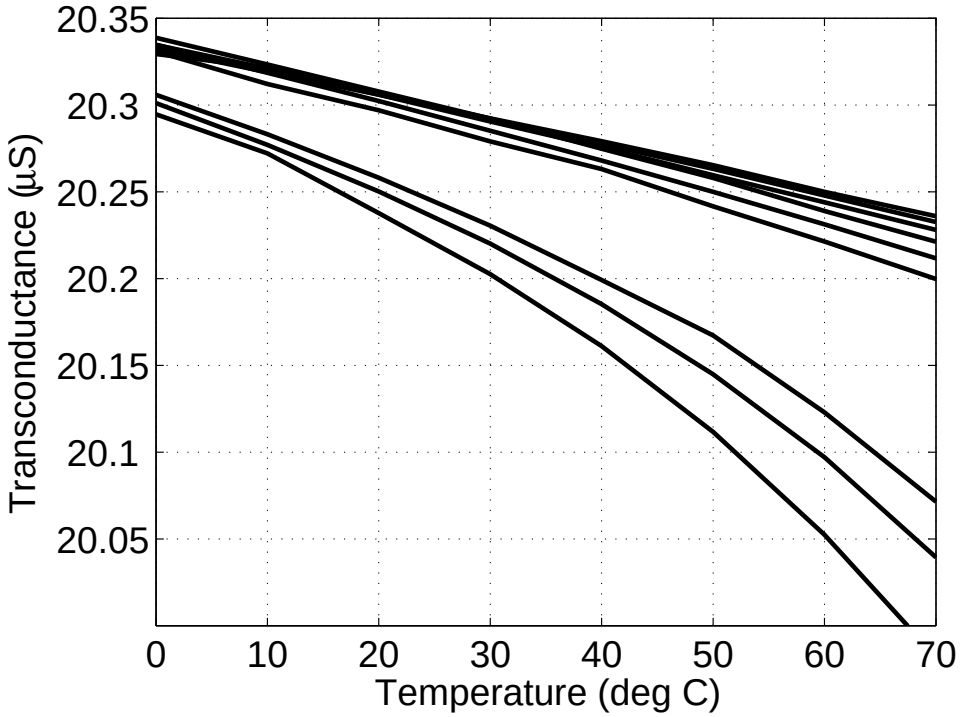


Figure 7.18: Variation of transconductance of triode transistors with process and temperature

Hence, we need to improve the distortion of the buffer. The circuit schematic of the modified buffer is shown in Fig. 7.20.

The distortion of the buffer is contributed by the common drain stage and the transconductor differential pair. In order to improve the distortion contributed by the source follower stage, the current sources are replaced by cascode sources M8 and M9. The sizes of transistors M10a and M10b are modified to increase their transconductance. This helps in increasing the loop gain of the common drain stage, thereby decreasing its distortion. The distortion contribution of the transconductor stage is reduced by varying the attenuating factor. The factor is changed from eight in the previous design to sixteen. In order to keep the output signal current the same, the size of the transistors M4a and M4b are doubled. The rest of the working of the buffer is same as before. Transistors Mb1-Mb10 form the local bias network for the buffer.

On the whole, two buffers are used to characterize the filter. One of them is

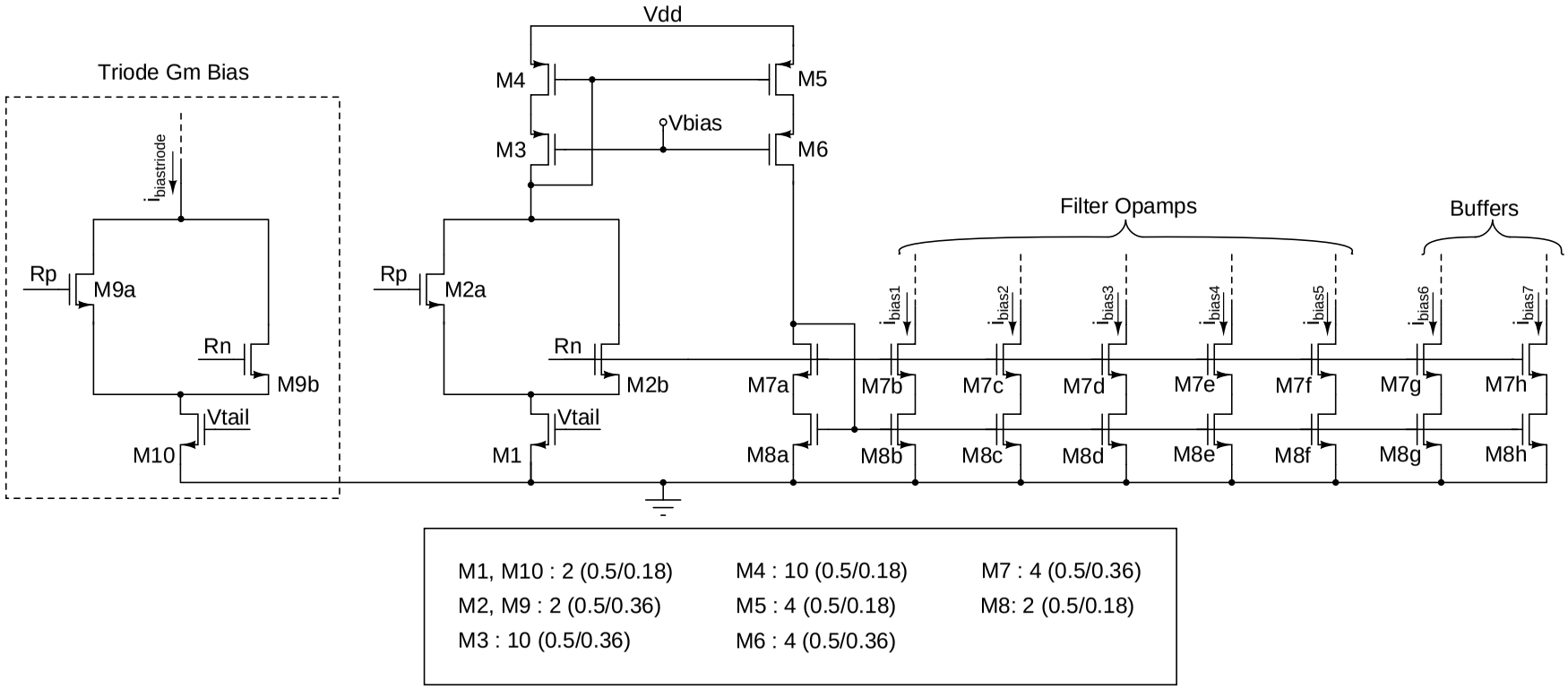
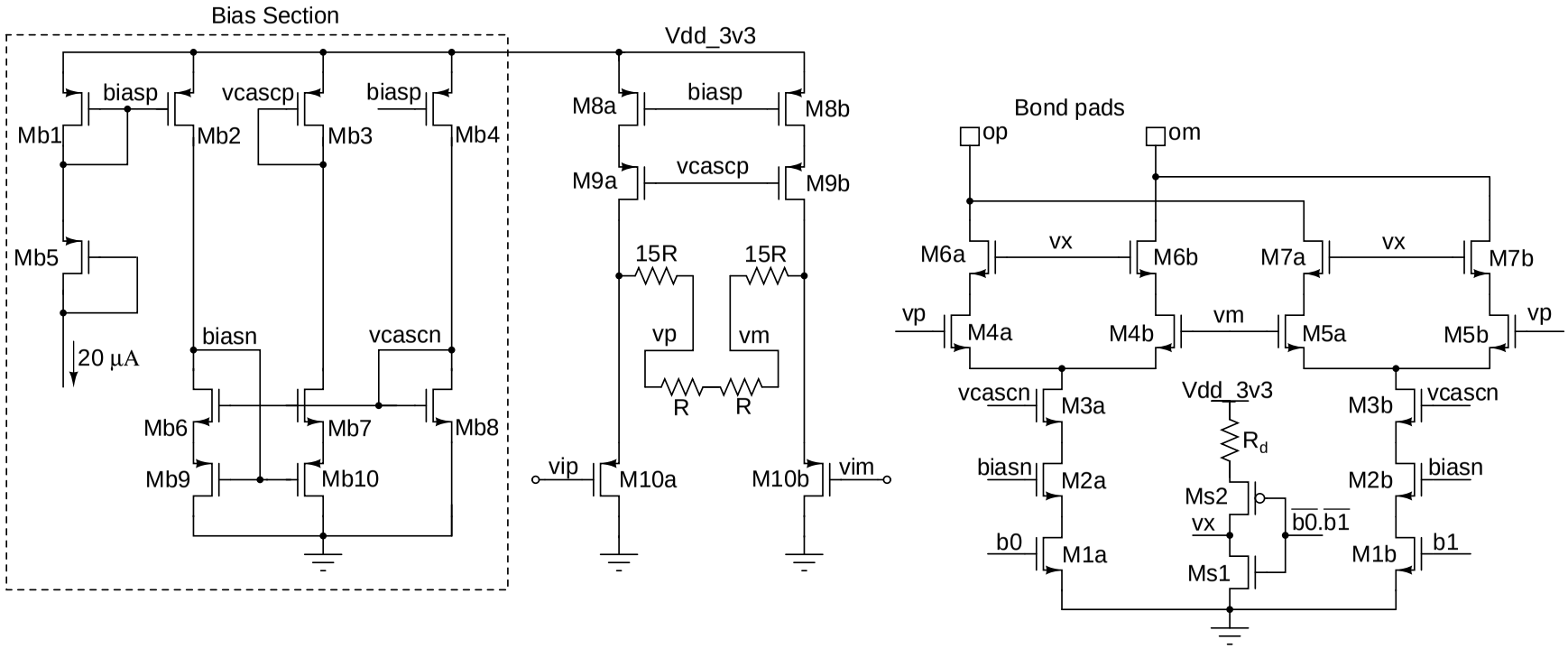


Figure 7.19: Circuit schematic of the bias distribution



M1-M3 : 40 (2/0.34)	M10 : 8 (1/0.68)	Mb6, Mb7, Mb9, Mb10 : 2 (2/0.34)	R = 10 kΩ
M4-M5 : 8 (0.24/0.34)	Mb1, Mb2, Mb4 : 8 (2/0.34)	Mb8 : 2 (0.5/0.4)	R_d = 110 Ω
M6-M7 : 16 (0.5/0.34)	Mb3 : 2 (1/0.34)	Ms1 : 2 (0.5/0.34)	
M8-M9 : 16 (2/0.34)	Mb5 : 16 (2/0.34)	Ms2 : 6 (0.5/0.34)	

Figure 7.20: Circuit schematic of the modified buffer used in the filter

used to measure the direct path and the other the filter path.

7.9 Decoder

In order to control the two buffers used in the chip, a decoder is used to minimize the number of control pins required. Fig. 7.21 and 7.22 shows the circuit description of the decoder used. It is a simple 2×4 decoder which generates states shown in Table 7.1. c0, c1, c2 and c3 are used to control the bits b0 and b1 of the two buffers used.

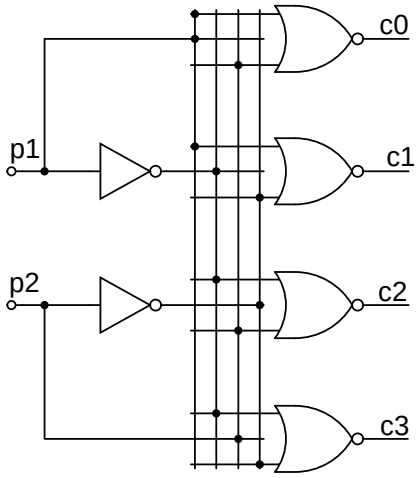


Figure 7.21: Circuit schematic of the decoder

Table 7.1: Truth table of decoder

p1	p2	c0	c1	c2	c3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

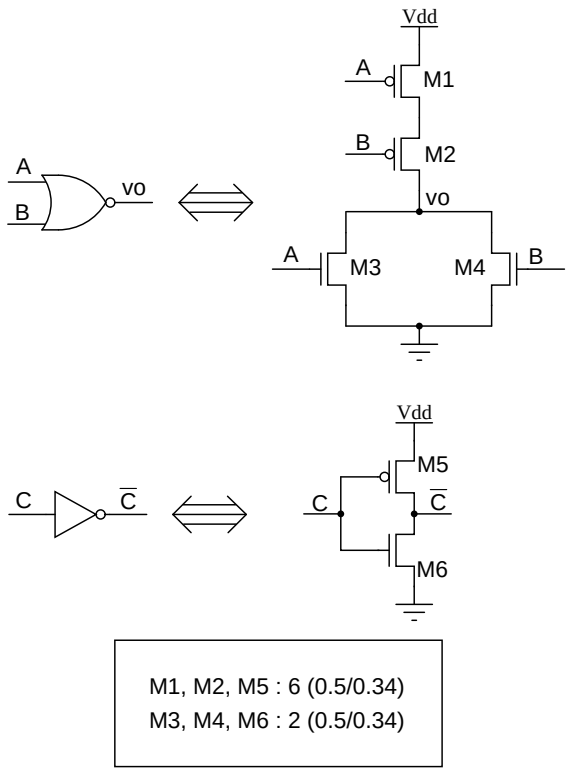


Figure 7.22: Details of CMOS gates used

7.10 Filter Layout

The layout of the filter without current injection is shown in Fig. 7.23. The filter core consists of the FOS, BQ1 and BQ2 sections in cascade. The bias block consists of the fixed transconductance bias and the bias distribution section. The two buffers used in the chip are also shown. The layout of the filter with current injection is shown in Fig. 7.24. The regions bound by the blue rectangle show the triode transconductors used for current injection. The bias section also contains the fixed transconductance bias for triode transistors. Fig. 7.25 shows the bonding diagram of the chip.

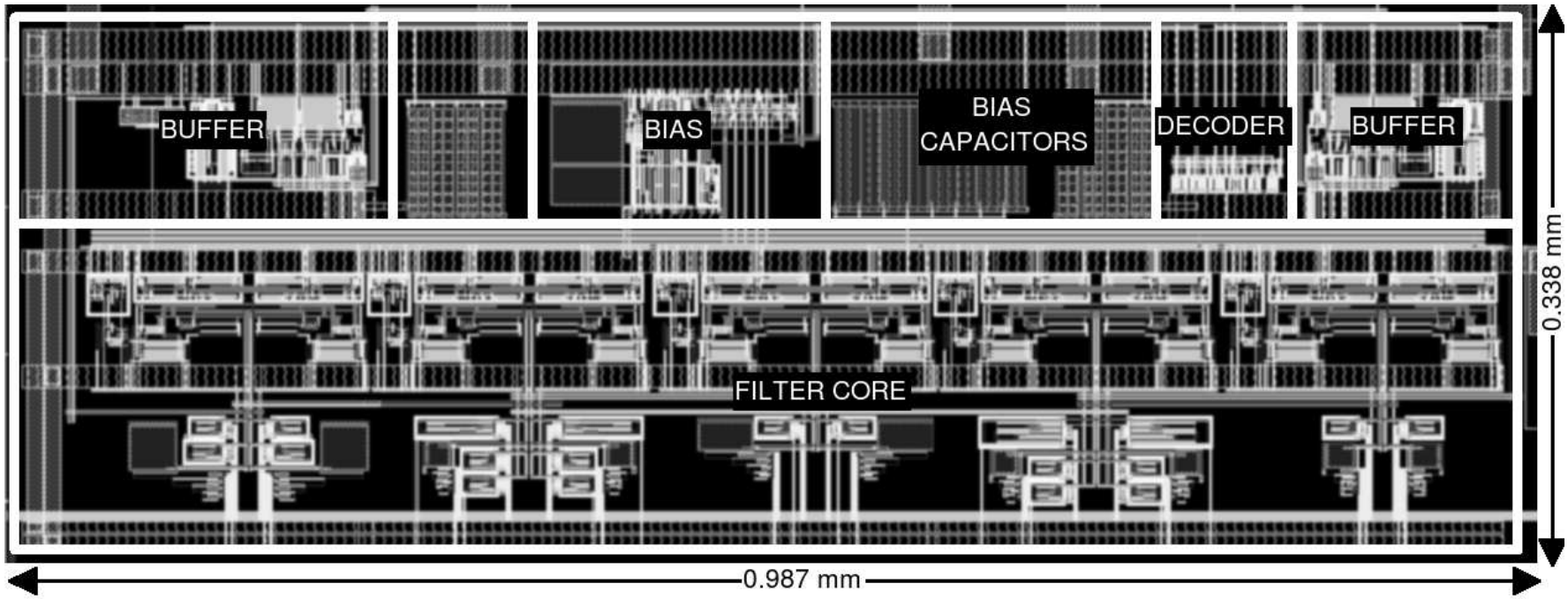


Figure 7.23: Layout of the designed filter without current injection

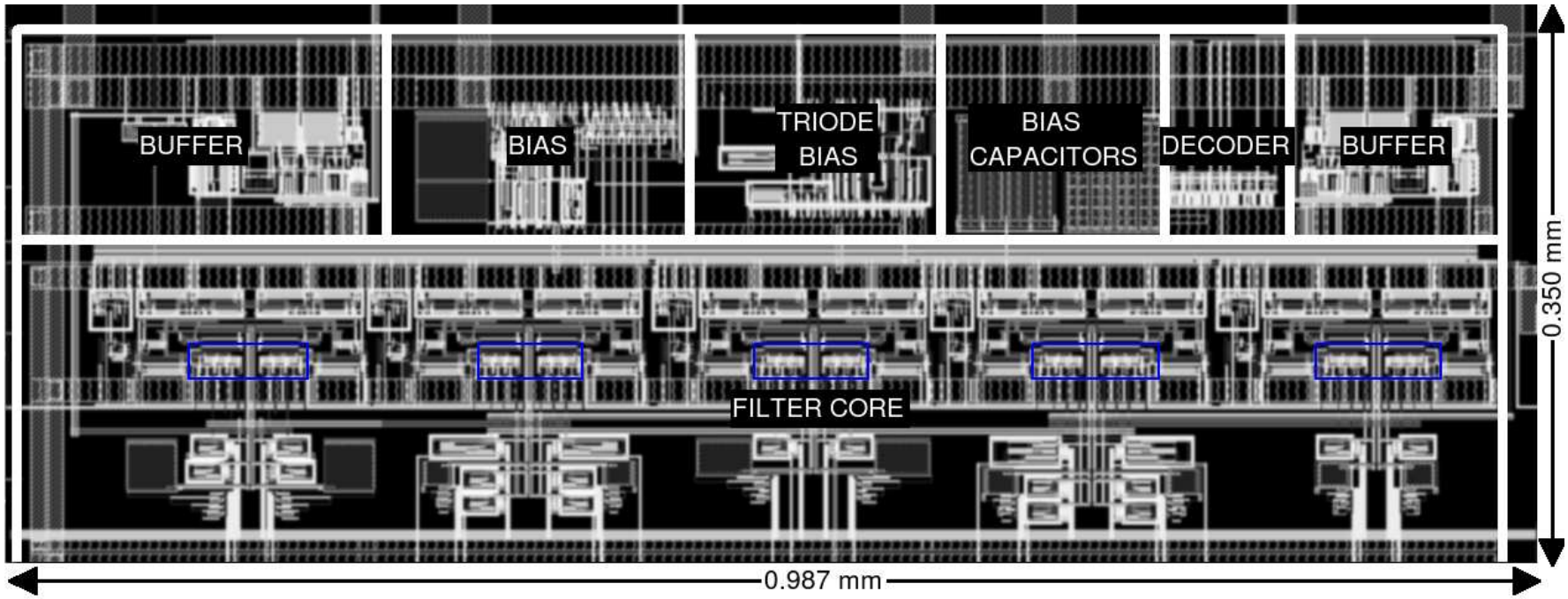


Figure 7.24: Layout of the designed filter with current injection

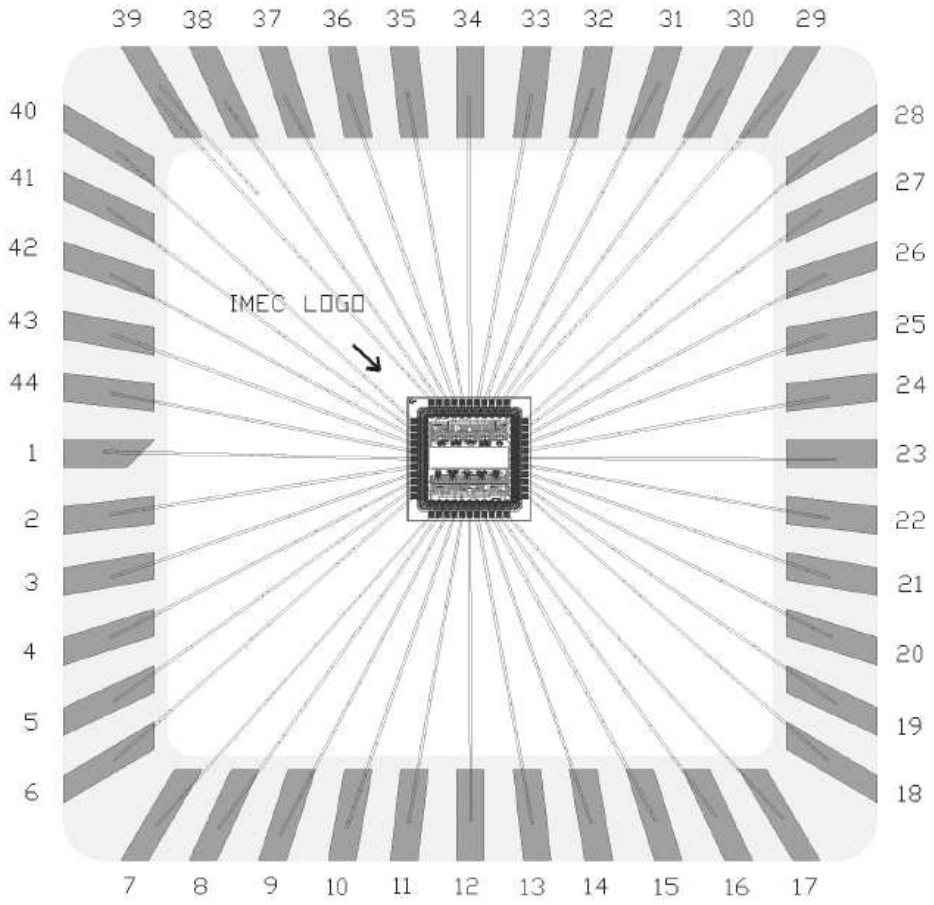


Figure 7.25: Bonding diagram of the designed filter

CHAPTER 8

Simulation Results for Active-RC Chebyshev filter with Current Injection using Triode transconductors

Two fifth order Chebyshev Active-RC filters (without/with injection) with pass-band ripple of 1 dB and bandedge of 20 MHz were implemented in a 0.18 μm CMOS process and fabricated through Europractice program. A 44 pin JLCC was used for packaging the chip. The chip without injection occupies an area of 0.33 mm^2 and that with injection occupies 0.35 mm^2. In this section, we present simulation results for the designed filters.

8.1 Frequency Response

The simulated frequency response of the filter without/with current injection is shown in Fig. 8.1. The bandedge of the filter is 20 MHz. We see that there is a droop in the frequency response near dc due to low opamp gain. With current injection, the gain increases and the response droop reduces.

8.2 Noise

Fig. 8.3 shows the simulated thermal output noise spectral density of the filter without/with current injection. We see that the noise without/with current injection are almost the same. This is because the injected noise current is negligible compared to the inherent noise of the filter. The noise of the filter with current injection is slightly less than that without injection, due to difference in the resistor

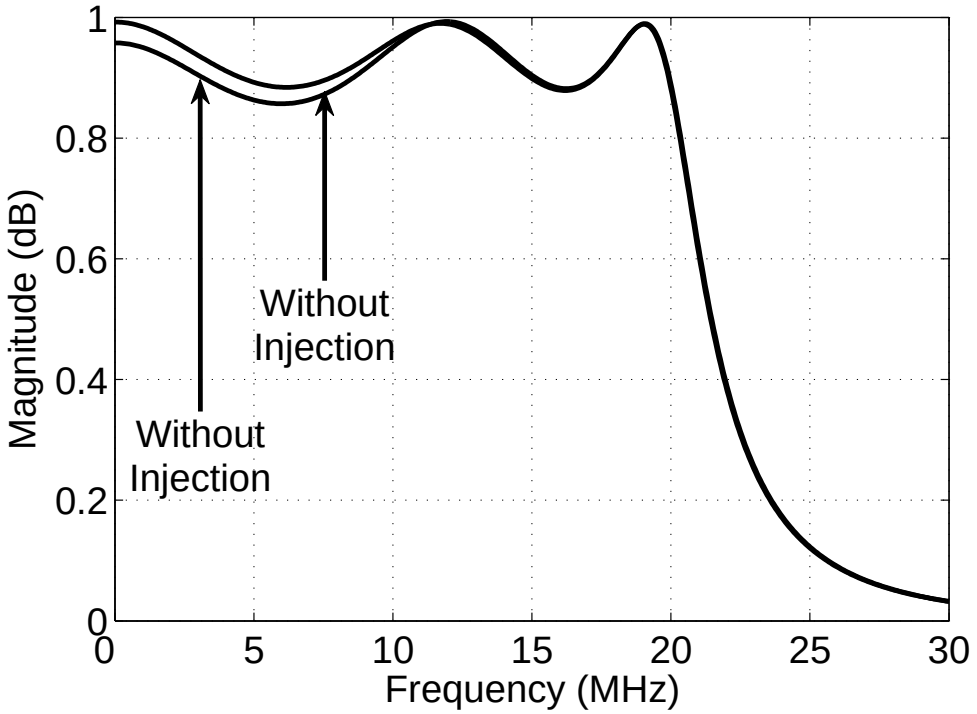


Figure 8.1: Simulated Frequency Response without/with current injection

values. When the ideal filter is replaced with single stage opamps, the response droops. To correct for the response, the Q resistor values are increased. With current injection, the opamp tends towards ideal behaviour. Hence, the response peaks. To revert back to the required response, the Q resistors have to be reduced. Hence, the resistor value with current injection is less than that without injection, contributing to lesser noise.

8.3 Distortion

The distortion of the filter was simulated using IMD measurements. Two tones at $f_0 - 0.2\,\text{MHz}$ and $f_0 + 0.2\,\text{MHz}$ were given as input with f_0 varying from 2 MHz to 48 MHz. Fig. 8.3 shows the IMD simulation for an input differential amplitude of 375 mV per tone. A 512 point FFT of the output waveform was used to calculate the distortion. From the plots, we observe that there is improvement throughout

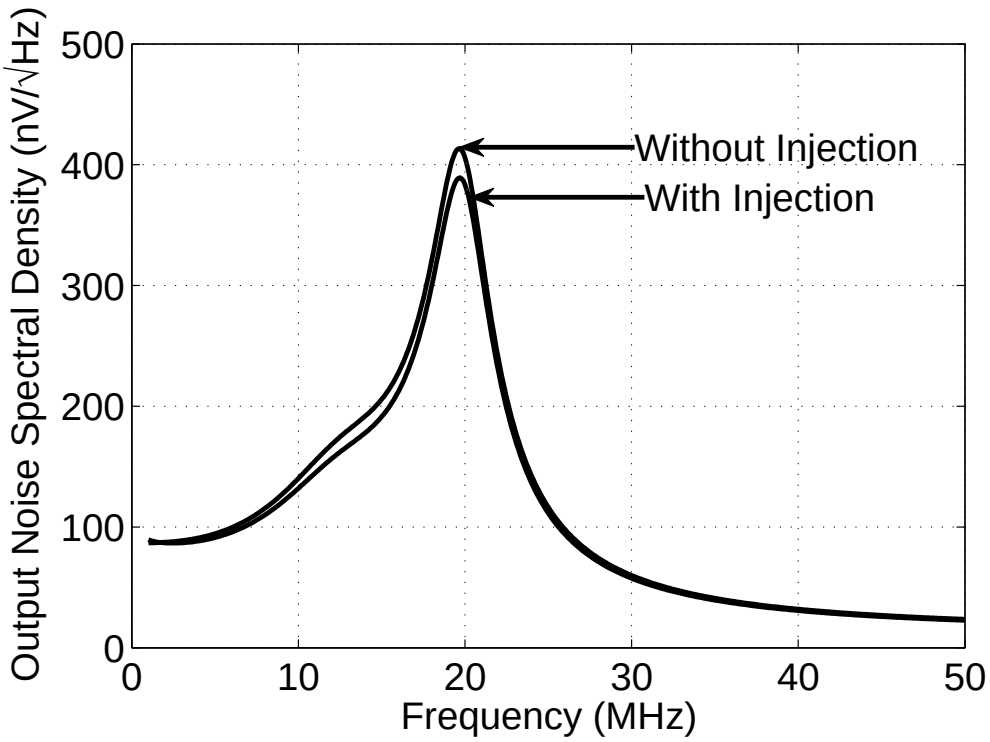


Figure 8.2: Simulated Thermal Output Noise Spectral density

the filter band due to current compensation in all stages of the filter. The improvement is significant with around 14 dB at the point of maximum distortion. Table 8.1 shows the improvement in IMD across MOS and RC corners. We see a good improvement across corners.

To get a good estimate of the amount of improvement in distortion we plot the IIP3 with frequency. The measure of distortion through IIP3 is independent of the input and output amplitudes. Fig. 8.4 shows the variation in IIP3 with frequency. We see that the least IIP3 occurs at the bandedge as expected. We also observe improvement throughout the filter band with an improvement of 10 dB near the bandedge. This shows the efficacy of the technique. Table 8.2 summarizes the filter performance.

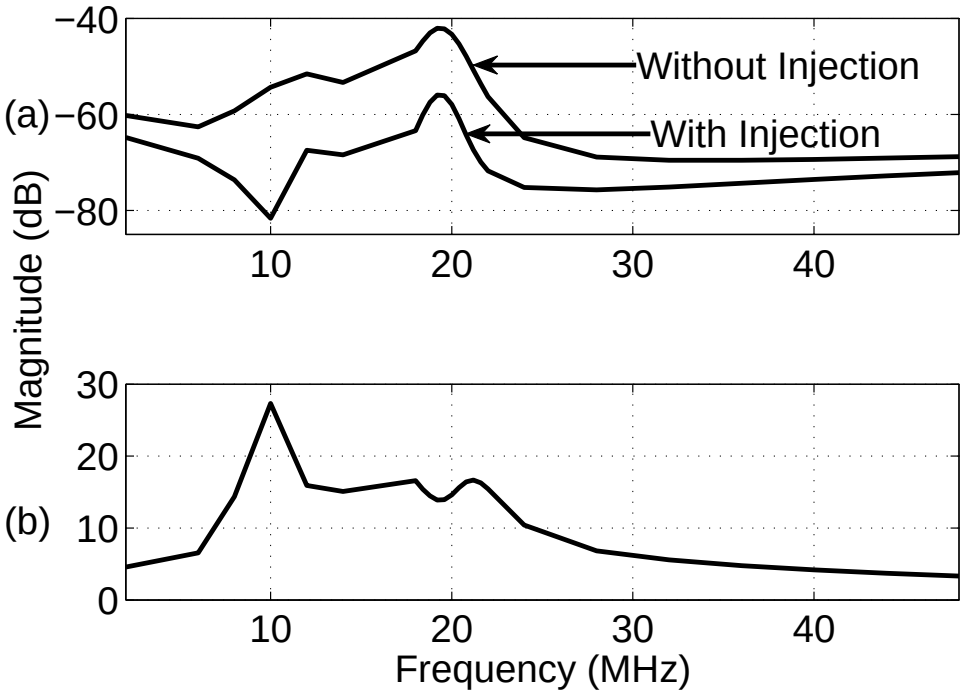


Figure 8.3: (a) IMD as a function of frequency for input differential amplitude 375 mV per tone (b) Improvement in IMD

Table 8.1: Improvement in IMD for input amplitude of 1.5 Vppd

Sl.	Corners (MOS, Res, Cap)	Improvement (dB)
1	ss,typ,typ	14.0
2	tt,typ,typ	16.9
3	ff,typ,typ	15.6
4	tt,min,min	19.0
5	tt,min,typ	19.0
6	tt,min,max	18.0
7	tt,typ,min	15.8
8	tt,typ,typ	16.6
9	tt,typ,max	16.2
10	tt,max,min	15.4
11	tt,max,typ	15.7
12	tt,max,max	15.1

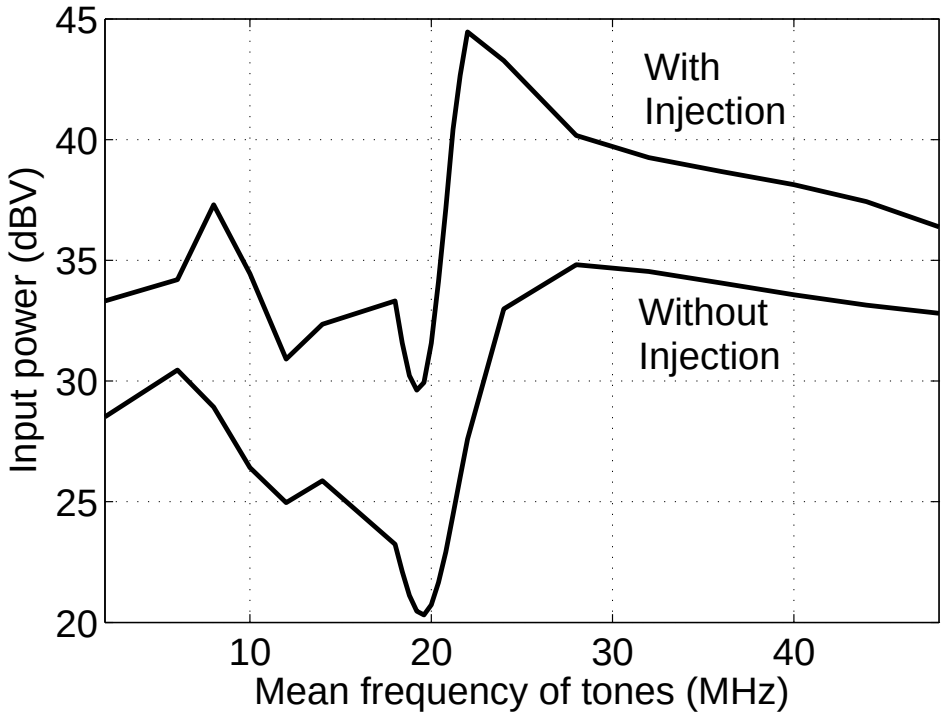


Figure 8.4: IIP3 as a function of frequency

Table 8.2: Summary of Simulation Results

	Without Injection	With Injection
Technology	0.18 μm CMOS	
Filter type	5^{th} order Chebyshev single-stage opamp	
Supply voltage	1.8 V	
Bandwidth	20 MHz	
Active chip area	0.33 mm^2	0.35 mm^2
Power	5.54 mW	5.61 mW
Integrated output thermal noise	1.04 mVrms	0.98 mVrms
IMD test tones at 19.8 MHz and 20.2 MHz with amplitude 375 mV differential per tone		
IMD @ 20.0 MHz	-43.32 dB	-57.94 dB
IIP3 @ 20.0 MHz	7.69 Vrms	26.79 Vrms

CHAPTER 9

Conclusion and Future Work

9.1 Conclusion

A technique for reducing distortion in Active-RC filters using the method of current injection was discussed. The basic idea behind the proposed technique is to reduce the swing at the input of the transconductor and keep it within its linear regime. This technique does not affect the noise of the filter and is also efficient in terms of power. Two variations of the technique had been discussed. Fifth order Chebyshev filters, one using a two-stage Miller compensated opamp and the other using a single-stage folded cascode opamp have been implemented. The second design is highly efficient in terms of distortion, noise and power. Experimental results for the first design show that for an improvement in IIP3 by a factor of 1.9, the extra power requirement for the whole filter is approximately 50%. The same is achieved in the design with 23% extra power.

9.2 Future Work

The implementation of the technique in the second design takes care of all the required performance characteristics of the filter. For the design with the two-stage Miller compensated opamp, the current injection technique can be applied to the first stage of the opamp using the method of the second design. In this way noise of the filter is not affected. To account for process and temperature variations, the compensating capacitor of the opamp must be tunable. Implementing this would be complicated, but the injection at the first stage will certainly help in reducing distortion much more than injection in the second stage alone. In the first design,

the replica biquad has been scaled only by a factor of two. By minimizing the capacitance at the controlling node of the transconductor used for injection, the replica may be further scaled down to save power.

APPENDIX A

PIN DETAILS OF THE CHIP USING TWO-STAGE OPAMP

Pin out details of the chip designed using a two-stage Miller compensated opamp is shown in Fig. A.1. The details and functionality of each pin are given in Table A.1.

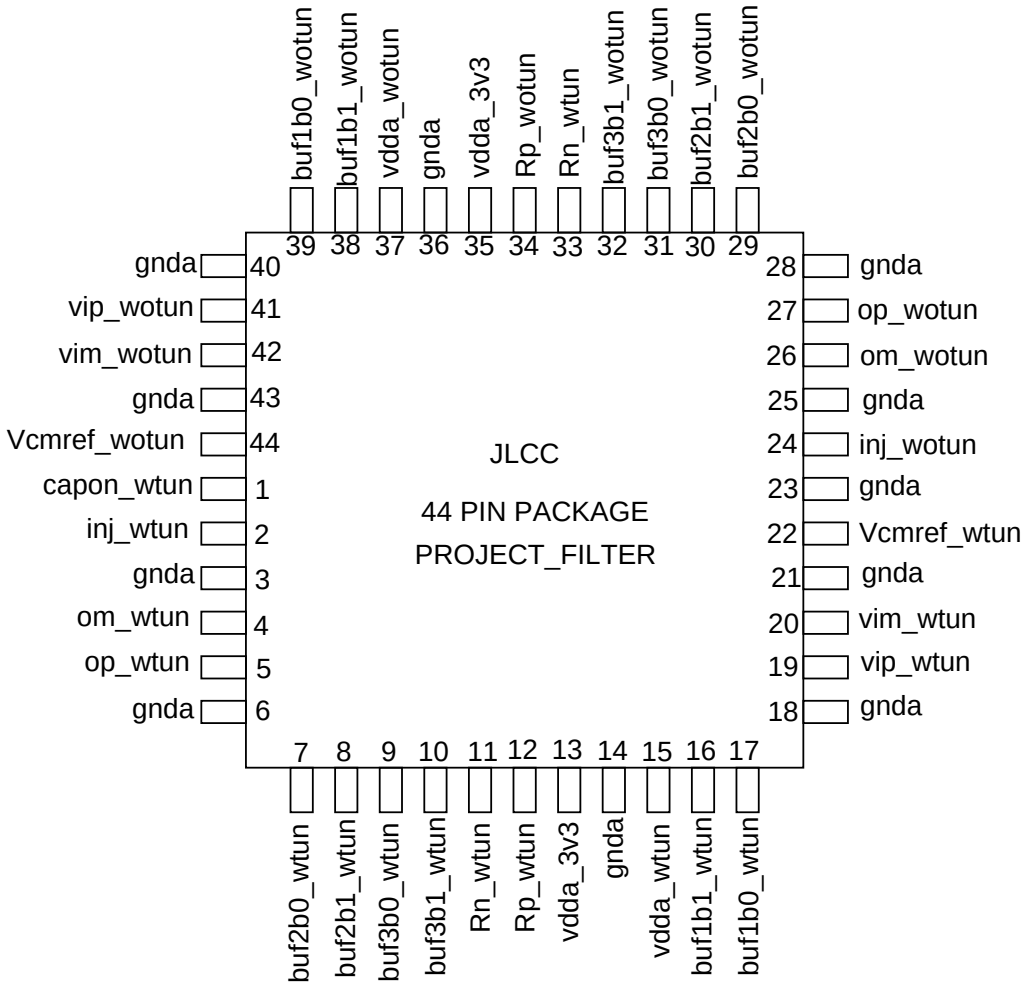


Figure A.1: Pin details of chip designed using two-stage opmap

Table A.1: Functionality of each pin of the chip designed using two-stage opamp

Pin	Name	Functionality
1	cap_wtun	Capacitor tuning control for filter with tuning
2	inj_wtun	Injection control for filter with tuning
3,6,14,18, 21,23,25,28, 36,40,43	gnda	Ground
4, 5	op_wtun, om_wtun	Differential output for filter with tuning
7, 8	buf2b0_wtun, buf2b1_wtun	Control bits of buffer 2 for filter with tuning
9, 10	buf3b0_wtun, buf3b1_wtun	Control bits of buffer 3 for filter with tuning
11, 12	Rp_wtun, Rn_wtun	Terminals for external resistor of fixed transconductance bias for filter with tuning
13, 35	vdda_3v3	3.3 V supply voltage
15	vdda_wtun	1.8 V supply voltage for filter with tuning
16, 17	buf1b1_wtun, buf1b0_wtun	Control bits of buffer 1 for filter with tuning
19, 20	vip_wtun, vim_wtun	Differential input for filter with tuning
22	Vcmref_wtun	Commmon mode input 0.9 V for filter with tuning
24	inj_wotun	Injection control for filter without tuning
26, 27	om_wotun, op_wotun	Differential output for filter without tuning
29, 30	buf2b0_wotun, buf2b1_wotun	Control bits of buffer 2 for filter without tuning
31, 32	buf3b0_wotun, buf3b1_wotun	Control bits of buffer 3 for filter without tuning
33, 34	Rn_wotun, Rp_wotun	Terminals for external resistor of fixed transconductance bias for filter without tuning
37	vdda_wotun	1.8 V supply voltage for filter without tuning
38, 39	buf1b1_wotun, buf1b0_wotun	Control bits of buffer 1 for filter without tuning
41, 42	vip_wotun, vim_wotun	Differential input for filter without tuning
44	Vcmref_wotun	Commmon mode input 0.9 V for filter without tuning

APPENDIX B

PIN DETAILS OF THE CHIP USING SINGLE-STAGE OPAMP

Pin out details of the chip designed using a single-stage Folded cascode opamp is shown in Fig. B.1. The details and functionality of each pin are given in Table B.1.

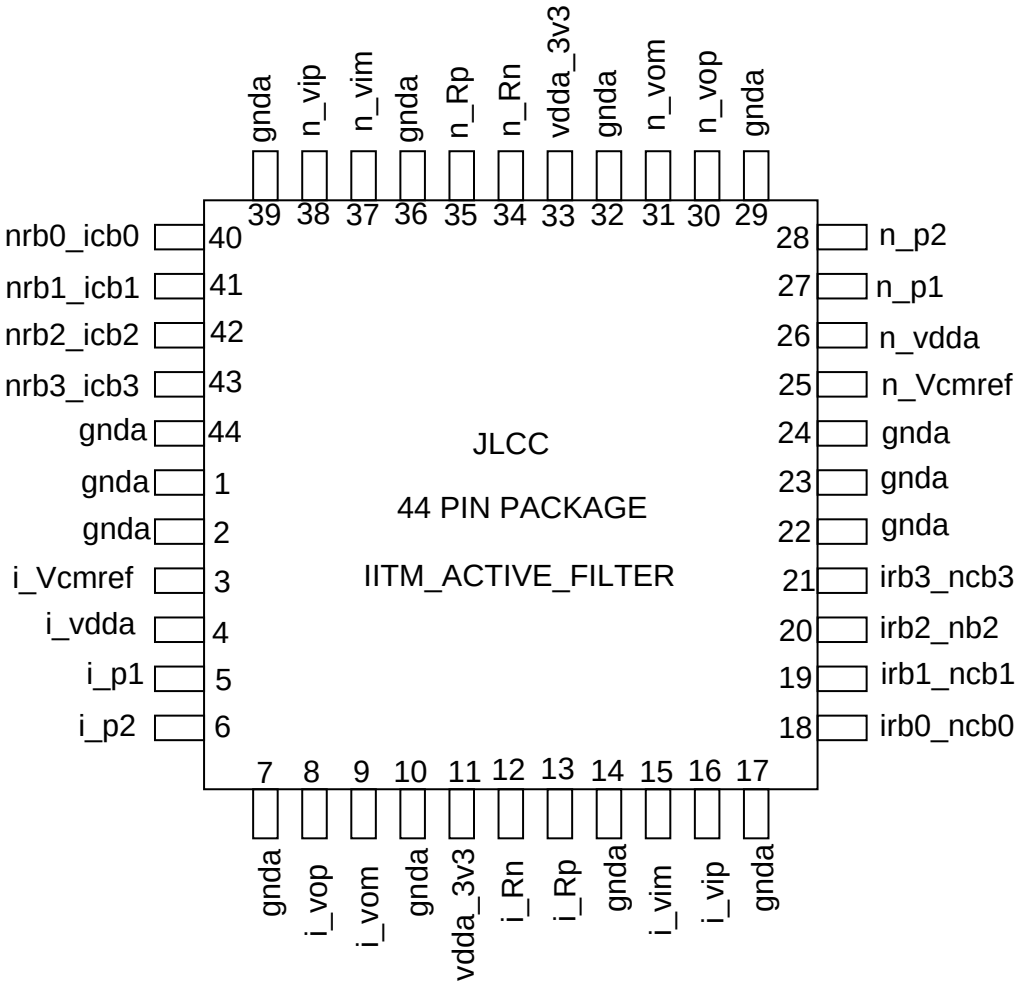


Figure B.1: Pin details of chip designed using single-stage opmap

Table B.1: Functionality of each pin of the chip designed using two-stage opamp

Pin	Name	Functionality
1,2,7,10, 14,17,22,23, 24,29,32,36, 39,44	gnda	Ground
3	i_Vcmref	Commmon mode input 0.9 V for filter with injection
4	i_vdda	1.8 V supply voltage for filter with injection
5, 6	i_p1, i_p2	Control bits of decoder for filter with injection
8, 9	i_vop, i_vom	Differential output for filter with injection
11, 33	vdda_3v3	3.3 V supply voltage
12, 13	i_Rn, i_Rp	Terminals for external resistor of fixed transconductance bias for filter with injection
15, 16	i_vim, i_vip	Differential input for filter with injection
18, 19, 20, 21	irb0_ncb0,irb1_ncb1, irb2_ncb2,irb3_ncb3	Control bits for resistive tuning for filter with injection, capacitive tuning for filter without injection
25	n_Vcmref	Commmon mode input 0.9 V for filter without injection
26	n_vdda	1.8 V supply voltage for filter without injection
27, 28	n_p1, n_p2	Control bits of decoder for filter without injection
30, 31	n_vop, n_vom	Differential output for filter without injection
34, 35	n_Rn, n_Rp	Terminals for external resistor of fixed transconductance bias for filter without injection
37, 38	n_vim, n_vip	Differential input for filter without injection
40, 41, 42, 43	nrb0_icb0,nrb1_icb1, nrb2_icb2,nrb3_icb3	Control bits for resistive tuning for filter without injection, capacitive tuning for filter with injection

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