Design of a Decimator and a Delta Sigma Modulator for Audio Bandwidth

A THESIS

submitted by

P. SHANKAR

for the award of the degree

of

MASTER OF SCIENCE

(by Research)

Department Of Electrical Engineering

Indian Institute of Technology Madras, India

November 2011

CERTIFICATE

This is to certify that the thesis titled **Design of a Decimator and a Delta Sigma Modulator for Audio Bandwidth**, submitted by **P. Shankar**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Research Advisor
Associate Professor
Dept. of Electrical Engineering
IIT Madras
Chennai 600 036

Place: Chennai

Date:

ACKNOWLEDGEMENTS

காலத்தி னாற்செய்த நன்றி சிறிதெனினும்
ஞாலத்தின் மாணப் பெரிது.

திருக்குறள் : 102, அதிகாரம் : செய்ந்நன்றி அறிதல்

A timely help and support given by someone is of earthly value regardless of how small the help is. I take this as an opportunity to thank and acknowledge the people around me who helped me in numerous occasions throughout my life.

P. Shankar

உள்ளுவ தெல்லாம் உயர்வுள்ளல் மற்றது
தள்ளினும் தள்ளாமை நீர்த்து.
திருக்குறள் : 66, அதிகாரம் : ஊக்கமுடைமை

Let the aim, thoughts and actions be strong and lofty. The virtue of them stands irrespective of their failures.

ABSTRACT

This work explores the design of a decimator and a Delta Sigma $(\Delta\Sigma)$ modulator for audio bandwidths. These are the essential components of the front end of a digital audio system. The first part of the work explores the design of a low power decimator and the second part of the work involves with the design of a very high resolution $\Delta\Sigma$ modulator.

A decimator for a low power $(90\,\mu\text{W})$ $\Delta\Sigma$ modulator [1] with 24 kHz bandwidth and an in-band resolution of 16 bits is designed in a 1.8 V, 0.18 μm CMOS process. To achieve a low power consumption comparable to that of the modulator, various optimizations like retiming of registers, canonical signed digits (CSD) encoding for tap weights of the filters, polyphase implementation of the filters and optimal selection of data path width are employed. The decimator occupies an area of 0.46 mm^2 and consumes a power of $100\,\mu$W from a supply of 1.8 V and is operational down to a reduced supply of 0.9 V.

A high resolution continuous-time $\Delta\Sigma$ modulator targeting a resolution of 18 bits (108 dB SNR) in audio bandwidth (20 Hz-24 kHz) is designed in a 1.8 V, 0.18 μm CMOS process. The resolution of the internal quantizer is 4 bit and the modulator runs at the over-sampled frequency of 3.072 MHz. The modulator is designed for an SNR of 108 dB and the simulated SQNR is in excess of 115 dB. The modulator occupies an area of 0.89 mm^2 and consumes a current of $540\,\mu$A from a supply of 1.8 V. The measured idle channel in-band integrated noise is $6.5\,\mu\text{V}_{rms}$ and the modulator is stable up to -0.7 dBFS.

TABLE OF CONTENTS

LIST OF TABLES

ix

LIST OF FIGURES

ABBREVIATIONS

ADC   Analog to Digital Converter

CAD   Computer Aided Design

CIFB   Cascade of Integrators Feedback

CIFF   Cascade of Integrators Feed Forward

CMOS   Complementary Metal Oxide Semiconductor

CSD   Canonical Signed Digits

CTDSM   Continuous-Time Delta Sigma Modulator

CTS   Clock Tree Synthesis

DAC   Digital to Analog Converter

DEM   Dynamic Element Matching

DNL   Differential Non Linearity

DR   Dynamic Range

DSP   Digital Signal Processor

DWA   Data Weighted Averaging

FIR   Finite Impulse Response

FPGA   Field Programmable Gate Array

HDL   Hardware Description Language

INL   Integral Non Linearity

LSB   Least Significant Bit

MOSFET   Metal Oxide Semiconductor Field Effect Transistor

MSA   Maximum Stable Amplitude

NRZ   Non Return to Zero

OBG   Out of Band Gain

OSR	Oversampling Ratio
Op-amp	Operational Amplifier
PSD	Power Spectral Density
PCB	Printed Circuit Board
RTL	Register Transfer Level
RZ	Return to Zero
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
SoC	System on Chip
UGF	Unity Gain Frequency
VCD	Value Change Dump

CHAPTER 1

Introduction

There has been a huge emphasis on System on a Chip (SoC) designs over the last decade. In SoCs, all components of an electronic system are integrated into a single chip. E.g. Mobile phone, personal media players, routers. Data and signal processing in such a system is mostly digital in nature. Digital signals are immune to noise, can be stored easily and are easier for processing. A typical SoC contains a core Digital Signal Processor (DSP) for digital data/signal processing, memory blocks to store data, phase locked loops to control timing and data converters (Analog to digital converters, ADCs, and digital to analog converters, DACs) to interface with the real world.

An ADC is characterized by its resolution, speed and power. The design described in this thesis lays emphasis on high resolution and low power. High resolution data converters are used in seismic monitoring, high fidelity audio, high accuracy instrumentation like strain gauges, pressure sensors. $\Delta\Sigma$ ADCs can resolve signals as high as 20 bits in audio bandwidths. $\Delta\Sigma$ ADCs are a class of oversampled converters wherein high resolution is obtained by virtue of oversampling and negative feedback that shapes the quantization noise out of the signal band. A $\Delta\Sigma$ modulator encodes the analog signal with a smaller number of bits (1-4) at the oversampled rate. A decimator (decimation filter) is required to remove the out-of-band noise to a sufficient level and achieve the full resolution at the Nyquist rate of the signal.

This thesis aims at building the components of a $\Delta\Sigma$ data conversion system for audio bandwidth with a low power consumption.

Very low power (90 μW), high resolution (15 bit) $\Delta\Sigma$ modulators for digital audio have already been proposed in [1][2]. This necessitates a decimator with a correspondingly low power in order to realize a low power analog to digital data conversion system.

The first part of the thesis deals with the design of a low power decimator for a power optimized continuous-time $\Delta\Sigma$ modulator for digital audio. The second part of the thesis deals with the design of a very high resolution, 18 bit (108 dB SNR), continuous-time $\Delta\Sigma$ modulator in the bandwidth 20 Hz - 24 kHz.

1.1   Organization of the thesis

Chapters 2 - 5 form the first part of the thesis about the decimator.

Chapter 2 gives a brief introduction to the concepts of decimation and the design targets for the decimator.

Chapter 3 describes the architecture of the decimator and contains the description of various blocks in the decimator.

Chapter 4 gives information about the digital synthesis of the decimator using standard cells and CAD tools. The simulation results are given in this chapter.

Chapter 5 contains results from testing of the fabricated decimator chip and concludes the first part.

Chapters 6 - 11 form the second part of the thesis about the design of a 18 bit $\Delta\Sigma$ modulator.

Chapter 6 contains a brief introduction on continuous-time $\Delta\Sigma$ modulation and its implementation issues. It is then followed by the description of the targeted design and the system level design details.

Chapter 7 describes the architecture and design of the continuous-time loop filter of the modulator.

Chapter 8 describes the design of the four bit internal flash ADC and generation of multiphase clocks for the ADC.

Chapter 9 contains the design of the feedback DAC and a dynamic element matching algorithm that fixes the effect of mismatch between DAC unit elements.

Chapter 10 shows the details of the fabricated chip and top level simulation results.

Chapter 11 gives the measured results from the fabricated $\Delta\Sigma$ modulator chip and concludes the design.

Chapter 12 draws some conclusions from this work.

CHAPTER 2

Introduction to decimators

2.1 $\Delta\Sigma$ modulation

$\Delta\Sigma$ modulators are a class of data converters wherein the signal is oversampled and the quantizer is placed inside a negative feedback loop. The factor by which the sampling frequency (f_s) is greater than the Nyquist rate of the signal (f_{nyq}) is termed as oversampling ratio, OSR=$\dfrac{f_s}{f_{nyq}}$. Figure 2.1 shows the block diagram of a discrete-time $\Delta\Sigma$ modulator.
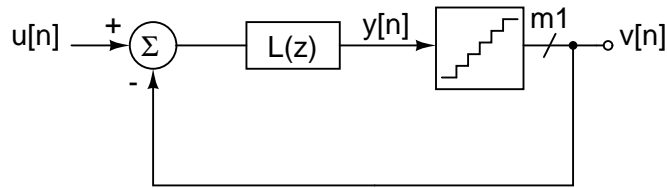
Figure 2.1: Block diagram of a discrete-time $\Delta\Sigma$ modulator.

A continuous-time $\Delta\Sigma$ modulator (CTDSM) employs a continuous-time loop filter and the sampling is done within the loop. The loop filter also behaves as an anti-aliasing filter [3]. Figure 2.2(a) shows the block diagram of a continuous-time $\Delta\Sigma$ modulator. The quantizer is modelled as an additive noise source at the input of the quantizer.
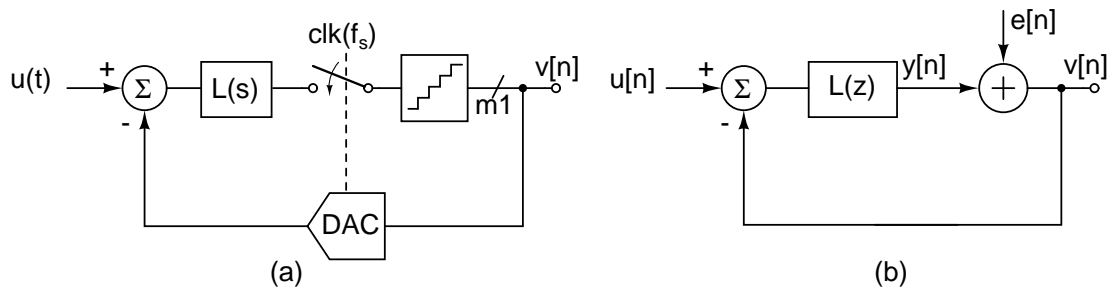
Figure 2.2: CTDSM (a) Block diagram, (b) Discrete time equivalent with additive quantization noise model.

Figure 2.2(b) shows the additive noise equivalent. The quantization noise is assumed to be white and possess a uniform distribution. Denoting the quantization noise by $e[n]$, the input signal by $u[n]$ and the output signal by $v[n]$, the transfer function from input to the output of the quantizer is written as

$$
\begin{aligned}
V(z) &= \frac{L(z)}{1 + L(z)} \times U(z) + \frac{1}{1 + L(z)} \times E(z) & (2.1) \\
&= \text{STF} \times U(z) + \text{NTF} \times E(z) & (2.2)
\end{aligned}
$$

where STF (Signal transfer function) denotes the transfer from the input signal to the modulator output. NTF (Noise Transfer function) denotes the transfer function from the quantization noise to the modulator output. They are expressed as

$$
\begin{aligned}
\text{STF}(z) &= \frac{V(z)}{U(z)} = \frac{L(z)}{1 + L(z)} & (2.3) \\
\text{NTF}(z) &= \frac{V(z)}{E(z)} = \frac{1}{1 + L(z)} & (2.4)
\end{aligned}
$$

Usually a coarse quantizer of 1 to 4 bits resolution is used. The order of the modulator is same as the order of the loop filter. The NTF is designed to shape the quantization noise out of the signal band by appropriately choosing the loop filter. A typical spectrum of the output of a $\Delta\Sigma$ modulator in response to a sine wave input is shown in Figure 2.3. The quantization noise is high pass shaped by the loop filter. The in-band signal to noise ratio (SNR) of the spectrum is 118 dB. Higher order modulators and higher quantizer resolutions are used to obtain higher resolution for $\Delta\Sigma$ modulators [3]. The design of a $\Delta\Sigma$ modulator is given in the second part of this thesis from Chapter 6.
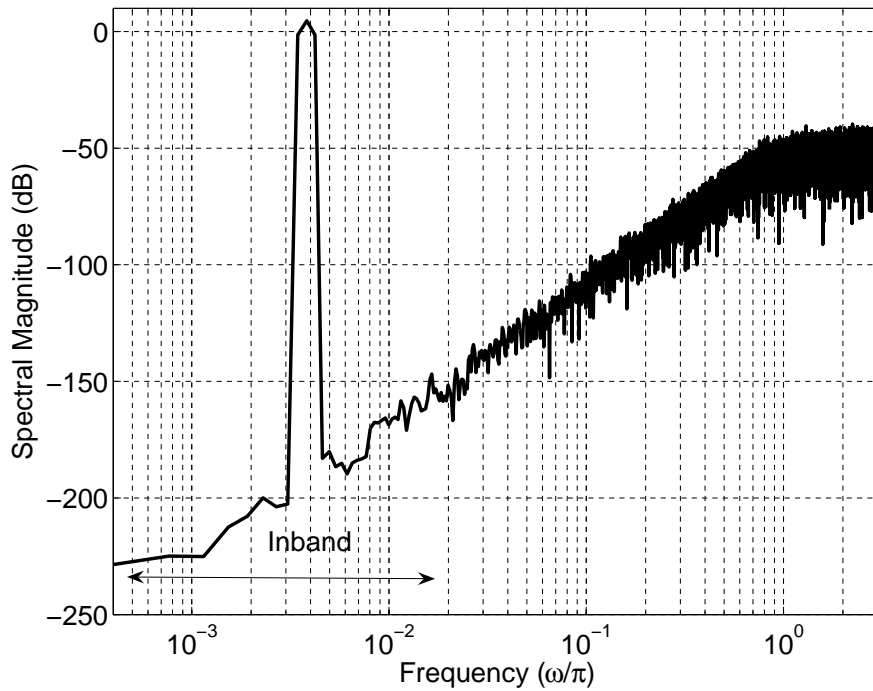
Figure 2.3: Spectrum of a $\Delta\Sigma$ modulator, Order: 3, OSR: 64.

2.2 Overview of decimation

2.2.1 Downsampling

Downsampling is the process of reduction in the sampling rate of a discrete-time signal by dropping samples. Downsampling by a factor of M implies that out of M consecutive samples, $M-1$ samples are discarded and one sample is retained. Correspondingly the sampling rate of the downsampled signal changes from f_s to f_s/M. This is shown in Figure 2.4.
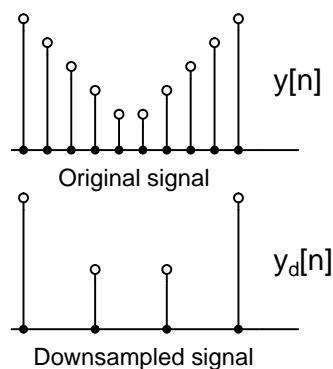
Figure 2.4: Illustration of downsampling by a factor of three.

6

Mathematically downsampling by a factor of M is expressed as

$$y_d[n] = y[Mn] \tag{2.5}$$

Let $Y(e^{j\omega})$ and $Y_d(e^{j\omega})$ denote the spectrum of the signal $y[n]$ and $y_d[n]$ respectively. The spectrum of the downsampled signal can be written as, [4]

$$Y_d(e^{j\omega}) = \frac{1}{M} \sum_{k=0}^{M-1} Y\left(e^{j\frac{\omega-2\pi k}{M}}\right) \tag{2.6}$$

The spectrum of the downsampled signal in relationship with the original signal is illustrated in Figure 2.5. It can be seen that the spectrum of the signal $y[n]$ expands after
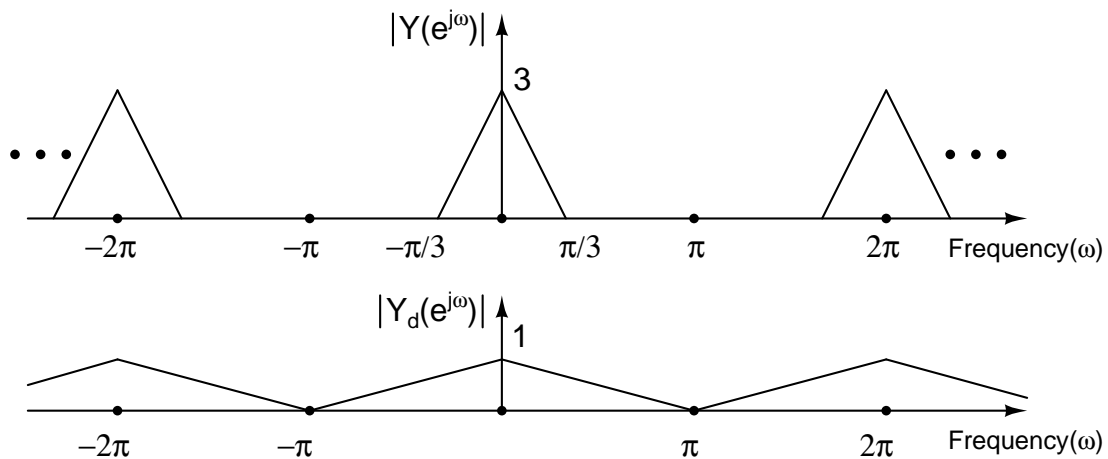
Figure 2.5: Spectrum of the downsampled signal when $M = 3$.

downsampling. To prevent aliasing of the signal, $Y(e^{j\omega})$ has to be restricted to $\dfrac{\pi}{M}$ or $\dfrac{f_s}{2M}$. Hence a digital anti-alias filter is necessary to filter out the components that alias into this band. Anti-alias filtering along with downsampling is termed as decimation. The block level representation of a decimator which downsamples by a factor of M is shown Figure 2.6.
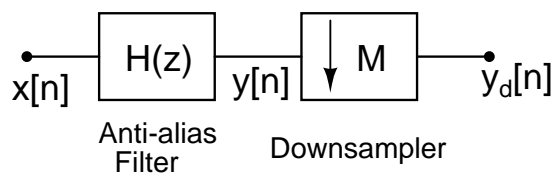
Figure 2.6: A decimator that downsamples by M.

2.2.2 Decimation in $\Delta\Sigma$ modulation

The output of a $\Delta\Sigma$ modulator contains the required in-band signal and the shaped noise as shown in Figure 2.3. To convert this oversampled signal to its Nyquist rate, the signal is downsampled by a factor of OSR. To prevent aliasing of the boosted quantization noise to the in-band the signal is digitally low pass filtered a priori. The block level equivalent of a decimator for a $\Delta\Sigma$ modulator is shown in Figure 2.7.
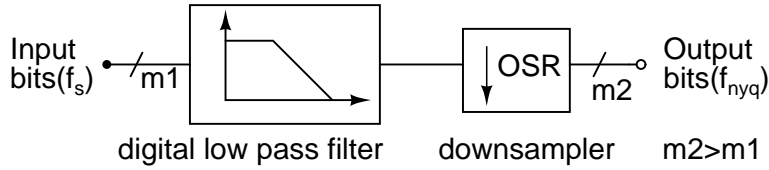
Figure 2.7: Decimator for a $\Delta\Sigma$ modulator.

2.3 Design targets for the decimator

The decimator described in this thesis is designed for a power optimized continuous-time $\Delta\Sigma$ modulator [1] that was built in a $0.18\,\mu$m CMOS process with $1.8\,$V supply. It is four bit modulator that has an OSR of 64 and operates at the sampling frequency, $f_s = 3.072\,$MHz. The modulator has an SNR of 93 dB in the bandwidth 20 Hz to 24 kHz and consumes a power of 90 μW. A power target of 100 μW is chosen for the decimator so that a low power $\Delta\Sigma$ data conversion system can be realized. The characteristics of the $\Delta\Sigma$ modulator and the requirements of the decimator are tabulated in Table 2.1 and Table 2.2 respectively.

Table 2.1: Modulator characteristics

Sampling rate	3.072 MHz
OSR	64
Nyquist rate	48 kHz
Modulator order	3
SNR(20 Hz-24 kHz)	93 dB
Power	90 μW
Technology	0.18μm CMOS

Table 2.2: Decimator requirements

No. of input bits	4
Input rate	3.072 MHz
Output rate	48 kHz
SNR	16 bits (96 dB)
Passband edge	21.6 kHz
Passband ripple	$< \pm 0.05$ dB
Target power	$< 100\,\mu$W

8

CHAPTER 3

Architecture of the decimator

3.1   Multistage decimation

The objective of the decimator is to sufficiently attenuate the aliasing noise before downsampling so that the in-band signal to noise ratio (SNR) is not deteriorated. The relative bandwidth of a digital signal, defined as the ratio of the bandwidth of the signal to half the sampling rate, from a $\Delta\Sigma$ modulator is $1/(2\text{OSR})$. An ideal anti-alias filter accompanying the decimator has the following characteristics.

$$
H(f) = \begin{cases} 1 & 0 \leq f \leq 1/(2\,\text{OSR}) \\ 0 & 1/(2\,\text{OSR}) < f \leq 1/2 \end{cases} \tag{3.1}
$$

But in reality all filters have a transition band of finite width and a stop band gain that is not zero. The anti-alias filter to be realized for the decimator needs to have narrow transition band. Such a filter if realized as a single filter has a very high order (>1000) [5]. A high order filter operating at a high frequency consumes a very high power.

Therefore, instead of using a single anti-alias filter operating at the input sampling rate and then downsampling to the Nyquist rate, filtering and downsampling is done in multiple stages. This is termed as multistage decimation [5][6]. According to (2.6), when a signal of bandwidth f_b is downsampled from a sampling rate f_s to f_s/M, the aliasing region lies centered at $k\dfrac{f_s}{M}$ with a bandwidth of $2f_b$. Here k takes values $0,1,2...\lceil M/2 \rceil$ where $\lceil\ \rceil$ denotes the ceiling function. It is ensured that in each stage, the noise in these aliasing bands are sufficiently attenuated by the filter that precedes the downsampling. The block diagram of this decimator employing multistage decimation is shown Figure 3.1.

Figure 3.1: Block diagram of the multistage decimator.

The multistage decimator employs three stages of anti-alias filtering. The overall down-sampling factor of sixty four is divided as 16, 2, 2 in these three stages. The first stage filter before the initial downsampling (16) is a cascade of four moving average filters (SINC4 filter). This filter operates at the maximum rate, f_s. A moving average filter can be implemented with only adders (without coefficient multipliers) and helps in saving power [7]. The remaining filtering is done with halfband filters and a downsampling factor of two is employed after each filter [6]. The equalizer corrects the droop caused by the SINC4 filter. The scaling block restores the signal to fullscale of the $\Delta\Sigma$ modulator. It is intended to have linear phase response for the decimator, hence all filters used in this design have symmetric finite impulse response (FIR) characteristics. Each block and its implementation is described in detail in the rest of this chapter.

3.2 SINC4 filter

The simplest form of digital low pass filtering is averaging N consecutive samples. Averaging N samples is done with a moving average filter/SINC filter. The transfer function of an N tap moving average filter is

$$H(z) = 1 + z^{-1} + z^{-2} + z^{-3} + \ldots + z^{-(N-1)} \tag{3.2}$$

An N tap SINC filter has $N - 1$ complex zeros distributed equally around the unit circle in the $\mathcal{Z}$ plane as shown in Figure 3.2.

Figure 3.2: Zeros of a 16 tap SINC filter in the $\mathcal{Z}$ plane.

The signal is downsampled from 3.072 MHz to 192 kHz by a factor of sixteen after the first stage filtering. According to (2.6) the alias bands are located at integer multiples of $\dfrac{f_s}{16}$. The tap length of the SINC filter is chosen as $N = 16$ so that the complex zeros that creates nulls are located at the center of these alias bands.
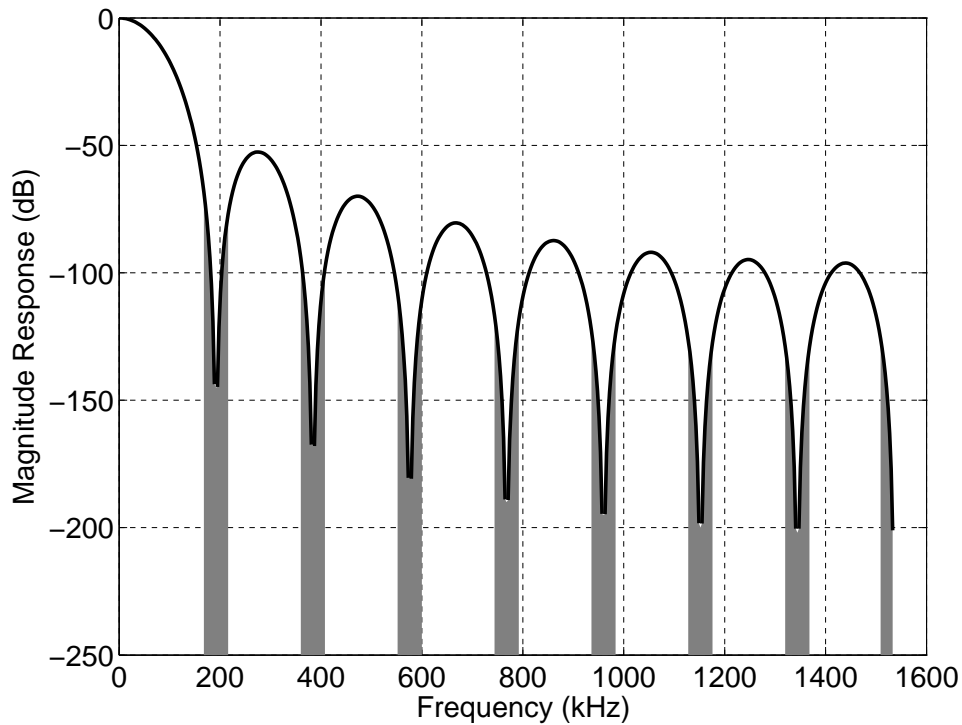
Figure 3.3: Frequency response of the SINC4 filter(aliasing bands in gray).

Attenuation provided in the stop band can be increased by cascading SINC filters. A third order $\Delta\Sigma$ modulator shapes the quantization noise at its output as $(1 - z^{-1})^3$ [3].

11

Hence the quantization noise power spectral density increases with frequency as f^3. Sufficient attenuation of the shaped quantization noise over the entire band is obtained with a cascade of four SINC filters (SINC4) that has a $\frac{1}{f^4}$ roll off [8]. The frequency response of the cascade of four sixteen tap SINC filters (SINC4) is shown in Figure 3.3. The shaded areas in the frequency response are the noise aliasing bands for the SINC4 filter.

3.2.1   Hogenauer structure

A convenient implementation of the SINC4 can be obtained by modifying the filter transfer function in (3.2) by introducing a pole and a zero at $z = 1$ [7].

$$H1(z) = \left[\frac{1 - z^{-16}}{1 - z^{-1}} \right]^4 = \left[\frac{1}{1 - z^{-1}} \right]^4 \left[1 - z^{-16} \right]^4 \tag{3.3}$$

$H1(z)$ along with the downsampling of sixteen is implemented in two steps as shown
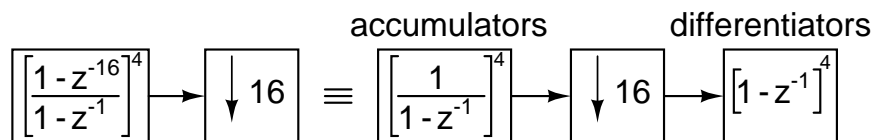
Figure 3.4: Implementation of SINC4 as Hogenauer structure.

in Figure 3.4. At first, the accumulation operations $\left(\frac{1}{1 - z^{-1}} \right)^4$ are done at the rate f_s. Then, the operation $[1 - z^{-16}]^4$ and the downsampling of sixteen are implemented with cascade of four differentiators $(1 - z^{-1})$ working at $f_s/16$. This structure is called Hogenauer structure [7].

3.2.2   Pipelining and retiming of SINC4

The accumulators are first pipelined by inserting a register at the input of each accumulators as shown in Figure 3.5. The registers are then retimed to a single register in the forward path of each accumulators [9]. Hence the glitches in combinational adders

in one accumulator are prevented from propagating to the next accumulator, thereby reducing unwanted switching power.
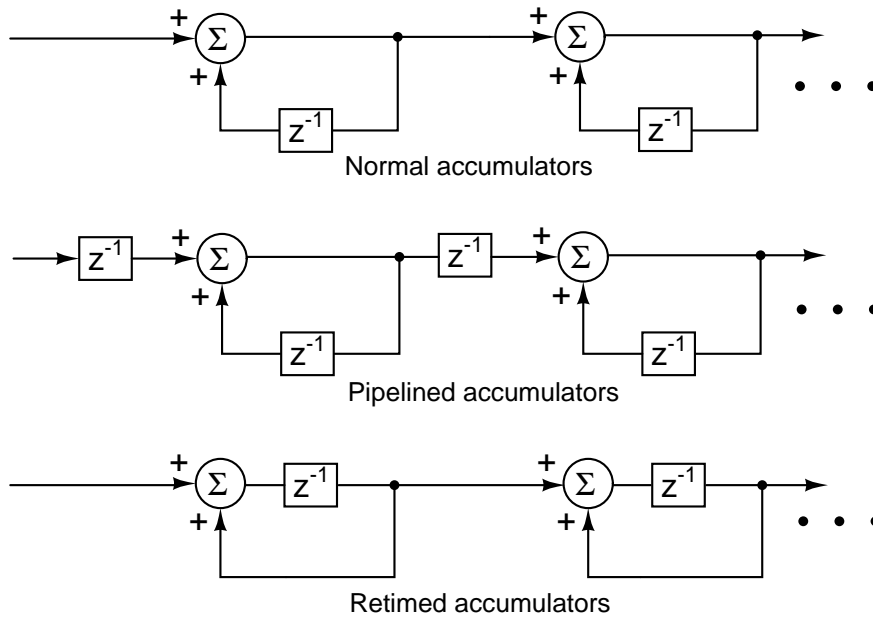
Figure 3.5: Retiming and pipelining of accumulators for power reduction.
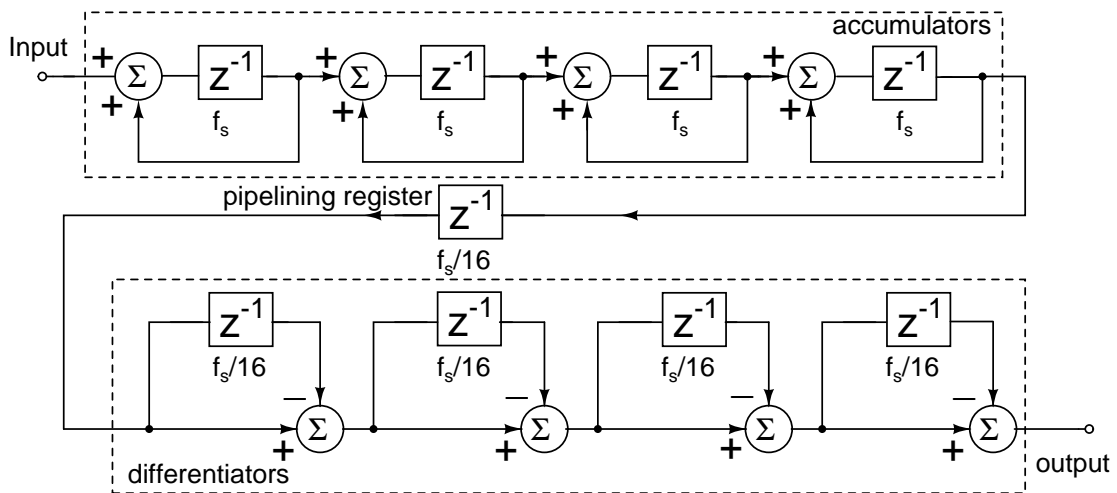
Figure 3.6: Implementation of the SINC4 filter.

Similarly the pipelining register at the output of the fourth accumulator (refer Figure 3.6) prevents the switching data at f_s propagating through the differentiators. It is determined through simulations that retiming of the registers in the accumulators and the pipelined register saves 46 % of power in the SINC4 stage.

Overflow in the accumulators does not cause signal distortion if the signal representa-

tion is based on wrap around arithmetic (binary, 2's complement) and all register widths are chosen according to the relationship [7].

$$\text{Bit width} \; = \; B_{in} + k \, log_2 N \tag{3.4}$$

Here B_{in} is the input bit width (4 bit binary), k (4) is the number of cascaded SINC stages and N (16) is the tap length of the SINC. Hence all the registers are chosen to be 20 bit wide.

3.3   Halfband filters

Halfband filters are a class of equiripple FIR filters with order $N_{ord} = 4\,P + 2$, where $P \in \{1,2,3\ldots\}$. Halfband filters have a gain of 0.5 at one fourth of the clock frequency ($f_{clk}/4$). Hence the maximum downsampling factor that can occur after a halfband filtering is two. The middle sample of the impulse response of a halfband filter is 0.5 and the impulse response is symmetric about this sample. Odd tap weights are zero and hence there is a reduction in the number of multipliers employed.

The signal at the output of the SINC4 filter is at four times the Nyquist rate (192 kHz). Two halfband filters along with the downsampling by a factor of two after each filter downconverts the signal to its Nyquist rate. The orders of the halfband filters are chosen such that the overall passband ripple of the decimator is constrained to ± 0.05 dB and the aliasing noise does not cause degradation in the in-band SNR.

The first halfband filter is chosen to have a wide transition band. A tenth order halfband filter that has a stop band attenuation of 60 dB is chosen. This filter operates with the clock frequency of 192 kHz. The aliasing band lies in the region 72 kHz to 96 kHz.

The second halfband filter provides the final filtering before the signal is downsampled to its Nyquist rate (48 kHz). The filter is designed to have a narrow transition band and a

stop band attenuation of 50 dB. A fiftieth order filter is chosen. This filter operates with the clock frequency of 96 kHz. The aliasing band lies in the region 24 kHz to 48 kHz. The frequency response of the first and the second halfband filters are shown in Figure 3.7. The aliasing bands of each downsampling operation is shaded gray.
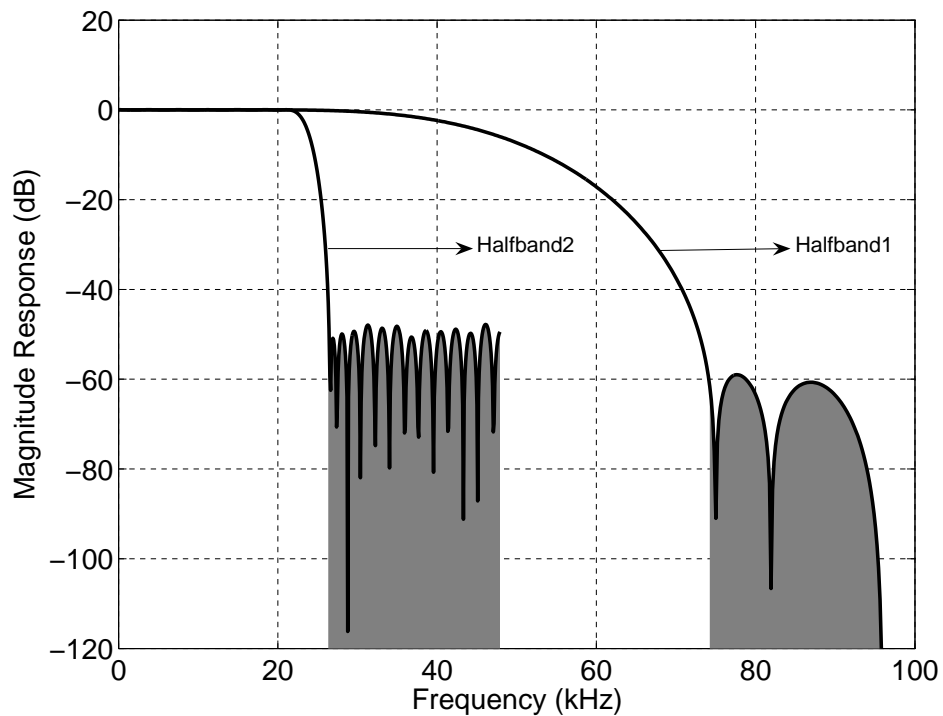
Figure 3.7: Frequency response: The first and the second halfband filters.

3.3.1 Implementation of the halfband filters

This section deals with various optimization techniques that are implemented in the halfband filters which aid reduction of power and hardware. The three techniques that are employed in halfband filters are

1. Polyphase structure
2. Canonical signed digits encoding
3. Optimal data width in arithmetic units

The signal in halfband filters and subsequent other blocks are encoded in 2's complement.

3.3.1.1 Polyphase structure

Any filter followed by downsampling can be implemented as a polyphase structure [4][9]. The input data stream is split into multiple phases. The filter transfer function is also split into multiple parts and each transfer function operates on each phase of the signal. Outputs from all these phases are combined to produce the filtered and downsampled version of the signal. Each individual phase operates at the downsampled rate and hence the effective frequency of operation of the filter is reduced thereby saving power.

Implementation of a halfband filter as a polyphase structure is explained by the following illustration. Let the filter transfer function be $G(z)$ and the downsampling factor be two. Let $G(z)$ be represented as

$$G(z) = \sum_{i=0}^{L} a_i z^{-i} \tag{3.5}$$

The transfer function is split into two phases as given in (3.6).

$$
\begin{aligned}
G(z) &= \left\{ a_0 + a_2 z^{-2} + a_4 z^{-4} + \ldots + a_L z^{-L} \right\} + \\
&\quad z^{-1} \left\{ a_1 + a_3 z^{-2} + a_5 z^{-4} + \ldots + a_{L-1} z^{-(L-2)} \right\} \\
&= G_e(z) + z^{-1} G_o(z) \tag{3.6}
\end{aligned}
$$

Polyphase implementation of the filtering and downsampling is explained in Figure 3.8.

The circuit that splits the input data into odd and even data streams is shown in Figure 3.9. It can be seen that the filters $G_e(z^{1/2})$ and $G_o(z^{1/2})$ work at half the clock rate.
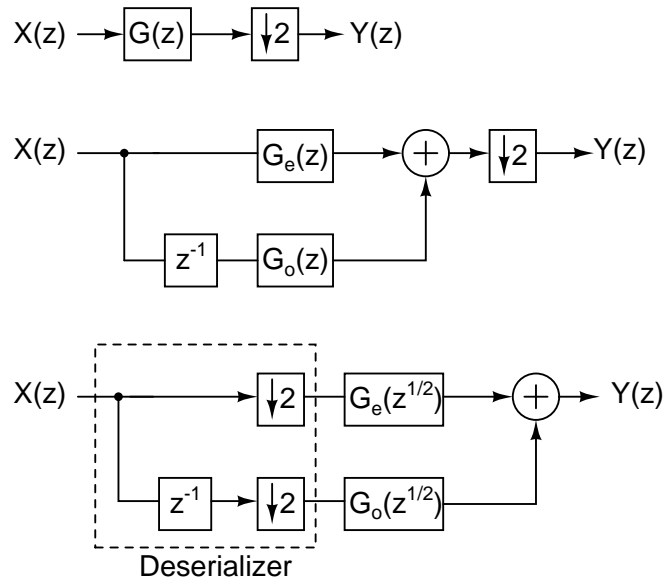
Figure 3.8: Polyphase structure in halfband filters.
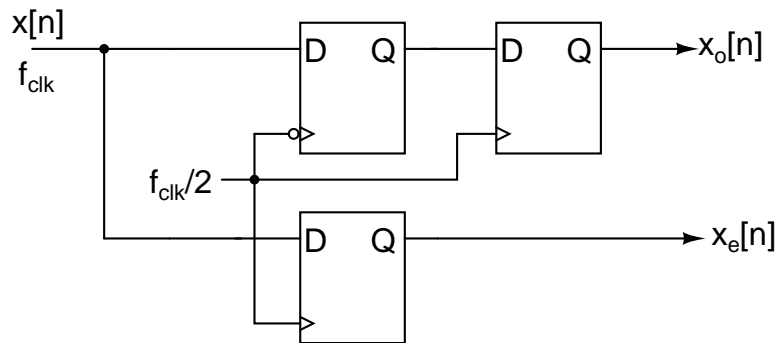
Figure 3.9: Deserializer: Splits data into even and odd streams.

3.3.1.2 Canonical Signed Digits

In a binary representation of a number, digits are either 0 or 1. In signed digit representation of binary numbers, digits belong to the triplet $\{-1,0,1\}$. Signed digit representation of a number is not unique [10]. For example, the number 7 can be written in following ways in signed digit representation.

$$
\begin{aligned}
(0 \quad 1 \quad 1 \quad 1)_2 &= 7 \\
(1 \quad 0 \quad -1 \quad 1)_2 &= 7 \\
(1 \quad -1 \quad 1 \quad 1)_2 &= 7 \\
(1 \quad 0 \quad 0 \quad -1)_2 &= 7
\end{aligned}
$$

Encoding a binary number in signed digits representation such that it contains the fewest number of non-zero bits is called canonic signed digit (CSD) [11]. Hence encoding the tap weights of a filter in CSD reduces the number of multiplication operations that saves hardware and power. Unlike the signed digit representation, the CSD representation of a number is unique.

The CSD representation is also applicable for fractional numbers. For e.g. $0.4375 = 2^{-1} - 2^{-4}$. Truncation of tap weights to finite number of CSD alters the frequency response of the filter. The number of CSDs in tap weights is decided by the accuracy of the frequency response (passband ripples). In this decimator design, the tap weights are fourteen bits wide.

3.3.1.3 Data width in halfband filters

In order to ensure proper filtering of the quantization noise in halfband filters, the digital signal should support adequate dynamic range. More the number of bits in the filtering operation, higher is the dynamic range of the filtered signal. A high dynamic range filtering is required to ensure adequate suppression of the noise in the aliasing bands. The minimum number of bits required is explained with the help of Figure 3.10.
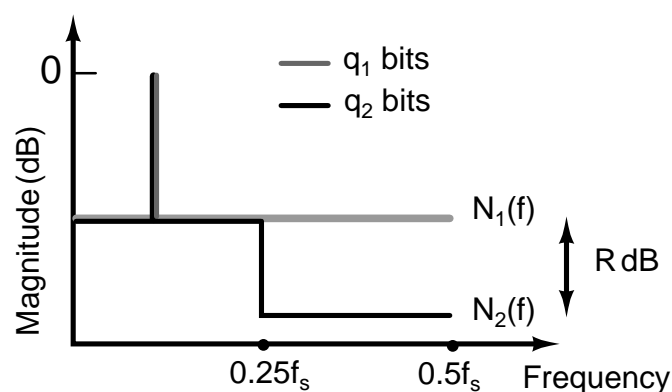
Figure 3.10: Filtering of quantization noise floor.

The quantization noise Power spectral density (PSD) of a digital signal, with fullscale $0\,\mathrm{dB}$, quantized to q_1 bits at a sampling rate $1\,\mathrm{Hz}$ is $N_1(f) = 10^{-6q_1/10}$. To attenuate

a small band of its quantization noise by R dB, the quantization noise floor has to be lowered by increasing the number of bits to q_2 (Refer Figure 3.10). Hence for the filtered signal the quantization noise PSD is $N_2(f) = 10^{-6q_2/10}$. It can be concluded from Figure 3.10 that

$$R = 10 \, log_{10} \frac{N_2(f)}{N_1(f)} \tag{3.7}$$

$$\text{or} \quad q_2 = q_1 + \frac{R}{6} \tag{3.8}$$

It can be seen that every extra bit handles 6 dB more dynamic range in filtering. The signal to be filtered has a resolution of 96 dB ($q_1 = 16$). It is found that a 48 dB attenuation of aliasing noise (with respect to the in-band noise floor) is sufficient to preserve the in-band SNR. Hence the internal states of the filter (adders and multipliers) are twenty four bit wide ($q_2 = 24$).

3.3.1.4 Implementation details of the first halfband filter

The block diagram of the polyphase implementation of the first halfband filter is shown in Figure 3.11. The P_4 block pads four LSBs to the data path to increase the dynamic range to 24 bits. The tap weights of the filter, b_0, b_2, b_4, b_5 are symmetric about the middle sample $b_5 = 0.5$.
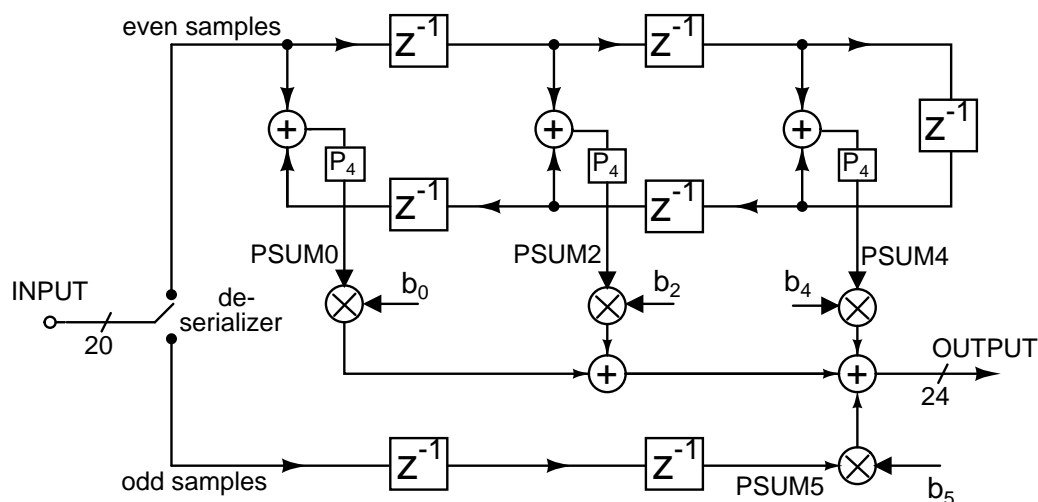
Figure 3.11: Polyphase implementation of the first halfband filter (10th order).

The output of the filter is obtained from the internal states $PSUM0$, $PSUM2$, $PSUM4$, $PSUM5$ as shown in Figure 3.12. The tap weights are less than unity and hence are expanded in powers of 2^{-1} with CSD encoding. A 2^{-m} in the tap weight corresponds to right shifting the signal by dropping its m LSBs. Hence a tap weight multiplication is obtained by adding and subtracting right shifted signals. This multiplication is further nested based on Horner's rule [6]. This reduces the effective right shift operation and hence the effect of truncation noise. For e.g. $2^{-3}-2^{-5}-2^{-7} = 2^{-3}\{1-2^{-1}(2^{-1}+2^{-3})\}$. This nested multiplication requires extra shifting operations compared to the non nested multiplication. However no explicit hardware is required to implement a shifter because shifting involves dropping LSBs.
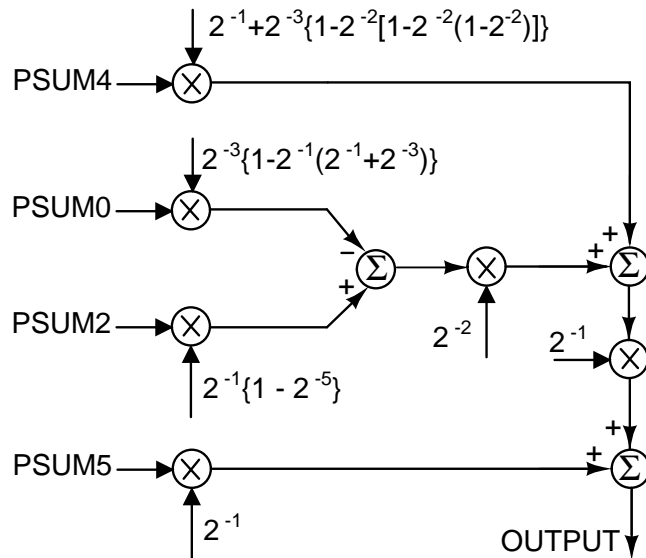
Figure 3.12: Obtaining output from the internal states.

3.4 Equalizer

It is required for the decimator to have a passband gain error that is constrained to $\pm\,0.05\,\text{dB}$. The equalizer is an FIR filter that corrects the passband droop caused by the SINC4 filter [8]. The equalizer works at the Nyquist rate. The magnitude response of the equalizer is inverse that of the SINC4 filter in the in-band (0-24 kHz). A thirty fourth order FIR filter is chosen for equalization. The tap weights of the equalizer are

found using *Parks McClellan* method. As in the halfband filters, the tap weights are encoded in CSD and multiplications are nested. Figure 3.13 shows frequency response of the equalizer, the passband frequency response of the unequalized decimator and the equalized decimator. The inset shows that passband ripples of the decimator is constrained to $\pm\,0.05$ dB. After equalization the signal is rounded from 24 bits to 16 bits by dropping the eight LSBs.
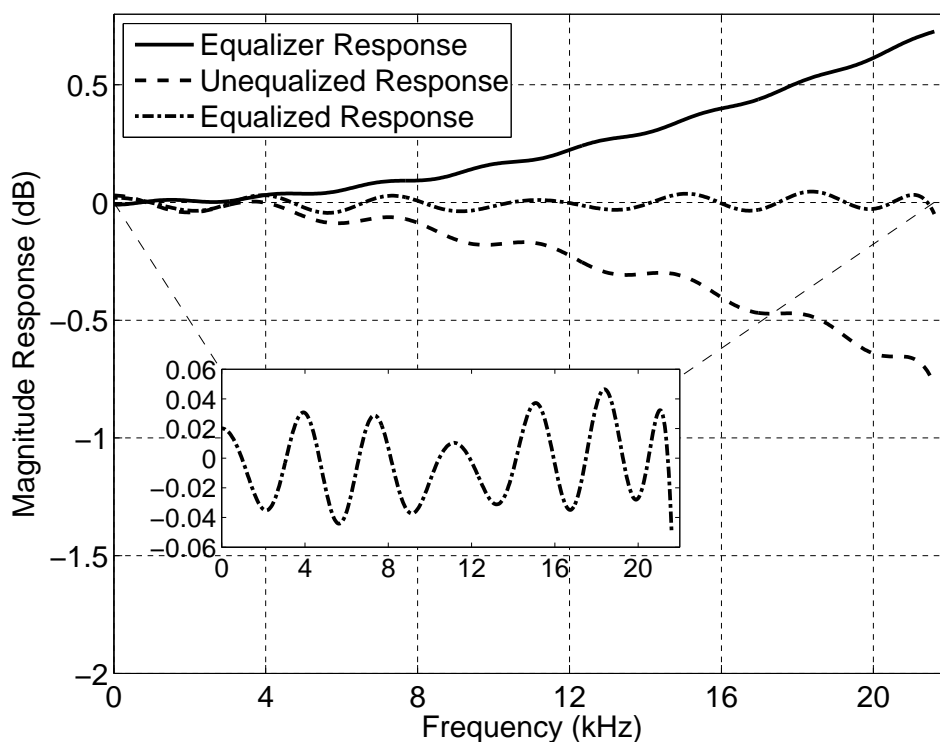
Figure 3.13: Frequency response of the Equalizer, the unequalized & the equalized decimator.

3.5 Scaling block

A $\Delta\Sigma$ modulator has a maximum stable amplitude (MSA) at which the peak SNR is obtained. Beyond the MSA the modulator goes to instability and the SNR reduces and finally approaches zero [3]. MSA is expressed in percent of fullscale. At peak SNR the output swing of the modulator is MSA $\times$ fullscale. In order to achieve the peak SNR at the Nyquist rate, after decimation and truncating the signal to appropriate number of

bits, the signal has to swing to its fullscale. Hence the signal is scaled by $\frac{1}{MSA}$ to obtain fullscale swings at the output of the decimator.

The $\Delta\Sigma$ modulator in [1] has an MSA around 85 % of the fullscale. The output of the modulator swings fully in its available range due to the presence of large quantization noise. At the output of the first halfband filter, the maximum output swing is found to be 85 % of the fullscale, same as the MSA of the modulator. Hence the scaling is done after the first halfband filter where the quantization noise is attenuated to a level comparable to the noise floor in the in-band.

$$S = \frac{1}{0.8605} = 1 + 2^{-2}\left\{2^{-1} + 2^{-2}\left(2^{-1} + 2^{-3}\left[1 - 2^{-2}\right]\right)\right\}$$

The scaling value is kept slightly smaller than $\frac{1}{MSA}$ to prevent overflow. The presence of passband ripples in other filters and the fact that the decimator operates with a finite number of bits can result in a overflow when the filter processes a signal of amplitude that is close to the fullscale. This scaling value is encoded in CSD and implemented with Horner's rule.

CHAPTER 4

Synthesis of the decimator

The decimator is designed in a 0.18 μm CMOS process with a 1.8 V supply. To make it easy to port the design to different processes, handcrafted circuitry is avoided. The design is developed with standard cells using automated CAD tools. The behavioral description of the filter is written a hardware description language (Verilog) at register transfer level (RTL) abstraction. The CAD tools that are used for designing and testing the decimator are tabulated in Table 4.1.

Table 4.1: CAD tools used for the decimator design

Tool	Purpose
MATLAB	System design and modelling
Design Compiler (Synopsys)	Synthesis
SoC Encounter (Cadence)	Place & Route
Prime Time (Synopsys)	Timing verification
Prime Power (Synopsys)	Power analysis
Modelsim (Mentor)	Simulation

4.1   Description of design flow

The preliminary design involves testing the decimator in MATLAB to ensure that the SNR performance is satisfactory. The resolution of arithmetic operations in MATLAB is the precision of the computer (usually 32 bits). The description of the decimator is then coded in verilog with the appropriate bit precision as described in earlier chapters. An initial simulation of the entire system is carried out by simulating the verilog code with the tool *Modelsim* to verify the functionality and SNR performance.

The verilog netlist of the design is then translated to a gate level netlist using the tool *Design Compiler*. All design constraints such as load capacitance, area, power, frequency of operation are given during this synthesis.

In Place & Route the CAD tool performs three major tasks

- Place the layout of standard cells according to the floor plan
- Clock tree synthesis (CTS)
- Route the design to meet the timing

The timing closure is ensured after place and route with *Prime Time*. The design is ensured to be devoid of setup, hold, reset removal and rise/fall time violations. The design after place and route, with the annotation of interconnect delays, is simulated and verified for functionality. The layout of the final design is shown in Figure 4.1. The area occupied by the decimator core is $0.46\,\mathrm{mm}^2$.
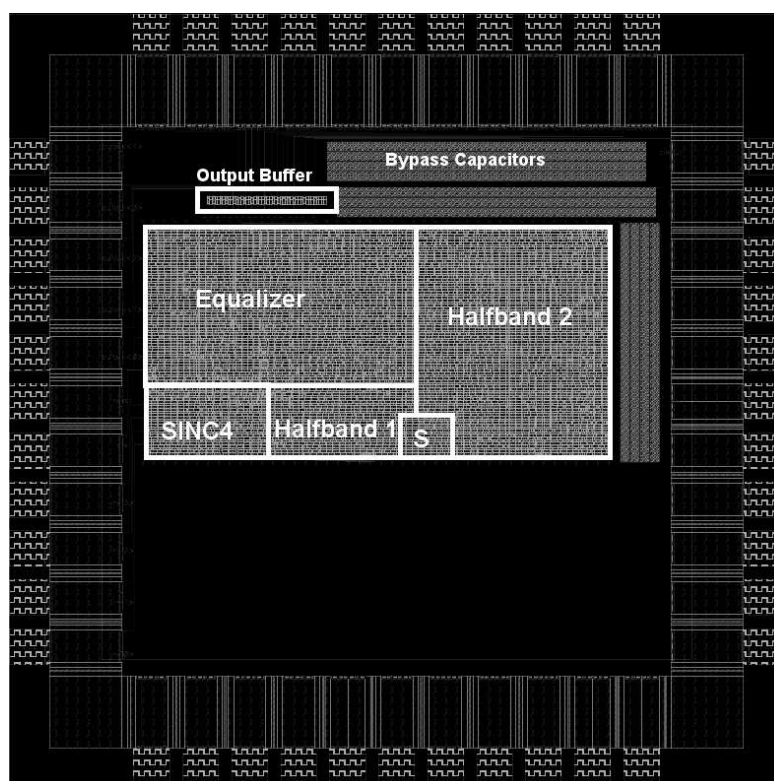
Figure 4.1: Layout of the decimator chip.

4.1.1 Synthesis & simulation results

The input test stimulus for the decimator is obtained through simulations in MATLAB with the help of the $\Delta\Sigma$ toolbox [3]. The signal is translated to corresponding verilog format for simulating it with the netlist obtained after Place & Route. The spectrum of the output signal is obtained and SNR is evaluated at the Nyquist rate. The decimator is tested for SNR performance with sine wave excitation of different frequencies. A sample spectrum from the output of the modulator is shown in Figure 4.2. The peak output SNR of the decimator is 95.8 dB.
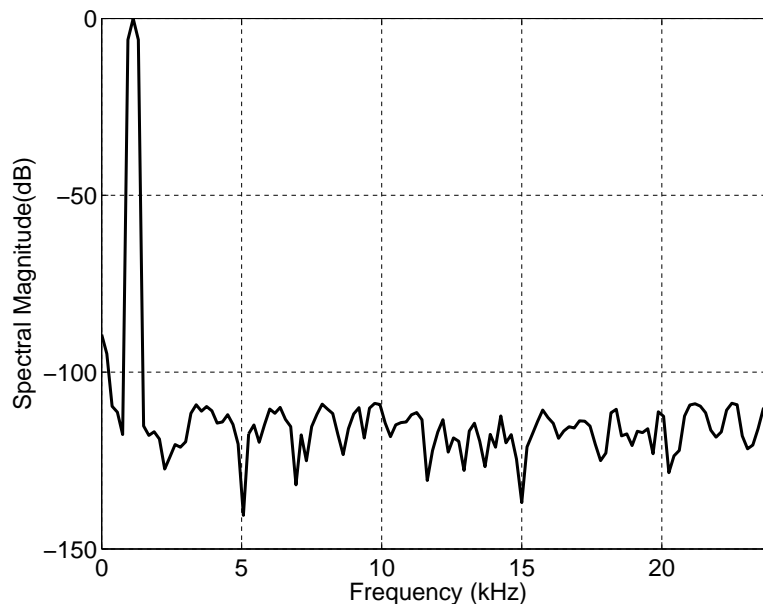
Figure 4.2: Simulated spectrum of the decimator output, SNR=95.8 dB.

4.1.2 Power estimation

The power consumption of a digital circuit depends upon the switching activity in the circuit. The signal dependent power consumption of a digital circuit is analyzed using the tool *Prime Power*. The power consumption is estimated based on observing the switching activity at all nodes in the circuit. A value change dump (VCD) file that represents the switching activity of a circuit for a particular test vector is generated using *Modelsim*. The tool *Prime Power* estimates the power using this VCD file and the

25

gate level netlist. The power consumption of the decimator for various test inputs is
tabulated in Table 4.2. It is seen that the power consumption of the decimator doesn't

Table 4.2: Power consumption for various test inputs

Test stimulus	Power (μW)
Tone at 1.6875 kHz	96.7
White noise	100.9
Zero input	99.7

depend upon the type of input. This is because a sequential circuit's toggling activity
depends mainly upon the clock rate. The power consumption of various blocks of the
decimator is given in Table 4.3.

Table 4.3: Power consumption of the blocks of the decimator

Block	Power (μW)
SINC4	46.4
First halfband	5.9
Second halfband	14.1
Equalizer	15.2
Scaling block	2.3
Clock tree	12.7
Total	**96.7**

4.2   Level translator

The power consumption of any digital circuit can be reduced by reducing the supply
voltage in trade off for the speed of operation of the system. It is intended to make the
decimator work at a supply smaller than 1.8 V to reduce power. The logic levels of the
output from the decimator is converted to 1.8 V with a level translator. The schematic
of the level translator is shown in Figure 4.3.

The level translator has a static power consumption if its input logic 1 voltage is lesser
than 1.8 V. Hence PMOS transistors with a large threshold voltage ($V_T = -0.72$ V) are
used to reduce this static power consumption.
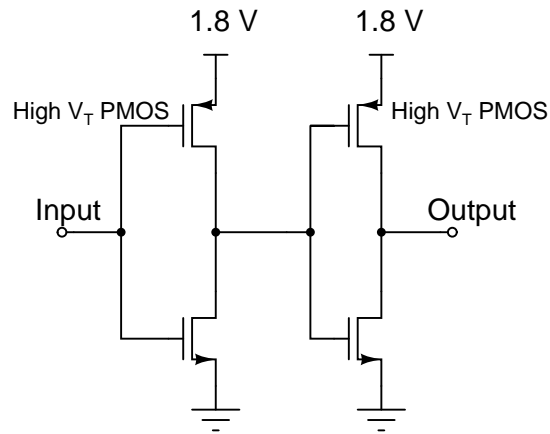
Figure 4.3: Schematic of the level translator.

Through simulations it is found that a single level translator consumes a power of 245 nA from 1.8 V supply at fast-fast transistor corner when level translating an alternating data that has logic levels 0.9 V and 0 V at a frequency of 48 kHz. Hence the power consumption of seventeen level translators (digital output data and clock) consumes a power of 7.5 μW. The power reduction in the decimator core at a reduced supply is expected to be much larger than the increased power consumption in level translators. Hence the overall power consumption of the decimator is expected to reduce further.

CHAPTER 5

Measured results from the decimator chip

5.1 Test setup

The block diagram of the test setup is shown in Figure 5.1. An FPGA is programmed to emulate the output of the $\Delta\Sigma$ modulator [1]. The FPGA generates the four bit data synchronized to a 3.072 MHz clock along with the RESET signal. The output signal from the decimator is captured with a logic analyzer.
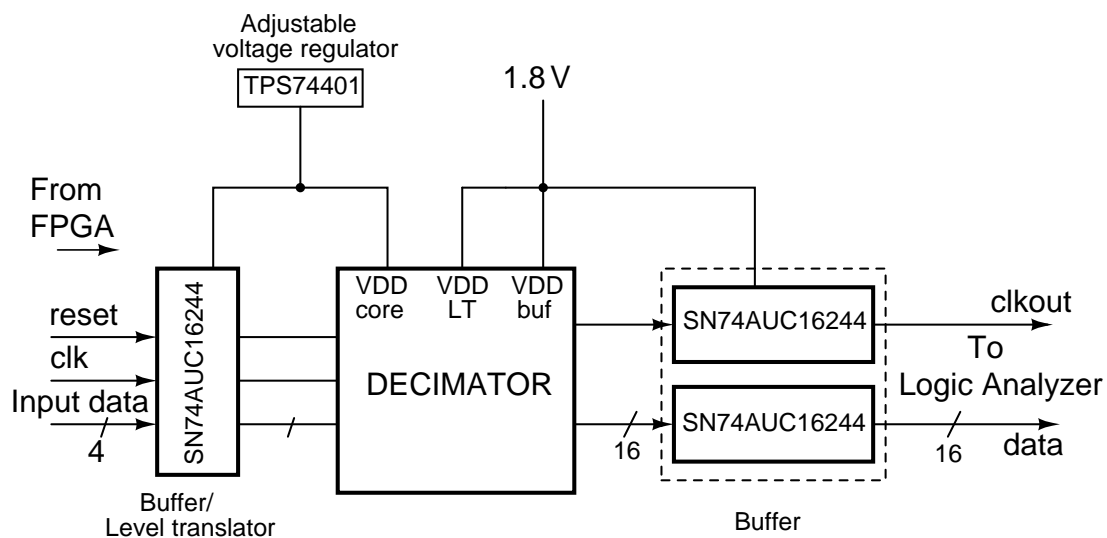
Figure 5.1: Block diagram of the test setup.

A two layer PCB is designed to test the chip. Provision is made to adjust the supply voltage of the decimator core. Figure 5.2 shows the picture of the PCB designed for testing the chip. The following measurements are made.

- To evaluate the SNR from the decimator's output spectrum for a tone input.

- Compare time domain samples from simulation and measurement for an impulse input.

- Scale the decimator core's supply voltage ensuring reliable operation and observe the power reduction.
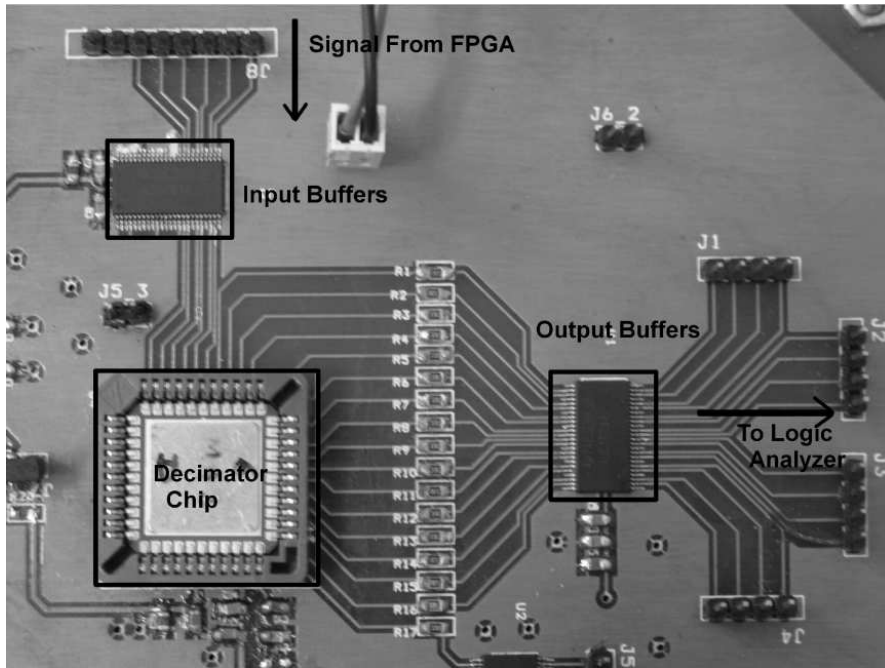
Figure 5.2: Picture of the test PCB.

5.2   Results from the fabricated chip

Figure 5.3 shows the spectrum obtained from the output of decimator excited by a sine wave input.
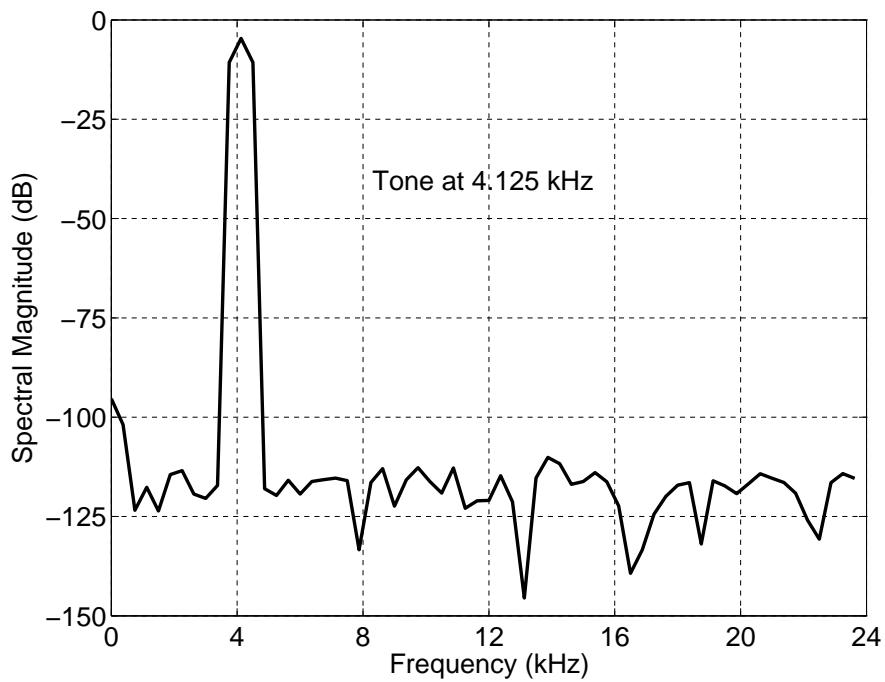
Figure 5.3: Measured spectrum of the decimator's output.

It is found that the SNR computed from this spectrum matches exactly with the SNR obtained from simulations. It is also verified that the time domain impulse response samples from the chip matches with the impulse response samples obtained through simulation. The impulse response samples from the chip and from simulation are shown in Figure 5.4.
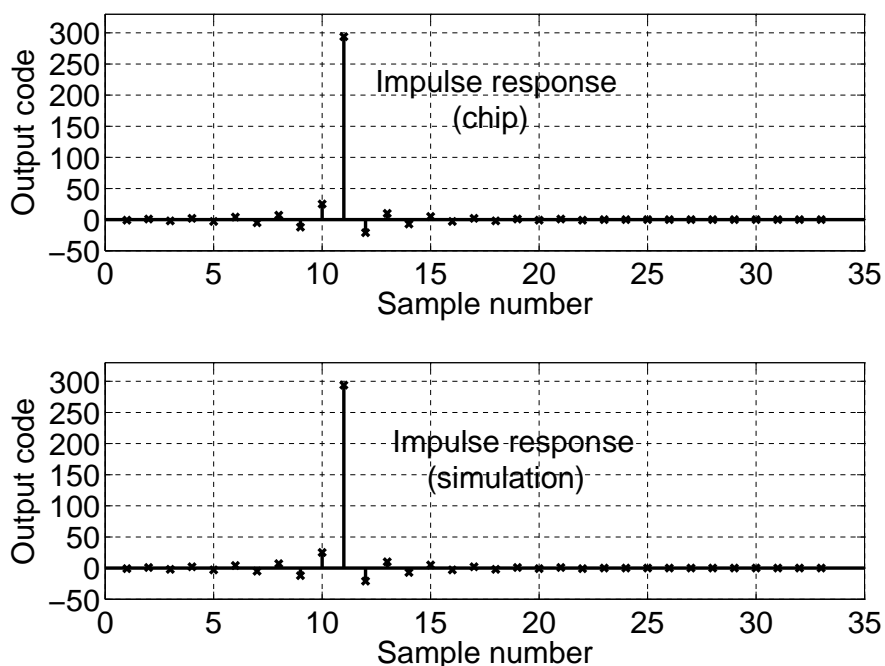
Figure 5.4: Comparison of the impulse responses.

5.2.1 Power measurement

At the nominal supply of 1.8 V, the power consumption of the chip is $104\,\mu$W. This matches closely with the simulation estimate of $96\,\mu$W. It is observed that the chip is functional correctly down to a power supply voltage of 0.9 V when the system is running at 3.072 MHz. The power consumption of the decimator and the level translator across multiple supply voltages is given in Table 5.1.

It is observed that the power reduction obtained in the core is 77.4% at the supply voltage of 0.9 V. The power consumption of the level translators when the core supply is 0.9 V is very high (12.7 times larger than the simulated estimate). It is found that the

Table 5.1: Power consumption for various supply voltages

Core power supply(V)	Decimator Core		Level Translator (1.8 V)	
	Current(μA)	Power(μW)	Current(μA)	Power(μW)
1.8	58	104.4	≈ 0	≈ 0
1.5	46	69.0	0.3	0.54
1.2	36	43.2	13.2	23.8
1.0	29	29.0	37.8	68
0.9	26	23.4	53.8	97

threshold voltage of the fabricated PMOS transistors are unusually very low $(-0.3\,\text{V}$ in comparison to its nominal value of $-0.72\,\text{V})$ resulting in a large static power consumption. To avoid this a level translator with latching action is preferred [12].

5.3   Summary

A low power decimator has been designed and implemented with the help of standard cells. All levels of optimizations are carried out in the architectural level and automated with CAD tools to obtain quick design. The power consumption of the decimator has been made as same as its modulator [1] which proves that it is possible to design a decimator with as low power as recently published low power $\Delta\Sigma$ modulators. As the decimator is functional down to 0.9 V, the power consumption can be further reduced by generating 0.9 V from a 1.8 V supply. Table 5.2 gives the performance summary of the decimator.

Table 5.2: Performance summary of the decimator

No. of input bits	4
Input rate	3.072 MHz
No. of output bits	16
Output rate	48 kHz
SNR	96 dB
Passband edge	21.6 kHz
Passband ripple	$< \pm 0.05$ dB
Power consumption(1.8 V supply)	104 μW
Technology	0.18 μm CMOS

CHAPTER 6

$\Delta\Sigma$ modulator fundamentals

Analog to digital converters (ADCs) are systems that convert an analog signal to digital bits through sampling and quantization. An analog signal that is bandlimited to a frequency (f_b) can be perfectly reconstructed from its discrete-time samples if the sampling rate (f_s) is greater than its Nyquist rate i.e. $f_s > 2 f_b$. This principle is referred to as the Nyquist-Shannon sampling theorem. Quantizing the amplitude of the discrete samples can be treated as an addition of an error to the original signal. This error, called the quantization noise, is assumed to be random, uncorrelated with the original signal, uniformly distributed and to have a white spectrum. These assumptions become less valid when the quantization interval (difference between adjacent quantization levels) becomes comparable to the signal amplitude. The block level representation of an ADC is shown in Figure 6.1.
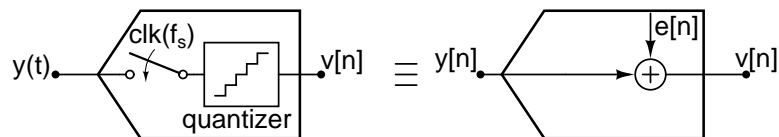
Figure 6.1: Block level representation of an ADC and its additive quantization noise model.

The quality of the digital signal depends on the strength of the quantization noise which in turn depends on the quantization interval V_{lsb}. The mean squared value of the quantization noise is $V_{lsb}^2/12$. The term signal to quantization noise ratio (SQNR) which is the ratio of mean squared value of the signal to the mean squared value of the quantization noise is a measure of the quality of the digital signal. For an N bit ADC that has its fullscale (quantizer saturation limits) of A, the quantization interval is, $V_{lsb} = \frac{A}{2^N}$. Hence the maximum SQNR of a sine wave signal that swings fullscale can be expressed

as

$$\text{SQNR}_{\text{max}}(\text{dB}) = 6.02N + 1.76 \tag{6.1}$$

6.1 Continuous-time $\Delta\Sigma$ modulation

The quantization noise spectrum of a sampled and quantized signal at its Nyquist rate is shown in Figure 6.2(a). The total quantization noise power is $V_{lsb}^2/12$. The quantization noise spectrum of an oversampled and quantized signal is shown in Figure 6.2(b). The in-band quantization noise power of the oversampled signal in a bandwidth of f_b is $\dfrac{V_{lsb}^2}{12 f_s/2} f_b$. This can be written in terms of the oversampling ratio as $\dfrac{V_{lsb}^2}{12\text{OSR}}$.
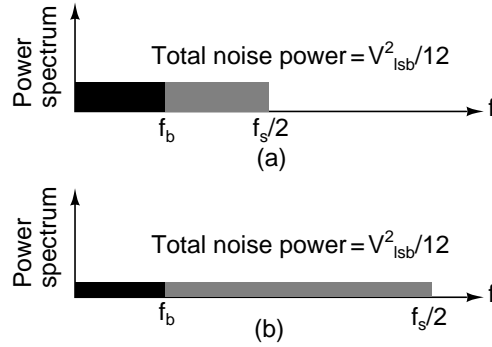
Figure 6.2: Quantization noise spectrum (a) Nyquist rate, (b) Oversampled rate.

Doubling the sampling rate reduces the in-band quantization noise power by a factor of two and hence increases the SQNR by 3 dB. The effective number of bits (N_{eff}) of the conversion is defined using (6.1) as

$$N_{eff} = \frac{\text{SQNR}_{\text{max}}(\text{dB}) - 1.76}{6.02} \tag{6.2}$$

The quantization noise in the in-band can be further attenuated by placing the ADC inside a negative feedback loop. This process is called $\Delta\Sigma$ modulation.

Figure 6.3 shows the block diagram of a continuous-time $\Delta\Sigma$ modulator (CTDSM). It has a continuous-time loop filter, $L(s)$, that has a large gain in the bandwidth of interest.

33
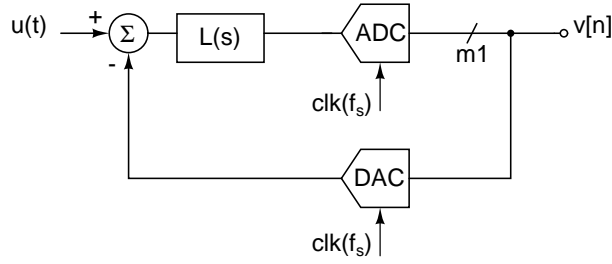
Figure 6.3: Block diagram of a continuous-time $\Delta\Sigma$ modulator.

The signal is oversampled and quantized to multiple levels by the internal ADC. The DAC feeds back an analog signal back to the loop filter.

Usually a coarse internal ADC of 1 to 4 bits resolution is used. The quantization noise of the internal ADC when referred at the output is suppressed by the large gain of the loop filter. Hence large SQNR of effective number of bits (N_{eff}) of 20 or higher is easily achieved. The required noise transfer function (NTF) is obtained by appropriately choosing the loop filter transfer function $L(s)$. Higher order loop filter provides more suppression of the quantization noise and have aggressive noise shaping. For an Lth order loop filter having noise transfer function, $\text{NTF}(z) = (1 - z^{-1})^L$, the in-band noise power is approximately [13].

$$P_e = \frac{V_{lsb}^2}{12} \frac{\pi^{2L}}{2L+1} \left(\frac{1}{\text{OSR}^{2L+1}} \right) \tag{6.3}$$

It can be seen that for a given order (L) of the modulator the in-band quantization noise power reduces as $6L+3$ dB for every doubling of OSR. Hence higher sampling rates are required to increase the effective number of bits (N_{eff}) for a given signal bandwidth (f_b). The in-band quantization noise power can also be reduced by increasing the order (L) of the modulator. Modulators with order greater than two are only conditionally stable [14]. For higher order modulators, the internal ADC gets overloaded even for an input to the modulator which is much smaller than the fullscale of the ADC. This reduces the maximum stable amplitude (MSA) of the modulator.

6.1.1 Advantages of a CTDSM

In discrete-time $\Delta\Sigma$ modulators (DTDSMs) the loop filter is a discrete-time filter and the sampling is done outside the loop whereas in CTDSMs the loop filter is a continuous-time filter and the signal is sampled inside the loop. CTDSMs are preferred over DTDSMs for the following reasons.

1. CTDSMs possess inherent anti-aliasing property which eliminates the need of an external anti-aliasing filter [13]. The loop filter behaves as an anti-alias filter.

2. The sampling is done at a less sensitive node of the loop. Hence any imperfections and errors due to sampling are shaped by the NTF.

3. CTDSMs can operate at a much higher clock rate compared to discrete-time modulators [13]. The loop filter in a CTDSM which is usually implemented with active RC integrators or $g_m - C$ integrators has less stringent requirements for the settling of the op-amps in comparison to a discrete-time modulator.

6.1.2 Performance measures

6.1.2.1 Signal to noise ratio

Signal to noise ratio (SNR) is the ratio of signal power to the integrated noise power in the in-band. The signal is usually a tone whose frequency is lesser than f_b. The in-band noise power is evaluated from the spectrum of the modulator's output by integrating the noise power in the bandwidth 0 - f_b. Signal to noise and distortion ratio (SNDR) is a term that is the ratio of signal power to the sum of the noise power and distortion components. Hence the effective number of bits (N_{eff}) of the digitization process is modified as

$$N_{eff} = \frac{\text{SNDR}_{\text{max}}(\text{dB}) - 1.76}{6.02} \qquad (6.4)$$

6.1.2.2 Dynamic range

There exists a range of input amplitudes for which the output SNR of the modulator is positive. As the input signal amplitude increases from a small value the SNR increases proportionally. The input amplitude to the internal ADC/quantizer that contains the signal and the shaped quantization noise also increases proportionally. When the input amplitude reaches a critical amplitude, termed as the maximum stable amplitude (MSA), the internal ADC gets overloaded and as a result the modulator tends to be unstable. Figure 6.4 shows an example plot of the input to the internal ADC as the input amplitude to the modulator is ramped slowly. The MSA is around 88 % of the fullscale at which the input to the ADC starts increasing rapidly.
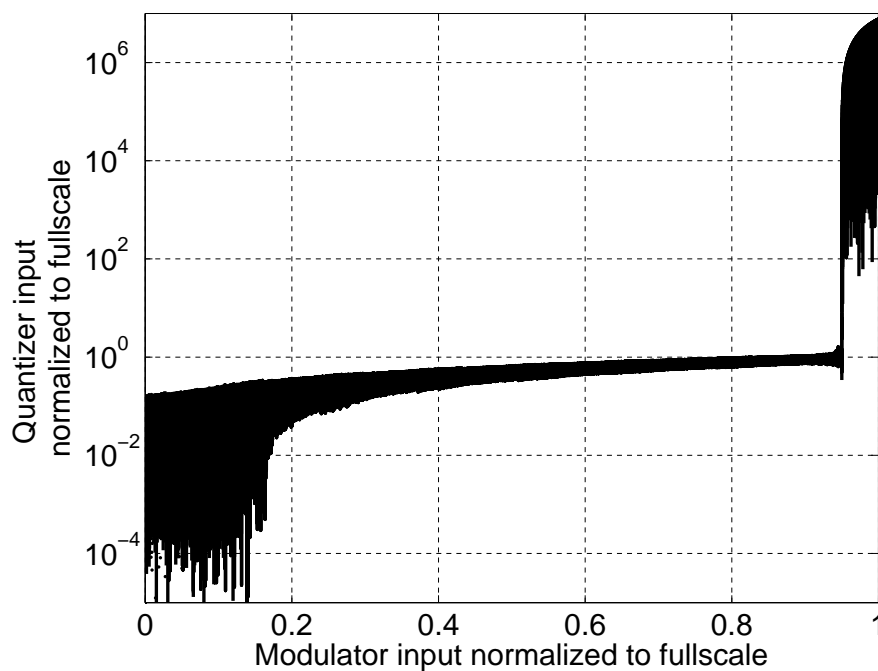
Figure 6.4: Plot of input to the internal ADC when the modulator input is a slow ramp.

For signal amplitudes larger than the MSA, the SNR rapidly drops to zero. The ratio of maximum signal amplitude to the minimum signal amplitude for which the SNR of the modulator remains positive is termed as the dynamic range (DR) of the modulator.

6.2 Design targets for the CTDSM

A large SQNR with effective number of bits of the order of 20 or more can be easily achieved in audio bandwidths with $\Delta\Sigma$ modulators. However, the circuit performance of a CTDSM is limited by electronic noise of resistors and transistors in the circuit, the nonlinearity of the feedback DAC and the loop filter, clock jitter and excess loop delay. The performance summary of a CTDSM that is designed for 15 bit resolution in audio bandwidth is given in Table 6.1.

Table 6.1: Performance summary of the CTDSM [1]

Signal bandwidth/Clock rate	24 kHz / 3.072 MHz
Dynamic range/SNR/SNDR	93.5 dB/92.5 dB/90.8 dB
Active area	0.72 mm^2
Process/Supply voltage	0.18 μm CMOS/1.8 V
Power dissipation	90 μW
Figure of merit	0.049 pJ/level

This work targets to design a CTDSM to achieve SNR of 108 dB (18 bit) by scaling the design [1] for noise and addressing various nonidealities. The design targets for the CTDSM are given in Table 6.2.

Table 6.2: CTDSM design specifications

Signal bandwidth	20 Hz - 24 kHz
SNR/Dynamic Range	108 dB
Quantizer fullscale	3 V$_{ppd}$
Technology	0.18 μm CMOS
Supply voltage	1.8 V

6.3 Nonidealities in a CTDSM

This section contains a brief description of various blocks of a CTDSM, viz. the loop filter, the ADC and the DAC and addresses the effect of various nonidealities in these blocks and other system level issues like clock jitter and excess loop delay.

6.3.1 Clock jitter

If a clock of time period T is jittery then its edges occur at $nT + \Delta t[n]$ where $\Delta t[n]$ is a random variable and $n \in (0,1,2,3 \cdots)$. Hence the sampling instance which is defined by the clock edge has an uncertainty. The sampling uncertainty that occurs in the internal ADC and in the feedback DAC in a CTDSM is illustrated in Figure 6.5.
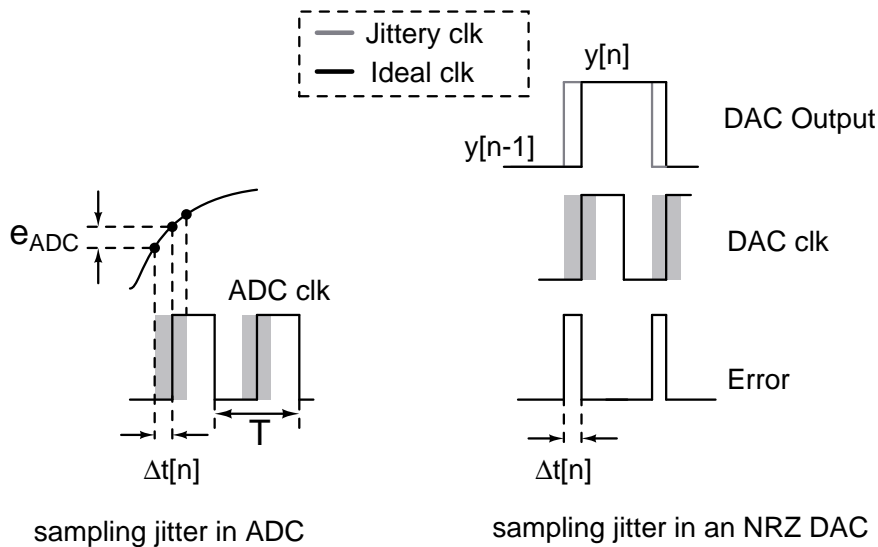
Figure 6.5: Sampling error due to clock jitter in ADC and DAC.

From Figure 6.5 it can be ascertained that an uncertainty in clock edge results in a sampling error that can be modelled as additive noise sources e_{ADC} and e_{DAC} respectively at the input of the ADC and the DAC as shown in Figure 6.6. The sampling error caused
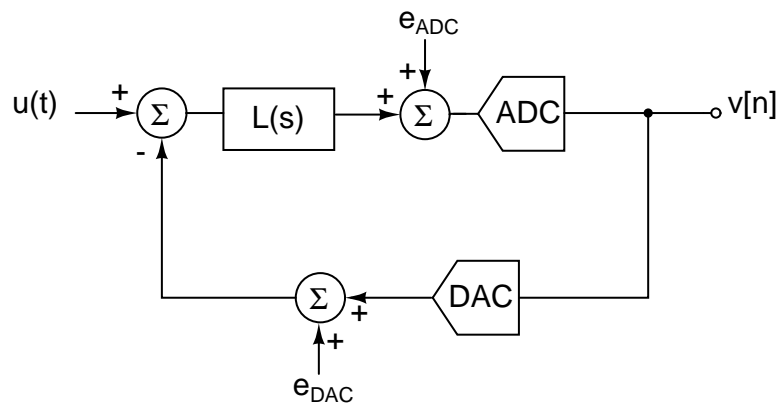
Figure 6.6: Modelling the effect of clock jitter in a CTDSM.

due to jitter in the ADC's clock, e_{ADC}, is noise shaped by NTF and its effect on the per-

formance of the modulator is benign. The sampling error caused due to jitter in the DAC clock, e_{DAC}, for a non return to zero (NRZ) DAC is written as

$$e_{DAC}[n] = (y[n] - y[n-1]) \frac{\Delta t[n]}{T} \tag{6.5}$$

where $y[n]$ is n^{th} output sample of the modulator. The error e_{DAC} when referred at the output of the modulator sees signal transfer function (STF) and directly degrades the in-band SNR. The in-band noise power due to clock jitter for an NRZ DAC can be evaluated as [15][16],

$$J = \frac{\sigma_{\delta t}^2}{T^2} \frac{\sigma_{lsb}^2}{\pi \, \text{OSR}} \int_o^\pi |(1 - e^{-j\omega}) \, \text{NTF}(e^{j\omega})|^2 d\omega \tag{6.6}$$

where $\sigma_{\delta t}^2$ is the variance of the clock jitter and $\sigma_{lsb}^2 = V_{lsb}^2/12$ is the variance of the quantization noise of the internal ADC. Hence multibit CTDSMs that has a smaller V_{lsb} has less sensitivity to clock jitter.

6.3.2 Excess loop delay

To obtain a certain NTF(z), the discrete-time equivalent of the continuous-time loop filter $L(s)$ must be $L(z) = \dfrac{1}{\text{NTF}(z)} - 1$. The discrete-time equivalent of a continuous-time loop filter $L(s)$ is the sampled output of the continuous-time loop filter $L(s)$ whose input is driven by a unit DAC pulse. Figure 6.7 gives a pictorial representation of the discrete-time filter $L(z)$ and its equivalent continuous-time loop filter $L(s)$.
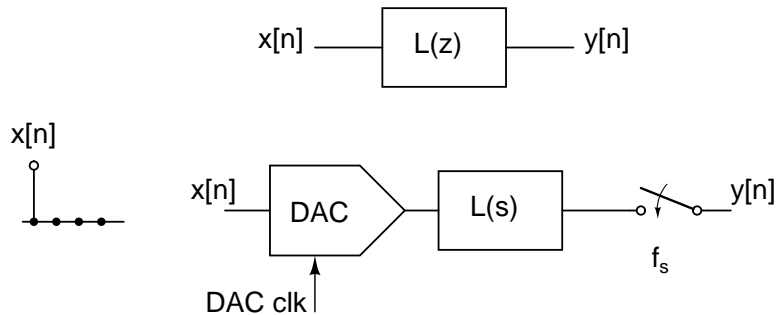
Figure 6.7: Continuous-time and discrete-time loop filter equivalence.

Let $\mathcal{L}^{-1}$ denote the inverse Laplace transform and $\mathcal{Z}^{-1}$ denote the inverse $\mathcal{Z}$ transform. Let $p(t)$ denote the pulse shape of the DAC and $P(s)$ its Laplace transform. Then the equivalence can be mathematically expressed as [17]

$$\mathcal{Z}^{-1}\{L(z)\} = \mathcal{L}^{-1}\{P(s)L(s)\}\Big|_{t=nT_s} \tag{6.7}$$

The ADC has a finite latency which includes the regeneration time of latches. There is also a finite delay in the digital path before the DAC. Hence the DAC is clocked with a delayed ADC clock. This latency or delay, τ, is called as *excess loop delay* (ELD). In the presence of ELD, the equivalent $L(z)$ obtained differs from that of desired. ELD tends to move the poles of the NTF(z) outside the unit circle resulting in NTF peaking leading to instability [17].

The exact effect of the ELD depends upon the pulse shape of the DAC. In case of an NRZ DAC, a delay of τ results in the falling edge of the pulse to cross the sampling instance of the ADC. Hence the order of the system increases by one [18]. In case of an RZ pulse shape, a delay greater than half clock period results in a higher order system. Excess loop delay lesser than one clock cycle can be compensated by adding a zero order path in the loop filter and modifying loop filter coefficients as described in [19]. Compensating for delay greater than one clock cycle is addressed in [20].

6.3.3   Loop filter

The transfer function of the loop filter determines the NTF of the modulator. In a CTDSM the continuous-time loop filter is usually designed with integrators. Active RC integrators are commonly used due to their linearity for large amplitudes. Finite gain and bandwidth of the op-amps used in active RC integrators degrades the performance of the modulator.

6.3.3.1 Effect of finite op-amp gain

Finite DC gain of op-amps results in integrators having a finite DC gain. Therefore the DC gain of the loop filter is finite. Due to the reduced DC loop gain the suppression of quantization noise at low frequencies is reduced. This results in a reduced SQNR. Effect of finite DC gain of op-amps on the NTF is shown in Figure 6.8. A rule of thumb
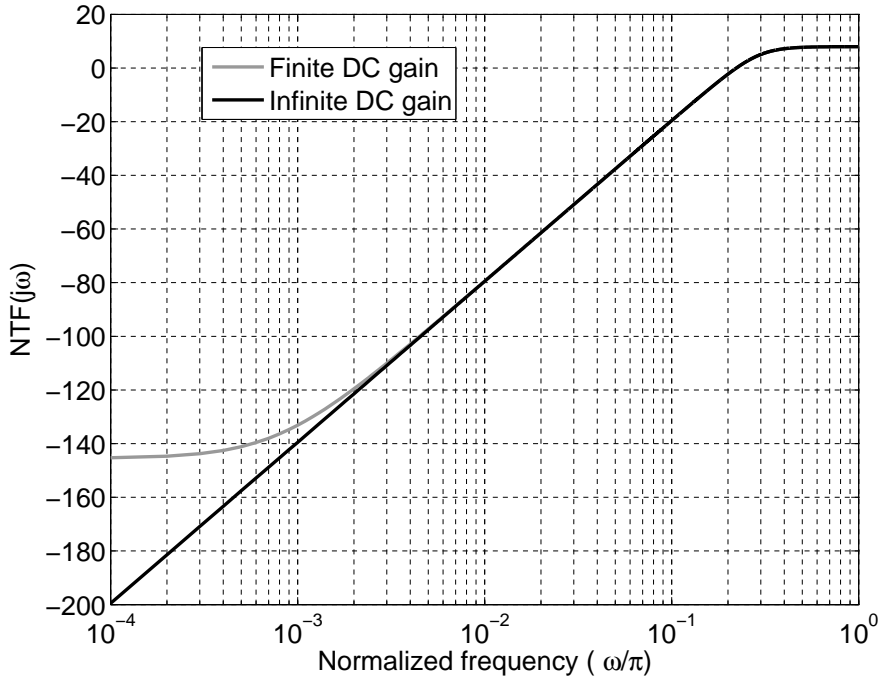
Figure 6.8: NTF magnitude response for finite DC gain of the op-amps.

is that the DC gain of the op-amps be greater than the OSR [21]. This ensures that the additional in-band noise compared to when the DC gain is infinite is less than $0.2\,\mathrm{dB}$.

6.3.3.2 Effect of finite op-amp bandwidth

The transfer function of an op-amp having finite unity gain frequency (UGF), ω_u, is $A(s) = \dfrac{\omega_u}{s}$. Figure 6.9 shows the circuit diagram of an active RC integrator in which the transfer function of the op-amp is $A(s)$. Let $k_1 = \dfrac{1/RC}{\omega_u}$. The transfer function of

41
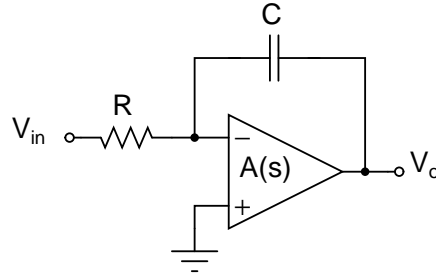
Figure 6.9: Schematic of an active RC integrator.

the integrator is expressed as

$$\frac{V_o(s)}{V_{in}(s)} = \frac{-1}{sRC(1+k_1)} \frac{1}{1 + \dfrac{s}{\omega_u(1+k_1)}} \tag{6.8}$$

From (6.8) it can be inferred that the gain of the integrator is modified from $\dfrac{1}{RC}$ to $\dfrac{1}{RC(1+k_1)}$ and the integrator has an additional pole at $\omega_u(1+k_1)$. The step response of the integrator due to a parasitic pole is a delayed ramp as shown in Figure 6.10. Hence an op-amp with finite UGF modifies the integrator gain and also causes a delay (τ_d) in the step response.
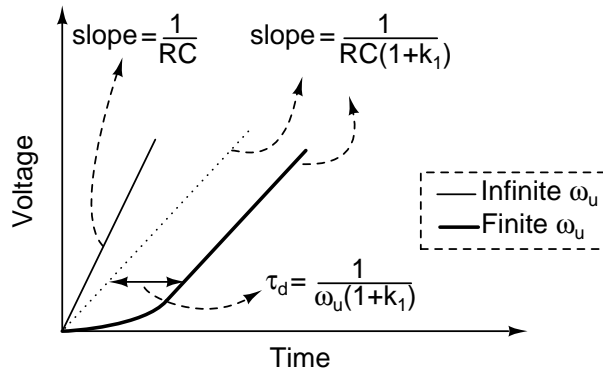
Figure 6.10: Step response of an integrator having finite UGF.

6.3.3.3 Variation of RC time constants

The gain $\left(\frac{1}{RC}\right)$ of an active RC integrator depends on the absolute value of the resistor and the capacitor. Due to process variations and temperature, the fabricated value of the resistors and the capacitors deviate largely from their nominal value. Large variations in

42

the RC time constants can potentially drive the modulator to instability. If all RC time constants in the loop filter decrease from their ideal values, the gain of the loop filter at low frequencies increases. As a result of this, NTF attenuation at low frequencies increases. By the principle of *Bode sensitivity integral* the NTF gain near $f_s/2$ increases [22]. This reduces the MSA and the dynamic range of the modulator[13]. The opposite occurs when RC time constants increase. The variations in NTF for $\pm 30\%$ variations in RC time constants is shown in Figure 6.11. Variation in RC time constants can be reduced by trimming all the integrating resistors or all the integrating capacitors or the both.
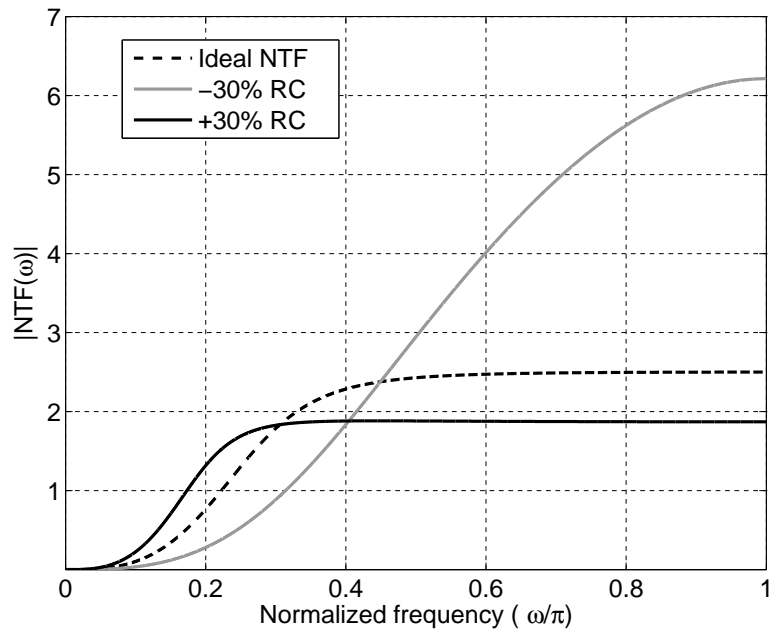
Figure 6.11: Variation of the NTF for $\pm 30\%$ change in RC time constants.

6.3.4 ADC

The internal ADC samples and quantizes the signal from the loop filter and gives the digital output of the modulator. A four bit flash ADC is used in this design. A flash ADC that has the least conversion time is usually employed in a $\Delta\Sigma$ modulator because the conversion time of the internal ADC determines the maximum clock speed of the modulator.

43

A multibit flash ADC has a resistive ladder that produces the reference voltages and latches that resolves the signal to various levels. Mismatch between the transistors in the latches and the mismatch among the resistors in the resistive ladder results in the quantization intervals being unequal. These mismatches can be modelled as an additive error to the reference voltages. The spectrum of the modulator's output when the standard deviation of the mismatch error in the reference voltages is 0.25 LSB is shown in Figure 6.12.
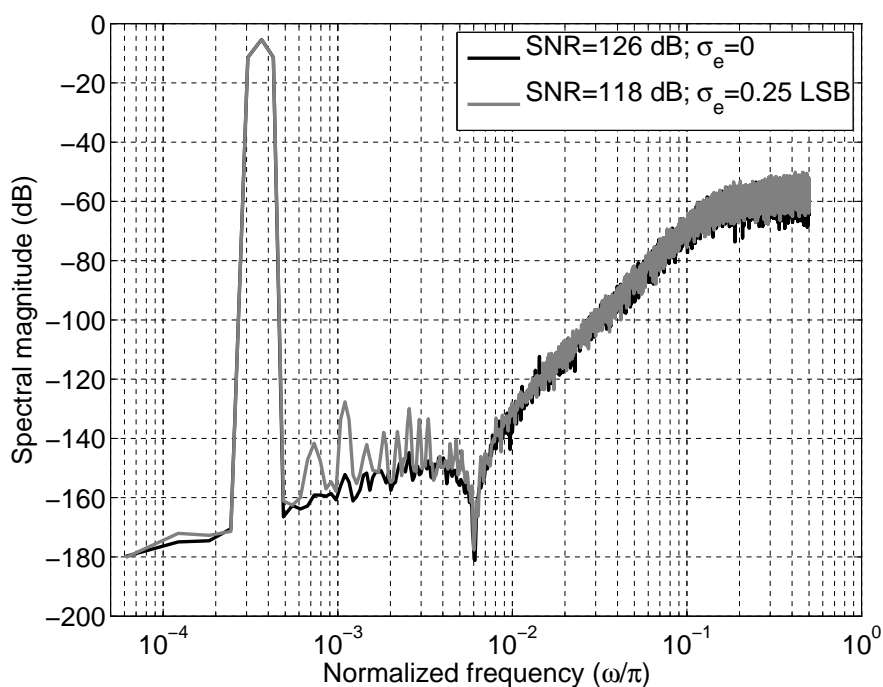
Figure 6.12: Modulator's spectrum for 0.25 LSB error in the references.

Mismatch errors are in general reduced by increasing the area of the device. The appropriate sizing of the latch transistors and the ladder resistors are given in Section 8.2.

6.3.5 DAC

The DAC converts the digital output from the ADC to an analog signal that is fed back to the loop filter. Since the DAC is present in the feedback part of a negative feedback system, the accuracy requirements of the DAC are as high as that of the modulator's performance. Mismatch among unit elements in the DAC causes nonlinearity in the

DAC transfer characteristics. This is shown in Figure 6.13.
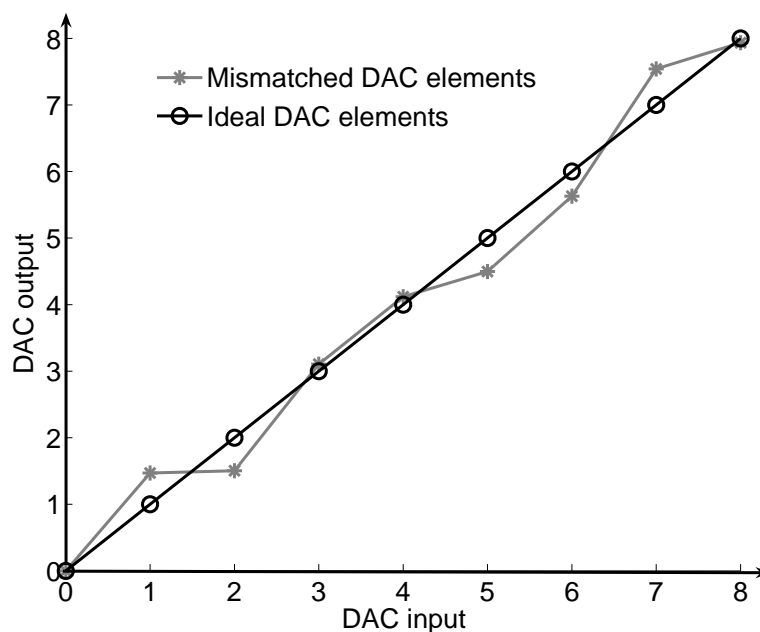
Figure 6.13: Transfer characteristic of a DAC with mismatched elements.

This nonlinearity in the DAC causes the high frequency quantization noise to fold back to the in-band and causes the in-band noise to increase. The nonlinearity in the DAC causes the output of the modulator to be nonlinearly related to the input and hence harmonics of the input signal are seen in the output spectrum. Figure 6.14 shows the spectrum of the output of the modulator when its fifteen level thermometer DAC elements have 0.3 % mismatch. Techniques like dynamic element matching [23] (DEM) and calibration [24] are used to mitigate the effects of element mismatch in the DAC. Details on the sizing of the DAC elements and the DEM technique are discussed in Chapter 9.

6.4 Block level design

This section deals with the choice of system level parameters of the CTDSM to achieve 18 bit SNR. Appropriate choice of the noise transfer function and its macromodel simulation results are presented first. Then the details of scaling the circuit for noise is given.
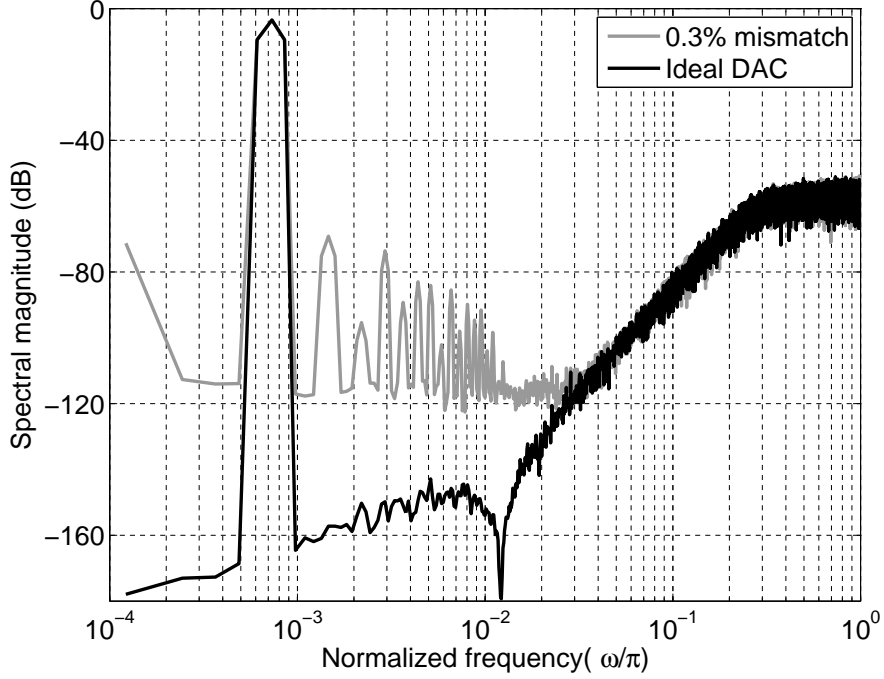
Figure 6.14: Modulator's spectrum for 0.3% mismatched DAC elements.

6.4.1 Choice of the NTF

An oversampling ratio of sixty four is chosen which corresponds to a sampling frequency of f_s=3.072 MHz for the signal bandwidth of 24 kHz. The NTF is designed using the $\Delta\Sigma$ toolbox for MATLAB [13]. A third order NTF with an out-of-band gain (gain of the NTF at $f_s/2$) of 2.5 is chosen. NTF with complex zeros are chosen to maximize the in-band SQNR. The designed NTF is

$$\text{NTF}(z) = \frac{(z-1)(z^2 - 1.999z + 1)}{(z-0.4169)(z^2 - 0.8774z + 0.3803)} \tag{6.9}$$

Macromodel simulations of the modulator that has this NTF and a four bit quantizer gives a peak SQNR of 127.5 dB and the dynamic range is 125 dB. A sample output spectrum of the modulator corresponding to a sine wave input is shown in Figure 6.15(a). The MSA of the modulator is estimated by simulating the modulator with a slow ramp as input and observing the input of the quantizer. The plot of the quantizer input versus the input amplitude is shown in Figure 6.15(b). The input amplitude at which the quantizer input crosses the fullscale and starts increasing rapidly is the MSA. The MSA of
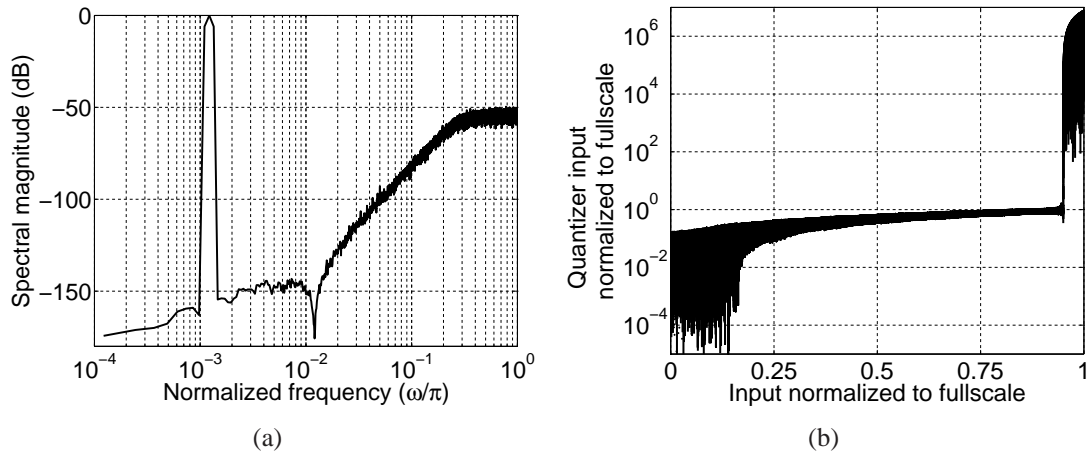
Figure 6.15: Macromodel simulation results: (a) Spectrum of the modulator output, (b) Plot of quantizer input as a function of input amplitude.

this modulator is around 88 %.

6.4.2 Designing for noise

The peak SQNR of the modulator corresponding to the NTF in (6.9) is 127.5 dB. However, in a circuit level implementation the performance of the modulator is limited by the intrinsic noise from various active and passive components in the system. Various noise sources in a CTDSM are

1. Thermal noise generated by resistors of integrators

2. Thermal noise generated from MOS transistors in op-amps

3. Flicker or 1/f noise generated by MOS transistors in op-amps

Voltage noise equivalent from resistors is reduced by reducing the value of the resistor. Input referred thermal noise (voltage) of a MOS transistor is reduced by increasing the transconductance, g_m, of the transistor and the flicker noise is reduced by increasing the length of the transistor.

The $\Delta\Sigma$ modulator is designed that its performance is limited by the random noise. To achieve a peak SNR of 108 dB for a quantizer range of ± 1.5 V and MSA of 88 %, the input referred noise of the modulator is constrained by the following relationship.

$$20 \log_{10} \frac{0.88 \times 1.5/\sqrt{2}}{\text{Integrated noise voltage}} = 108 \, \text{dB} \qquad (6.10)$$

This gives the constraint on the input referred integrated noise voltage as $V_{eqn} = 3.7 \, \mu V_{rms}$. Figure 6.16 shows the block diagram of the CTDSM emphasizing the noise contribution from various elements. The dominant noise contributing elements are the first integrating resistors (R_1), the DAC resistors (R_{dac}) and the first integrating op-amp. The noise from other components are attenuated by the large gain of the first stage when referred at the input.
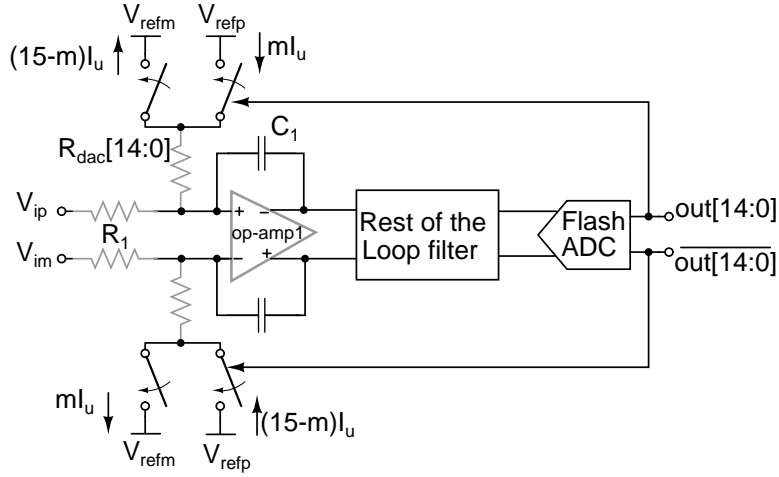
Figure 6.16: Circuit diagram of the CTDSM showing the important noise contributing elements (shaded gray).

The input referred noise equivalent from all these components is easily evaluated with the help of the single ended equivalent model of the CTDSM in Figure 6.17.

The term $S_{vopa}(f)$ represents the voltage noise spectral density of the first integrating op-amp. The term $S_{vr1}(f)$ represents the voltage noise spectral density of the first integrating resistor (R_1) and is written as

$$S_{vr1}(f) = 4 \, kT \, R_1 \qquad (6.11)$$

48
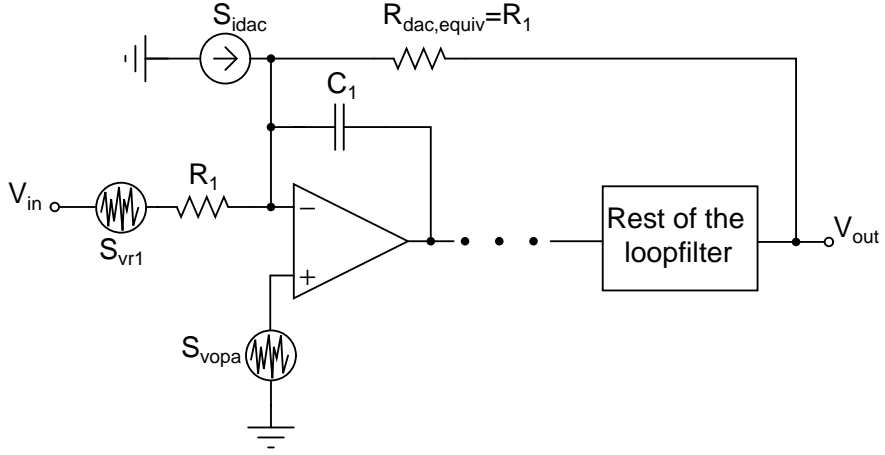
Figure 6.17: Equivalent circuit of the modulator for noise analysis.

where k is the Boltzmann constant and T is the absolute temperature. The term $S_{idac}(f)$ represents the current noise spectral density of the fifteen differential thermometer DAC resistors (R_{dac}) and is written as

$$S_{idac}(f) = 15\frac{4kT}{R_{dac}} \tag{6.12}$$

The total input referred voltage noise spectral density (S_{veq}) of the modulator is

$$S_{veq}(f) = 2\,S_{vr1}(f) + 4S_{vopa}(f) + 2\,S_{idac}(f)R_1{}^2 \tag{6.13}$$

The factor of two in the first and the third terms in the above equation accounts for the additional noise contribution in the differential implementation of the modulator. The input referred noise spectral density, $S_{veq}(f)$, is integrated in the desired bandwidth (20 Hz - 24 kHz) to obtain the input referred mean squared noise voltage (V_{eqn}^2).

The input resistor is chosen to be a small value of $R_1 = 4\,\text{k}\Omega$. The input referred integrated noise voltage due the first integrating resistors in the bandwidth 20 Hz - 24 kHz at a temperature of 300 K is

$$\sqrt{\int_{20\,Hz}^{24\,kHz} 2\,S_{vr1}(f)df} = 1.78\,\mu V_{rms} \tag{6.14}$$

49

The first op-amp is designed so that its input integrated noise voltage in the bandwidth 20 Hz - 24 kHz at 300 K is,

$$\sqrt{\int_{20\,Hz}^{24\,kHz} S_{vopa}(f)df} = 1\,\mu V_{rms} \tag{6.15}$$

Given the input resistor, R_1, the DAC unit cell resistor, R_{dac}, is chosen such that the STF of the modulator is unity. The relationship between R_{dac} and R_1 under this condition is found as follows:

The LSB voltage of the four bit internal ADC that has its fullscale of 3 V is 187.5 mV. Let $I_u = \dfrac{V_{refp(m)} - V_{cm}}{R_{dac}}$ represent the current flowing through a unit cell DAC resistor R_{dac}. In this design V_{refp}, V_{refm} and V_{cm} are 1.8 V, 0 V and 0.9 V respectively. If the thermometer input control for the DAC has m logic ones then the differential current that is injected into the loop filter is $2\{mI_u - (15 - m)I_u\} = (4m - 30)I_u$ (Refer Figure 6.17). Hence the LSB current of a differential thermometer DAC is $4I_u$. The equivalent LSB voltage of the DAC is hence $4I_uR_1$. To have unity gain for the modulator, the LSB voltage of the DAC and that of the ADC has to be equal. Hence $4I_uR_1 = 187.5$ mV. This gives $R_{dac} = 19.2\,R_1 = 76.8\,k\Omega$. Hence the input referred noise of the DAC resistors is

$$\sqrt{\int_{20\,Hz}^{24\,kHz} 2\,S_{idac}(f)R_1{}^2 df} = 1.57\,\mu V_{rms} \tag{6.16}$$

The input referred noise power from various components of the ADC are summarized in Table 6.3. The input referred noise voltage of the ADC is $\sqrt{9.61\,pV^2} = 3.1\,\mu V_{rms}$.

Table 6.3: Noise contributions from various elements

Component	Input referred noise power(pV^2)	% of total noise power
First integrating resistor (R_1)	3.17	32.8
DAC Resistor (R_{dac})	2.47	25.8
First integrating op-amp	4.0	41.4
Total	9.61	100

The next three chapters deals with the circuit design of the individual blocks of the modulator, the loop filter, the four bit flash ADC and the thermometer DAC.

CHAPTER 7

Continuous-time loop filter

7.1 Loop filter topology

The structure of the loop filter that is used in this modulator is CIFF (Cascade of integrators feedforward). Another possible topology is CIFB (Cascade of integrators with distributed feedback). The block diagrams of the CIFF and CIFB structures for a third order loop filter are shown in Figure 7.1 and Figure 7.2 respectively. In CIFF structure
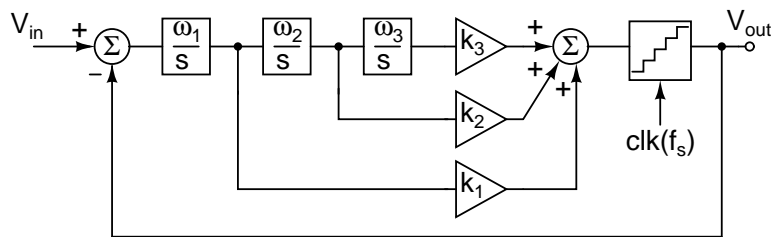
Figure 7.1: Third order loop filter: CIFF structure.
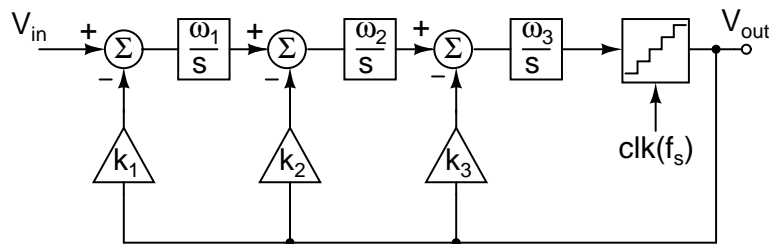
Figure 7.2: Third order loop filter: CIFB structure.

the first integrator has a very small component of the input signal and its strength increases along the subsequent integrators [25]. The opposite occurs in a CIFB structure. In a CIFF structure the nonlinearities due to large input signal component in the subsequent integrators are noise shaped. Hence the nonlinearity of the first integrator alone is critical in a CIFF structure whereas the linearity of the first few integrators are critical in a CIFB structure [25]. A CIFF structure is chosen for the loop filter in this design to obtain better linearity.

7.2 Integrator topology
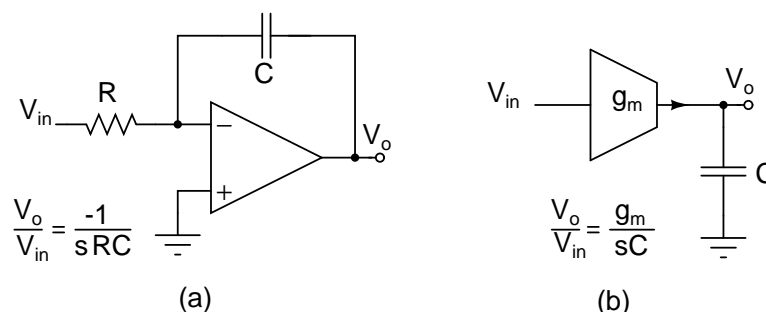
Figure 7.3: Integrator types: (a) Active RC integrator, (b) g_m-C integrator.

Active RC integrators and g_m-C integrators are two of the very commonly used integrator realizations. Schematic representations of an active RC integrator and a g_m-C integrator are shown in Figure 7.3. For a given signal swing an active RC integrator has a better linearity due to the presence of negative feedback. The linearity of the DAC is better in an active RC integrator where the feedback DAC output is connected to the virtual ground of the op-amp. Active RC integrators are chosen in this design to obtain good linearity.

7.3 Realization of the loop filter

The discrete-time loop filter transfer function for the NTF described in (6.9) is obtained as

$$L(z) = \frac{1 - \text{NTF}(z)}{\text{NTF}(z)} = \frac{1.7043(z^2 - 1.322z + 0.4937)}{(z-1)(z^2 - 1.999z + 1)} \tag{7.1}$$

The continuous-time loop filter transfer function is obtained using the equivalence described in 6.7. The DAC used in this modulator has a non return to zero (NRZ) pulse shape. The equivalent continuous-time loop filter is obtained using the *d2c* command in MATLAB.

$$L(s) = \frac{1.2243(s^2 + 0.7049s + 0.2396)}{s(s^2 + 0.001446)} \tag{7.2}$$

This loop filter $L(s)$ corresponds to a sampling frequency of 1 Hz. The sampling frequency (f_s) in this design is 3.072 MHz. The CIFF loop filter scaled to the frequency f_s is shown in Figure 7.4. The feedback resistor R_z creates the complex poles of the loop filter. The integrators have been scaled such that swings at the output of each integrator is approximately ± 500 mV. The next sections give the circuit descriptions of the op-amps in the loop filter.
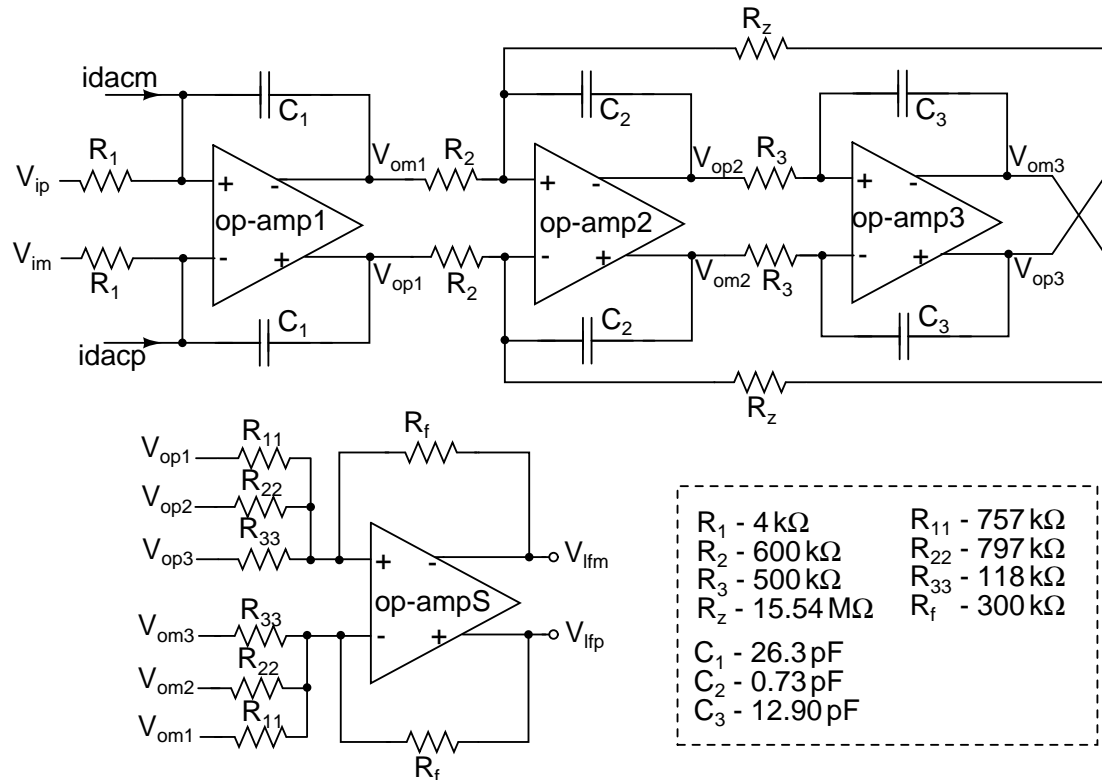
Figure 7.4: Realization of the CIFF loop filter.

7.4 First integrating op-amp

Op-amps with high DC gain and large output swings are designed easily with two stage Miller compensated structure. The drawback of this structure is that the stability is attained at the expense of bandwidth reduction. Feedforward structure for op-amps achieves the same bandwidth at a lesser power [26]. Op-amps for all integrators in the design are realized with feedforward structure. The block diagram of a feedforward

op-amp is given in Figure 7.5. Transconductances g_{m1} and g_{m2} realize the high gain
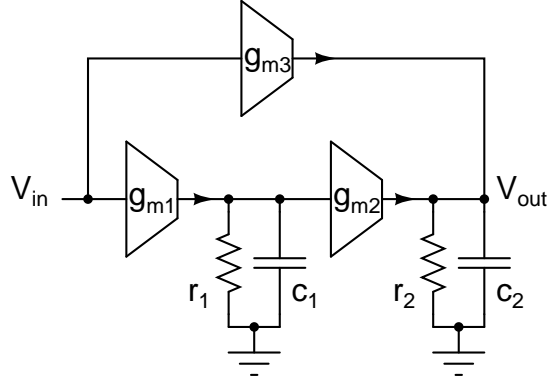
Figure 7.5: Block diagram of a feedforward op-amp.

at low frequencies. This path has two poles and the magnitude response rolls off at -40 dB/decade at high frequencies. The feedforward path through the transconductance g_{m3} rolls off at -20 dB/decade at high frequencies and sets the high frequency gain of the op-amp. Hence the op-amp is made stable with a unity gain frequency $\omega_u = \dfrac{g_{m3}}{c_2}$. The transfer function of the op-amp $A(s)$ can be expressed as

$$
\begin{aligned}
A(s) &= \left(\frac{g_{m1}g_{m2}r_1}{1 + sc_1r_1} + g_{m3} \right) \frac{r_2}{1 + sc_2r_2} \\
&= \frac{g_{m1}g_{m2}r_1r_2 \left(1 + \dfrac{g_{m3}}{g_{m1}g_{m2}r_1} \right) \left(1 + \dfrac{sc_1g_{m3}}{g_{m1}g_{m2}(1 + \frac{g_{m3}}{g_{m1}g_{m2}r_1})} \right)}{(1 + sc_1r_1)(1 + sc_2r_2)} \\
&\approx \frac{g_{m1}g_{m2}r_1r_2 \left(1 + \dfrac{sc_1g_{m3}}{g_{m1}g_{m2}} \right)}{(1 + sc_1r_1)(1 + sc_2r_2)}
\end{aligned}
\tag{7.3}
$$

The op-amp is designed such that its input referred integrated noise in the bandwidth 20 Hz-24 kHz is $1\,\mu V_{rms}$. To reduce the flicker noise contribution PMOS transistors are used for the input pair. The second stage is designed with sufficient bias current to provide the error current (the difference between the DAC and the input current ≈ 4 LSB DAC current) to its integrating capacitor and to provide current to the load that comprises of the second integrator and the summing amplifier. The schematic of the op-amp is shown in Figure 7.6. The open loop AC response and the loop gain of the
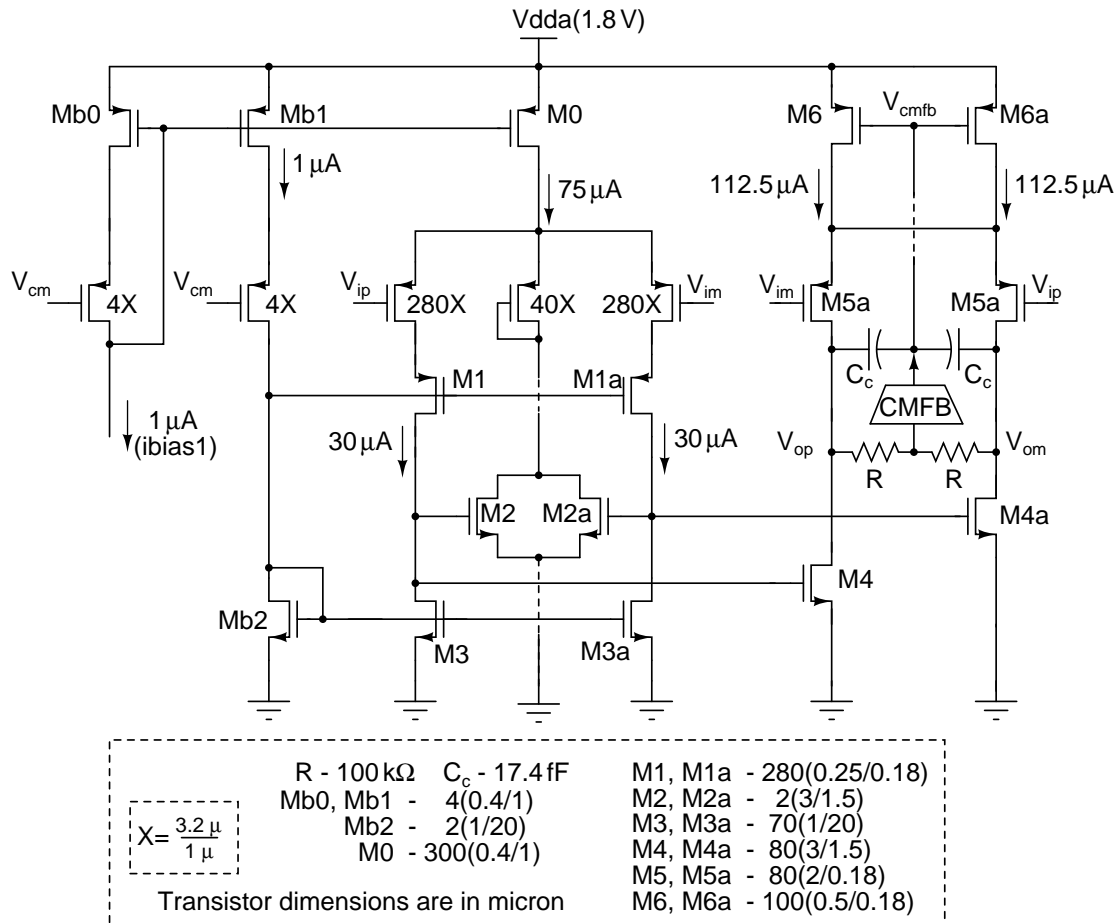
Figure 7.6: Schematic of the first op-amp.

op-amp configured as an integrator is shown in Figure 7.7. The performance summary of the op-amp is given in Table 7.1.
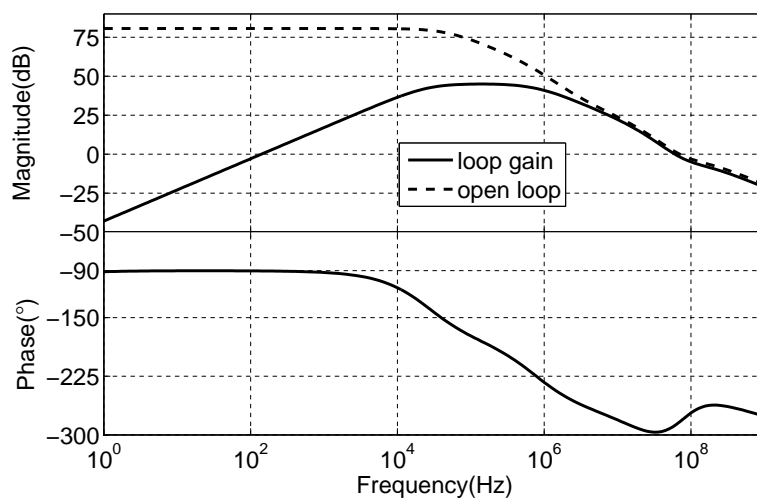
Figure 7.7: Frequency response of the first op-amp.

Table 7.1: Performance summary of the first op-amp/integrator

Parameter	Value
DC gain	80 dB
Unity gain frequency	69 MHz
Phase margin	70°
Integrated noise (20 Hz - 24 kHz)	$1\,\mu V_{rms}$
Current consumption	$305\,\mu A$

7.5 The second and the third integrating op-amps

The op-amps used for the second and the third integrators are the scaled down versions of the first op-amp. The nonlinearity and the noise of these op-amps are attenuated by the large gain of the first integrator when referred to the input of the $\Delta\Sigma$ modulator. The schematic of the op-amp used in the second and the third integrator is shown in Figure 7.8.
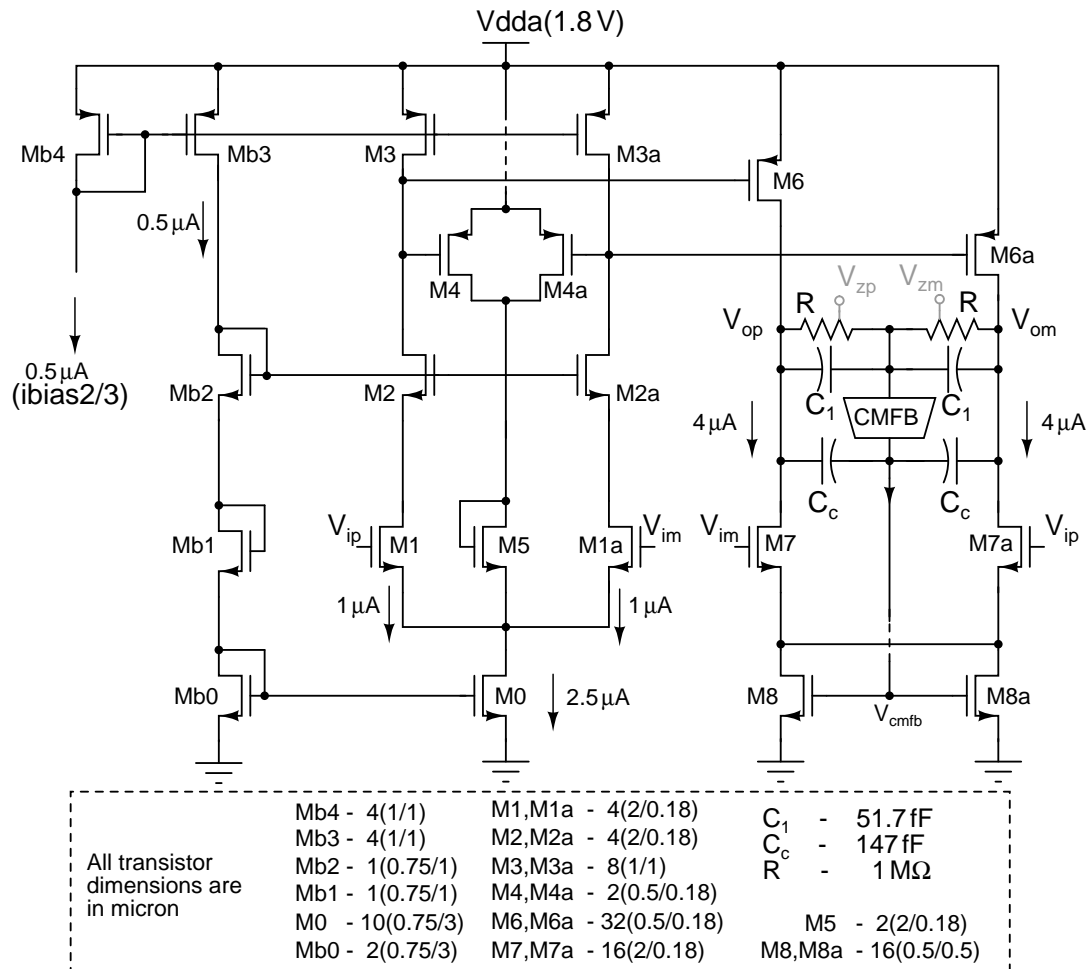
Figure 7.8: Schematic of the second and the third integrating op-amps.

7.5.1 Implementation of the complex poles

The zeros of the NTF are the poles of the loop filter. The optimized complex zeros of the NTF are realized by creating a resonator in the loop filter transfer function. A resonator is formed around the second and the third integrator using negative feedback which moves a pair of poles from the origin to 18.59 kHz. The location of the complex poles in the circuit is controlled by the feedback resistor (R_z) from the third integrator output to the second integrator input as shown in Figure 7.4. The complex pole frequency is given by

$$f_p = \frac{1}{2\pi\sqrt{R_z C_2 R_3 C_3}} \tag{7.4}$$

A very large value of the resistor R_z (15.54 MΩ) is necessary to obtain the pole at such a low frequency. This requires a very long length of the resistor that has a large parasitic capacitance which introduces delay in the resonator loop. This moves the poles of the resonator from the $j\omega$ axis to its right. Hence the attenuation of the NTF at the resonant frequency becomes finite. To overcome this problem the concept of "Y $-$ Δ" transformation is used to realize a larger equivalent resistor with a smaller resistor at the expense of extra power consumption. The "Y $-$ Δ" transformation is explained in Figure 7.9.
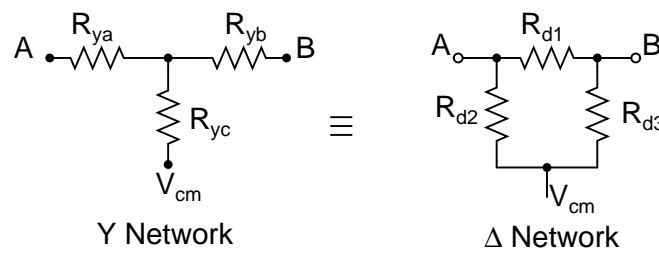
Figure 7.9: Illustration of Y $-$ Δ transformation.

$$R_{d1} = R_{ya} + R_{yb} + \frac{R_{ya}R_{yb}}{R_{yc}} \tag{7.5}$$

To realize a large resistance R_{d1} between nodes A and B, the third term in (7.5) is made large by choosing a smaller R_{yc}. In this resonator implementation the nodes A and B are the virtual ground node of the second op-amp and the output of the third integrator

respectively. The implementation of the resonator is shown in Figure 7.10.
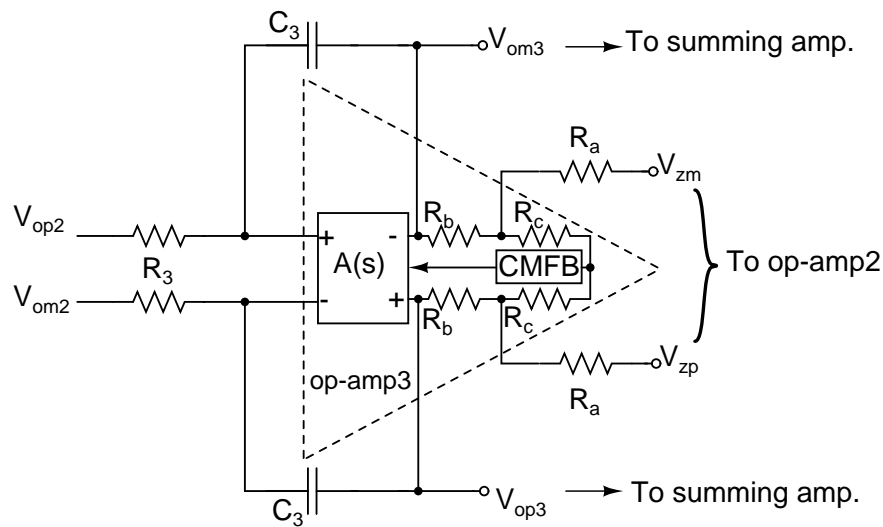
Figure 7.10: Implementation of complex poles with the CMFB.

The resistors R_b and R_c are the part of the common mode feedback (CMFB) loop that stabilizes the output common mode of the second stage of the third op-amp. The sum of R_b and R_c is $1\,\text{M}\Omega$. The value of R_a is chosen according to (7.5) such that it implements a resistor of value of $R_{d1} = 15.54\,\text{M}\Omega$. The value of R_a, R_b, R_c are chosen as $72.85\,\text{k}\Omega$, $995\,\text{k}\Omega$, $5\,\text{k}\Omega$ respectively. The load for the third op-amp is $R_b + R_c \| R_a \approx R_b + R_c = 1\,\text{M}\Omega$.

7.6 Summing amplifier

A summing amplifier is required in CIFF architecture to scale and sum the output of all integrators. The output of the summing amplifier is fed to the four bit flash ADC. The summing amplifier needs to swing to the fullscale range $\pm 1.5\,\text{V}$. The feedforward op-amp that is used in the integrators cannot be employed here because its swing limit is approximately $\pm 2\,\text{V}_T$ ($\pm 1\text{V}$). Hence a two stage miller compensated op-amp is used for the summing amplifier. The output stage is designed such that it has sufficient strength to drive the flash ADC and supply the current to the feedback resistor. The schematic of the summing op-amp is shown in Figure 7.11. The performance summary

of the summing op-amp is given in Table 7.2.
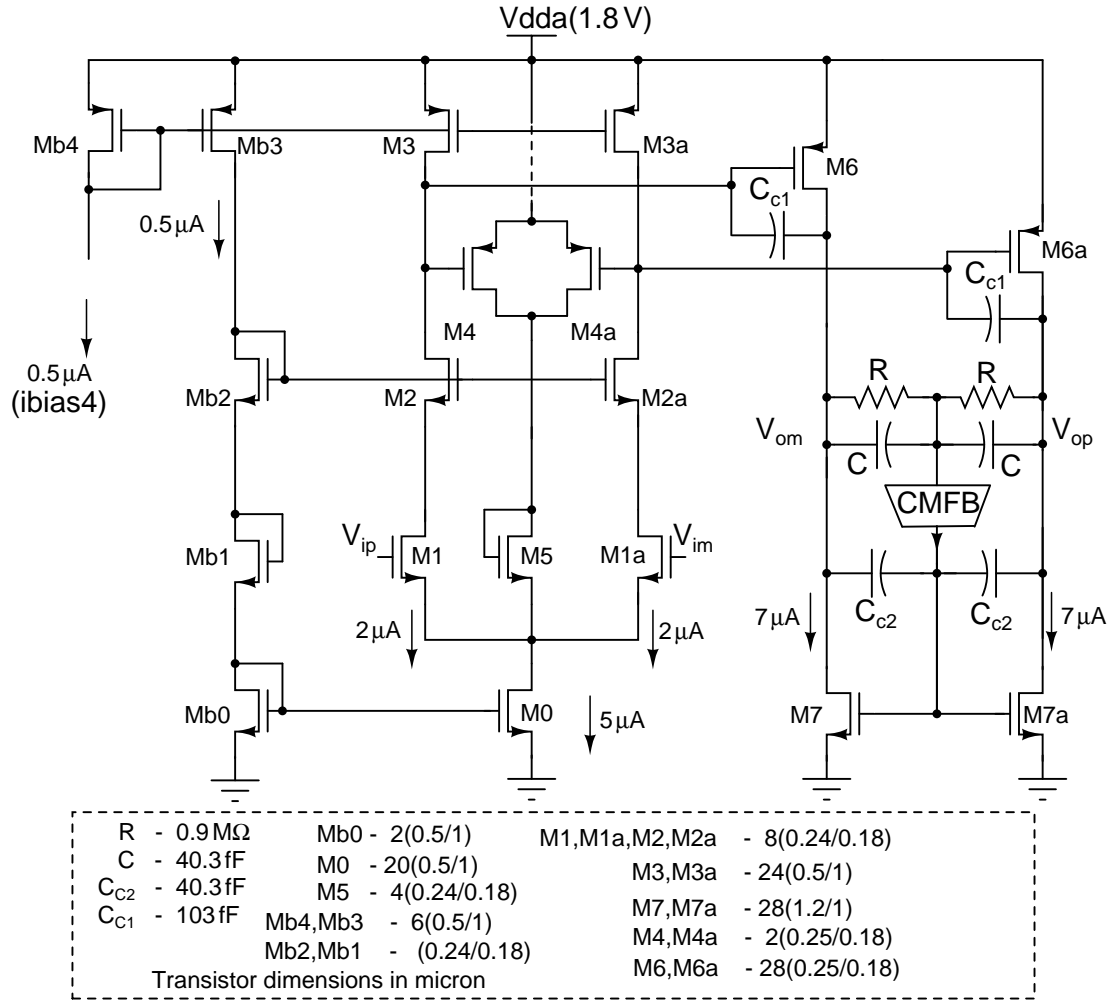
Figure 7.11: Schematic of the summing op-amp.

Table 7.2: Performance summary of the summing op-amp

Parameter	Value
Open loop DC Gain	69 dB
Loop unity gain frequency	10 MHz
Phase Margin	46°
Current consumption	20.5 μA

Excess loop delay as described in 6.3.2 is compensated by adding a zero order path from the DAC output to the summing amplifier. To nullify the effect of the excess loop delay, the gain of the direct path and gains of higher order path through integrators are modified as described in [19]. An easier way of implementing the direct path without an extra DAC is to differentiate the first integrator output [1]. This is accomplished

60

by introducing a capacitor C_c in parallel with the resistor R_{11}. The final loop filter's schematic is shown in Figure 7.12.
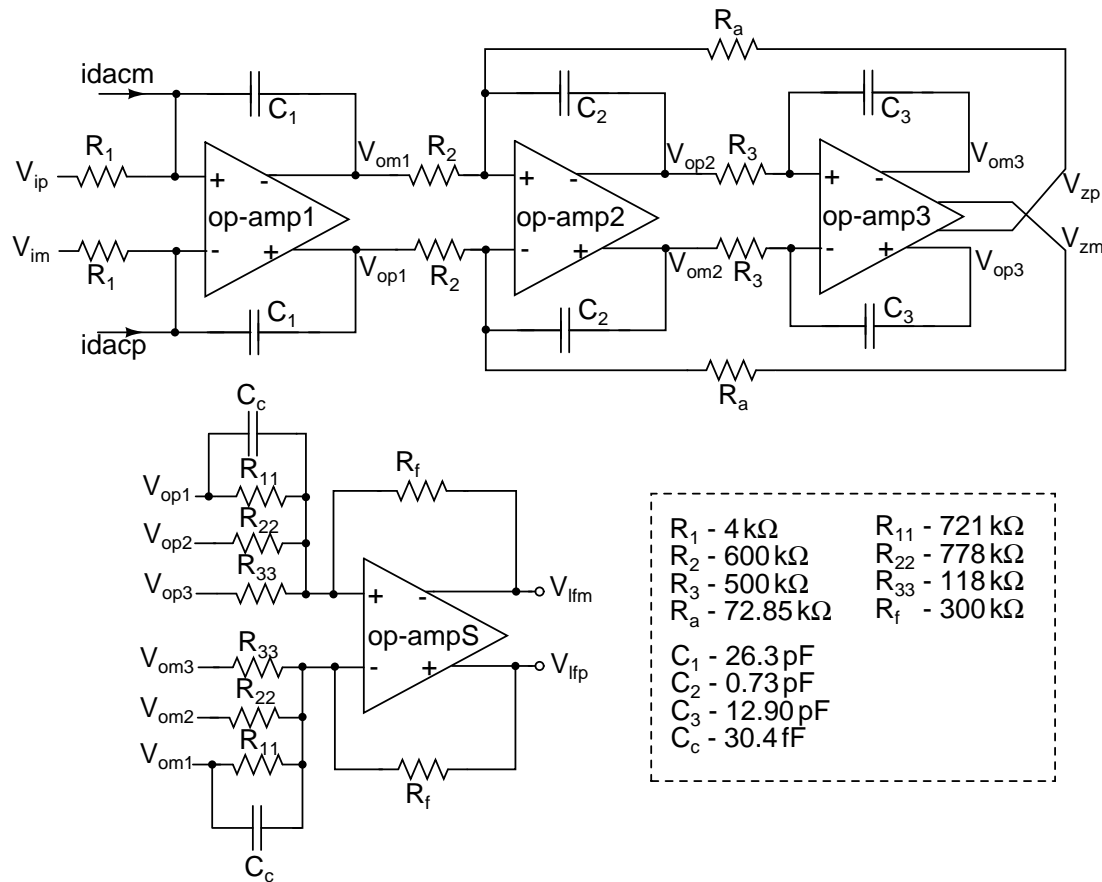
Figure 7.12: Loop filter with excess loop delay compensation.

7.7 Tuning of R & C variations

The high resistivity polysilicon resistor is used as the integrating resistor and the metal-insulator-metal (MIM) is used as the integrating capacitor. In the process used for this design, the tolerance of these resistors and capacitors are $\frac{\Delta R}{R} = \pm\, 35\,\%$ and $\frac{\Delta C}{C} = \pm\, 15\,\%$ respectively. Hence the RC time constant varies from -44.75 % to 55.25 %. As described in section 6.3.3.3, large variations in the RC time constants can lead to modulator instability and trimming of these elements is necessary to restore the loop filter transfer function. The NTFs corresponding to the maximum and minimum deviation in time constants in this process are plotted in Figure 7.13.
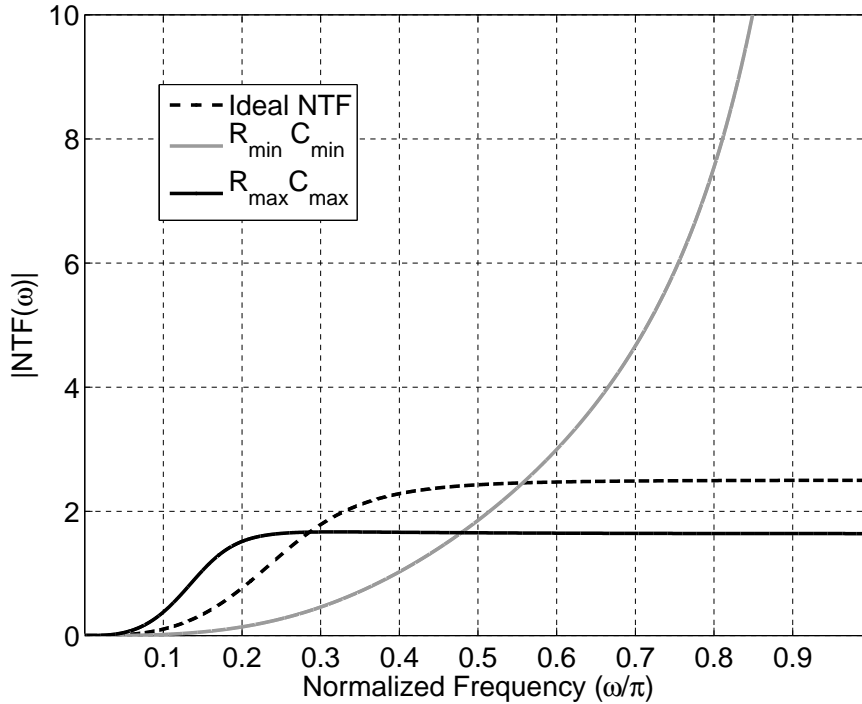
Figure 7.13: NTF variation for $\pm 35\%$ R variation and $\pm 15\%$ C variation.

In this design the integrating capacitors are trimmed by realizing the capacitor as a combination of a fixed capacitor C_f and a bank of seven switchable capacitors each of value C_t. This is shown in Figure 7.14. The total capacitance between nodes 'A' and 'B' can be vary from C_t to $C_f + 7C_t$ in discrete steps of C_t based on the thermometer control signal ctrl[6:0]. Hence the RC time constant can be adjusted in discrete steps to make it closer to the ideal value.
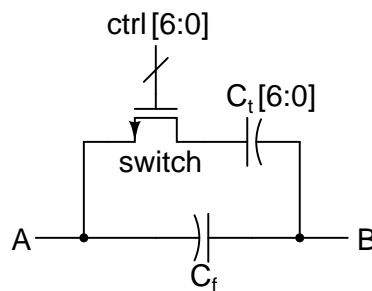
Figure 7.14: Integrating capacitor tuning bank.

The thermometer control ctrl[6:0] is obtained from a three bit binary signal bwc[2:0] with the help of a binary to thermometer converter. The signal bwc[2:0] is generated external to the chip. The terminal 'A' is connected to the virtual ground node of the op-

amps to ensure that the gate-source voltage of the MOSFET switch is constant. Hence the resistance of the switch does not vary even when the integrator is processing the signal. This reduces the distortion caused by the MOS switch. For three bit tuning, the values of C_t and C_f are chosen by solving the following equations.

$$C_f + 3C_t = C_{req} \tag{7.6}$$

$$\frac{C_t}{C_f} = R_{tio} \tag{7.7}$$

Here C_{req} is the capacitor value to be realized for the integrator. Let τ_i be the time constant to be realized and τ_a be the time constant obtained after tuning. The value of R_{tio} is chosen to make $\dfrac{\tau_a}{\tau_i}$ close to unity across all process corners. The ratio $\dfrac{\tau_a}{\tau_i}$ can be written as.

$$\frac{\tau_a}{\tau_i} = \frac{(R + \Delta R)\{(C_f + \Delta C_f) + k(C_t + \Delta C_t)\}}{R(C_f + 3C_t)} \tag{7.8}$$

All fabricated capacitors are nominally identical, i.e. $\dfrac{\Delta C_t}{C_t} = \dfrac{\Delta C_f}{C_f} = \dfrac{\Delta C}{C}$ Hence (7.8) is written as,

$$\frac{\tau_a}{\tau_i} = \frac{(1 + \dfrac{\Delta R}{R})(1 + \dfrac{\Delta C}{C})(1 + kR_{tio})}{(1 + 3R_{tio})} \tag{7.9}$$

The parameter k is a number which decides how many capacitors (C_t) are connected in parallel with C_f. The value of k is decided by tuning bits, bwc[2:0], and $k \in \{0,1,2,3...7\}$. It can be seen that the best tuning obtained depends only on the number of tuning bits and the ratio R_{tio}.

The optimal value of R_{tio} is the one which evaluates (7.9) closer to unity for $\frac{\Delta R}{R}$ in the range (-0.35 to 0.35) and $\frac{\Delta C}{C}$ in the range (-0.15 to 0.15) with the appropriate value for the tuning variable k. The optimal value of R_{tio} is found with the help of MATLAB. $\dfrac{\tau_a}{\tau_i}$ is evaluated for $\frac{\Delta R}{R}$ and $\frac{\Delta C}{C}$ with in its permissible deviation to an accuracy of 0.001. For each value of $\frac{\Delta R}{R}$ and $\frac{\Delta C}{C}$ the expression (7.9) is evaluated to minimum deviation from unity by correct choice of the tuning variable k. It is found that for a value of $R_{tio} = 0.293$, $\dfrac{\tau_a}{\tau_i}$ deviates least from unity.
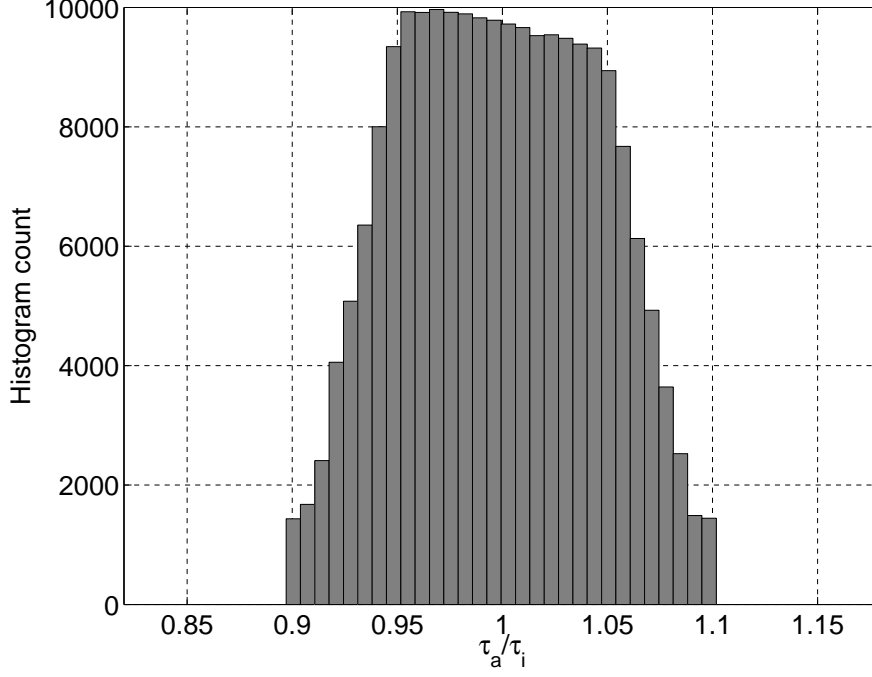
Figure 7.15: Histogram of $\dfrac{\tau_a}{\tau_i}$ for $\mathrm{R_{tio}} = 0.293$.

For the value of $R_{tio} = 0.293$ and for $\frac{\Delta R}{R}$ and $\frac{\Delta C}{C}$ in its permissible range, $\dfrac{\tau_a}{\tau_i}$ is evaluated. A histogram plot of this is $\dfrac{\tau_a}{\tau_i}$ is shown in Figure 7.15. It can be found from this graph that the variation in time constant is constrained to $0.9\,\tau_i$ to $1.1\,\tau_i$. The untrimmed variations in the time constants (-44.75 % to 55.25 %) is reduced to $\pm\,10$ % with three bit trimming. The variation in NTF corresponding to $\pm\,10$ % variation in time constants is shown in Figure 7.16.

The dynamic range and the peak SQNR of the modulator are evaluated using MATLAB for both cases, with and without tuning. The results are tabulated in Table 7.3. It is found that three bit tuning is sufficient enough to reduce the performance variation by less than $3\,\mathrm{dB}$.

Table 7.3: Modulator performance with time constant (τ) tuning

Corner	Without tuning		With tuning	
	Peak SQNR (dB)	Dynamic range (dB)	Peak SQNR (dB)	Dynamic range (dB)
Ideal	127.7	126.3	127.7	126.3
τ max	114.0	119.3	125.7	126.0
τ min	Modulator unstable		128.9	124.5

64
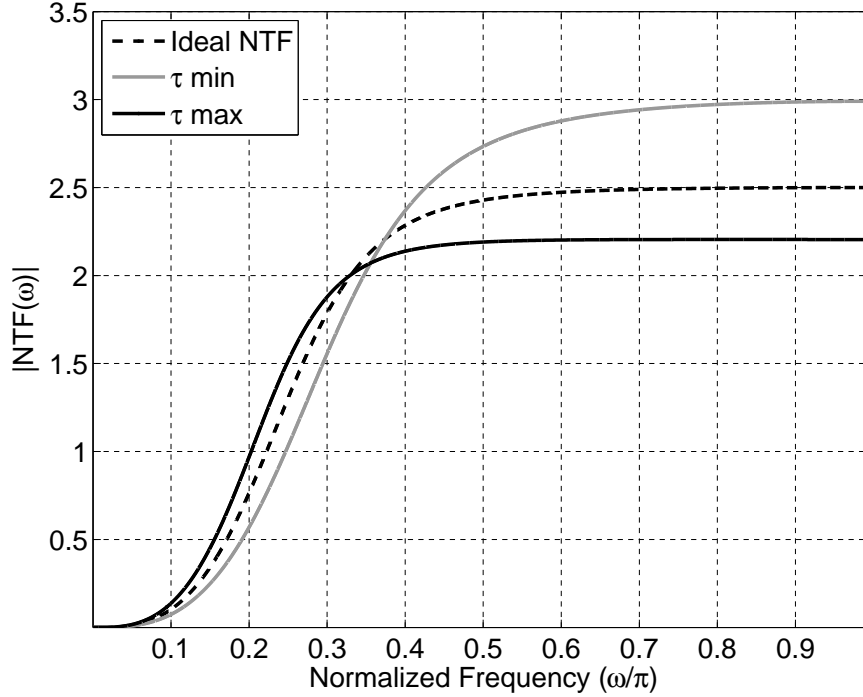
Figure 7.16: NTF variation for $\pm\,10\,\%$ variation in time constants.

7.8   Summary

A third order loop filter which has an NTF out-of-band gain of 2.5 has been designed with active RC integrators. The loop filter operates at a 1.8 V supply and has a differential output swing of $\pm\,1.5$ V. All op-amps have been designed with feedforward architectures except the summing op-amp which is a two stage miller compensated op-amp. The first op-amp has been designed to produce low noise by increasing the bias current and gate area. The current consumed by various blocks of the loop filter is given in Table 7.4.

Table 7.4: Current consumption of the loop filter

Block	Current (μA)
First integrator	305
Second integrator	11.5
Third integrator	11.5
Summing amplifier	20.5
Total	348.5

CHAPTER 8

Four bit flash ADC

Sampling and quantization of the signal from the loop filter is done with a flash ADC. The digital output of the $\Delta\Sigma$ modulator is obtained from this ADC. The primary advantage of employing multibit quantizer in $\Delta\Sigma$ modulators is that the total quantization noise power reduces by $6\,\mathrm{dB}$ for every additional bit [13]. It also increases the maximum stable amplitude of the converter. A flash ADC has the least latency but has the trade off of exponentially increased area and complexity with the increase in number of levels to be resolved. A four bit flash ADC is used in the modulator.

8.1 Architecture of the flash array

An 'N' bit flash ADC requires $2^{\mathrm{N}} - 1$ comparators and $2^{\mathrm{N}} - 1$ reference voltages. The reference voltages for the comparators are generated a using resistor divider. The block diagram of the four bit flash ADC implemented in differential fashion is shown in Figure 8.1. A comparator output gives a logic '1' output if its differential input voltage is greater than its differential reference voltage. This four bit flash ADC gives a fifteen level thermometer code at its output which consists of consecutive logic '0' followed by consecutive logic '1'. This thermometer code is converted to binary signal before it is taken out of the chip.

8.1.1 Resistive ladder

The resistive ladder is a string of sixteen $100\,\mathrm{k}\Omega$ resistors that generates the differential reference voltages (V_{refx}, V_{refy}) for each comparator. Large resistors are used in the lad-
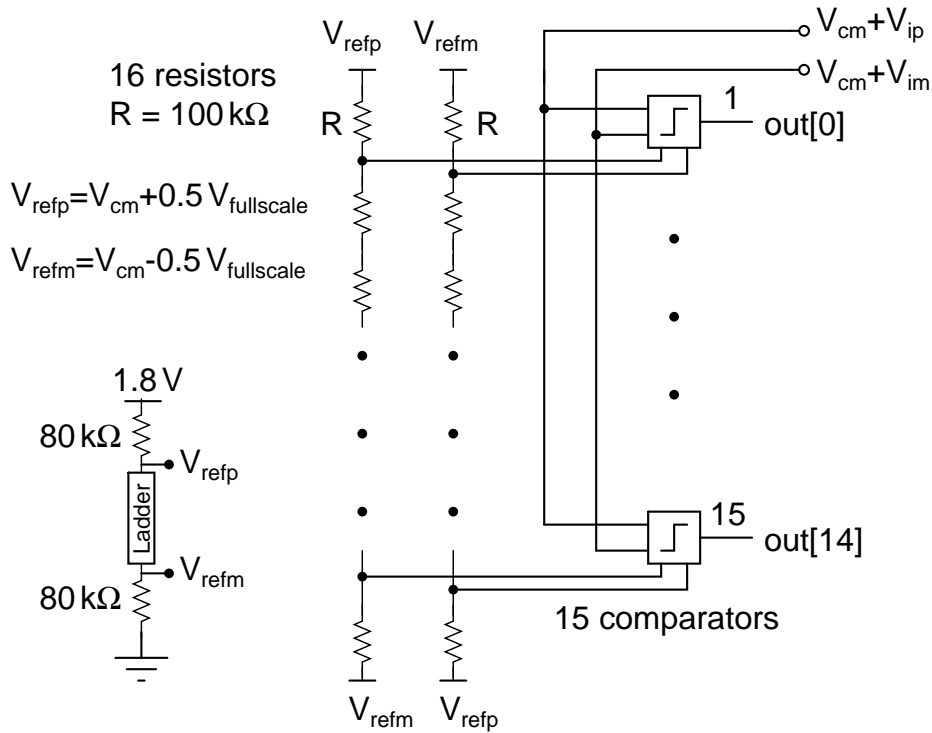
Figure 8.1: Block diagram of the 4 bit flash ADC.

der to minimize the power consumption. The differential fullscale voltage of the ADC is ± 1.5 V and the common mode voltage is $V_{cm} = 0.9$ V. Hence the reference voltages for the ladder are $V_{refp} = 1.65$ V and $V_{refm} = 0.15$ V. These references are generated from the supply voltage of 1.8 V using a resistive divider as shown in Figure 8.1. The voltage drop across a resistor in the ladder is 93.75 mV. Hence the LSB voltage (differential) of the flash ADC is 187.5 mV. The center node of the two resistive ladders are at the common mode voltage $V_{cm} = 0.9$ V. Small amounts of transient currents are drawn from the reference ladder during the comparator operation. Hence each reference voltage node is bypassed to ground with a 1 pF capacitor to keep the reference node voltages stable.

8.1.2 Comparator

Each comparator produces a digital output that indicates if the differential input ($V_{ip} - V_{im}$) is greater than its differential reference ($V_{refx} - V_{refy}$). The block diagram of the comparator is shown in Figure 8.2.
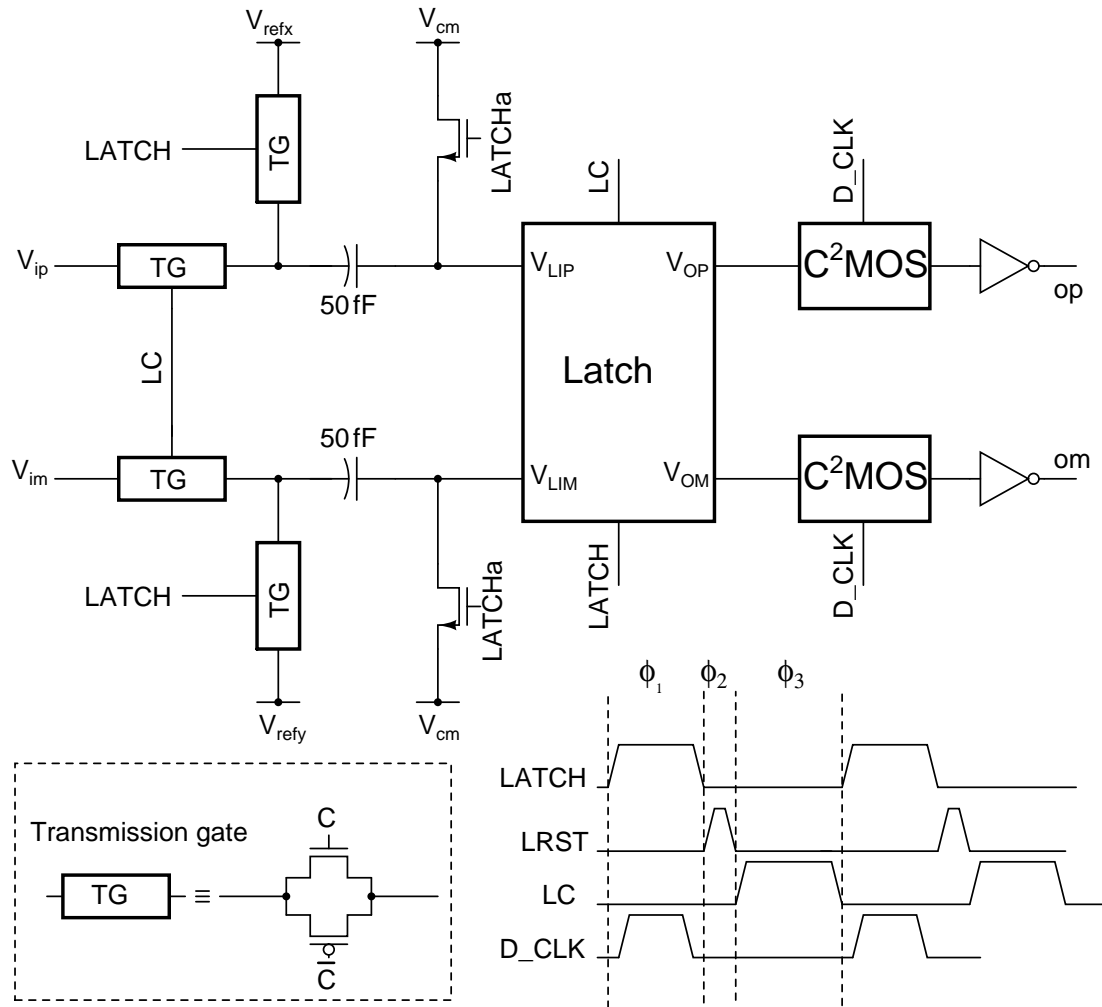
Figure 8.2: Block diagram of the comparator.

It consists of a regenerating latch and two 50 fF capacitors to store the reference voltages. There are three phases of operation ϕ_1, ϕ_2 and ϕ_3 whose timing is shown in Figure 8.2. During the phase ϕ_1 the reference voltages are stored in the capacitors. The falling edge of the signal LATCHa is advanced with respect to that of the signal LATCH. This is to prevent the reference voltage ($V_{refx,y}$) dependent charge injection on the capacitors. During the phase ϕ_2 these capacitors are floating and hence their charge is preserved.

During the phase ϕ_3 the inputs are connected to the bottom plates of these capacitors and its top plates are connected to the regenerating latch. The capacitor acts like a battery and hence the differential voltage at the input of the latch is the difference between the input ($V_{ip} - V_{im}$) and the reference voltage ($V_{refx} - V_{refy}$). The latch regenerates during the phase ϕ_1 and hence the sampling instance of the ADC is the falling edge of the

68

signal LC (ϕ_3). The logical decision from the latch, after regeneration, is sampled using a C^2MOS inverter [27] with D_CLK. The rising edge of D_CLK occurs 230 ps after the rising edge of the signal LATCH. All switches in the comparator are made with minimum sized transistors.

8.1.3 Latch

The latch used for each comparator is a cross coupled inverter pair which is enabled or disabled by the control signal LATCH. The circuit diagram of the latch is shown in Figure 8.3.
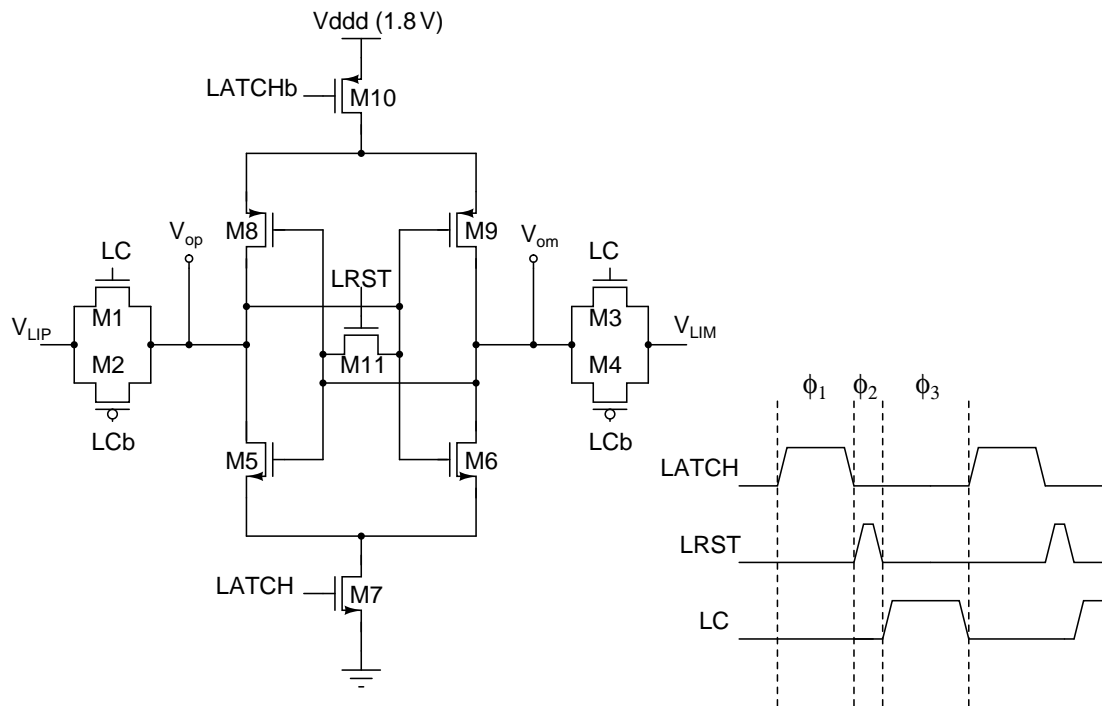
Figure 8.3: Circuit diagram of the latch.

During the track phase, ϕ_3, the cross coupled inverters are disabled and the input signal is charged on the parasitic capacitors at nodes V_{op} and V_{om}. The cross coupled inverters are activated during the regeneration phase ϕ_1. During the reset phase ϕ_2 the latch is reset to remove its memory of its past input and hence the hysteresis is eliminated.

At the beginning of the regenerating phase ϕ_1 if the input voltages of the cross coupled

inverter pairs are close to each other, the latch can be linearized with the equivalent circuit shown in Figure 8.4. Let ΔV be the difference between V_x and V_y and ΔV_0 be
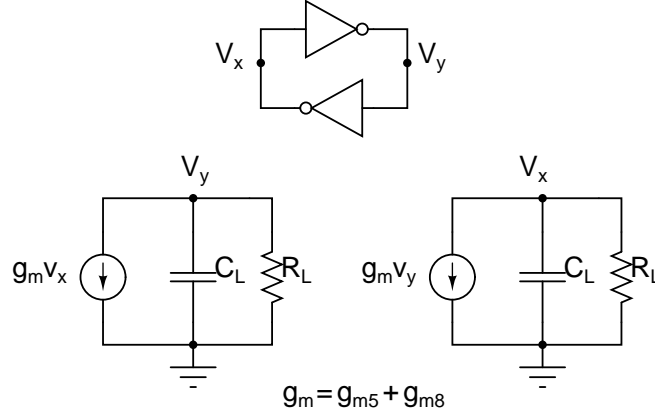
Figure 8.4: Equivalent circuit of the latch.

the value at the beginning of the regeneration phase. The differential equation for this circuit is

$$\frac{d\Delta V}{dt} = (\frac{g_m R_L - 1}{R_L C_L})\Delta V \tag{8.1}$$

For the cross coupled inverter to regenerate, $g_m R_L > 1$. The solution of this differential equation is

$$\Delta V(t) = \Delta V_0 \, e^{t/\tau} \tag{8.2}$$

where $\tau = \dfrac{R_L C_L}{g_m R_L - 1} \approx \dfrac{C_L}{g_m}$. The time required to regenerate to a logic level V_{logic} is given by $T_{latch} = \tau \ln(\dfrac{V_{logic}}{\Delta V_0})$. If ΔV_0 is small enough the latch does not regenerate to the logic levels at the end of the phase ϕ_1. Hence at the output of C^{2}MOS inverters, incorrect logic decision is obtained. This phenomenon is called *metastability* and is avoided by designing the latch with small time constant τ.

8.2 Element mismatches in the ADC

Random mismatch among the unit elements in the flash array can degrade the performance of the modulator as described in Section 6.3.4. The main sources of the mismatch are the variation in the threshold voltages of the transistors in the latches and the ladder

resistors. The maximum tolerable mismatch error is found through macromodel simulations and the elements are sized appropriately so that the mismatch error is within the tolerable limit.

8.2.1 Mismatch in latch transistors

Random variation in threshold voltages of the transistors are modelled as an additive offset at the input of an ideal latch. The offset of a latch in terms of its threshold voltage variation is calculated as follows:

Let g_{mp} and g_{mn} respectively denote the transconductance of the PMOS and the NMOS transistors that form the cross coupled inverter pair. Let ΔV_{tp} and ΔV_{tn} denote the variation in the threshold voltage of the PMOS and NMOS transistors respectively. The output offset current of the cross coupled inverter pair is given as

$$I_{off} = g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn} \tag{8.3}$$

Hence the equivalent input referred offset voltage is written as

$$V_{off} = \frac{g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn}}{g_{mp} + g_{mn}} \tag{8.4}$$

If $\sigma_{V_{tpn}}$ and $\sigma_{V_{tn}}$ respectively are the standard deviation of the variation in threshold voltages of the PMOS and the NMOS transistors, the standard deviation of the offset voltage can be expressed as

$$\sigma_{off} = \frac{\sqrt{g_{mp}^2\sigma_{V_{tp}}^2 + g_{mn}^2\sigma_{V_{tn}}^2}}{g_{mp} + g_{mn}} \tag{8.5}$$

The constraint on the maximum allowable σ_{off} is found through macromodel simulations. The $\Delta\Sigma$ modulator is simulated by adding a set of randomly generated offset voltages (with a given standard deviation σ_{off}) at the input of each latch. Thousand

such trials are performed for a given σ_{off} and the peak SNR is evaluated for each trial. The scatter plot of the SNR for different σ_{off} is given in Figure 8.5.
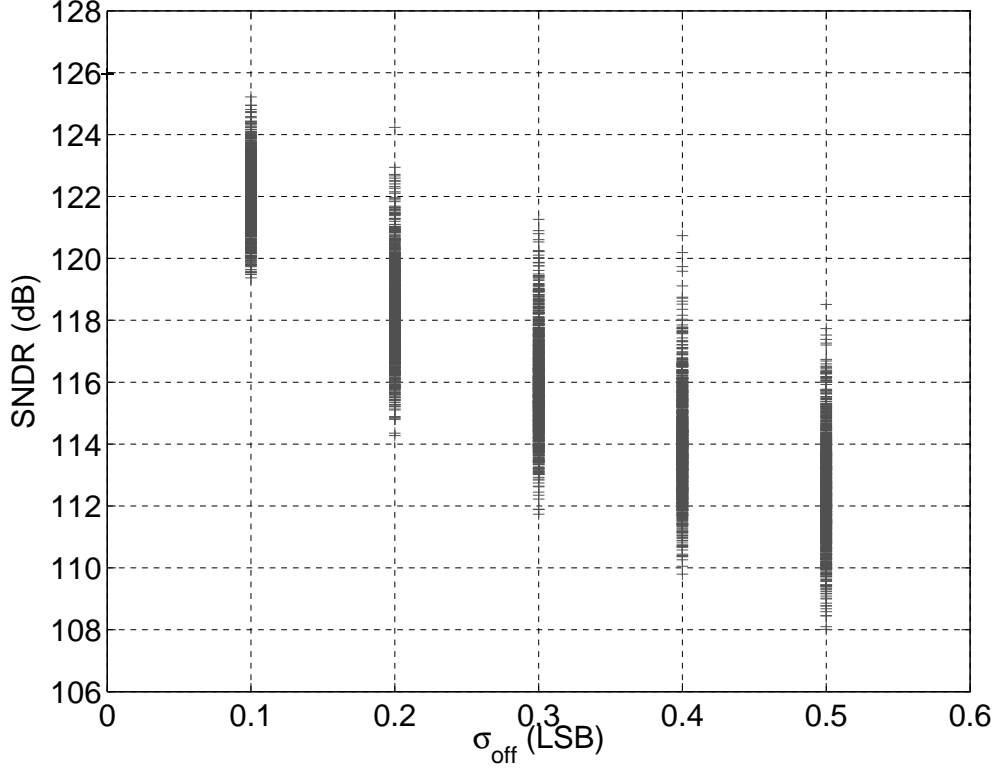
Figure 8.5: Scatter plot of the SNR for 1000 simulations with different latch offsets.

To meet the specification for the modulator, $\mathrm{SNR_{mean}} - 3\sigma_{\mathrm{SNR}}$ is made to be greater than 108 dB. Using Figure 8.5 it is decided to constrain the latch offset (σ_{off}) to be lesser than 0.4 LSB (75 mV). Sizes of the transistors M5, M6, M7, M8 are chosen as 0.5 μm/0.18 μm. The $\sigma_{V_{tp}}$ and $\sigma_{V_{tp}}$ are found with the following relation

$$\sigma_{V_{tp}} = \frac{A_{V_{tp}}}{\sqrt{WL}} + Cx_p \quad \sigma_{V_{tn}} = \frac{A_{V_{tn}}}{\sqrt{WL}} + Cx_n \tag{8.6}$$

Here $A_{V_{tp}} = 4.7 \,\mathrm{mV}/\mu\mathrm{m}$, $A_{V_{tn}} = 4.79 \,\mathrm{mV}/\mu\mathrm{m}$, $Cx_p = 0.1894 \,\mathrm{mV}$, $Cx_n = 0.5328 \,\mathrm{mV}$. The transconductance of the PMOS and NMOS transistors for this sizing are $g_{mp} = 81.5 \,\mu\mathrm{S}$ and $g_{mn} = 167 \,\mu\mathrm{S}$. Using (8.5) the offset voltage is calculated as $\sigma_{V_{off}} = 12.23 \,\mathrm{mV}$. The latch is hence designed to have its σ_{off} much smaller than 0.4 LSB (75 mV).

8.2.2 Mismatch between ladder resistors

Random mismatch in the ladder resistors causes the reference voltages to deviate from its ideal value. Let $\sigma_{\frac{\Delta R}{R}}$ denote the standard deviation of $\frac{\Delta R}{R}$ where R is the ladder resistor ($100\,\mathrm{k\Omega}$) and ΔR is the deviation in the fabricated value. The maximum tolerable $\sigma_{\frac{\Delta R}{R}}$ is found through macromodel simulations. Sixteen randomly chosen resistors of nominal value $100\,\mathrm{k\Omega}$ and standard deviation $\sigma_{\frac{\Delta R}{R}}$ are used to generate the reference voltages for the modulator. Thousand simulations of the modulator are performed for a given $\sigma_{\frac{\Delta R}{R}}$ and the peak SNR is evaluated from the output spectrum. The scatter plot of the thousand SNR values for different values of $\sigma_{\frac{\Delta R}{R}}$ is shown in Figure 8.6.
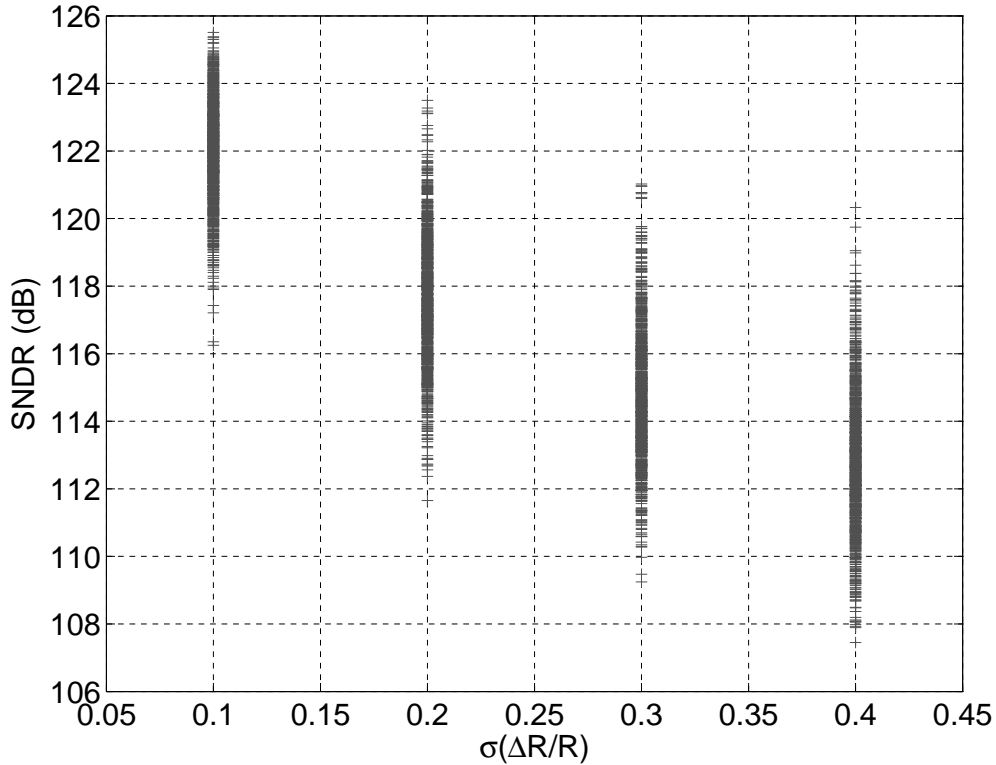
Figure 8.6: Scatter plot of the SNR for 1000 simulations with mismatched ladder resistors.

To meet the specifications for the modulator, $\mathrm{SNR_{mean}} - 3\sigma_{\mathrm{SNR}}$ is made to be greater than $108\,\mathrm{dB}$ and hence the constraint on the resistors is chosen as $\sigma_{\frac{\Delta R}{R}} < 0.2$. The matching, $\sigma_{\frac{\Delta R}{R}}$, is inversely proportional to the square root of the area of the resistor. For the high resistivity polysilicon resistor in this process, $\sigma_{\frac{\Delta R}{R}} = 0.001$ for a resistor

that has its dimension of $1\mu m \times 90\mu m$. The dimensions of the resistors used in the ladder is $0.18\mu m \times 13.5\mu m$. For the chosen dimensions, the resistors are matched to 0.006 which is much smaller than the maximum tolerable $\sigma_{\frac{\Delta R}{R}}$.

8.3 Clock generation for the flash ADC

The operation of the flash ADC requires a pair of non-overlapping clocks, LC and LATCH as shown in Figure 8.2. The falling edge of LC is the ADC's sampling instant and the latch starts regenerating at the rising edge of LATCH. Hence they must be non-overlapping for proper operation of the flash ADC. The clocks for the flash ADC are generated using a non overlapping NAND clock generator as shown in Figure 8.7.
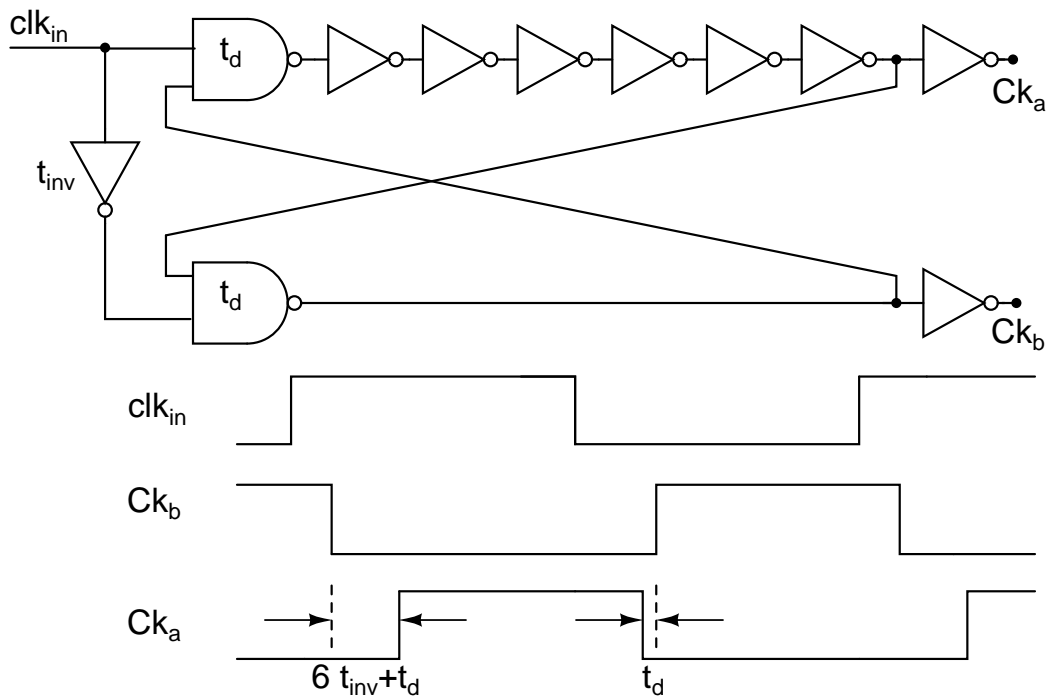
Figure 8.7: Non-overlapping clock generator.

The clock Ck_b is used as the LATCH signal and a slightly delayed version of Ck_a is used as the LC signal. All the other clocks are generated from Ck_a, Ck_b and their delayed versions using appropriate combinational logic. According to Figure 8.2, it is required for the D_CLK to go low before the LRST pulse goes high to prevent the

C^2MOS in sampling the wrong value from the latch. The pulse width of the LRST is wide enough to reset the comparator outputs to erase the memory of the previous cycle. The LRST and the LATCH are never made high at the same time to avoid static power consumption in the comparator. The comparator consumes a small transient current from the supply only during the regeneration phase.

CHAPTER 9

Feedback DAC

The DAC feeds back an analog signal corresponding to the digital output of the flash ADC. An 'N' bit flash ADC has $2^N - 1$ thermometric code as output. A thermometer DAC has $2^N - 1$ unit elements which are controlled by the thermometer output of the ADC. The output of the DAC is the sum of outputs from these thermometer elements. A thermometer DAC is preferred over a binary weighted DAC because it suffers from lesser differential nonlinearity (DNL) compared to the latter. As explained in Section 6.3.5, nonidealities of the DAC have direct impact on the performance of the modulator resulting in increased noise floor and spurious tones.

9.1 The DAC unit element

The four bit flash ADC used in this modulator has fifteen thermometer bits (out[14:0]) as its output each of which controls one element in the thermometer DAC. A DAC unit element turns ON in one direction (source current) when the control is logic 1 and turns ON in the other direction (sink current) when the control is logic 0. Outputs of all unit elements are summed at the virtual ground nodes $idacp$ and $idacm$ of the loop filter (Refer Figure 7.4). The nodes $idacp$ and $idacm$ are at the common mode voltage, $V_{cm} = V_{dd}/2 = 0.9\,\text{V}$.

The DAC unit element can be a resistor driven by a reference voltage or a current source. A resistive DAC is preferred over a DAC implemented with MOSFET due to the lesser noise from the former. This is explained with the help of Figure 9.1. Let $S_{IM}(f)$ and $S_{IR}(f)$ denote the power spectral density of the noise current in the MOS transistor
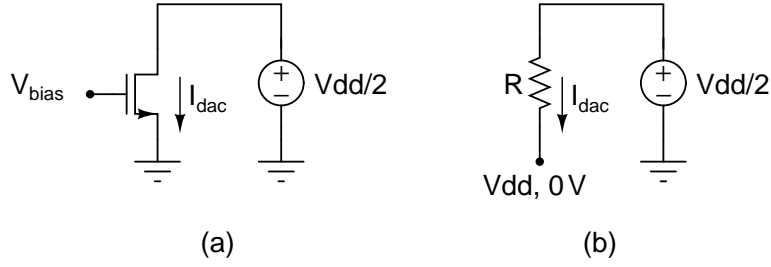
Figure 9.1: Implementation of a DAC unit element: a) A current source constructed with MOSFET, b) A current source using a resistor.

and the resistor respectively. Let V_{dsat} denote the overdrive of the MOSFET. The noise power spectral densities of these two cases is written as

$$S_{IM}(f) = \frac{8}{3}kT\frac{2I_{dac}}{V_{dsat}} + S_{IF}(f) \tag{9.1}$$

$$S_{IR}(f) = 4kT\frac{I_{dac}}{V_{dd}/2} = 4kT\frac{2I_{dac}}{V_{dd}} \tag{9.2}$$

The additional term $S_{IF}(f)$ corresponds to that of the flicker noise current in a MOS transistor. The overdrive (V_{dsat}) of a MOS transistor is usually much lesser than the supply voltage (V_{dd}) in a technology. Hence it can be inferred that for a given DAC current I_{dac}, the current noise spectral density of a resistor is much lower than that of the MOS transistor. Hence a resistive DAC is chosen in this design. Figure 9.2 shows the schematic of the differential DAC.

x : 16(0.24μ/0.18μ)

R_{dac} : 76.8 kΩ
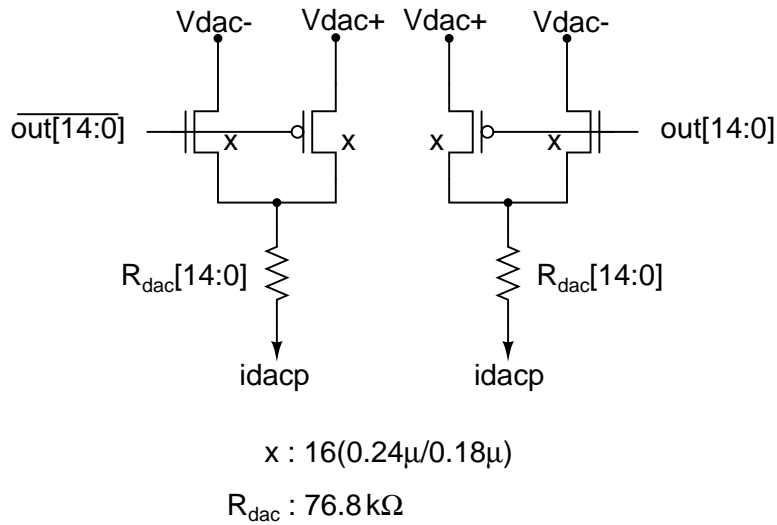
Figure 9.2: Schematic of the resistive DAC.

The reference voltages for the DAC, $Vdac+$ and $Vdac-$, are 1.8 V and 0 V respectively. The magnitude of the DAC unit cell current is $\dfrac{0.9\,\text{V}}{76.8\,\text{k}\Omega} = 11.71875\,\mu\text{A}$. Hence the total DAC current for 15 thermometer elements is 175.78125 μA. The thermometer control signal from the ADC, out[14:0], controls if a DAC unit element sources or sinks current into the loop filter.

The reference voltages for the DAC, 1.8 V and 0 V, are obtained external to the chip. The reference 1.8 V is bypassed to ground with a 400 pF MOS capacitor internal to the chip. The series bondwire inductance (few nanohenry) due to the packaging of the chip and the bypass capacitor forms a high quality resonant circuit whose step response can ring for a long time. To reduce the quality factor of the circuit a very small resistor $R_{damp} = 15\,\Omega$ is connected in series as shown in Figure 9.3. Assuming a bondwire inductance of $L_{bond} = 5\,nH$ the quality factor of the circuit at resonant frequency is $Q = 0.23$ which is sufficiently lesser than unity to prevent ringing.

$$R_{damp} - 15\,\Omega$$
$$C_{byp} - 400\,\text{pF}$$
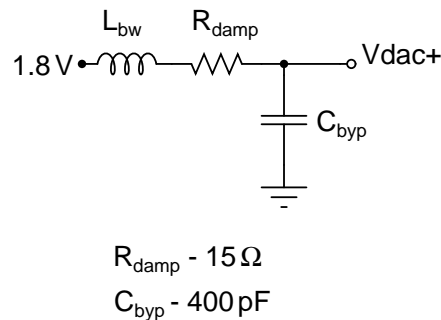
Figure 9.3: Generation of the references for the DAC.

9.2 Accuracy of DAC elements

For a resolution of 18 bits with a fullscale voltage of 3 V, the LSB is $3/2^{18} = 11.44\,\mu\text{V}$. The DAC elements should be accurately matched enough such that the mismatch errors is much smaller than this LSB voltage. As discussed in 6.3.5 mismatch among the unit elements causes nonlinearity in the DAC characteristics which results in an increased in-band noise floor and poor SNDR. It is found through simulations that the

matching requirement for the DAC resistors is $1 \times 10^{-5}\%$ to attain SNR in excess of 108 dB without spurious tones in the spectrum. Such highly matched resistors are impractical to realize in standard CMOS processes. To overcome this, a dynamic element matching (DEM) algorithm is used.

9.3   Dynamic element matching

Dynamic element matching (DEM) is a technique that dynamically rearranges the interconnections of the mismatched elements in each cycle so that the time average of each unit elements are almost equal. Depending upon the algorithm used for the rearrangement, the mismatch errors can be either converted to white noise (randomization [28]) or be shaped out of the signal bandwidth (data weighted averaging [23]). In this design the technique data weighted averaging is employed.

9.3.1   Data weighted averaging

The data weighted averaging (DWA) technique cycles through all elements quickly based on the the input thermometer code. Using elements at the maximum possible rate ensures that the mismatch errors will quickly sum up to zero, moving distortion to high frequencies [23]. The DWA algorithm can be easily understood with the help of the diagram shown in Figure 9.4. The fifteen cells in the column represents the DAC unit elements. Shaded box indicates that the cell is being used in the cycle and the blank box indicate that the cell is not being used. In the first cycle for a code of value 'k' first 'k' elements of the DAC are used. In the next cycle if the code is 'm' then 'k+1' to 'k+m' elements are used. Once all elements are used up, elements are reused again in a cyclic fashion. The element averaging is controlled by the input signal and hence the name data weighted averaging. The DWA technique provides first order shaping of the mismatch errors [23].
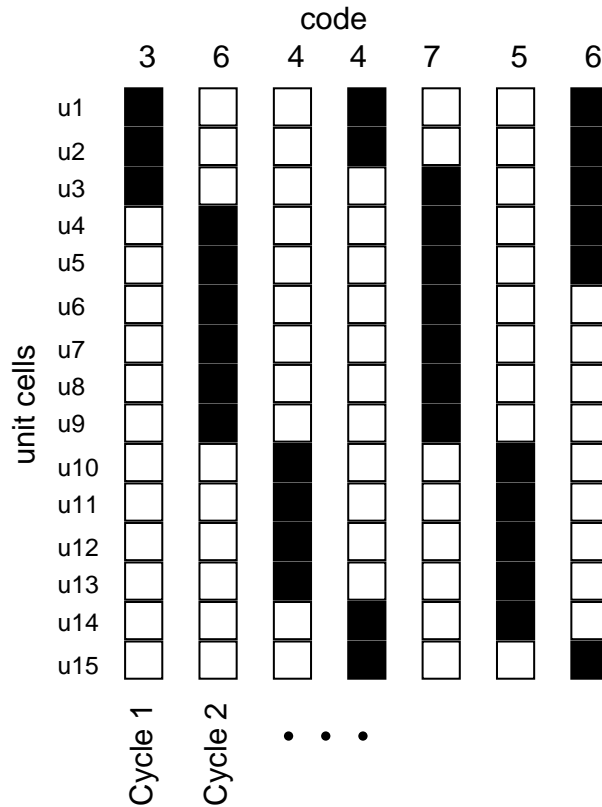
Figure 9.4: Illustration of the DWA.

For a small DC input signal, the DWA algorithm tends to reuse the mismatched elements periodically. If the number of unit elements in the DAC is M, then the output spectrum of the modulator contains spurious tones at harmonics of f_s/M. Hence the DWA algorithm tends to produce tones at the subharmonics of the sampling frequency. In this design these tones fall outside the signal band because the OSR (64) is greater than the number of elements (15) in the DAC.

9.3.2   Implementation of the DWA

Instead of switching the unit elements every cycle, the locations of logic '1' in the thermometer code is switched in every cycle with the help of a barrel shifter. The shifting control to the barrel shifter is based on the previous input data/codes. A thermometer to binary converter converts the input thermometer code from the flash ADC to a four bit binary signal $ADCout$. An accumulator accumulates this digital data $ADCout$ in ev-

ery cycle and provides the shifting control to the barrel shifter. The shifted thermometer code is retimed with the clock DAC_CLK which is delayed 4.5 ns with respect to the D_CLK. This resampled data is buffered and then controls the switches in the unit elements the DAC. The block diagram of the implementation of DWA is shown in Figure 9.5.
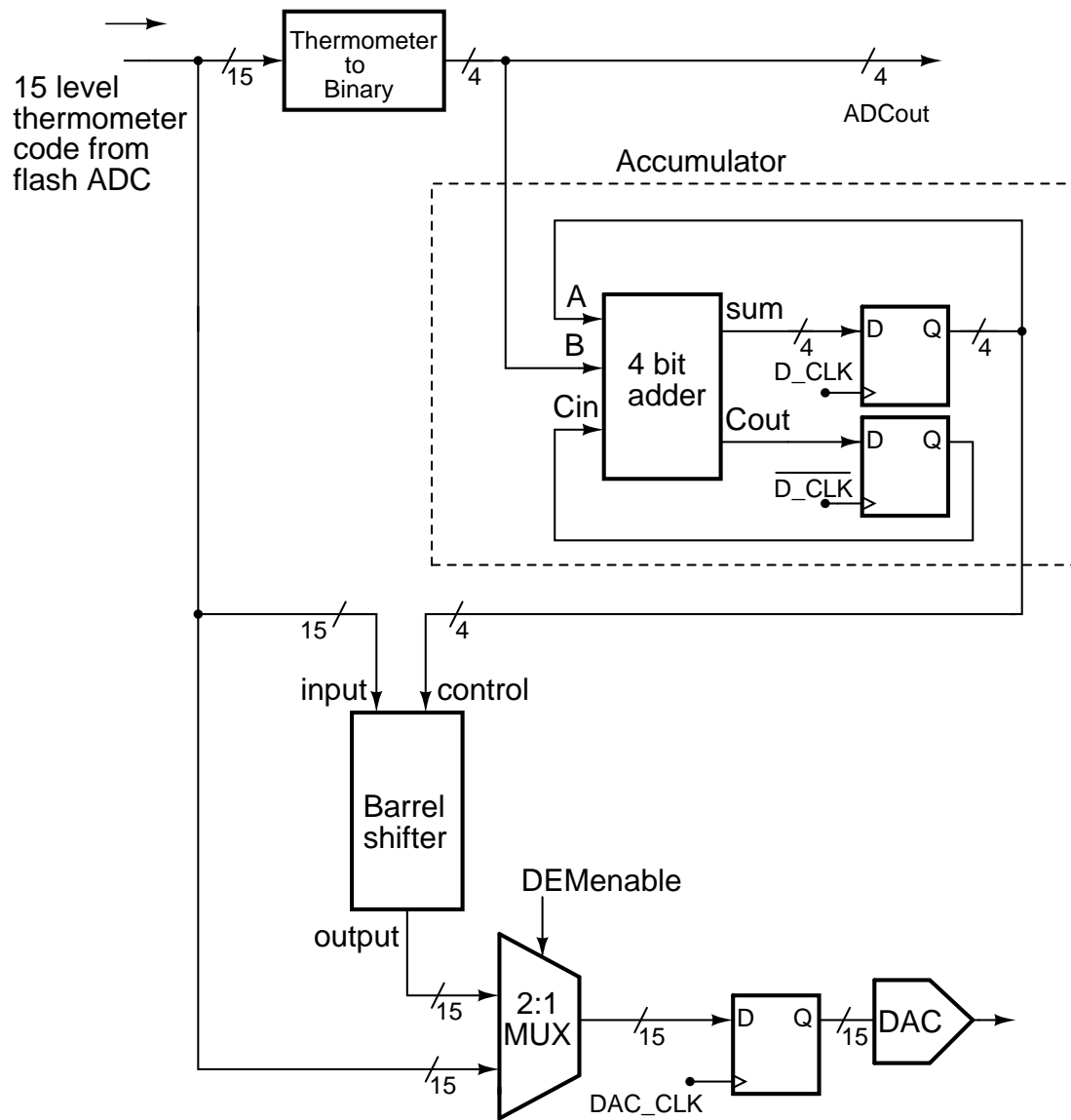
Figure 9.5: Block level implementation of the DWA.

A behavioral verilog module of the DEM logic is written and is then synthesized with digital standard cells using automated CAD tools. A provision to enable/bypass the DWA is made with the control signal, $DEMenable$, which is obtained external to the chip.

9.4 DAC resistor sizing

The minimum required matching with DWA algorithm is found through macromodel simulations of the modulator having mismatched DAC resistors. Thousand simulations are performed by generating thousand sets of fifteen resistors having a standard deviation of $\sigma_{\frac{\Delta R}{R}}$. The spectrum is obtained for each case and the maximum SNR is evaluated. The scatter plot of the SNR for different $\sigma_{\frac{\Delta R}{R}}$ is shown in Figure 9.6.
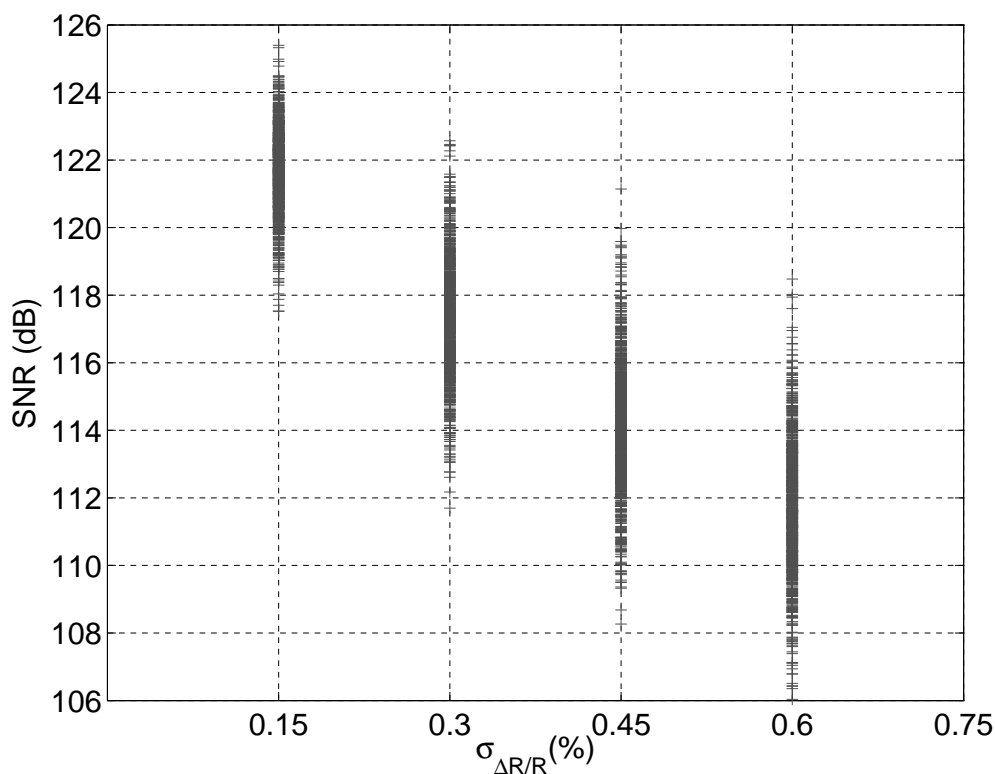
Figure 9.6: Scatter plot of the SNR for various $\sigma_{\frac{\Delta R}{R}}$.

On observation from the scatter plot, it is decided to constrain the matching of resistors to 0.3 %. For the high resistivity polysilicon resistor in this process, $\sigma_{\frac{\Delta R}{R}}$=0.1 % for a resistor with dimensions 1μm$\times 90\mu$m. The dimensions of the $76.8\,$kΩ resistor used in the DAC is 2μm$\times 145\mu$m. This corresponds to a matching of 0.055 %.

The spectrum from the output of the modulator for 0.3 % mismatched elements is shown in Figure 9.7. The ideal SNR of the modulator is $126\,$dB. The SNR of the modulator when the DWA is enabled is $118\,$dB.
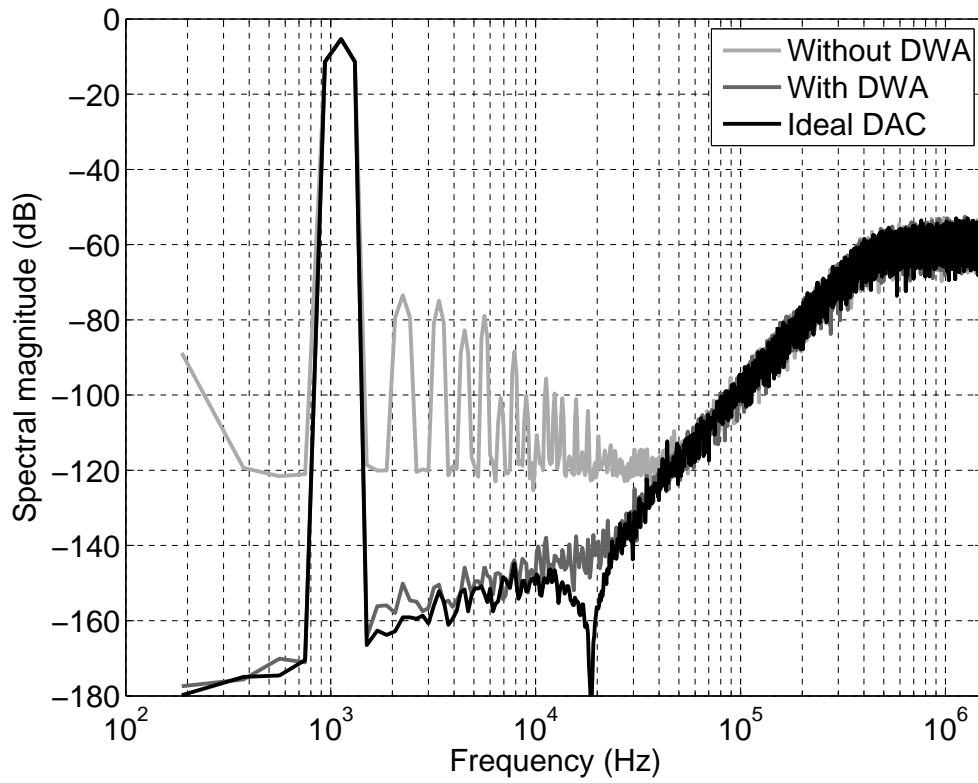
Figure 9.7: Spectrum of the modulator output with and without DWA for 0.3 % matched DAC elements.

CHAPTER 10

Layout and top level simulation results

10.1   Layout

The $\Delta\Sigma$ modulator is fabricated as a chip in $0.18\,\mu$m technology with $1.8\,$V supply. Figure 10.1 shows the layout, highlighting various blocks of the modulator. The active area of the modulator is $0.89\,\text{mm}^2$. The total area of the die is $1.5\,$mm x $1.5\,$mm.
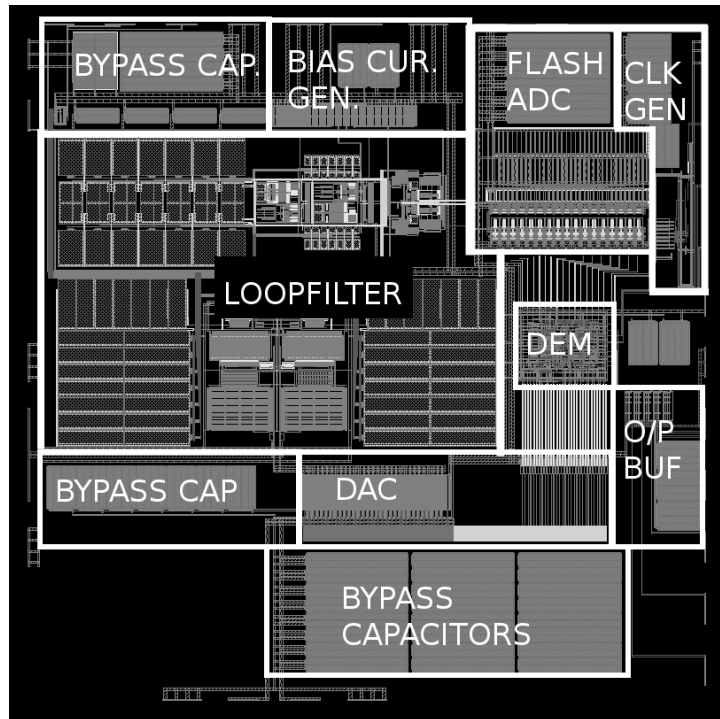
Figure 10.1: Layout of the $\Delta\Sigma$ modulator.

10.2   Simulation results

In order to evaluate the performance of the modulator transient simulations are performed, with various blocks of the modulator in the schematic view as well as the

capacitance extracted view obtained after layout. Transient simulations of $\Delta\Sigma$ modulator are in general time intensive. Hence various combinations of tests as shown in Table 10.1 are done to evaluate the performance of the modulator. The signal chosen is a sinusoid at 4.5 kHz with an amplitude of -3.5 dBFS. It is found through various test cases that worst corners for the modulator performance are slow NMOS, slow PMOS transistor corner at temperature T=0 °C and Fast NMOS, Fast PMOS transistor corner at temperature T=70 °C. Table 10.2 gives the performance of the modulator in the presence of RC variation and the tuning bits bwc[2:0] appropriately set.

Table 10.1: Simulation results: SNDR for various test cases

Loop Filter	Flash ADC	Clock Generator	DAC	Transistor Corner	Temperature (°C)	SNDR (dB)
sch	sch	ideal	sch	TT	27	121.7
				SS	0	119.5
				FF	70	121.0
sch	ext	ideal	sch	TT	27	119.6
				SS	0	117.5
				FF	70	121.3
sch	ext	sch	sch	TT	27	122.0
				SS	0	121.2
				FF	70	121.8
sch	sch	sch	sch	TT	27	121.7
ext	ext	sch	sch	TT	27	121.0
ext	sch	sch	ext	TT	27	116.0

sch - Schematic view
ext - Capacitance extracted view
ideal - Ideal macro model

Table 10.2: Simulation results: SNDR for RC corners with tuning

Loop Filter	Flash ADC	Clock Generator	DAC	Transistor Corner	RC Corner	Temp (°C)	SNDR (dB)
sch	ext	sch	sch	SS	Rmin Cmin	0	115.9
				FF	Rmax Cmax	70	123.5
				TT	Rtyp Ctyp	27	119.0
ext	ideal	sch	sch	SS	Rmin Cmin	0	114.9
				FF	Rmax Cmax	70	119.0
				TT	Rtyp Ctyp	27	122.0

The spectrum of the modulator output corresponding to the penultimate row in Table 10.1 is shown in Figure 10.2.
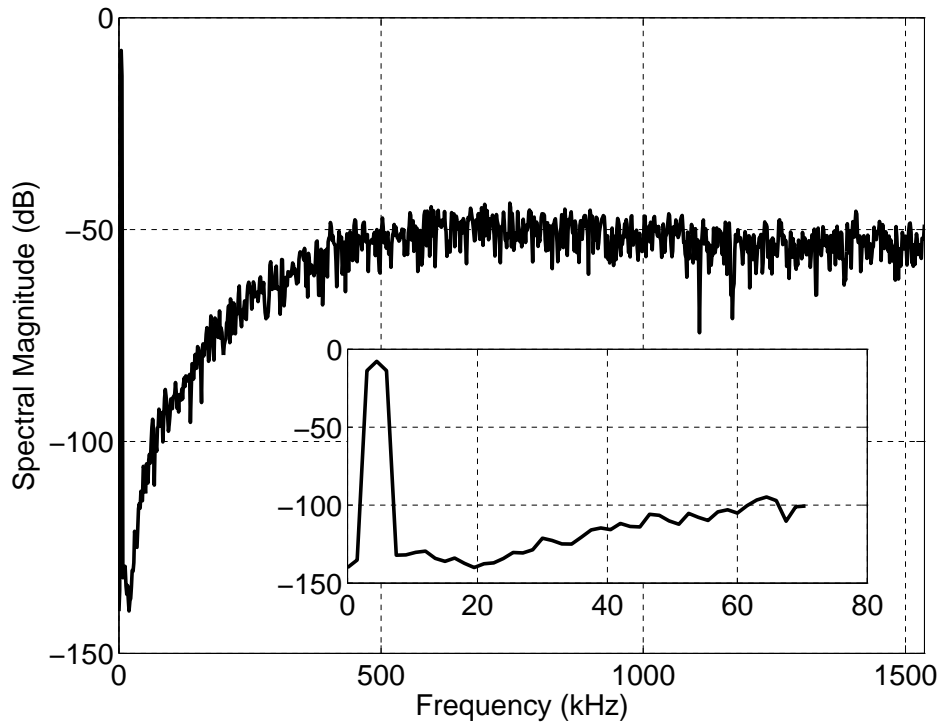
Figure 10.2: Simulated spectrum of the $\Delta\Sigma$ modulator for a tone input at 4.5 kHz.

10.3 Power consumption

The total power consumption of various blocks is tabulated in Table 10.3. The most power hungry blocks in the design are the first integrator which consumes 56 % of the total power and the DAC which consumes 32.5 % of the total power of the modulator. The large power consumption in these blocks are attributed to the very small noise contribution from these blocks to attain the 108 dB performance for the modulator.

Table 10.3: Power consumption of the $\Delta\Sigma$ modulator blocks

Component	Current (μA)
Loop Filter	348.5
Flash ADC	4.0
Clock generator	11.0
DEM Logic	12.2
DAC	175.8
Total	541.5

Table 10.4 gives the summary of the $\Delta\Sigma$ modulator design.

Table 10.4: Summary of the $\Delta\Sigma$ modulator design

Specification	Value
Sampling frequency	3.072 MHz
Bandwidth	20 Hz - 24 kHz
Quantizer range	3 Vpp,differential
Peak SNR	108 dB
Power	975 μW(1.8 V)
Active area	0.89 mm^2
Supply voltage	1.8 V
Technology	0.18 μm CMOS

CHAPTER 11

Measurement results from the $\Delta\Sigma$ modulator chip

11.1   Test setup

Figure 11.1 shows the block diagram of the test setup for the $\Delta\Sigma$ modulator chip. The
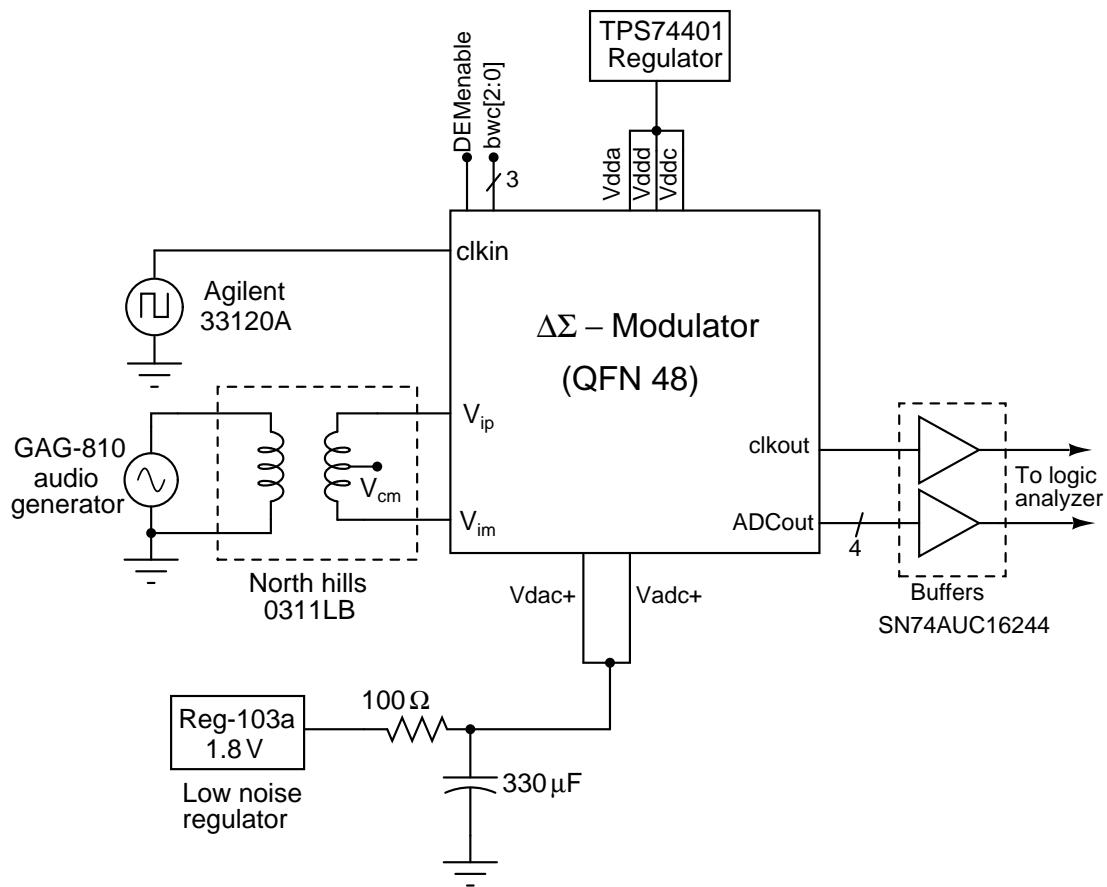
Figure 11.1: Test setup of the $\Delta\Sigma$ modulator.

input sinusoidal signal generated using an audio precision signal source is converted from single ended to differential using a balun transformer. The Agilent 33120A clock source generates the $3.072\,\mathrm{MHz}$ clock for the chip. The reference voltages for the DAC (Vdac+) and flash ADC (Vadc+) are generated using a low noise voltage regulator Reg-103a. The reference voltage is low pass filtered with a first order low pass filter

whose cutoff frequency is 5 Hz. The output integrated noise of the reference voltage after filtering is $0.6\,\mu$V in the bandwidth 20 Hz - 24 kHz. The output signal is captured using a logic analyzer. Figure 11.2 shows the snapshot of the four layer PCB designed for the test setup.
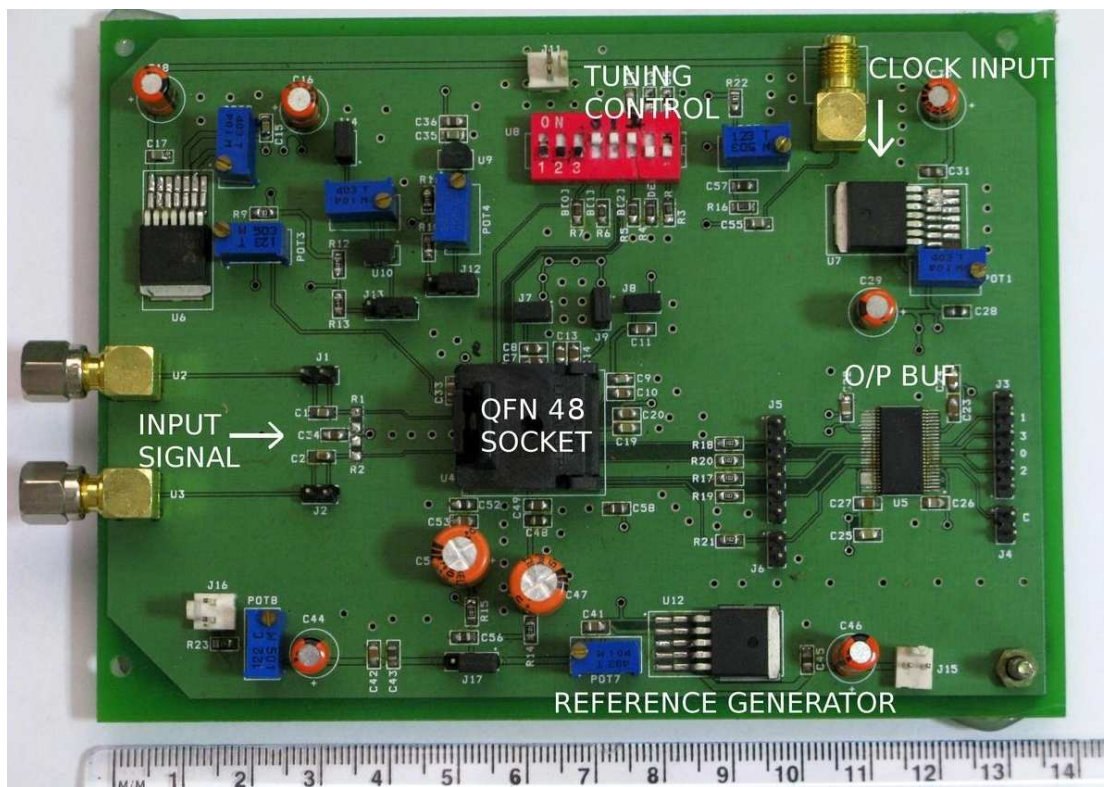
Figure 11.2: Picture of the PCB for testing the $\Delta\Sigma$ modulator.

11.2 Measurement results

Two types of measurements are performed for testing the modulator viz. without signal (Idle channel performance) and with a sinusoidal signal.

11.2.1 Idle channel performance

When no input signal is given to the input of the modulator, the output of the modulator contains only the shaped noise. On integrating the noise power spectral density in the in-

band (20 Hz - 24 kHz) the integrated in-band noise power of the modulator is obtained. The differential input signal is shorted to the common mode voltage and the output spectrum is obtained. Figure 11.3 shows the idle channel performance of the modulator. It is found that the integrated in-band noise when the DEM is disabled is $6.5\,\mu V_{rms}$
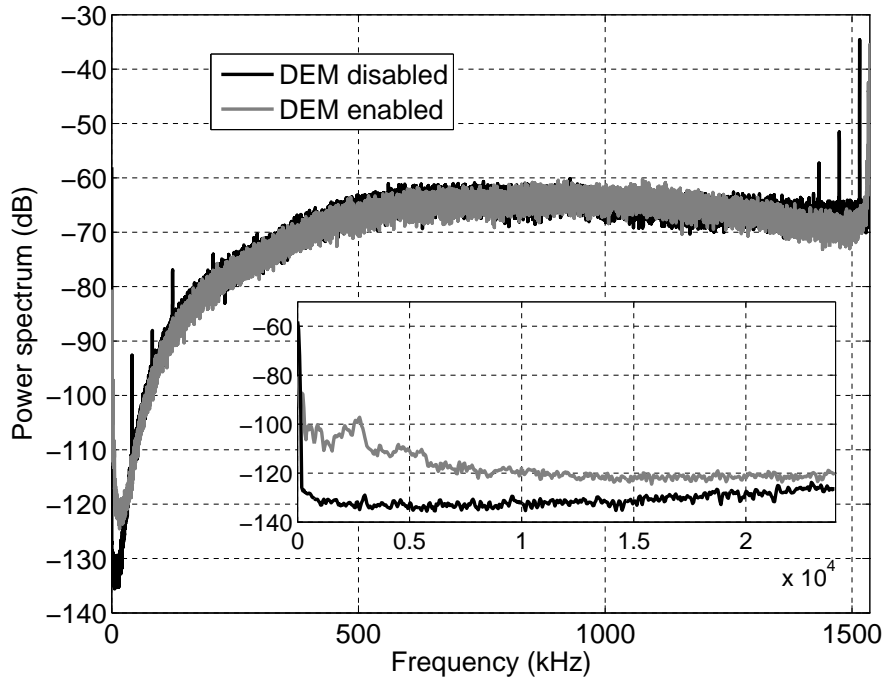
Figure 11.3: Idle channel performance of the $\Delta\Sigma$ modulator chip.

which is 5 dB degradation from the targeted performance of $3.7\,\mu V_{rms}$. There are three tones near $f_s/2$ and few tones out of the signal band which have a beat frequency of 18 kHz. It is suspected that the large jitter of the clock source is the cause of this 5 dB loss. When the DEM is enabled these tones vanish due the DEM action and the in-band noise floor increases, because at very low frequency the noise floor at the output of the modulator is decided by the first order mismatch error shaping of the DEM. However, the increase in the noise floor is found to be around 20 dB which is much larger than the simulation estimate.

On changing the bias currents of the loop filter, the supply voltage of the loop filter, the clock generation circuits/buffers, the reference voltage for the DAC, the frequency of the sampling clock, all within $\pm 5\,\%$ of its nominal value, similar performance trends and no appreciable change in the in-band integrated noise was observed. A possible

experiment in which the differential input signals to the modulator are left floating rather than being connected to its common mode voltage. In this setup the noise due to the input resistors doesn't contribute to the output. Further the noise of the first op-amp sees a transfer function of unity rather than a value of two. Hence the integrated noise at the output of the modulator is expected to reduce to $1.86\,\mu V_{rms}$ as per the calculations done in Section 6.4.2. On the contrary the noise profile remains more or less the same as observed in Figure 11.4. The in-band integrated noise in the open circuit condition is $6.1\,\mu V_{rms}$. This indicates that most of the noise contribution arises from the DAC. It is then suspected that the performance limitation arises due to stray coupling into the sensitive DAC reference voltage in the PCB.
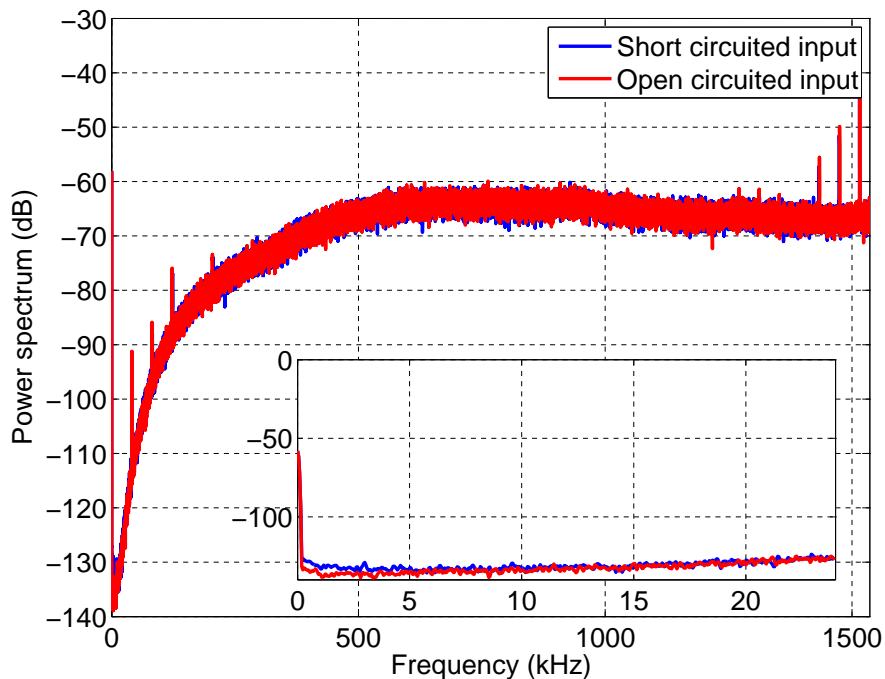
Figure 11.4: Idle channel performance with the differenital inputs open circuited.

11.2.2 Performance with sinusoidal input

The $\Delta\Sigma$ modulator chip is excited by a sinusoid at $5\,kHz$. Two million samples are taken from the output of the modulator and a Blackman-Harris window is applied before evaluating the power spectrum of the signal. The signal amplitude is varied from

millivolt to amplitudes near fullscale (3 V). It is found that the modulator is stable up to -0.7 dBFS. Figure 11.5 shows the output power spectrum of the signal for various input signal amplitudes.
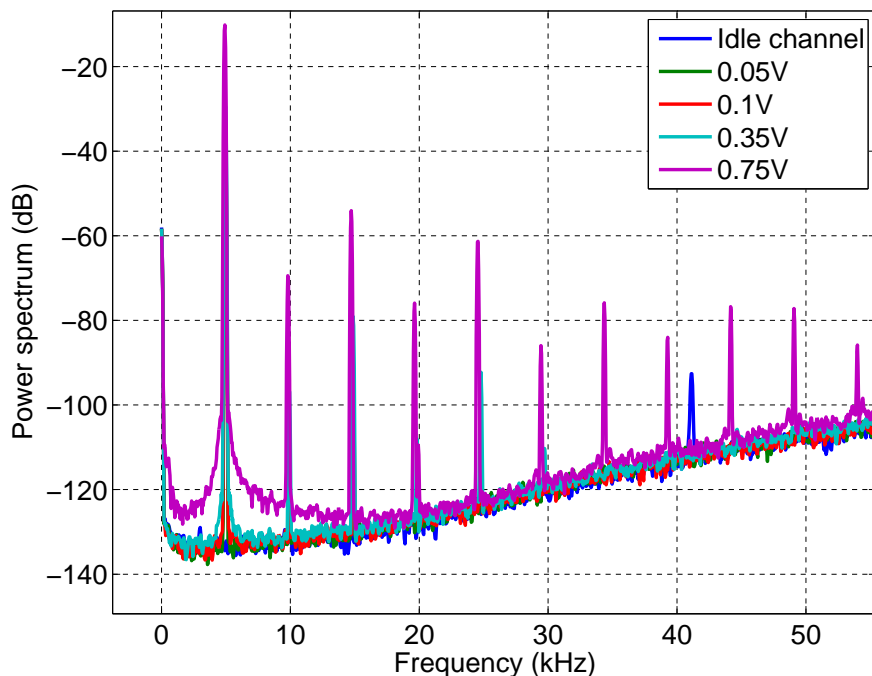
Figure 11.5: Spectrum from the $\Delta\Sigma$ modulator chip for a sinusoidal input at 5 kHz.

Very large harmonic distortion of the input sinusoid is found in the output spectrum. Further, the spectrum of the input signal spreads to multiple bins as the signal amplitude is increased. The noise floor of the modulator remains almost constant at smaller input amplitudes. It is suspected that the signal source used for generating the sinusoid and the single ended to differential converter limit the harmonic distortion of the modulator.

CHAPTER 12

Conclusions

This thesis involved with the design of low power and high precision components of a $\Delta\Sigma$ ADC for digital audio.

In the first part of the thesis a low power decimator of $100\,\mu\text{W}$ for audio bandwidths (20 Hz - 24 kHz) is designed in a $0.18\,\mu\text{m}$ CMOS process with 1.8 V supply. The decimator is designed with standard cells using automated CAD tools that helps to port the design across multiple processes easily. The measurement results from the decimator chip show that the chip consumes a power of $100\,\mu\text{W}$ from a 1.8 V supply and is operational down to a reduced supply of 0.9 V. Hence the power consumption of the decimator can be further reduced by generating a 0.9 V supply.

In the second part of the thesis a continuous-time $\Delta\Sigma$ modulator targeting a resolution of 18 bits (108 dB SNR) to digitize the signal in the bandwidth of 20 Hz - 24 kHz is designed in a $0.18\,\mu\text{m}$ CMOS process with 1.8 V supply. The measurement results from the chip show an idle channel in-band integrated noise voltage of $6.5\,\mu\text{V}_{rms}$ that is a 5 dB degraded performance from the target of $3.7\,\mu\text{V}_{rms}$. It is also found that the $\Delta\Sigma$ modulator is stable up to an amplitude of -0.7 dBFS. From the testing of the chip so far, it is concluded that the idle channel noise and the harmonic distortion of the modulator is limited by the jitter of the clock source and the harmonic distortion of the input signal source respectively.

APPENDIX A

Pin details of the decimator chip

Figure A.1 shows the layout of the decimator inside the pad frame. The functionality of each pin is described in Table A.1.
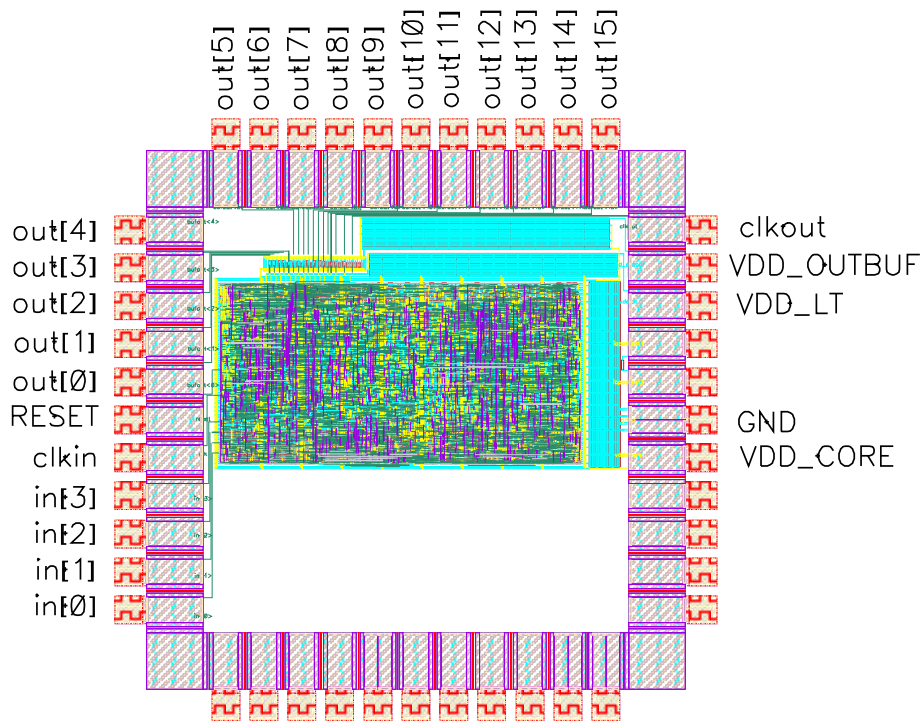
Figure A.1: Decimator chip.

Table A.1: Pin details of the decimator chip.

Pin Name	Description
in[0-3]	Four bit digital signal input
RESET	Active high reset, initializes output of all registers to logic zero
clkin	Input synchronizing clock (Rising edge)
out[0-15]	Sixteen bit digital output
clkout	Synchronization clock for the output data (Rising edge)
VDD_CORE	Supply voltage for decimator core
VDD_LT	1.8 V supply for the level translator
VDD_OUTBUF	1.8 V supply for the output buffers
gnd	Ground pin of the chip

APPENDIX B

Table of coefficients of the filters in the decimator

Table B.1: Coefficients of the first halfband filter (10th order)

Tap weight	Value	CSD
b0, b10	+0.0107421875	$+2^{-6} - 2^{-8} - 2^{-10}$
b2, b8	−0.0605468750	$-2^{-4} + 2^{-9}$
b4, b6	+0.2998046875	$+2^{-2} + 2^{-4} - 2^{-6} + 2^{-8} - 2^{-10}$
b5	0.5	$+2^{-1}$
b1, b3, b7, b9 are zero		

Table B.2: Coefficients of the second halfband filter (50th order).

Tap weight	Value	CSD
b0, b50	+0.002929687500	$+2^{-8} - 2^{-10}$
b2, b48	−0.002929687500	$-2^{-8} + 2^{-10}$
b4, b46	+0.004394531250	$+2^{-8} + 2^{-11}$
b6, b44	−0.006103515625	$-2^{-7} + 2^{-9} - 2^{-12}$
b8, b42	+0.008544921875	$+2^{-7} + 2^{-10} - 2^{-12}$
b10, b40	−0.011718750000	$-2^{-6} + 2^{-8}$
b12, b38	+0.015869140625	$+2^{-6} + 2^{-12}$
b14, b36	−0.021240234375	$-2^{-5} + 2^{-7} + 2^{-9} + 2^{-12}$
b16, b34	+0.028808593750	$+2^{-5} - 2^{-9} - 2^{-11}$
b18, b32	−0.040283203125	$-2^{-5} - 2^{-7} - 2^{-10} - 2^{-12}$
b20, b30	+0.059814453125	$+2^{-4} - 2^{-8} + 2^{-10} + 2^{-12}$
b22, b28	−0.103759765625	$-2^{-3} + 2^{-5} - 2^{-7} - 2^{-9} - 2^{-12}$
b24, b26	+0.317382812500	$+2^{-2} + 2^{-4} + 2^{-8} + 2^{-10}$
b25	+0.5	$+2^{-1}$
b1, b3, b7, … b21, b23, b27, b29, … , b47, b49 are zero		

Table B.3: Coefficients of the equalizer (34$^{\text{th}}$ order).

Tap weight	Value	CSD
b0, b34	-0.00054931640625	$-2^{-11} - 2^{-14}$
b1, b33	$+0.00006103515625$	$+2^{-14}$
b2, b32	-0.00006103515625	-2^{-14}
b3, b31	$+0.00012207031250$	$+2^{-13}$
b4, b30	-0.00012207031250	-2^{-13}
b5, b29	$+0.00012207031250$	$+2^{-13}$
b7, b27	$+0.00018310546875$	$+2^{-12} - 2^{-14}$
b8, b26	-0.00024414062500	-2^{-12}
b9, b25	$+0.00036621093750$	$+2^{-11} - 2^{-13}$
b10, b24	-0.00042724609375	$-2^{-11} + 2^{-14}$
b11, b23	$+0.00061035156250$	$+2^{-11} + 2^{-13}$
b12, b22	-0.0009155273437	$-2^{-10} + 2^{-14}$
b13, b21	$+0.00140380859375$	$+2^{-9} - 2^{-11} - 2^{-14}$
b14, b20	-0.00256347656250	$-2^{-9} - 2^{-11} - 2^{-13}$
b15, b19	$+0.00567626953125$	$+2^{-7} - 2^{-9} - 2^{-12} + 2^{-14}$
b16, b18	-0.02166748046875	$-2^{-5} + 2^{-7} + 2^{-9} - 2^{-12} + 2^{-14}$
b17	$+1.03527832031250$	$+2^{0} + 2^{-5} + 2^{-8} + 2^{-13}$

APPENDIX C

Reference currents for the $\Delta\Sigma$ modulator

The $\Delta\Sigma$ modulator needs four reference currents for biasing the four op-amps of the loop filter. The bias current for the first integrating op-amp $ibias1$ $(1\,\mu\text{A})$ is obtained external to the chip. The bias currents for the second, third integrating op-amps and the summing op-amp is obtained through the current mirror shown in Figure C.1. The master current $Iref$ $(0.5\,\mu\text{A})$ is obtained external to the chip.
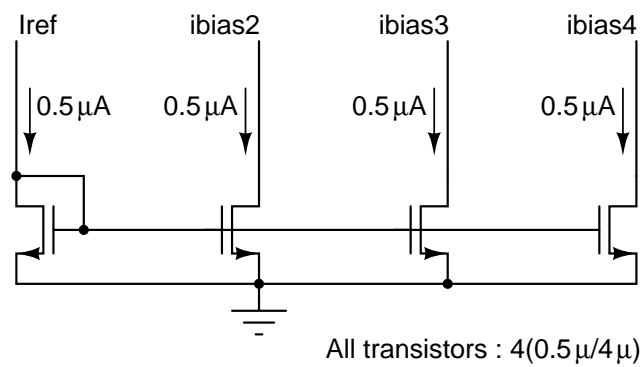

Figure C.1: Bias current generation for op-amps.

APPENDIX D

Pin details of the $\Delta\Sigma$ modulator chip

Figure D.1 shows the layout of the $\Delta\Sigma$ modulator inside the pad frame. The functionality of each pin is described in Table D.1.
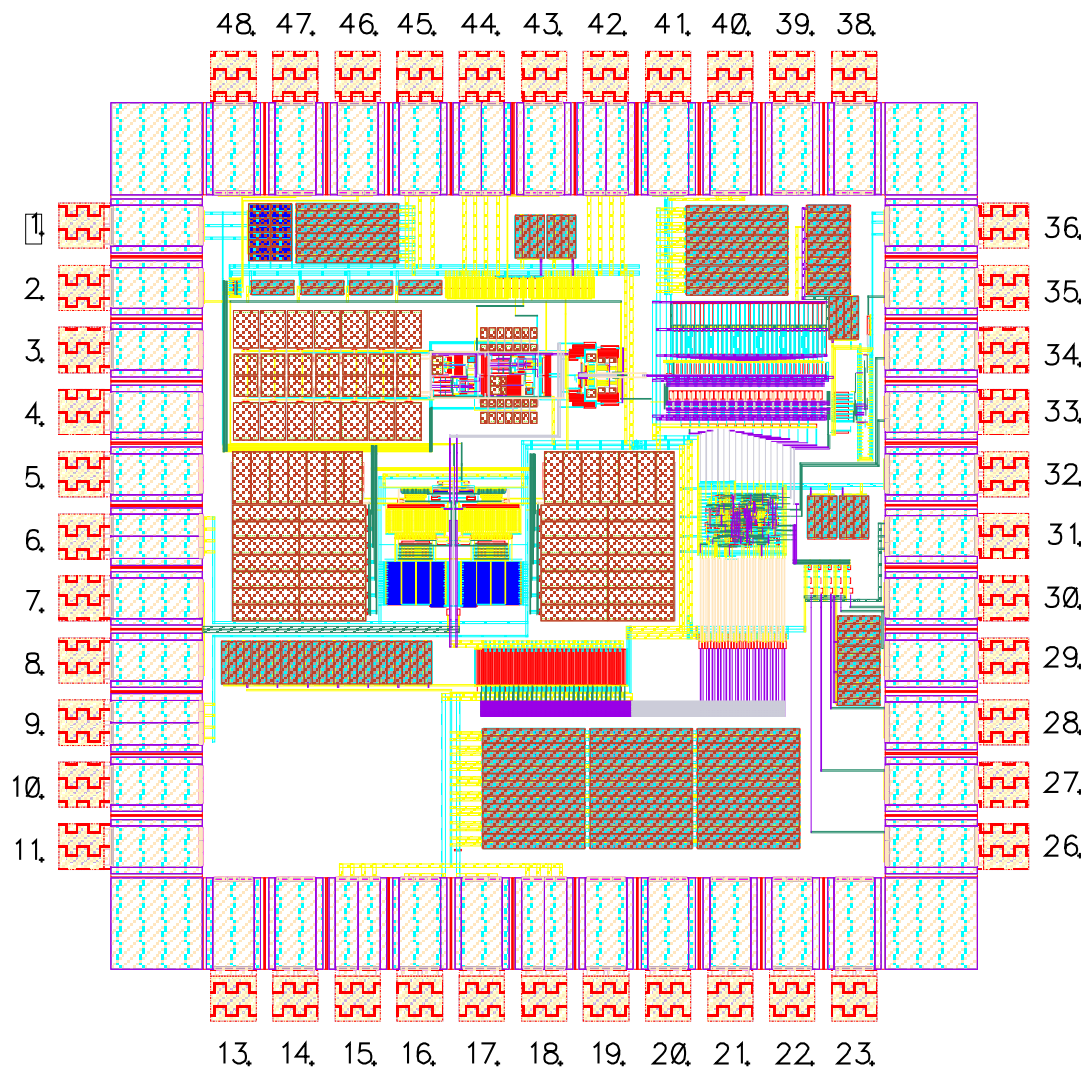

Figure D.1: $\Delta\Sigma$ modulator chip.

Table D.1: Pin details of the $\Delta\Sigma$ modulator chip.

Pin No	Pin name	Pin description
7,8	V_{ip}, V_{im}	Differential inputs to the modulator
1	ibias1	Bias current for the first integrator (1 μA, sink)
43	Iref	Bias current for the loop filter (0.5 μA, source)
46,47,48	bwc[2:0]	Three bit tuning control for the capacitor bank
2	V_{cm}	Common mode voltage (0.9 V)
40	Vadcref+	Reference voltage for the Flash ADC (1.8 V)
41	Vadcref-	Reference voltage for the Flash ADC 0 V (gnda)
17	Vdacref+	Reference voltage for DAC (1.8 V)
16	Vdacref-	Reference voltage for DAC 0 V (gnda)
35	clkin	Input clock (3.072 MHz)
27,28,29,30	adcout[3:0]	Four bit modulator output
26	clkout	Output sampling clock (negative edge)
45	Vdda	1.8 V Analog supply for the loop filter
32	Vddd	1.8 V Digital supply for the Flash ADC and the DEM
36	Vddc	1.8 V supply for clock generation circuit
31	Vdd_driver	1.8 V supply for the output clock and data buffers
6,9,15,18,42,44	gnda	Common ground pin
34	demenable	Enable/Disable DEM (1.8 V/0 V)
33	reset	Reset for DEM digital logic
Pins 3-5,10-15,19-25,37-39 are left unconnected		

REFERENCES

[1] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time $\Delta\Sigma$ ADC for audio applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 351–360, Feb. 2008.

[2] S. Pavan and P. Sankar, "A 110 μW single bit audio continuous-time oversampled converter with 92.5 dB dynamic range," in *Proceedings of ESSCIRC, 2009*, Sept. 2009, pp. 320–323.

[3] S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Wiley-IEEE press, New York, 1997.

[4] A. V. Oppenheim, R. W. Schafer, and J. R. Buck, *Discrete-Time Signal Processing*, 2nd ed. Prentice Hall, 1999.

[5] R. Crochiere and L. Rabiner, "Interpolation and decimation of digital signals - a tutorial review," *Proceedings of the IEEE*, vol. 69, no. 3, pp. 300 – 331, Mar. 1981.

[6] C. Barrett, "Low-power decimation filter design for multi-standard transceiver applications," Master's thesis, University of California, Berkeley, 1997.

[7] E. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. 29, no. 2, pp. 155–162, Apr. 1981.

[8] J. Candy, "Decimation for sigma delta modulation," *IEEE Transactions on Communications*, vol. 34, no. 1, pp. 72 – 76, Jan. 1986.

[9] K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*. Wiley India Pvt. Ltd., 2007.

[10] [Online]. Available: http://en.wikipedia.org/wiki/Signed-digit_representation

[11] R. Hewlitt and J. Swartzlantler, E.S., "Canonical signed digit representation for FIR digital filters," in *IEEE Workshop on Signal Processing Systems*, 2000, pp. 416–426.

[12] A. Chavan and E. MacDonald, "Ultra low voltage level shifters to interface sub and super threshold reconfigurable logic cells," in *IEEE Aerospace Conference*, 2008, pp. 1–6.

[13] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*. IEEE press, Piscataway NJ, 2005.

[14] H. Wang, "A geometric view of $\Sigma\Delta$ modulations," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 39, no. 6, pp. 402 –405, Jun. 1992.

[15] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta sigma modulators due to clock jitter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 10, pp. 2184 –2194, Oct. 2007.

[16] J. Cherry and W. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 6, pp. 661–676, Jul. 1999.

[17] J. A. Cherry, "Theory, practice, and fundamental performance limits of high-speed data conversion using continuous-time delta-sigma modulators," Ph.D. dissertation, Carleton University, Ottawa, Ontario, Canada, Nov. 1998.

[18] J. Cherry and W. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 376–389, Apr. 1999.

[19] S. Pavan, "Excess loop delay compensation in continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 11, pp. 1119–1123, Nov. 2008.

[20] V. Singh, N. Krishnapura, and S. Pavan, "Compensating for quantizer delay in excess of one clock cycle in continuous-time $\Delta\Sigma$ modulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 9, pp. 676–680, Sept. 2010.

[21] M. Hauser and R. Brodersen, "Circuit and technology considerations for mos delta-sigma A/D converters," *Oversampling delta-sigma data converters: theory, design, and simulation*, pp. 1310–1315, 1991.

[22] H. W. Bode, *Network Analysis and Feedback Amplifier Design*, 2nd ed. Princeton, NJ: Van Nostrand Reinhold, 1945.

[23] R. Baird and T. Fiez, "Linearity enhancement of multibit delta sigma A/D and D/A converters using data weighted averaging," *IEEE Transations Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[24] D. Groeneveld, H. Schouwenaars, H. Termeer, and C. Bastiaansen, "A self-calibration technique for monolithic high-resolution D/A converters," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 6, pp. 1517–1522, Dec. 1989.

[25] A. Leuciuc, "On the nonlinearity of integrators in continuous-time delta-sigma modulators," in *Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, 2001. MWSCAS 2001*, vol. 2, 2001, pp. 862–865.

[26] S. Ouzounov, R. van Veldhoven, C. Bastiaansen, K. Vongehr, R. van Wegberg, G. Geelen, L. Breems, and A. van Roermund, "A 1.2V 121-mode CT $\Delta\Sigma$ modulator for wireless receivers in 90nm CMOS," in *Digest of Technical Papers, IEEE International Solid-State Circuits Conference, 2007. ISSCC 2007*, Feb. 2007.

[27] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed. Prentice Hall, 2002.

[28] L. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 2, pp. 267–273, Apr. 1989.

Publications resulting from this work

International conference

1. **S. Parameswaran and N. Krishnapura**, A $100\,\mu$W decimator for a 16 bit 24 kHz bandwidth audio $\Delta\Sigma$ modulator, *2010 International Symposium on Circuits and Systems (ISCAS)*, Paris, France, 31 May-2 Jun. 2010.