A 0.5 V 90 dB SNDR 24kHz Continuous Time $\Delta\Sigma$ Modulator

&

Automatic Tuning of Time Constants in Single Bit Continuous Time $\Delta\Sigma$ Modulators

A Project Report

submitted by

SAURABH SAXENA

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THESIS CERTIFICATE

This is to certify that the thesis titled **A 0.5 V 90 dB SNDR 24kHz Continuous Time $\Delta\Sigma$ Modulator & Automatic Tuning of Time Constants in Single Bit Continuous Time $\Delta\Sigma$ Modulators**, submitted by **Saurabh Saxena**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally, I would like to dedicate this thesis to my parents, my sister and my brother for their support and encouragement through my entire life.

ABSTRACT

In the first project, a 0.5 V third order single bit fully differential continuous time $\Delta\Sigma$ modulator is presented. The presented modulator architecture uses true low-voltage design techniques, and does not require internal voltage boosting or low-threshold devices. A feedforward bulk-input OTA incorporating a current compensation for low frequency input signals is proposed. Fixing the common mode voltage of the bulk-input OTAs with error amplifiers is also proposed. Charge rejection in bulk-input comparators and power dissipation in bulk-input pre-amplifiers and regeneration circuits have been addressed in the design. Circuit techniques to reduce the change in delays implemented by a chain of inverters, due to systematic variations, have been proposed. Implemented on a 180 nm CMOS process, the modulator achieves a peak SNDR of 90 dB in a 24 kHz bandwidth, and occupies an area of 0.65 mm^2; the modulator consumes 370 μW at 25°C for the 'tt' process corner.

In the second project, we describe an in-situ analog technique for estimating time constant shifts in continuous-time single bit delta sigma modulators. We show that the variance of the first integrator output of the modulator's loop filter is a good indicator of RC time constants. The nominal values of the time constants are restored by digitally controlling the resistance and capacitance values (realized as switched banks). Simulation results that demonstrate the efficacy of the time-constant tuning system are given for a third order CIFF modulator.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CIFF	Cascaded Integrators with distributed feedforward
CMFB	Common Mode Feed-Back
CT	Continuous Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DSM	Delta Sigma Modulator
MSA	Maximum Stable Amplitude
NTF	Noise Transfer Function
OBG	Out of Band Gain
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PSD	Power Spectral Density
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
$V_{pp,diff}$	Peak to Peak Differential Voltage

CHAPTER 1

Introduction

The continuous reduction of minimum feature sizes in modern CMOS technologies into the nanoscale requires a proportional reduction of the supply voltage to well below 1 V to maintain reliability. At the same time, the threshold voltage (V_T) of the devices is not scaled proportionally to limit the leakage currents. The combination of low supply voltages and high device thresholds poses very challenging constraints on analog circuit design. A solution to operate analog circuits from a low supply voltage is to use internal voltage boosting techniques [1]-[4]. However, this approach increases the risk of gate-oxide breakdown, and could affect reliability of nanoscale CMOS implementations. Another solution for low-voltage analog circuit design is to use low-threshold-voltage devices or even depletion MOS. As many modern CMOS technologies provide low-threshold options, this is a viable solution, but involves additional masks and higher fabrication costs.

The objective in the first part of this work is to explore new circuit-level and architechture-level solutions for *true* low-voltage analog ICs, i.e, without using internal voltage boosting or low-threshold voltage devices so that the designs will be compatible with future nanoscale standard digital technologies, when the target supply voltage is 0.5 V. For any high-performance application that requires high bandwidth or sampling rate, MOS devices are biased in strong inversion, i.e., ($V_{Gs} - V_T = 0.2$ V). The devices act as transconductors or current sources as long as $V_{DS} \geq V_{DS,sat}$. A good estimate of $V_{DS,sat}$ at the edge of strong inversion or in weak and moderate inversion is about 0.15 V [5]. So, in any region of operation, we need to maintain V_{DS} of at least 0.15V, irrespective of device V_T. The common-source configuration thus has the potential to operate at supply voltages of 0.5 V.

Forward biasing of the body-source junction lowers the V_T of the transistors. We typically apply a forward bias of about 250 mV, which results in a lowering

of the V_T by about 50 mV. In the context of 0.5 V operation, the risk of forward-biasing the junctions is minimized since parasitics bipolar devices cannot be activated even when the full power supply is applied as forward bias, provided that supply transient overvoltages are adequately kept under control.

Delta Sigma modulators find an extensive use in modern signal processing, with their high resolution output achieved by high oversampling rate and the concept of noise shaping. Authors in [8] have implemented "An audio-band CTDSM with 74 dB SNDR at supply voltage 0.5 V". Using improved low-voltage circuit techniques and with nearly same power dissipation as in [8], a 0.5 V single bit 90 dB SNDR 24 kHz CTDSM with NRZ DAC has been implemented in this work.

The organization of the thesis discussing the topics related to 0.5 V single bit CTDSM is as follows:

In Chapter 2 we present the design specifications of the single bit continuous time delta sigma modulators.

Basic circuit techniques at 0.5 V supply are discussed in the following two chapters.

In Chapter 3 we discuss the error amplifier.

In Chapter 4 we discuss the bulk-input transconductance amplifier.

In Chapter 5 we present the circuit implementation of a 0.5 V single bit CTDSM.

A practical problem with CTDSMs is the change in the loop Noise Transfer Function (NTF) due to systematic variations of the loop filter time constants with process and temperature spreads. It is seen that some kind of time-constant tuning system is necessary to realize CTDSM whose performance remains robust with process and temperature variations.

In Chapter 6 we present a new automatic time-constant tuning technique for single bit CTDSMs.

CHAPTER 2

Design Specifications of a Single Bit CTDSM

2.1 Introduction

Continuous-time Delta-sigma Modulators (CTDSM), as alternatives to their discrete-time counterparts, have been receiving much attention due their ineherent anti-aliasing properties and low power dissipation. While a multi-bit modulator has many advantages over a single bit design, the latter is attractive in several aspects. The inherent linearity of the single bit feedback DAC eliminates the need for Dynamic Element Matching (DEM) circuitry that would be needed in multibit design. At high sampling rates, the DEM block can be power hungry, apart from introducing a significant delay in the loop. For modulators operating at low speeds (for example, those designed for audio applications), a single bit modulator can be significantly smaller due to the reduced size of the feedback DAC.

In this thesis, a single bit third order Continuous Time Delta Sigma Modulator (CTDSM) has been implemented as a Cascaded Integrators with Feed Forward (CIFF) topology, in a 180 nm technology at 0.5 V supply, with the basic concepts of the modulator design as given in [18]. The sampling frequency (f_s) and Over Sampling Ratio (OSR) of the modulator are 6.144 MHz and 128 respectively. The Noise Transfer Function (NTF) has optimized zeros in the signal band. For stability reasons, the out of band gain of the NTF in the modulator is 1.5 [18]. Thermal noise limits SNR of the modulator to 90 dB whereas quantization noise and harmonic distortion limit SNDR to 96 dB over process and temperature.

The block diagram of the single bit third order CTDSM is shown in Fig. 2.1. Intergator coefficients k_{i1}, k_{i2} and k_{i3} are chosen to limit the swings at the output of the integrators. Summing coefficients k_0, k_1, k_2 and k_3 are chosen to match NTF

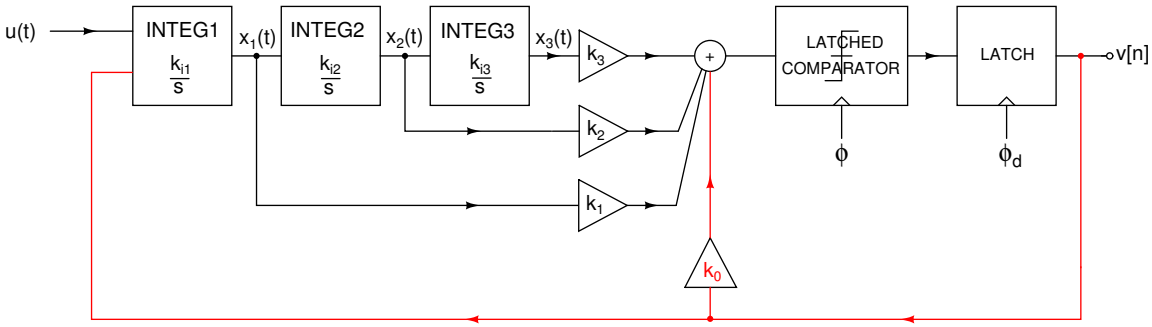


Figure 2.1: Block diagram of a third order CTDSM. k_{i1}, k_{i2} and k_{i3} are integrator scaling factors. k_0, k_1, k_2 and k_3 are summing coefficients for the summing amplifier. ϕ_d is delayed version of clock ϕ.

for the modulator in circuit with the desired ideal NTF. These coefficients are calculated by closed loop NTF fitting as given in [9]. The circuit implementation of the modulator is explained in Chap. 5.

CHAPTER 3

Error Amplifier Design

3.1 Introduction

The error amplifier referred to in this thesis is an inverter whose switching threshold voltage is governed over process and temperature by a bias voltage V_{amp}, applied to the bulk terminals of MOSFETs used in the inverter [6]. This bias voltage is generated by a closed loop of three inverters in a chain. We find an extensive use of error amplifiers in biasing circuits at 0.5 V supply voltage.

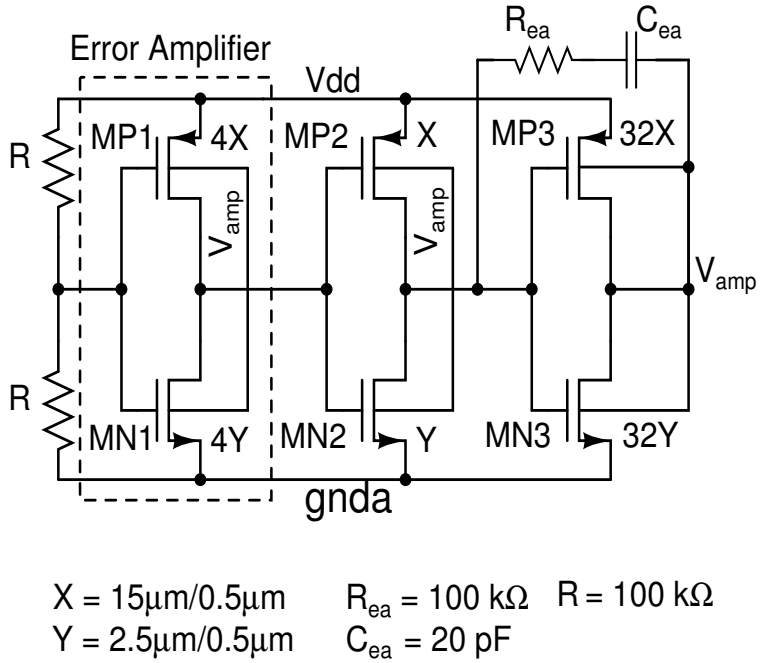


Figure 3.1: Error Amplifier biasing loop to fix the switching threshold voltage to $V_{dd}/2$.

The circuit diagram of the error amplifier biasing loop is shown in Fig. 3.1. Sizes of the pMOS and nMOS devices are chosen such that the input and output voltages and the bulk terminals of both the MOSFETs for an inverter is $V_{cm} = V_{dd}/2$,

for a given process and temperature. When these inverters with sizing for one particular process and temperature are used in a loop as shown in Fig. 3.1, the bulk terminals of both pMOS and nMOS devices are controlled to fix the switching threshold voltage at V_{cm}. Consider a case when threshold voltage of the nFET in the inverter increases, then the output of the first inverter in the loop will increase. As a result, output of the second inverter will decrease and output of the third inverter will increase. Now, an increased bulk potential will reduce the threshold voltage of nMOS and will bring the switching threshold voltage of nMOS back to V_{cm}. A similar case holds true for decrease in threshold voltage of nMOS and variation in threshold voltage of pMOS.

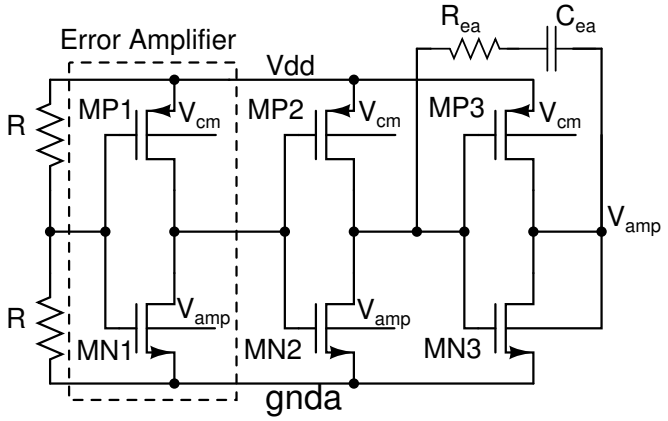


Figure 3.2: Circuit diagram of the error amplifier biasing loop to fix the switching threshold voltage to $V_{dd}/2$ as given in [6].

The biasing voltage V_{amp} can also be generated by applying feedback to either of the pMOS or nMOS devices only as shown for the nMOS device case in Fig. 3.2. Here, the feedback is applied to the bulk terminals of the nMOS devices only. As the pMOS devices are biased at fixed voltages, they show a large variation in current over process and temperature. Also, the feedback gain has reduced in the form of reduced g_{mb}. So, it seems beneficial to control both the devices as shown in Fig. 3.1. The power consumption for the error amplifier biasing loop shown in Fig. 3.1, varies from 2.3 μW to 6 μW from 'ss' process to 'ff' process corners in 180 nm CMOS technology.

In general, the bias voltage (V_{in}) generated by a biasing circuit goes through

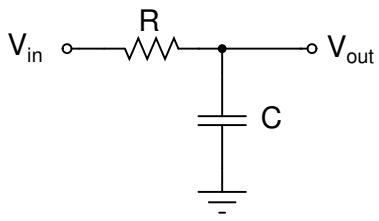


Figure 3.3: Low pass filter.

a low pass filter (output of the low pass filter is V_{out}) before it is applied to the desired node as shown in Fig. 3.3. However, if the bulk controlling bias voltage (V_{amp}) has to go through a filter in Fig. 3.3, there will be a potential drop from V_{in} to V_{out}. It is not advisable to filter this bias voltage (V_{amp}) because control in threshold voltage is directly dependent on bulk to source voltage (V_{sb}) and any resistance in the path of this bias voltage will vary the desired potential V_{sb} and the properties of MOSFETs after biasing.

The number of inverters to be used in the error amplifier biasing loop depends on the load at node V_{amp}. The bulk current supplied at node V_{amp} should be much smaller than the drain current of the inverter at the output of the biasing loop. R_{ea} and C_{ea} form the Miller compensation network for the feedback loop. The DC characteristics of an error amplifier biased using V_{amp} is shown in Fig. 3.4.

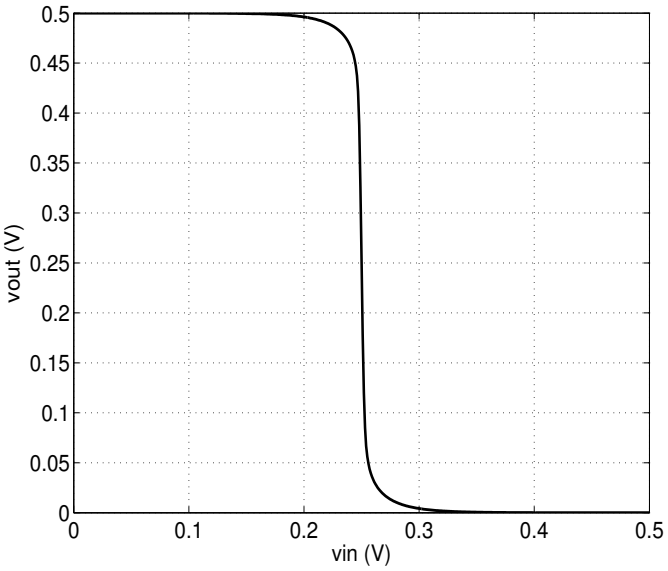


Figure 3.4: DC characteristics of an error amplifier biased at V_{amp} for the 'tt' process corner at 70°C.

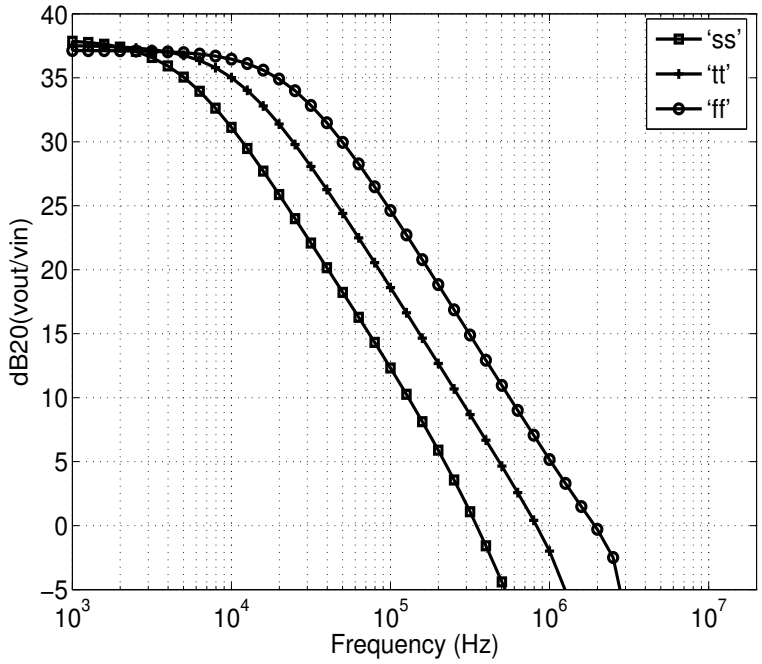


Figure 3.5: AC characteristics of an error amplifier for different process corners at 70°C.

The AC characteristics of an error amplifier biased with V_{amp} and V_{cm} as bulk and gate voltages respectively, a drain current of 120 nA and a load of 1 pF capacitor, are shown in Fig. 3.5.

3.2 Biasing with Error Amplifiers

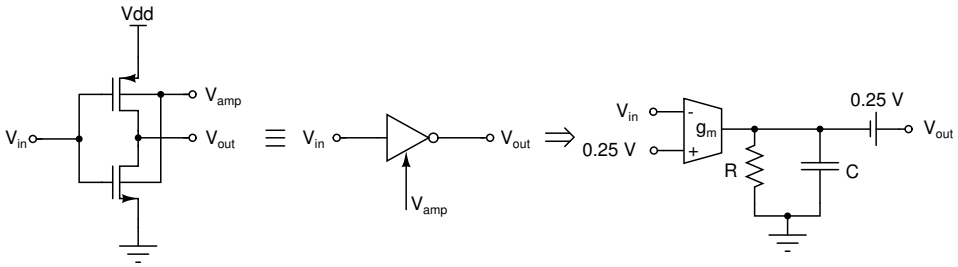


Figure 3.6: Linear model of an error amplifier biased using V_{amp} .

The linear model of an error amplifier is shown in Fig. 3.6. Biased with V_{amp} and V_{cm} voltages, the error amplifier behaves like an inverting amplifier with a transconductance g_m. A circuit to bias a MOSFET with a fixed current can

be derived from the conventional bias circuit shown in Fig. 3.7(a), using error amplifiers as shown in Fig. 3.7(b).

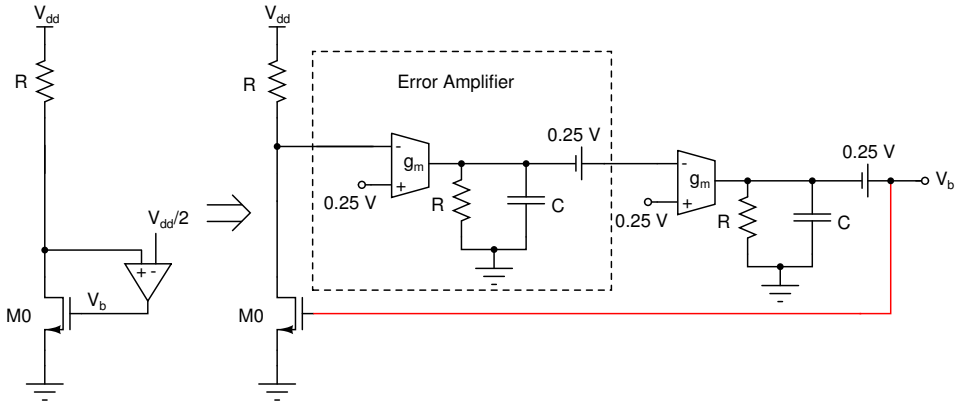


Figure 3.7: (a) A conventional bias circuit and (b) a bias circuit using error amplifiers.

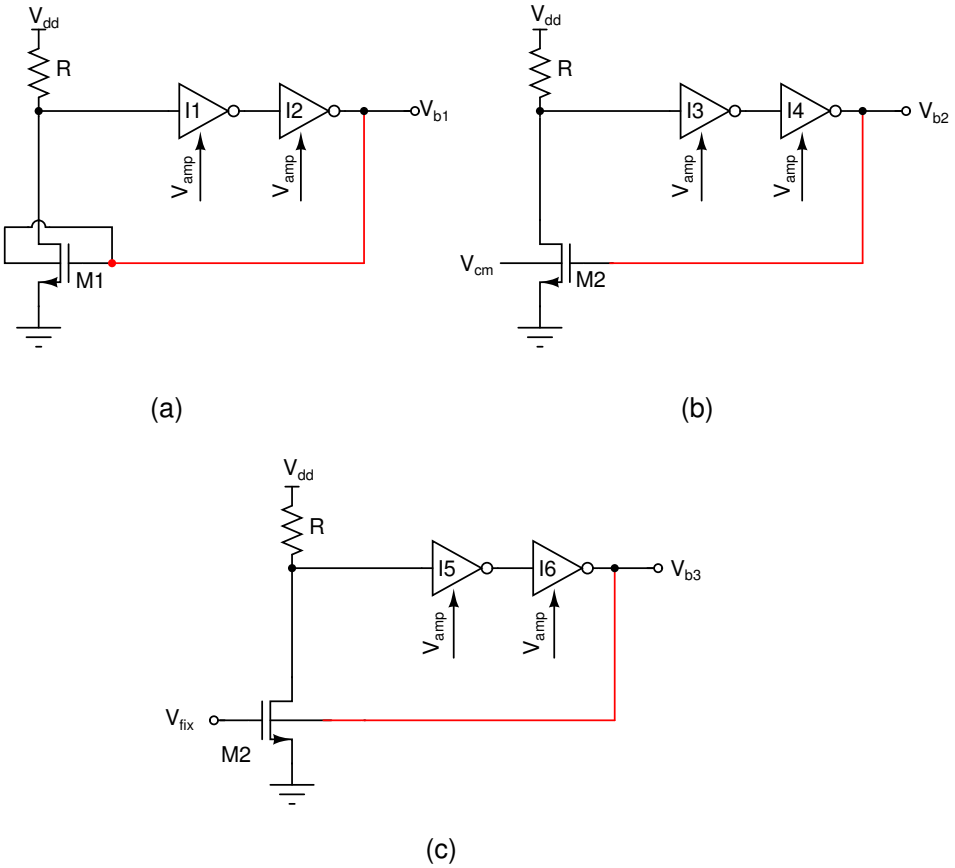


Figure 3.8: Generating bias voltage by controlling (a) both gate and bulk voltage, (b) only gate voltage and (c) only bulk voltage of a MOSFET.

Fig. 3.8 shows three different circuit diagrams for biasing MOSFETs with fixed

current. For same value of a current, size of a nMOS device can be decreased by controlling both the bulk and gate terminals as shown in Fig. 3.8(a) as compared to the case when only gate potential is controlled as shown in Fig. 3.8(b). However, this will put an extra burden on the error amplifier I2 to supply the bulk current to other current sources in the circuit. Whereas when a MOSFET is biased for fixed current by controlling only gate potential, the bias circuit does not have to provide any current to the current sources biased with same bias voltage in other circuits. So, the bias voltage generation circuit shown in Fig. 3.8(b) is preferred. One can also think of generating a bias voltage by controlling only bulk terminal with fixed gate potential as shown in Fig. 3.8(c). However, it has been found that in such a case even the variation of the bulk bias voltage over full supply voltage is not sufficient to carry the same current over different process corners. This is due to the fact that drain current has a weaker dependence on the bulk voltage as compared to the gate voltage.

When MOSFETs are biased for fixed current using error amplifiers, sizes of these devices have to be chosen in a manner such that the bias voltage like V_{b2} in Fig. 3.8(b), should be atleast 50 mV away from the supply voltages. In case this bias voltage goes near to the supply voltage, the error amplifiers will be much away from the region of operation near V_{cm}. This will drift away the input voltage of the error amplifier sensing the drain terminal of M0 in Fig. 3.8 and the current will not be $V_{dd}/2R$ anymore.

The bias circuit shown in Fig. 3.8(b) has a high loop gain with three integrators namely error amplifier I3, error amplifier I4 and nFET M0 in the loop. The biasing loop can be stabilized by reducing the gain in the bias loop using error amplifier I5 and Miller compensation with R_m and C_m as shown in Fig. 3.9.

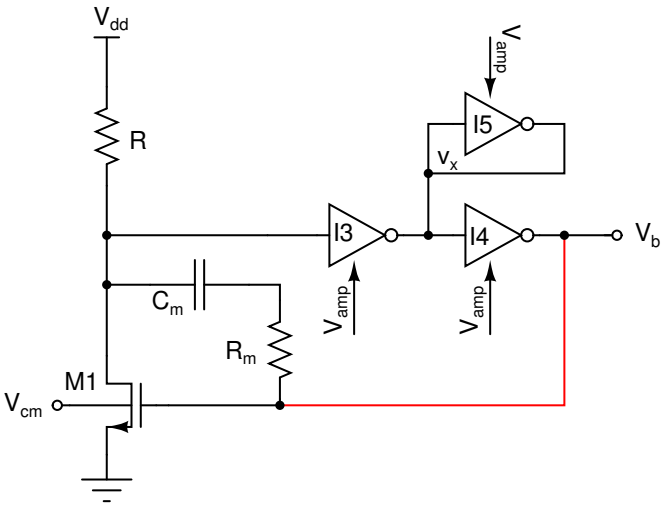


Figure 3.9: Bias generation circuit with Miller compensation.

CHAPTER 4

Bulk Input Operational Transconductance Amplifier (OTA)

4.1 Introduction

A safe acess to bulk terminals of MOSFETs, to apply signals without allowing any significant current leakage due to forward biasing of the bulk-source junction at low supply voltages, gives a way to a new family of operational transconductance amplifiers named as bulk-input OTAs.

4.2 Bulk-input OTA

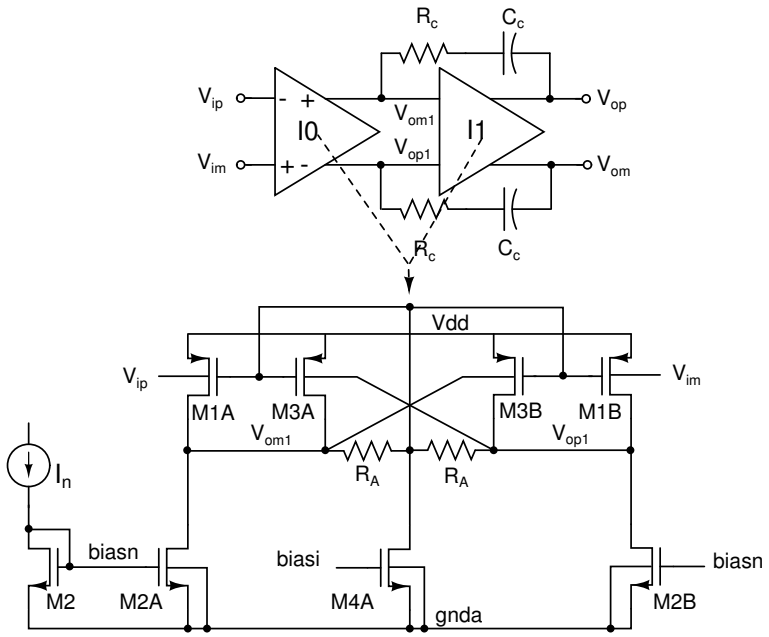


Figure 4.1: Circuit diagram of a Miller compensated bulk-input OTA.

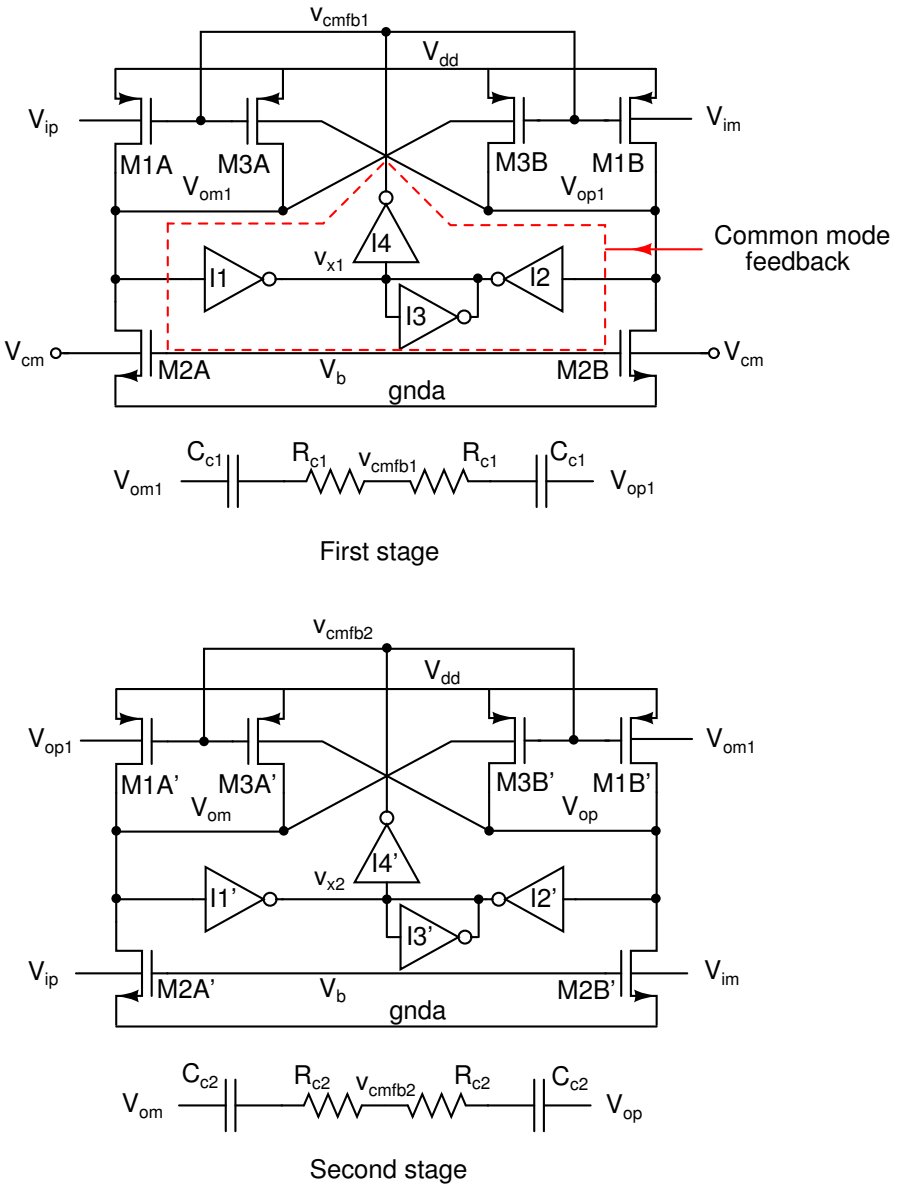
Bulk terminal behaves similar to gate terminal for signals other than the fact that it draws some current whereas gate terminal is inert in this respect. This current can be limited by the swing at the bulk terminals. Gain of a bulk-input OTA is proportional to g_{mb} (bulk transconductance). As g_{mb} is smaller than g_m for MOSFETs, gain of the bulk-input amplifier is lesser than the gain of the gate-input OTA. The circuit diagram of a Miller compensated bulk-input OTA as given in [8], is shown in Fig. 4.1.

The gain of the bulk-input OTA is increased by introducing negative resistance at the output of each stage of the OTA in the form of bulk controlled pMOS devices M3A and M3B. Resistors R_A are used for local common mode feedback. However, it reduces DC gain at the output. Output common mode voltage for a two stage bulk-input OTA is controlled by controlling *biasi* in Fig. 4.1, using a replica OTA and error amplifiers [8]. This leads to extra power dissipation. Common mode voltage can also be sensed by using source followers. Keeping size in consideration, the gate overdrives have to be about 0.4 V and 0.1 V for nMOS and pMOS devices respectively for 'ss' process corner. So, sensing a common mode voltage of $V_{cm} = V_{dd}/2$ using either of the source followers pMOS or nMOS devices, is not reasonable. After sensing common mode voltage, a single ended opamp is required to fix the common mode voltage. It adds to the power dissipation in a bulk-input OTA. Using large Miller compensating capacitors limits the bandwidth of the OTA. Addressing these issues, a new design of a bulk-input OTA in the form a feedforward bulk-input OTA has been proposed as shown in Fig. 4.2.

The DC gain of the first stage of the bulk-input OTA is given by eq.(4.1).

$$\frac{V_{out}}{V_{in}} = \frac{g_{mb,M1A}}{g_{ds,M1A} + g_{ds,M2A} + g_{ds,M3A} - g_{mb,M3A}} \tag{4.1}$$

The negative resistance introduced by $g_{mb,M3A}$ at the output of the first stage should be carefully designed to keep the above gain positive over process and temperature variations and similarly for the second stage. It has been found that if the denominator in (4.1) is close to zero (positive) to have a high gain in first



M1A, M1B, M1A', M1B'	18(6µm/0.5µm)
M2A, M2B, M2A', M2B'	10(2µm/0.5µm)
M3A, M3B, M3A', M3B'	2(6µm/0.5µm)
I1, I2, I3, I4, I1', I2', I3', I4'	Single finger error amplifier
R_{c1}, R_{c2} 8 kΩ	C_{c1}, C_{c2} 0.3 pF

Figure 4.2: Circuit diagram of a feedforward bulk-input OTA. Error amplifiers are biased with V_{amp}.

place, it may become negative over process and temperature spreads.

Current sources M2A, M2B, M2A' and M2B' are biased for 10 μA of current each, using error amplifiers as shown in Fig. 4.3. The biasing loop is stabilized using R_m & C_m. Error amplifiers I1 and I3 form an inverter of gain -1.

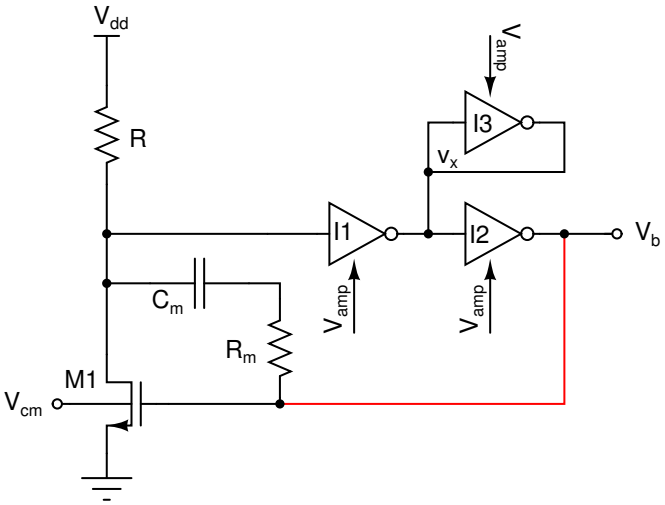


Figure 4.3: Bias circuit for bulk-input OTA.

Feedforward compensation of the bulk-input OTA is implemented by applying the opamp input to the bulk terminals of nMOS transistors in the second stage. The gain of the bulk-input OTA in Fig. 4.2 is given by (4.2).

$$\begin{aligned}\frac{V_{out}}{V_{in}} = & \frac{g_{mb,M2A'}}{g_{ds,M1A'} + g_{ds,M2A'} + g_{ds,M3A'} - g_{mb,M3A'}} \\ & + [\frac{g_{mb,M1A'}}{(g_{ds,M1A'} + g_{ds,M2A'} + g_{ds,M3A'} - g_{mb,M3A'})} \\ & \times \frac{g_{mb,M1A}}{(g_{ds,M1A} + g_{ds,M2A} + g_{ds,M3A} - g_{mb,M3A})}]\end{aligned} \tag{4.2}$$

Error amplifiers biased with V_{amp} can be used to sense and fix the common mode voltage as shown in Fig. 4.2, where error amplifiers I1, I2, I3 and I4 form the common mode feedback loop. Here, error amplifiers I1 and I2 sense the common

mode voltage and the feedback is applied by I4 to the gate terminals of the pMOS transistors. We know that an error amplifier used in a feedback loop and biased at V_{amp} will try to push its input to V_{cm} because of its high gain at V_{cm}. Error amplifier I3 is used to reduce the gain in the common mode feedback loop. R_{c1} (R_{c2}) and C_{c1} (C_{c2}) are used for Miller compensation in the common mode feedback loop.

4.2.1 Characteristics of the bulk-input OTA

The bulk-input OTA (as shown in Fig. 4.2), has been characterized with a differential load of 50 kΩ resistance and 2 pF capacitance in series as shown in Fig. 4.4.

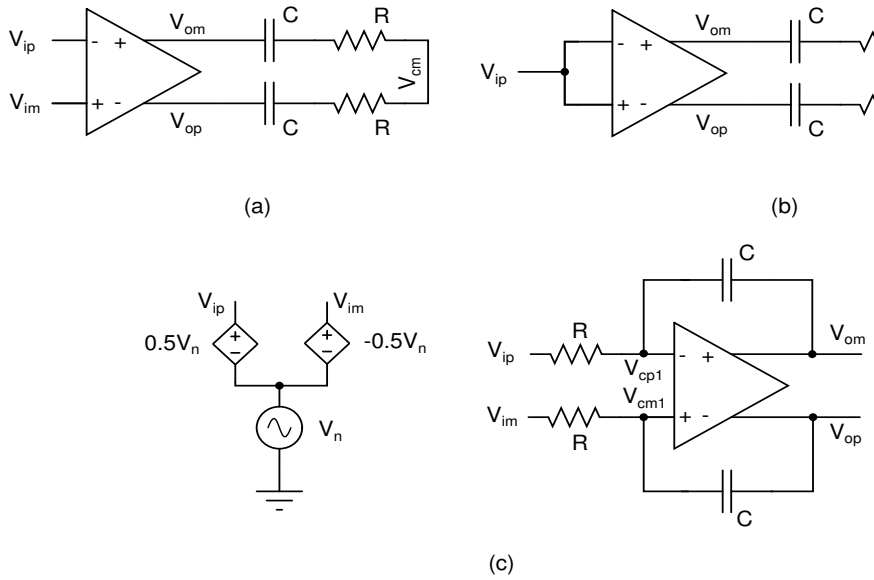


Figure 4.4: (a) Circuit for differential frequency response, (b) Circuit for common mode frequency response and (c) Circuit for finding input referred noise referring it to voltage source V_n.

The differential and common mode frequency responses of the bulk-input OTA is given by eq.(4.3) and eq.(4.4) respectively.

$$H(s) = \frac{V_{op}(s) - V_{om}(s)}{V_{ip}(s) - V_{im}(s)} \tag{4.3}$$

$$H_c(s) = \frac{V_{op}(s) + V_{om}(s)}{2V_{ip}(s)} \tag{4.4}$$

The differential frequency and phase response of the OTA is shown in Fig. 4.5. The common mode frequency response of the OTA is shown in Fig. 4.6. The characteristics of bulk-input OTA over process variation at 70°C is tabulated in Table. 4.1.

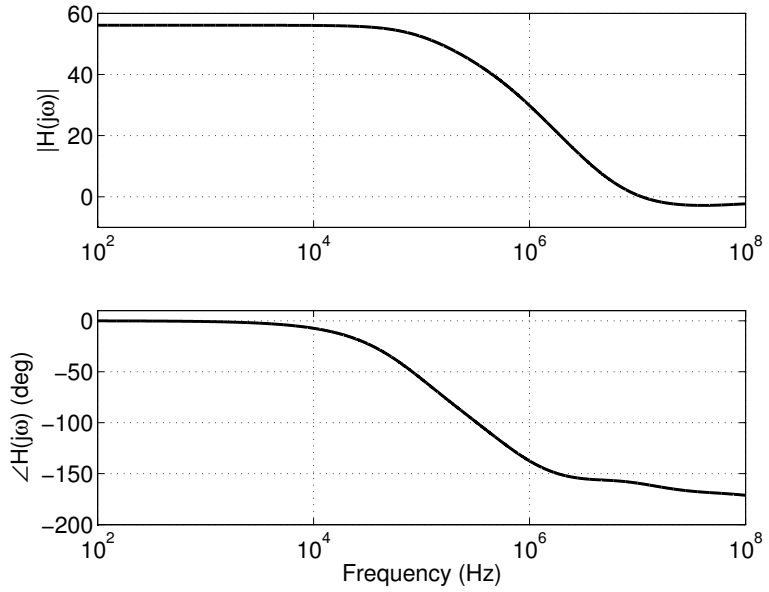


Figure 4.5: Magnitude and phase response of the bulk-input OTA for the 'tt' process corner at 70°C.

Table 4.1: Characteristics of the bulk-input OTA.

Process	ss	tt	ff
Output dc voltage (V)	0.249	0.249	0.249
DC gain (dB)	59.8	56.1	53.51
Phase Margin (degrees)	37	40	42
Bandwidth (MHz)	10.86	10.96	11.03
Power (μW)	20.04	20.34	20.92
Input ref. noise @ 10 kHz (nV/$\sqrt{\text{Hz}}$)	85.81	86.60	87.46
Input ref. noise @ 1 MHz (nV/$\sqrt{\text{Hz}}$)	80.58	81.10	81.69

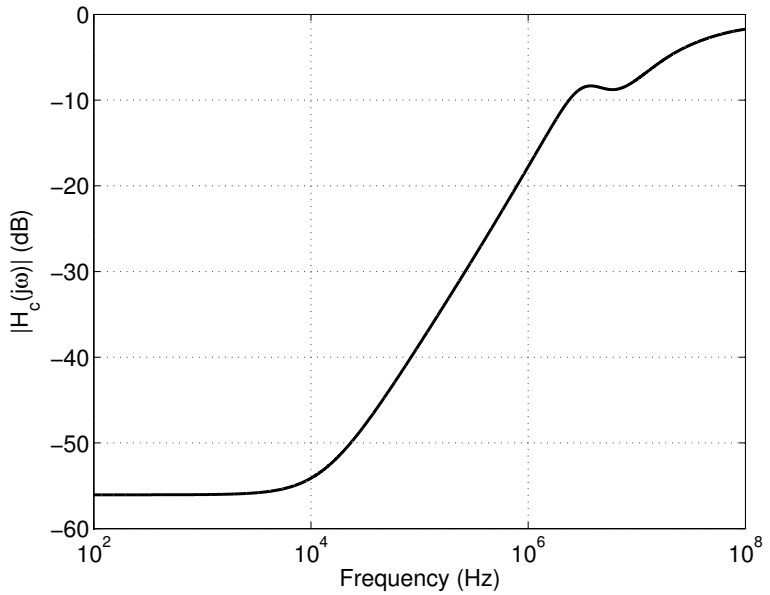


Figure 4.6: Common mode magnitude response of the bulk-input OTA for the 'tt' process corner at 70°C.

CHAPTER 5

Circuit Design of a 0.5 V Single Bit Continuous Time $\Delta\Sigma$ Modulator

5.1 Introduction

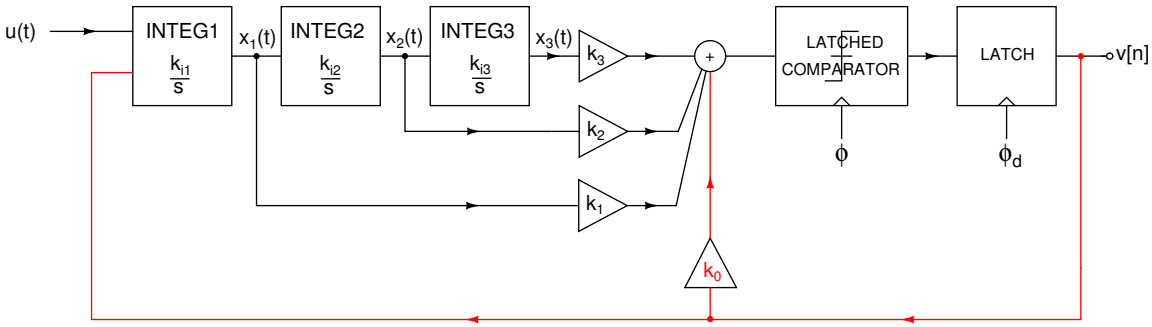


Figure 5.1: Block diagram of a third order CTDSM. k_{i1}, k_{i2} and k_{i3} are integrator scaling factors. k_0, k_1, k_2 and k_3 are summing coefficients for the summing amplifier. ϕ_d is delayed version of clock ϕ.

The block diagram of the single bit third order CTDSM is shown in Fig. 5.1. In active-RC implementation of the CTDSM, intergator coefficients k_{i1}, k_{i2} and k_{i3} and summing coefficients k_0, k_1, k_2 and k_3 decide the values of resistors and capacitors for integrator and summer blocks.

Process and temperature variations will vary RC time-constant for the integrators. It is difficult to tune RC time-constant with reasonable switch size in R and C banks at such a low supply voltage. The increase in RC time-constant degrades SNDR by increasing in-band quantization noise whereas decrease in RC time-constant reduces the Maximum Stable Amplitude (MSA) for the modulator and it may make the modulator unstable. To lessen the effects of the decrease in RC time-constant, all R and C values for the integrators are increased by 5%

from their nominal values. All the blocks in Fig. 5.1 are discussed in detail in the follwing sections.

5.2 First Integrator

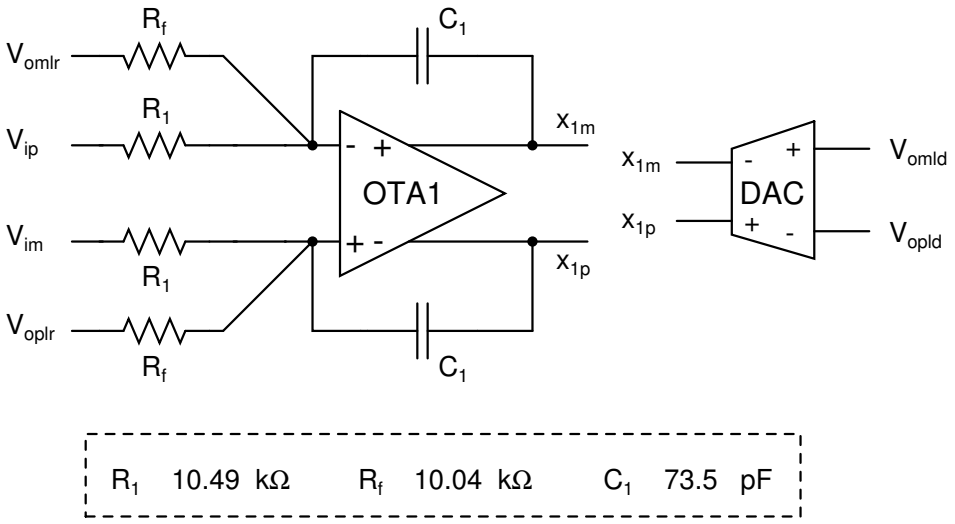
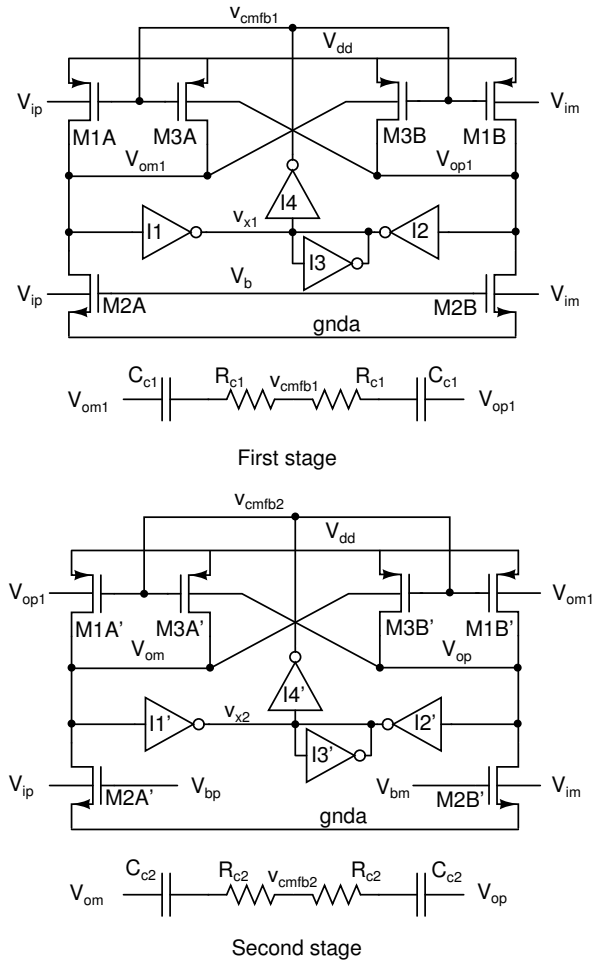


Figure 5.2: Circuit diagram of the first integrator (INTEG1).

Fig. 5.2 shows the circuit diagram of the first integrator. The first integrator in the modulator consists of OTA1, the resistors for the input and feedback signals (R_1 and R_f respectively) and the integrating capacitor (C_1). R_1 and R_f are determined by thermal noise considerations.

Non-linearity in an OTA contributes to significant distortion in the output of the modulator. This non-linearity can be as a result of large signal swings at input and output of an OTA and a sudden change in current supplied by OTA whenever the modulator output changes state. In the first OTA design used in the modulator, a change in current due to input signal is compensated by a g_m compensation technique incorporated in OTA1. Switching current through feedback resistor R_f is compensated using current steering DAC at the output of OTA1. Hence, the distortion due to large signal swings and current change are minimized for OTA1. The idea was first reported in [10].

5.2.1 Operational Transconductance Amplifier 1 (OTA1)



M1A, M1B	148(14µm/1.5µm)		M1A', M1B'	96(6µm/0.5µm)	
M2A, M2B	80(2µm/0.5µm)		M2A', M2B'	50(2µm/0.5µm)	
M3A, M3B	12(14µm/1.5µm)		M3A', M3B'	6(6µm/0.5µm)	
R_{c1}	1.2 kΩ	R_{c2} 3.0 kΩ	I1, I2, I3, I4	Error amplifiers with 4 fingers each	
C_{c1}	3.0 pF	C_{c2} 2.0 pF	I1', I2', I3', I4'	Error amplifiers with 2 fingers each	

Figure 5.3: Circuit diagram of OTA1 in CTDSM.

OTA1 is a two stage feedforward bulk-input amplifier. The circuit diagram of OTA1 is shown in Fig. 5.3. The length of the pMOS transistor in first stage is chosen to be 1.5 μm to reduce flicker noise. The input signal is applied to the bulk terminals of pMOS and nMOS devices. An increased input $g_{mb} = g_{mb,pMOS} + g_{mb,nMOS}$ will reduce the input referred noise of OTA1. The bias voltage V_b for the first stage in OTA1, is generated as shown in Fig. 4.3. As shown in the bias

generation circuit, the bulk terminal of the nMOS transistor is connected to V_{cm}. So, the nMOS devices in the bias generation circuit and the first stage of OTA1 differ in their bulk potential. Hence, the current source properties of the nMOS devices in OTA1 differ from that of the nMOS device in the bias circuit. The bias signals V_{bp} and V_{bm} in the second stage of OTA1 are used for compensating the input current in OTA1.

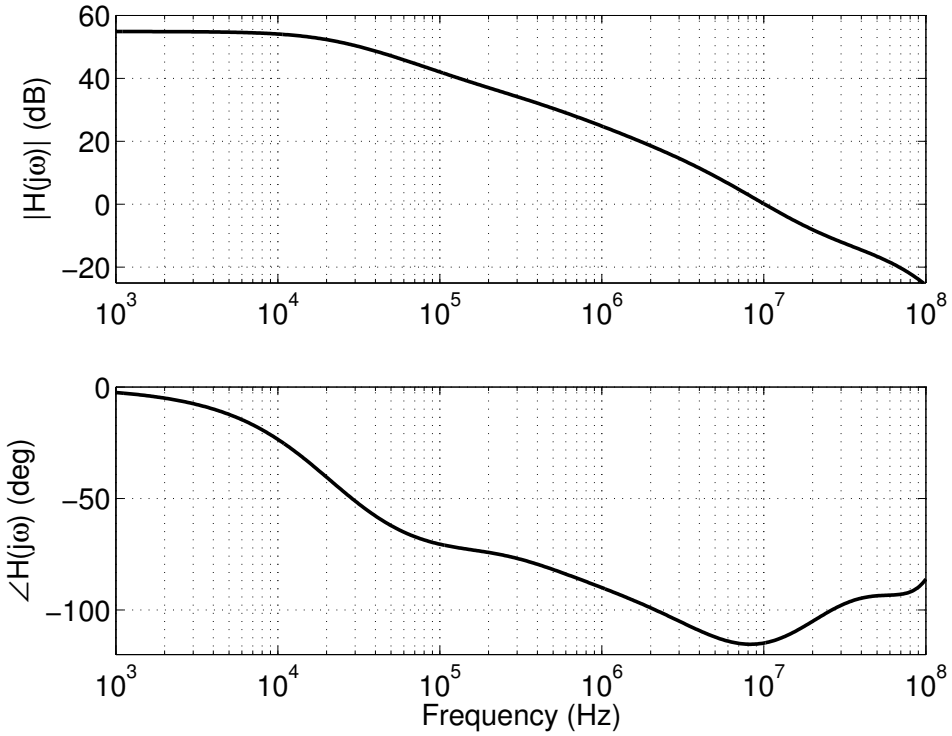


Figure 5.4: Open loop differential magnitude and phase response of OTA1 for the 'tt' process corner at 70°C.

The open loop differential magnitude and phase response of OTA1 with a series differential load of 147 pF capacitance and 5.25 kΩ resistance, is shown in Fig. 5.4. The open loop common mode frequency response with the same load as for the differential circuit is shown in Fig. 5.5. The bias signals V_{bp} and V_{bm} are replaced by V_b while calculating open loop frequency response. The characteristics of OTA1 over different process corners at 70°C are tabulated in Table. 5.1.

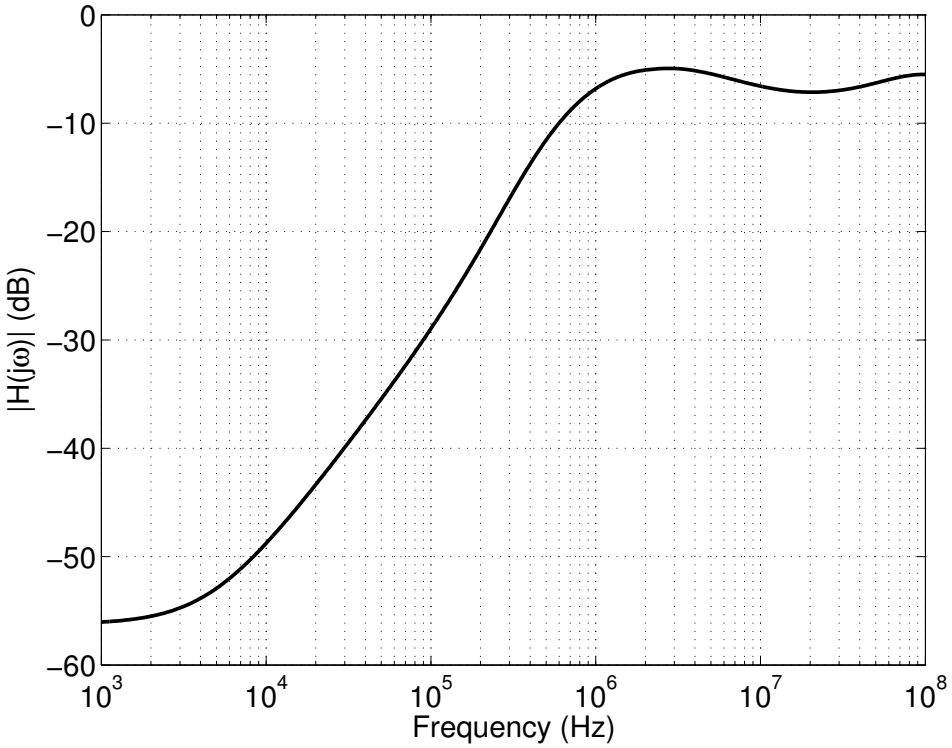


Figure 5.5: Open loop common mode magnitude response of OTA1 for the 'tt' process corner at 70°C.

Table 5.1: Characteristics of OTA1.

Process	ss	tt	ff
Output DC voltage (V)	0.249	0.249	0.249
DC gain (dB)	57.0	54.9	53.3
Phase Margin (degrees)	63.8	65.4	66.9
Bandwidth (MHz)	10.0	10.2	10.5
Power (μW)	129.3	130.5	132.4
Integ. Inp. ref. RMS noise (50 Hz - 24 kHz) μV	3.58	3.79	3.94

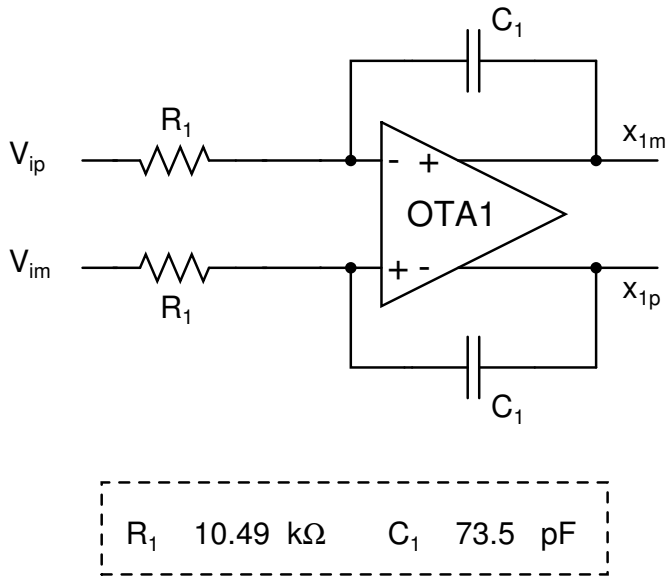


Figure 5.6: Circuit diagram showing the input signal path in the first integrator.

5.2.2 Current Compensation in OTA1

The resistance in the path of the input signal of the modulator is nominally 10 kΩ. as shown in Fig. 5.6. When a sine wave of amplitude 0.6 V peak to peak differential (MSA for the modulator) is applied across V_{ip} and V_{im}, the maximum current supplied by OTA1 is 15 μA for the input signal. So, the biasing current in the second stage of OTA1 has to be more than 15 μA. If the current sources in the second stage of OTA1 can be modulated as per the input signal by enhancing their current capacity when more current is needed of the OTA, the swing of the virtual ground nodes will be reduced resulting in improved linearity.

Fig. 5.7 shows a bias generation technique where a bias voltage V_{bp} is varied by the feedback loop as the input V_{ip} is changed. So, any change in current through resistor R_{gm} is compensated by the change in current through nMOS transistor M3. Such a current compensation technique is implemented in OTA1 by using bias signals V_{bp} and V_{bm} as shown in Fig. 5.3 and which in turn are generated according to the input signals as shown in Fig. 5.7 (V_{im} is used for generating V_{bm}).

The input signal has a bandwdith of 24 kHz, so speed requirement of V_{bp} and

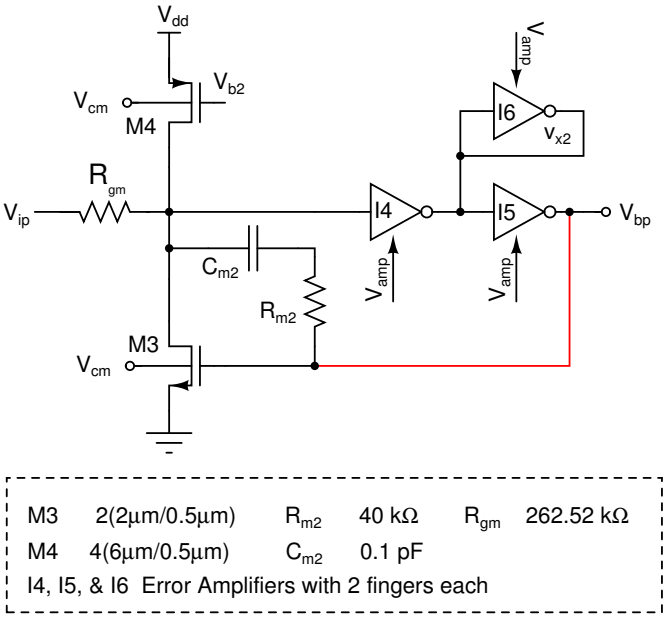


Figure 5.7: Bias generation circuit for V_{bp}.

V_{bm} generation circuit is less. The feedback DAC signal in the modulator can have a maximum frequency component of 6.144 MHz. So, if the feedback DAC current in the first integrator is to be compensated by a similar technique, the bias generation loop has to be fast enough.

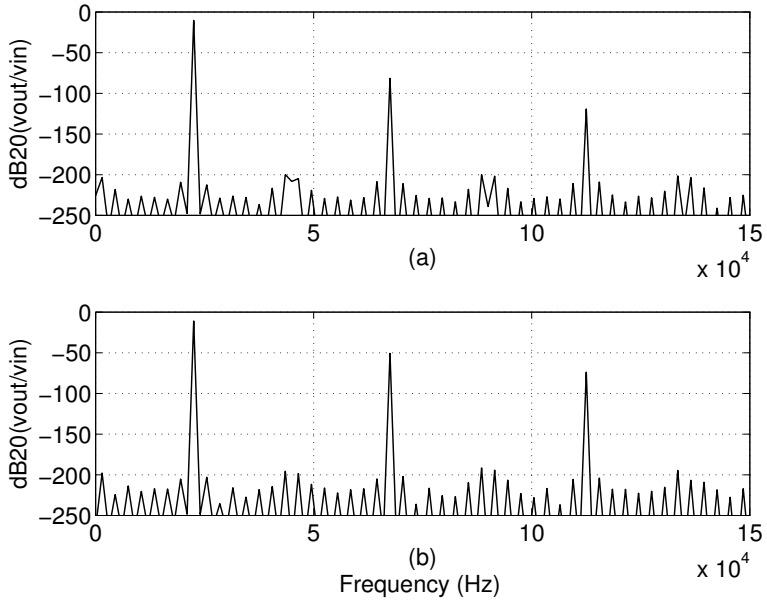


Figure 5.8: 4096 points FFT of the output of OTA1 connected in resistive feedback with (a) OTA1 compensated for input current and (b) OTA1 not compensated for input current.

The effectiveness of such a current compensation technique is proved in Fig. 5.8. Here, OTA1 is used in resistive feedback with a gain of half at the output and an input resistance of 10.5 kΩ. A 22.5 kHz sine wave of amplitude 0.6 V (peak to peak differential) is applied at the input. Fig. 5.8(a) & (b) show 4096 points FFT of the output of OTA1 with and without current compensation respectively. The third harmonic distortion in Fig. 5.8(a) is 31 dB lesser than the third harmonic distortion in Fig. 5.8(b).

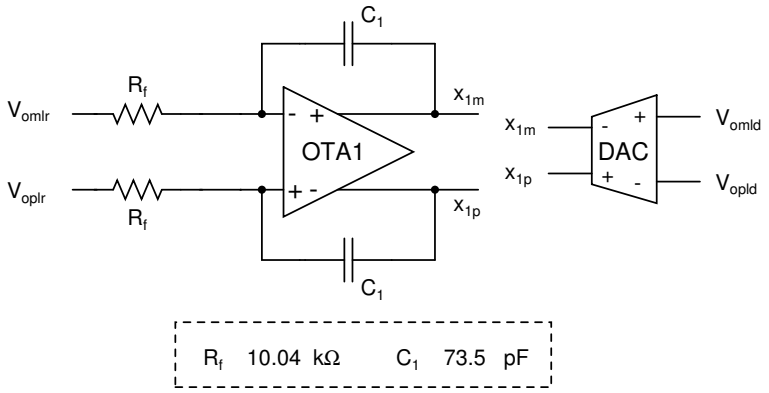
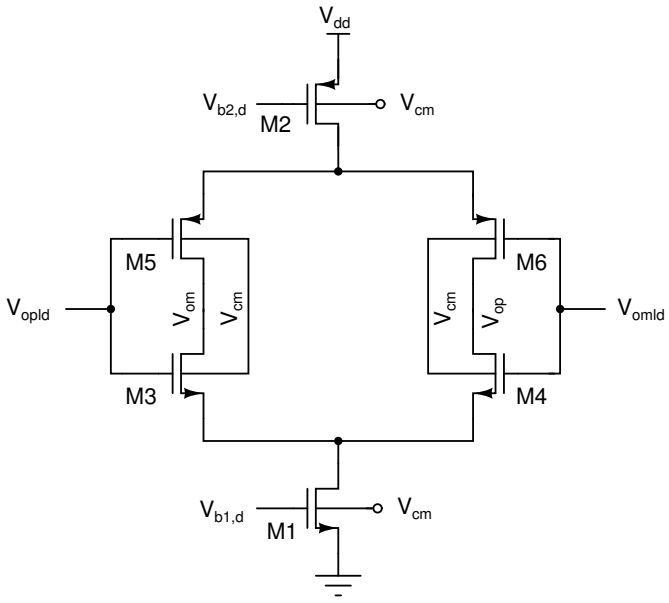


Figure 5.9: Compensation of feedback signal current using current steering DAC at the output.

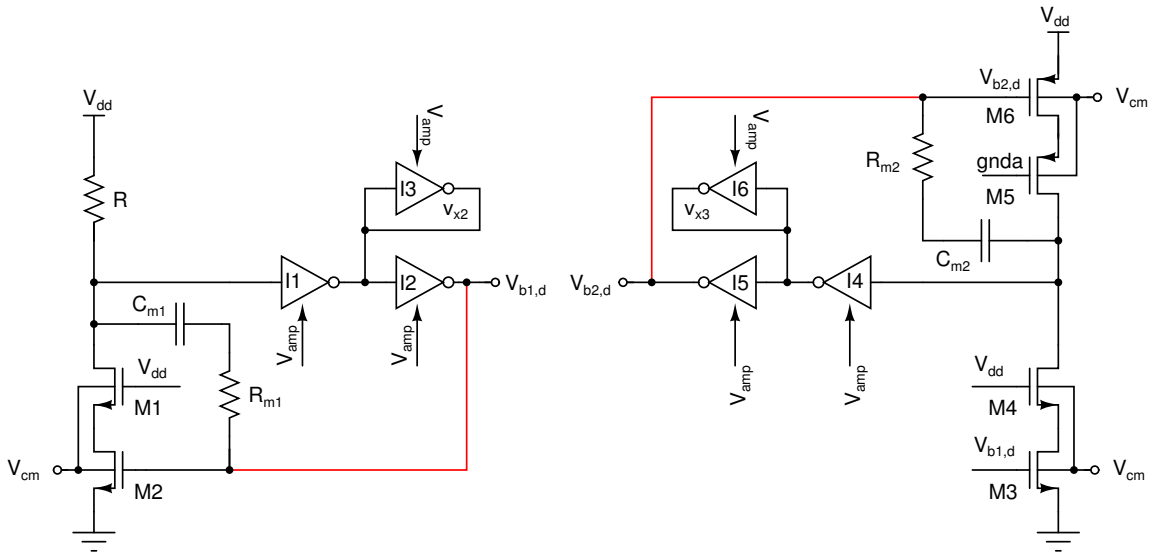
Resistance used for negative feedback (R_f) in the modulator is nominally 10 kΩ. As the feedback signal swings between supply voltages [0,0.5] V, the current going into OTA1 is ±25 μA. In case this current is drained out from the output terminals of OTA1, the current supplied by OTA1 will be nominally zero and the non-linearities contributed by OTA1 will be reduced. Such current injection is possible at the output of OTA1 as shown in Fig. 5.9, using a current steering DAC shown in Fig. 5.10.

The length of current sources M1 and M2 is chosen to be 0.5 μm to reduce mismatch. The length of switching MOSFETs M3, M4, M5 and M6 is chosen to be 0.18 μm to reduce the capacitance switched every clock cycle. The switch size can be reduced by applying the DAC control signal V_{opld} (V_{omld}) to the bulk terminals also. However, as the switching signals are 0 and 0.5 V, the variation in bulk current will alter the current supplied by the DAC. It will also put an extra burden on the circuit driving this DAC.



M1	8(8.25µm/0.5µm)	M3, M4	8(5µm/0.18µm)
M2	32(12µm/0.5µm)	M5, M6	32(5µm/0.18µm)

Figure 5.10: Current Steering DAC.

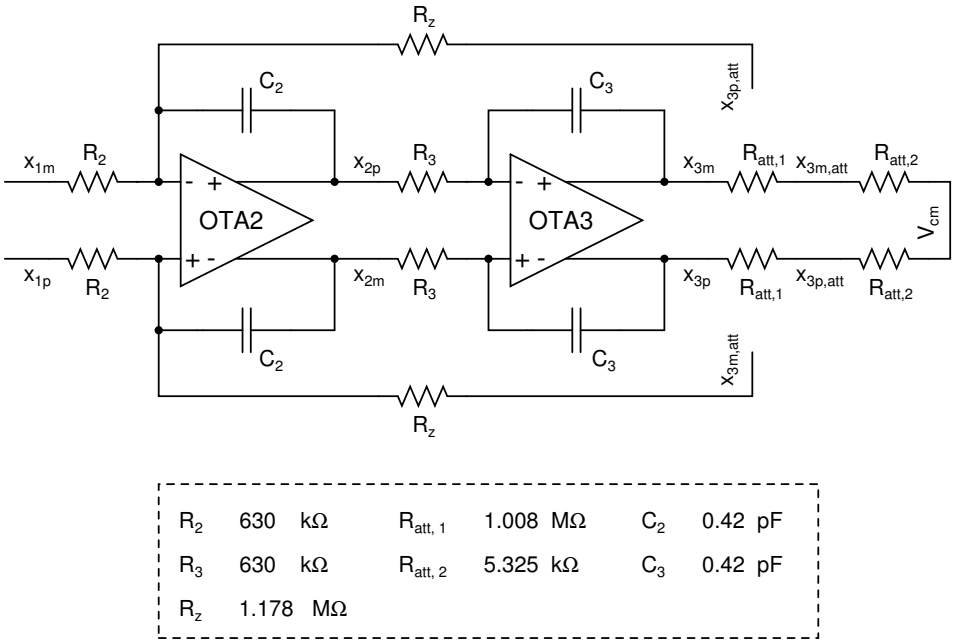


M1, M4	2(5µm/0.18µm)	M6	8(12µm/0.5µm)	R_{m2}	14 kΩ
M2, M3	2(8.25µm/0.5µm)	R	41.56 kΩ	C_{m1}	1 pF
M5	8(5µm/0.18µm)	R_{m1}	15 kΩ	C_{m2}	1 pF

I1, I2, I3, I4, I5 & I6 Error Amplifiers with 2 fingers each

Figure 5.11: Biasing circuit for current steering DAC.

M1 and M2 in the DAC are biased for fixed current using the current biasing circuit shown in Fig. 5.11. The resistor R in Fig. 5.11 tracks the feedback current through R_f in Fig. 5.2. In the DAC biasing circuit, the biasing voltage V_{amp} is separately generated to avoid any feed-through to the rest of the modulator circuit because of high switching in the DAC.



R_2	630	kΩ	$R_{att,1}$	1.008	MΩ	C_2	0.42 pF
R_3	630	kΩ	$R_{att,2}$	5.325	kΩ	C_3	0.42 pF
R_z	1.178	MΩ					

Figure 5.12: Circuit diagram of second and third integrator.

5.3 Second and Third Integrators

The circuit diagrams of the second and third integrators are shown in Fig. 5.12. Large valued integrating resistors are used to reduce the current supplied by OTA2 and OTA3. The bulk-input OTA2 and OTA3 have exactly the same design specifications as specified for the bulk-input OTA in Fig. 4.2. The nominal frequency of the optimized zeros in the modulator is 18 kHz and is implemented by using resistor R_z. If this zero is implemented with the direct outputs of the third integrator (x_{3p} and x_{3m}), the value of R_z will be very high. Here, the output of the third integrator is attenuated using $R_{att,1}$ and $R_{att,2}$ to reduce the value of R_z.

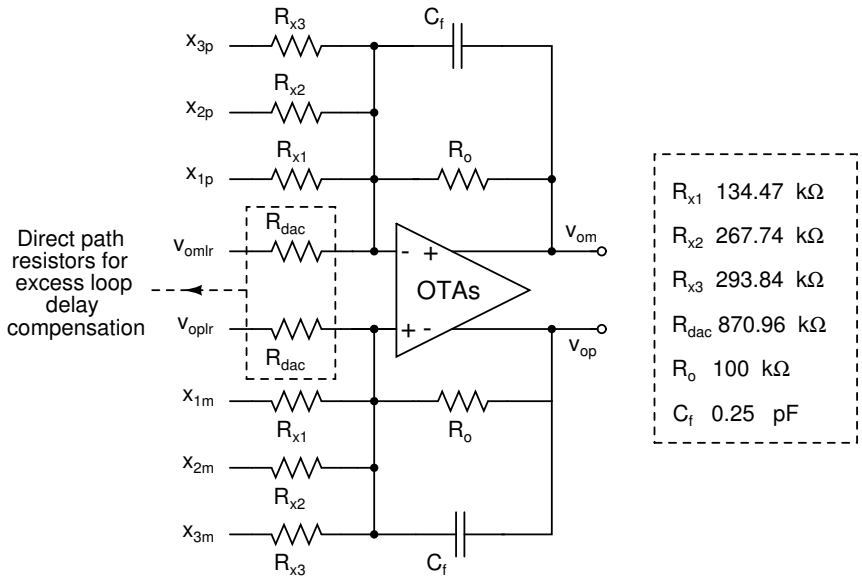


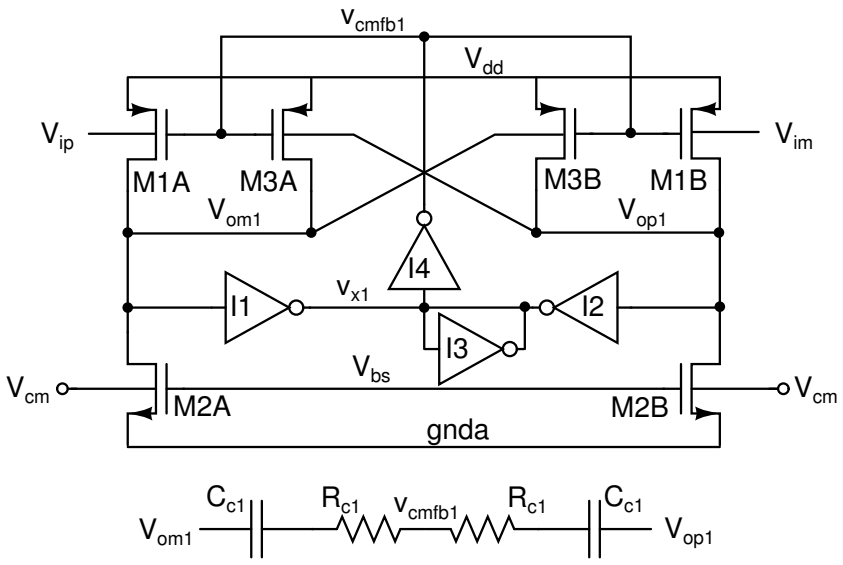
Figure 5.13: Circuit diagram of a summer block.

5.4 Summing Amplifier

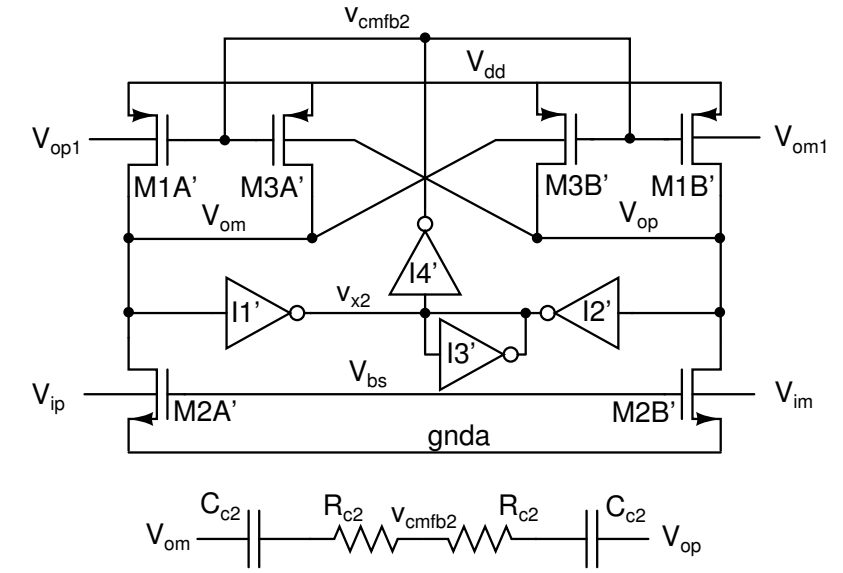
The summing amplifier in the modulator consists of a bulk-input OTA (OTAs) and resistors R_o, R_{x1}, R_{x2}, R_{x3} and R_{dac} to implement the summing coefficients k_0, k_1, k_2 and k_3. The circuit diagram of the summer is shown in Fig. 5.13. For single-bit CTDSMs, only the sign of the output (differential output) of the summer block is significant to decide the output of the modulator, so all the input resistors can be scaled to higher values to reduce the current supplied by opamps in the three integrators. However, high values of these resistors will reduce the pole frequency at the input of OTAs. High swing at the output of summing amplifier can be achieved by increasing R_o and it will facilitate the comparator for accurate and faster comparison.

The circuit diagram of OTAs is shown in Fig. 5.14. Bias voltage (V_{bs}) for current sources M2A, M2B, M2A' and M2B', is generated using the circuit shown in Fig. 5.15.

The length of the MOSFETs in OTAs is chosen to be $0.36\,\mu$m to increase the phase margin for the OTA by reducing capacitance in the circuit. An extra capacitance of 0.25 pF is added across the feedback resistor R_o to increase the



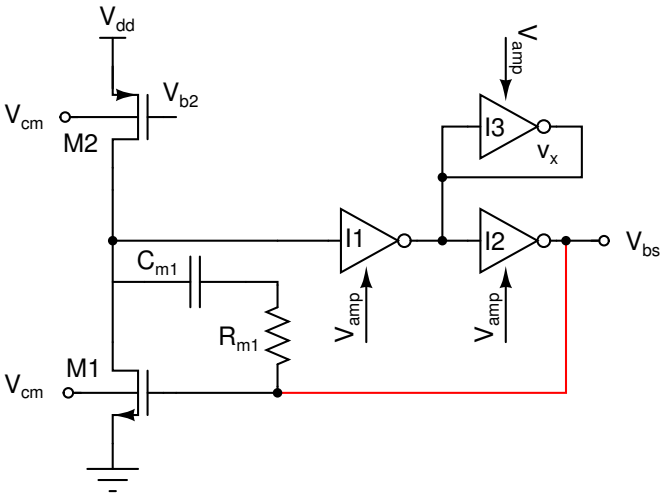
First stage



Second stage

M1A, M1B	36(5µm/0.36µm)	M1A', M1B'	72(5µm/0.36µm)
M2A, M2B	20(2µm/0.36µm)	M2A', M2B'	40(2µm/0.36µm)
M3A, M3B	4(5µm/0.36µm)	M3A', M3B'	8(5µm/0.36µm)
R_{c1}	4.17 kΩ	R_{c1}	2.0 kΩ
C_{c1}	0.35 pF	C_{c1}	0.6 pF
I1, I2, I3, I4, I1', I2', I3', I4'	Error Amplifiers with two fingers each		

Figure 5.14: Circuit diagram of a summing amplifier (OTAs).

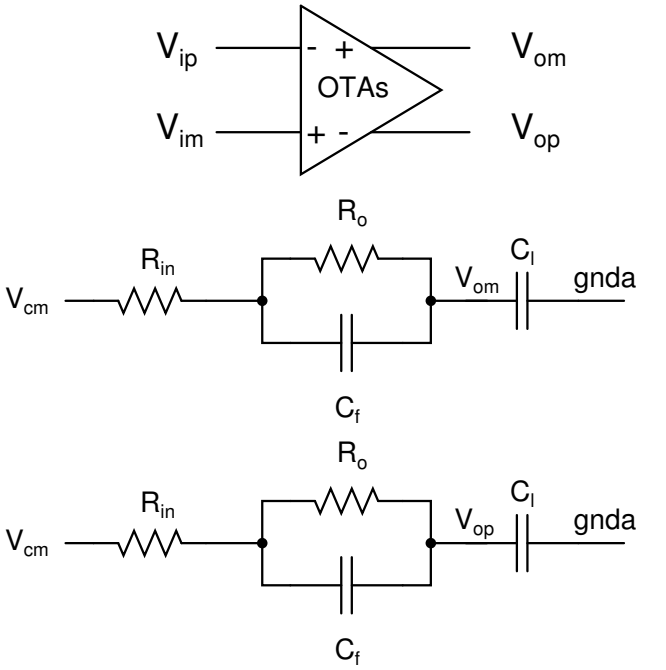


M1	2(2µm/0.36µm)	R_{m1}	40 kΩ
M2	4(6µm/0.5µm)	C_{m1}	0.1 pF

I1, I2, & I3 Error Amplifiers with 2 fingers each

Figure 5.15: Bias generation circuit for OTAs.

phase margin and improve pulse response of OTAs.



R_{in}	63.6 kΩ	R_o	100 kΩ	C_l, C_f	0.25 pF

Figure 5.16: Circuit used for testing AC response of the OTAs. Load impedance for OTAs is same as in case of the modulator.

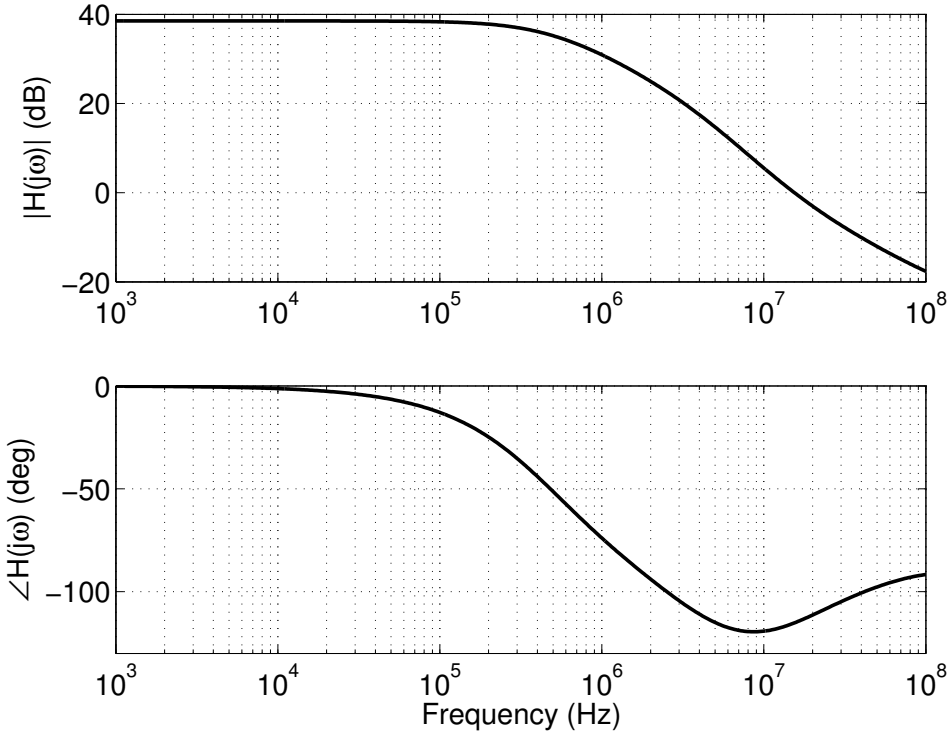


Figure 5.17: Magnitude and phase response of OTAs.

The magnitude and phase response of OTAs are shown in Fig. 5.17 for the load as shown in Fig. 5.16. The characterisitcs of OTAs have been tabulated for process corners at 70°C in Table. 5.2.

Table 5.2: Characteristics of OTAs.

Process	ss	tt	ff
Output dc voltage (V)	0.249	0.249	0.249
DC gain (dB)	40.76	38.52	36.87
Phase Margin (degrees)	65.7	65.9	66.0
Bandwidth (MHz)	15.32	15.5	15.65
Power (μW)	59.7	60.4	61.6
Input ref. noise @10 kHz (nV/$\sqrt{}$Hz)	60.18	60.70	61.66
Input ref. noise @1 MHz (nV/$\sqrt{}$Hz)	54.42	54.59	54.85

The bandwidth of OTAs has to be large enough to respond to high frequency signals (6.144 MHz signal in this modulator) in the direct path from the output of the modulator through R_{dac} for delay compensation in the modulator. The pulse response of OTAs for 1 V peak to peak differential input at R_{dac} terminals in Fig. 5.13 with all other input terminals connected to V_{cm}, is shown in Fig. 5.18.

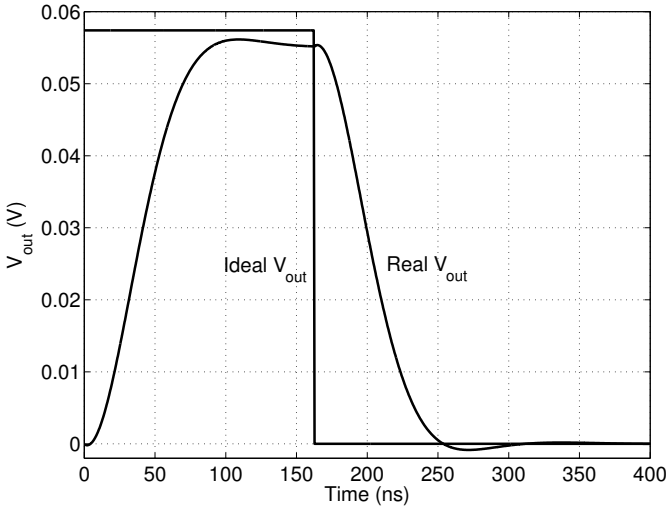


Figure 5.18: Pulse response of OTAs for the 'tt' process corner at 70°C.

5.5 Latched Comparator

A conventional way to decide the sign of the output of the loop filter is to sample the output using MOS switches and then to regenerate the sampled output using inverters connected in positive feedback. Sampling is not possible with a reasonable switch size when the output signal rides over $V_{cm} = 0.25\,V$ and threshold voltages for MOSFETs are in range $[0.25,0.50]\,V$ for different process corners and temperature.

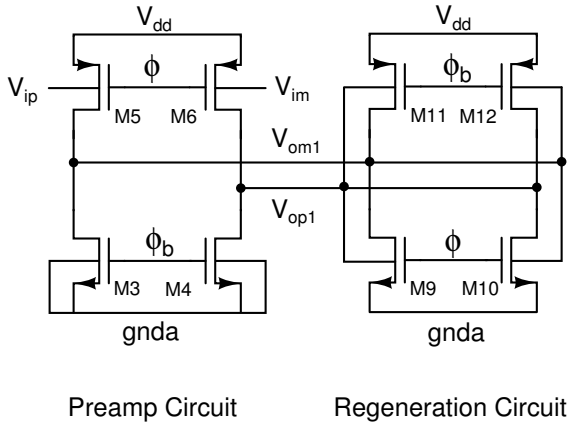
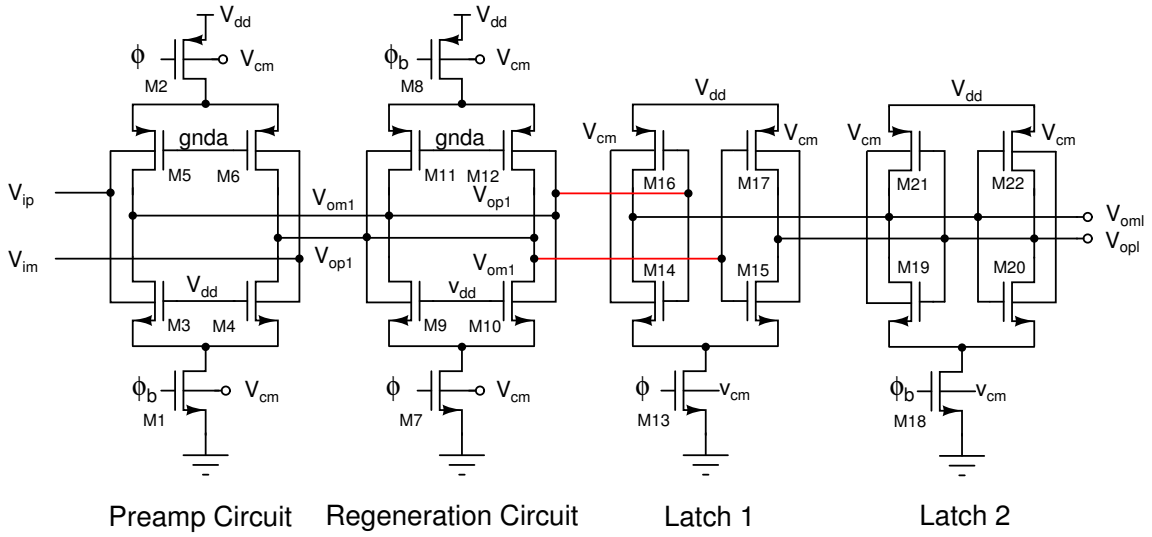


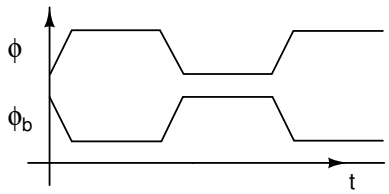
Figure 5.19: Circuit diagram of a latched comparator in [8]. ϕ and ϕ_b are non-overlapping clocks.

An alternate way of sampling the output of the summer block and then regenerating this signal is shown in Fig. 5.19. Here, the input is sampled by clocking

both the pMOS and nMOS devices connected between the supply voltages and applying the input to the bulk terminals of the pMOS transistors. Such a technique leads to a large charge injection through the bulk and drain terminals during switching. Due to the excessive loading, it distorts the summer block output and changes the sampled signals which will be regenerated later.

Authors in [8] used the regeneration circuit shown in Fig. 5.19. Unlike the regeneration in a CMOS latch (with positive feedback between the gate and drain terminals), here, the positive feedback between the bulk and drain terminals is not strong enough to switch OFF either of the MOSFETs in the inverters by driving V_{ds} to zero in regeneration phase. Even a 50 mV drop across the MOSFETs allow a large steady state current to flow. It leads to a large power dissipation which varies by nearly four times over process variations.





M1	8(0.6µm/0.18µm)	M7	20(9µm/0.18µm)
M2	8(2.0µm/0.18µm)	M8	20(19µm/0.18µm)
M3, M4	4(4.4µm/0.18µm)	M9, M10	4(9µm/0.18µm)
M5, M6	4(9.7µm/0.18µm)	M11, M12	4(19µm/0.18µm)
M13	4(20µm/0.18µm)	M18	2(20µm/0.18µm)
M14, M15	2(20µm/0.18µm)	M19, M20	1(20µm/0.18µm)
M16, M17	2(20µm/0.18µm)	M21, M22	1(20µm/0.18µm)

Figure 5.20: Circuit diagram of a latched comparator. ϕ and ϕ_b are non-overlapping clocks.

The effect of charge injection during switching can be reduced by clocking the current sources in a comparator like M1 and M2 as shown in Fig. 5.20 rather than the input MOSFETs like M3, M4, M5 and M6. Using the switched current sources in the regeneration circuit helps in limiting the steady state current.

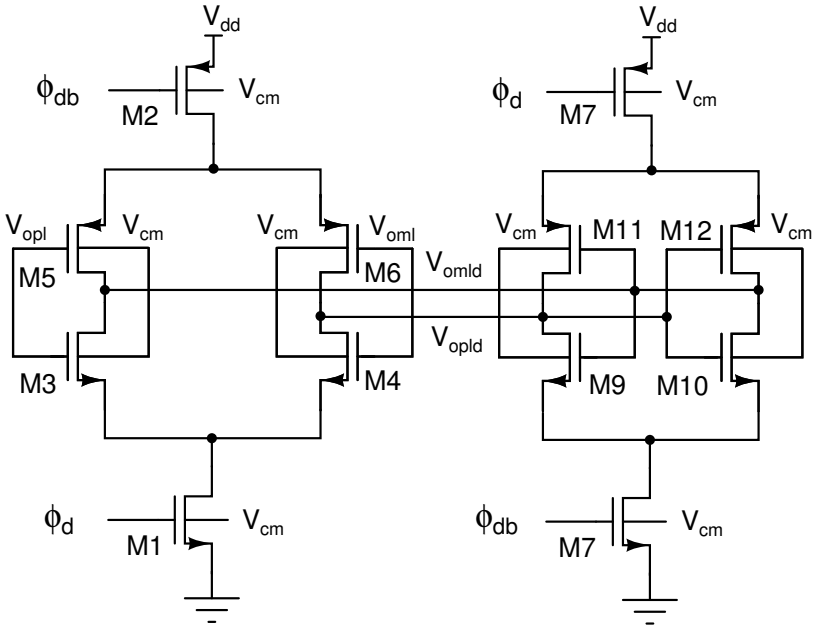
The regenerated signal is sampled and held over one clock cycle, using Latch 1 and Latch 2 as shown in Fig. 5.20. Latch 1 isolates the output V_{opl} from the Preamp output V_{op1} during sampling phase.

5.6 Feedback Latch

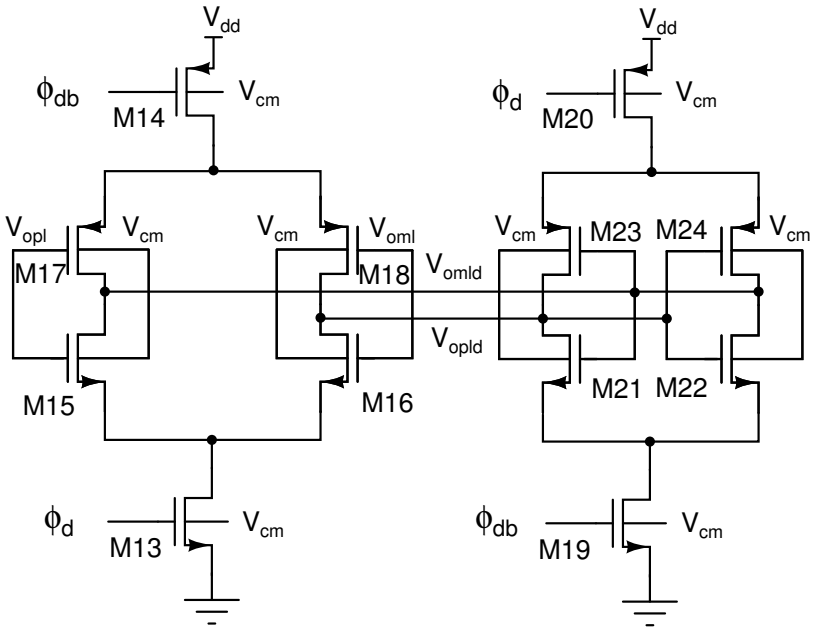
As discussed in Sec. 5.2, the modulator uses a resistive feedback DAC, and a current steering DAC injects current into the output of the first integrator. Hence, the feedback signal from the output of the modulator should be able drive a 10 kΩ resistor, as well as the input capacitance of a current steering DAC carrying a nominal current of 25 μA. Latch 3 and Latch 4 as shown in Fig. 5.21 are used to provide control signals for the current steering and resistive DACs respectively. The voltage drop across the current sources in Latch 4 is compensated by changing the feedback resistor (R_f) value in the first integrator. A large voltage drop across the current sources will cause a large variation in current over process corners. The sizes of the MOSFETs in Latch 4 are determined so that they have a maximum voltage drop of 20 mV across the current sources and switches over process variations. The MOSFETs in Latch 3 are sized to have a similar clock to output delay as Latch 4. Latch 3 and Latch 4 are clocked with delayed clocks ϕ_d and ϕ_{db} where the delay is decided by the delay in regeneration phase.

5.7 Clock Generation

Delayed clocks are required in the modulator to ensure that the output of the comparator has been fully regenerated before it is applied to the feedback DAC.



Latch 3



Latch 4

M1, M7	6(10µm/0.18µm)	M3, M4, M9, M10	6(11µm/0.18µm)
M2, M8	6(20µm/0.18µm)	M5, M6, M11, M12	6(21µm/0.18µm)
M13, M19	10(10µm/0.18µm)	M15, M16, M21, M22	12(11µm/0.18µm)
M14, M20	10(20µm/0.18µm)	M17, M18, M23, M24	12(21µm/0.18µm)

Figure 5.21: Circuit diagram of feedback latch. ϕ_d and ϕ_{db} are non-overlapping delayed version of clock ϕ.

For 0.5 V supply voltage, the delay through an inverter exhibits significant variation over process and temeprature. Generating a delayed clock using a chain of inverters largely does not seem robust with process and temperature. Our simulations show that a delay implemented by a simple chain of inverters can even become smaller than the regeneration time of the latch. Variations in the delay implemented by a chain of inverters can be reduced if the current during switching can be tracked over process. Such a delay has been realized using current starved inverters as shown in Fig. 5.22, where these current sources are biased using circuit in Fig. 5.23, for fixed current over process and temperature.

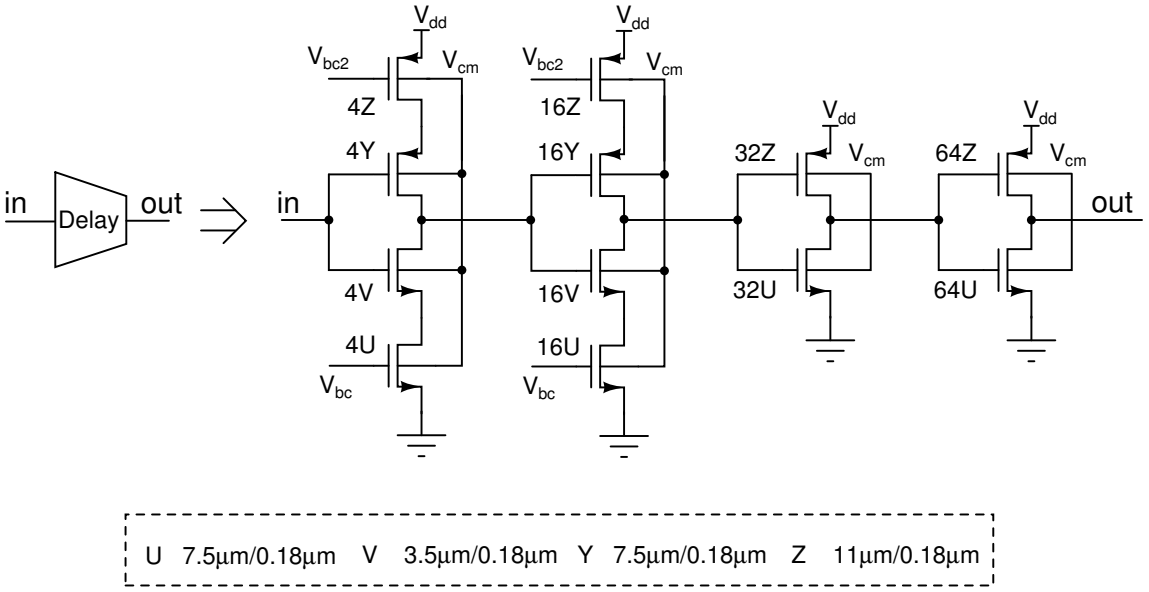


Figure 5.22: Delay element in a clock generation circuit.

Clocks ϕ, ϕ_b, ϕ_d and ϕ_{db} are generated from the input clock 'clk' as shown in Fig. 5.24 using the delay element shown in Fig. 5.22.

Here, most of the delay is contributed by the first two inverters. Last two inverters are used to drive a large load. Large sizes of the first inverters in generation of ϕ_b and ϕ_{db} are chosen as compared to ϕ and ϕ_d, to reduce the overlapping region between ϕ and ϕ_b (ϕ_d and ϕ_{db}) over process.

The variation of delay (Δ_{td}: difference between the rising edge of ϕ and ϕ_d) implemented in Fig. 5.24, is tabulated in Table. 5.4 for different process and tem-

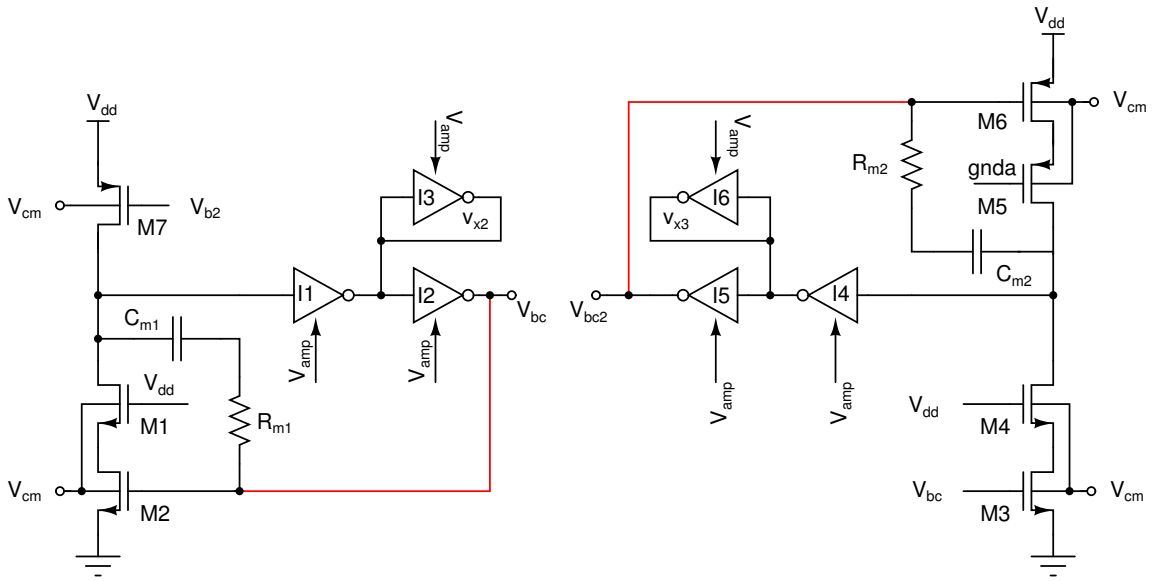


Figure 5.23: Bias generation circuit for clock.

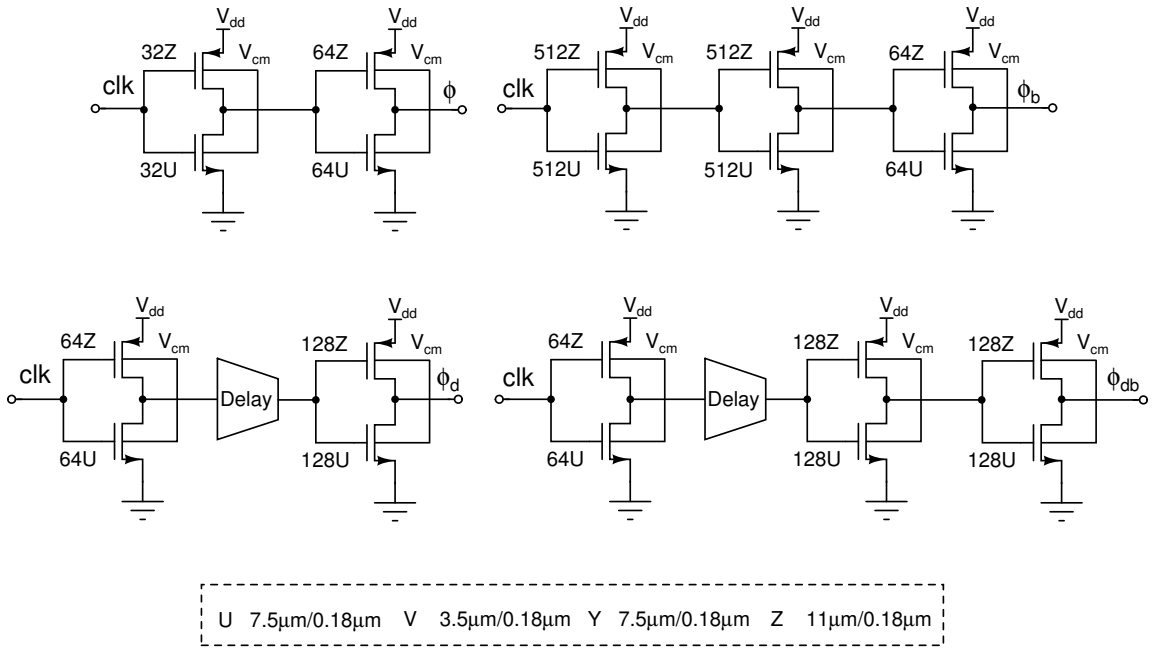


Figure 5.24: Clock generation circuit.

peratures.

Table 5.3: Delay (Δ_{td})

Process	ss	ff
0 °C	68 ns	52 ns
25 °C	62 ns	50 ns
70 °C	54 ns	46 ns

5.8 Noise and SNR calculation

Thermal noise at the input of the modulator is mainly contributed by the thermal noise of the input resistors of the first integrator ($V_{n,R1}$ and $V_{n,Rf}$) and the input referred noise of the first OTA ($V_{n,OTA1}$). The input referred thermal noise of the resistors within the signal bandwidth (24 kHz) is given by

$$\begin{aligned} V_{n1} &= V_{n,R1} + V_{n,Rf} \\ &= 8kT(R_1 + R_f) \times 24\,\text{kHz} \end{aligned} \tag{5.1}$$

At 70°C, $V_{n1,rms} = 4.32\,\mu V$. Maximum input referred thermal noise of OTA1 as given in Table. 5.1, is for the 'ff' process corner and $V_{n,OTA1,rms} = 3.94\,\mu V$. If thermal noise dominates over the quantization noise for the modulator, SNR for the modulator is given by

$$\text{SNR} = 10\log[\frac{V_{in,rms}^2}{V_{n1,rms}^2 + V_{n,OTA1,rms}^2}] \tag{5.2}$$

where $V_{in,rms}$ is the input RMS voltage. For 0.3 V peak to peak differential MSA, SNR from eq. (5.2) is found to be 91 dB.

5.9 Simulation Results

The 0.5 V single bit continuous time $\Delta\Sigma$ modulator has been impelmented in 180 nm technology with the design specifications of different parts as discussed above. Power spectral density of the output of the modulator with a 0.6 V peak to peak differential sine wave input voltage (in the third bin for 4096 points FFT) for extracted view of the modulator is shown in Fig. 5.25. In band PSD is shown in Fig. 5.26.

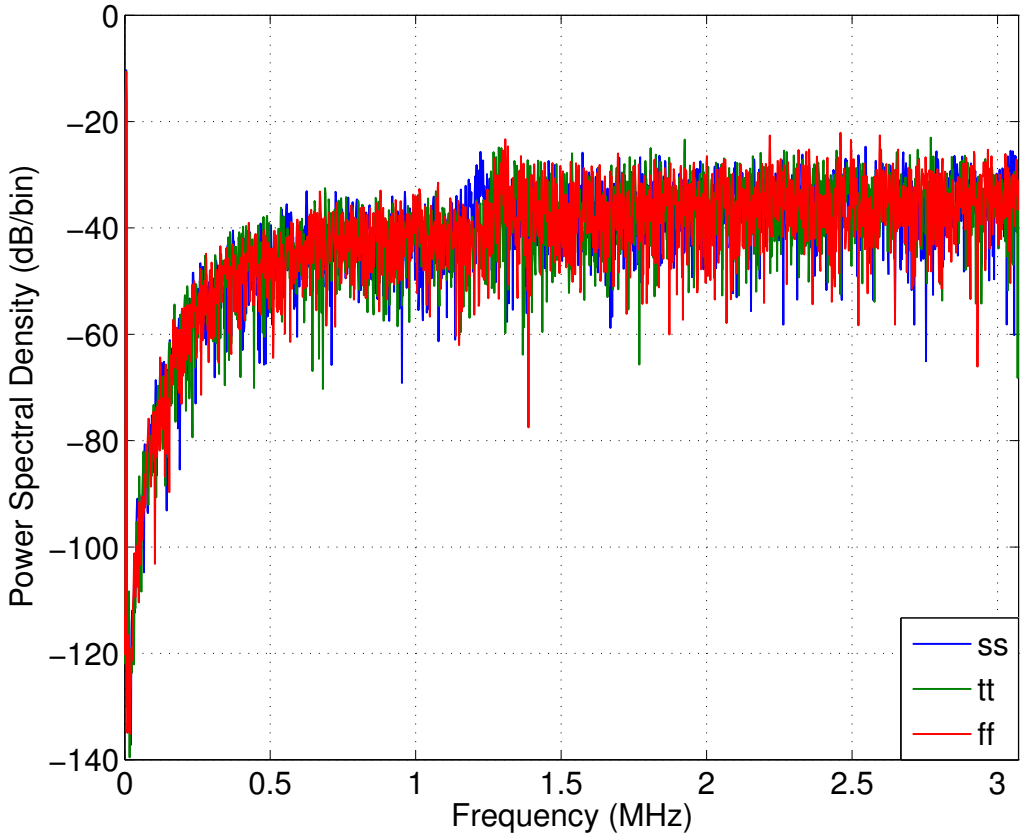


Figure 5.25: Power Spectral Density of the modulator output.

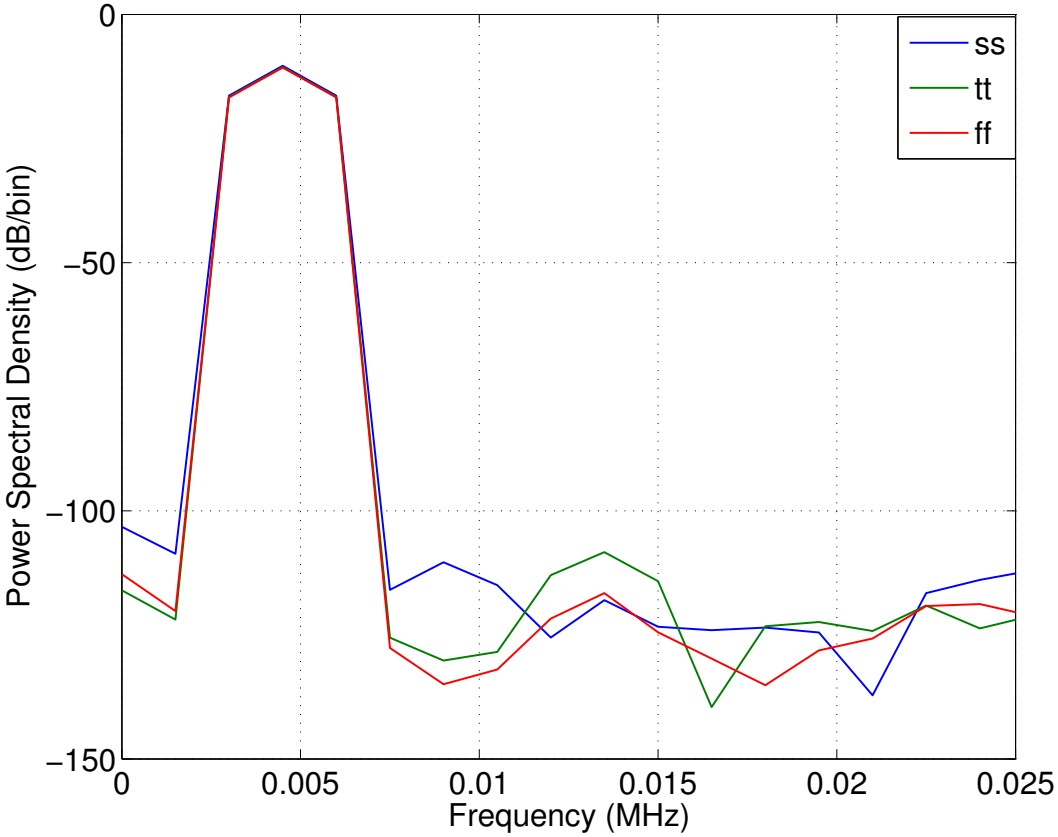


Figure 5.26: In band Power Spectral Density of the modulator output.

Table 5.4: Modulator Performance Summary at 25 °C

Modulator type	1-bit, 3^{rd} order, continuous time
Signal bandwidth	24 kHz (50Hz-24kHz)
Sampling frequency / OSR	6.144 MHz/128
Difference input signal voltage range	0.6 $V_{pp,diff}$
Supply Voltage	0.5 V
SNR @ Vin=0.6 $V_{pp,diff}$	97 dB (ss), 96 dB (tt), 103 dB (ff)
Power Consumption (total) Sigma Delta Modulator (filter + comparator + DAC + clock)	310 μW (ss), 372 μW (tt), 498 μW (ff)
Active die area	0.65 mm^2
Technology	0.18 μm CMOS (standard VT, triple-well NMOS, MIM capacitors, and RNHR1000MM resistors

CHAPTER 6

Automatic Tuning of Time Constants in Single Bit Continuous-Time Delta-Sigma Modulators

6.1 Introduction

Continuous-time Delta-sigma Modulators (CTDSM), as alternatives to their discrete-time counterparts, have been receiving much attention lately due their ineherent anti-aliasing properties and low power dissipation. In such modulators, the loop filter is realized using contiunous-time circuitry (typically using active-RC or Gm-C techniques) as shown in Fig. 6.1.

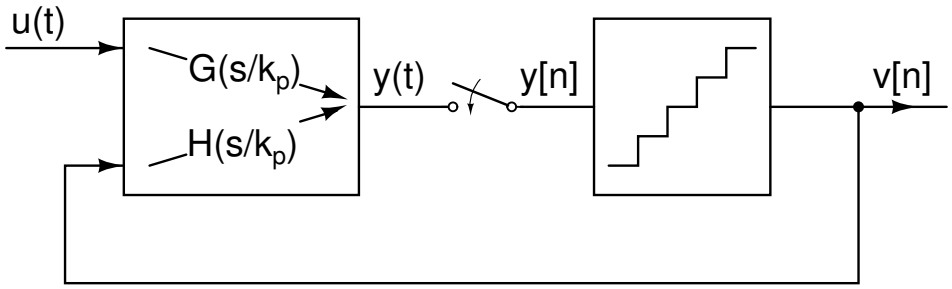


Figure 6.1: Block diagram of continuous-time $\Delta\Sigma$ modulator.

A practical problem with CTDSMs is the change in the loop NTF due to systematic variations of the loop filter time constants with process and temperature spreads. Systematic variations in the loop filter time constants can be modelled by the frequency scaling parameter k_p, where $k_p = 1$ for the nominal process corner. If $k_p > 1$, the MSA for the modulator decreases. For k_p significantly larger than unity, the loop can become unstable. A k_p smaller than unity results in an increased in-band quantization noise. It is thus seen that some kind of time-constant tuning system is necessary to realize CTDSM whose performance remains robust

with process and temperature variations. Most work on time-constant tuning in CTDSMs has heavily borrowed from the tuning literature of continuous-time filters. Here, the basic idea is to infer k_p from the replica oscillator (or integrator) and use this information to apply the appropriate correction to the loop filter of CTDSM [11], [12]. Some works have attempted to infer the value of k_p from the properties of the quantization noise during the loop operation. This is an example of direct tuning - where the filter to be tuned is measured in-situ. An advantage of these methods over replica based schemes is the saving of active area. In [13], the authors measure the variance of the in-band quantization noise *after decimation* to infer the value of k_p.

A similar idea is used in [14] to tune RC time constants in a cascaded modulator. The technique of [15] determines k_p by measuring the variance of the highpassed output sequence of a multibit modulator. In that work, the authors observed that the dependence of in-band and out-of-band gain of an NTF can be exploited to infer the bandwidth scaling factor of the loop filter. Through simulations, the efficacy of the technique was shown for a third order four-bit modulator. Since the approach used the additive white noise approximation for the quantizer (valid only for a multilevel quantizer), it was not effective in a single bit design, as pointed out in [15].

While a multi-bit modulator has many advantages over a single bit design, the latter is attractive in several aspects. The inherent linearity of the single bit feedback DAC eliminates the need for Dynamic Element Matching (DEM) circuitry that would be needed in multibit design. At high sampling rates, the DEM block can be power hungry, apart from introducing a significant delay in the loop. For modulators operating at low speeds (for example, those designed for audio applications), a single bit modulator can be significantly smaller due to the reduced size of the feedback DAC. A new automatic time-constant tuning technique for single bit CTDSMs has been proposed and discussed in detail in the following sections.

6.2 In-Situ Time-Constant Estimation In CTDSMs

To better explain the technique proposed here, we first review the time-constant estimation scheme of [15], which is based on the following observation. If $k_p > 1$ (the loop filter bandwidth increases), the in-band quantization noise reduces. This means that the out-of-band gain of the NTF must increase (as per the Bode Sensitivity Integral, as applied to discrete-time linear systems [16]), implying an increased gain for quantization noise at higher frequencies, when compared to nominal NTF. The opposite phenomenon occurs when the loop filter becomes slower. Thus, the deviation of k_p from unity can be estimated by comparing the variance of quantization noise in the modulator output sequence $v[n]$, as shown in Fig. 6.2.

The output consists of the desired in-band signal in addition to the shaped quantization noise - so measuring the variance of the first difference of $v[n]$ should largely eliminate the in-band signal, and should be an indicator of k_p. Defining $p[n] = v[n]$ - $v[n-1]$, assuming a linear model for the modulator, and denoting the step size of the quantizer by Δ, the variance of $p[n]$ is given by eq. 6.1.

$$\sigma_p^2 = \frac{\Delta^2}{12\pi} \int_0^{\pi} |\mathrm{NTF}(e^{j\omega})(1 - e^{-j\omega})|^2 d\omega \tag{6.1}$$

Fig. 6.3 shows the normalized variation of σ_p with k_p for different NTF Out-of-band Gains (OBG). A third order CTDSM with 16-level quantizer was used. From the figure, it is seen that σ_p increases with k_p (as expected intutively) - however, the sensitivity to k_p reduces for small OBGs. Note specifically the very small variation in σ_p due to time-constant changes when the OBG = 1.5. The low sensitivity of σ_p for small OBGs is not an issue in multibit loops, since the NTFs of such modulators are designed to have large OBGs anyway. However, single bit modulators cannot be tuned in this manner, since the stability issue mandate that the OBG of such loops be restricted to around 1.5 [17]. When σ_p for a single bit

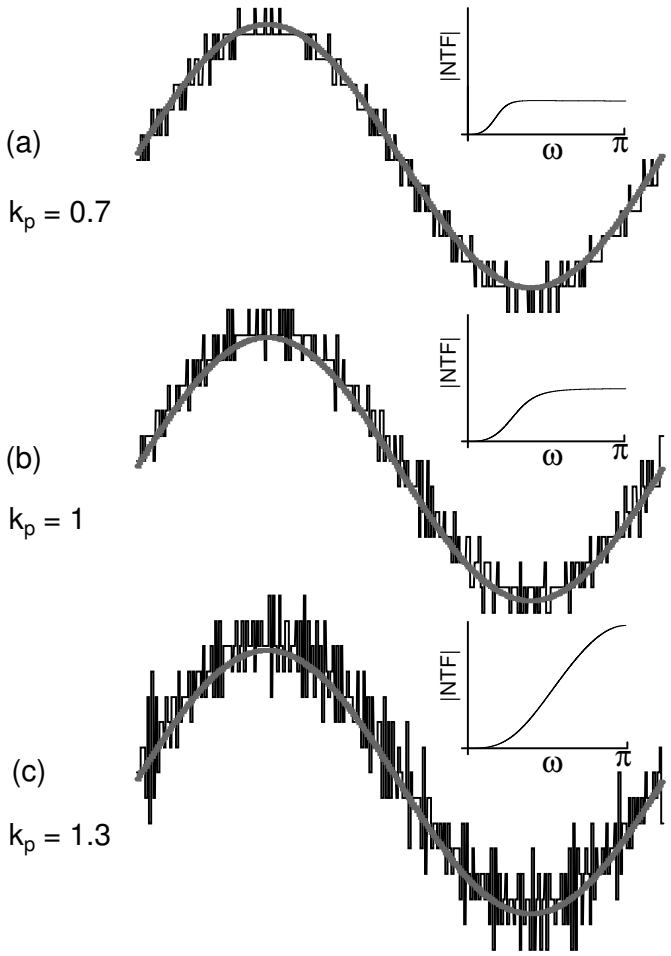


Figure 6.2: Time-domain output stream of a 4-bit CTDSM when - (a) Loop filter is slow, $k_p = 0.7$. The out-of-band gain of the NTF is smaller than the nominal value, and the modulator output "wiggles" less frequently than the nominal case. (b) Nominal Loop filter, $k_p = 1$. The out-of-band gain is 3. (c) Loop filter is fast, $k_p = 1.3$. Notice the significant increase in the out-of-band gain, resulting in more frequent, larger amplitude "wiggles" [15].

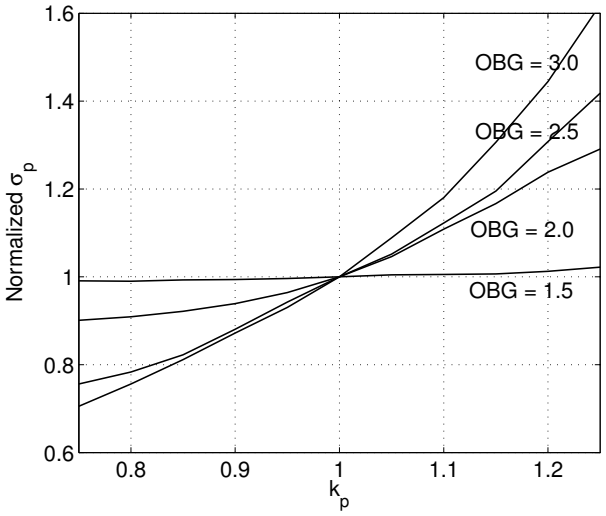


Figure 6.3: Normalized σ_p as a function of k_p (normalized to its value when $k_p = 1$).

modulator (obtained from time-domain simulations, not from eq. 6.1) was plotted as a function of k_p, it was found to *decrease slighlty* with k_p. This was attributed to quantizer saturation.

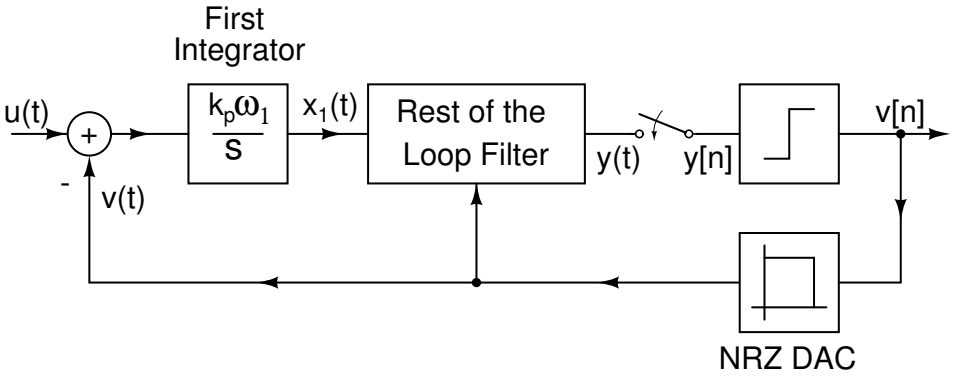


Figure 6.4: Block diagram of a CTDSM - the first integrator output is denoted by $x_1(t)$.

6.2.1 Proposed Technique

From the discussion above, it is seen that σ_p cannot be used as an indicator of k_p in single bit designs. This motivates for a new technique, which is explained in the context of high order modulator. Fig. 6.4 shows CTDSM with an NRZ feedback DAC. We focus on the output of the first integrator. Without loss of generality,

the sampling rate is assumed to be 1 Hz. Assuming that the modulator input is sufficiently slow and denoting the NRZ pulse shape by $p(t)$, the input to the first integrator can be written as in eq. 6.2

$$u(t) - v(t) \approx \sum_{k} (u[k] - v[k])p(t-k) \tag{6.2}$$

$u[k]$ - $v[k]$ represents the shaped quantization noise sequence and does not contain the input signal. For an n^{th} order modulator, the spectrum of this signal goes as ω^n around DC. The output of the first integrator in the loop filter, denoted by $x_1(t)$ is an integral of $u(t) - v(t)$. For the modulator orders greater than one, the DC value of $x_1(t)$ is zero, since it is the integral of the n^{th} shaped noise. The variance of $x_1(t)$ is an indicator of k_p, as explained with the help of Fig. 6.5. The figure shows the spectrum of $x_1 t$ for three values of k_p - 0.5, 1 and 1.5. When $k_p = 1$, the nominal NTF is realized and the variance of $x_1(t)$ is proportional to the shaded area in part (b) of the figure. When k_p reduces, the OBG of the NTF decreases. Simultaneously, the gain of the first integrator also reduces - resulting a reduced variance of $x_1(t)$, as indicated by the area under the shaded portion of Fig. 6.5(a). When k_p increases, the OBG is greater than the nominal value. Since the gain of the first integrator also increases, the variance of $x_1(t)$ is larger than that found in the nominal case, as indicated in Fig. 6.5(c).

From the intuition presented above, we see that the variance of $x_1(t)$ is an indicator of k_p. The proposed tuning technique is summarized as follows -

1. Measure σ_{x1}, the variance of the continuous-time signal $x_1(t)$. This can be implemented using simple circuits as explained later.
2. Compare σ_{x1} with that expected for $k_p = 1$. The nominal value of σ_{x1} is obtained from simulations of the modulator.
3. Vary k_p in the right direction until σ_{x1} comes sufficiently close to the desired value. This is possible, since σ_{x1} is monotonic with k_p.

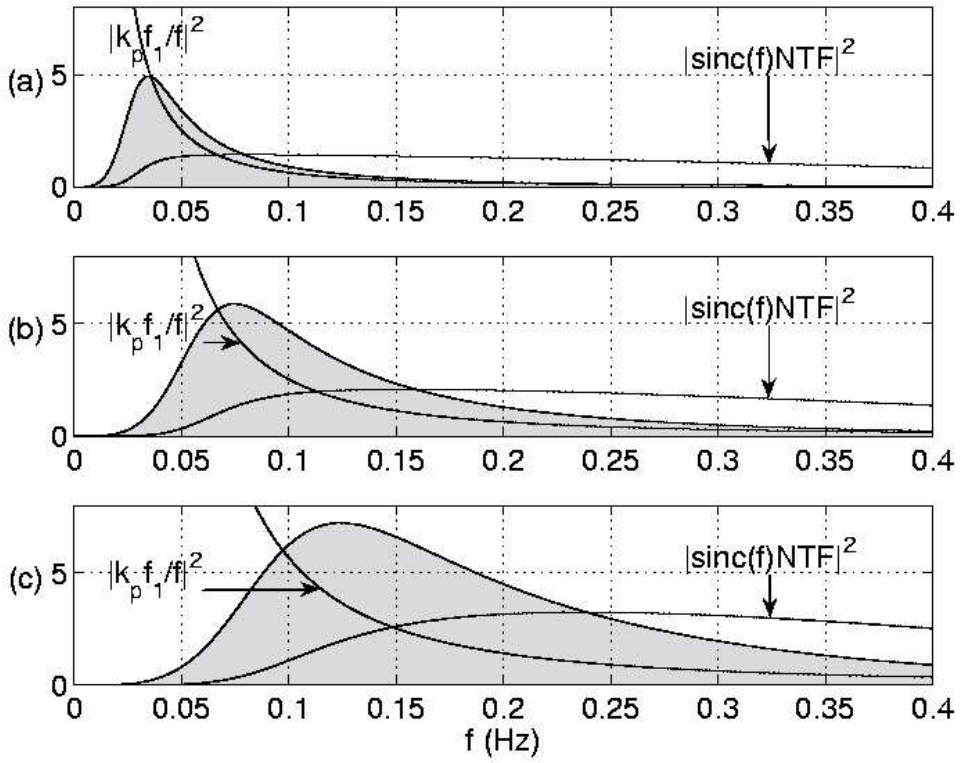


Figure 6.5: Spectrum of $x_1(t)$ for (a) $k_p < 1$ (b) $k_p = 1$ and (c) $k_p > 1$. The area under the shaded portion is proportional to σ_{x1}^2.

6.3 Simulation and Experimental Results

Matlab simulation results assure that σ_{x1} can be used as an indicator of variation in k_p and can be used as a reference to tune RC time constant. A third order single bit modulator with a sampling rate of 6.144 MHz and an OSR of 128 was chosen as an example. An NRZ feedback DAC was used. The loop filter was implemented using a Cascaded Integrators with Feed Forward (CIFF) topology. Fig. 6.6 shows the simulated σ_{x1} for eight random bandlimited input waveforms as k_p of the loop filter is varied from 0.75-1.25. Fig. 6.7 shows σ_{x1} as a function of k_p for sinusoidal inputs with varying amplitudes. From these figures, it is seen that the estimate of k_p obtained is largely independent of the type of the modulator input.

To tune k_p in a robust manner, one must also ensure that any technique that estimates k_p is not overly sensitive to random mismatch in component values

for a given value of k_p for all integrators in the modulator. Hundred Montecarlo simulations were run to estimate the sensitivity of σ_{x1} to random mismatch. These simulations were run for k_p values of 0.75, 1 and 1.25. A worst case random mismatch of 1.5% was assumed for resistors and capacitors for different integrators. Fig. 6.8 shows the histograms of σ_{x1} obtained, which show that it varies by only a few percent due to random mismatch in component values.

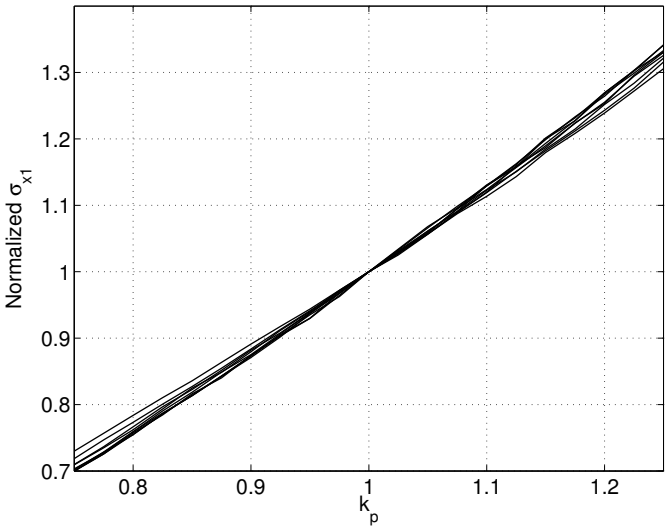


Figure 6.6: Variation of σ_{x1} with k_p for eight random bandlimited inputs.

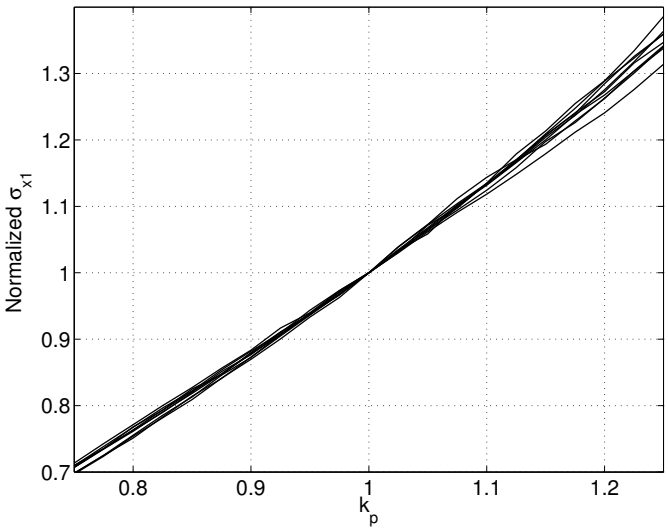


Figure 6.7: Variation of σ_{x1} with k_p for sinusoidal inputs with amplitudes varying from 0.1-0.9 MSA.

A single ended model of above CTDSM with sampling rate of 10 kHz and an OSR of 128, was implemented on a breadboard. The circuit diagram of this

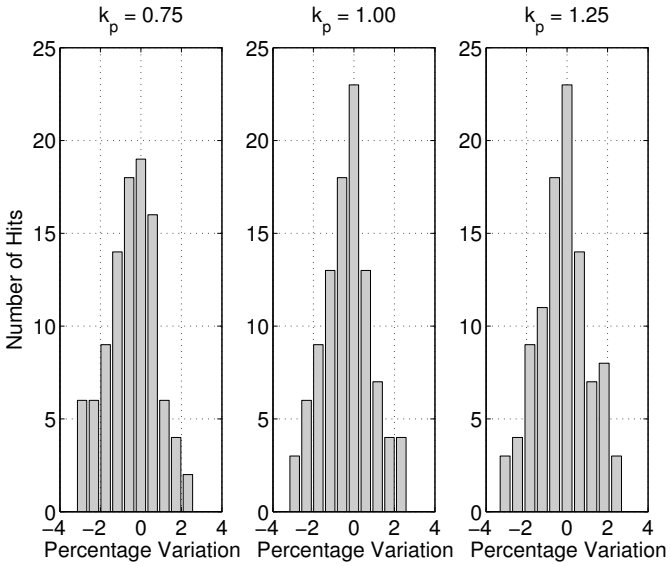


Figure 6.8: Variation of σ_{x1} for a worst case 1.5% random mismatch in R & C: (a) $k_p = 0.75$ (b) $k_p = 1.0$ and (c) $k_p = 1.25$. The number of trials is 100.

modulator is shown in Fig. 6.9. Monotonous nature of variation of σ_{x1} with k_p for different sine wave inputs as shown in Fig. 6.10, for this experimental circuit verifies that σ_{x1} is an indicator of k_p.

Fig. 6.11 shows the variations that would be seen in the NTF of the third order modulator without tuning. Part(b) of the figure shows the NTF after tuning process has been completed. It has been seen that the variations in the NTF are largely suppressed, thereby verifying the efficacy of our technique.

6.4 Hardware Implementation of the Tuning System

Automatic tuning of RC time-constant has been implemented with a fully differential loop filter realized using active-RC techniques in a 0.18 μm CMOS process. k_p is adjusted by using switchable resistor and capacitor banks. As described earlier, σ_{x1} is compared with a reference and a digital engine uses this information to appropriately adjust switches in the RC-banks. Block diagram for the

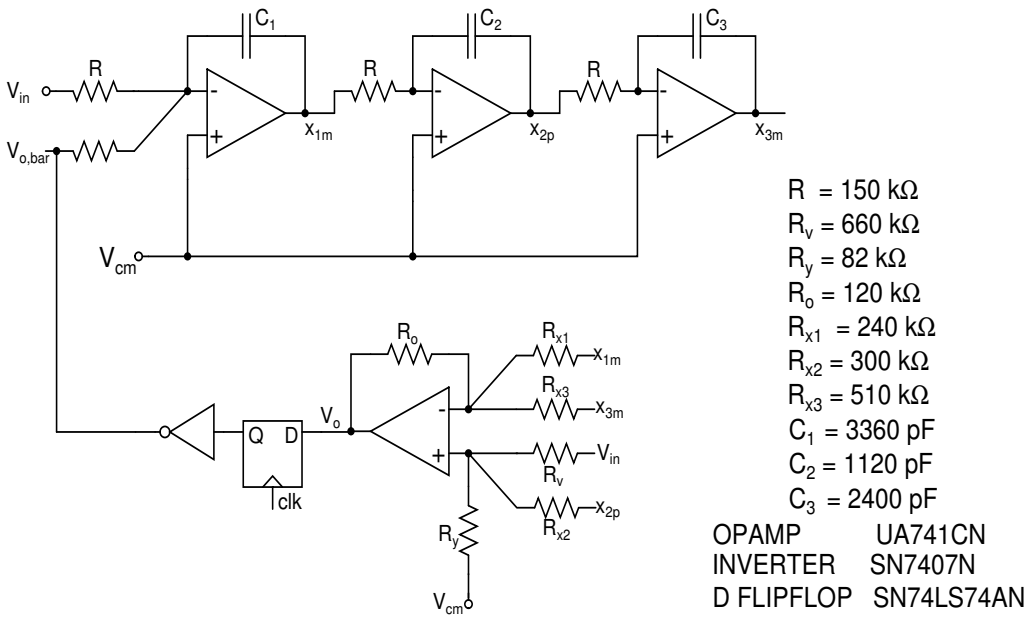


Figure 6.9: Circuit diagram of a single ended CTDSM implemented on a breadboard.

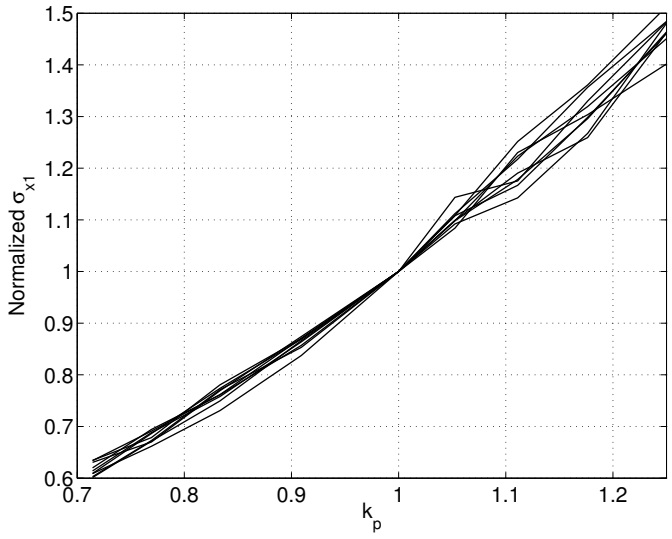


Figure 6.10: Variation of σ_{x1} with k_p for different sine wave inputs for modulator on a breadboard

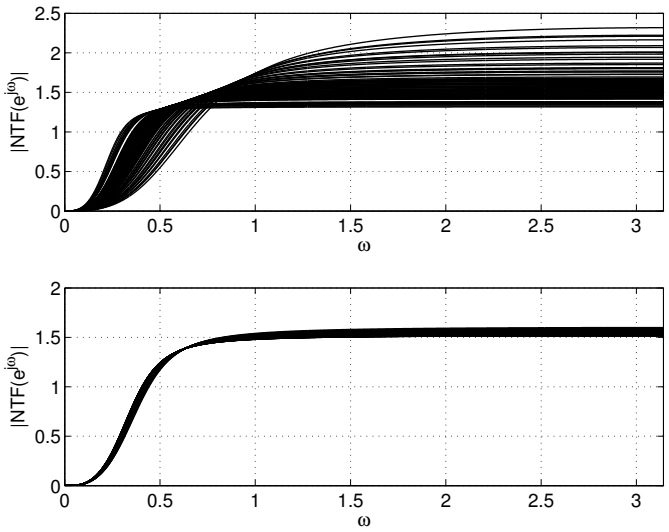


Figure 6.11: Modulator NTF (a) before tuning and (b) after tuning.

implementation of tuning scheme is shown in Fig. 6.12.

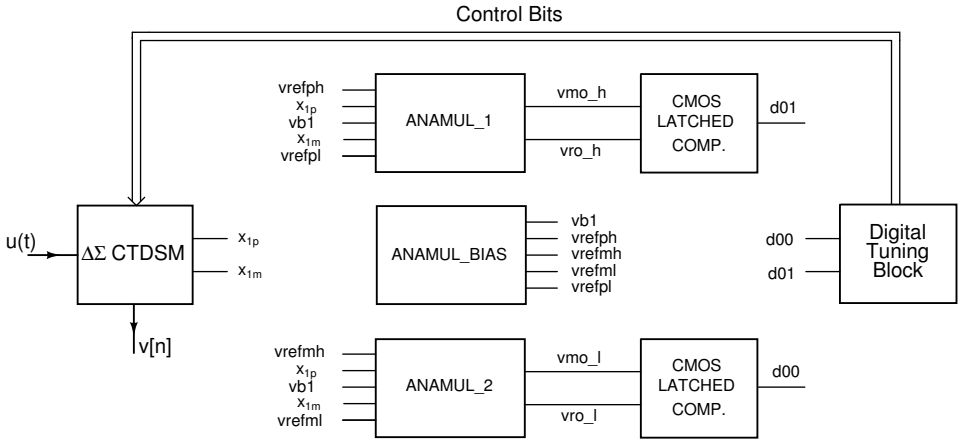


Figure 6.12: Block diagram for implementation of the tuning scheme. ANAMUL_1 and ANAMUL_2 are analog multipliers to calculate and compare a mean square value. ANAMUL_BIAS is used to generate bias voltages for analog multipliers. CMOS LATCHED COMP. gives digital logic signal to digital tuning block.

6.4.1 Measurement of σ_{x1}

The square law of the MOSFET is exploited to measure σ_{x1} as shown in Fig. 6.13. ϕ_1 and ϕ_2 are non-overlapping control signals. x_{1p} and x_{1m} are the single ended outputs of the first integrator, while V_{rp} and V_{rm} are the reference voltages for

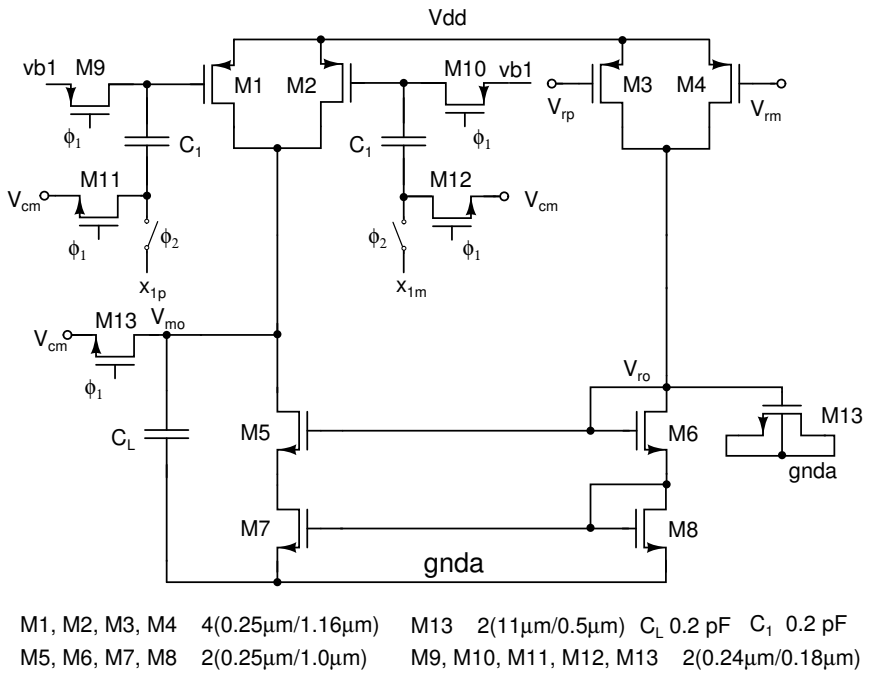


Figure 6.13: Circuit that compares σ_{x1}^2 with a reference mean square value. ϕ_1 and ϕ_2 are two non-overlapping clocks. Switches clocked by ϕ_2 are transmission gates with minimum sizes.

a given value of σ_{x1}. V_{cm} is the common mode voltage of $x_1(t)$. The capacitors labelled C_1 serve as level shifters. C_1 is decided according to the parasitic capacitance at the gate of M1 and M2, so that $x_1(t)$ is effectively transferred from the output of the first integrator to M1 and M2. C_L is the averaging capacitor.

When ϕ_1 is high, the level shifting capacitors are charged to $V_{cm} - vb1$, while C_L is charged to V_{cm}. Here, $vb1 = Vdd - |V_{th}|$ for M1 and M2. ϕ_2 is the comparison phase. Assuming square law operation for the transistors, it is quite straightforward to show that the sum of the drain currents of M1 and M2 is dependent on the square of x_{1p} and x_{1m}. In a similar faishon, the drain current of M6 is proportional to the square of reference voltages. Since the MOSFETs are biased at threshold voltage, only a positive gate overdrive will result in a current proportional to the square of the input voltage. So, it depends on the value of x_{1p} and x_{1m}, whether M1 (M2) is conducting in strong inversion region or subthreshold region.

In order to tune RC time-constant within $\pm 5\%$, both high and low reference values are required for σ_{x1}. As shown in Fig. 6.12, two analog multipliers are used

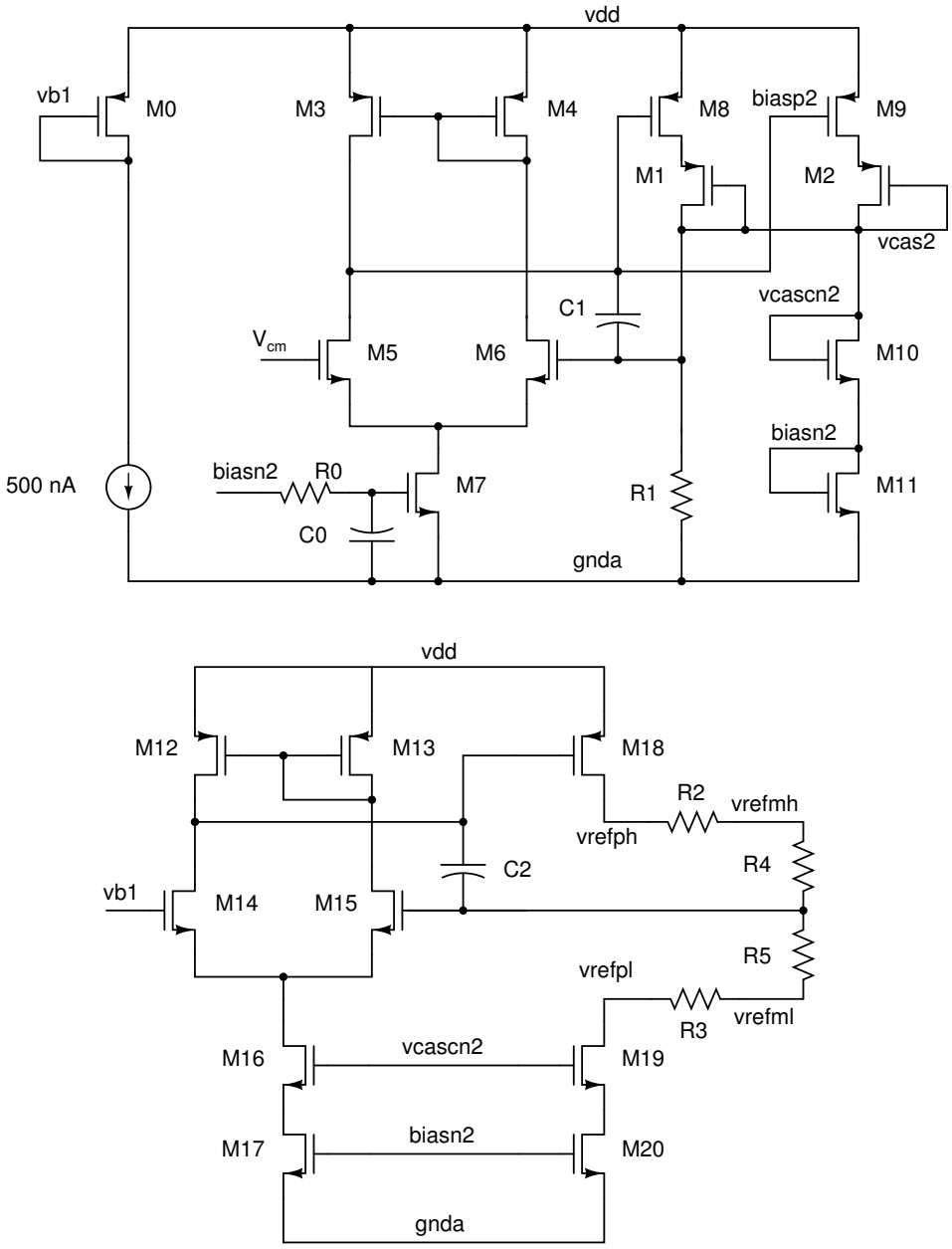
to decide if the actual σ_{x1} is within a range or not. Here, $vrefph$ and $vrefpl$ correspond to reference voltages for higher σ_{x1} and *vrefmh* and *vrefml* correspond to lower value of σ_{x1}. M3 and M4 are biased with V_{rp} and V_{rm}, which are *vrefph* (*vrefmh*) and *vrefpl* (*vrefml*) as generated by a bias circuit shown in Fig. 6.14. As $vrefph$ and $vrefpl$ rides over $vb1 = V_{dd} - |V_{th}|$, only either of M3 and M4 will conduct in the strong inversion region. The bias voltages are generated in a manner such that they are independent of process variation in resistance.

In Fig. 6.13, V_{ro} is a potential proportional to the mean square value of $x_1(t)$ and is used as a reference. If actual mean square value of $x_1(t)$ is greater than the reference value, then V_{mo} will be higher than V_{ro} and vice-versa. Now, V_{mo} and V_{ro} are compared using CMOS latched comparator as shown in Fig. 6.15. Output V_{op} serves as an input to the Digital Tuning Block (DTB) to decide if RC product has to be incresed or decreased. DTB is clocked with sampling frequency (f_s) in the modulator. Clocks *LC, LCb, L, Lb* and *LR* are generated by DTB. $t_{S,DTB}$ is the sampling instant when the compared logic V_{op} is registered in the tuning block.

6.4.2 *RC* Bank Adjustment

k_p can be adjusted by varying the integrating resistors, or capacitors, or both. Tuning only one kind of component (R or C) places undue requirements on the range of the other component bank. For example, modifying only the resistors to compensate for R and C variations will result in increased thermal noise when all the capacitors are smaller than their nominal values. On the other hand, tuning only capacitor values will necessitate larger bias currents in the opamps to drive the larger-than-nominal capacitive loads when the resistors are smaller than their nominal values. Here, R and C, both are varied to tune the time constants. Such an approach avoids the need for over-design of the opamps.

Fig. 6.16 shows resistor and capacitor banks across an integrator. nMOS switches are used in the banks where size of a switch connected to a resistor/capacitor, is scaled up by the factor by which a resistor is decreased or a capacitor is in-



M0	20(0.25µm/1.16µm)	M11, M17, M20	2(1µm/0.5µm)
M7	2(1µm/0.5µm)	M10, M16, M19	2(1µm/0.18µm)
M1, M2	2(1µm/0.18µm)	M3, M4, M12, M13	2(1µm/0.5µm)
M8, M9, M18	4(1µm/0.5µm)	M5, M6, M14, M15	2(2µm/2µm)
R0	200 kΩ	R1	1.86 MΩ
C0	1.25 pF	C1, C2	0.30 pF
R4, R5	171.36 kΩ	R2, R3	22.29 kΩ

Figure 6.14: Biasing circuit for analog multiplier (ANAMUL).

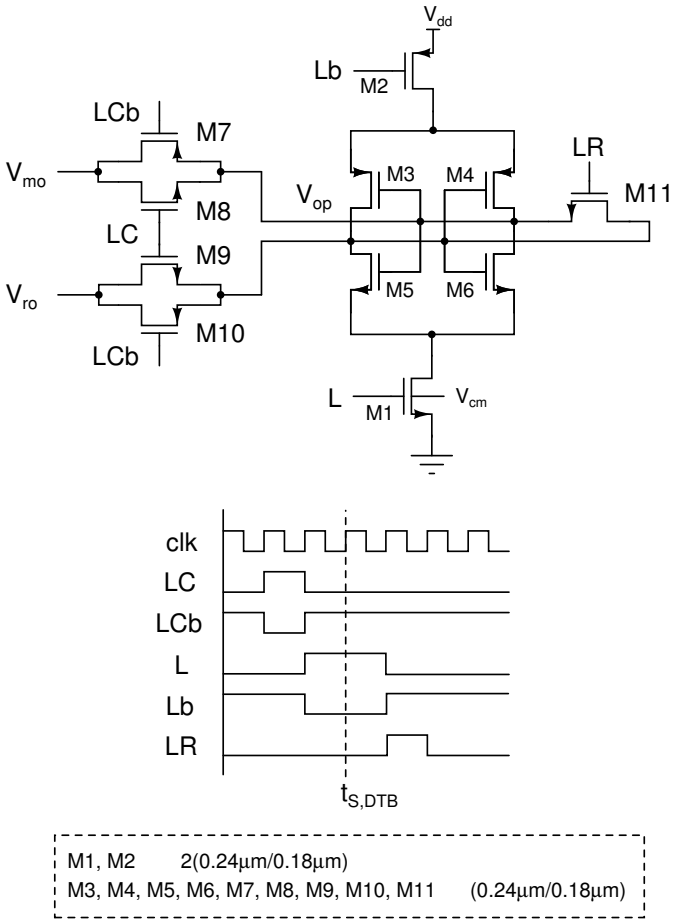


Figure 6.15: Circuit diagram for CMOS latched comparator.

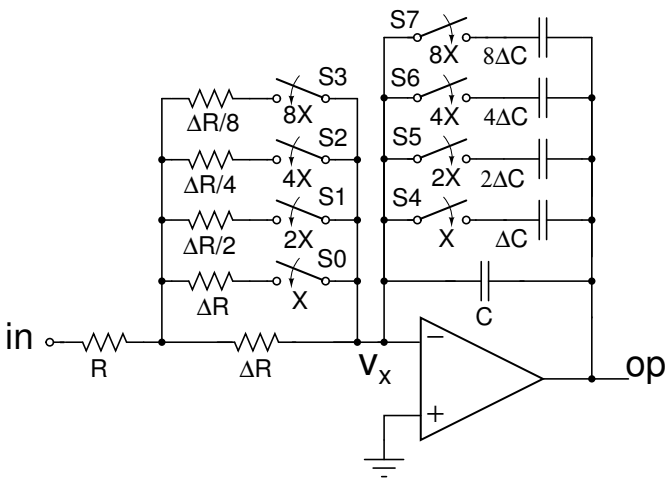


Figure 6.16: Resistor and Capacitor bank across an integrator

creased. For tuning RC within ±5%, four tunable resistors and capacitors were used, whose values for tuning close to their nominal values (R_{nom} and C_{nom}) are given by solving following eqs.

$$R_{nom} = (R + \frac{\Delta R}{2^m}) \times (1 + \sigma_{pr}) \tag{6.3}$$

$$R_{nom} = (R + \Delta R) \times (1 - \sigma_{nr}) \tag{6.4}$$

$$C_{nom} = (C + (2^n - 1)\Delta C) \times (1 - \sigma_{nc}) \tag{6.5}$$

$$C_{nom} = C \times (1 + \sigma_{pc}) \tag{6.6}$$

where n = 4 and m = 4. σ_{pr}/σ_{nr} and σ_{pc}/σ_{nc} are maximum/minimum deviation in resistance and capacitance values respectively over process variation. Component values are found for R and C banks such that each bank can be tuned independently to nominal values of R and C over extreme process corners. Here, resistors are used for coarse tuning and capacitors are used for fine tuning.

6.4.3 Digital Tuning Block (DTB)

Tuning of RC product starts with maximum resistance and capacitance in the circuit. DTB checks for the incoming logic signals *d00* and *d01*. Final tuned state is when *d00* is high and *d01* is low. For a R and C combination when both *d00* and *d01* are logic high, it means RC product is more than the upper reference value. And when both are low, RC product is lesser than the lower reference value. Based on the above logic combination, DTB validates its previous decision after analyzing *d00* and *d01*.

CHAPTER 7

APPENDIX

PIN DETAILS OF THE CHIP USING 0.5 V DSM

Pin out details of the chip designed using 0.5 V single bit CTDSM is shown in Fig. 7.1. The details and functionality of each pin are given in Table. 7.1.

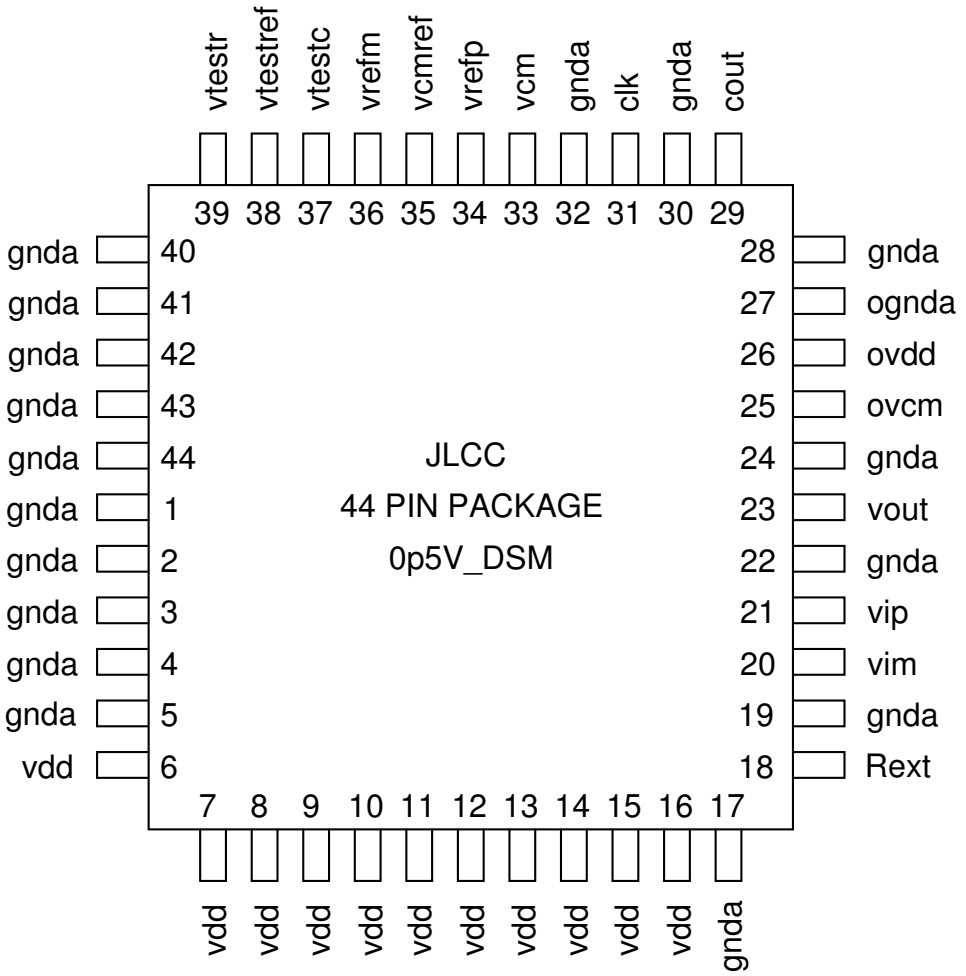


Figure 7.1: Pin details of the chip designed using 0.5 V CTDSM.

Table 7.1: Functionality of each pin of the chip designed using 0.5 V CTDSM.

Pin	Name	Functionality
1-5,17,19,22,24	gnda	Ground pin in the modulator
28,30,32,40-44	gnda	Ground pin in the modulator
6-16	vdd	VCC pin in the modulator (0.5 V)
18	Rext	Pin for external resistor for current bias
20,21	vim, vip	Differential input terminals
23	vout	Output of the modulator
25	ovcm	V_{cm} for output drivers
26	ovdd	Supply voltage (V_{dd}) for output drivers
27	ognda	Ground for output drivers
29	cout	Output clock derived from the clock generation circuit on the chip
31	clk	Input clock
33	vcm	V_{cm} for the modulator
34	vrefp	Supply voltage (V_{dd}) for current steering DAC
35	vcmref	V_{cm} for current steering DAC
36	vrefm	Ground for current steering DAC
37	vtestc	Positive plate of a testing capacitor
38	vtestref	Negative plate of a testing capacitor and one end of a testing resistor
39	vtestr	Other end of a testing resistor

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