DESIGN OF 16-BIT $\Sigma\Delta$ MODULATOR IN 0.35μm CMOS PROCESS

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CERTIFICATE

This is to certify that the project report titled **Design of 16-Bit $\Sigma\Delta$ Modulator in 0.35μm CMOS Process** submitted by **Sasi Pavan Majety** to the Indian Institute of Technology, Madras, for the award of the degree of ***Master of Technology*** **in** ***Electrical Engineering*** is a bonafide record of the work carried out by him under my supervision .

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Abstract

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Analog-to-digital converters (A/D) form the interface between analog and digital domains. These form an important role in the present day mixed signal processing. $\Sigma\Delta$ A/Ds form a class of oversampled A/D converters that get high resolution using low bit quantizers (typically 1-bit). This class of A/Ds are best suited for audio, video signals and for instrumentation purposes, where in the signal frequency is few kHz. With technology scaling the frequency range of operation of these A/Ds is also increasing. The project aims at implementing $\Sigma\Delta$ modulator with 16-bit resolution for audio applications (4 kHz bandwidth). A bandgap voltage reference which is a part of $\Sigma\Delta$ is also designed. Various constraints governing the system performance are studied. These constraints are then modelled in Matlab and Cadence and the design specifications are met. The system is then implemented on a typical 0.35μm CMOS process and is simulated. The layout of the system was also done in Cadence and sent for fabrication. A PCB has been designed for testing the chip.

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Acknowledgments

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Chapter 1

Introduction

1.1 Overview of $\Sigma\Delta$ Modulators

$\Sigma\Delta$ ADC form a class of oversampled data converters. These converters trade for resolution in time to that of resolution in amplitude. These acquire high resolution without much trimming in the component values. These are widely used in many applications like audio and video signal processing, instrumentation, telecommunication and etc. The present section gives a brief review of the modulator and some of the technical terms being used in the literature for these modulators.

$\Sigma\Delta$ modulator uses a recursive algorithm (feedback loop) for finding the digital value of the analog input. For, each input level it generates an output sequence whose average represents the input level by a number of necessary or sufficient bits. Each sequence is generated using clock. So the clock has to run at speed much higher than the signal itself. Hence these are called *oversampled* converters. Once the sequence is obtained further processing can be done in digital domain which is easy to realize. Fig .1.1 shows the basic idea of the modulator. The 1 bit quantizer generates a +1 or -1 depending on whether the output of the summer is positive or negative respectively. The DAC generates an analog output voltage corresponding to this value and feeds back to the summer in a negative manner. This will ensure that the output of the summer is restricted in both directions. The difference (Δ) between the input sample and feedback signal is accumulated in

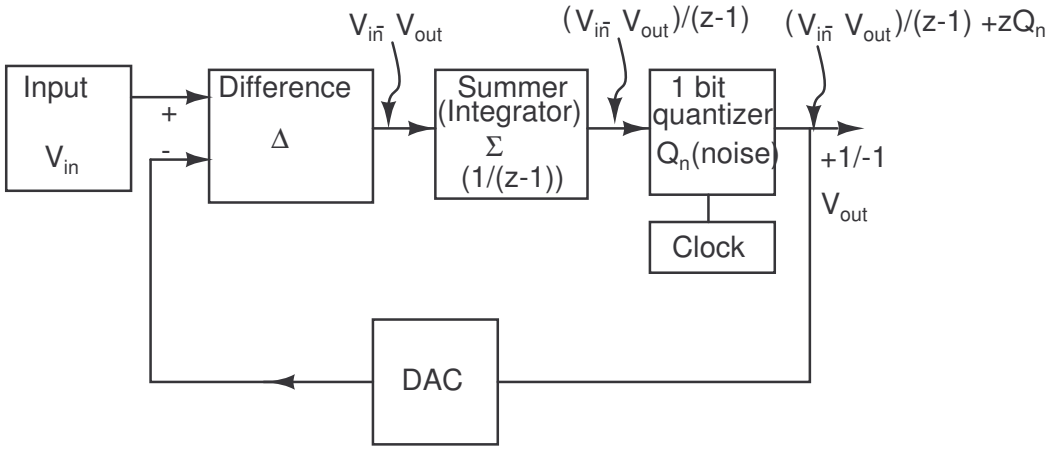


Figure 1.1: Basic idea of the $\Sigma\Delta$ Modulator

the summer (Σ) for each clock pulse. Hence the modulator gets its name $\Sigma\Delta$. The output of the Δ block after n clock pulses can be written as

$$nV_{in} - \Sigma V_{out} = \delta \tag{1.1}$$

where, δ is a bounded quantity due to negative feedback. Rearranging terms in the above equation one can write

$$V_{in} = \Sigma V_{out}/n + \delta/n \tag{1.2}$$

As, n increases the average of output matches the input. This idea can be well extended to a second order modulators where in there will be two integrators in cascade. The above relation for this case is given by

$$V_{in} = \frac{\Sigma\Sigma V_{out}}{n(n+1)/2} + \frac{\delta}{n(n+1)/2} \tag{1.3}$$

This relation shows that n need not be as high as in the first order case to get the same error. So, for obtaining same resolution in both order modulators one needs lesser oversampling ratio in a second order system compared to a first order system.

The quantization of analog sampled data signal to create finite number of levels introduces quantization error. If the signal itself is unpredictable, the error due to quantization process is also unpredictable. So this error can be called as

quantization noise. The quantization noise is assumed to be uniform ie constant over all frequencies. In literature it is termed as *white noise* [12]. Referring back to Fig. 1.1 the input and output relations in Z-domain can be written as follows

$$zV_{out}(z) = (V_{in}(z) - V_{out}(z))/(z-1) + zQ_n(z) \tag{1.4}$$

where, $Q_n(z)$ is the Z-transform of the quantization noise added by the quantizer.

$$\Rightarrow V_{out}(z) = z^{-1}V_{in}(z) + (1-z^{-1})Q_n(z) \tag{1.5}$$

Thus the quantization noise gets high pass filtered in the modulator. In other-words, the modulator reduces the in band quantization noise and pushes it away from the signal band. This is called as *noise shaping* in $\Sigma\Delta$ modulators.The out of band noise can be filtered out using digital filters. Thus a high resolution is obtained using a single bit quantizer.

1.2 Ideal 2nd Order $\Sigma\Delta$ Modulator

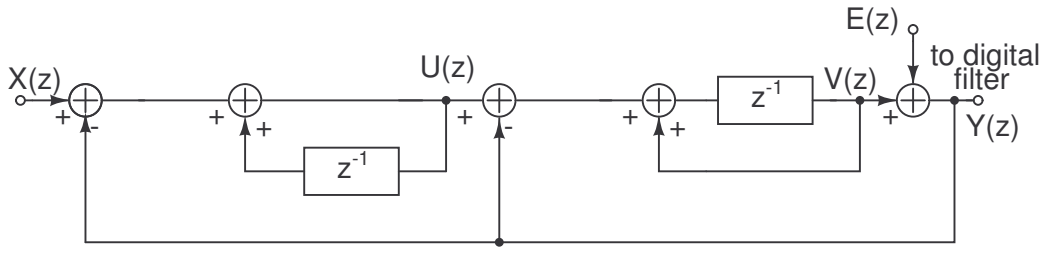


Figure 1.2: Block diagram of 2nd order $\Sigma\Delta$ modulator

The block diagram of 2nd order $\Sigma\Delta$ ADC is given in Fig. 1.2. Fig. 1.3 shows the modified architecture of Fig. 1.2 [1]. Simulations reveal that Fig. 1.2 is easy to realise and has lesser signal ranges within the integrators [1]. So, the modified architecture has been chosen for the implementation. $E(z)$ represent Z-transform of the quantization noise which is assumed to be random and uncorrelated with the previous values. $X(z)$ and $Y(z)$ are the Z-transforms of the input and output

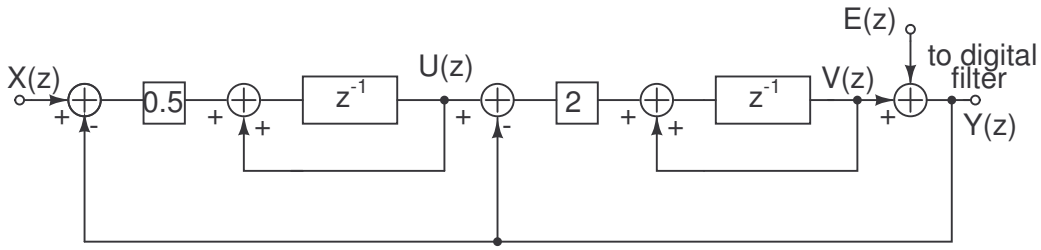


Figure 1.3: Modified block diagram of 2nd order $\Sigma\Delta$ modulator

respectively.

$$U(z) = \left(\frac{0.5\,z^{-1}}{1-z^{-1}}\right)(X(z) - Y(z)) \tag{1.6}$$

$$V(z) = \left(\frac{2\,z^{-1}}{1-z^{-1}}\right)(U(z) - Y(z)) \tag{1.7}$$

$$Y(z) = V(z) + E(z) \tag{1.8}$$

Using (1.6) and (1.7) in the above equation after some simplification Y(z) is given by

$$Y(z) = z^{-2}X(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{1.9}$$

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{1.10}$$

where,

STF(z) is the signal transfer function obtained by suppressing quantization noise in (1.9)

NTF(z) is the noise transfer function obtained by keeping
input zero in (1.9)

$$|NTF(f)| = |1 - e^{-j2\pi fT_s}|^2 \tag{1.11}$$

where,

T_s: Sampling period

$$\Rightarrow NTF(f) = 4\sin^2(\pi fT_s) \tag{1.12}$$

Let Δ be the LSB of the quantizer. If white noise nature is assumed for the quantization error, it can be shown that the noise power is given by $\Delta^2/12$ [3]. The input

is sampled at a rate f_s. The quantization noise is distributed uniformly in the range $[-f_s/2, f_s/2]$ (since white noise nature assumed). The noise power spectral density of the modulator is obtained by multiplying the quantization noise power spectral density with the square of the noise transfer function obtained in (1.12).

$$S_{\Sigma\Delta}(f) = \frac{NTF^2(f)\Delta^2}{12f_s} \tag{1.13}$$

where,

$S_{\Sigma\Delta}(f)$: noise power spectral density for the modulator

If the input signal is assumed to be in the band $[-f_b/2, f_b/2]$, then, the total noise power in the signal band is obtained by integrating the above expression over the band $[-f_b/2, f_b/2]$.

$$N_{inBW} = \int_{-f_b/2}^{f_b/2} S_{\Sigma\Delta}(f)df \tag{1.14}$$

where,

N_{inBW} : Noise power in the input signal band

Input is sampled at much higher rate than the signal frequency itself. So, $f_s >> f_b$. For low frequencies (frequencies within the input signal band), $\sin(\pi f T_s)$ is approximately equal to $\pi f T_s$. Using this relation in (1.14) the noise power is given by

$$N_{inBW} = \frac{\Delta^2}{12\,f_s}\int_{-f_b/2}^{f_b/2} (2\,\pi f T_s)^4\,df \tag{1.15}$$

$$\Rightarrow N_{inBW} = \frac{\Delta^2\pi^4 f_b^5}{60 f_s^5} \tag{1.16}$$

Oversampling ratio is given by f_s/f_b. Substituting for f_s/f_b in above, we get

$$N_{inBW} = \frac{\Delta^2\pi^4}{60\,OSR^5} \tag{1.17}$$

where,

OSR : oversampling ratio

If the signal is assumed to have a maximum power of P_{sig}, then the signal to noise ratio (SNR_{max}) can be defined as

$$SNR_{max} = 10\log\left(\frac{P_{sig}}{N_{inBW}}\right) \quad \text{dB} \tag{1.18}$$

Assuming the input to be a sinusoidal wave, the maximum peak value with out clipping is Δ. So, the maximum power associated with this amplitude is $\Delta^2/2$. Using this in (1.18)

$$SNR_{max} = 10\log\left(\Delta^2/2\right) - 10\log\left(\frac{\Delta^2\pi^4}{60\,OSR^5}\right) \quad \text{dB} \tag{1.19}$$

$$SNR_{max} = 50\log\left(OSR\right) - 5.115 \quad \text{dB} \tag{1.20}$$

Thus, by every doubling of OSR the SNR is increased by 15 dB. In otherwords, there is a 2.5 bit gain in every doubling of OSR. This illustrates how a low bit (1-bit here) quantizer is used to get resolution higher than the quantizer itself.

Chapter 2

Nonidealities in ΣΔ Modulators

2.1 Effect Of Gain Of opamp On ΣΔ Modulators

This section covers the effect of both the finite linear gain and non linear gain of the opamp on the performance of the ΣΔ modulators.

2.1.1 Effect of finite gain

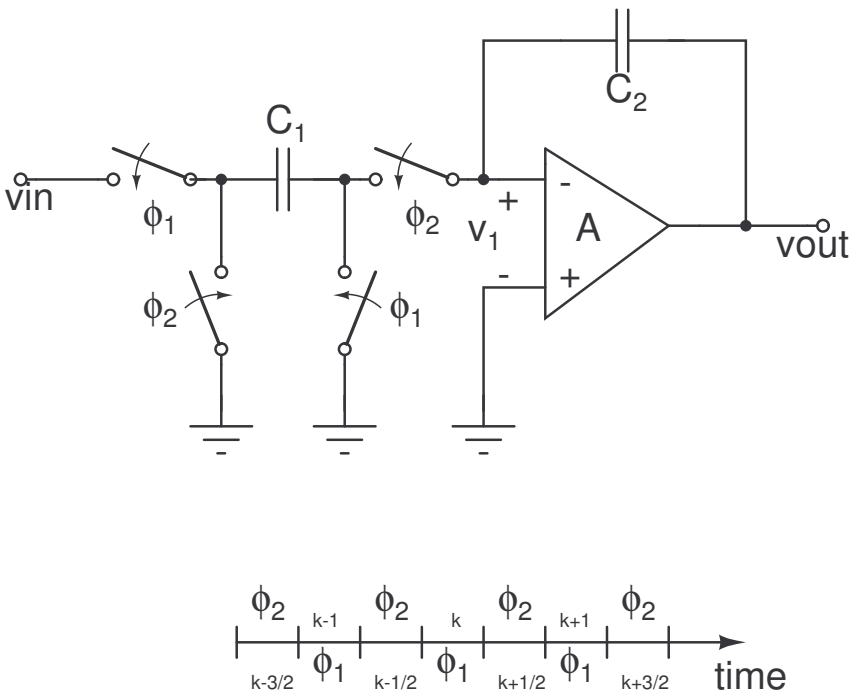


Figure 2.1: Switched capacitor integrator

This section covers the effect of finite gain of the opamp on the performance of $\Sigma\Delta$ modulators. Fig. 2.1 shows the schematic of the switched capacitor integrator. Each clock cycle is split into even and odd phases as shown in Fig. 2.1. It is assumed that the input and output voltages are constant when ϕ_1 is high. The charge stored on C_1 at the end of phase 1 (i.e ϕ_1 ON)

$$Q_{C_1} = C_1 v_{in}((k+1/2)T_s) = C_1 v_{in}(kT_s) \tag{2.1}$$

where,

T_s: sampling frequency (frequency of operation of the switches)

k: integer representing k^{th} clock cycle

Similarly,the charge stored on C_2 during this phase is,

$$Q_{C_2} = C_2\left(v_{out}((k+1/2)T_s) - v_1((k+1/2)T_s)\right) \tag{2.2}$$

Assuming the open loop gain of the amplifier to be equal to A, (2.2) can be rewritten as

$$Q_{C_2} = C_2 v_{out}((k+1/2)T_s)\left(1+1/A\right) \tag{2.3}$$

v_{out} is constant during this phase. So,

$$Q_{C_2} = C_2 v_{out}(kT_s)\left(1+1/A\right) \tag{2.4}$$

When ϕ_2 is ON C_1 discharges until v_{C_1} equals v_1. The charge on both the capacitors during this phase can be written as

$$Q_{C_1} = -C_1 v_1((k+1)T_s) \tag{2.5}$$

$$Q_{C_2} = C_2 v_{out}((k+1)T_s)\left(1+1/A\right) \tag{2.6}$$

Charge conservation states that the change in charge across both the capacitors should be equal.

$$\Rightarrow C_1 v_{in}(kT_s) - C_1 v_1((k+1)T_s) = C_2\left(1+1/A\right)\left(v_{out}(kT_s) - v_{out}((k+1)T_s)\right) \tag{2.7}$$

After some simplifications and applying the Z - transforms on the above result we get

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{\frac{C_1}{C_2}z^{-1}}{\left(1+1/A\right)\left(1-z^{-1}\right)+\frac{C_1}{AC_2}} \tag{2.8}$$

One more way of writing the above equation is

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{\frac{AC_1}{AC_2+C_1+C_2}z^{-1}}{1-\frac{AC_2+C_2}{AC_2+C_1+C_2}z^{-1}} \tag{2.9}$$

From [1] we have,

$$\Rightarrow H(z) = \frac{G_0 z^{-1}}{1-P_0 z^{-1}} \tag{2.10}$$

where,

$G_0 = \frac{AC_1}{AC_2+C_1+C_2}$

$P_0 = \frac{AC_2+C_2}{AC_2+C_1+C_2}$

When A tends to ∞ (2.8) approaches the ideal integrator transfer function. The finite gain causes only a fraction of the previous output to be added to the new sample [1] .

2.1.2 Effect of non linear gain

The opamp is assumed to have only odd order non-linearity. This is a valid assumption because fully differential configuration of the opamp cancel even order terms of the non linear gain. The model for the opamp is assumed to be of the form $\alpha\tanh(\beta v_i)$ where v_i is the input voltage across the positive and negative terminals of the opamp, α and β are the constants pertaining to the opamp being used. The model used for the analysis of the non linear gain is given in Fig. 2.2. During ϕ_1 phase the charge on both capacitors C_1 and C_2 is given by

$$Q_{C_1} = C_1 vin \tag{2.11}$$

$$Q_{C_2} = C_2(v_{out} - \Delta v) \tag{2.12}$$

$$\Rightarrow Q_{C_2} = C_2 v_{cap} \tag{2.13}$$

The polarity of these charges is shown in Fig. 2.2. During the next phase these charges can be rewritten as

$$Q_{C_1} = C_1(D v_{ref} - \Delta v) \tag{2.14}$$

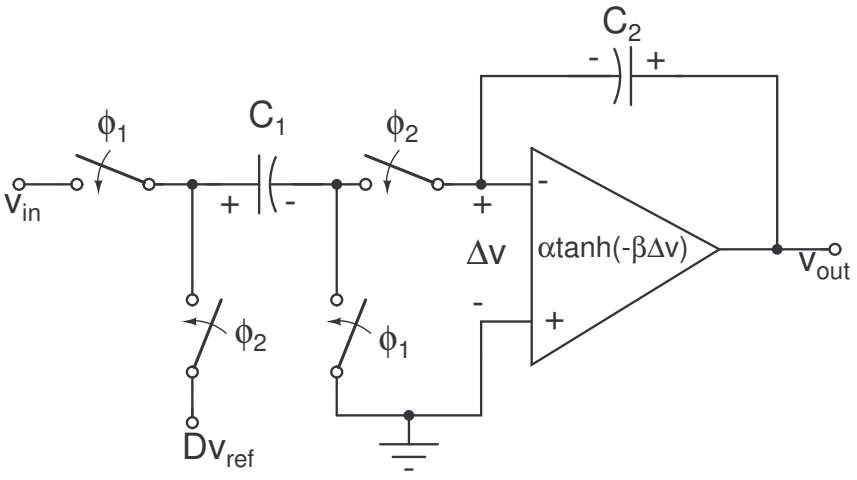


Figure 2.2: Modelling the non linear gain of opamp

$$Q_{C_2} = C_2(v_{out} - \Delta v) \tag{2.15}$$

$$\Rightarrow Q_{C_2} = C_2\left(\alpha\text{tanh}(-\beta\Delta v) - \Delta v\right) \tag{2.16}$$

If one considers a closed Gaussian surface around the bottom plate of both the capacitors, Gauss law states that the sum of net change in charge on both the capacitors is zero. So,

$$\Delta Q_{C_1} + \Delta Q_{C_2} = 0 \tag{2.17}$$

$$\Rightarrow C_1\left(vin - Dv_{ref} + \Delta v\right) + C_2\left(v_{cap} - \alpha\text{tanh}(-\beta\Delta v) + \Delta v\right) = 0 \tag{2.18}$$

$$\Rightarrow -C_2\alpha\text{tanh}(-\beta\Delta v) + C_2\Delta v + (vin - Dv_{ref})C_1 + C_2 v_{cap} = 0 \tag{2.19}$$

The above is a nonlinear equation that has to be solved for Δv. Form, Δv we can write v_{out} and v_{cap} for the next phase as

$$v_{out} = \alpha\text{tanh}(-\beta\Delta v) \tag{2.20}$$

$$v_{cap} = v_{out} - \Delta v \tag{2.21}$$

A Matlab code is written to solve 2.19 for Δv and find v_{out} and v_{cap}. α and β are estimated form the designed opamp characterstics. These values turn out to be 3.196 and 1094 respectively. Fig. 2.3 shows the frequency spectrum of the output for the modelling done in Matlab. The low frequency components are shown in Fig. 2.4.

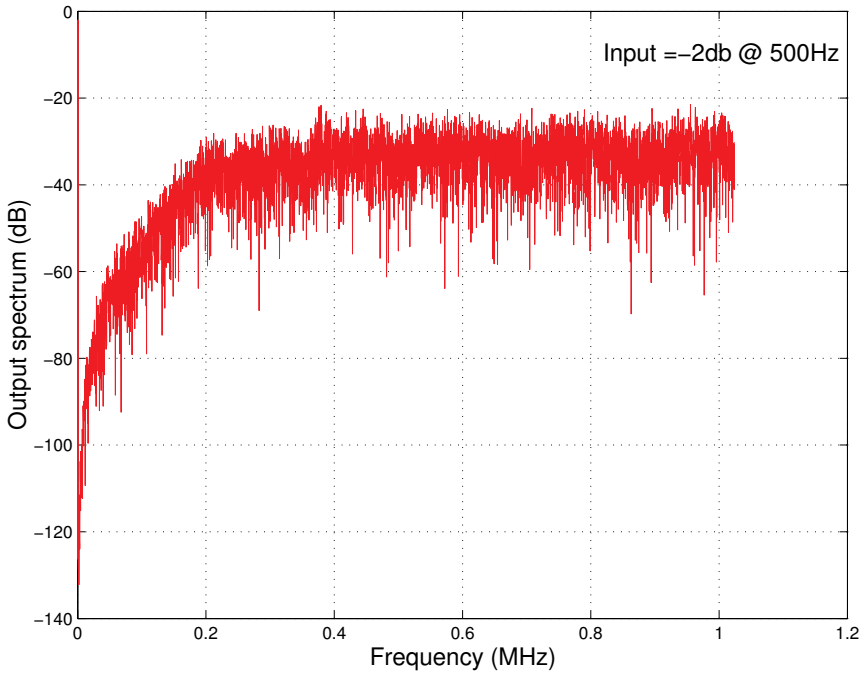


Figure 2.3: Output spectrum of the non linear model

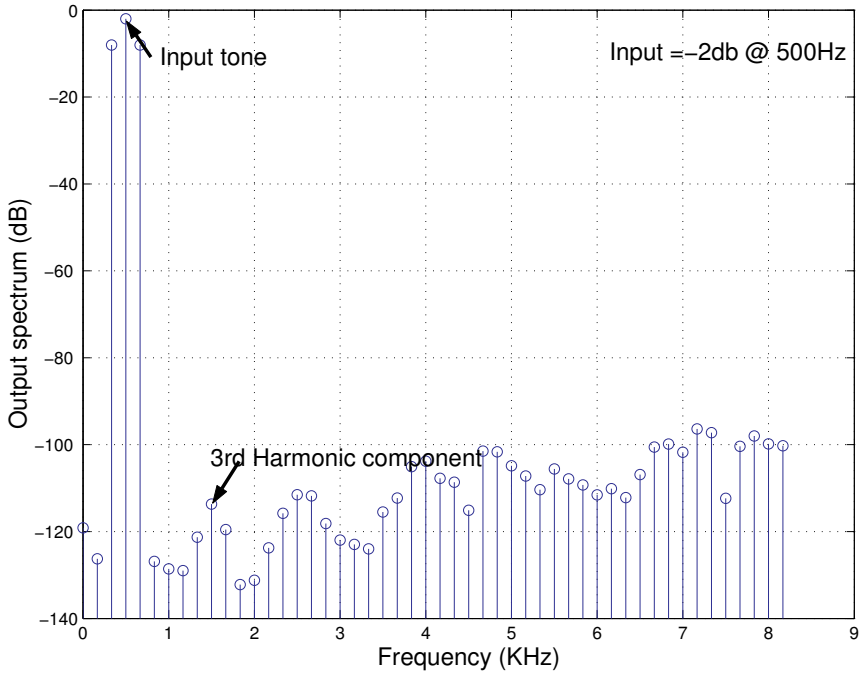


Figure 2.4: Low frequency components of Fig. 2.3

2.2 Settling Process In $\Sigma\Delta$ Modulators

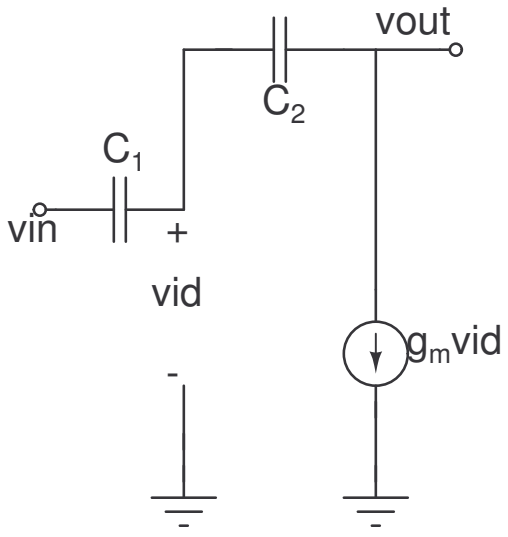


Figure 2.5: Model of integrator for settling analysis

In this section the effect of settling of the integrator in $\Sigma\Delta$ modulators is discussed. The settling process can be classified into two types. Linear settling and the non linear settling. The later is caused due to the slewing of the opamp. Linear settling appears as a gain error [1]. The present section mainly covers the non linear settling or the slewing in the integrator. Fig. 2.5 shows the model assumed for the analysis of non linear settling process. This is the equivalent circuit during the integration phase. During this phase the voltage vin is a constant whose value is equal to the charge stored on the capacitor during the sampling phase. Here only single pole model is assumed. The I-V characteristics of the transconductor are given in Fig. 2.6. g_m is the transconductance and is equal to the slope of the straight line AB. From this plot a few equations can be derived.

$$V_{max} = I_{tail}/g_m \tag{2.22}$$

$$V_{max} = SR\tau \tag{2.23}$$

where SR and $1/\tau$ are the slew rate of the transconductor and dominant pole of the integrator respectively. Depending on the input applied three ways of settling can

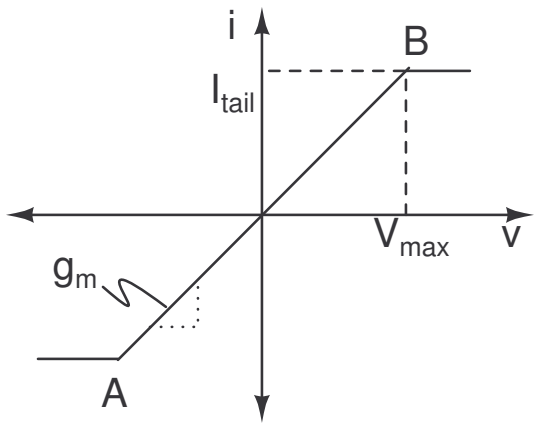


Figure 2.6: I-V characteristics of the transconductor

be thought of.

Case 1: Completely linear settling

From Fig. 2.5

$$vid = vout\frac{C_2}{C_1 + C_2} + vin\frac{C_1}{C_1 + C_2} \tag{2.24}$$

Assuming $G_o = C_1/C_2$ equal to 0.5

$$\Rightarrow vid = 2\,vout/3 + vin/3 \tag{2.25}$$

$$g_m vid(t) = C_2\frac{d\left(vid(t) - vout(t)\right)}{dt} \tag{2.26}$$

$$\Rightarrow g_m\left(2\,vout(t) + vin(t)\right) = -C_2\frac{d\left(vout(t)\right)}{dt} \tag{2.27}$$

(2.28)

$$\Rightarrow \frac{d(vout(t))}{dt} + \frac{2g_m vout(t)}{C_2} = -\frac{g_m}{C_2}vin(t) \tag{2.29}$$

Solution of the above differential equation gives

$$vout(t) = vout(nT - T) + G_o V_{samp}\left(1 - e^{-t/\tau}\right) \tag{2.30}$$

where,

$vout(nT - T)$: initial charge at the beginning of the integrating phase

$1/\tau$: $g_m/C2$ (bandwidth of integrator)

V_{samp}: charge sampled on to C_1 during sampling phase phase

Case 2: Completely slewing

This is the case when the input is so large compared to V_{max}, such that by the end of the integrating phase the opamp is still in the nonlinear region. For this case the output voltage can be written as

$$vout(t) = vout(nT - T) + SR\,t \tag{2.31}$$

Case 3: Partial slewing

In this case the opamp initially slews and then enters the linear region. The expression for this case is similar to that in (2.30) with the initial conditions changed. The general solution of (2.29) can be written as

$$vout(t) = A + B\left(1 - e^{-t/\tau}\right) \tag{2.32}$$

Let the time for slewing be t_0. At $t = t_0$ the output voltage form case 2 can be written as

$$vout(t_0) = vout(nT - T) + SR\,t_0 \tag{2.33}$$

(2.32) can be rewritten as

$$vout(t) = A + B\left(1 - e^{-(t-t_0)/\tau}\right) \tag{2.34}$$

Using (2.33) in (2.34) A equals to $vout(nT - T) + SR\,t_0$. In steady state the output voltage equals $vout(nT - T) + G_oV_{samp}$. Using this condition the value of B is obtained. The complete solution for this case can hence, be written as

$$vout(t) = vout(nT - T) + SR\,t_0 + (G_oV_{samp} + SR\,t_0)\left(1 - e^{-(t-t_0)/\tau}\right) \tag{2.35}$$

$$\Rightarrow vout(t) = vout(nT - T) + G_oV_{samp} + (SR\,t_0 - G_oV_{samp})\left(1 - e^{-(t-t_0)/\tau}\right) \tag{2.36}$$

The above results are modelled in Matlab and the effect of the settling process on the singal to noise ratio is studied. Fig. 2.7 shows the relative error in the signal to noise ratio for different slew rates.

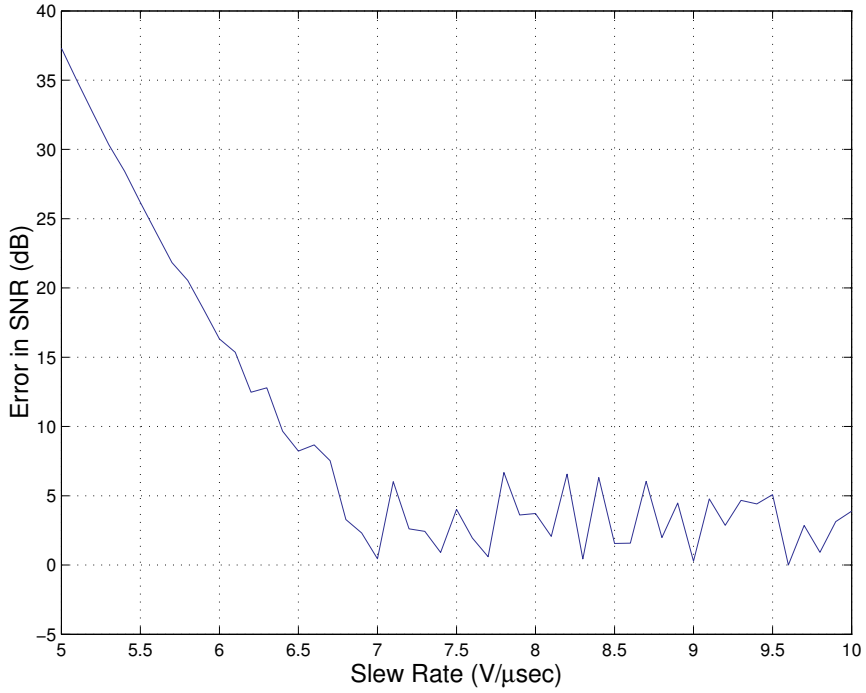


Figure 2.7: Relative change in SNR for various slew rates

2.3 Noise Analysis In $\Sigma\Delta$ Modulators

There are many sources of noise in the $\Sigma\Delta$ modulators apart from the quantization noise. But, the one that is of intrest to us is the noise at the input of the first integrator. The noise present at input of the comparator undergoes the second order noise shaping and the noise at the input of second integrator undergoes first order noise shaping [1]. Another way of explaining is the the noise at the input of the second integrator gets divided down by the large DC gain of the first opamp, when refered back at the input of first integrator. Hence, both are neglected. The noise appearing at the input of the first integrator is only described below.

2.3.1 Thermal Noise

The switched capacitor integrator ac equivalent circuit is given in Fig. 2.8. ϕ_1 and ϕ_2 are two non overlapping clocks. C_1 and C_2 are the sampling and integrating capacitors respectively. v_{in} and v_{out} are the input and output voltage respectively. The major contributors to the thermal noise are the input refered noise of the opamp

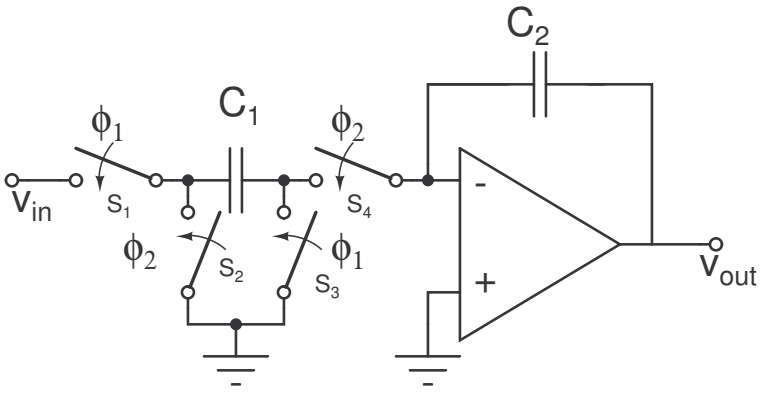


Figure 2.8: AC Equivalent of SC Integrator

and the finite on resistance of the switches. The leakage resistance of the capacitors also contributes to the thermal noise but is not considered here. Since, this is a time varying system having two phases, two cases are to be considered separately.

2.3.1.1 CASE 1 : ϕ_1 ON

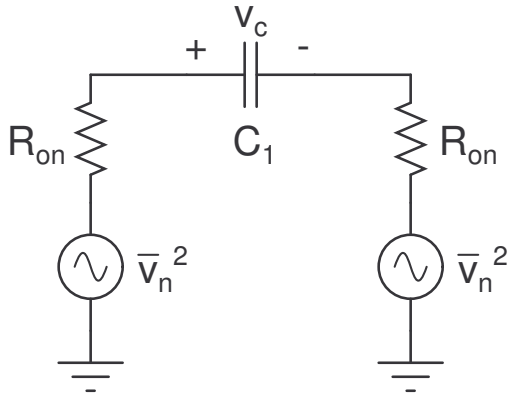


Figure 2.9: AC Equivalent during phase ϕ_1

During this phase, the thermal noise is only due to the finite ON resistance of the switches. The AC equivalent including the noise sources is shown in Fig. 2.9. $\overline{v}_n^2$ is the noise spectral density of the resistor, given by $4kTR_{on}$. The voltage transfer function across the capacitor from each of the noise sources is given by

$$H(j\omega) = \frac{1}{1 + j\omega 2R_{on}C_1} \tag{2.37}$$

$$|H(j\omega)|^2 = \frac{1}{1 + 4\left(\omega R_{on}C_1\right)^2} \tag{2.38}$$

The total noise power is obtained by multiplying (2.38) by the voltage spectral density and integrating along the entire frequency range. Hence, total Noise power during this phase is given by (two switches so $8kTR_{on}$)

$$N_{\phi 1} = \int_0^\infty 8kTR_{on} \left|H(\omega)\right|^2 d\omega \tag{2.39}$$

This value turns out to be equal to kT/C_1.

2.3.1.2 CASE 2 : ϕ_2 ON

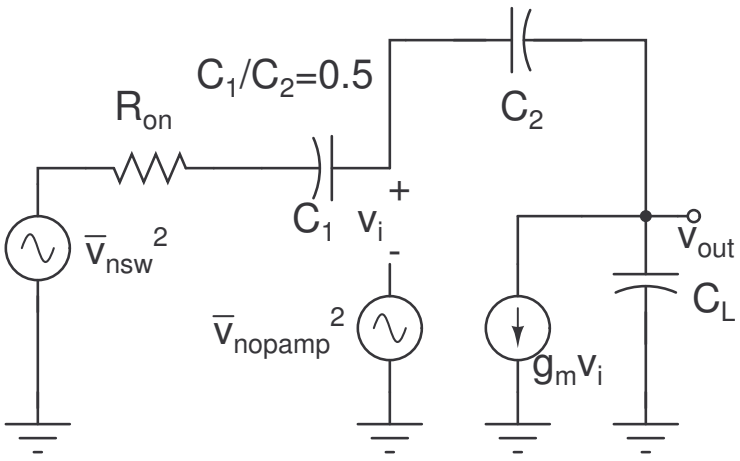


Figure 2.10: AC Equivalent during phase ϕ_2

The noise contributors in this case are the same as the previous one except for the opamp. In this phase the thermal noise of the opamp must also be considered. Fig. 2.10 shows the equivalent circuit along with their noise sources. The two noise sources ($\overline{v}^2_{nsw}$, $\overline{v}^2_{nopamp}$) are uncorrelated. Hence, noise from these sources is considered one at a time and then their powers are added to get the total noise power.

Noise contribution due to Integrating Switch (S_2, S_4)

The integrating capacitor keeps on accumulating the charge being sampled by the sampling capacitor. The comparator following this, switches state in accordance to

the charge on integrating capacitor. So, the noise voltage across C_2 is considered. Voltage across C_2 is v_i-v_{out} (see Fig. 2.10).

$$\frac{(v_i(s) - v_{nsw}(s))\, C_1}{1 + R_{on}C_1 s} + (v_i(s) - v_{out}(s))\, C_2 = 0 \tag{2.40}$$

$$(v_{out}(s) - v_i(s))\, sC_2 + g_m v_i(s) + v_{out}(s) sC_L = 0 \tag{2.41}$$

From (2.41) we have

$$v_{out}(s) = v_i(s) \frac{sC_2 - g_m}{s\,(C_L + C_2)} \tag{2.42}$$

From (2.40)

$$v_i(s) \left(\frac{C_1}{1 + R_{on}C_1} + C_2 \left(1 - \frac{sC_2 - g_m}{s\,(C_L + C_2)} \right) \right) = v_{nsw}(s) \frac{C_1}{1 + sR_{on}C_1} \tag{2.43}$$

$$v_i(s)\,(sC_1\,(C_L + C_2) + C_2\,(1 + sR_{on}C_1)\,(sC_L + g_m)) = v_{nsw}(s) sC_1\,(C_L + C_2) \tag{2.44}$$

$$\Rightarrow \frac{v_i(s)}{v_{nsw}(s)} = 0.5 \frac{s\,(C_L + C_2)}{s^2 R_{on}C_1C_L + s\,(R_{on}C_1 g_m + 1.5C_L + C_1) + g_m} \tag{2.45}$$

$$\Rightarrow v_{out}(s) = 0.5 v_i(s) \frac{sC_2 - g_m}{s^2 R_{on}C_1C_L + s\,(R_{on}C_1 g_m + 1.5C_L + C_1) + g_m} \tag{2.46}$$

Using (2.45) and (2.46)

$$v_{out}(s) - v_i(s) = 0.5 v_{nsw}(s) \frac{1 + \frac{sC_L}{g_m}}{1 + \frac{s}{g_m}\,(R_{on}C_1 g_m + 1.5C_L + C_1) + \frac{s^2 R_{on}C_1C_L}{g_m}} \tag{2.47}$$

$$NTF_{1,\phi_2}(s) = \frac{v_{out}(s) - v_i(s)}{v_{nsw}(s)} \tag{2.48}$$

where,NTF_{1,ϕ_2} denotes the required noise transfer function from $\overline{v}^2_{nsw}$ to the voltage across integrating capacitor.

$$\Rightarrow NTF_{1,\phi_2}(s) = 0.5 \frac{1 + \frac{sC_L}{g_m}}{1 + \frac{s}{g_m}\,(R_{on}C_1 g_m + 1.5C_L + C_1) + \frac{s^2 R_{on}C_1C_L}{g_m}} \tag{2.49}$$

We have $\overline{v}^2_{nsw}$ is equal to $4kTR_{on}$. The total integrated noise spectral density is obtained by integrating the above expression [2].

$$N_{1,\phi_2} = \int_0^\infty 4kTR_{on} |NTF_{1,\phi_2}(\omega)|^2 d\omega \tag{2.50}$$

$$\Rightarrow N_{1,\phi_2} = \frac{0.25\,(C_L + g_m R_{on}C_1)kT}{C_1\,(R_{on}C_1 g_m + 1.5C_L + C_1)} \tag{2.51}$$

Noise contribution due to OPAMP

The total thermal noise contributed by the OPAMP is represented using a single equivalent noise voltage source $\overline{v}^2_{nopamp}$ at the input. Referring to Fig. 2.10 contribution of opamp to total noise power is derived as follows

For this case v_{nsw} is made zero and the transfer function is obtained

$$v_i(s)\frac{C_1}{1+sR_{on}C_1} + \left(v_i(s) - v_{out}(s)\right)C_2 = 0 \tag{2.52}$$

$$\Rightarrow v_i(s)\left(\frac{C_1}{C_2\left(1+sR_{on}C_1\right)+1}\right) = v_{out}(s) \tag{2.53}$$

$$\left(v_{out}(s) - v_i(s)\right)sC_2 + v_{out}(s)sC_L + g_m\left(v_i(s) - v_{nopamp}(s)\right) = 0 \tag{2.54}$$

$$\Rightarrow v_{out}(s)\left(s\left(C_2+C_L\right)\right) - v_i(s)\left(sC_2 - g_m\right) = g_m v_{nopamp}(s) \tag{2.55}$$

Substituting (2.53) in (2.55) we get,

$$v_i(s)\left(\frac{s\left(C_2+C_L\right)}{\frac{0.5}{1+sR_{on}C_1}+1} - sC_2 - g_m\right) = g_m v_{nopamp}(s) \tag{2.56}$$

$$\Rightarrow v_i(s) = v_{nopamp}(s)\frac{g_m\left(1+R_{on}C_1\right)}{s^2R_{on}C_1C_L + s\left(g_mR_{on}C_1 + 1.5C_L + 0.5C_2\right) + g_m} \tag{2.57}$$

$$\Rightarrow v_i(s) = v_{nopamp}(s)\frac{\left(1+R_{on}C_1\right)}{s^2\frac{R_{on}C_1C_L}{g_m} + s\frac{\left(g_mR_{on}C_1+1.5C_L+0.5C_2\right)}{g_m}+1} \tag{2.58}$$

Using the results from (2.53)

$$v_{out}(s) = v_{nopamp}(s)\frac{\frac{C_1}{C_2}\left(1+sR_{on}C_1\right)}{s^2\frac{R_{on}C_1C_L}{g_m} + s\frac{\left(g_mR_{on}C_1+1.5C_L+0.5C_2\right)}{g_m}+1} \tag{2.59}$$

$$v_{out}(s) - v_i(s) = \frac{0.5v_{nopamp}(s)}{s^2\frac{R_{on}C_1C_L}{g_m} + s\frac{\left(g_mR_{on}C_1+1.5C_L+0.5C_2\right)}{g_m}+1} \tag{2.60}$$

$$NTF_{2,\phi_2}(s) = \frac{v_{out}(s) - v_i(s)}{v_{nopamp}(s)} \tag{2.61}$$

where, NTF_{2,ϕ_2} denotes the noise transfer function from the opamp noise source to the voltage across integrating capacitor.

$$\Rightarrow NTF_{2,\phi_2}(s) = \frac{0.5(s)}{s^2\frac{R_{on}C_1C_L}{g_m} + s\frac{\left(g_mR_{on}C_1+1.5C_L+0.5C_2\right)}{g_m}+1} \tag{2.62}$$

We have, $\overline{v}^2_{nopamp}$ equal to $4kT\gamma g_m$. Integrating the above equation gives the noise contribution due to opamp during this phase.

$$\Rightarrow N_{2,\phi_2} = \int_0^\infty 4kT\gamma g_m |NTF_{2,\phi_2}(\omega)|^2 d\omega \tag{2.63}$$

After simplification from [2] we can write

$$\Rightarrow N_{2,\phi_2} = \frac{kT\gamma}{g_m R_{on} C_1 + 1.5C_L + 0.5C_2} \tag{2.64}$$

The above equation is modelled in Matlab and the results are compared with those obtained by modelling the circuit shown in Fig. 2.10 in Cadence. Fig. 2.11 shows the results obtained both in Matlab and Cadence.

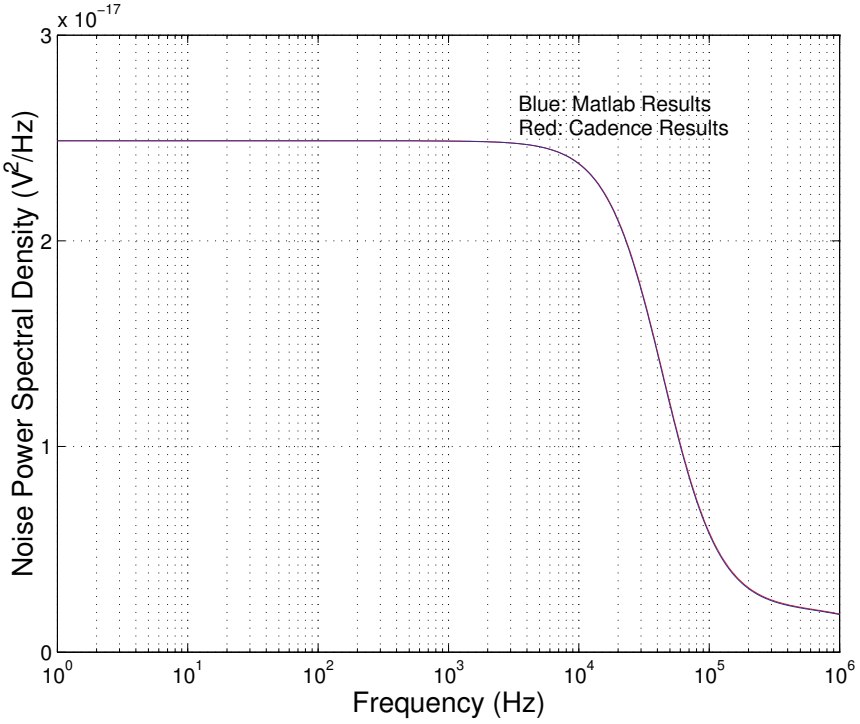


Figure 2.11: Simulation results of the thermal noise model obtained in Matlab and Cadence

Residual noise due to Opamp during phase ϕ_1

The opamp noise voltage of first opamp $\overline{v}^2_{nopamp}$ causes some noise voltage at its output during the sampling phase. This noise is sampled by the second sampling capacitor. The equivalent circuit for this is given in Fig. 2.12

$$\left(v_{nopamp}(s) - v_{out}(s)\right) g_m - v_{out}(s) s C_L = 0 \tag{2.65}$$

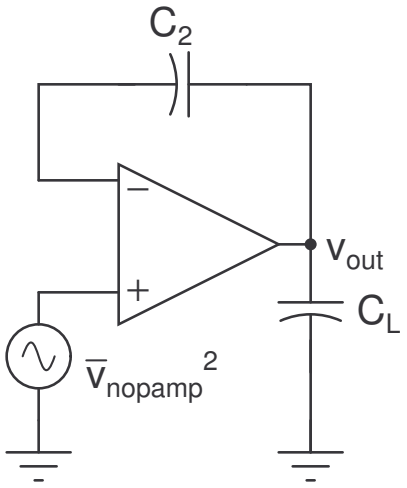


Figure 2.12: AC Equivalent during phase ϕ_1 for Opamp

$$\Rightarrow v_{out}(s) = v_{nopamp}(s)\frac{1}{1+s\frac{g_m}{C_L}} \tag{2.66}$$

The total noise contribution is obtained by integrating (2.66)

$$N_{op,\phi_1} = \int_0^\infty |v_{out}(\omega)|^2 d\omega \tag{2.67}$$

$$\Rightarrow N_{op,\phi_1} = \frac{g_m}{C_L}\overline{v}^2_{nopamp} \tag{2.68}$$

$$\Rightarrow N_{op,\phi_1} = \frac{4kT\gamma}{C_L} \tag{2.69}$$

When ϕ_1 is ON the sampling capacitor stores noise due to the switch. During the other phase the integrating capacitor accumulates this noise in additon to the noise contributed by the opamp and the integrating switches. Since, all the noise sources are uncorrelated their noise powers are added to get the total thermal noise during both the phases.

$$N_{th} = N_{\phi_1} + N_{1,\phi_2} + N_{2,\phi_2} + N_{op,\phi_1} \tag{2.70}$$

This power is uniformly distributed over the entire frequency range. Since the system is sampled periodically at a frequency f_s the power from higher frequencies is aliased back into the base band, the noise spectral density is given by $\frac{N_{th}}{f_s}\, V/\sqrt{Hz}$. Hence, the power in a bandwidth (BW) is

$$N_{th,BW} = \left(N_{\phi_1} + N_{1,\phi_2} + N_{2,\phi_2} + N_{op,\phi_1}\right) BW/f_s \tag{2.71}$$

$$\Rightarrow N_{th,BW} = kT\left(\frac{1}{C_1} + \frac{0.25\left(C_L + g_m R_{on} C_1\right) + \gamma C_1}{C_1\left(R_{on} C_1 g_m + 1.5C_L + C_1\right)} + \frac{4\gamma}{C_L}\right)\left(\frac{BW}{f_s}\right) \tag{2.72}$$

This is the total integrated noise power in the singal band due to the switch ON resistance and due to the opamp thermal noise. This expression is used to find the minmum value of the sampling capacitor being used and is explained in detail later.

Chapter 3

$\Sigma\Delta$ Modulator Design

3.1 $\Sigma\Delta$ Modulator Design

Fig. 3.1 shows the schematic of the 2nd order $\Sigma\Delta$ modulator. Fully differential configuration is preferred to the single ended version since the former has the advantage of cancelling any signal symmetrical to both positive and negative inputs. The circuit consists of two switched capacitor integrators with gain of 0.5 each followed by a comparator, latch and a DAC. Comparator and the latch convert analog output of the second integrator into binary bits (*outp*, *outn*). DAC generates two analog levels, *vrefp+* and *vrefp-*, to be fedback into the integrators. The analog value being fedback is determined by the binary bits generated by the comparator and latch. The switched capacitor integrators are controlled by two phase non overlapping clocks generated form a single master clock. Switch S_5 is opened slightly ahead of S_2. This ensures that the bottom plates of the sampling capacitors (1.6 pF and 0.5 pF) are floating for sometime before the next phase starts. During this time no charge can leak through the sampling capacitors and hence onto the integrating capacitors. Thus, signal dependent charge injection will be reduced. Similar reason is accounted for opening S_4 ahead of S_1 and S_3. If only NMOS or PMOS devices are used as switches at the input, as the input changes the gate source voltage of the device change. So the resistance of the switch is different for different values of input voltage. This causes harmonic distortion in the sampled voltage. Hence, reduce SNR of the modulator. If the gate source voltage of the device is

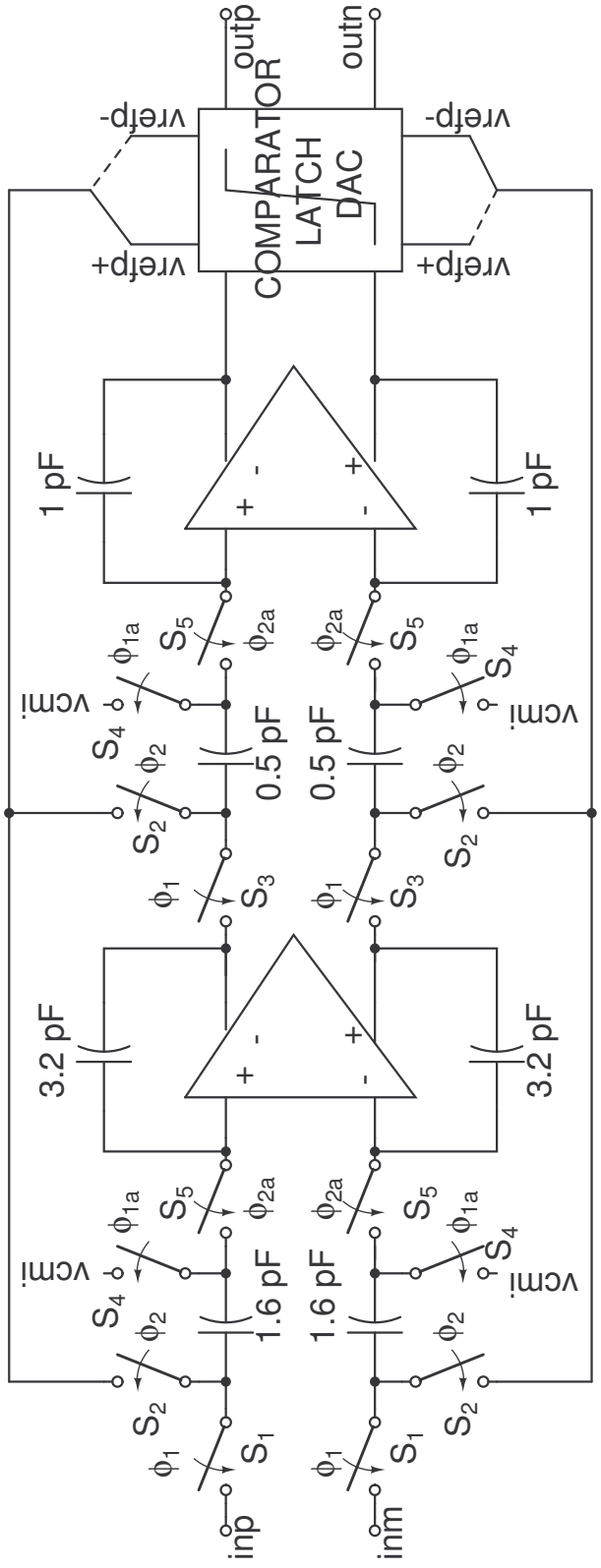


Figure 3.1: Schematic of 2nd order $\Sigma\Delta$ modulator

held constant for different values of input voltage, the resistance will be a constant and hence harmonic distortion is reduced. Bootstrap switch given in Fig. 3.2

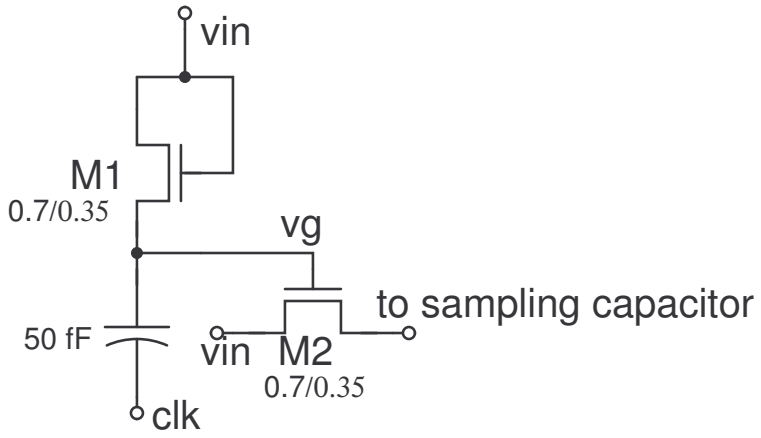


Figure 3.2: Bootstrap switch used to reduce harmonic distortion

serves this purpose. When the clock (clk) signal is low M1 conducts. Since, diode connected, the device operates in the saturation region. The capacitor during this phase charges to a voltage vg given by

$$vg(nT_s) = vin(nT_s) - (v_{th} + V_{Dsat,M1}) \tag{3.1}$$

where,

T_s: clock period

v_{th}: threshold voltage of the device M1

$V_{Dsat,M1}$: gate overdrive of M1

$vin(nT_s)$ denotes the input voltage in n^{th} clock cycle

During the next phase when the clock is high M1 turns OFF and the voltage vg will be the sum of clock signal voltage and the voltage stored on the capacitor during the earlier phase.

$$vg\left((n+1/2)T_s\right) = v_{clk} + vin(nT_s) - (v_{th} + V_{Dsat,M1}) \tag{3.2}$$

The gate to source voltage of M2 during this phase is given by

$$v_{gs,M2} = v_{clk} + vin(nT_s) - (v_{th} + V_{Dsat,M1}) - vin\left((n+1/2)T_s\right) \tag{3.3}$$

Input signal (vin) operates at much lower frequency compared to that of the clock frequency. Hence, it can be assumed that $vin(nT_s)$ is equal to $vin\left((n+1/2)T_s\right)$. So, (3.3) can be approximately written as

$$v_{gs,M2} = v_{clk} - (v_{th} + V_{Dsat,M1}) \tag{3.4}$$

which is a constant to a first order approximation (body effect neglected). When clock is low both source and drain of M2 are higher than vg. So, M2 is OFF when clock is low. Fig. 3.3 shows the harmonic distortion of the voltage across the sam-

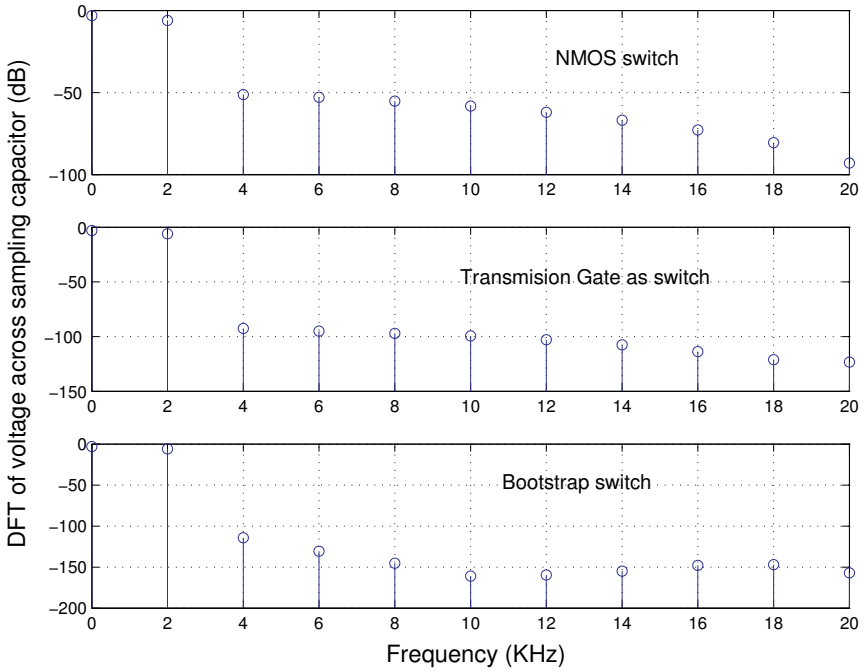


Figure 3.3: Harmonic distortion for different switches

pling capacitor when the input switch is made from only NMOS device, transmision gate and bootstrapped switch. From the figure it is evident that the bootstrapped switch gives less harmonic distortion compared to the other two.

3.2 Clock Generation

As mentioned earlier the modulator needs two phase non overlapping clocks for proper operation. Fig. 3.4 shows the schematic for generating two phase clocks.

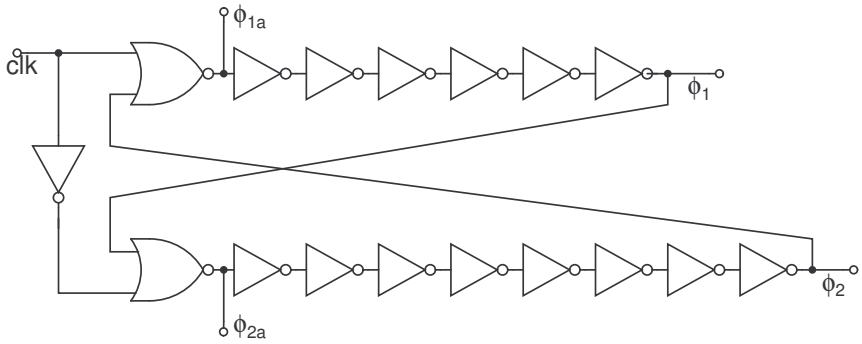


Figure 3.4: Two phase clock generation

The circuit is a latch whose outputs are connected back to back after some delay. The inverters provide delays to each phase of the clock. So, the advanced clocks required for reducing signal dependent charge injection are also simultaneously obtained. The inverters and the NOR gates used are of static CMOS type. Fig. 3.5 shows the obtained waveforms for the designed clock generation scheme.

3.3 Choosing Capacitors

Two capacitors are used in each of the two integrators of the modulator. The choice of these is made based on the noise contributions by the finite ON resistance of the switch and those due to the opamp. Desired SNR for the ADC was 109 dB. The modulator should not be limited by the thermal noise. So, the thermal noise floor has to be 109 dB. For the switch size chosen the ON resistance was around 2 KΩ. The transconductance was 340 μS. The load capacitance will be of the order of few femto farads and hence neglected. γ is taken as 0.7 (approximately). Using, the above values in (2.72) the value of sampling capacitor is obtained as 1.6 pF. The value of larger capacitance justifies the reason for neglecting the load capacitance. The gain of the integrator is taken as 0.5 [1]. Hence, the value of the integrating capacitance for this value of sampling capacitance is 3.2 pF. It was explained earlier that the thermal noise of the second interator was not much of a concern. So, the capacitance values can be decreased. This inturn reduces the power budget of

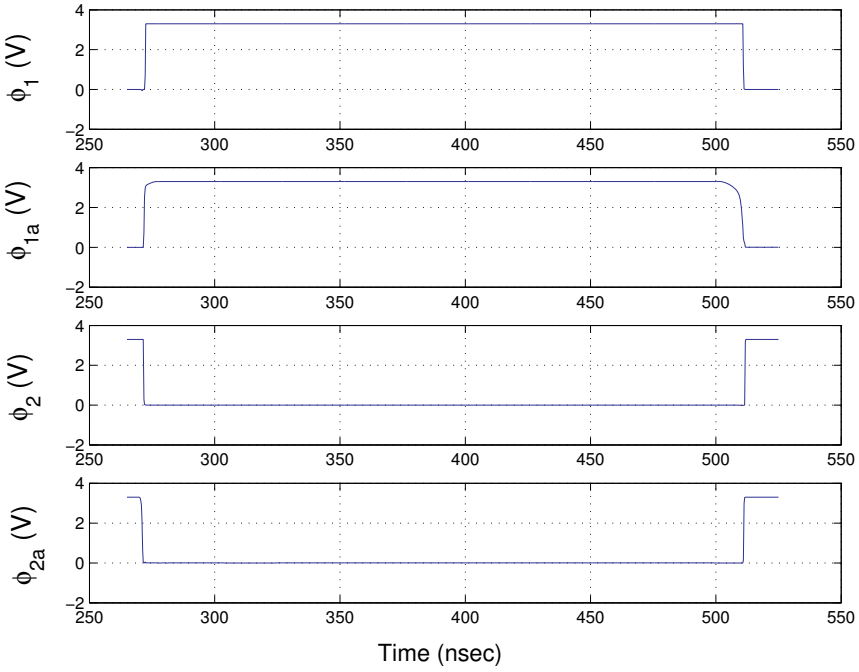
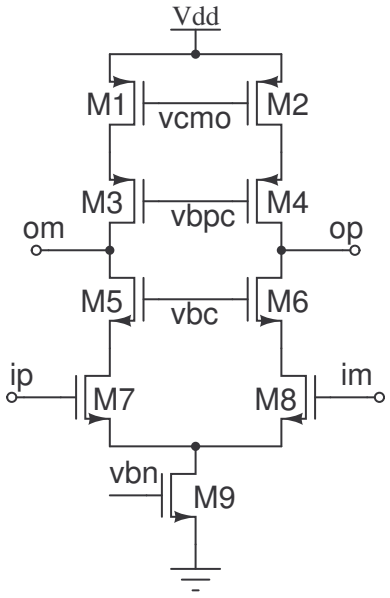


Figure 3.5: Two phase non overlapping clocks

the opamp. So, the value of sampling and integrating capacitance for the second integrator are taken as 0.5 pF and 1 pF respectively.

3.4 Opamp Design

For an single pole system about 99% of settling can be achieved in five time constants. In a sampled data system only half the clock period is available for settling. Hence unity gain frequency of the opamp has to be at least 10 times that of the clock frequency. In otherwords the bandwidth of the opamp has to be at least one order of magnitude greater than clock frequency [1]. From this value and the capacitance value obtained above, the transconductance is obtained. The tail current is obtained form the slew rate and the capacitance values. Simulations given in [1] indicate that opamp should have minimum gain equal to oversampling ratio. For a given Δ value, from the Matlab simulations the input and output voltage swings are obtained. Based on the above arguments the specifications of the opamp are



Transistor	W/L in µm	Fingers
M1, M2	5/1	12
M3, M4	5/0.5	12
M5, M6	5/2	6
M7, M8	5/2	24
M9	2.5/0.5	24

Figure 3.6: Telescopic Opamp

shown in the table given below. Fig. 3.6 shows the schematic of the opamp being

Specification	Value
Bandwidth	20.48 MHz
Gain	256
Slewrate	20 V/μsec
Output Swing	3.6 V peak to peak differential
Tail Current	120 μA

Table 3.1: Opamp Specifications

used. Fully differential telescopic configuration is chosen to meet the specifications. The input devices M7 and M8 are made large to bring down the 1/f noise to the thermal noise floor. The widths of all the devices is kept same so that while doing the layout all the devices can be stacked one over the other easily. Lengths of M5, M6 are made large so as to increase the gain. For the second opamp all the devices sizes are simply scaled down by a factor of 3 to reduce the power by a factor of 3.

3.4.1 Opamp bias

The important part in the design of the opamp is the bias circuit. Fig. 3.7 shows the bias circuit being used. All the bias node voltages are derived form a single master current source. The master current is given from external source and doesn't form the part of the design. The devices M3 - M10 are the slave devices taking current from the master device M1 - M2. The devices M17 - M20 from a precision bias circuit to get the exact value of tail current. Similar setup is used for generating the bias voltage for the top PMOS devices. Devices M21 - M23, M26 and M27 are used to generate the bias voltage for the gates of cascode NMOS devices and the input common mode voltage. Similar setup is done to generate the cascode PMOS device gate voltage. The input common mode voltage is given to a switch. So, whenever switching takes place it demands currents higher than the normal bias value for short duration. In the absence of this excess current there will be a fair amount of spikes at the gate of M22. This modulates the current through the device and due to feedback action all the bias node voltages begin to ring. So, a common source stage is put so as to meet this extra current required during switching. The devices M24 and M25 serve this purpose. Finally, a lowpass filter is put to further reduce ringing on that node. All the bias nodes have capacitors so as to maintain their voltages constant when switching takes place. The capacitance value are derived from MOS devices as they have higher density compared to the poly capacitors.

3.4.2 Common mode feedback circuit

Fully differential opamps need a common mode feedback circuit to fix the output common mode voltage. Many schemes of common mode feed back are present in literature [4], [3]. The one that is being used here is the switched capacitor common mode feed back circuit and is shown in Fig. 3.8. The switches S_1 and S_2 operate in anti phase. When S_1 is ON the capacitor C_b is charged to a voltage equal to vbp - vcmref. The voltage vbp is generated from the bias circuit discussed in previous section. The voltage vcmref is given from the external source. When

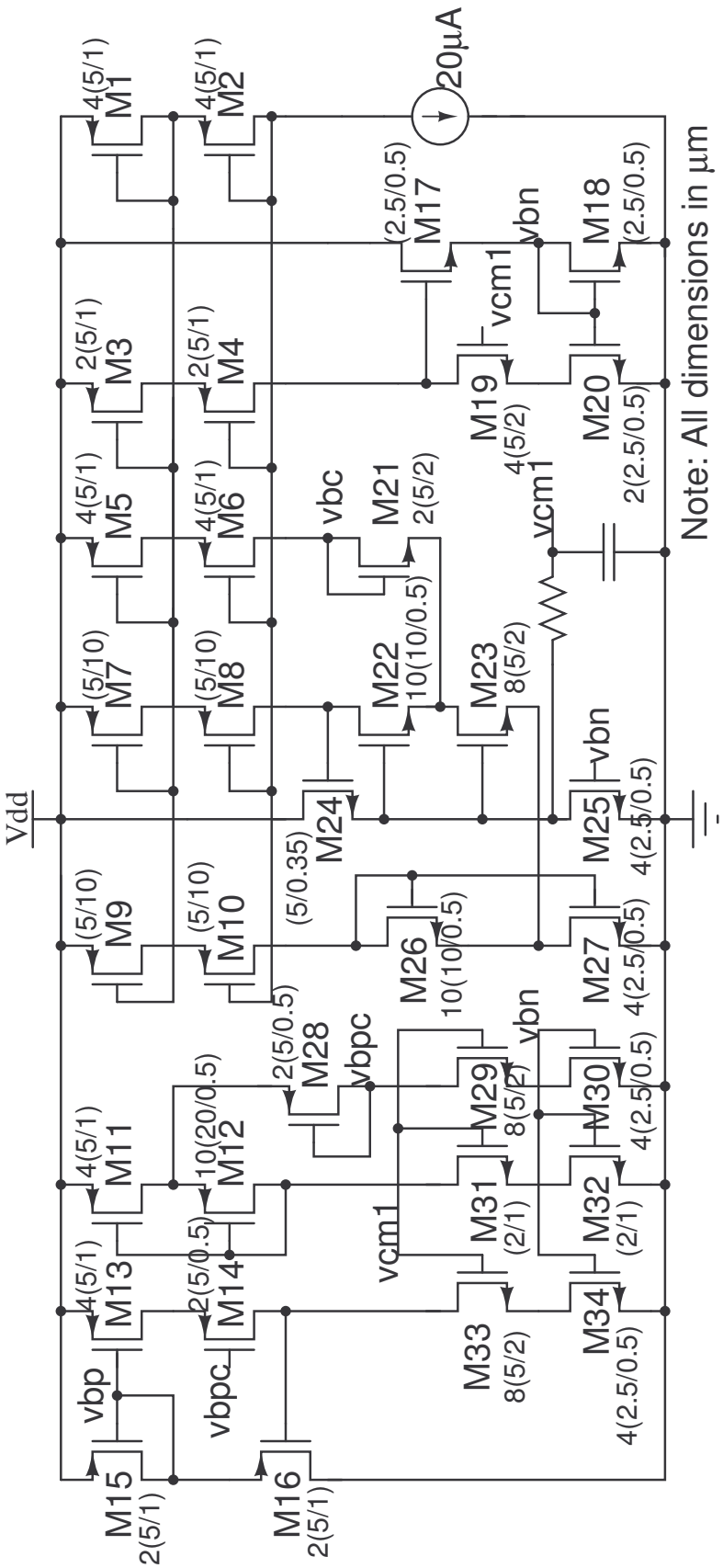


Figure 3.7: Bias circuit schematic

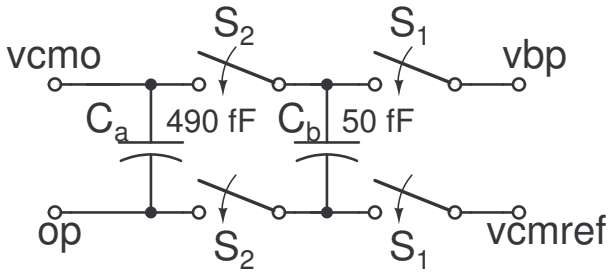


Figure 3.8: Switched capacitor common mode feedback

S_2 is ON C_b, dumps the charge it has gained during the previous phase on to C_a. Under steady state the voltage vcmo equals the voltage vbp. This voltage (vcmo) is given to the gates of M1 and M2 given in Fig. 3.6. Fig .3.9 shows that part of the

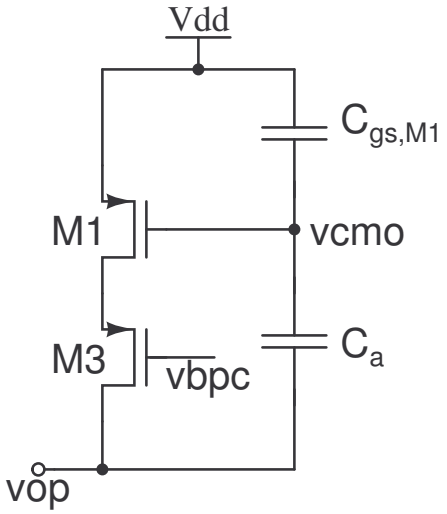


Figure 3.9: Part of circuit used for finding C_a

opamp used for finding the sizes of the common mode feedback capacitors. The purpose of C_a is to act like a fixed voltage source. So, any small change Δv in vop appears directly at the gate of M1. The negative feedback in the loop makes sure that the voltage vop changes in opposite direction, thus, stabilizing the circuit to a fixed operating point. In addition to C_a, there is a gate source capacitance of M1 ($C_{gs,M1}$) in series with C_a. The amount of Δv appearing at the gate depends on the

relative values of C_a and $C_{gs,M1}$. The more C_a the less is the attenuation of Δv. This gives a minimum value for the capacitance C_a. The value of C_b is chosen such that the output common mode settles to a final value in few cycles. This is done by adjusting the ratio of C_a and C_b.

3.4.3 Simulation results of opamp

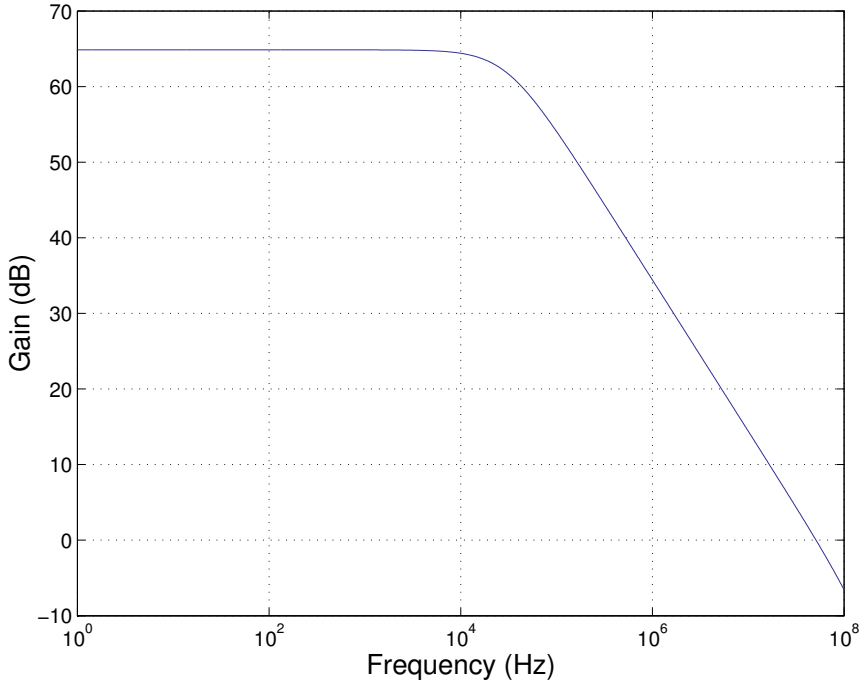


Figure 3.10: Frequency response of the opamp

Fig. 3.10 shows the frequency response for typical mean corner, of the opamp designed. The load capacitance used is 1 pF. Fig. 3.11 shows the output voltage swing of the opamp for the same typical mean corner. From the DC characterstics the values of α and β used in Section. 2.1.2 are calculated as 3.196 and 1094 respectively. Table. 3.2 shows the variation of gain for different corners. The first opamp consumes a power of 0.95 mW, while the second one consumes about 0.7 mW. A switched capacitor integrator is made from the opamp designed. The integrator is operated in open loop to check its functionality. Fig. 3.12 shows the output voltage

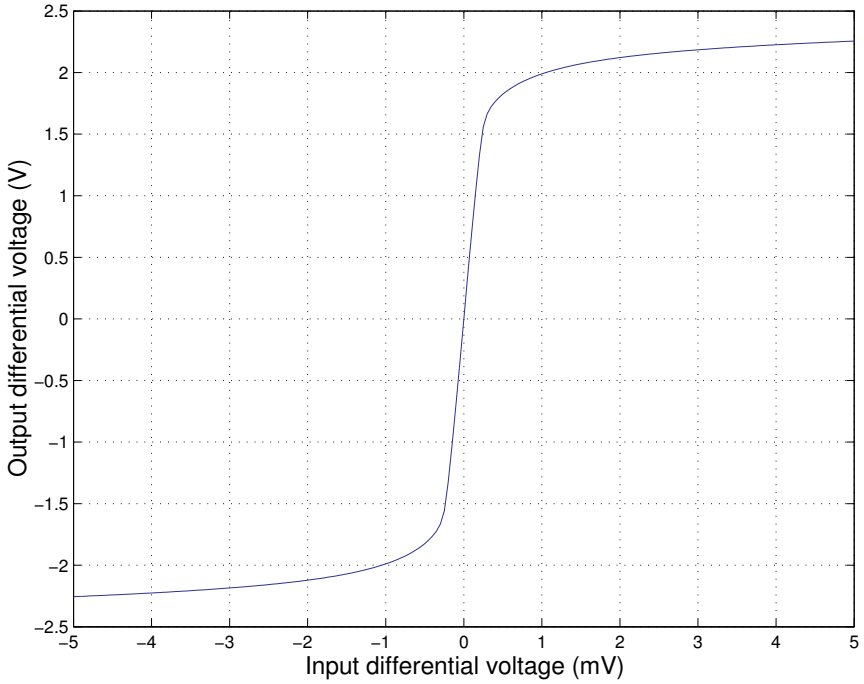


Figure 3.11: DC response of the opamp

Corner	DC gain
tt	64.86 dB
ff	64.1 dB
ss	65.49 dB
sf	64.8 dB
fs	64.9 dB

Table 3.2: DC gain of Opamp for different corners

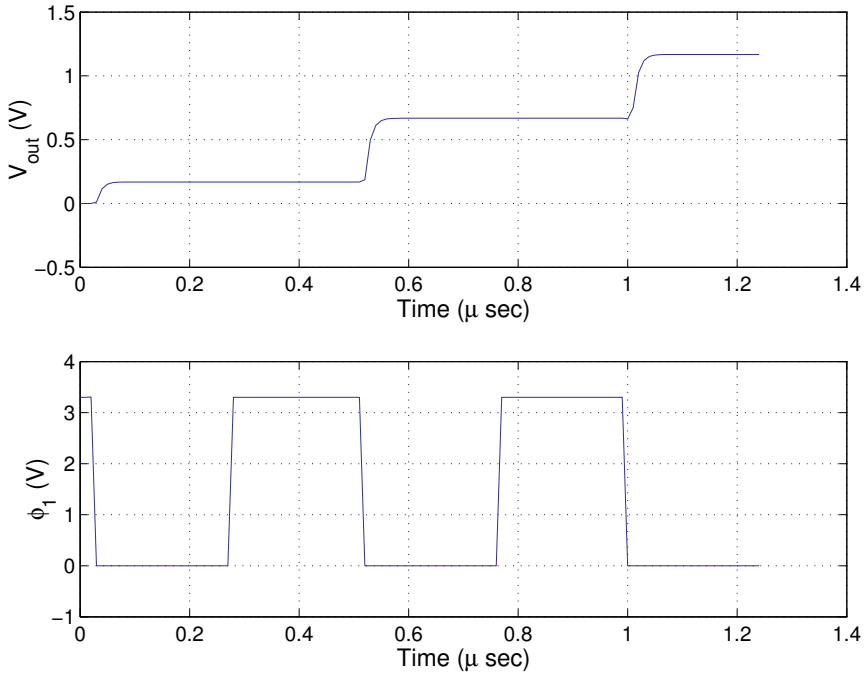
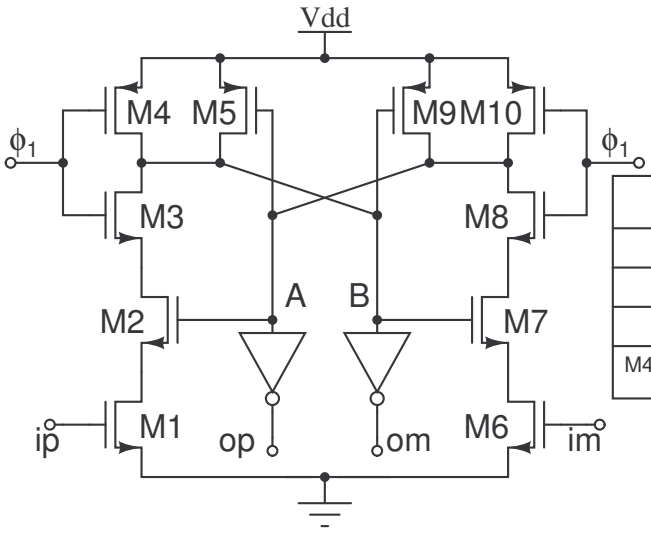


Figure 3.12: Integrator response

for a DC voltage at the input. From the figure it is observed that the output voltage settles in a few nano seconds of delay, that is well with in half the clock period.

3.5 Comparator Design

The output of the integrator is fed into the comparator. Based on the relative values of both positive and negative inputs comparator produces a valid output. The output is valid only when ϕ_1 is high. During the other phase the output of the integrator changes so the comparator should not evaluate this value. Hence, the comparator has to be disabled when the integrator is in the evaluation phase. The comparator used here is the one given in [4], the schematic of which is shown in Fig. 3.13. The circuit consists mainly of two inverters connected back to back to get regenerative feedback. Devices $M2,\ M5$ and $M7,\ M9$ serve this purpose. Transistors $M3,\ M4$ and $M8,\ M10$ from two inverters used to reset the comparator when the integrator is in the evaluation phase. When ϕ_1 is high $M3,\ M8$ are ON connect-



Transistor	W/L in μm	Fingers
M1, M6	1.5/0.5	2
M2, M7	1.5/0.5	2
M3, M8	1.5/0.5	2
M4, M5, M9, M10	1.5/0.5	2

Figure 3.13: Comparator

ing the inverters formed by $M2,\ M5$ and $M7,\ M9$ back to back. The transistors $M1$ and $M6$ operate in the triode region. Depending on *ip* and *im* the resistance seen at the source of $M1$ and $M6$ is different. Hence, there will be unequal current through inverters formed by $M2,\ M5$ and $M7,\ M9$. Since, there is a positive feedback in the circuit this inequality builds up until one of the output saturates (goes till the supply voltage). The purpose of inverters placed at nodes A and B is explained in next section. The sizes of all the devices are chosen in such a way that the delay in the comparator is minimum.

3.6 Latch Design

In the previous section the necessity for reseting the comparator was explained. When the comparator is reset once every clock period the reset value should not be fedback into the modulator again. So, it is necessary to latch the output during the reset period. The latch used is shown in Fig. 3.14. The output will be previous value if both the inputs are zero (low). This, explains the need for the two inverters being placed at the nodes A and B of the comparator. The NAND gates used are of static CMOS type. The inputs S and R to the latch are connected to the output

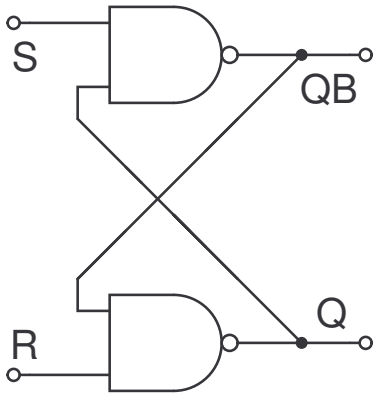


Figure 3.14: Latch

of the comparator. The output of the latch go to the external world.

3.7 Digital-To-Analog Converter Design

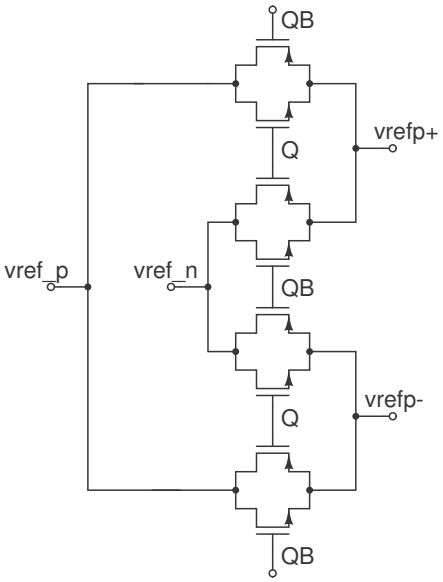


Figure 3.15: 1-bit DAC

The DAC used is a multiplexer that selects either positive or negative voltage depending on the digital output of the latch. Fig. 3.15 shows the schematic of the DAC implemented. The sizes of all PMOS devices are kept as 16/0.35 μm and

NMOS devices as 5.5/0.35 μm. The sizes were chosen so that the bottom plate of the sampling capacitor charges to the analog voltage of the DAC in a few nano seconds of delay. The gates are controlled by the output of the latch. $vref_p$ and $vref_n$ are the positive and negative analog voltages given from either bandgap voltage reference or external source.

Chapter 4

Simulation Results Of The $\Sigma\Delta$ Modulator

4.1 Simulation Results

The complete sigma delta modulator is designed in a $0.35\mu m$ CMOS process. The simulation of the system is done in CADENCE and MATLAB. A input tone of -3 dB at a frequency of 2 kHz was given. The output common mode was set at 1.65 V using an external source. The two reference voltages for the DAC were supposed to be given from the designed Bandgap. But, because of time constraints the reference voltages are also given externally. Fig. 4.1 shows the frequency spectrum of the output for the given input tone. To see the distortion and SNR till the 4 kHz bandwidth the same figure is zoomed at low frequencies and is shown in Fig. 4.2. The system is also modelled in Matlab and Fig. 4.3 shows the output spectrum obtained in Matlab.

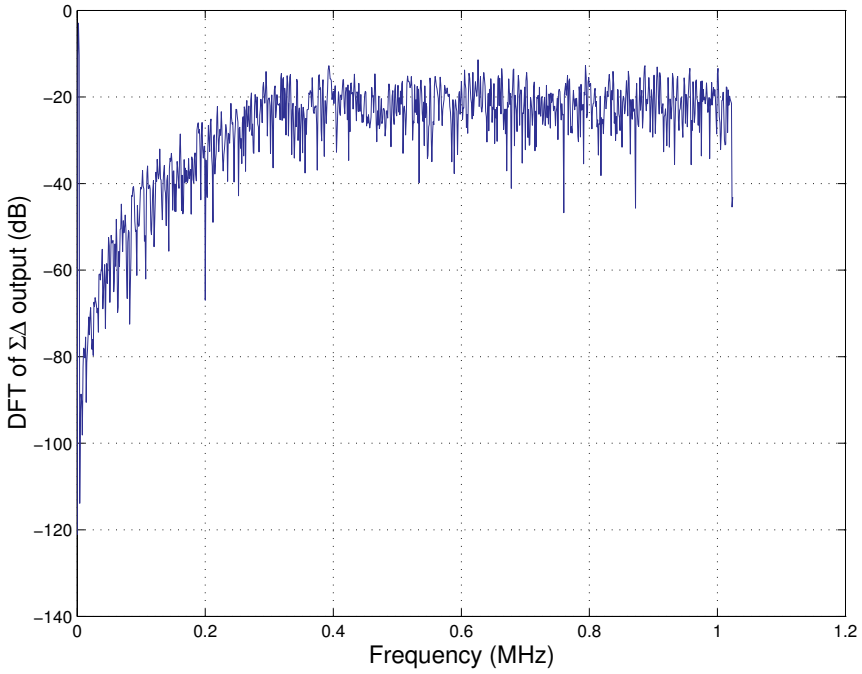


Figure 4.1: Output spectrum of $\Sigma\Delta$ obtained in Cadence

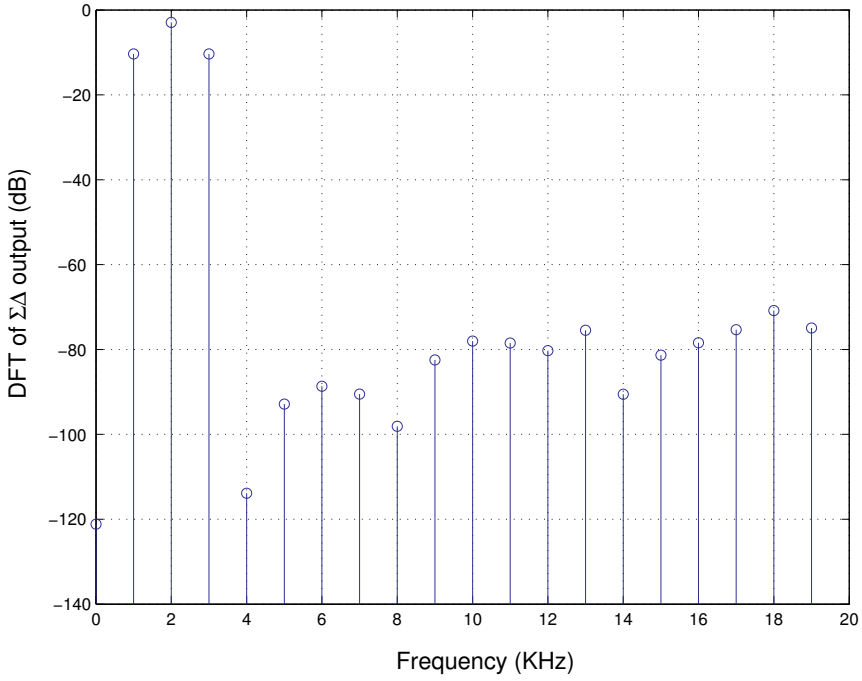


Figure 4.2: Low frequency components of output spectrum

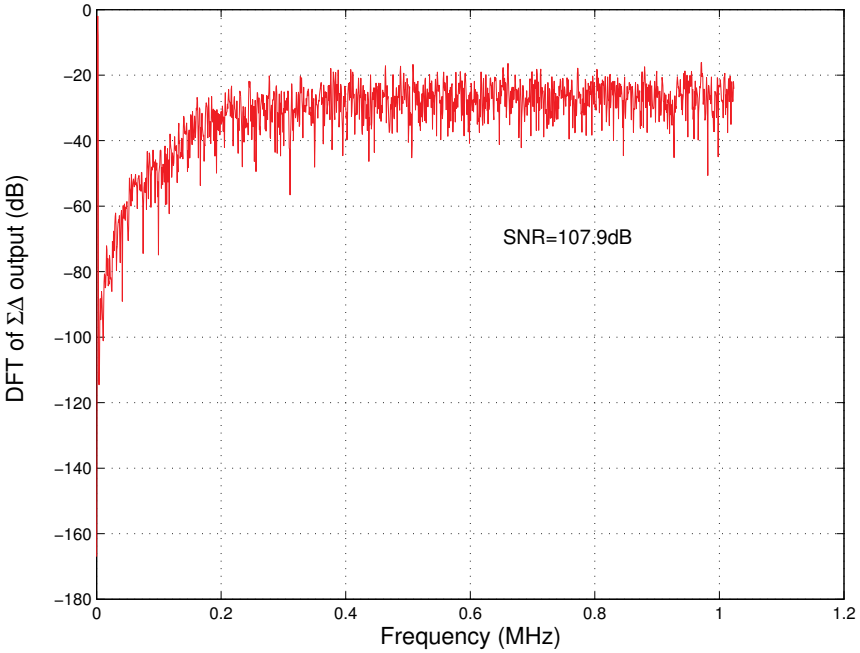


Figure 4.3: Output spectrum of $\Sigma\Delta$ obtained in Matlab

Chapter 5

Bandgap Voltage Reference Design

5.1 Introduction

There is a growing need of basic voltage reference generated on chip for almost all of the mixed signal applications. In recent years a lot of work has been done in obtaining fixed voltages for low supply voltages [6] and [7]. Most of these use an additional opamp for generating the fixed voltage. While this meets the requirement of stable voltage, still the power supply noise is not that much taken care of. An opamp less bandgap reference is given in [8]. The circuit is slightly modified so as to achieve a better stable voltage over process, temperature and noise in power supply.

5.2 Implementation Of The Circuit

This section deals with concept of generating fixed voltage reference. The section throws light on the ideas that were present in the literature.

5.2.1 Implementation using opamp in CMOS technology

In the present CMOS technology we have vertical and lateral PNP transistors in an n-well process. The base emitter junction of any of these transistors has a voltage with negative temperature coefficient. And the difference between the base emitter junction voltages of two BJTs' has a positive temperature coefficient. This is called as **P**roportional **T**o **A**bsolute **T** emperature (PTAT) voltage. Multiplying

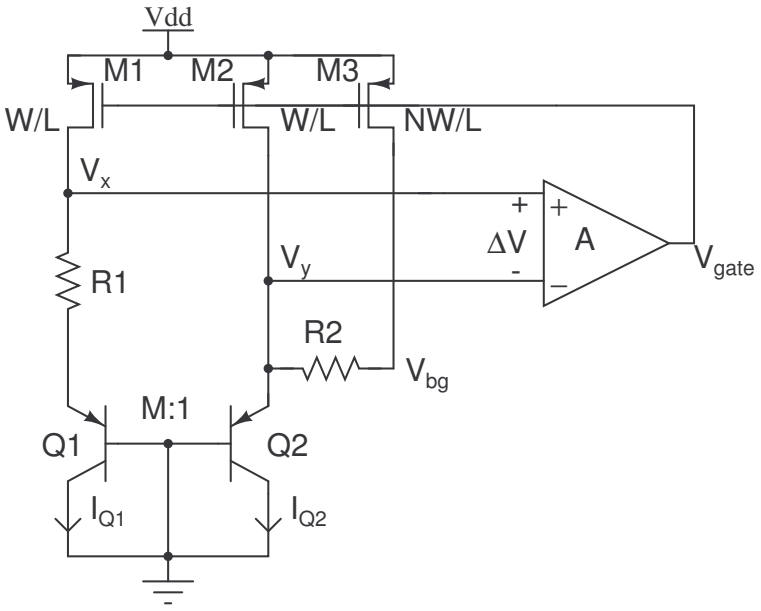


Figure 5.1: Bandgap Reference in CMOS technology

this with suitable gain we can compensate for the negative temperature coefficient of bandgap voltage of Si. The schematic of the circuit is given in Fig. 5.1. The three PMOS devices $M1$, $M2$ and $M3$ are used as current sources that pump in currents into the emitters of $Q1$ and $Q2$. Opamp maintains the voltages V_x and V_y the same. Hence, the voltage across $R1$ is equal to difference in V_{be}'s of $Q1$ and $Q2$. By having different current densities in $Q1$ and $Q2$ a PTAT voltage is generated. Hence, $R1$ has a current proportional to PTAT voltage. This current is multiplied by N so as to compensate for negative temperature coefficient voltage (V_{be}) by $M3$. Finally, the sum of v_y and the voltage across $R2$ is taken to get the required reference voltage. The mathematics involved in the circuit are described later.

5.2.1.1 Effect of variation in power supply on circuit in Fig. 5.1

$$I_{Q1} = \frac{kp}{2}\left(Vdd - A\Delta V - V_{th}\right)^2 \tag{5.1}$$

where,

$$kp = \mu_p C_{ox} W/L \tag{5.2}$$

V_{th}: threshold voltage of PMOS device

Differentiate (5.1) partially with respect to Vdd. We have,

$$\frac{\partial I_{Q1}}{\partial Vdd} = kp\left(Vdd - A\Delta V - V_{th}\right)\left(1 - A\frac{\partial \Delta V}{\partial Vdd}\right) \tag{5.3}$$

$$V_x = I_{Q1}R1 + V_t \ln\left(I_{Q1}/I_s\right) \tag{5.4}$$

where,

I_s: reverse saturation current

$$V_y = V_t \ln\left(I_{Q2}/I_s\right) \tag{5.5}$$

$$\frac{\partial V_x}{\partial Vdd} = R1\frac{\partial I_{Q1}}{\partial Vdd} + \frac{V_t}{I_{Q1}}\frac{\partial I_{Q1}}{\partial Vdd} \tag{5.6}$$

$$\frac{\partial V_y}{\partial Vdd} = \frac{V_t}{I_{Q2}}\frac{\partial I_{Q2}}{\partial Vdd} \tag{5.7}$$

$$\Delta V = V_x - V_y \tag{5.8}$$

$$\Rightarrow \Delta V = R1I_{Q1} + V_t \ln\left(\frac{I_{Q1}}{I_s}\right) - V_t \ln\left(\frac{I_{Q2}}{I_s}\right) \tag{5.9}$$

$$\frac{\partial \Delta V}{\partial Vdd} = R1\frac{\partial I_{Q1}}{\partial Vdd} + \frac{V_t}{I_{Q1}}\frac{\partial I_{Q1}}{\partial Vdd} - \frac{V_t}{I_{Q2}}\frac{\partial I_{Q2}}{\partial Vdd} \tag{5.10}$$

$$\Rightarrow \frac{\partial \Delta V}{\partial Vdd} = R1\frac{\partial I_{Q1}}{\partial Vdd} \tag{5.11}$$

Using (5.11) in (5.3) we have,

$$\frac{\partial I_{Q1}}{\partial Vdd} = g_m\left(1 - AR1\frac{\partial I_{Q1}}{\partial Vdd}\right) \tag{5.12}$$

where,

$$g_m = kp\left(Vdd - A\Delta V - V_{th}\right) \tag{5.13}$$

$$\Rightarrow \frac{\partial I_{Q1}}{\partial Vdd} = \frac{g_m}{1 + Ag_mR1} \tag{5.14}$$

$$V_{bg} = NI_{Q1}R2 + V_y \tag{5.15}$$

$$\frac{\partial V_{bg}}{\partial Vdd} = NR2\frac{\partial I_{Q1}}{\partial Vdd} + \frac{V_t}{I_{Q2}}\frac{\partial I_{Q2}}{\partial Vdd} \tag{5.16}$$

$$\Rightarrow \frac{\partial V_{bg}}{\partial Vdd} = \left(NR2 + V_t/I_{Q1}\right)\frac{\partial I_{Q1}}{\partial Vdd} \tag{5.17}$$

$$\Rightarrow \frac{\partial V_{bg}}{\partial Vdd} = \left(NR2 + V_t/I_{Q1}\right)\frac{g_m}{1 + Ag_mR1} \tag{5.18}$$

if $g_m R1 >> 1$ then,

$$\frac{\partial V_{bg}}{\partial Vdd} = (NR2 + V_t/I_{Q1}) \frac{1}{AR1} \tag{5.19}$$

From the above result it is clear that for an ideal opamp whose gain is infinite the bandgap voltage doesn't vary with the power supply. But, in practice opamp has finite gain so the circuit has finite PSRR. In the analysis above, the effect of finite output impedance of three MOS devices and the variation of opamp gain (A) with power supply, have been neglected. These terms further degrade the power supply rejection. In simple terms, the effect of power supply on the circuit can be explained as follows :

If Vdd increases then, both V_x and V_y increase. But, the negative feedback tries to restore them back to the original value. The amount which this feedback can bring V_x and V_y back to old value depends on the gain, A, of the opamp. If the gain is infinite the values are fully restored. In presence of finite gain there is slight change in values of V_x and V_y. Hence, bandgap voltage is modulated by power supply.

5.2.2 Implemented circuit

The bandgap circuit implemented here is given in [8]. This circuit is slightly modified to meet the required specifications and is given in Fig. 5.2. The error in voltage between node 1 and node2 is sensed and is fed back to the source of the $M1$ through the cascode amplifier formed by $M4 - M7$. The circuit being selfbiased needs a startup circuitry. This is formed by the transistors $M18 - M20$. The transistors $M18$ and $M20$ forms an inverter that sense the voltage at the transistor $M23$. When this transistor conducts the output of the inverter that is the gate of $M19$ goes low, disconnecting the start up circuit from the main circuit. On the other hand, when the circuit is at 0 operating point the output of the inverter is high. Thus, $M19$ is turned ON, which inturn takes current from drain of $M13$. This starts up the circuit. Two resistors are kept at the drains of $M1$ and $M2$ so as to create the same environment that is there for $M3$. This ensures that currents are mirrored in a better way, which is essential for the compensation. The equations governing the operation of the circuit are given in next section. The circuit is laid in

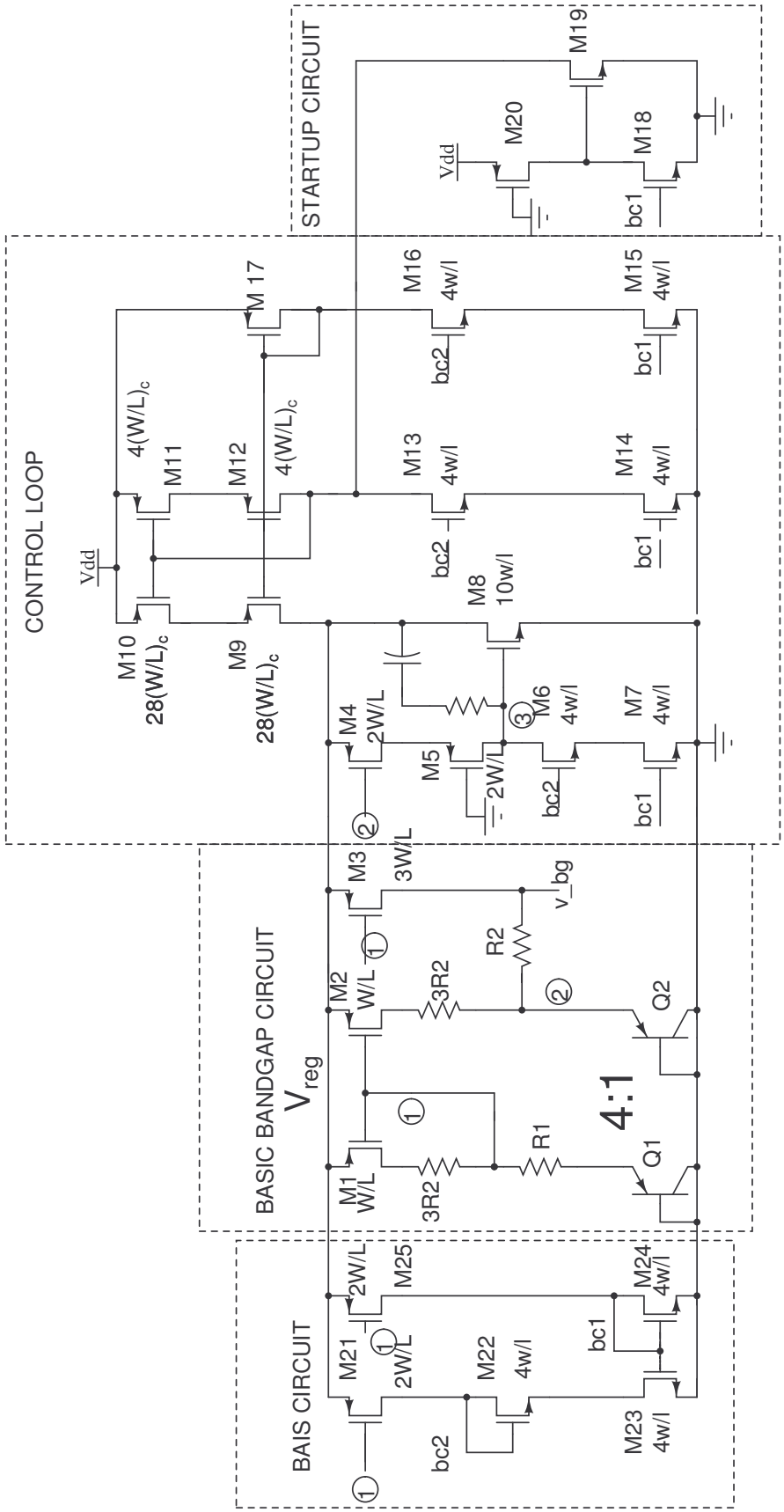


Figure 5.2: Complete Bandgap Reference

0.35 μm AMS process. Dummy devices are placed where ever current mirroring is required. This was essential so as to create same environment as that of the master devices. The BJTS are replaced with MOS diodes since BJT's were not available in the technology being used.

5.2.2.1 Effect of variation in power supply on circuit in Fig. 5.2

In the circuit shown in Fig. 5.2, the supply is not directly connected to sources of M1, M2 and M3, but, rather connected to a cascode PMOS pair. The voltage coming at the source of the transistors is much more stable to the power supply variation than that of the one in Fig. 5.1. So, we have a better power supply rejection. This is explained below :

Detailed analysis of the equations derived here is given later

Assume Vdd changes by ΔV. Then, the change in V_{reg} is given by

$$v_{reg} = g_{M10} r_{reg} \tag{5.20}$$

where, r_{reg} is the impedance looking into node v_{reg}

$$i_{M1} = \frac{v_{reg}}{1/g_{M1} + R1 + r_{e1}} \tag{5.21}$$

$$v_2 = \frac{v_{reg}}{1/g_{M1} + R1 + r_{e1}} r_{e1} \tag{5.22}$$

$$\Rightarrow i_{M4} = g_{M4} v_{reg} \text{ (approximately)} \tag{5.23}$$

$$\Rightarrow v_3 = \left(g_{M4} - \frac{2}{1/g_{M1} + R1 + r_{e1}} \right) r_3 v_{reg} \tag{5.24}$$

$$i_{M8} = g_{M8} v_3 \tag{5.25}$$

$$\Rightarrow i_{M8} = g_{M8} \left(g_{M4} - \frac{2}{1/g_{M1} + R1 + r_{e1}} \right) r_3 v_{reg} \tag{5.26}$$

$$r_{reg} = v_{reg}/i_{M8} \tag{5.27}$$

From the above two equations we see that the value of r_{reg} is very low. So, the variation of (5.20) with power supply is very low. Hence, we have a better power supply rejection. If the bodies of PMOS devices are connected to Vdd then any variation in the supply will change the threshold of the device and hence modulate

the current. So, PSRR is reduced. This is prevented by connecting the bodies of the PMOS devices to their respective sources and thus cancelling the body effect. PSRR is further increased by the cascode pair formed by $M9 - M12$.

5.3 Expressions For Bandgap Voltage And Loopgain

5.3.1 Calculation of the bandgap voltage

In this section the bandgap voltage compensation for temperature is calculated. Some of the terms which are used in the present section

I_S: transistor reverse saturation current

V_{G0}: bandgap voltage of silicon extrapolated to 0 K (approximately 1.206)

k: Boltzmann constant

q: charge of the electron

T_0: reference temperature

J_C: collector current density at temperature T

J_{C0}: collector current density at temperature T_0

From [10]

$$V_{be} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right) \tag{5.28}$$

From (5.28), the difference in the base emitter voltage of two transistors having different current densities has positive temperature coefficient. Multiplying, this difference in voltage by some factor say N we can compensate for the negative temperature coefficient of the bandgap voltage. This is done in Fig. 5.1. Referring to Fig. 5.1

$$\Delta V_{be} = \frac{kT}{q}\ln\left(\frac{(N+1)\,A_{Q1}}{A_{Q2}}\right) \tag{5.29}$$

$$V_{bg} = \frac{R2}{R1}\Delta V_{be} + V_{be2} \tag{5.30}$$

For the implemented circuit (see Fig. 5.2) the fixed voltage can be derived as follows

$$I_{R1} = \frac{V_1 - V_{be1}}{R1} \tag{5.31}$$

The control loop makes sure that the voltage at node 1 and 2 are both the same.

$$\Rightarrow I_{R1} = \frac{V_2 - V_{be1}}{R1} \tag{5.32}$$

since, M1 and M3 have same gate to source voltages. Neglecting their V_{ds} difference, one can write

$$I_{M3} = 3\, I_{R1} \tag{5.33}$$

$$V_{bg} = I_{M3} R2 + V_{be2} \tag{5.34}$$

From (5.33) & (5.32)

$$V_{bg} = 3\, R2 \frac{(V_2 - V_{be1})}{R1} + V_{be2} \tag{5.35}$$

$$\Rightarrow V_{bg} = \frac{3\, R2}{R1} \left(\frac{kT}{q}\right) \ln(16) + V_{be2} \tag{5.36}$$

5.3.2 Calculation of loop gain

Open the loop at node v_{reg}

At node 3, we have

$$v_3 = (v_2 - v_{reg})\, g_{M4} r_3 \tag{5.37}$$

$$i_{M8} = v_3 g_{M8} \tag{5.38}$$

$$i_{M1} = \frac{v_{reg}}{1/g_{M1} + R1 + r_{e1}} \tag{5.39}$$

$$v_2 = i_{Q2} r_2 \tag{5.40}$$

where, r_2 is parallel combination of r_{e1}, $r_{ds_{M2}}$ and $R2$ and $r_{ds_{M3}}$. This is approximately equal to r_{e2}.

$$\Rightarrow v_2 = i_{M1} r_{e1} \tag{5.41}$$

Since i_{M2}=4 i_{M1} and r_{e1}=4 r_{e2}

$$v_2 = \frac{v_{reg}}{1/g_{M1} + R1 + r_{e1}} r_{e1} \tag{5.42}$$

$$i_{M4} = g_{M4} (v_{reg} - v_2) \tag{5.43}$$

From (5.42) & (5.43)

$$i_{M4} = g_{M4} v_{reg} \left(1 - \frac{r_{e1}}{1/g_{M1} + R1 + r_{e1}}\right) \tag{5.44}$$

$$\Rightarrow i_{M4} = g_{M4} v_{reg} \text{ (approximately)} \tag{5.45}$$

From this v_3 can be written as

$$v_3 = (i_{M4} - i_{M7})\, r_3 \tag{5.46}$$

where r_3 is equal to parallel combination of $g_{M5} r_{ds4} r_{ds5}$ and $g_{M6} r_{ds7} r_{ds6}$.

$$i_{M7} = 2\, i_{M1} \tag{5.47}$$

$$\Rightarrow v_3 = \left(g_{M4} - \frac{2}{1/g_{M1} + R1 + r_{e1}}\right) r_3 v_{reg} \tag{5.48}$$

$$v_{reg} = g_{M8} v_3 r_{reg} \tag{5.49}$$

where r_{reg} is the impedance at node v_{reg}

From above two equations the loopgain A_v can be written as follows:

$$A_v = g_{M8} r_{reg} r_3 \left(g_{M4} - \frac{2}{1/g_{M1} + R1 + r_{e1}}\right) \tag{5.50}$$

5.4 Simulation Results

The circuit is implemented in 0.35 μm CMOS technology and the simulation results are presented below. The variation of bandgap voltage over temperature for

Corner	Bandgap variation over 70 ^oC	PSRR
tt	5.5 mV	-110 dB
ff	2 mV	-101 dB
ss	6 mV	-107 dB
sf	20 mV	-102 dB
fs	4 mV	-90 dB

Table 5.1: Bandgap output variation for different corners

the typical mean corner is given in Fig. 5.3. Parabolic nature is observed in the

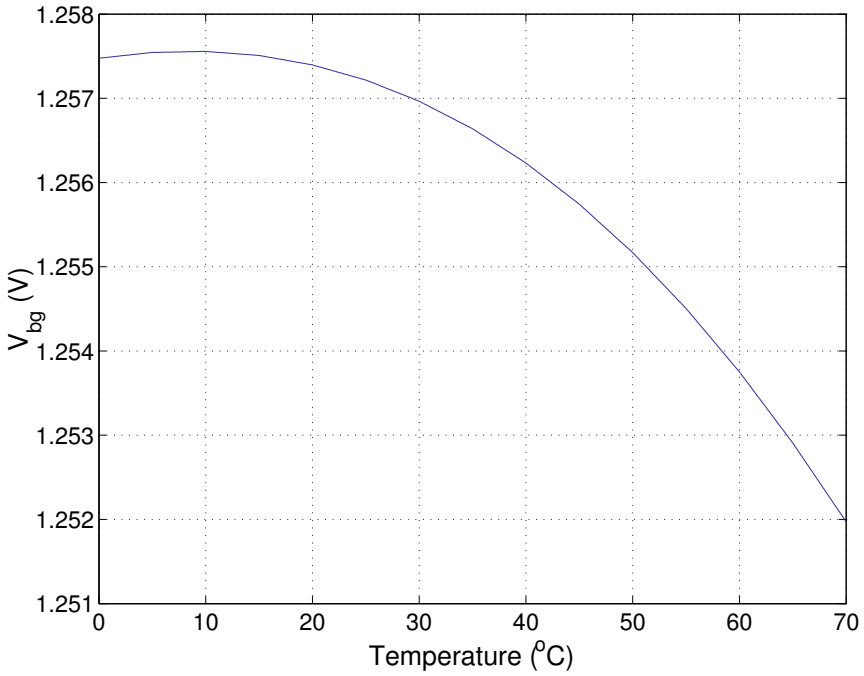


Figure 5.3: Bandgap voltage as a function of temperature

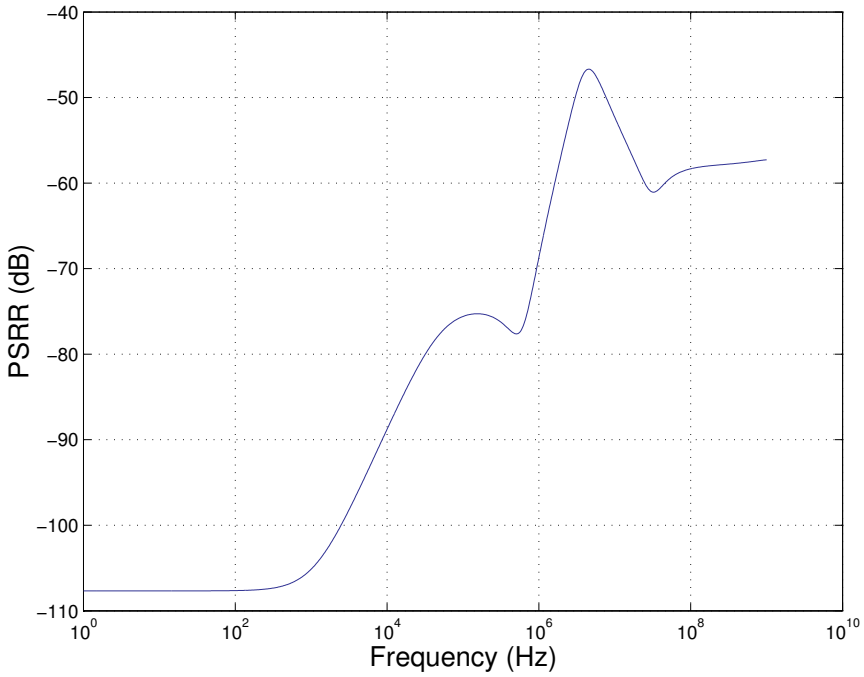


Figure 5.4: Variation of bandgap voltage with power supply

bandgap voltage. This is due to the higher order temperature dependent terms that are not cancelled by the PTAT voltage. The power supply rejection ratio is plotted in Fig. 5.4. The plot shows that the variation of bandgap voltage is more than 40 dB over 10 MHz that is around 10 mV for 1 V change in supply. This high rejection was possible mainly due to the design considerations adopted in Section. 5.2.2.

5.5 Deviations From The Expected Performance

This section covers the sources of errors that are encountered and measures to avoid them. The first source of error occurs in current mirroring. That is the currents in $M1$ and $M3$ are not the same. This is due to the difference in their V_{ds}. This in turn introduces an offset error in the voltages V_1 and V_2. This has to be included in (5.36). The equation is again quoted here including the offset term

$$V_{bg} = \frac{3\,R2}{R1}\left(\frac{kT}{q}\ln(16) + V_{offset}\right) + V_{be2} \tag{5.51}$$

To get the exact matching of the currents, V_{offset} has to be small compared to the other term inside the brackets. This is ensured by pumping more current through $M3$ or increasing the ratio of the areas of $Q1$ and $Q2$ or both. This simultaneously ensures that the spread in the resistors $R1$ and $R2$ is also reduced to get the compensation. Increasing the lengths of devices also reduces offset. Implementing all these strategies the V_{offset} was 0.6 mV while ΔV_{be} was about 70 mV. The second source of error is the noise introduced due to the various transistors and the resistors in the circuit. The major contribution is from diode connected transistors $Q1$ and $Q2$. To reduce the noise higher currents are used. This increases the power consumption. So, choice has to be made between the two. The equivalent output refered noise was found to be 0.3 mV. This value can also be included in (5.51) and the exact expression can be obtained. One important thing that has to be taken care of is the stability of the circuit. This is a concern because there are two high gain stages. Hence, it is likely that the circuit might oscillate. This is avoided using the lead compensation technique given in [3].

Chapter 6

Layout Of The Chip

6.1 Layout

Fig. 6.1 shows the die photo of the chip obtained after fabrication. The die photo contains bandgap voltage reference, $\Sigma\Delta$ modulator and a 5^{th} order switched capacitor filter.

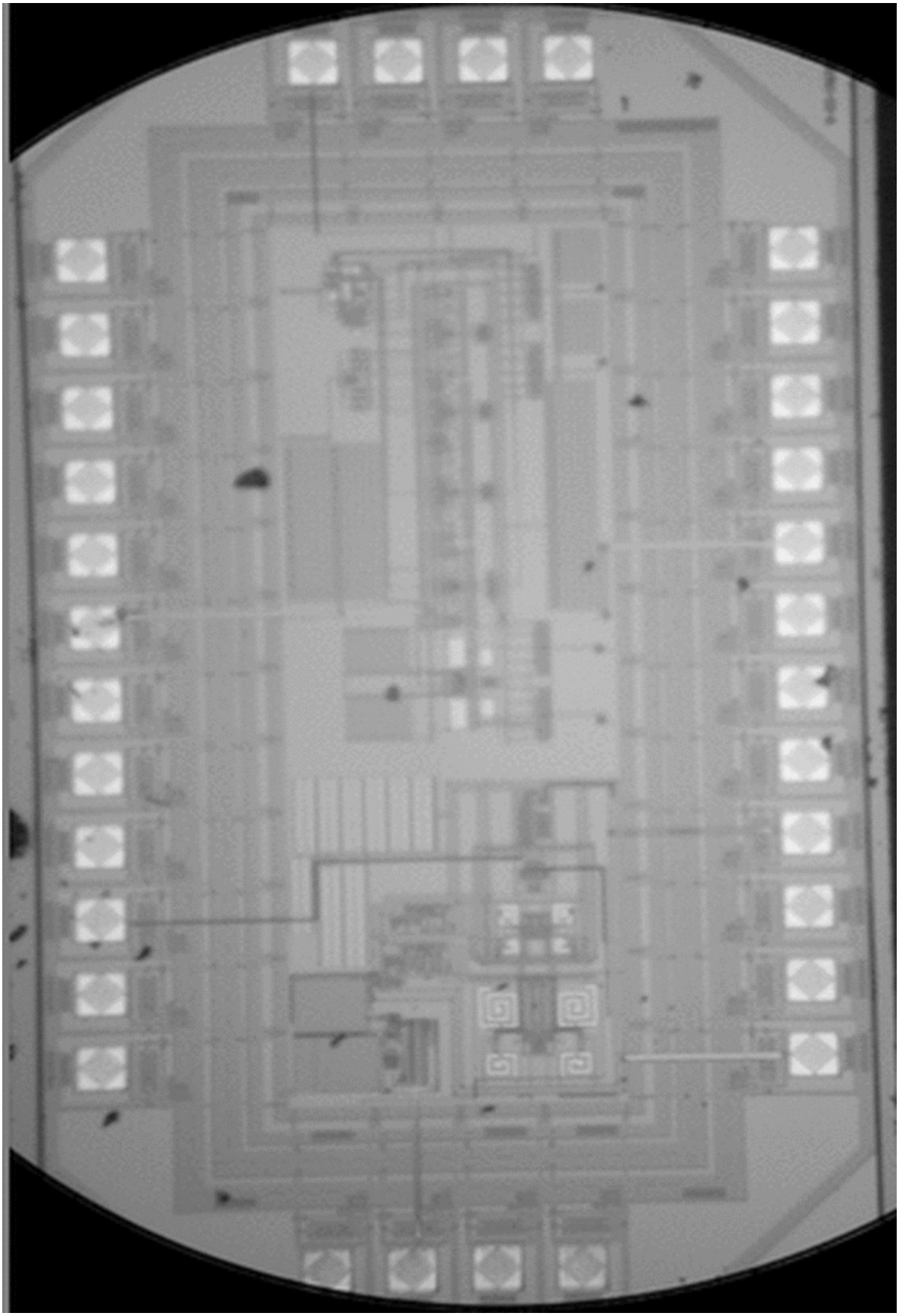


Figure 6.1: Die photograph of the chip

Chapter 7

Testing Of The Chip

7.1 Packaging The Chip

The chip sent for fabrication had 32 - pins. The packaging available was of only 28 - pins. So some of the pins that are left unused on the chip are not connected in the package. The mapping of the pins both on the chip and the package is given in Fig. 7.1. Table . 7.1 gives the pin details of the chip.

7.2 PCB Design For Testing The Chip

Fig. 7.2 shows the block diagram to test the chip. AAB_MSP_CHIP is the chip that contains the designed bandgap voltage reference and the $\Sigma\Delta$ modulator. The reference clock for generating the two phase non overlapping clocks is generated in the master clock block using a crystal. Fig. 7.3 shows the schematic for the master clock generation. The input for the modulator need to be differential. The available source is single ended. So a single ended to differential converter is made whose schematic is shown in Fig. 7.4. All the voltage references viz vcmref,vref_p, vref_n are generated form the supply using resistor ladder. The realization of these references is shown in Fig. 7.5. The master current source for the bias circuit is obtained using LM334. To prevent the loading of the measurement system on the chip, buffers are placed at the bandgap voltage reference output and the modulator output. Fig. 7.6 shows the schematic of the printed circuit board design (PCB) used for testing the chip. The purpose of various IC's used in the design is given in

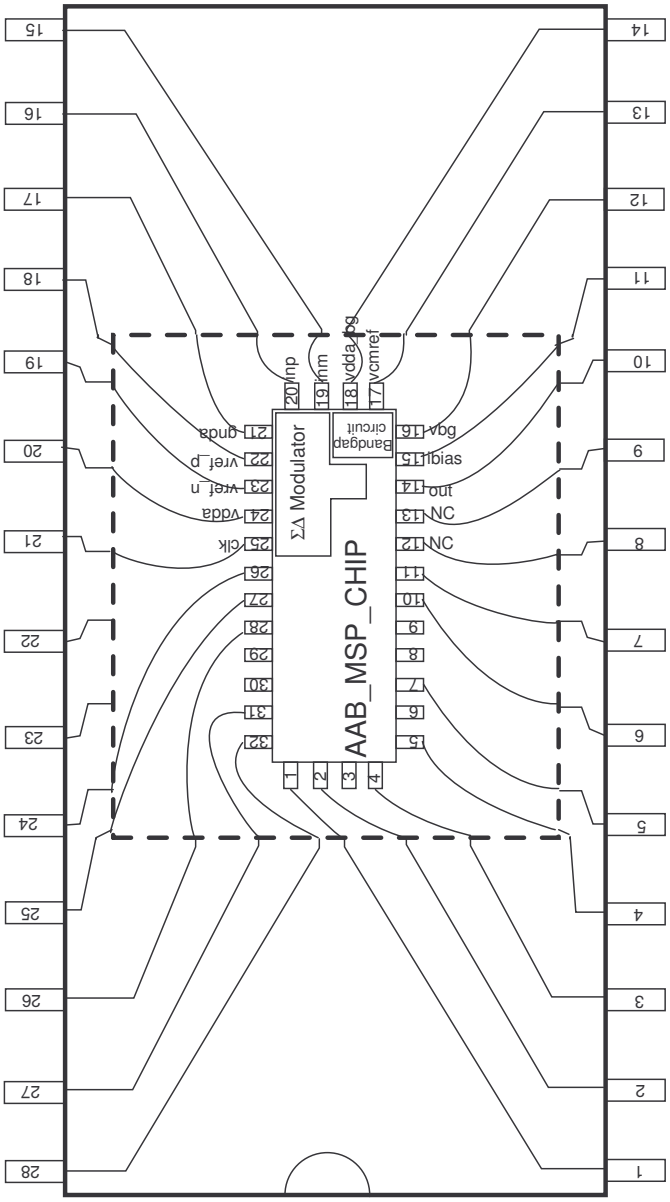


Figure 7.1: Bonding diagram for the package

Pin No	Name	Description
1-7		Filter Pins (Not used here)
8	NC	No connection
9	NC	No connection
10	out	Output of Modulator
11	ibias	Master current source
12	vbg	Bandgap voltage reference output
13	vcmref	Output common mode reference for opamp
14	vdda	positive supply for bandgap circuit
15	vim	negative input for modulator
16	vip	positive input for modulator
17	gnda	common ground
18	vref_p	positive reference for DAC
19	vref_n	negative reference for DAC
20	vdda	positive supply for modulator
21	clk	clock for the modulator
22-28		Filter Pins (Not used here)

Table 7.1: Pin details for the chip

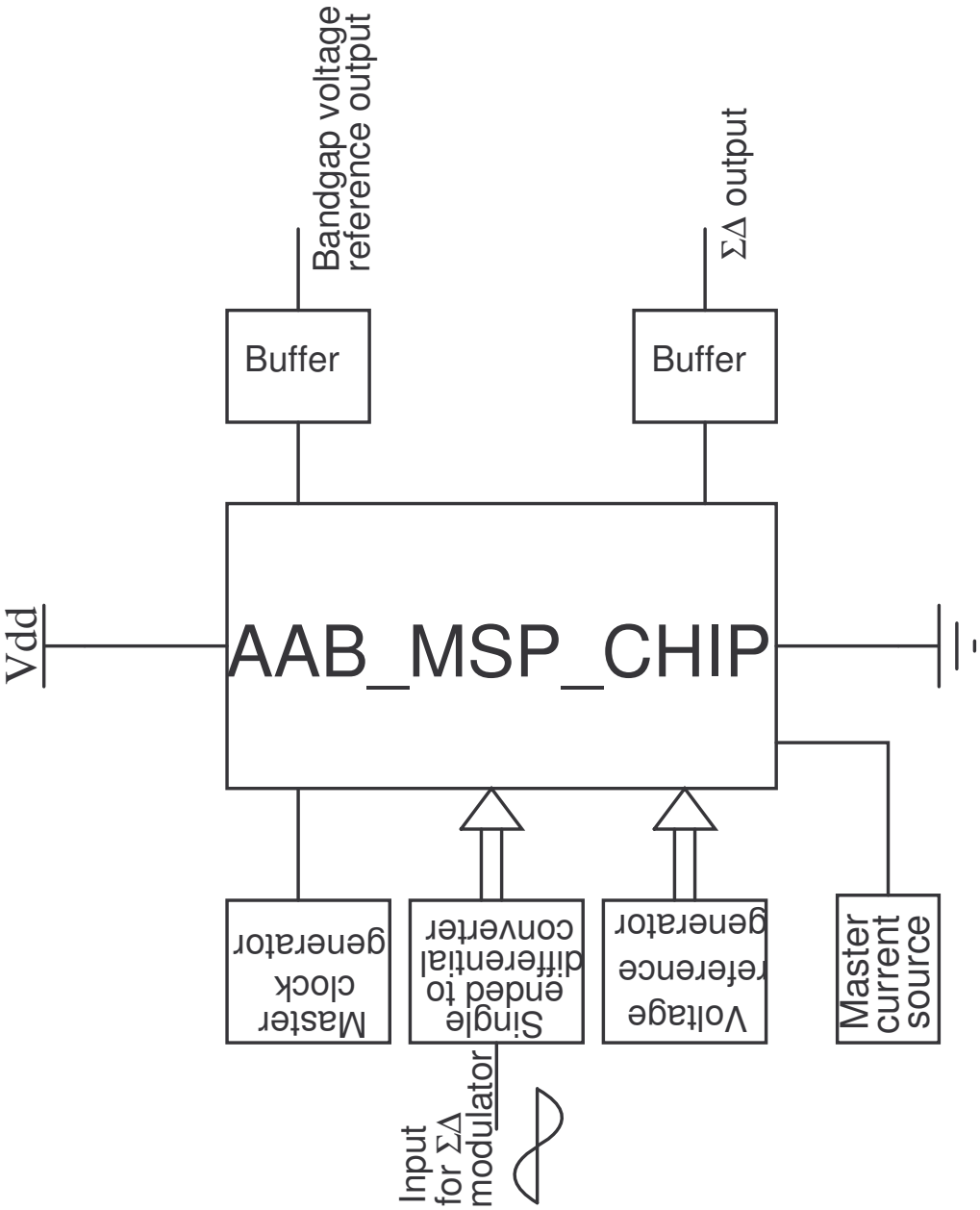


Figure 7.2: Block diagram for testing

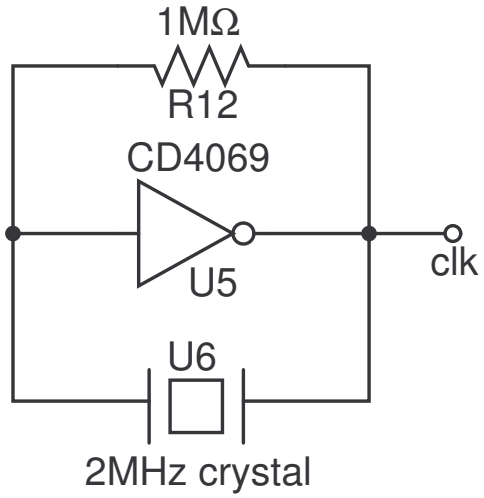


Figure 7.3: Reference clock realization

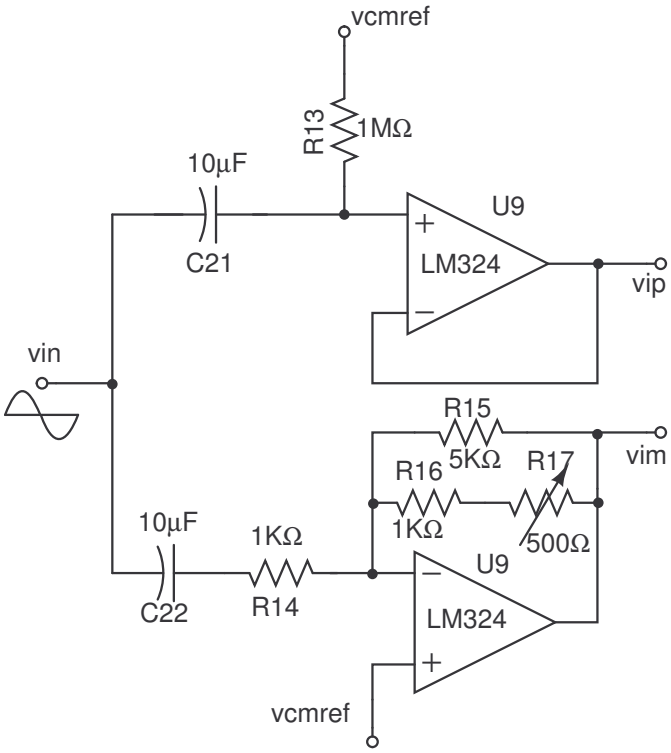


Figure 7.4: Single ended to Differential conversion

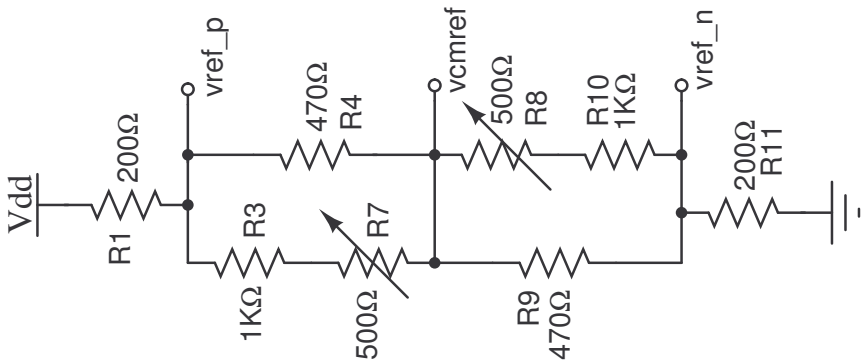


Figure 7.5: Voltage reference generation

Table. 7.2. All the ICs need bypass capacitors for their supplies. So, two capcitors

Component	Purpose
AAB_MSP_CHIP	Designed chip containing $\Sigma\Delta$ modulator and Bandgap voltage reference
LM324	Single ended opamp used as a buffer at the output of bangap reference and in single ended to differential conversion
LM334	Current reference used for generating the master bias current
74HC04	Hex inverter used as a buffer at the output of $\Sigma\Delta$ modulator
CD4069	Hex inverter used in the crystal oscillator circuit
RCA	Connector for giving input to the modulator
Single ended to differential converter	Converts single ended input for modulator to differential input
Master clock generator	Clock for generating the non overlapping clocks for the modulator
Voltage reference generator	Generates voltages vcmref, vref_p and vref_n for the modulator

Table 7.2: ICs used in the PCB

of value 10 μF and 0.01 μF are placed in parallel between positive supply for the IC and its ground. The high value acts for low frequencies and the lower one for higher frequencies. The references viz *vcmref, vref_p, vref_n* are also bypassed. The numbering of the various components used in the PCB is described in the Table. 7.3.

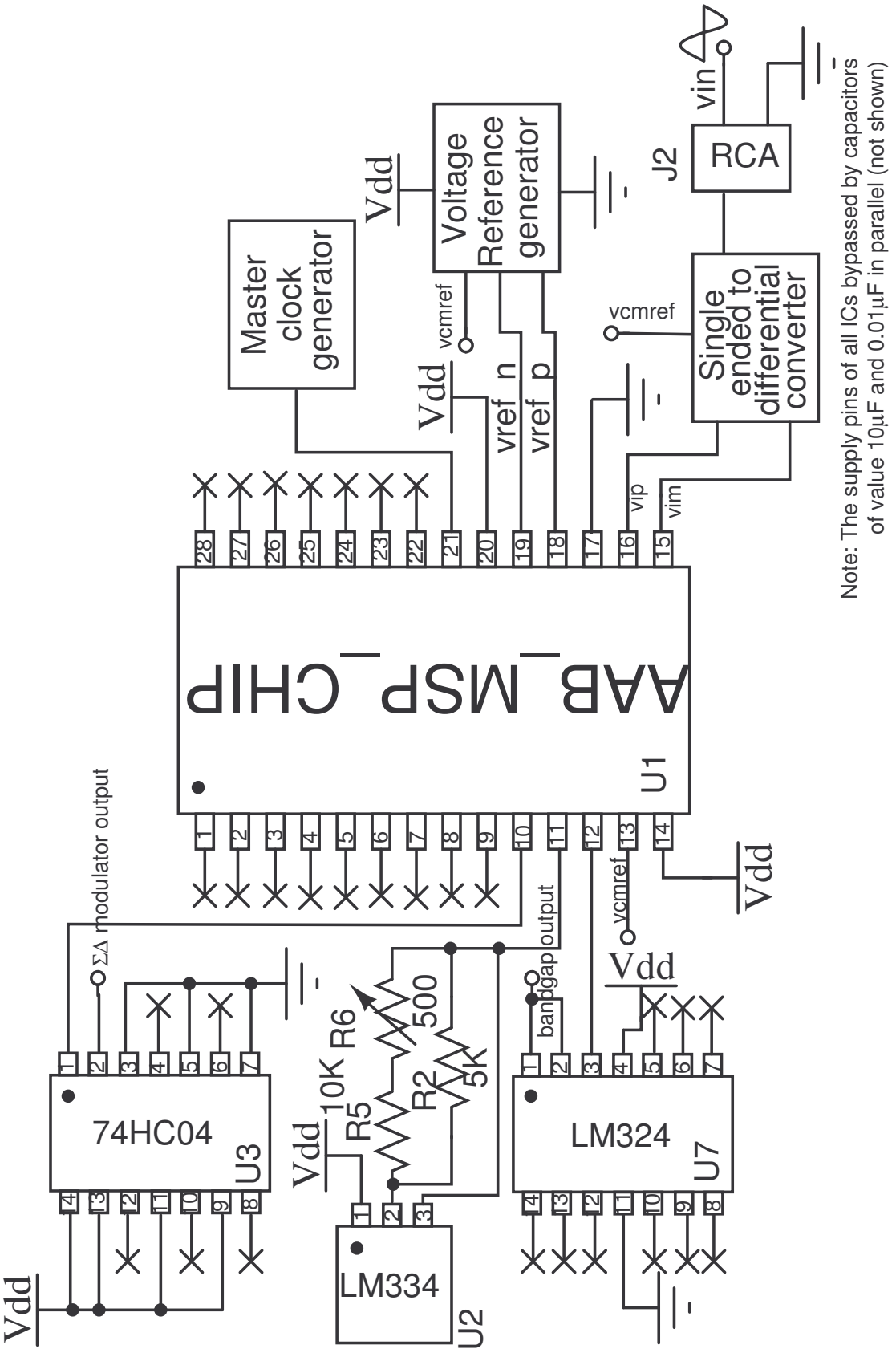


Figure 7.6: PCB schematic for testing

Component No	Description
U1	Main chip
U2	LM334
U3	74HC04
U4	POD for modulator output
U5	CD4069
U6	Crystal
U7	LM324(Buffer for bandgap)
U8	POD for bandgap
U9	LM324(for single ended to differential conversion)
R1, R3, R4, R7-R11	Resistors used for voltage references
R5, R2, R6	Resistors used for current generation(LM334)
R12	Resistance used in clock generation R13-R17 Resitors used in single ended to differential conversion
C1-C8, C10, C12	Supply bypass capacitors
C15-C20	Bypass capacitors for voltage references

Table 7.3: Component numbers given by Orcad for the PCB

Chapter 8

Blocks used in Cadence

8.1 msp_delsig_TOP

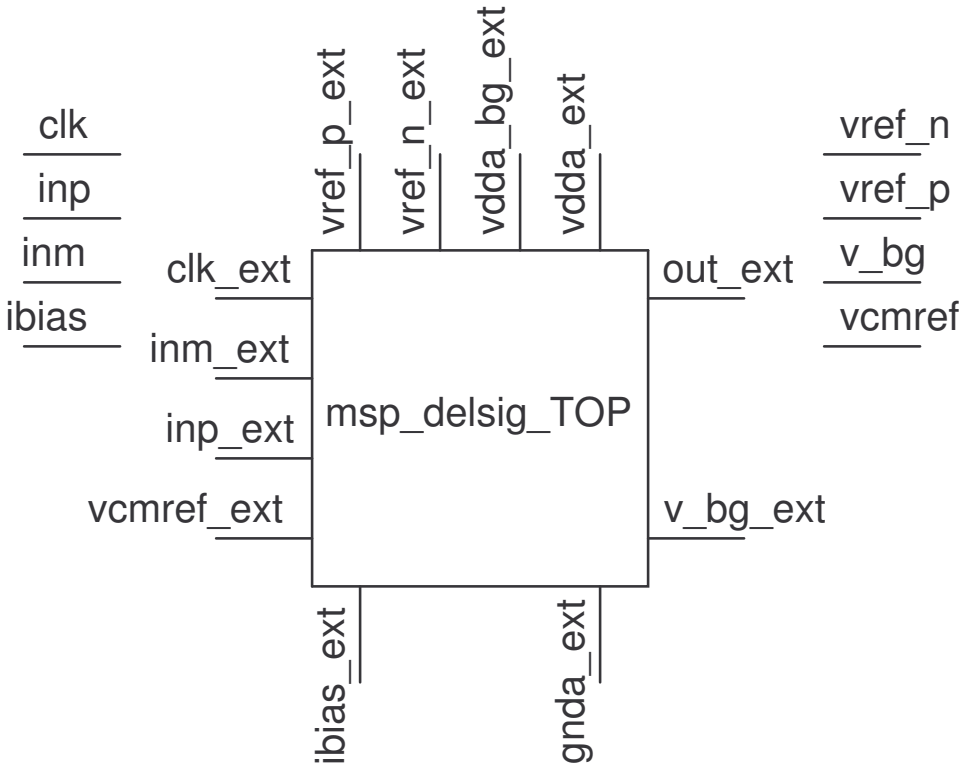


Figure 8.1: msp_delsig_TOP

Top level module includes, $\Sigma\Delta$ modulator and the bandgap modules with the pads.

Pin	Type	Description
inp	input-output	positive input voltage (inside chip, not connected)
inm	input-output	negative input voltage (inside chip, not connected)
inp_ext	input-output	positive input voltage (to be connected outside)
inm_ext	input-output	negative input voltage (to be connected outside)
clk	input-output	master clock (inside chip, not connected)
clk_ext	input-output	master clock (to be connected outside)
ibias	input-output	master current source (inside chip, not connected)
ibias_ext	input-output	master current source (to be connected outside)
vcmref	input-output	common mode reference voltage (inside chip, not connected)
vcmref_ext	input-output	common mode reference voltage (to be connected outside)
vref_p	input-output	positive reference voltage for DAC (inside chip, not connected)
vref_n	input-output	negative reference voltage for DAC (inside chip, not connected)
vref_p_ext	input-output	positive reference voltage for DAC (to be connected outside)
vref_n_ext	input-output	negative reference voltage for DAC (to be connected outside)
v_bg	input-output	bandgap output voltage (inside chip, not connected)
v_bg_ext	input-output	bandgap output voltage (to be connected outside)
out_ext	input-output	$\Sigma\Delta$ modulator output voltage (to be connected outside)
vdda_bg_ext	input-output	suppply voltage for bandgap circuit (to be connected outside)
vdda_ext	input-output	supply voltage for $\Sigma\Delta$ modulator (to be connected outside)
gnda_ext	input-output	common ground for the entire chip (to be connected outside)

Table 8.1: msp_delsig_TOP

8.1.1 msp_2ndorder_sig

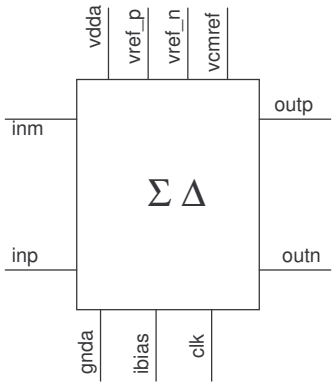


Figure 8.2: msp_2ndorder_sig

Second order $\Sigma\Delta$ modulator

Pin	Type	Description
inm	input-output	positive input voltage
inp	input-output	negative input voltage
vdda	input-output	positive supply voltage
gnda	input-output	analog ground
outp	input-output	positive output voltage
outn	input-output	negative output voltage
vref_p	input-output	positive reference voltage for the DAC
vref_n	input-output	negative reference voltage for the DAC
vcmref	input-output	common mode reference voltage for opamp
ibias	input-output	bias current for opamp
clk	input-output	master clock

Table 8.2: msp_2ndorder_sig

8.1.1.1 msp_1st_integrator

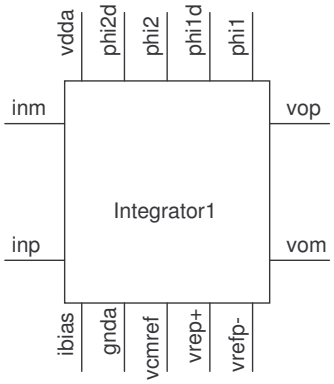


Figure 8.3: msp_1st_integrator

First switched capacitor integrator of the $\Sigma\Delta$ modulator

Pin	Type	Description
inm	input-output	positive input voltage
inp	input-output	negative input voltage
vdda	input-output	positive supply voltage
gnda	input-output	analog ground
vop	input-output	positive output voltage
vom	input-output	negative output voltage
vrefp-	input-output	negative feedback voltage from DAC
vrefp+	input-output	positive feedback voltage from DAC
vcmref	input-output	common mode reference voltage
ibias	input-output	bias current for opamp
phi1	input-output	clock for the switched capacitor integrator
phi1d	input-output	advanced version of phi1
phi2	input-output	clock non overlapping with phi1
phi2d	input-output	advanced version of phi2

Table 8.3: msp_1st_integrator

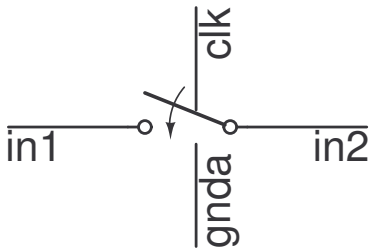


Figure 8.4: msp_switch

8.1.1.1.1 msp_switch Switch used in the integrators

Pin	Type	Description
clk	input-output	clock for controlling the switch
gnda	input-output	ground
in1	input-output	input/output of the switch
in2	input-output	input/output of the switch

Table 8.4: msp_switch

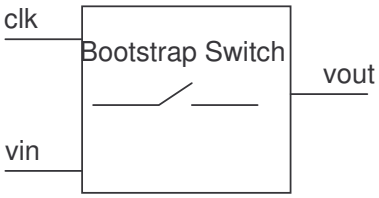


Figure 8.5: msp_bootstrap_switch

8.1.1.1.2 msp_bootstrap_switch A switch similar to a bootstrap switch. Used in 1st integrator.

Pin	Type	Description
vin	input-output	input voltage
vout	input-output	output voltage
clk	input-output	clock

Table 8.5: msp_bootstrap_switch

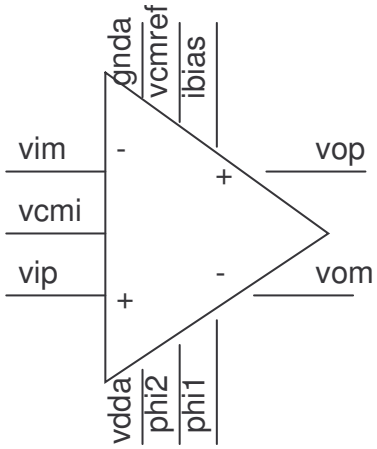


Figure 8.6: msp_opamp1

8.1.1.1.3 msp_opamp1 Opamp used in switched capacitor integrator. Two different opamps used. Both have the same pins.

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
vip	input-output	input positive voltage
vim	input-output	input negative voltage
vcmi	input-output	common mode input voltage generated by bias circuit
vop	input-output	output positive voltage
vom	input-output	output negative voltage
vcmref	input-output	output common mode reference voltage
phi1	input-output	clock for common mode feedback circuit
phi2	input-output	clock for common mode feedback circuit
ibias	input-output	master current for the bias circuit

Table 8.6: msp_opamp1

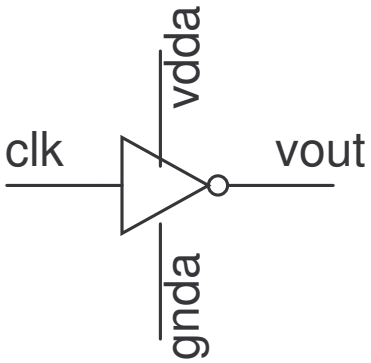


Figure 8.7: msp_sig_inv

8.1.1.1.4 msp_sig_inv Inverter used in both integrators for the switches

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
clk	input-output	inverter input
vout	input-output	inverter output

Table 8.7: msp_sig_inv

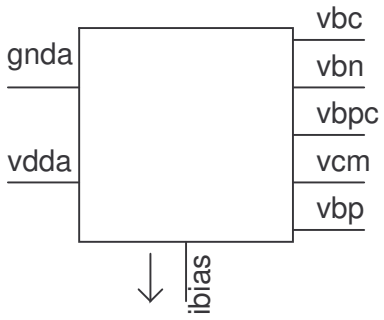


Figure 8.8: msp_bias_opamp

8.1.1.1.4.1 msp_bias_opamp Bias circuit for opamp. Two bias circuits are used for two opamps. Both have the same pins. The transistor sizes only differ in both the circuits.

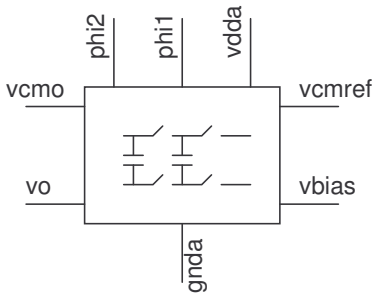


Figure 8.9: msp_swcmfb

8.1.1.1.4.2 msp_swcmfb Switched capacitor common mode feedback circuit for the opamp

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	analog ground
vbc	input-output	cascode NMOS device bias voltage
vbn	input-output	tail current device bias voltage
vbpc	input-output	cascode PMOS device bias voltage
vcm	input-output	input common mode bias voltage
vbp	input-output	common mode feedback circuit bias voltage
ibias	input-output	master current

Table 8.8: msp_bias_opamp

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
vo	input-output	connected to output voltage of opamp
vcmo	input-output	gate bias for the top PMOS cascode device of opamp
vcmref	input-output	common mode output reference voltage
vbias	input-output	bias voltage from the bias circuit
phi1	input-output	clock for switches
phi2	input-output	clock for switches

Table 8.9: msp_swcmfb

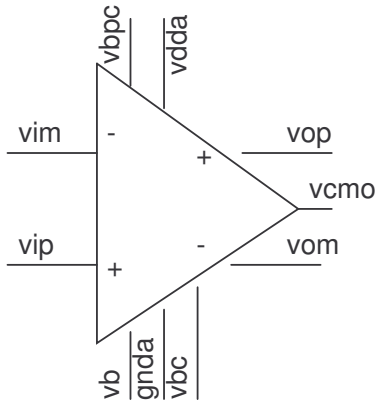


Figure 8.10: msp_tele_opamp

8.1.1.1.4.3 msp_tele_opamp Telescopic opamp without bias and the common mode feedback circuit.

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
vim	input-output	input negative voltage
vip	input-output	input positive voltage
vom	input-output	output negative voltage
vop	input-output	output positive voltage
vcmo	input-output	gate bias voltage for the top of the PMOS cascode devices
vbpc	input-output	gate bias voltage for the bottom of the PMOS cascode devices
vbc	input-output	gate bias voltage for the top NMOS cascode devices
vbc	input-output	gate bias voltage for the tail current device

Table 8.10: msp_tele_opamp

8.1.1.2 msp_2nd_integrator

Second switched capacitor integrator of the $\Sigma\Delta$ modulator. It has the blocks same as that of the first integrator with extension as 2.

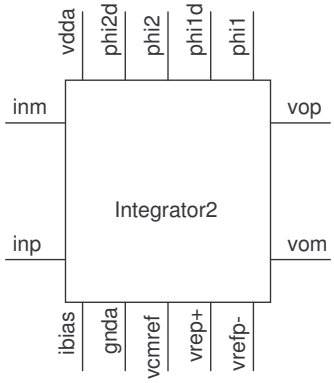


Figure 8.11: msp_2nd_integrator

Pin	Type	Description
inm	input-output	positive input voltage
inp	input-output	negative input voltage
vdda	input-output	positive supply voltage
gnda	input-output	analog ground
vop	input-output	positive output voltage
vom	input-output	negative output voltage
vrefp-	input-output	negative feedback voltage from DAC
vrefp+	input-output	positive feedback voltage from DAC
vcmref	input-output	common mode reference voltage
ibias	input-output	bias current for opamp
phi1	input-output	clock for the switched capacitor integrator
phi1d	input-output	advanced version of phi1
phi2	input-output	clock non overlapping with phi1
phi2d	input-output	advanced version of phi2

Table 8.11: msp_2nd_integrator

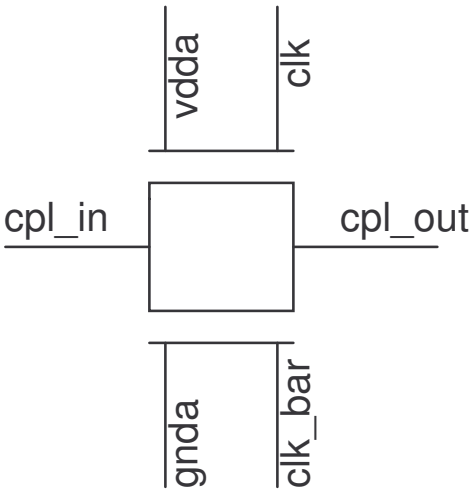


Figure 8.12: msp_switch_cpl

8.1.1.2.1 msp_switch_cpl Transmission gate used in second integrator

Pin	Type	Description
clk	input-output	clock for controlling the NMOS device
clk_bar	input-output	clock for controlling the PMOS device
vdda	input-output	positive supply voltage
gnda	input-output	ground
cpl_in	input-output	input/output of the switch
cpl_out	input-output	input/output of the switch

Table 8.12: msp_switch_cpl

8.1.1.3 msp_caldac

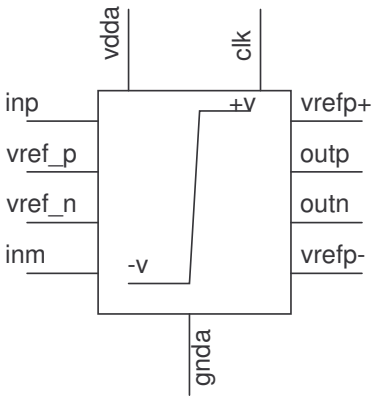


Figure 8.13: msp_caldac

Module includes comparator, latch and 1 bit DAC.

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
inp	input-output	input positive voltage
inm	input-output	input negative voltage
outp	input-output	latch output positive voltage
outm	input-output	latch output negative voltage
vref_p	input-output	positive reference voltage for DAC
vref_n	input-output	negative reference voltage for DAC
vrefp+	input-output	positive analog feedback voltage form DAC
vrefp-	input-output	negative analog feedback voltage form DAC
clk	input-output	clock for comparator

Table 8.13: msp_caldac

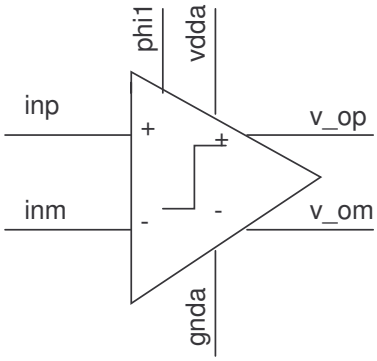


Figure 8.14: msp_comparator

Comparator used to digitze the output voltage of the integrator (second).

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
phi1	input-output	clock
inp	input-output	positive input voltage
inm	input-output	negative input voltage
v_op	input-output	positive output voltage
v_om	input-output	negative output volatge

Table 8.14: msp_comparator

8.1.1.3.1 msp_comparator

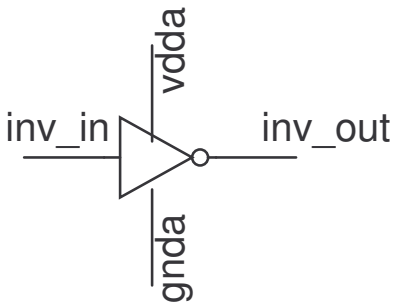


Figure 8.15: msp_comp_inv

8.1.1.3.1.1 msp_comp_inv Inverter used in the comparator

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
inv_in	input-output	inverter input
inv_out	input-output	inverter output

Table 8.15: msp_comp_inv

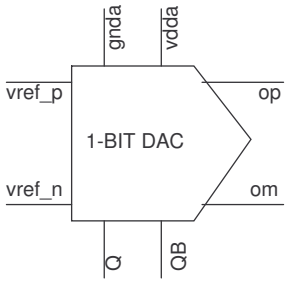


Figure 8.16: msp_dac_onebit

8.1.1.3.2 msp_dac_onebit 1 - bit analog to digital converter

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
vref_p	input-output	positive reference voltage for DAC
vref_n	input-output	negative reference voltage for DAC
op	input-output	positive analog feedback voltage form DAC
om	input-output	negative analog feedback voltage form DAC
Q	input-output	positive output voltage form latch
QB	input-output	negative output voltage form latch

Table 8.16: msp_dac_onebit

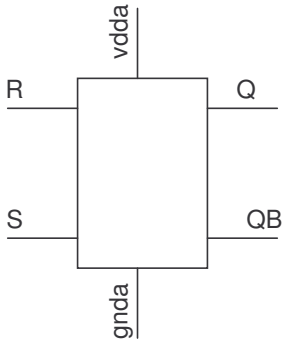


Figure 8.17: msp_latch

8.1.1.3.3 msp_latch Latch used for latching comparator outputs.

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
R	input-output	reset input
S	input-output	set input
Q	input-output	positive output voltage to DAC
QB	input-output	negative output voltage to DAC

Table 8.17: msp_latch

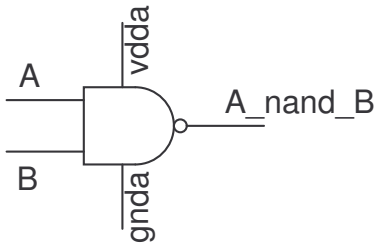


Figure 8.18: msp_nand

8.1.1.3.3.1 msp_nand NAND gate used in latch

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
A	input-output	one of the gate input
B	input-output	other gate input
A_nand_B	input-output	NAND gate output

Table 8.18: msp_nand

8.1.1.4 msp_clk

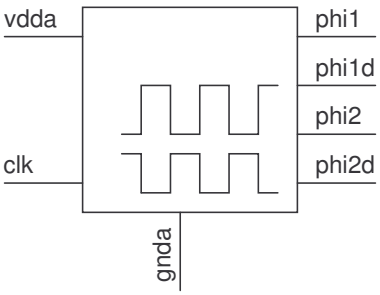


Figure 8.19: msp_clk

Twp phase non overlapping clock module

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
clk	input-output	master clock
phi1	input-output	clock for the switched capacitor integrator
phi1d	input-output	advanced version of phi1
phi2	input-output	clock non overlapping with phi1
phi2d	input-output	advanced version of phi2

Table 8.19: msp_clk

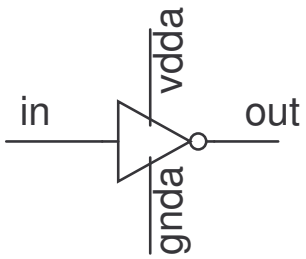


Figure 8.20: msp_clk_inv

8.1.1.4.1 msp_clk_inv Inverter used in the clock

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
in	input-output	inverter input
out	input-output	inverter output

Table 8.20: msp_clk_inv

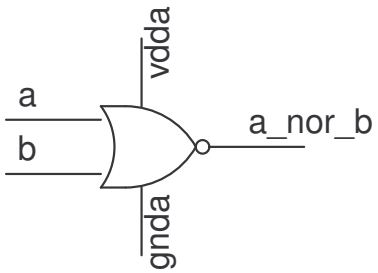


Figure 8.21: msp_nor

8.1.1.4.2 msp_nor NOR gate used in two phase non overlapping clock generator

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
a	input-output	one of the gate input
b	input-output	other gate input
a_nor_b	input-output	NOR gate output

Table 8.21: msp_nor

8.1.1.5 msp_buffer1

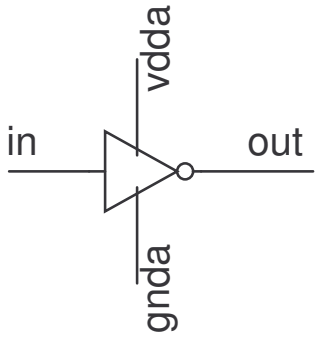


Figure 8.22: msp_buffer1

Output buffer. First stage.

8.1.1.6 msp_buffer2

Output buffer. Second stage.

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
in	input-output	input voltage
out	input-output	output voltage

Table 8.22: msp_buffer1

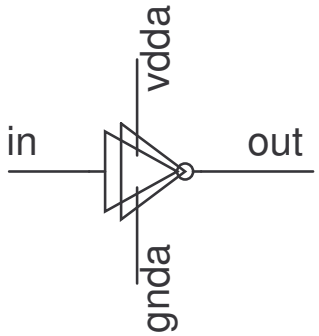


Figure 8.23: msp_buffer2

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	ground
in	input-output	input voltage
out	input-output	output voltage

Table 8.23: msp_buffer2

8.1.2 msp_bandgap

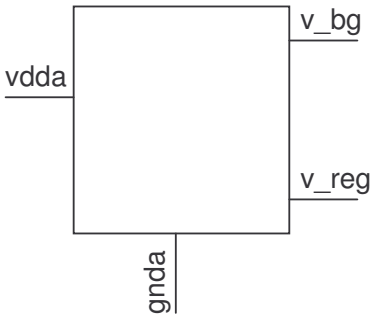


Figure 8.24: msp_bandgap

Bandgap voltage reference

Pin	Type	Description
vdda	input-output	positive supply voltage
gnda	input-output	analog ground
v_bg	input-output	bandgap output voltage
v_reg	input-output	regulated supply voltage (not used)

Table 8.24: msp_bandgap

8.1.3 msp_pad

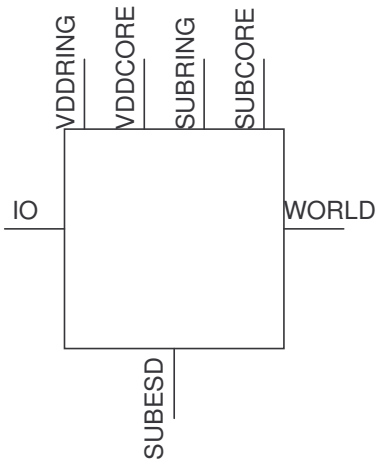


Figure 8.25: msp_pad

Pad used in the chip

Pin	Type	Description
IO	input-output	pin to be connected inside the chip
WORLD	input-output	pin to be connected to the external world
VDDCORE	input-output	pin for ESD protection of the chip (connected to positive supply)
VDDRING	input-output	pin for ESD protection of the chip (connected to positive supply)
SUBCORE	input-output	pin for ESD protection of the chip (connected to ground)
SUBRING	input-output	pin for ESD protection of the chip (connected to ground)
SUBESD	input-output	pin for ESD protection of the chip (substrate of the pad, connected to ground)

Table 8.25: msp_pad

Chapter 9

Conclusion

A 16-bit $\Sigma\Delta$ modulator has been designed in 0.35μm CMOS process Non idealities like the effect of finite gain, noise and slew rate of the opamps on the performance of the modulator are studied and modelled in Matlab to meet the system specifications. The opamp non linear gain is also modelled. A code is written in Matlab to find the system performance for a given opamp non linearity. Further, a bandgap voltage reference generator is designed and the effect of the power supply rejection on the circuit is calculated. These two circuits are simulated in Cadence and layout is done. These are sent for fabrication. A PCB has been designed to test the chip.

Appendix A

Matlab Code

The following is the matlab code for modelling the non linear gain for the opamp and study its effect on the performance of the modulator.

```
close all;
clear all;
vin = s_h(-2,500,5); %computes the input samples
delta = 1.25; %bin width;
c_samp = 0.5e-12;
c_int = 1e-12;
vout_cap = 0; %initial voltage across integrating capacitor
vout_cap2 = 0;
%k3*x^3+k1*x+k0+vout_cap = 0 is the equation for vi during
%integrating phase
alpha = 3.196; %opamp model alpha*tanh(beta*vi)
beta = 1094;
a = alpha*beta; %first order term
b = alpha*beta^3/3; %third order term
y_out(1:length(vin)) = 0;
y_out_2(1:length(vin)) = 0;
bin(1:length(vin)) = -1*delta;
for n = 2:length(vin)
```

```
(y_out(n),vcap1) =
cal_next(vin(n-1),vout_cap,bin(n-1),c_samp,c_int,alpha,beta);
vout_cap=vcap1;
(y_out_2(n),vcap2) =
cal_next(y_out(n-1),vout_cap2,bin(n-1),c_samp,c_int,alpha,beta);
vout_cap2=vcap2;
if (y_out_2(n) >= 0)
bin(n) = delta;
else
bin(n) = -1*delta;
end
end
%fft comuptation
y_fft_mod = comp_fft(bin);
y_fft_mod_fin = db(y_fft_mod); %computes fft in dB
%ploting of the result
f = 2.048e6*(0:length(y_fft_mod)-1)/length(y_fft_mod);
plot(f(1:length(f)/2)*1e-6,y_fft_mod_fin(1:length(f)/2),'r');
```

Code of *cal_next* subroutine

```
function [vout,vcap_next] =
cal_next(input,vcap_prev,dig_code,c1,c2,alpha,beta);
k0 = c1*(input-dig_code)+c2*vcap_prev;
range = 0;
options = optimset('TolX',1e-8);
delta_v = fzero(@op_model,range,options,alpha,beta,c2,k0);
vout = alpha*tanh(beta*(-delta_v));
vcap_next = vout - delta_v;
```

Code of *s_h* subroutine

```
%sampling function
%inp_amp :  input amplitude in db
```

```
%fin :  input frequency
%cycles :  no of cycles
function inp_samp = s_h(inp_amp,fin,cycles)
n = 0:4.88281e-7:cycles/fin;
inp_smap(1:length(n)) = 0;
inp_amp = 10^(inp_amp/20);
inp_samp = inp_amp*sin(2*pi*fin*n);
```

Code of *comp_fft* subroutine

```
function y = comp_fft(x)
n = 0:12287;
win = .5*(1- cos(2*pi*n/(12288)) );
x = x(length(x)-12287:length(x)).*win;
y = abs(fft(x))*4/12288;
```

Code of *db* subroutine

```
function out = db(x)
out = 20*log10(x);
```

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