ANALYSIS OF CLOCK JITTER IN CONTINUOUS TIME $\Delta\Sigma$ MODULATORS

A THESIS

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INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

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THESIS CERTIFICATE

This is to certify that the thesis titled **Analysis of clock jitter in continuous time $\Delta\Sigma$ modulators**, submitted by **Reddy Karthikeyan**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Science**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Delta sigma($\Delta\Sigma$) modulators are high resolution, oversampled analog-to-digital (ADC) and digital-to-analog converters (DAC). They are closed loop converters wherein the quantization noise is high pass filtered by the loop. They are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators. CTDSMs are lower power alternatives to their discrete time counterparts. Several advantages accrue by implementing the modulator loop filter with continuous-time circuitry. However, clock jitter degrades the signal to noise ratio (SNR) of the modulator. In this work, we examine noise due to clock jitter in single-loop low pass continuous-time delta-sigma modulators employing non-return to zero (NRZ) feedback DACs. As an extension of the theoretical study, a third order modulator intended for wide-band applications which is less sensitive to jitter noise, has been designed, fabricated and tested. It operates at 300MHz and has a signal bandwidth of 15MHz. The chip was implemented in a 0.18μm CMOS process. Measurements from fabricated chips indicate a peak SNR of 67 dB and a dynamic range of 70.5 dB. The modulator occupies an active area of 1mm^2 and consumes 20 mW from a 1.8 V supply.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

Introduction

Delta sigma ($\Delta\Sigma$) modulators are high resolution, oversampled analog-to-digital and digital-to-analog converters. They are closed loop converters wherein the quantization noise is high pass filtered by the loop. They are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators. CTDSMs are lower power alternatives to their discrete time counterparts. In recent years, CTDSM has been the preferred choice for high speed data conversion applications. Several advantages accrue by implementing the modulator loop filter with continuous-time circuitry. The ADC does not require high order anti-alias filters, thus saving power and area. However, clock jitter degrades the signal to noise ratio (SNR) of the modulator. In previous works, the effect of clock jitter has been mostly analyzed for single bit modulators. Multi-bit modulators have received much attention in recent times. Hernandez *et al.* (2004) numerically optimized the noise transfer function (NTF) of a multi-bit modulator for least clock jitter sensitivity. The work stopped short of giving an explanation for the method. This prompted us to explore the effect of clock jitter on CTDSMs which forms a major part of the thesis. In this work, we examine noise due to clock jitter in single-loop low pass continuous-time delta-sigma modulators employing non-return to zero (NRZ) feedback DACs. As an extension of the theoretical study, a third order modulator intended for wide-band applications which is less sensitive to jitter noise, has been designed. It operates at 300 MHz and has a signal bandwidth of 15 MHz (OSR of 10). The design was implemented in a 0.18μm CMOS process. It occupies an active area of 1mm^2. The

design consumes a power of 20 mW from a 1.8 V supply and the obtained ENOB is 11 bits with a peak SNR of 67 dB and SNDR of 63 dB. The dynamic range measured is 70.5 dB.

1.1 Organization

The rest of the thesis is organized as follows. Chapter 2 introduces the concept of $\Delta\Sigma$ modulators. Chapter 3 analysis the effect of clock jitter on the performance of the modulator. Chapter 4 deals with the design of the continuous time delta sigma modulator. Chapter 5 explains the design centering technique for optimizing the NTF of the modulator in the presence of the circuit non-idealities. Test setup and measurement results are given Chapter 6. Chapter 7 concludes the thesis.

CHAPTER 2

$\Delta\Sigma$ Modulator Concepts

In an upfront analog-to-digital converter (ADC) sampling at f_s, if V_{lsb} is the level spacing, then the quantization noise power σ_q^2 is given by $V_{lsb}^2/12$. The quantization noise is assumed to be white and has a power spectral density of $\frac{\sigma_q^2}{f_s/2}$ V^2/Hz and is shown in Figure 2.1. Now if the signal bandwidth f_b is underutilized, i.e., if it is less than the Nyquist rate, then the in-band noise is reduced. For every doubling of the sampling rate, the noise reduces by a factor of 3 dB.

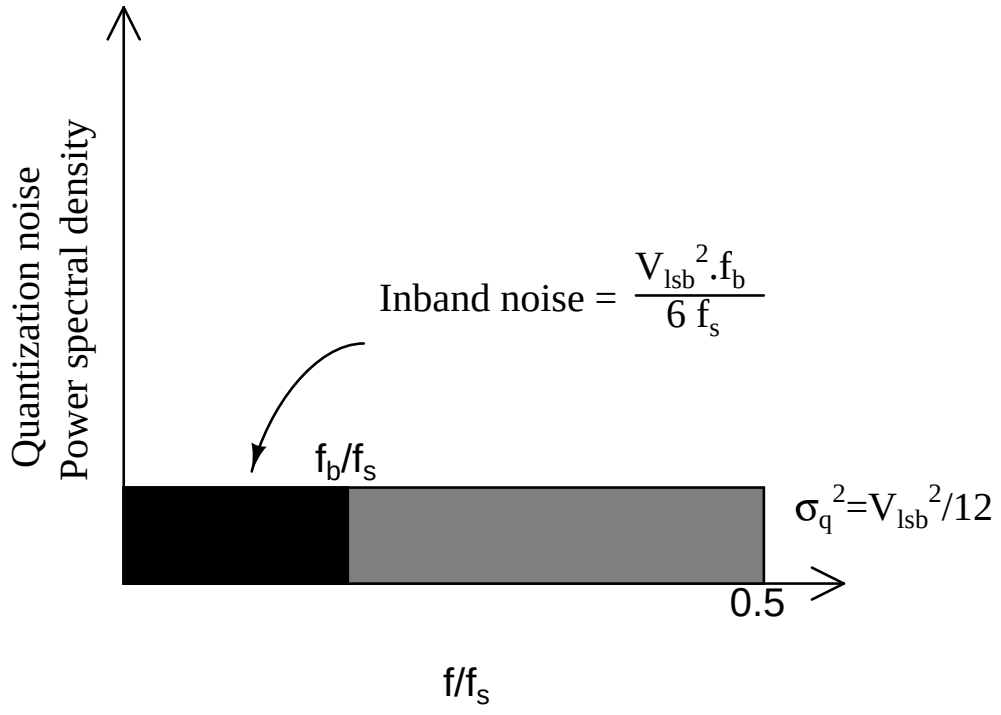


Figure 2.1: Quantization noise spectrum of ADC

A better way of utilizing this advantage of oversampling is to filter away the noise in the signal bandwidth to higher frequencies, and this what the $\Delta\Sigma$ modulator accomplishes. The block diagram of a discrete time $\Delta\Sigma$ modulator is shown in Figure 2.2. A

discrete time modulator is shown for ease of explaining the operation of the modulator. The closed loop architecture can be linearized by modeling the quantization noise as an additive noise. If the filter is a low pass filter, then the noise transfer function (NTF) from the quantization noise to the output would be high pass filtered. The signal transfer function (STF) from the input *u*, to the output is a low pass filter with gain equals 1 in the signal bandwidth.

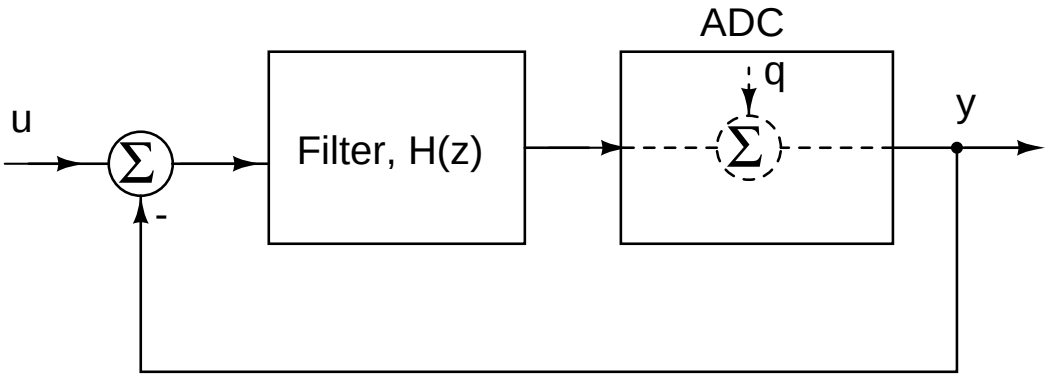


Figure 2.2: $\Delta\Sigma$ modulator

Figure 2.3 shows the typical spectrum of the shaped quantization noise. Inside the signal bandwidth the quantization noise is attenuated approximately by the large gain of the filter H(z). The output spectrum of the modulator is given by,

$$Y(z) = STF(z)X(z) + NTF(z)E_q(z) \tag{2.1}$$

where $STF(z) = \dfrac{H(z)}{1 + H(z)}$
and $NTF(z) = \dfrac{1}{1 + H(z)}$

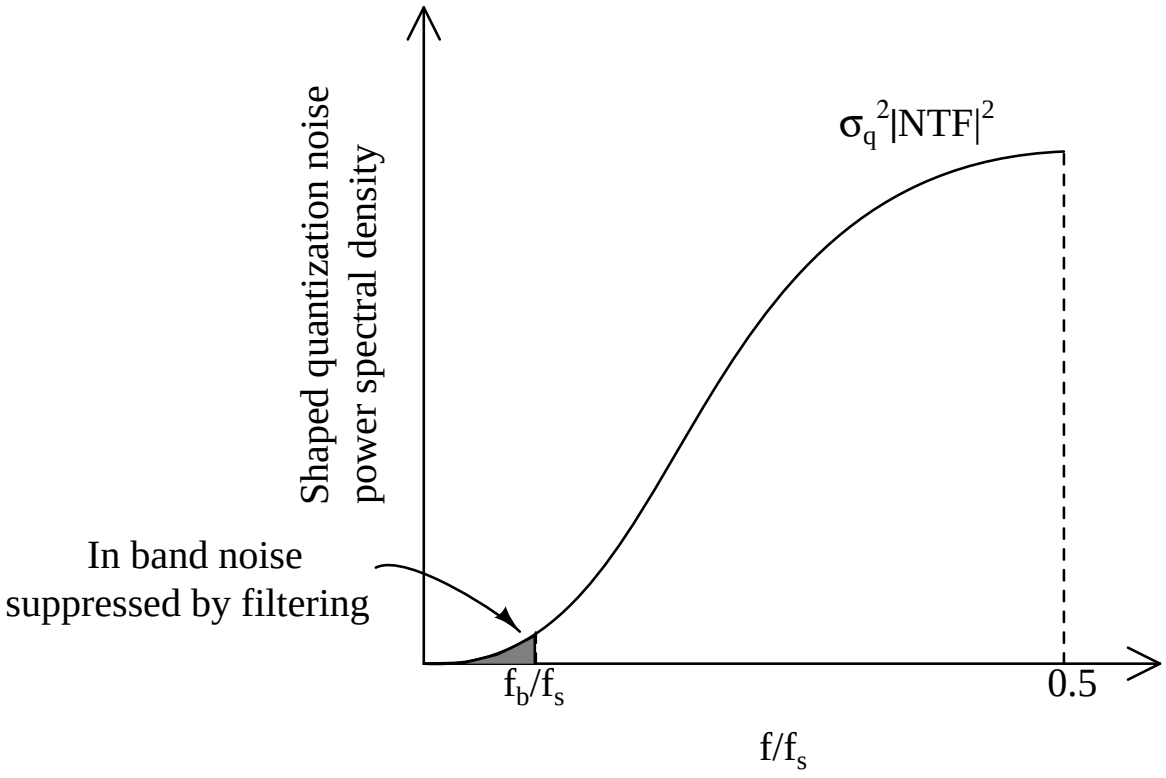


Figure 2.3: Spectrum of the shaped quantization noise

2.0.1 Continuous time modulators and their limitations

Continuous time modulators score over their discrete time counterparts as they are power efficient, have inherent anti aliasing characteristics. Along with the advantages, they also come with some drawbacks which limit their performance. Before going into the drawbacks, let us look at the general block diagram of the continuous time modulator shown in Figure 2.4.

The basic components of the modulator are:

1. **Loopfilter:** The loopfilter, H(s) is realized using integrators. The opamps used to realize the integrators have finite gain and bandwidth. This results in a deviation of the NTF from the desired one. Chapter 5 proposes an optimization method by which this could be overcome.

2. **ADC:** The ADC produces the output of the modulator. Any circuit level non-

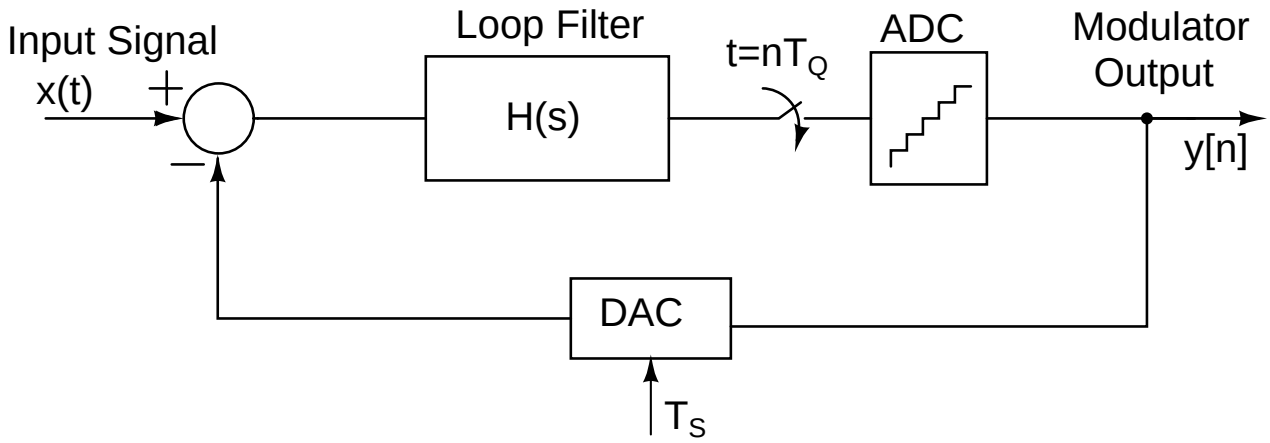


Figure 2.4: Block Diagram of Continuous time $\Delta\Sigma$ Modulator

idealities in the ADC would be shaped out of the signal bandwidth, hence the design constraints on the ADC are very relaxed.

3. **DAC:** The digital to analog converter closes the loop. Hence, any non-idealities in the DAC are expected to appear directly at the output of the modulator. The DAC elements are bound to have mismatch, but standard practices like having a Dynamic element matching techniques mitigate this problem. The delay between the clocking of the ADC and the DAC produces an excess loop delay which is also overcome by the method described in Chapter 5. The main limitation comes from the clock jitter in the DAC clock. The clock jitter modulates the width of the feedback DAC pulse, hence acting as a source of noise and limiting the performance of the modulator. The next chapter would deal with the detailed analysis of the clock jitter which forms a major part of this thesis.

CHAPTER 3

Fundamental Limitations of clock jitter in Continuous time $\Delta\Sigma$ modulators

3.1 Introduction to clock jitter in CTDSMs

Continuous-time delta-sigma modulators are lower power alternatives to their discrete-time counterparts. Several advantages accrue by implementing the modulator loop filter with continuous-time circuitry. An explicit anti-alias filter, which would be required in a switched-capacitor implementation is not necessary. The bandwidth requirements for the active elements in the loop are relaxed (Schreier and Temes (2005)), which results in a lower power consumption. However, clock jitter degrades the performance of the modulator.

Clock jitter influences the sampling instant of the flash quantizer, as well as the width of the feedback DAC pulse. To the authors' best knowledge, the effect of clock-jitter in continuous time delta-sigma modulators was first studied in Cherry and Snelgrove (1999*a*) and Oliaei (1999). Both these papers conclude that noise due to the modulation of the feedback DAC pulsewidth is the dominant cause of jitter noise. This is intuitively satisfying due to the following - the error due to the variation of the sampling instant of the quantizer is noise shaped due to the high loop gain. Hence, the in-band noise power should not be dominated by this noise. However, the error in the DAC feedback pulsewidth adds directly at the input of the modulator and is not noise shaped. A similar conclusion was reached in Tao *et al.* (1999).

Most studies on jitter noise have concentrated on single-bit modulators, where stability considerations restrict the out-of-band gain (OBG) of the loop NTF to around 1.5 (Chao *et al.* (1990)). Thus, the amount of freedom in choosing an NTF is restricted. Multi-bit modulators have been receiving much attention recently due to their potential for very low power dissipation. A multi-bit quantizer in the loop has several advantages. The in-band quantization noise is reduced when compared with a single bit design since the inherent quantizer is more precise. More importantly, the use of a multi-bit quantizer permits the choice of a more aggressive NTF, further decreasing the in band noise. It is thus seen that multi-bit operation permits a larger range of NTFs when compared to a single bit design. The basic intuition regarding the effect of jitter in the multi-bit case is similar to that in a single bit modulator. Since a larger range of choices exist for the NTF, a relevant question is if and how the choice of the NTF influences the performance of the modulator with clock jitter.

In Hernandez *et al.* (2004), the authors numerically optimized the shape of the NTF (by varying the pole and zero locations) to minimize jitter noise, for a given quantization noise. Experimental results for a sigma-delta modulator incorporating the optimized NTF were reported in Paton *et al.* (2004). The optimization process resulted in an NTF with a peak of transmission, as well as zeros spread in the signal band. This work builds on the observations in Hernandez *et al.* (2004), and aims to understand the ramifications of NTF design on the jitter properties of CTDSMs. The rest of the chapter is organized as follows.

Section 3.2 gives a brief overview of jitter noise in CTDSMs. We show that the noise due to jitter and quantization are interrelated in a manner dependent on the NTF of the

modulator. In Section 3.3, we review the Bode sensitivity integral for discrete-time systems and extend its application to the evaluation of jitter and quantization noise. Given an NTF, we show there is a lower bound on the jitter noise of the modulator (Reddy and Pavan (2006)). Intuition is derived for the shape of the NTF derived by numerical optimization in Hernandez *et al.* (2004).

In Section 3.4, we derive approximate versions of the lower bound that are valid for a family of commonly used NTFs. We show that there exists a trade-off between quantization noise and jitter noise, one can be decreased at the expense of another. Section 3.5 compares the effect of clock jitter in RZ (Return-to-Zero) and NRZ DACs.

Section 3.6 discusses NTF design implications resulting from the jitter bound. The arguments used for a $\Delta\Sigma$ ADC are also directly applicable to a $\Delta\Sigma$ DAC, for which we present experimental results in Section 3.7.

3.2 An overview of clock jitter effects in CTDSMs

As explained in the introduction, the effect of clock jitter can be modeled as an additive sequence at the input of a jitter-free modulator. For the case of NRZ feedback DACs considered in this work, the error sequence is given by

$$e_j(n) = [y(n) - y(n-1)] \frac{\Delta T_s(n)}{T} \tag{3.1}$$

where $y(n)$ is the n^{th} output sample of the modulator, T is the sampling time and $\Delta T_s(n)$ is the clocking uncertainty of the n^{th} edge of the DAC and is assumed as independent identically distributed random variables (Cherry and Snelgrove (1999*a*)). The

spectral density of e_j is white and has a variance σ_{ej}^2 given by

$$\sigma_{ej}^2 = \sigma_{dy}^2 \frac{\sigma_{\Delta T_s}^2}{T^2} \tag{3.2}$$

where $\sigma_{\Delta T_s}^2$ is the variance of the clock jitter. Clearly, σ_{ej}^2 is dependent on the input signal through $y(n)$ and $y(n-1)$. When the input is nulled, the modulator will exhibit idle-channel noise, which is dependent on clock jitter and quantization noise (Hernandez *et al.* (2004)). Then, σ_{dy}^2, the variance of $y(n) - y(n-1)$ is given by

$$\sigma_{dy}^2 \approx \frac{\sigma_{lsb}^2}{\pi} \int_0^{\pi} |(1 - e^{-j\omega})\, NTF(e^{j\omega})|^2 d\omega \tag{3.3}$$

where, σ_{lsb}^2 is the variance of the quantization noise of the internal quantizer used in the modulator.

The analysis of the clock jitter in the rest of the chapter is based on (3.3), which is derived assuming the modulator is linear and quantization noise is additive. These assumptions tend to be largely valid when a multi-bit quantizer is used in the loop (Schreier and Temes (2005)). To check the validity of the assumptions, a fourth order modulator having a maximally flat NTF with an OBG of 2.5 was simulated with clock jitter ($\sigma_{\Delta Ts} = 10^{-3}T$). The over sampling ratio (OSR) was 32. Simulations were run for two and four bit quantizers. Figure 3.1 shows the computed and analytical PSD of the modulator output. The values of in-band jitter noise for the two cases are shown in Tab. 3.1. Good agreement is seen.

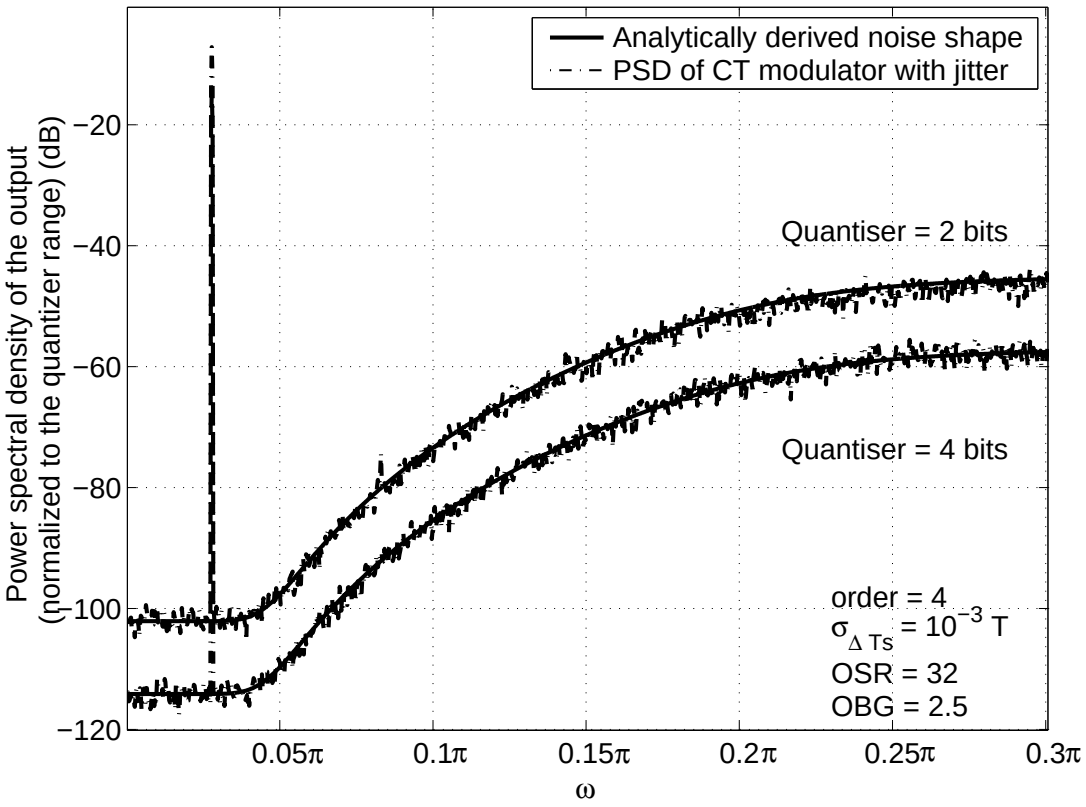


Figure 3.1: Output PSD for modulators with different quantizer bits in the presence of clock jitter.

Quantizer Resolution	Calculated in-band RMS Jitter noise	Simulated in-band RMS Jitter noise
2 bits	89.4×10^{-6}	91.5×10^{-6}
4 bits	22.3×10^{-6}	22×10^{-6}

Table 3.1: Simulated and Calculated Jitter noise in a Fourth Order CTDSM with a maximally flat NTF with OBG=2.5, OSR=32. A Four Bit Quantizer with an input range of 1 is assumed.

Using (3.3) in (3.2), the in-band noise due to jitter is

$$J = \frac{\sigma^2_{\Delta T_s}}{T^2} \frac{\sigma^2_{lsb}}{\pi OSR} \int_0^{\pi} |(1 - e^{-j\omega})\, NTF(e^{j\omega})|^2 d\omega \tag{3.4}$$

It is thus seen (Hernandez *et al.* (2004)) that the in-band jitter noise J depends on the area A_J under the $|(1 - e^{-j\omega})\, NTF(e^{j\omega})|^2$ curve, where

$$A_J = \int_0^{\pi} |(1 - e^{-j\omega})\, NTF(e^{j\omega})|^2 d\omega \tag{3.5}$$

The in-band quantization noise Q, on the other hand is given by

$$Q = \frac{\sigma^2_{lsb}}{\pi} \int_0^{\frac{\pi}{OSR}} |NTF(e^{j\omega})|^2 d\omega \tag{3.6}$$

From (3.4), it is clear that jitter noise is predominantly determined by the behaviour of the NTF outside the signal band, since $|NTF(e^{j\omega})|$ is very small within the signal bandwidth. Quantization noise, on the other hand, only depends on the NTF within the signal bandwidth. In order to better understand the trade-offs implied by (3.4) and (3.6), consider the set of NTFs that are maximally flat. For this family, once the order is specified, the NTF is fully defined by the OBG. It is well known (Schreier (1993)) that increasing the OBG results in a lower in-band quantization noise Q. However, increasing the OBG results in a large in-band jitter noise J.

Figure 3.2 shows the effect of clock jitter on fourth order modulators with OBGs of 3 and 7. A four bit quantizer is assumed. Notice that the modulator with the lower OBG has *lower* noise, since most of the in-band noise is dominated by that contributed by jitter.

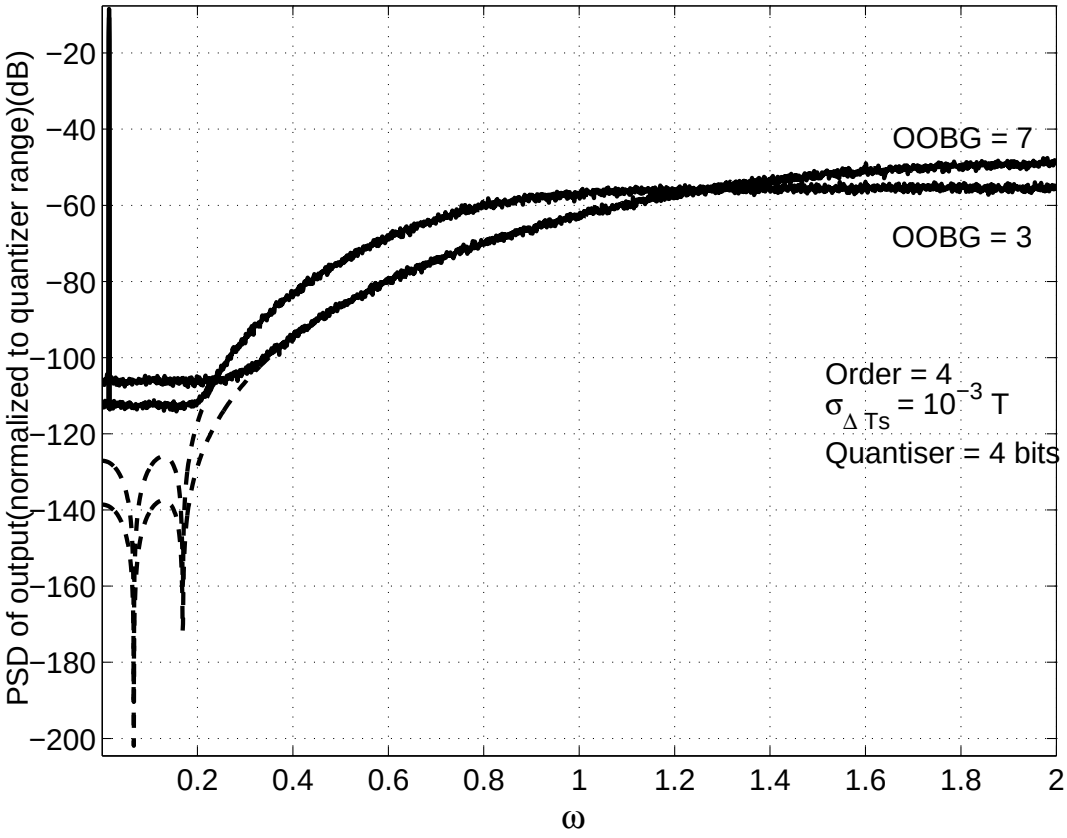


Figure 3.2: Output PSD for modulators with different out-of-band gains in the presence of clock jitter. The PSDs for jitter free operation are also shown for comparison.

Figure 3.3 shows the peak SNR for modulators as the OBG is varied, for different values of clock jitter. For small values of OBG, Q is large, leading to a low SNR. Increasing OBG increases the SNR, as Q decreases with increasing OBG. However, beyond a certain point, increasing the OBG has a detrimental effect on the SNR, as the noise is swamped by the in-band jitter noise J. A large OBG also reduces the maximum stable amplitude (MSA) of the modulator. It is thus seen that given the order and the amount of clock jitter, there is an optimum OBG at which the SNR is maximum. Understandably, this optimum OBG decreases with increasing clock jitter. Note that the peak SNR is a three dimensional trade-off, involving jitter noise, quantization and thermal noise and the MSA.

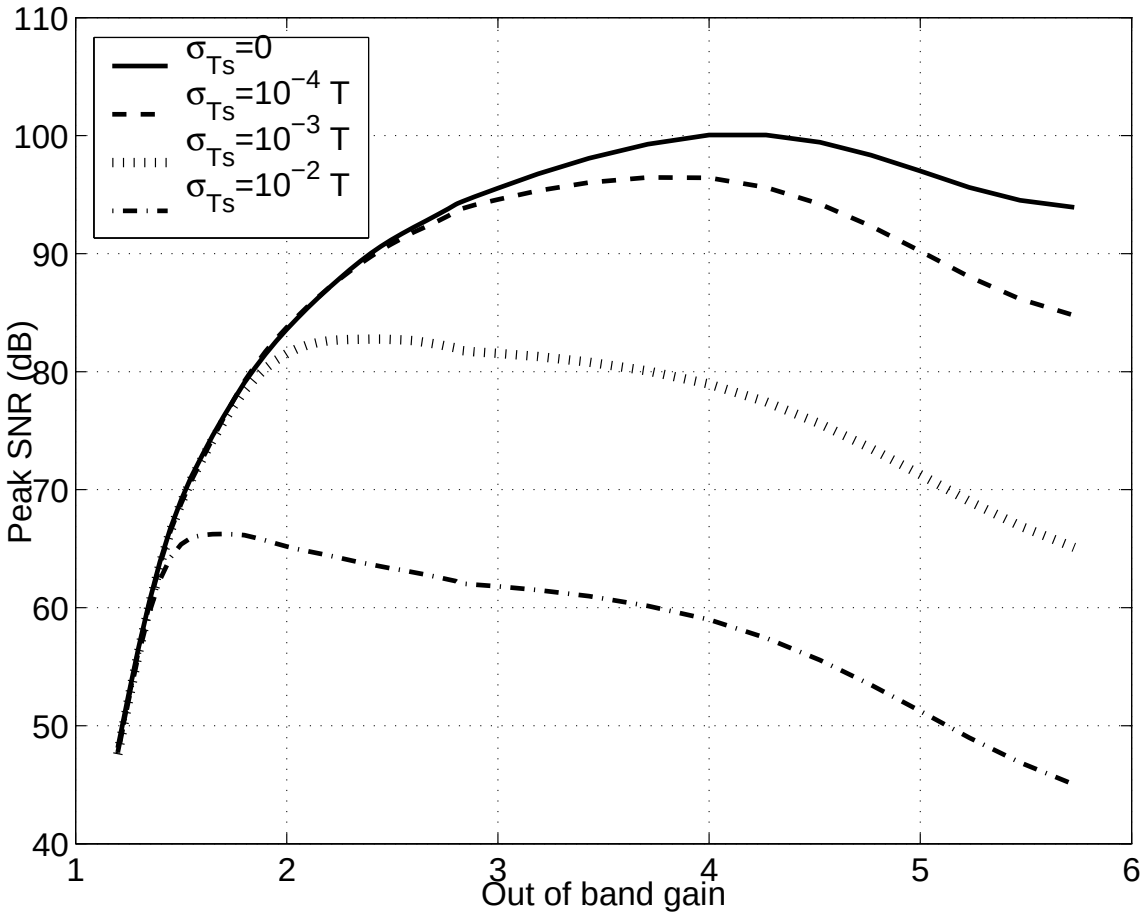


Figure 3.3: Peak SNR versus OBG for varying amounts of clock jitter, for a fourth order NTF, OSR=16 and 4-bit quantizer.

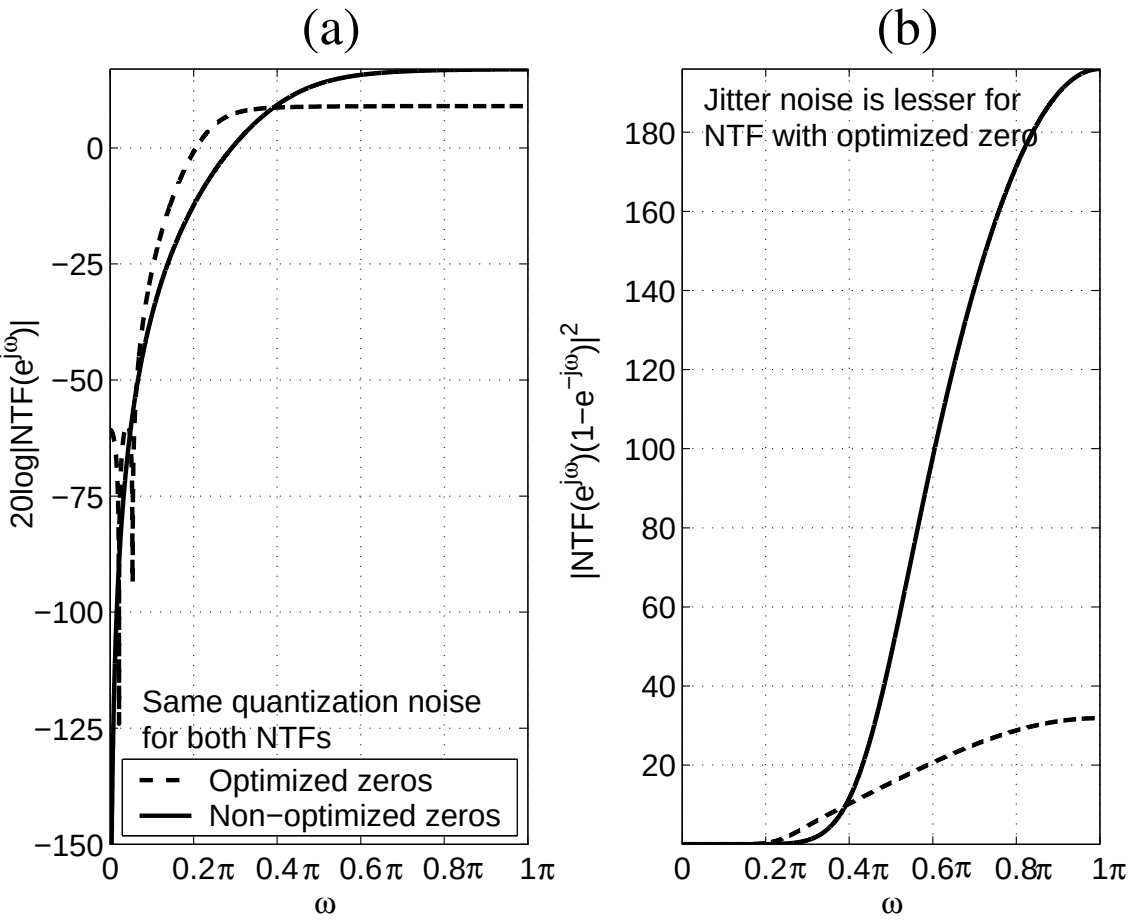


Figure 3.4: Noise transfer functions(log scale) and $|NTF(e^{j\omega})(1-e^{-j\omega})|^2$, with and without optimized zeros.

For a given Q and NTF order, the OBG for a modulator with optimally spread passband zeros is smaller than that of an NTF with all zeros at the origin (Schreier and Temes (2005)), as shown with a fourth order example in Figure 3.4(a). Part(b) of the figure shows $|NTF(e^{j\omega})(1-e^{-j\omega})|^2$, from which it is evident that the jitter noise J is lower for the modulator with optimally spread zeros.

If the (artificial) constraint that the NTF be maximally flat is removed, many NTFs with the same in-band characteristics, but different out of band behaviour can be conceived. Figure 3.5 shows the pole-zero plot of two NTFs, one which is maximally flat and one which has a transmission peak. The NTF zeros are the same in both cases, but the pole locations are different. The corresponding magnitude responses are shown in

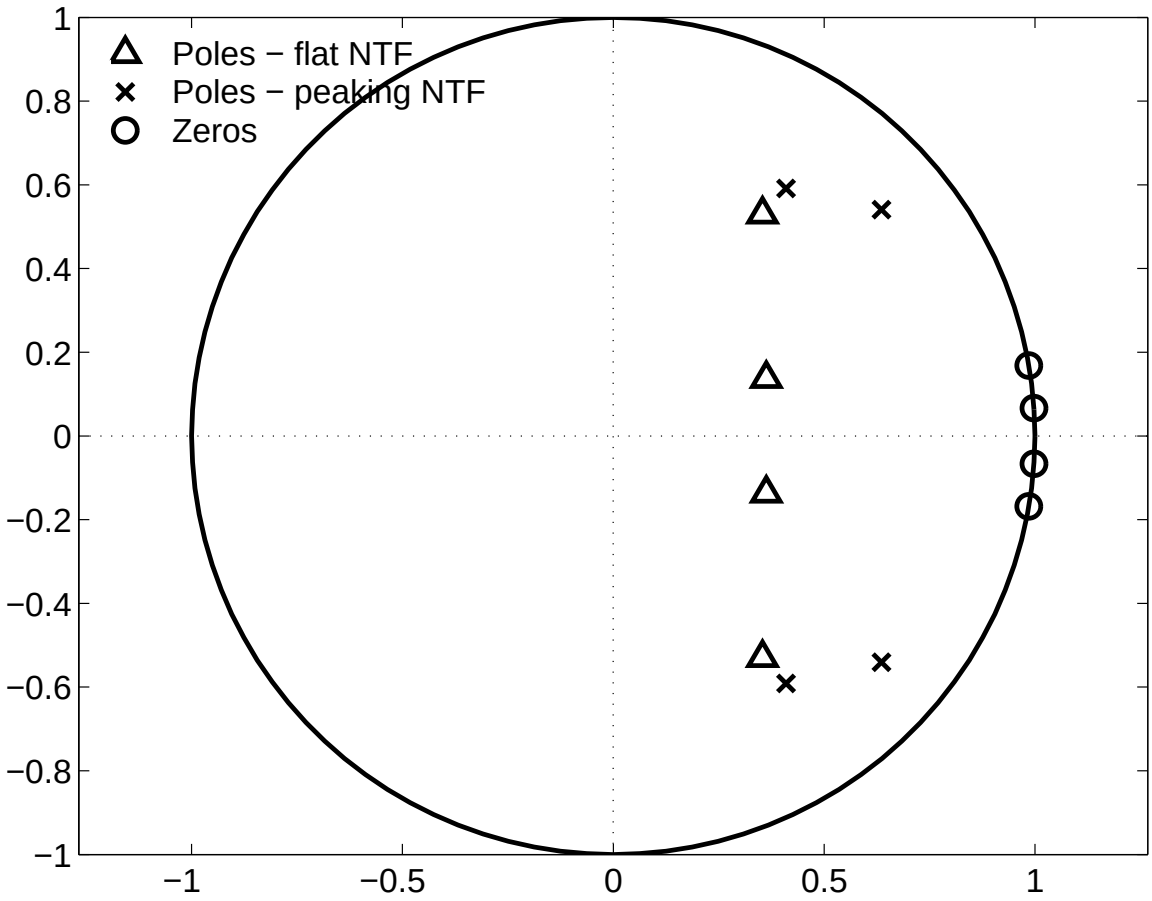


Figure 3.5: Pole-zero plot of a maximally flat and peaking noise transfer function having same in-band characteristics.

Figure 3.6. Observe that both the modulators will have the same quantization noise. However, in-band jitter noise J can be expected to be be different for the modulators since the out-of-band characteristics are not the same.

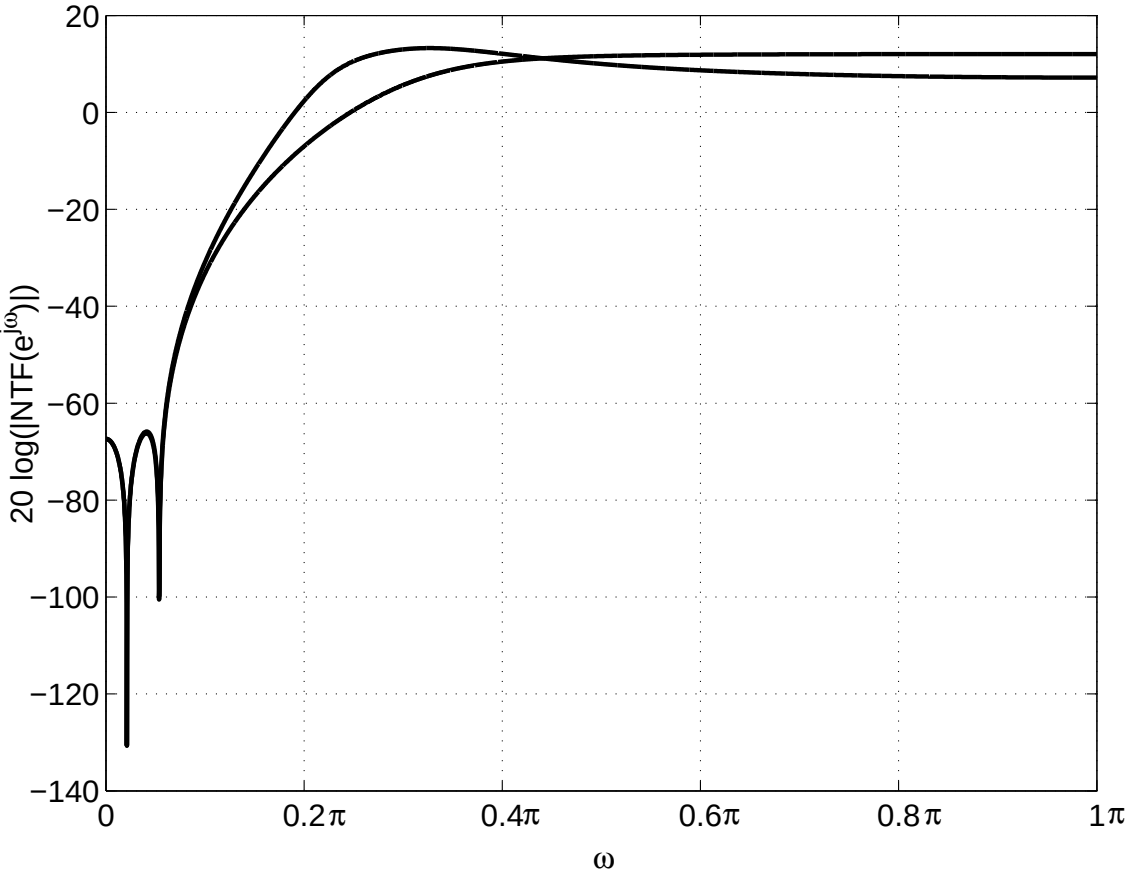


Figure 3.6: Two noise transfer functions with the same in-band response, but different out-of-band characteristics.

The above discussion begs the following question : for a given quantization noise, is there a specific choice of the out-of-band behaviour of the NTF that results in the lowest jitter sensitivity? This can be answered by understanding the Bode Sensitivity Integral described in the next section.

3.3 Bode's sensitivity integral for discrete-time systems and a lower bound on jitter noise

Consider the discrete-time feedback system shown in Figure 3.7.

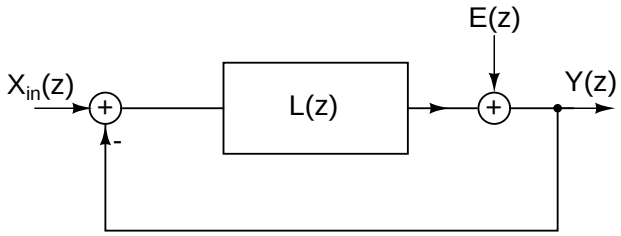


Figure 3.7: Linearized diagram of a $\Delta\Sigma$ modulator.

In the control systems literature, the quantity $\frac{1}{1+L(z)}$ is referred to as the *sensitivity function* of the loop. It quantifies the ability of the loop to reject disturbances (like $E(z)$) in the forward path as a function of frequency. For a continuous-time system, z is replaced by the Laplace variable s.

Bode (Bode (1945)) showed that for a minimum-phase loop filter $L(s)$, the continuous-time sensitivity function satisfies the following :

$$\int_0^\infty \log\left(\left|\frac{1}{1+L(j\omega)}\right|\right) d\omega = 0 \tag{3.7}$$

Physically, this means that the rejection of noise cannot be high at all frequencies, low sensitivity in one frequency band must be achieved through high sensitivity outside that band. The same idea applies to discrete-time feedback systems (Mohtadi (1990)), where it can be shown that if the loop filter has no poles and zeros outside the unit circle

the sensitivity function is constrained by the following integral.

$$\int_0^{\pi} \log\left(\left|\frac{1}{1+L(e^{j\omega})}\right|\right) d\omega = 0 \tag{3.8}$$

In the context of a delta-sigma modulator, the sensitivity function is the same as the noise transfer function, assuming the quantizer can be modeled as an additive noise source. Hence, (3.8) can be written as

$$\int_0^{\pi} \log\,|NTF(e^{j\omega})|\, d\omega = 0 \tag{3.9}$$

Using the relation $\int_0^{\pi} \log\,|(1-e^{-j\omega})|\, d\omega = 0$, in conjunction with (3.9), we see that

$$\int_0^{\pi} \log\,|NTF(e^{j\omega})(1-e^{-j\omega})|\, d\omega = 0 \tag{3.10}$$

Thus, when $20\,\log\,|NTF(e^{j\omega})(1-e^{-j\omega})|$ is plotted as a function of ω, the area above the 0 dB line is equal to the area below the line, as shown in Figure 3.8. Consider now the evaluation of the jitter noise J. Let ω_1 denote the frequency at which $\log\,|NTF(e^{j\omega})(1-e^{-j\omega})|$ crosses 0 dB. From (3.5), it is seen that

$$A_J > \int_{\omega_1}^{\pi} |(1-e^{-j\omega})\, NTF(e^{j\omega})|^2 d\omega \tag{3.11}$$

In order to arrive at a lower bound on J, we use the following inequality, shown in Appendix A.

$$\int_a^b |f(x)|^2\, dx \geq (b-a)\exp\left(\frac{2}{(b-a)}\int_a^b \log(|f(x)|)\, dx\right) \tag{3.12}$$

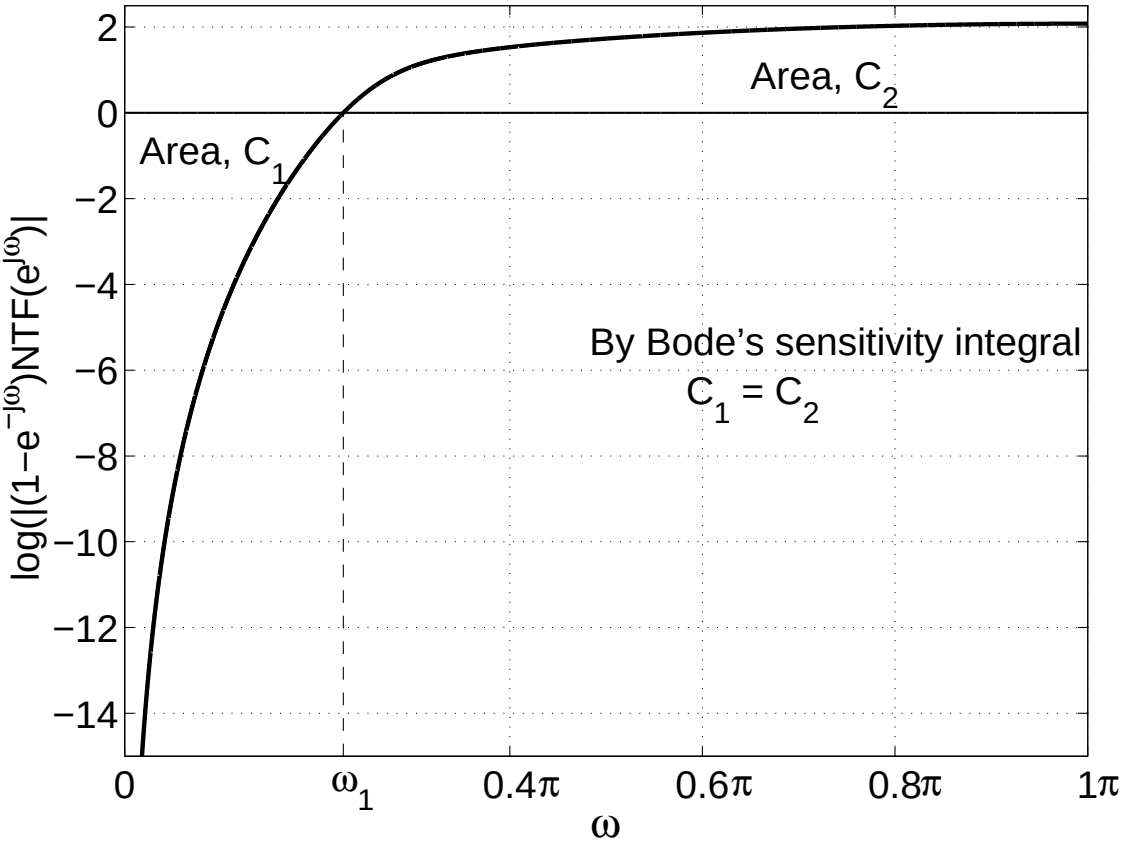


Figure 3.8: The Bode sensitivity integral.

From (3.12) and (3.11), we have

$$A_J \geq (\pi - \omega_1) \exp\left(\frac{2}{\pi - \omega_1} \int_{\omega_1}^{\pi} \log |(1 - e^{-j\omega})\, NTF(e^{j\omega})| d\omega\right) \tag{3.13}$$

Denoting the area of $\log\ |NTF(e^{j\omega})(1 - e^{-j\omega})|$ below the 0 dB line by C, we see that

$$J > J_{min} \tag{3.14}$$

where

$$J_{min} = \frac{\sigma^2_{\Delta T_s}}{T^2} \frac{\sigma^2_{lsb}}{\pi OSR} (\pi - \omega_1) \exp\left(\frac{2\,C}{\pi - \omega_1}\right) \tag{3.15}$$

J_{min} is therefore a lower bound on the in-band jitter noise for a given NTF and clock jitter. The above expression shows that the jitter noise is exponentially related to the area of the $\log\ |NTF(e^{j\omega})(1 - e^{-j\omega})|$ curve above (below) the 0 dB line.

Consider the plots (Figure 3.9) of $\log\ |NTF(e^{j\omega})(1 - e^{-j\omega})|$ for modulators with two different NTFs with identical performance in-band. The NTF with peaking exhibits a sharper transition when compared to the maximally flat design. This results in smaller values of C and A_J when compared to the maximally flat NTF. It is clear, therefore, that in order to minimize J for the same quantization noise Q, the NTF must be designed to have a sharp transition band, so that lower values of ω_1 and C can be obtained.

We now list some observations and implications of the jitter bound derived above.

- J_{min} is a tight bound, since the area under the $|NTF(e^{j\omega})(1 - e^{-j\omega})|^2$ curve from $0 < \omega < \omega_1$ is negligible, so that (3.13) is almost an equality. Due to the tightness of this bound, it is useful in design as is shown in the next section.
- (3.15) relates jitter noise to two parameters of the NTF - C and ω_1. For NTFs normally used in practice, it turns out that a simple relation between C and ω_1 can be found. This in turn makes J_{min} simply a function of ω_1.

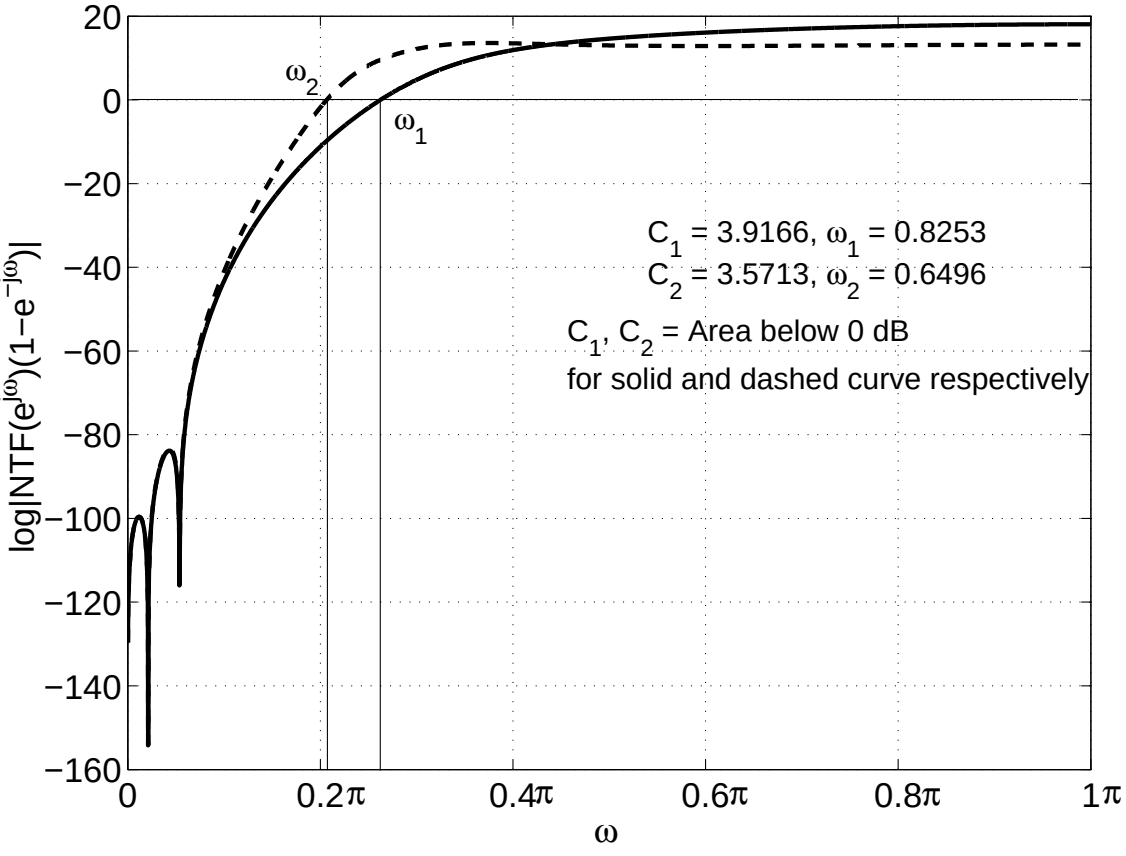


Figure 3.9: Noise transfer functions with the same in-band performance, but different out of band behaviour.

The problem of NTF design for reduced jitter sensitivity can be looked at in a different light as follows. Intuitively, it is seen that the area of $\log|NTF(e^{j\omega})(1-e^{-j\omega})|$ under the 0 dB line (i.e., C) is dependent on the quantization noise Q. By the Bode Sensitivity Integral the area above the 0 dB line must also be C. Varying the locations of the NTF poles will change the way C is distributed in the range $\omega_1 < \omega < \pi$ - so for least jitter sensitivity, one should "distribute" this C in such a manner as to minimize $\int_{\omega_1}^{\pi} |NTF(e^{j\omega})(1-e^{-j\omega})|^2$. From the discussion in Appendix A, this is achieved when $|NTF(e^{j\omega})(1-e^{-j\omega})|$ is a constant for $\omega_1 < \omega < \pi$. Since $|(1-e^{-j\omega})|$ is monotonically increasing with ω, it follows that J is minimized when $|NTF(e^{j\omega})|$ exhibits peaking. This explains the observation in Hernandez *et al.* (2004).

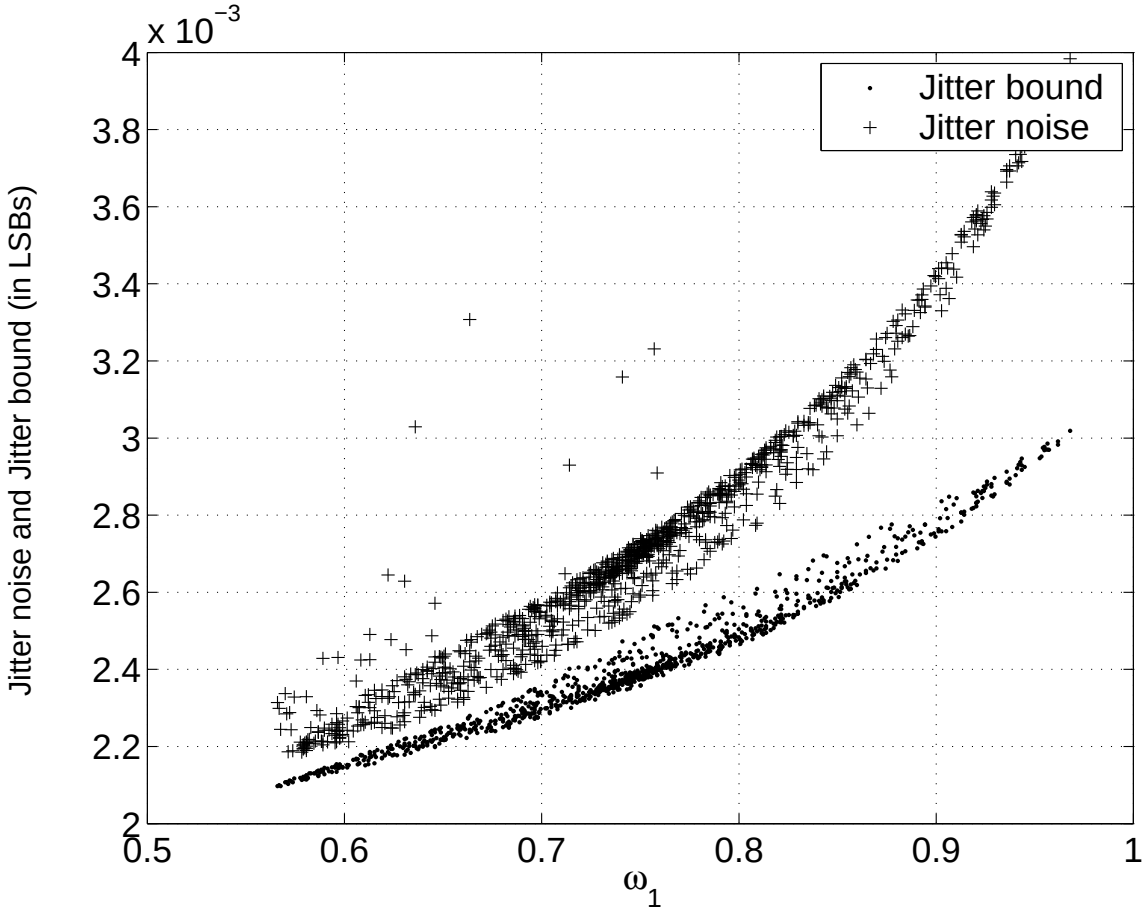


Figure 3.10: Jitter bound and jitter noise as a function of ω_1 for noise transfer functions having same in-band characteristics.

Figure 3.10 shows the jitter noise and the jitter bound (computed from (3.15)) for different fourth order NTFs having the same in-band quantization noise. This figure was generated as follows. The poles of an NTF was perturbed in a manner as to keep the NTF the same at low frequencies. For each NTF so generated, the jitter noise computed using (3.4) and the jitter bound from (3.15) were marked as a function of ω_1. From the figure, we see that for an NTF with a large ω_1 (corresponding to large values of $|NTF|$ at high frequencies), the jitter bound increases. This makes sense, since a large ω_1 implies a large C. Moreover, the actual jitter noise is far away from the bound. Thankfully, it is evident from the figure that the jitter bound is tight and close to being achievable (notice how close the bound and the actual noise are at around $\omega_1 = 0.57$). It turns out that this corresponds to a gentle peak in the NTF. It also turns out that a maximally flat NTF with *an appropriately chosen OBG*, though not optimal for minimizing J, is sufficiently close to the optimum that the jitter bound may actually be used as an estimate of J. The consequences of this observation are explored further in the next section.

3.4 Applications to commonly used NTFs

A useful approximation for the jitter bound of (3.15) can be derived for the family of maximally flat NTFs. The magnitude of an N^{th} order NTF may be written as

$$|NTF(e^{j\omega})| = \frac{\omega^l \prod_{r=1}^{N-l}(\omega - \omega_i)}{|D(e^{j\omega})|} \tag{3.16}$$

where the ω_i denote the zeros of transmission of the NTF within the signal band. Note that $\omega_i << \omega_1$. If the NTF does not have excessive peaking, $|D(e^{j\omega})|$ is approximately

a constant (whose reciprocal is denoted by k) in the range $0 < \omega < \omega_1$, so that

$$|NTF(e^{j\omega})| \approx k\,\omega^l \prod_{r=1}^{N-l}(\omega - \omega_i) \tag{3.17}$$

From the above equation, it is seen that

$$\omega_1 \approx \frac{1}{k^{1/(N+1)}} \tag{3.18}$$

$$C \approx (N+1)\,\omega_1 \tag{3.19}$$

Using the above in (3.15) results in the approximate relation

$$J \geq \frac{\sigma^2_{\Delta T_s}}{T^2}\,\frac{\sigma_q^2\,(\pi - \omega_1)}{\pi\,OSR}\exp\left(\frac{2\,(N+1)\omega_1}{\pi - \omega_1}\right) \tag{3.20}$$

3.4.1 Optimizing In-band Noise

In practice, one would try and minimize the total in-band noise : due to thermal noise, quantization and clock jitter. Thermal noise is always chosen to be several times larger than the quantization noise, so that the performance of the ADC is not limited by quantization noise. This strategy also reduces idle tones by dithering the modulator. The total in-band noise can be reduced by trying to minimize $J + \alpha Q$, where the thermal noise is seen to be $\alpha - 1$ times larger than the quantization noise. Using (3.16), the quantization noise can be approximated as

$$Q \approx \frac{\sigma_q^2}{\pi}\,\frac{\pi^{2N+1}}{(2\,N+1)\omega_1^{2N+2}OSR^{2N+1}}\,C_z \tag{3.21}$$

where $C_z \leq 1$ depends on the position of the NTF zeros ω_i within the signal band. $C_z = 1$ when all the zeros are at $\omega = 0$. From (3.20) and (3.21), it is seen that the jitter noise and quantization noise can be expressed as a function of a single parameter ω_1. As ω_1 increases, Q decreases while J increases. Recall that a higher ω_1 implies a higher out-of-band gain. The total in-band noise can be now optimized with respect to frequency ω_1. Q, J and total noise (assuming $\alpha = 3$) for an example fourth order modulator with a 4-bit quantizer are shown in Figure 3.11. The OSR is 16, and J

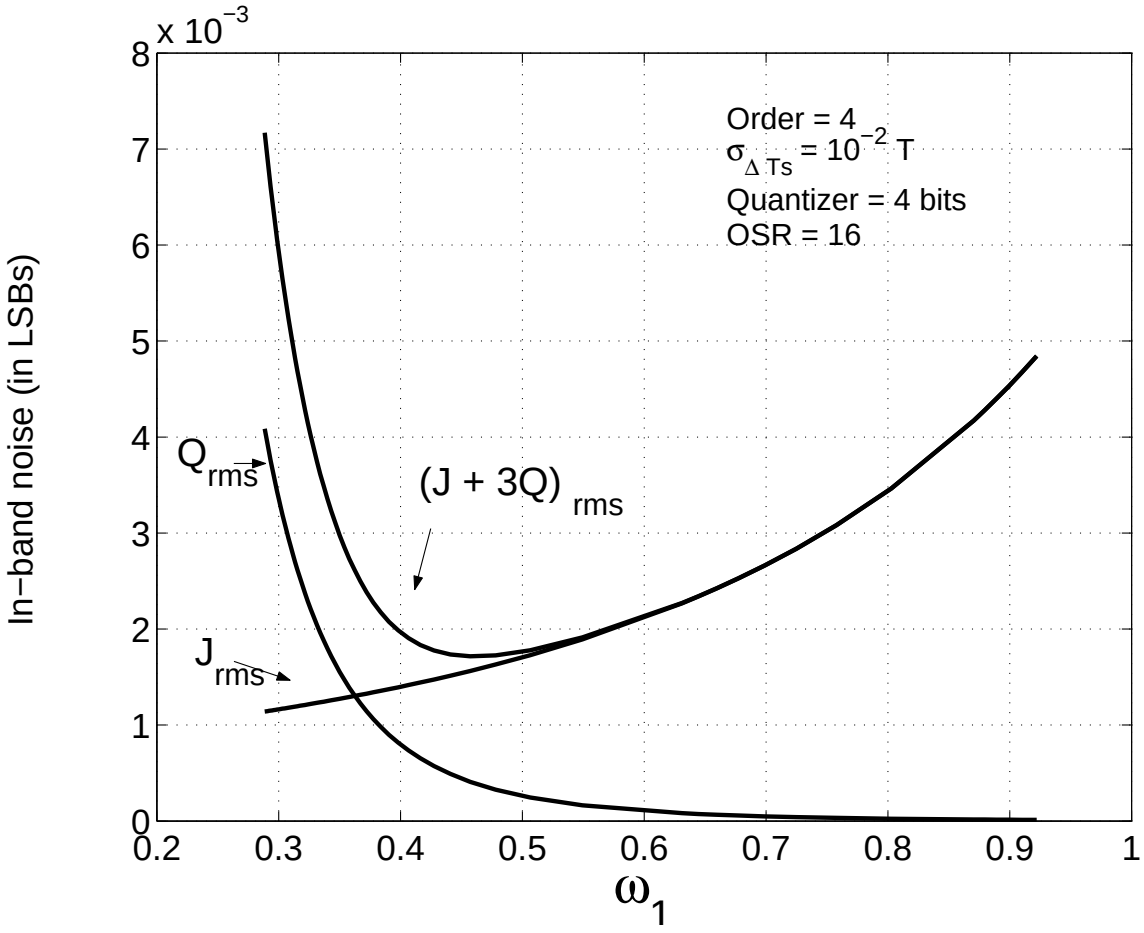


Figure 3.11: J, Q and total noise ($J + 3\,Q$) as a function of ω_1, for a fourth order modulator with a 4-bit quantizer and optimized NTF zeros.

is calculated for a 1% RMS clock jitter. From this plot, it seen that an ω_1 of about 0.44 results in the least amount of total noise. The knowledge of ω_1, along-with the constraint that the NTF is maximally flat can be used to determine the OBG that results

in the least total in-band noise for the modulator.

Alternatively, once ω_1 is known, the Bode Sensitivity integral can be used to arrive at an approximate value of the OBG, as discussed below.

3.4.2 Finding the optimum OBG

Consider a plot of $|NTF|$ shown in Figure 3.12. Let ω_2 denote the frequency at which $|NTF|$ goes to 0 dB. If the NTF can be approximated by (3.16), it is easily seen that ω_2 can be related to ω_1 as

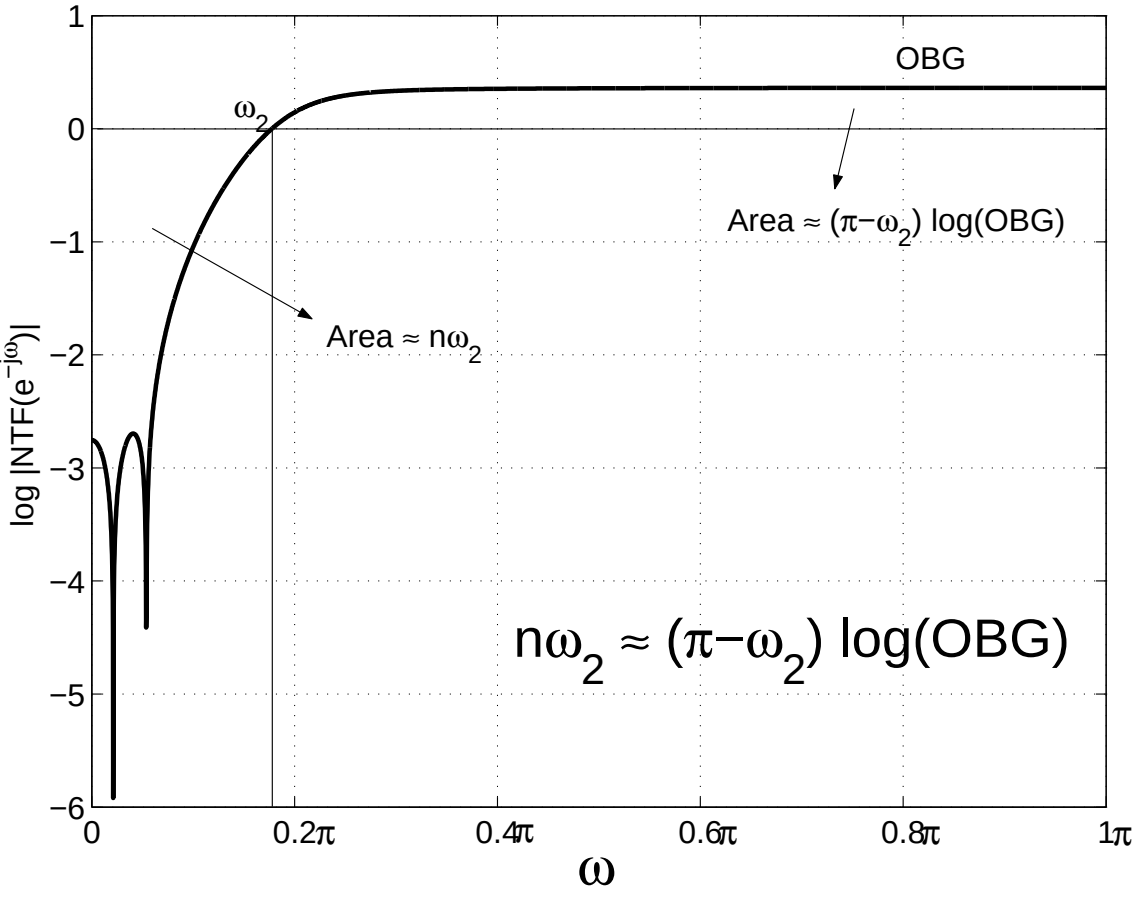


Figure 3.12: The use of the Bode sensitivity integral to determine (approximately) the out-of-band gain that results in the lowest total noise.

$$\omega_2 = \omega_1^{\frac{N+1}{N}} \tag{3.22}$$

The area of $\log\,|NTF(e^{j\omega})|$ below the 0 dB line can be shown to be $N\,\omega_2$. Approximating the area above the 0 dB line as $(\pi - \omega_2)\,\log(OBG)$ and using Bode's sensitivity integral, we see that

$$OBG \approx \exp\left(\frac{N\omega_1^{\frac{N+1}{N}}}{\pi - \omega_1^{\frac{N+1}{N}}}\right) \tag{3.23}$$

3.4.3 Analytic expression for jitter noise for a maximally flat NTF

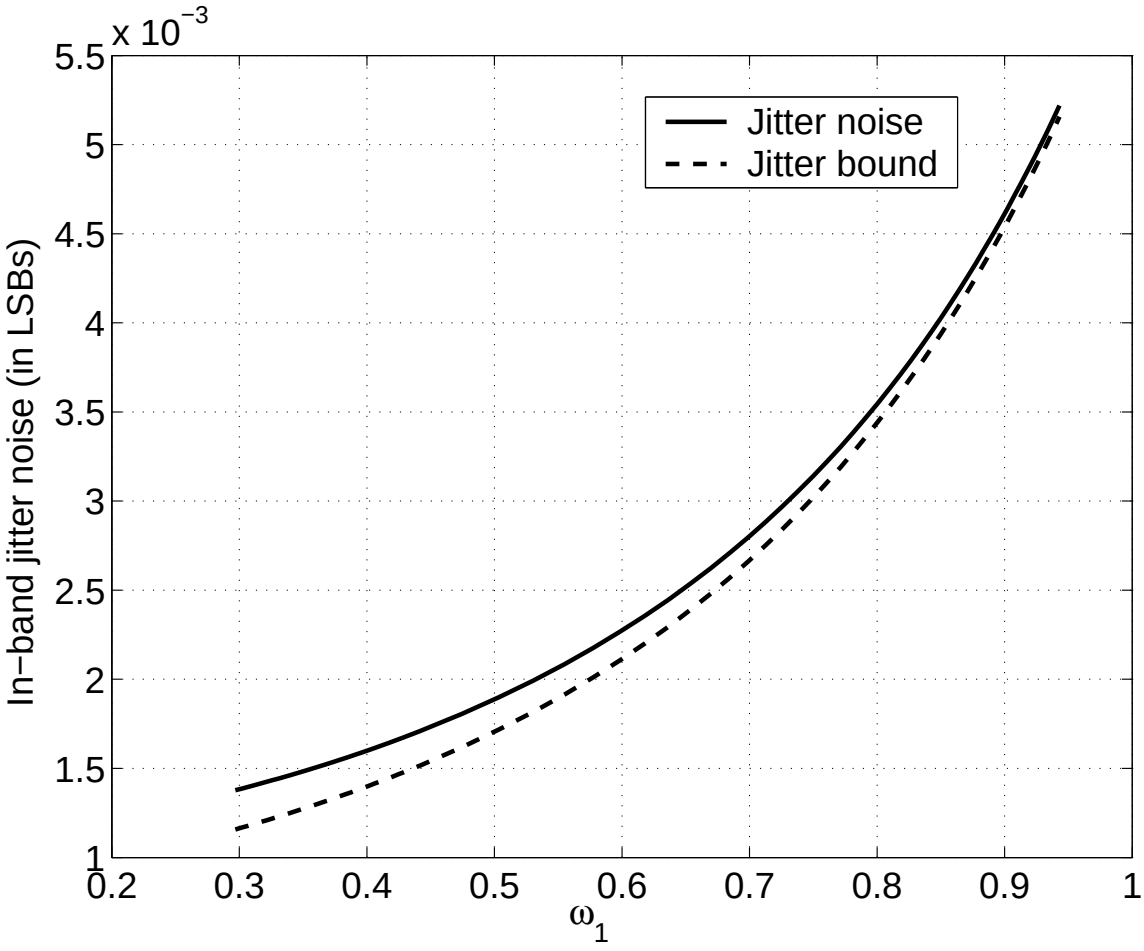


Figure 3.13: Jitter noise and jitter bound for maximally flat noise transfer functions.

Deriving an analytical expression for the jitter noise involves the computation of

(3.5). The magnitude squared response for a maximally flat NTF is given by

$$|NTF(e^{j\omega})|^2 = OBG^2 \frac{\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2n}}{1+\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2n}} \tag{3.24}$$

where ω_c denotes the 3 dB high pass corner of the NTF. As shown in Appendix B, the jitter noise can be derived as

$$J = \frac{\sigma^2_{\Delta T_s}}{T^2} \frac{\sigma^2_{lsb}}{OSR} \frac{8\, B_n^2 \left(\tan(\frac{\omega_c}{2})\right)}{\tan(\frac{\omega_c}{2})} |(c_1 + c_2)| \tag{3.25}$$

where c_1 and c_2 are functions of ω_c. B_n denotes the n^{th} order Butterworth polynomial. Using (3.25), (B.3), and (3.23), jitter noise can be plotted as a function of ω_1, as shown in Figure 3.13. The jitter bound of (3.15) is also plotted on the figure for comparison. It is thus seen that the jitter bound is very close to the actual jitter noise for a maximally flat NTF.

3.5 Clock jitter effects in multi-bit modulators using return-to-zero (RZ) DAC

The analysis of the effects of clock jitter have so far been performed for NRZ feedback DACs. RZ feedback DACs have been traditionally used to mitigate distortion arising from asymmetric rise and fall times in NRZ DACs. In this section, we examine the influence of clock jitter on a CTDSM employing an RZ DAC. Sample NRZ and RZ DAC waveforms are shown in Figure 3.14(a) and (b) respectively. Notice that the height of the pulses in an RZ DAC is twice that in the NRZ case. Moreover, there is now a timing uncertainty with respect to *two* edges. Thus, the error sequence for an RZ

DAC due to clock jitter is given by

$$e_j(n) = 2\,y(n)\left(\frac{\Delta T_{s1}(n)}{T} + \frac{\Delta T_{s2}(n)}{T}\right) \tag{3.26}$$

where $\Delta T_{s1}(n)$ and $\Delta T_{s2}(n)$ are the clocking uncertainties of the n^{th} rising and falling edges respectively.

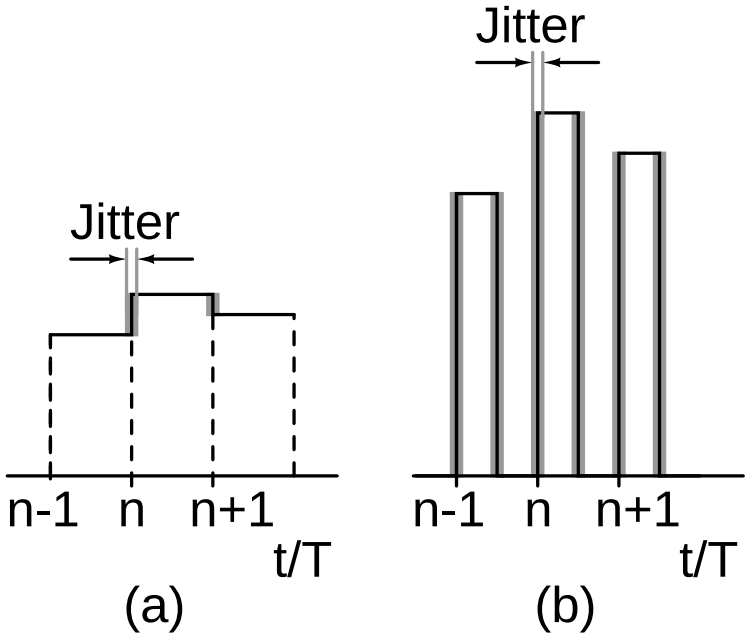


Figure 3.14: NRZ and RZ DAC waveforms.

The variance of e_j is

$$\sigma_{ej}^2 = 4\,\sigma_y^2\,\frac{1}{T^2}\left(\sigma_{\Delta T_{s1}}^2 + \sigma_{\Delta T_{s2}}^2\right) \tag{3.27}$$

Using $\sigma_{\Delta T_{s1}} = \sigma_{\Delta T_{s2}}$, the idle channel in-band jitter noise is given by

$$J_{rz} = 8\,\frac{\sigma_{\Delta T_s}^2}{T^2}\,\frac{\sigma_{lsb}^2}{\pi OSR}\int_0^{\pi} |NTF(e^{j\omega})|^2 d\omega \tag{3.28}$$

Thus, the idle channel in-band jitter noise due to an RZ DAC is worse than the NRZ DAC by a factor given by

$$\frac{J_{RZ}}{J_{NRZ}} = 8\,\frac{\int_0^{\pi} |NTF(e^{j\omega})|^2 d\omega}{\int_0^{\pi} |(1-e^{-j\omega})\,NTF(e^{j\omega})|^2 d\omega} \tag{3.29}$$

Since $|(1-e^{-j\omega})\,NTF(e^{j\omega})|^2 < 4\,|NTF(e^{j\omega})|^2$, we see that the idle channel noise with an RZ DAC is atleast 3 dB higher than the noise with an NRZ feedback DAC. Simulations show that $\frac{J_{RZ}}{J_{NRZ}}$ varies between 4 to 5 dB over NTFs of various orders and OBGs. The performance of CTDSMs with RZ DACs further deteriorate in the presence of an input signal. For large input signals, the jitter noise floor degrades by order of tens of dB. On the other hand, the transitions in a modulator with an NRZ DAC are of the form $y(n)-y(n-1)$. Due to oversampling, the contribution of the signal to jitter noise can be seen to be small.

To confirm the observations above, fourth order modulators with a four-bit quantizer, an OBG of 3 and $OSR = 10$ were simulated. RMS clock jitter was assumed to 1% of the clock period. The input was a single tone with a frequency close to the signal band edge and an amplitude of 80 % of the MSA. When compared to the idle-channel case, the noise floor in the CTDSM using an NRZ DAC increased by about 3 dB. For the RZ DAC case, however, the degradation was 14.2 dB. These simulation results are in line with similar observations elsewhere (Yan and Sanchez-Sinencio (2004),Samid and Manoli (2003)).

It is thus seen that the use of RZ DACs in a multi-bit modulator can lead to severe sensitivity to clock jitter when compared to CTDSMs with NRZ DACs. Much of this jitter noise component occurs due to the input signal, especially at large input

amplitudes.

3.6 Summary and design implications

We summarize the key points arising from the the previous sections and their implications on CTDSM design practice.

- *Jitter noise (J) and Quantization noise (Q) Trade-off* : There is a fundamental trade-off between jitter and quantization noise. For the same NTF shape, a decrease in Q has to be at the expense of J. Placing the zeros of the NTF optimally in the signal band has long been known to reduce Q when compared to an NTF with all zeros are at the origin. For the same Q, therefore, J can be reduced in a design having complex NTF zeros as the OBG for such an NTF will be smaller.
- *NTF Shape* : The most common choice for the shape of the NTF is the maximally flat transfer function. However, many other NTFs which have the same signal-band attenuation but different out-of-band characteristics can be conceived. An NTF with a “gentle" peak, as shown in Figure 3.6 can reduce J when compared to a maximally flat design. However, a modulator with a maximally flat NTF whose OBG has been appropriately chosen will have a jitter noise close to the optimum. The choice of OBG can be made my minimizing $J + \alpha Q$, as discussed in Section 4. With some loop filter architectures (for example, the cascade of integrators with feedforward), choosing an NTF with a peak can result in a peaking Signal Transfer Function (STF), which might not be desirable. In such a scenario, STF peaking can be mitigated by appropriate choice of the loop filter topology (Schreier and Temes (2005)).
- *Effect of Excess Loop Delay:* Excess loop delay due to the latency of the quantizer is known to cause peaking in continuous-time delta sigma modulators, if nothing is done to compensate for the excess delay (Cherry and Snelgrove (1999*b*)). Hence, a modulator with a nominal NTF that is maximally flat will exhibit peaking in the presence of excess loop delay. The magnitude of the peak depends on the amount of excess delay. From the discussion in Section 3.3, it is apparent that a small amount of excess delay is beneficial as it reduces the jitter noise J. Simulations of a fourth order modulator with a 4-bit quantizer (maximally flat NTF with OBG=2.5) show that with an RMS clock jitter of 1%, RMS jitter noise with and without an excess loop delay of $0.1\,T_s$ are 3.13×10^{-4} and 3.46×10^{-4} respectively.

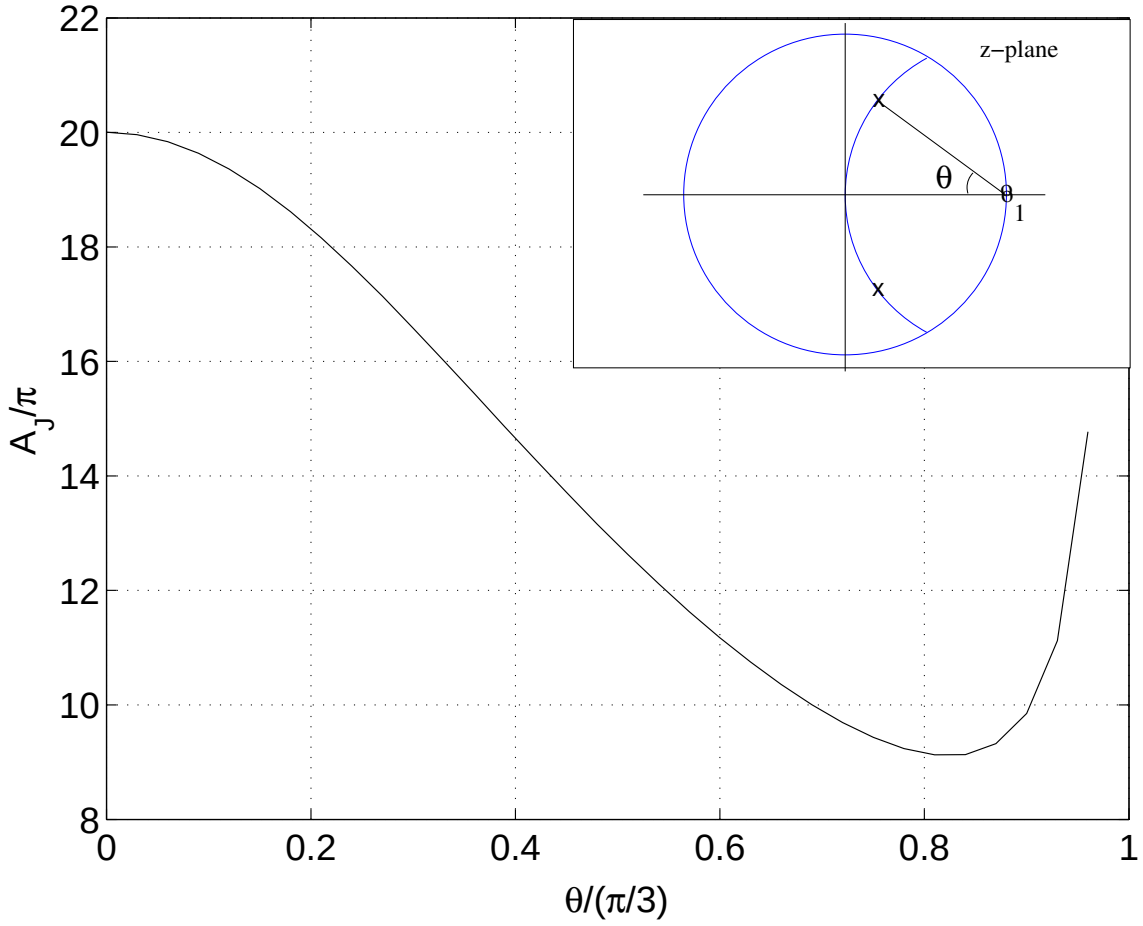


Figure 3.15: A_J/π as the poles are moved along an arc of unit radius centered at $z = 1$. The inset shows the pole-zero map of the second order NTF.

3.6.1 Special Case of a Second Order NTF

A second order loop with both poles at the origin, resulting in an NTF of $(1-z^{-1})^2$ is commonly used. The same in-band behaviour can be obtained by moving the poles along the arc of an arc of unit radius, centered at $z = 1$, as shown in the inset of Figure 3.15. As the poles approach the unit circle ($\theta = \pi/3$), the peaking in the NTF progressively increases. Thus, as θ is increased from 0 to $\pi/3$, the area under the $|NTF(e^{j\omega})(1-e^{-j\omega})|^2$ curve (A_J) first decreases and then increases as shown in the figure. When compared to the case with both poles at the origin ($\theta = 0$), A_J is seen to be a smaller for a peaky NTF (with $\theta \approx 0.8\frac{\pi}{3}$) by more than a factor of 2, resulting in a jitter noise that is lower by about 3.5 dB. Simulations show that the peak SQNR is virtually unaffected as θ varies over the range $0 - 0.85\frac{\pi}{3}$. It is thus seen that a proper choice of pole positions enables the modulator to tolerate more than twice the amount of white clock jitter for the same jitter noise.

3.7 Experimental results

A $\Delta\Sigma$ DAC was used as a test vehicle to verify some of the results in this chapter. Note that the analysis presented in the previous sections applies directly to DACs. An Agilent 33120A arbitrary waveform generator (AWG), the details of which are shown in Figure 3.16, is used as a $\Delta\Sigma$ DAC as described below. The AWG has an internal memory of 16000 words, with each word being 13 bits wide. The input data (which is a $\Delta\Sigma$ modulated sequence generated numerically) to the AWG is downloaded into the internal memory from a computer. A 13-bit Nyquist rate DAC with a fixed sampling clock of f_s = 40 MSPS converts the digital word read from the internal memory of the

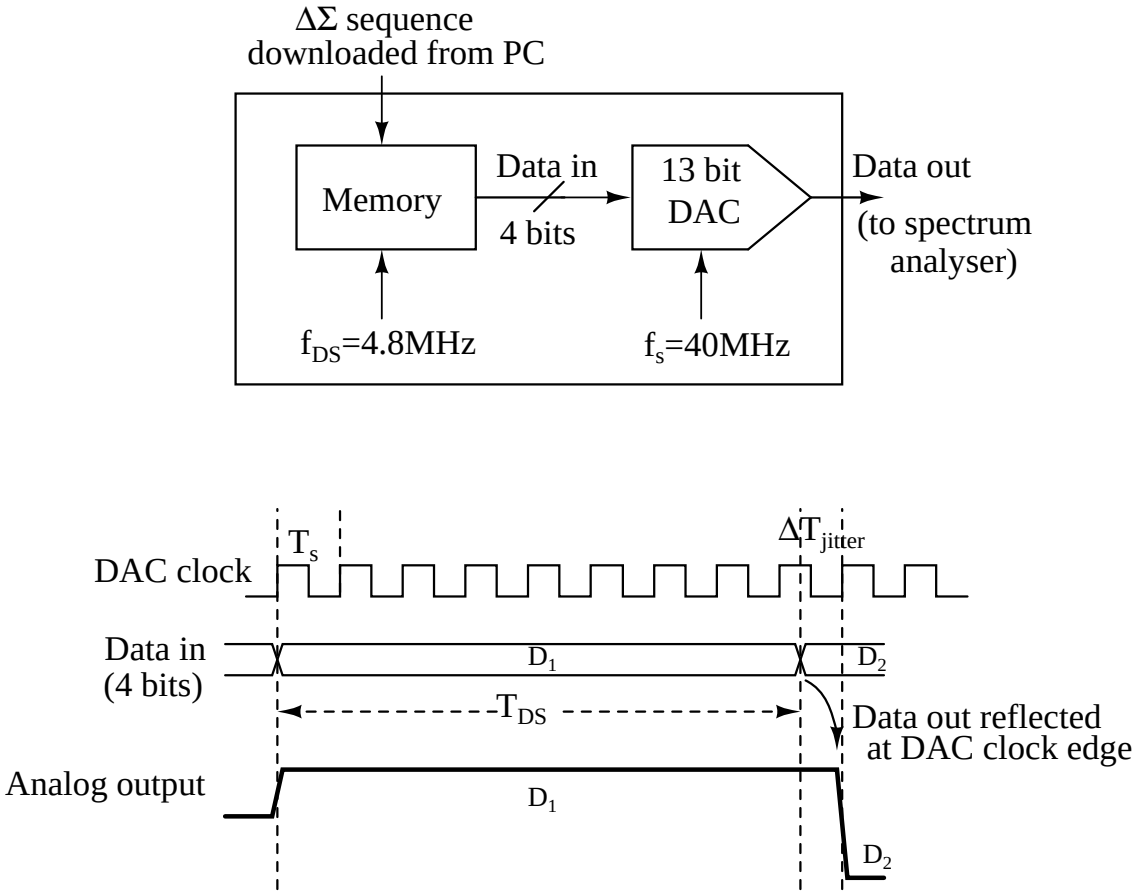


Figure 3.16: Experimental Setup.

AWG into an analog output. In other words, the analog output can only change at time instances which are integral multiples of $1/f_s$. The rate at which data is read from the memory is set on the front panel of the instrument. Note that the "data read" rate can be set independently of f_s. This forms the sampling rate of the $\Delta\Sigma$ DAC and is denoted as f_{DS}. If f_{DS} is set to a value that is not a factor of f_s (see Figure 3.16), the output of the AWG cannot change exactly at multiples of $1/f_{DS}$, but does so at the next rising edge of the internal sampling clock f_s - thereby resulting in a jittery output waveform. The AWG output is observed on an Agilent E4401B spectrum analyzer.

Fourth order noise transfer functions with f_{DS} fixed at 4.8 MHz and the $OSR = 16$ were used in the experiments. A four bit DAC sequence was used, in effect using only the 4 MSBs of the 13 bit internal DAC of the AWG. The zeros of the NTF were optimally spread Schreier (1993). The general form of the NTFs was

$$NTF(z) = \frac{\sum_{k=0}^{4} a_k z^{-k}}{\sum_{k=0}^{4} b_k z^{-k}} \tag{3.30}$$

Measurements were made for NTFs with various OBGs and shapes. The denominator coefficients of the NTFs are shown in Tab. 3.7. The coefficients of the numerator are the same for all NTFs: $a_0 = a_4 = 1, a_1 = a_3 = -3.9670$ and $a_2 = 5.9342$.

Table 3.2: Denominator Coefficients of the NTFs

NTF Type	b_0, b_1, b_2, b_3, b_4
Maximally Flat,OBG=3	1, -1.8975, 1.6164, -0.6665, 0.1092
Maximally Flat,OBG=7	1, -0.6923, 0.4194, -0.1361, 0.0186
Peaking NTF (with same quantization noise as the NTF with an OBG=7)	1,-1.775,2.1284,-1.1896,0.4479

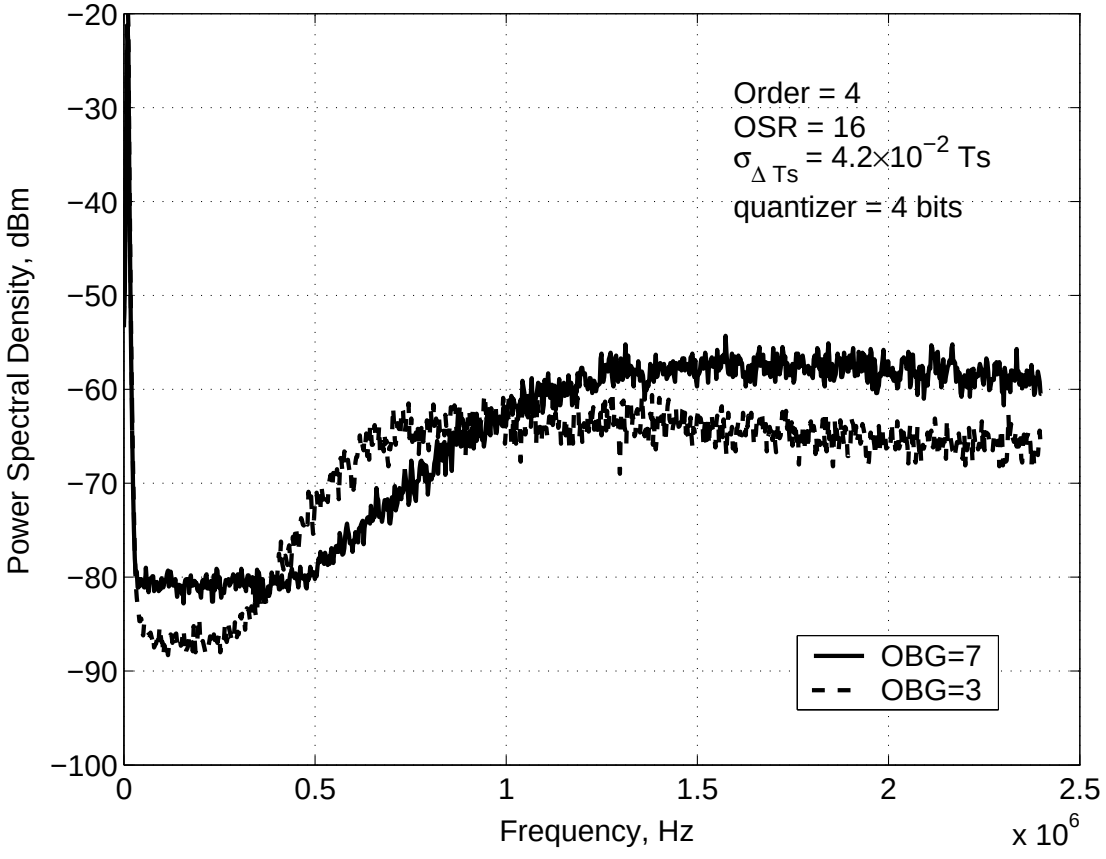


Figure 3.17: Measured $\Delta\Sigma$ DAC spectra for maximally flat NTFs with different out-of-band gains.

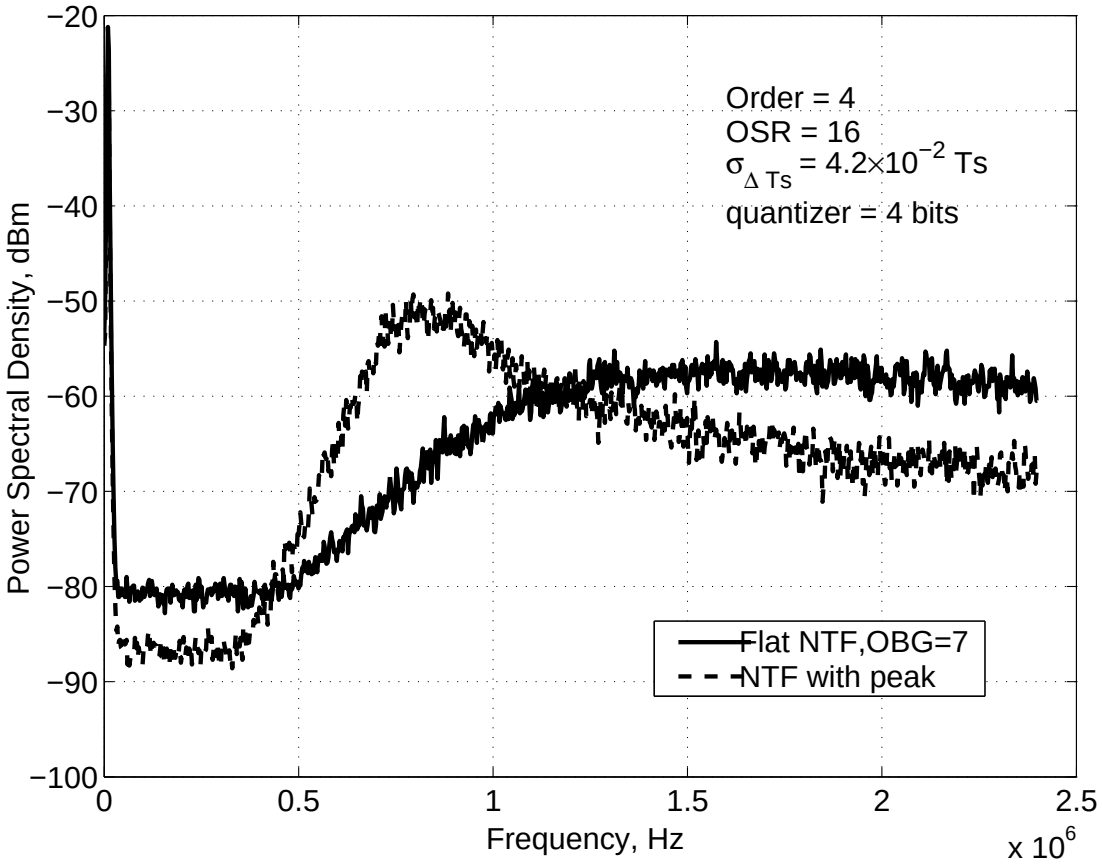


Figure 3.18: Measured $\Delta\Sigma$ DAC spectra for NTFs with the same in-band response but different out of band characteristics.

Figure 3.17 shows the DAC output spectra for two maximally flat NTFs with out-of-band gains of 3 and 7. Notice that the DAC with the lower out-of-band gain has *lower* in-band noise, as the noise is dominantly that due to clock jitter. Figure 3.18 shows the spectra for two NTFs that have the same response in the signal band. However, one of them is designed to have peaking out of band, while the other has a maximally flat transfer function. It is seen that the NTF with a carefully chosen peak has lower in-band noise when compared to the maximally flat one, for the same in-band quantization noise, confirming the analysis of Section 3.3. The jitter bound and the corresponding measured in-band noise for the three NTFs are tabulated in Table 3.7. In this case, the

Table 3.3: Comparison of Jitter noise with experimental results

NTF	Jitter bound (mV)	RMS In-band noise (mV)
Maximally Flat,OBG=3	1.4	2.1
Maximally Flat,OBG=7	2.53	4.1
Peaking NTF	1.85	2.1

quantization noise is very much negligible compared to the in-band noise. Hence we can consider the in-band noise to be dominated by jitter noise. It could be seen that the NTF with peaking has a low jitter bound and its jitter noise is close to the bound when compared to the maximally flat NTF with OBG of 7, again confirming the analysis of Section 3.3.

3.8 Summary

In this chapter, we investigated the ramifications of the choice of the NTF in a CTDSM on the sensitivity with respect to clock jitter. Using the Bode sensitivity integral, we derived a lower bound on the jitter noise in a single-loop CTDSM with white

clock jitter. We showed that in a CTDSM, quantization noise and jitter noise cannot be reduced simultaneously. Optimally spread zeros in the NTF also help in reducing jitter sensitivity, since a lower OBG can be used to achieve the same quantization noise. An NTF with moderate peaking was shown to have a lower jitter noise than a maximally flat NTF for the same in-band quantization noise, thereby giving intuition to the result in Hernandez *et al.* (2004), arrived at using numerical methods. A maximally flat NTF, though not optimal for jitter performance, was shown to be very close to the optimal NTF, provided the right OBG was chosen. Based on the Bode sensitivity integral, simplified expressions for jitter and quantization noise in a modulator with a maximally flat NTF were given. Some aspects of the theory were verified through experiments on a $\Delta\Sigma$ DAC.

CHAPTER 4

Design of a third order CT $\Delta\Sigma$ modulator

4.1 Introduction

The proposed third order modulator is operated at 300 MHz. It employs a 4 bit internal quantizer and targets a resolution of 12 bits for a signal bandwidth of 15 MHz. The overall power target for the design is 20 mW from 1.8 V supply.

4.2 Choice of the NTF

To meet the specifications of the modulator, various choices for the NTF are possible. The various parameters which decide the choice of the NTF are:

- order of the NTF
- out of band gain (which decides both the in-band quantization noise as well as the maximum stable amplitude)
- quantizer resolution
- oversampling ratio of the modulator

For the specifications targeted, a fourth order NTF with an OBG of 3, a 4 bit internal quantizer and OSR of 10 was chosen. An NRZ feedback DAC is chosen. The NTF of the modulator is shown in Figure 4.1. The zeros of the modulator are optimized for minimum in-band noise using the method given in Schreier (1993). The SNR vs amplitude plot is shown in Figure 4.2. The peak SNQR achieved is 79.5 dB at input amplitude of -1.7 dBFS. In the presence of clock jitter of 5 ps, the peak SNR obtained is 75.5 dB.

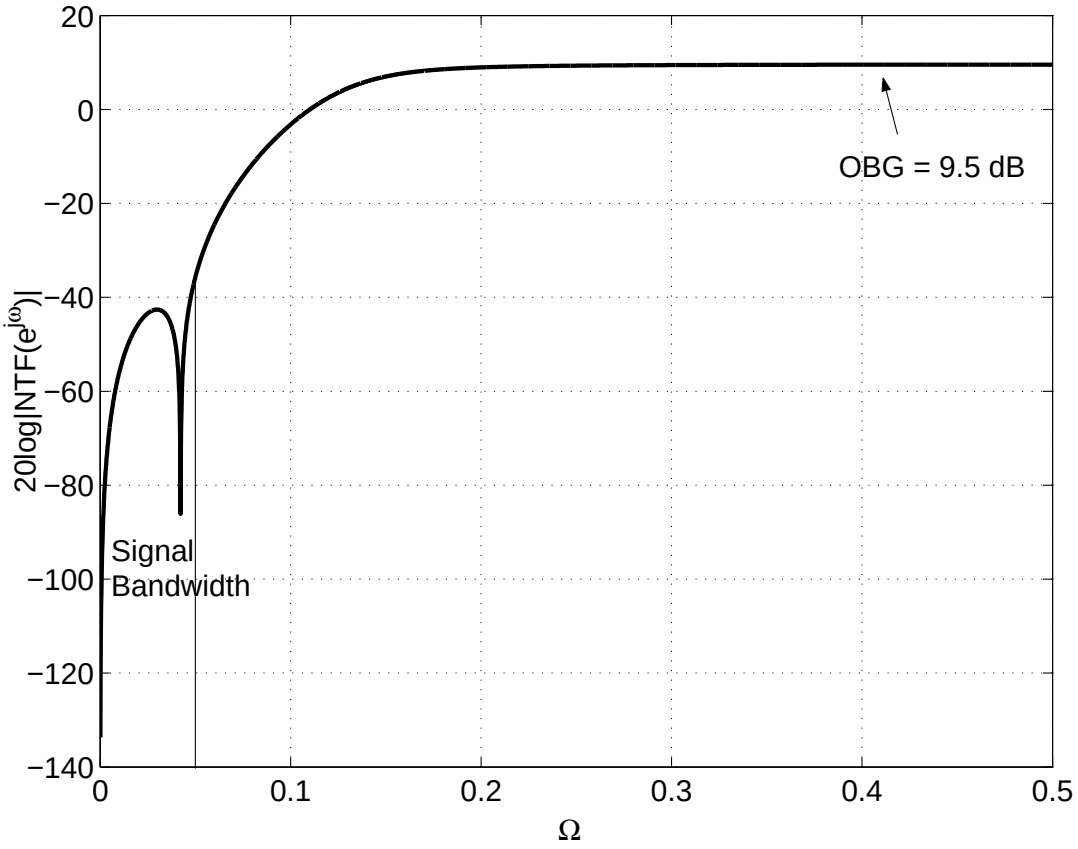


Figure 4.1: Noise Transfer function

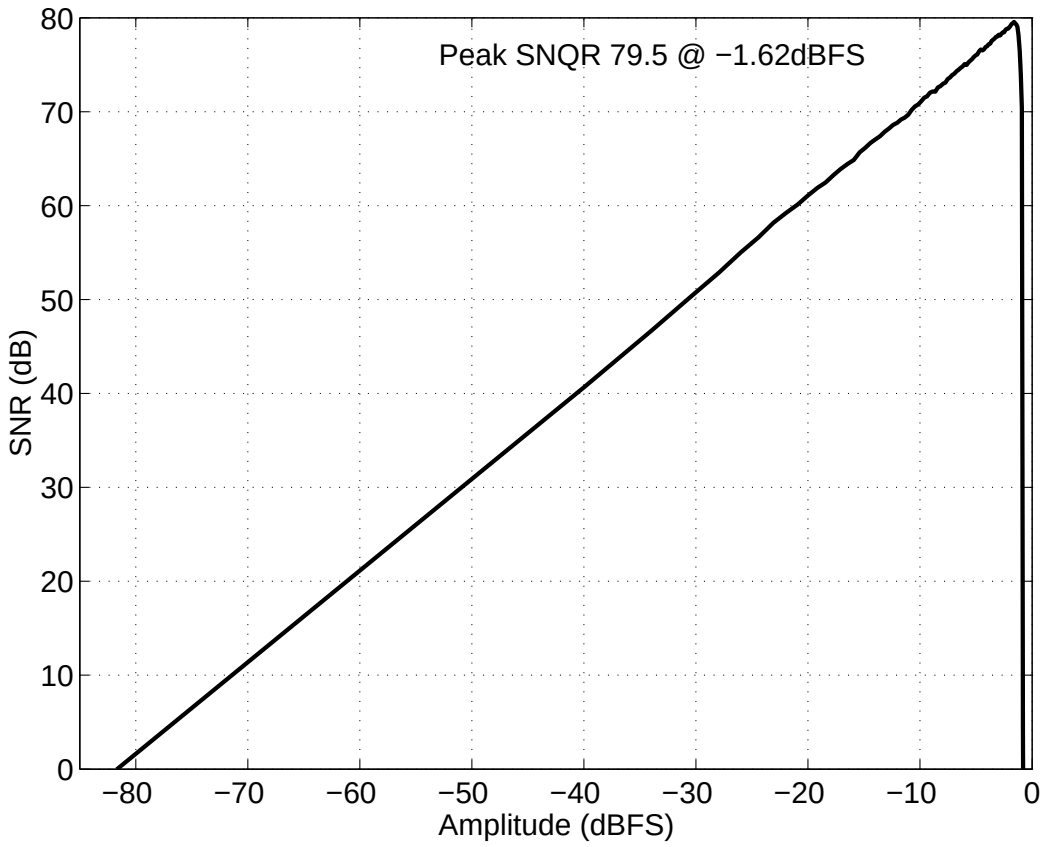


Figure 4.2: SNQR vs Amplitude plot

4.3 Architecture of the modulator

The architecture of the single loop $\Delta\,\Sigma$ modulator is shown in Figure 4.3. The main building blocks of the modulator are

- Loopfilter
- Analog to Digital Converter
- Digital to Analog Converter
- Dynamic element Matching

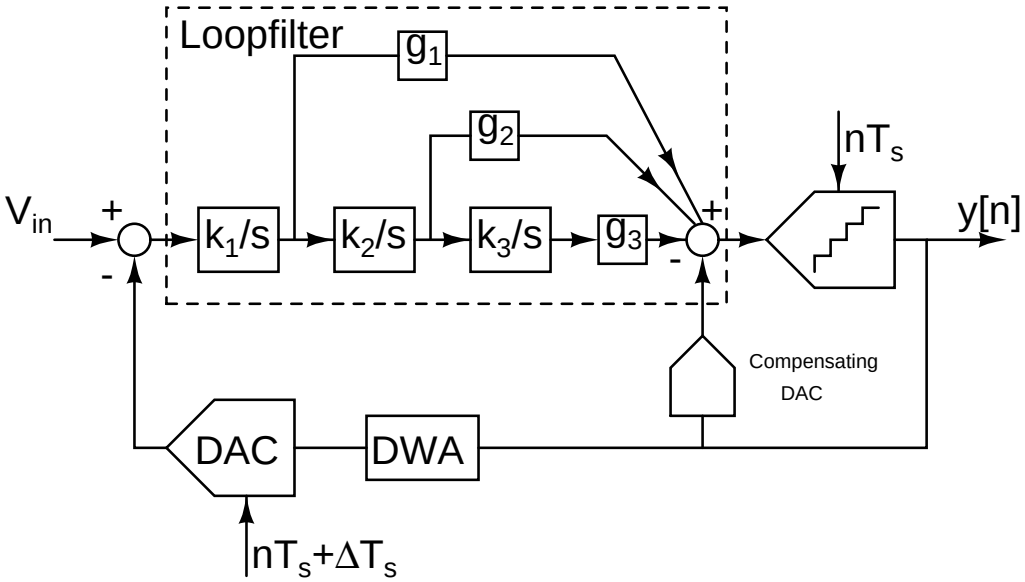


Figure 4.3: Architecture of the $\Delta\Sigma$ Modulator

The loopfilter is a third order continuous time filter implemented using opamp RC integrators. It is observed that the third order filter was enough to get the fourth order roll off required for the NTF when the excess loop delays became a big factor of the clock time period T_s. In this design, the excess loop delay is 2 ns ($0.6\,T_s$) which was large enough to have only three integrators to match the desired NTF. The trade off is that the in-band noise increases by approximately 2 dB. Hence the peak SNQR is around 77.5 dB.

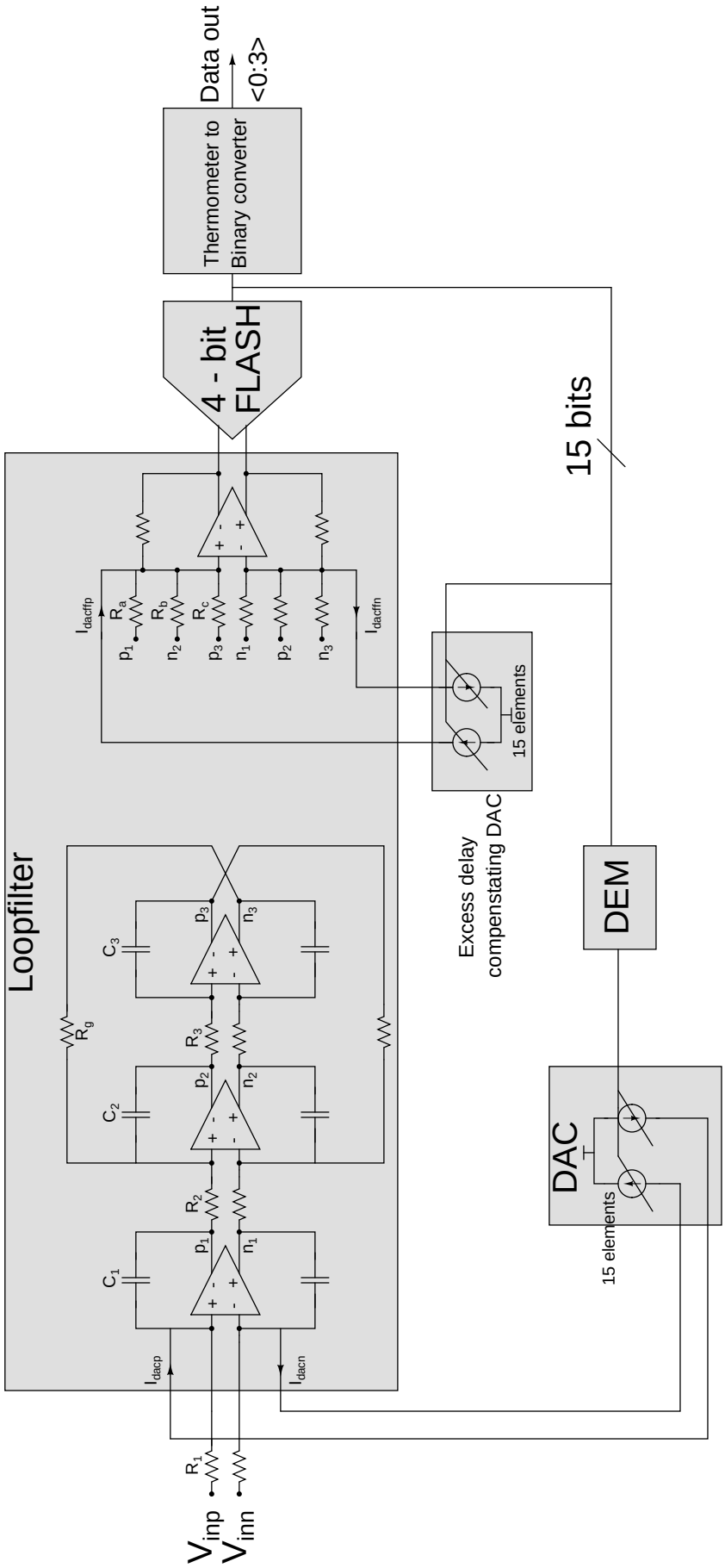


Figure 4.4: Architecture of the $\Delta\Sigma$ Modulator

The quantizer is a 4-bit flash ADC followed by the dynamic element matching which incorporates the Data Weighed Averaging algorithm (Baird and Fiez (1995)). The DAC uses both nMOS and pMOS current sources and a current steering DAC. The output binary code is obtained by summing the 15 bits of the thermometer code. The detailed block diagram of the modulator is shown in Figure 4.4. The details of each block are explained in the following sections of this chapter.

4.4 Loopfilter

The loopfilter is shown in Figure 4.5. It is a cascade of integrators with feedforward summation (CIFF).

Resistor	Value (kΩ)	Capacitor	Value (fF)
R1	7.5	C1	125
R2	45	C2	338
R3	29	C3	338
Rg	50		
Ra	13		
Rb	4.6		
Rc	4.3		

Table 4.1: RC values of the integrators and summer in the loopfilter

The factors which determine the choice of the R and C among the various values possible are: 1) input referred noise of the system 2) Node voltage swing. The first integrator resistor is the major contributor of the input referred noise and is thus decided by this noise. For the other integrators, the RC product are determined so as to have node swings equal to the maximum input swing. Having a large resistor (small capacitor) would be preferred to reduce power dissipation in the integrating opamp. Since the resistor is realized on the chip as poly resistor, the larger its value, the larger would be its

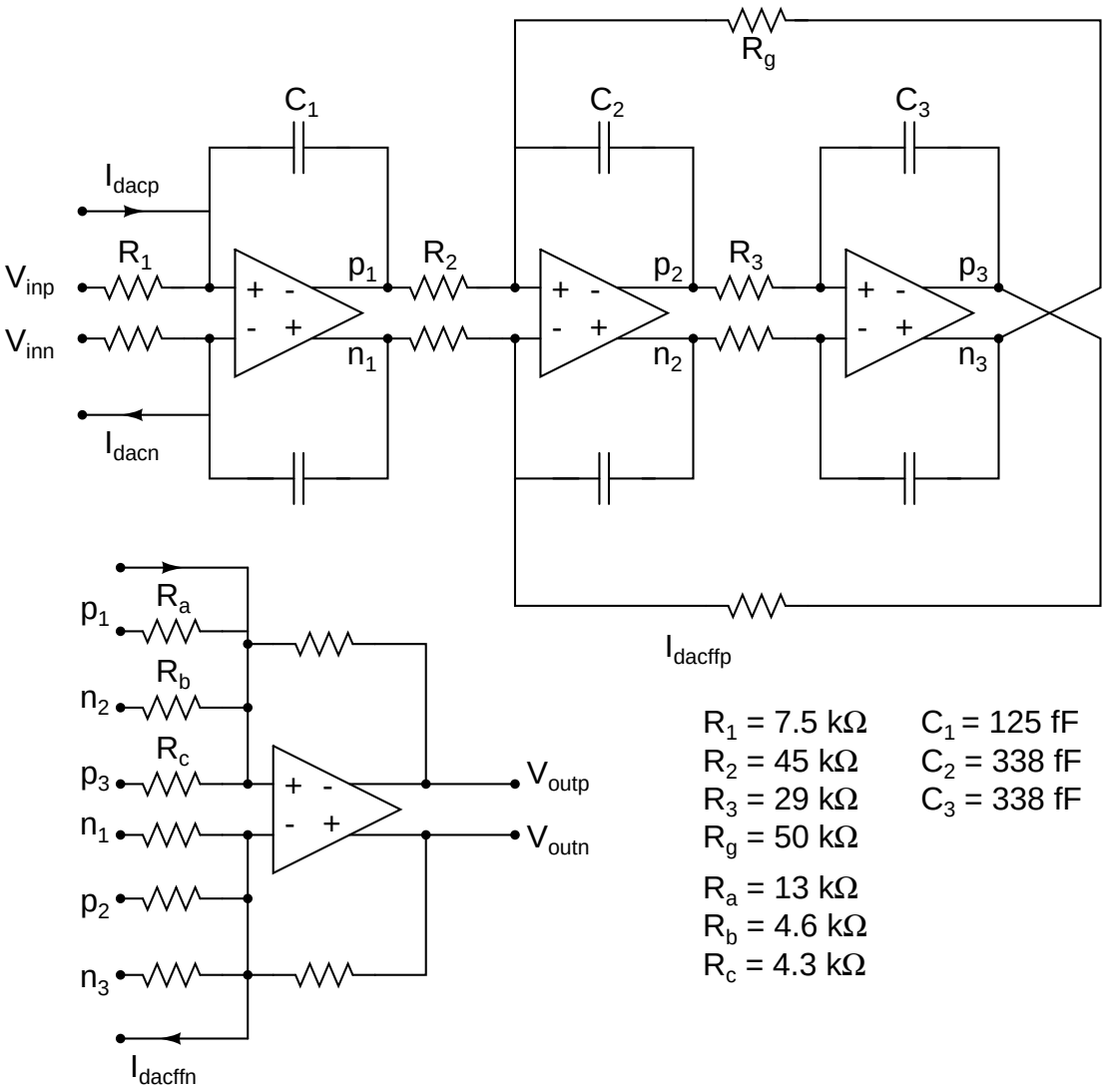


Figure 4.5: Loopfilter Block diagram

distributed capacitance. Hence it is restricted to the order of tens of kΩ. The values of the resistors and capacitors are given in Table 4.1 and are also shown in the Figure 4.5. The RC product varies by around $\pm 40\%$ across the process corners. This variation was overcome by having a bank of switchable capacitors. The schematic of the capacitor bank is shown in Figure 4.6. It is a bank of four capacitors with one capacitor being always connected and the others connected through a nMOS switch. The scaling factor of the capacitors are 0.3, 0.4, 0.5 and 0.7. Depending on the process corner, various combinations of the capacitor are used. The bank of capacitors reduces the maximum RC variation to around 10%.

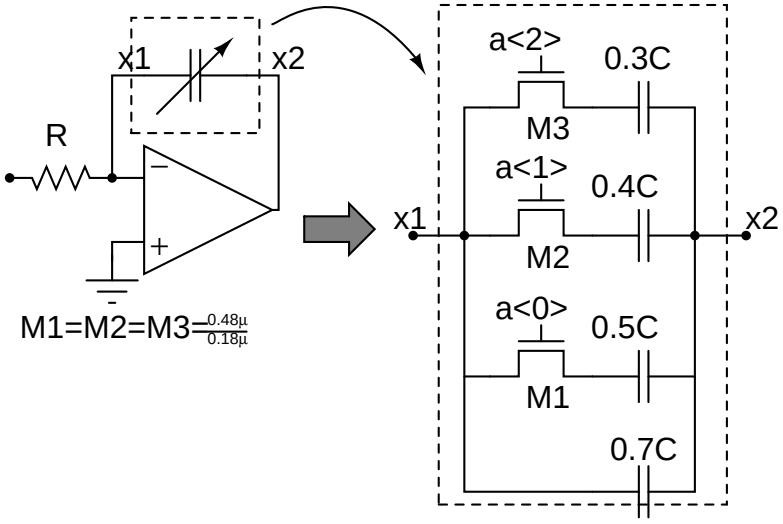


Figure 4.6: Schematic of the capacitor bank

Opamp design

A two stage opamp with Miller compensation was implemented as shown in Figure 4.7. The first stage is a telescopic stage and has a high DC gain. The second is a common source stage with a high output swing. The sizes of the components along with their operating points are shown in Table 4.2. The dc gain of the opamp is 71.2 dB.

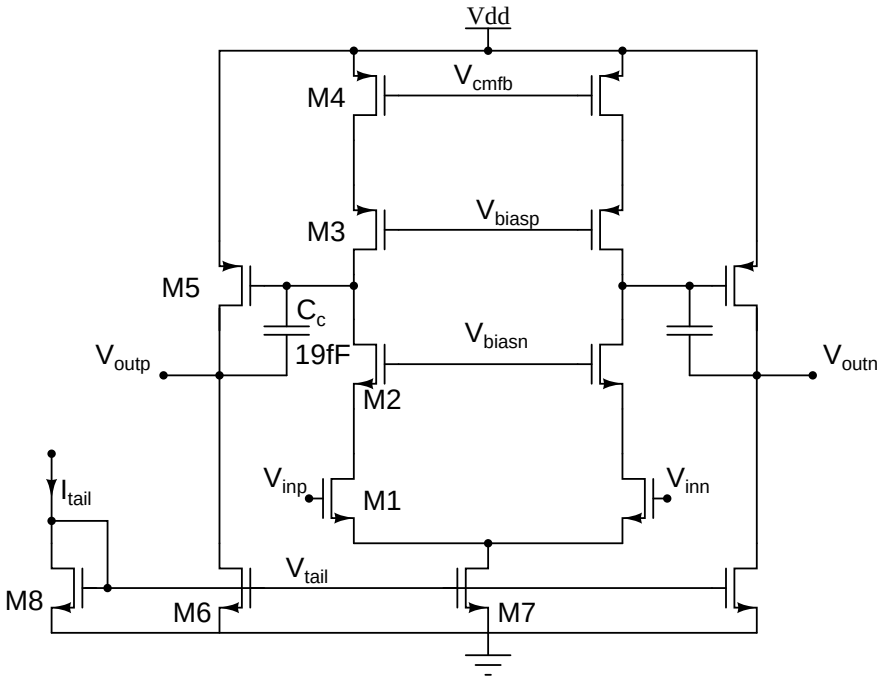


Figure 4.7: Schematic of the integrating opamp

	M_1	M_2	M_3	M_4	M_5	M_6	M_7
Size	$8(\frac{4}{0.72})$	$8(\frac{1}{0.18})$	$24(\frac{1}{0.24})$	$24(\frac{1}{0.24})$	$32(\frac{1}{0.18})$	$32(\frac{1}{0.18})$	$16(\frac{1}{0.18})$
I (mA)	0.11	0.11	0.11	0.11	0.61	0.61	0.22
ΔV (mV)	156	157	220	216	300	167	155
g_m (mS)	1.25	1.26	1.02	1.01	3.75	6.26	2.46
r_o (kΩ)	34	12.5	34.5	24.3	6.4	3.7	5.6

Table 4.2: Transistor sizes of the first integrator opamp

The common mode feedback circuit (CMFB) circuit is a replica of the first stage of the opamp, shown in Figure 4.8. When the input to the opamp is cut off, the CMFB circuit becomes dysfunctional. In order to have the output functional even in such conditions, the drains of M_9 and M_{11} are connected to the output of the first stage and thus keep the CMFB loop active (Banu *et al.* (1988)).

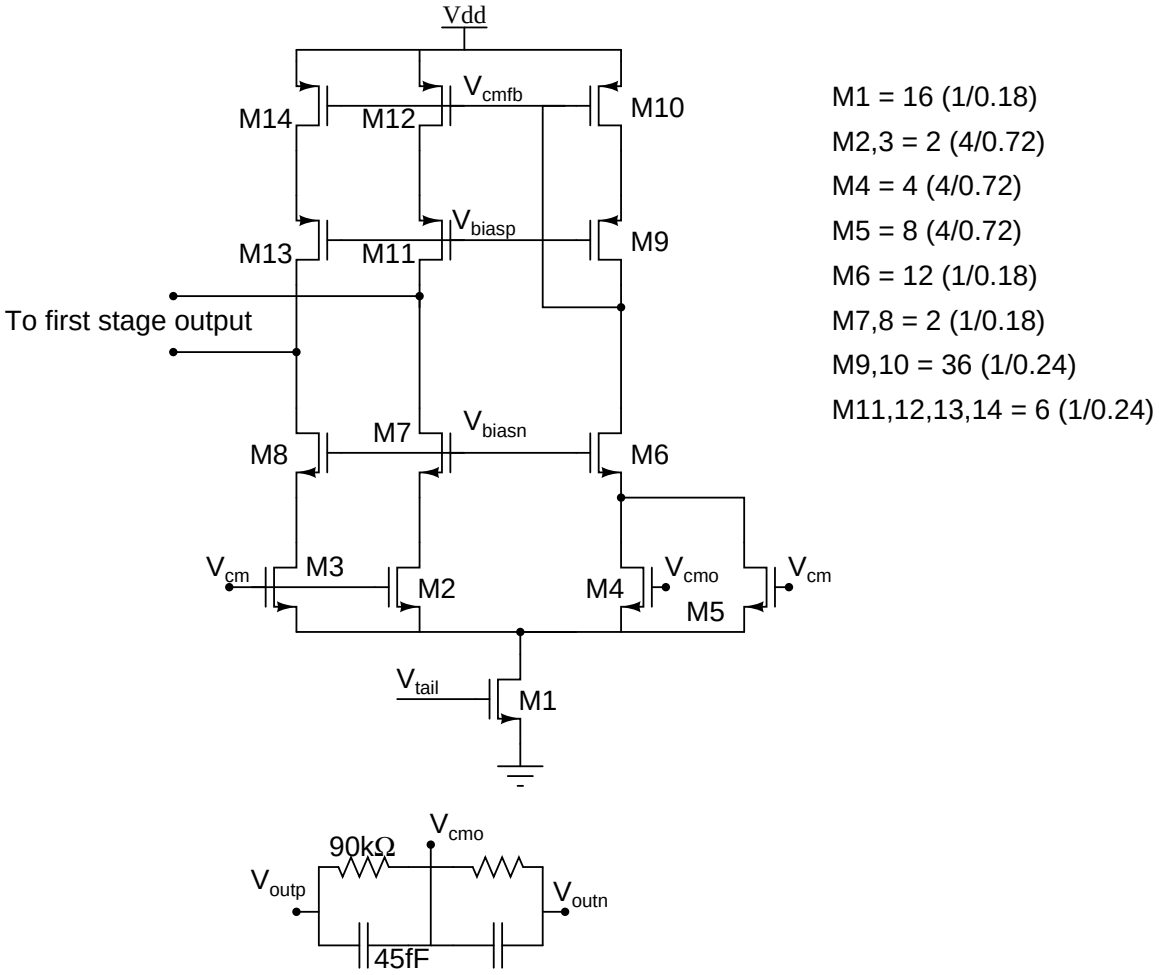


Figure 4.8: Schematic of the CMFB circuit

Bias Circuits

The bias circuit for the opamp consists of the following blocks: a fixed transconductance bias circuit, a current distribution circuit for mirroring the currents to the opamp

and a cascode bias generator. A fixed gm bias circuit (Zele and Allstot (1996)) (shown in Figure 4.9) servos the transconductance (gm) of the input pair MOS of the opamp to an off chip resistor. It generates the bias current which is mirrored to the opamp. This current is also used to generate the cascode bias voltages. The variation of the input pair opamp transconductance across all process, temperature and supply corners is around 12%. The current distribution circuit is shown in Figure 4.10. In the opamp, the current is mirrored from transistor M_8 to M_7 (refer to Figure 4.7). Because of the variations in v_{ds} of the transistors(M_8 and M_7), there would be mismatch in the currents. To compensate for this, the current is pre-distorted in the current distribution circuit when mirroring from M_1 to M_3 (Pavan *et al.* (2005)). The cascode bias generation circuit is shown in Figure 4.11.

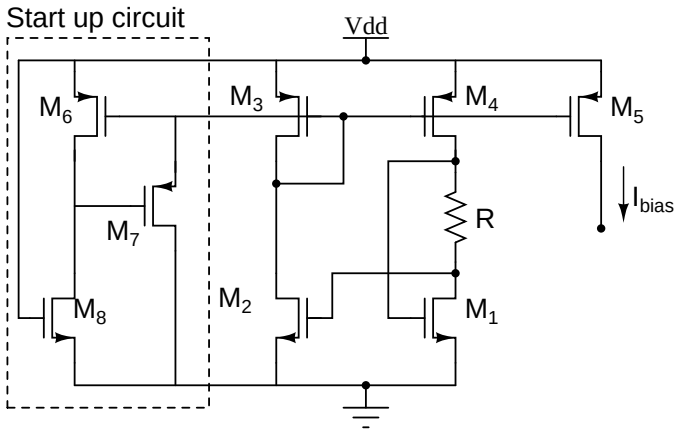


Figure 4.9: Schematic of the fixed gm bias

4.5 Low power 4-bit Flash ADC Design

The ADC used in the modulator is a 4 bit flash design. The output of the flash ADC is a thermometer code which drives the DEM and the DAC blocks that follow

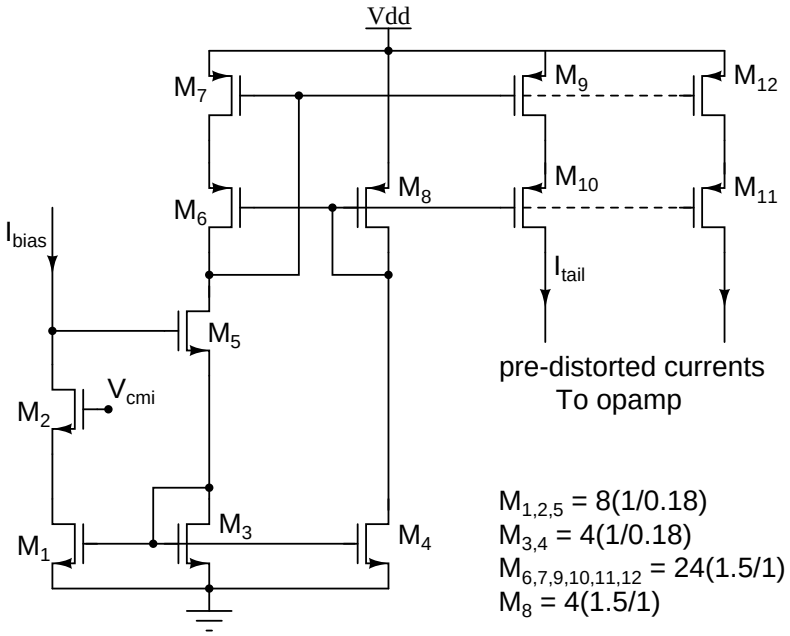


Figure 4.10: Schematic of the current distribution circuit

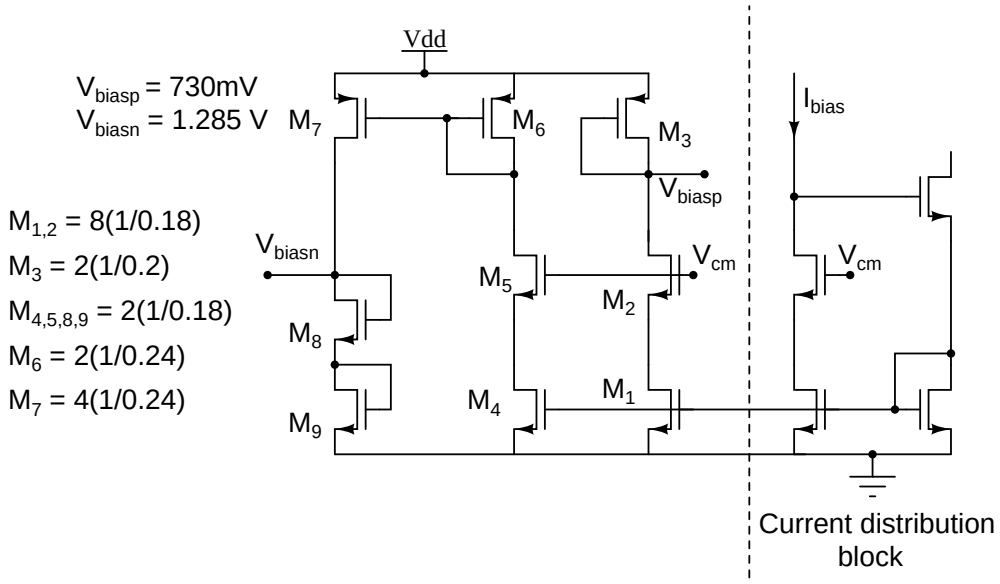


Figure 4.11: Schematic of the cascode bias generation circuit

it. The block diagram of the flash is shown in Figure 4.12. It consists of two main blocks, a bank of 15 comparators and the reference generator for the comparators. Each comparator compares the input signal with each reference level and gives the output digital data. A logic level of one is output if the input is more the reference and a zero is obtained if input is less than the reference. The 15 reference levels are tapped from the 15 nodes of the resistor ladder.

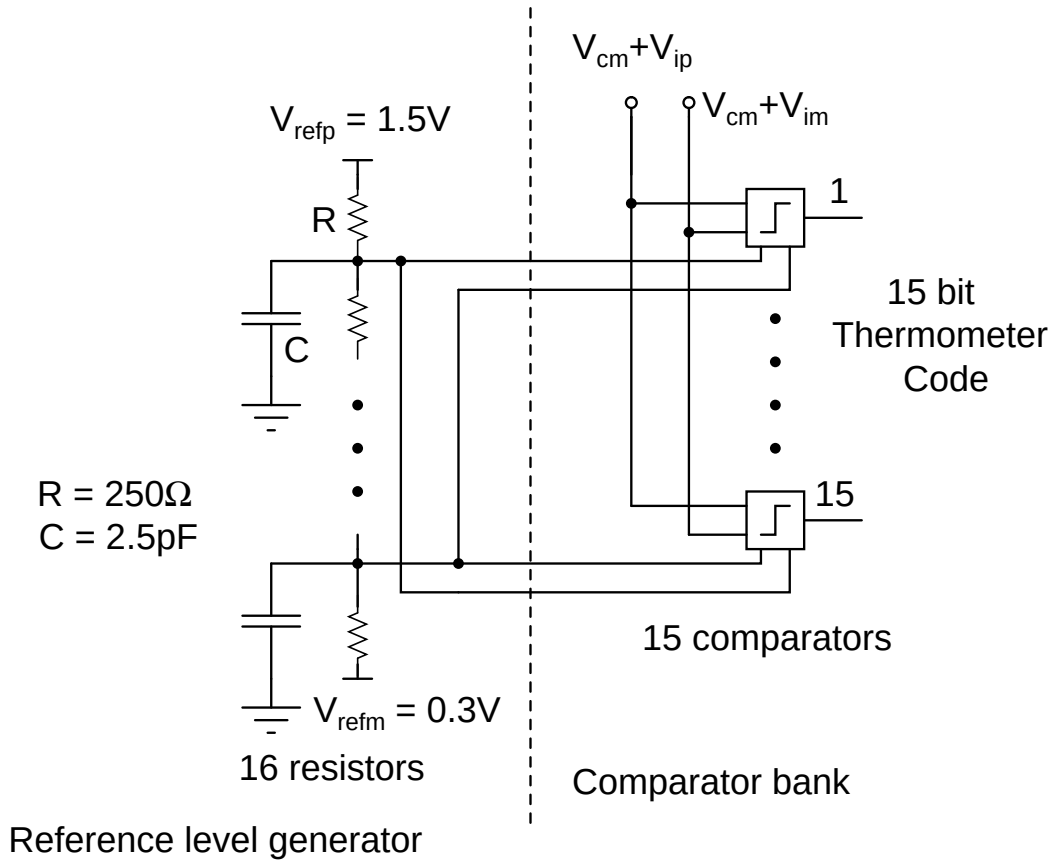


Figure 4.12: Block diagram of the 4-bit flash ADC

4.5.1 Comparator

The schematic of the comparator is shown in Figure 4.13. The comparator consists of a coupling capacitor ‘C’ which stores the references. The input signal of the flash ADC is coupled to the input of the latch through this capacitor. The latch is a back-

to-back connected inverter. The latch regenerates to appropriate logic levels difference between the input and the reference which are stored by a C^2MOS inverter. The outputs are buffered to drive the next stage DEM. The entire comparison operation takes place

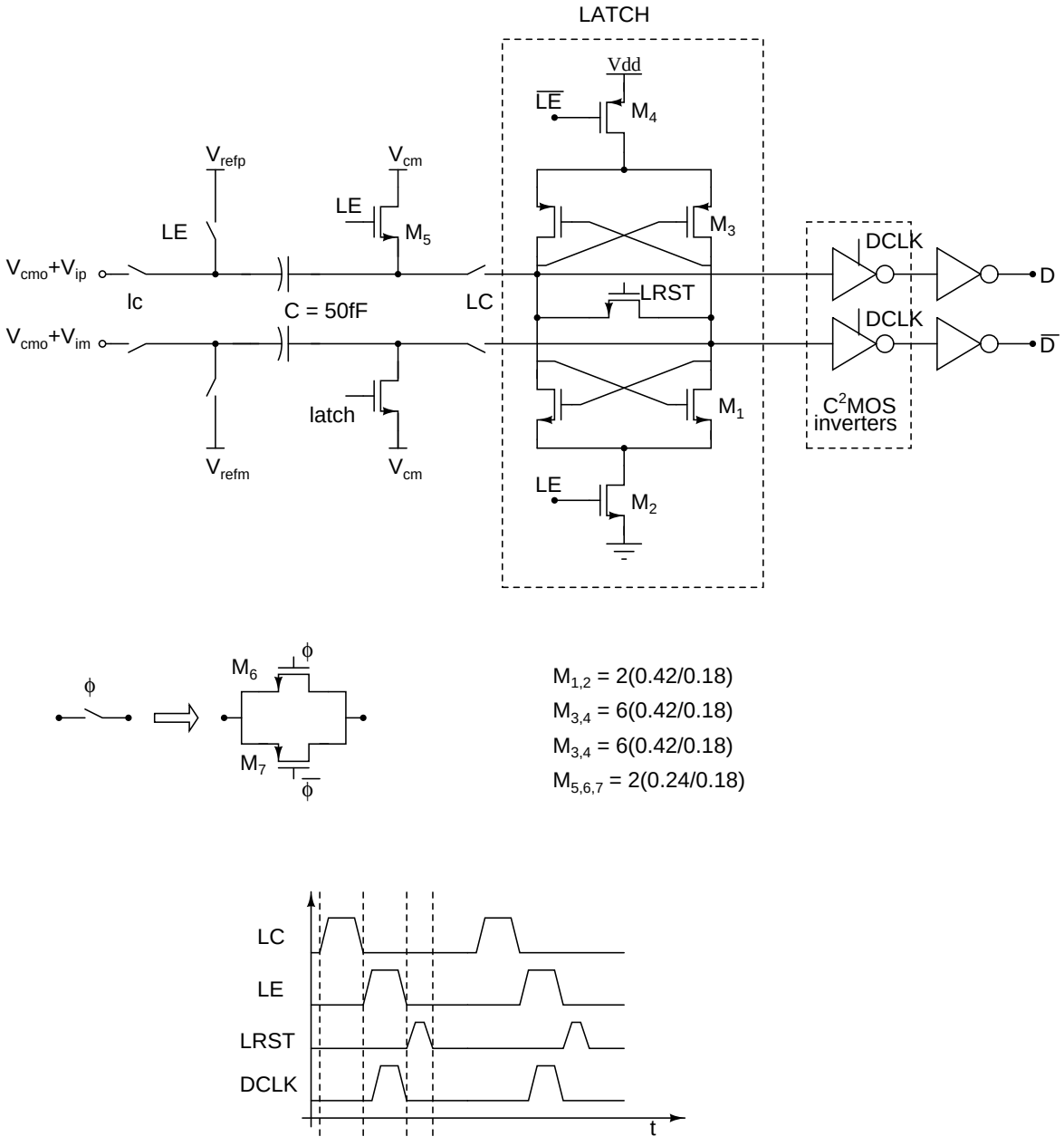


Figure 4.13: Schematic of the comparator

in three phases - ‘LE’ ,‘LC’ and ‘LRST’. These phases are shown in Figure 4.13 along with the schematic of the comparator.

Latch connect phase - LC

The latch is disabled during this phase by isolating it from the supplies, making the latch inputs to float. The coupling capacitor is charged to the reference in the previous LE phase. One end of the capacitor is connected to the input signal and the other end is connected to the the latch input. The voltage at the latch input would be the difference between the input signal and the reference.

Phase LE

In this phase, the latch is isolated from the coupling capacitor and is connected to the supplies. The latch would start to regenerate its input (the difference between the input signal for the flash and the reference at the beginning of the phase). Simultaneously, the references are stored on the coupling capacitor, ‘C’. The capacitor is disconnected from the latch, and the latch is allowed to regenerate the sampled data stored on its input during the previous ‘LC’ phase.

Phase LRST

Once the output is transfered to the next stage from the latch, the latch is reset, to avoid any memory transfer to the next clock cycle.

It could be observed that the comparator does not consume static power and there is only dynamic power consumption during the regeneration phase.

4.5.2 Reference Level Generator

The reference levels for each comparator are generated by a resistor ladder. The resistor ladder consists of 16 resistors each of 250 Ω and a capacitor of 2.5 pF. The capacitor is used to reduce the ripple at that node. The ends of the resistor ladder are connected to the two references, V_{refp} and V_{refm}. The references for the resistor ladder are generated (Figure 4.14) by passing differential current (I_{ref}) through resistors connected in negative feedback around an opamp. I_{const} supplies constant current to the resistor ladder, so the opamp only supplies a small amount of the ladder current. The current I_{ref} is generated by a voltage-to-current converter as shown in Figure 4.15.

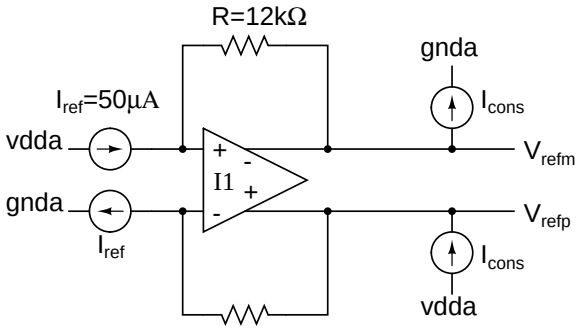
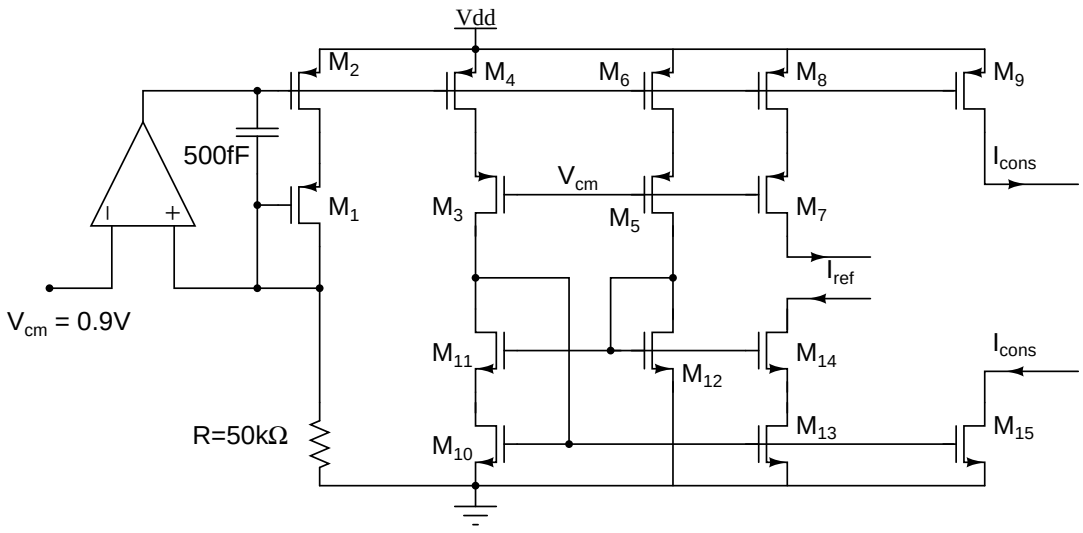


Figure 4.14: Reference generator for the resistor ladder

4.6 Dynamic Element Matching (DEM)

The algorithm implemented for dynamic element matching is Data Weighed Averaging (Baird and Fiez (1995)). The block diagram of the DEM is shown in Figure 4.16. The thermometer code from the flash ADC are barrel shifted by an index. The index is the accumulated value of the flash output. The DEM consists of a four stage barrel shifter. The n^{th} stage shifts the bits by 2^n levels. The modulo 16 accumulator is used to generate the 4-bit index. Since it is a modulo-16 accumulator, an additional zero level



$M_{1,2,3,4,5,6}$ = 10(0.3/0.2) M_9 = 30(3/0.2) M_{12} = 1(0.3/0.36) M_{15} = 30(3.2/0.36)
$M_{7,8}$ = 32(0.3/0.2) $M_{10,11}$ = 10(0.3/0.36) $M_{13,14}$ = 32(0.3/0.36)

Figure 4.15: Schematic of the I_{ref} generation circuit

bit was added to accommodate 16 bits of the shifter. This is compensated in the DAC by having an extra DAC cell with input as one. The shift is implemented using a 2:1 multiplexer. Each stage has 16 multiplexers, and the wiring is done according to the number of shifts. The multiplexer is shown in Figure 4.17.

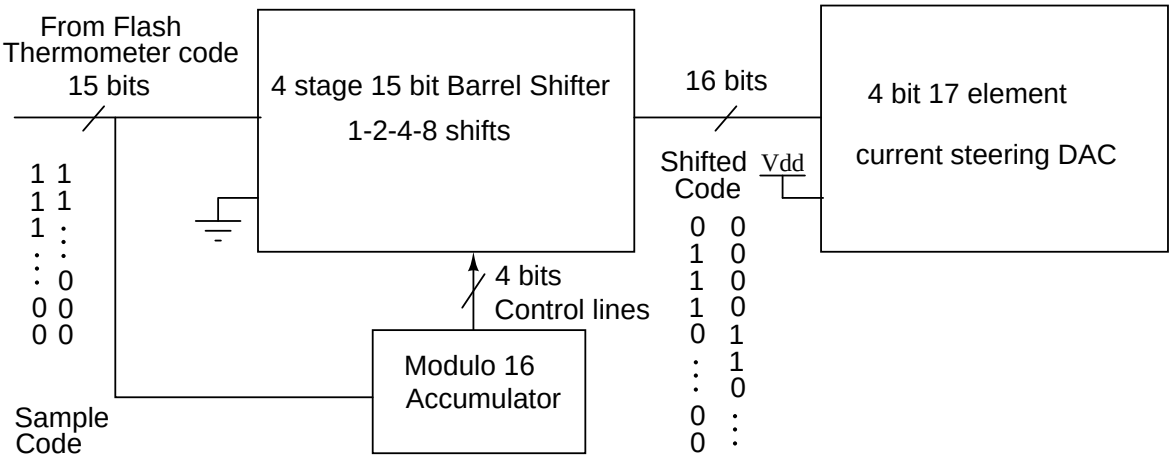


Figure 4.16: Block diagram of DEM

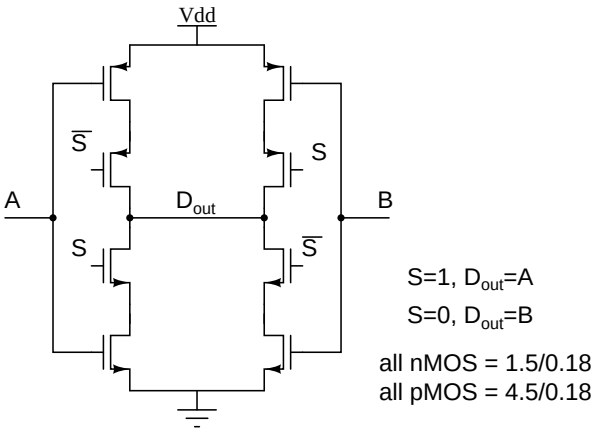


Figure 4.17: Implementation of the DEM

4.7 Digital-to-Analog Converter (DAC)

The Digital-to-Analog converter (DAC) is implemented as a current steering DAC. The current is steered by both nMOS and pMOS transistors. The schematic of the current steering cell is shown in Figure 4.18. The DAC current source contributes to the noise of the modulator. The overdrive of the current source is made large enough to reduce its contribution of thermal noise. The WL product is also adjusted so that the 1/f noise is reduced by maintaining the W/L ratio the same. The cascode transistors are made as small as possible to reduce any contribution of parasitic capacitance at the cascode drain node. The switches are all made minimum size. The bias generation circuit for the current sources and the cascode transistors are shown in Figure 4.19. The noise from the bias generation is removed by a RC filter at the output of the current source bias voltage.

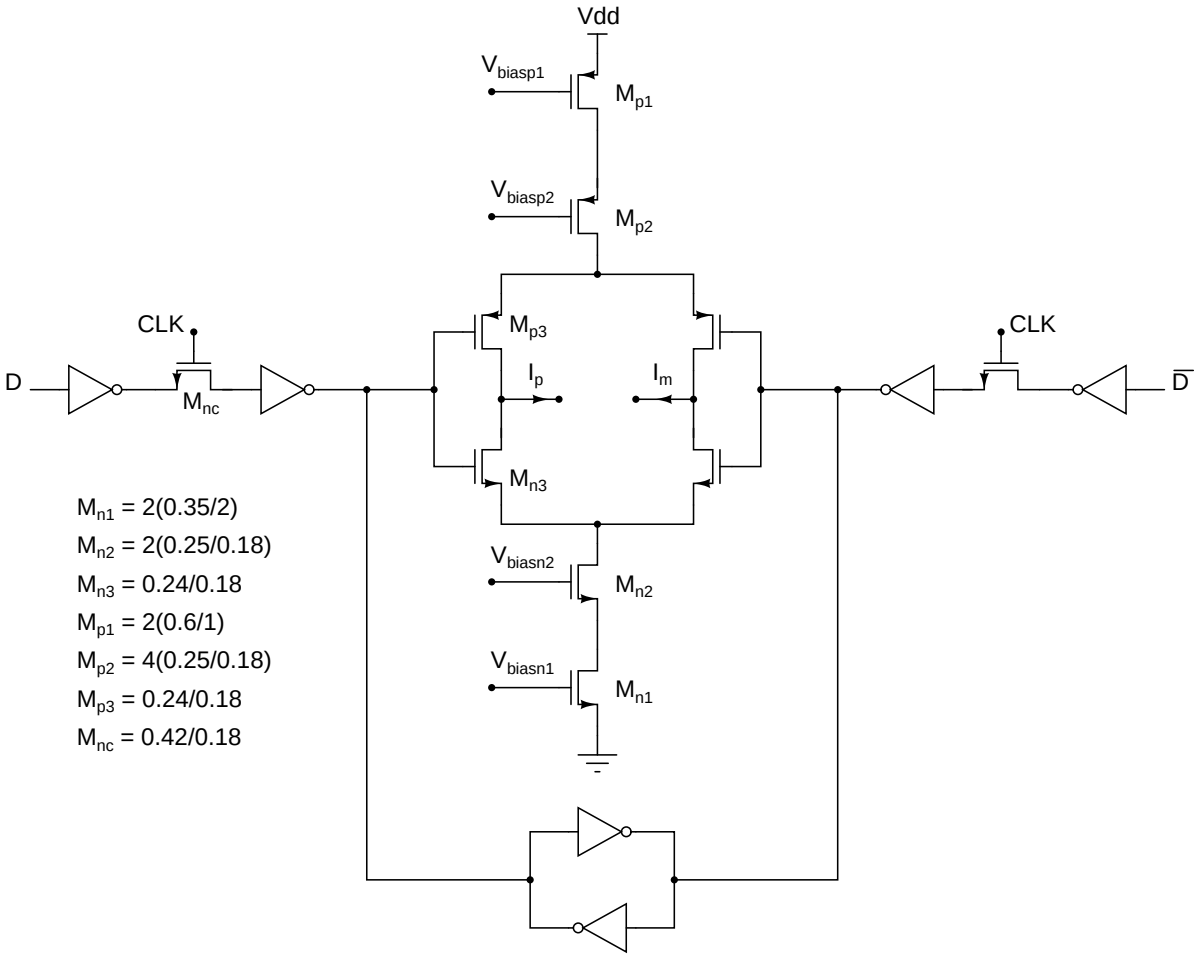


Figure 4.18: Schematic of current steering DAC cell

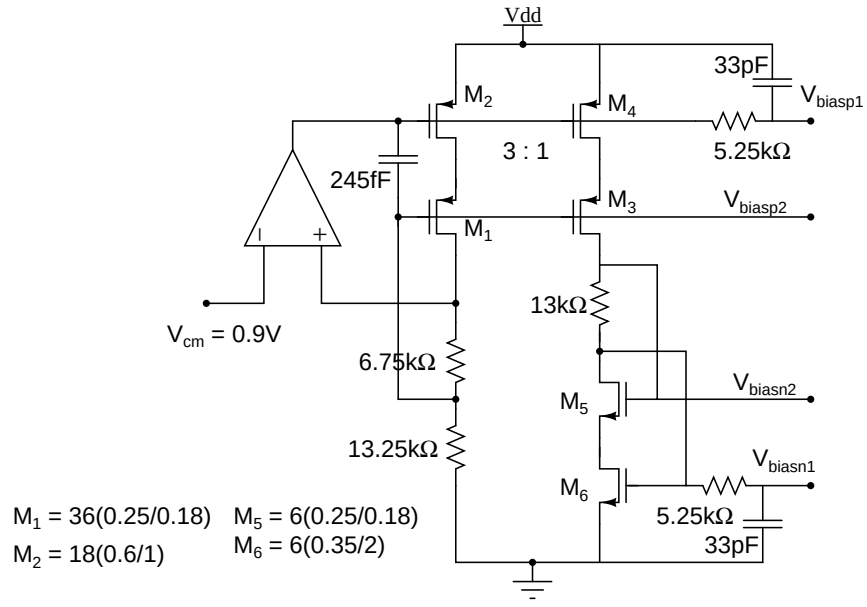
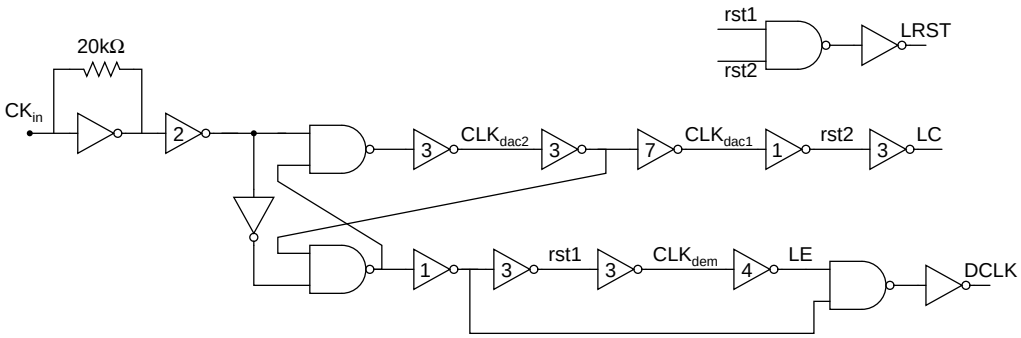


Figure 4.19: Schematic of current steering DAC bias generation circuit

4.8 Miscellaneous circuits

Clocks

The ADC,DWA and DAC require various clock pulses which have to be non-overlapping and have precise delays with respect to each other. The clock generation circuit is shown in Figure 4.20. The non-overlapping pulses are generated by the two back-to-back connected nand gates. The inverter chain is to realize the various desired clock phases.



All inverters are the same, pMOS = (1.5/0.18), nMOS = (0.5/0.18)

The numbers on the inverter indicate the number of chain of inverters

Figure 4.20: Non overlapping clocks

Output Stage

The output data is 4-bits at 300 MHz. For ease of board design and characterization, the data is converted into 8 bit stream at 150 MSPS. LVDS drivers are used to interface the test chip with the external world.

Floorplan of layout

The floorplan of the layout is shown in Figure 4.21. The snapshot of the layout of the chip is shown in Figure 4.22. The chip occupies an active area of approximately $1\,\mathrm{mm}^2$.

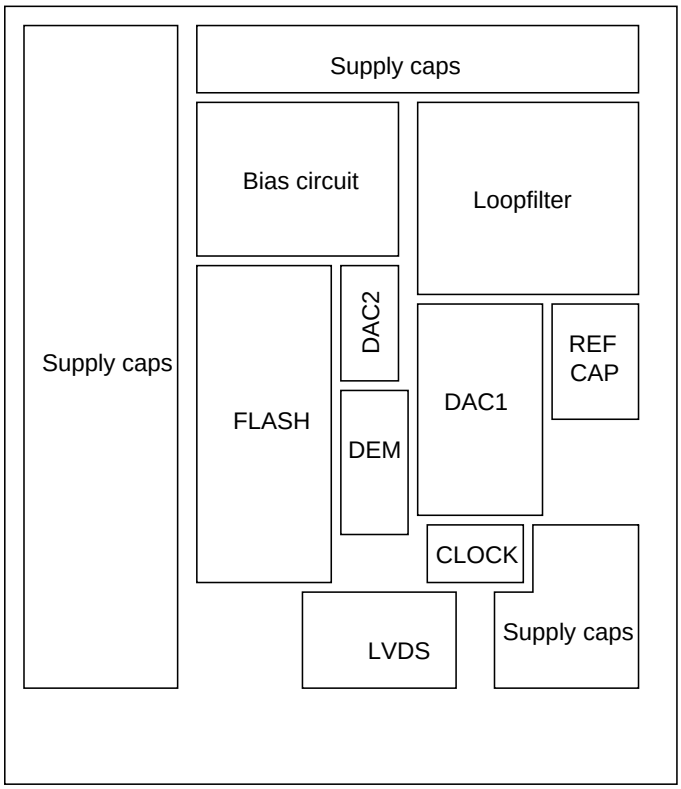


Figure 4.21: Floorplan of the layout of the $\Delta\Sigma$ Modulator

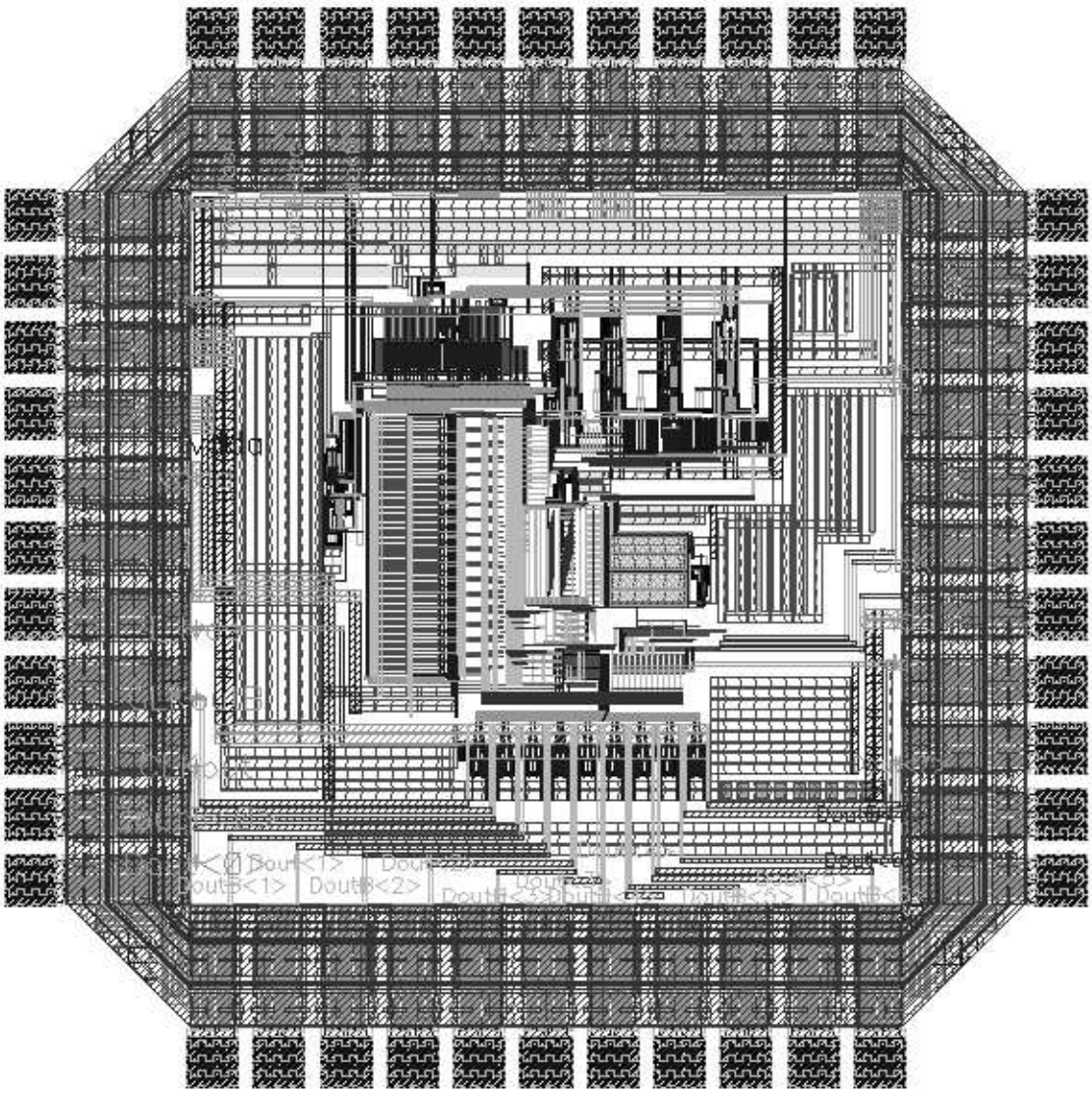


Figure 4.22: Snapshot of the layout of the $\Delta\Sigma$ Modulator

CHAPTER 5

Design Centering of the Loop Noise Transfer Function in the presence of circuit non-idealities

5.1 Introduction

Continuous time delta sigma modulators pose various design challenges in the course of their implementation. One such challenge involves the design of the modulator for the desired NTF in the presence of non-idealities of various blocks.

The modulator consists of a loopfilter which has integrators and summers as their prominent elements, an ADC and a DAC. All these blocks deviate from their desired ideal characteristics. Once these blocks replace their ideal counterparts in the modulator, the noise transfer function obtained would not be the desired one.

This chapter discusses a systematic design procedure for the continuous time modulator to mitigate the problem of such non-idealities present in the various blocks. The design procedure involves modelling the modulator using a state space description. The NTF of the modulator in the presence of the non-idealities is then determined using this state space description. An optimization routine is used to design centre the modulator.

The rest of the chapter is organized as follows. Section 5.2 revisits the modulator architecture designed in Chapter 4. The design centering process is applied to this modulator to realize the desired NTF. Section 5.3 discusses in detail the modelling of an opamp used in the integrators. Section 5.4 discusses deriving the state space description for the loopfilter. The optimization procedure for deriving the required NTF making use

of the state space representation of the loopfilter is discussed in section 5.5.

5.2 Modulator architecture

The architecture of the modulator is shown here again in Figure 5.1. Let us revisit some features of this modulator:

- The integrators are realized using opamp RC integrators. This integrator has a finite dc gain and also a finite bandwidth.
- The digital section consisting of the ADC, DEM and DAC has a propagation delay ΔT_s, which is around 2 ns.

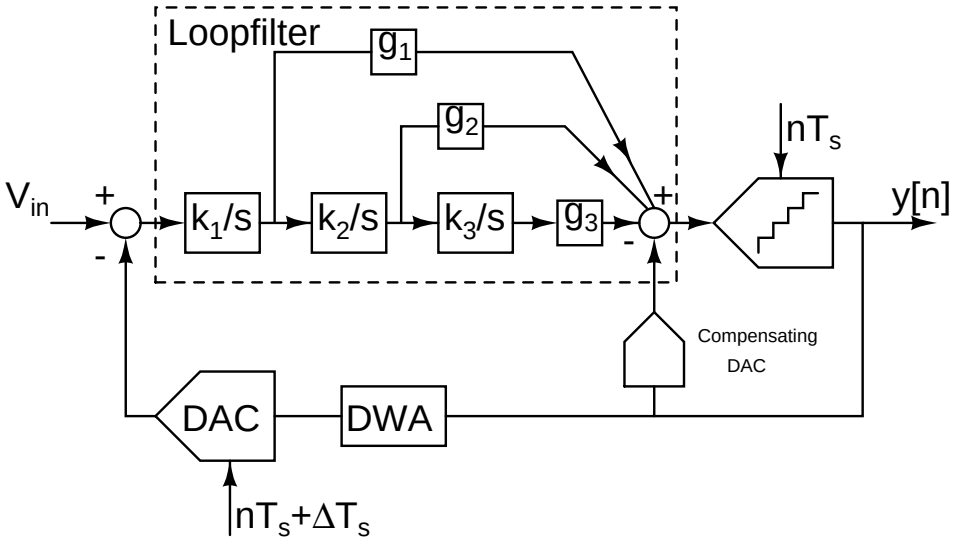


Figure 5.1: Block diagram of the modulator

In the presence of these non-idealities, the NTF response of the modulator deviates from the desired response. The design centering process involves varying the feedforward coefficients g_{1-3} and the compensating DAC coefficient to emend the NTF.

5.3 Modelling of the opamp

The small signal equivalent circuit of the opamp (see Figure 4.7) is shown in Figure 5.2. All MOS transistors are modelled using the complete quasi-static model (Tsividis (1999)). The parameters given in the equivalent circuit are explained below:

- G_{M1}, G_{M2} and G_{M3} are the transconductance of the transistors M_1, M_2 and M_5(of Figure 4.7) respectively.
- r_1 is $\frac{1}{G_{M2}}$,
  r_2 is $(G_{M2}\, r_{ds,M_2}\, r_{ds,M_1})||(G_{M3}\, r_{ds,M_3}\, r_{ds,M_4})$, and r_3 is $(r_{ds5}||r_{ds6})$
- $C_{in} = C_{gg1}$, $C_1 = (C_{dd1} + C_{jd1} + C_{ss2} + C_{js2})$, $C_2 = (C_{dd2} + C_{jd2} + C_{dd3} + C_{jd3} + C_{gg5})$ and $C_3 = (C_{dd5} + C_{jd5} + C_{dd6} + C_{jd6})$. The capacitors C_{in}, C_{1-3} apart from accounting for the device capacitors also includes the interconnect capacitors.
- The capacitors C_{4-9} are given as: $C_4 = C_{gd1}$, $C_5 = C_{dg1}$, $C_6 = C_{sd2}$, $C_7 = C_{ds2}$, $C_8 = C_{gd5}$ and $C_9 = C_{dg5}$.

The small signal parameters given above are obtained from the dc operating point of the circuit. In many occasions, the response (either the time or frequency domain) of the opamp model may not exactly match with the actual circuit response. The capacitors C_{1-9} can be varied slightly so that the model response matches with the circuit. The design centering process described in section 5.5 is followed to optimize the response.

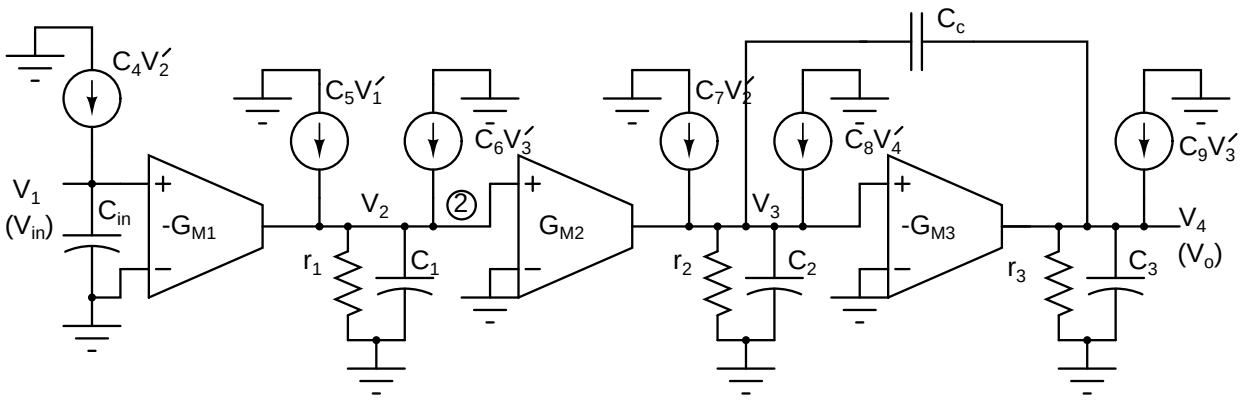


Figure 5.2: Model of the opamp.

5.4 State space model of the loopfilter

The state space representation is the model of a system which relates the input, output and the other nodes (known as the state variables) through first order differential equations, written in the form

$$\mathbf{H}\dot{\mathbf{x}}(t) = \mathbf{A_d}\mathbf{x}(t) + \mathbf{B_d}\mathbf{u}(t) \tag{5.1}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{5.2}$$

The schematic of the loopfilter with all the state variables is shown in Figure 5.3. The internal variables are as shown in Figure 5.2. The loopfilter has two inputs, one from

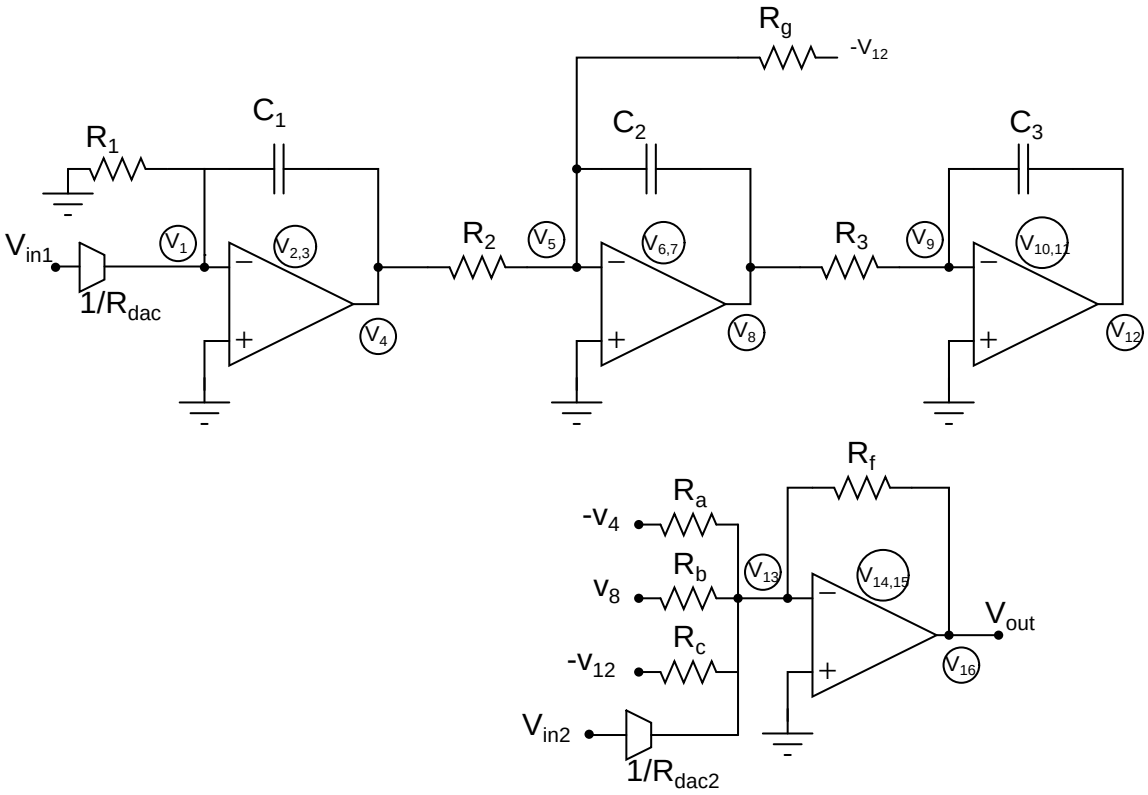


Figure 5.3: Schematic of the loopfilter with state variables.

the DAC and the other from compensating DAC. The descriptor state space matrix of

the loopfilter for the first DAC input can be written as

$$\begin{bmatrix} \mathbf{H_{11}} & \mathbf{H_{12}} & \mathbf{H_{13}} & \mathbf{H_{14}} \\ \mathbf{H_{21}} & \mathbf{H_{22}} & \mathbf{H_{23}} & \mathbf{H_{24}} \\ \mathbf{H_{31}} & \mathbf{H_{32}} & \mathbf{H_{33}} & \mathbf{H_{34}} \\ \mathbf{H_{41}} & \mathbf{H_{42}} & \mathbf{H_{43}} & \mathbf{H_{44}} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \\ \dot{\mathbf{x}}_3 \\ \dot{\mathbf{x}}_4 \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d_{11}}} & \mathbf{A_{d_{12}}} & \mathbf{A_{d_{13}}} & \mathbf{A_{d_{14}}} \\ \mathbf{A_{d_{21}}} & \mathbf{A_{d_{22}}} & \mathbf{A_{d_{23}}} & \mathbf{A_{d_{24}}} \\ \mathbf{A_{d_{31}}} & \mathbf{A_{d_{32}}} & \mathbf{A_{d_{33}}} & \mathbf{A_{d_{34}}} \\ \mathbf{A_{d_{41}}} & \mathbf{A_{d_{42}}} & \mathbf{A_{d_{43}}} & \mathbf{A_{d_{44}}} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d_1}} \\ \mathbf{B_{d_2}} \\ \mathbf{B_{d_3}} \\ \mathbf{B_{d_4}} \end{bmatrix} \mathbf{u}$$

$$\mathbf{y} = \begin{bmatrix} \mathbf{C_1} & \mathbf{C_2} & \mathbf{C_3} & \mathbf{C_4} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \end{bmatrix} \tag{5.3}$$

where,

$$\begin{aligned} \mathbf{x_1} &= \begin{bmatrix} v_1 & v_2 & v_3 & v_4 \end{bmatrix}^T \\ \mathbf{x_2} &= \begin{bmatrix} v_5 & v_6 & v_7 & v_8 \end{bmatrix}^T \\ \mathbf{x_3} &= \begin{bmatrix} v_9 & v_{10} & v_{11} & v_{12} \end{bmatrix}^T \\ \mathbf{x_4} &= \begin{bmatrix} v_{13} & v_{14} & v_{15} & v_{16} \end{bmatrix}^T \\ \mathbf{u} &= \begin{bmatrix} v_{in1} \end{bmatrix} \\ \mathbf{y} &= \begin{bmatrix} v_{16} \end{bmatrix} \end{aligned}$$

The dimensions of the sub matrices are given below:

$\dim[\mathbf{H_{ij}}(\cdot)] = 4 \times 4,\ \dim[\mathbf{A_{d_{ij}}}(\cdot)] = 4 \times 4,\ \dim[\mathbf{B_{d_i}}(\cdot)] = 4 \times 1,\ \dim[\mathbf{C_i}(\cdot)] = 1 \times 4.$

Each submatrix represents:

- $\mathbf{H_{ij}}$: For i=j, it shows the capacitive coupling within the nodes of an integrator/adder. For i≠j, it shows the capacitive coupling between nodes of different integrators/adder.
- $\mathbf{A_{d_{ij}}}$: For i=j, it shows the resistive coupling within the nodes of an integrator/adder. For i≠j, it shows the resistive coupling between nodes of different integrators/adder.
- $\mathbf{B_{d_i}}$: It shows the resistive coupling between the nodes of an ith integrator/adder and the input.
- $\mathbf{C_i}$: It shows the linear relation between the nodes of the ith integrator/adder and the output.

Certain observations which would help in simplifying the complexity of the model

- It is evident from the schematic that there is no capacitive coupling between any integrator(s)/adder. Hence $\mathbf{H_{ij}} = \mathbf{0}$ for i≠j
- The input is connected only to the node 1 of the first integrator. Hence $\mathbf{B_{d_1}} = \begin{pmatrix} \frac{1}{R_{dac}} & 0 & 0 & 0 \end{pmatrix}$ and $\mathbf{B_{d_i}} = \mathbf{0}$ for $i > 1$
- There is no resistive coupling between the integrator 1 and 3. Hence $\mathbf{A_{d_{13,31}}} = \mathbf{0}$
- The output is the state variable v_{16}. Hence we have $\mathbf{C_{1,2,3}} = \mathbf{0}$, and $\mathbf{C_4} = \begin{pmatrix} 0 & 0 & 0 & 1 \end{pmatrix}$
- There is no direct coupling from the input to the output which makes $\mathbf{D} = 0$.

Using the above observations, we get a much simplified descriptor state space model.

$$\begin{bmatrix} \mathbf{H_{11}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{H_{22}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{H_{33}} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{H_{44}} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_\mathbf{1} \\ \dot{\mathbf{x}}_\mathbf{2} \\ \dot{\mathbf{x}}_\mathbf{3} \\ \dot{\mathbf{x}}_\mathbf{4} \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d_{11}}} & \mathbf{A_{d_{12}}} & \mathbf{0} & \mathbf{A_{d_{14}}} \\ \mathbf{A_{d_{21}}} & \mathbf{A_{d_{22}}} & \mathbf{A_{d_{23}}} & \mathbf{A_{d_{24}}} \\ \mathbf{0} & \mathbf{A_{d_{32}}} & \mathbf{A_{d_{33}}} & \mathbf{A_{d_{34}}} \\ \mathbf{A_{d_{41}}} & \mathbf{A_{d_{42}}} & \mathbf{A_{d_{43}}} & \mathbf{A_{d_{44}}} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d_1}} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \mathbf{u}$$

The first row of the 5.4 is the state space related to the first opamp nodes (V_{1-4}). The state space equation corresponding to it is

$$\mathbf{H_{11}}\dot{\mathbf{x}}_\mathbf{1} = \mathbf{A_{d_{11}}}\mathbf{x_1} + \mathbf{A_{d_{12}}}\mathbf{x_2} + \mathbf{A_{d_{14}}}\mathbf{x_4} + \mathbf{B_{d_1}}\mathbf{u} \tag{5.4}$$

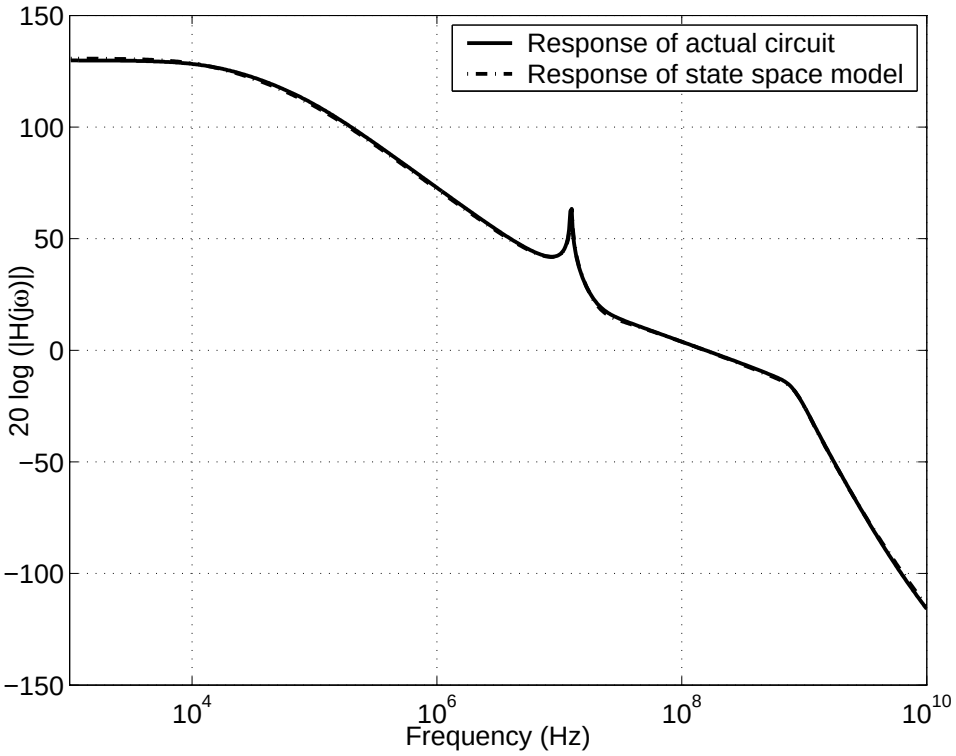


Figure 5.4: Response of the loopfilter for V_{in1}.

From figures 5.2 and 5.3, the matrices in equation 5.4 can be written

$$\mathbf{H_{11}} = \begin{bmatrix} -(C_{in} + C_{int1}) & C_4 & 0 & -C_{int1} \\ C_5 & -C_1 & C_6 & 0 \\ 0 & C_7 & -(C_2 + C_c) & C_c + C_8 \\ -C_{int1} & 0 & C_c + C_9 & -(C_2 + C_c + C_{int1}) \end{bmatrix}$$

$$\mathbf{A_{d_{11}}} = \begin{bmatrix} \frac{1}{R_1} & 0 & 0 & 0 \\ G_{M1} & \frac{1}{r_1} & 0 & 0 \\ 0 & -G_{M2} & \frac{1}{r_2} & 0 \\ 0 & 0 & G_{M3} & (\frac{1}{r_2} + \frac{1}{R_2} + \frac{1}{R_a} \end{bmatrix}$$

$$\mathbf{A_{d_{12}}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\frac{1}{R_2} & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{A_{d_{14}}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{R_a} & 0 & 0 & 0 \end{bmatrix}$$

Similarly, the matrices for the other opamp nodes could be derived. Once the matrices are derived, the transfer function of the loopfilter could be derived using the MATLAB function *ss2tf*. Let us denote the transfer function as $H_1(s)$ and is plotted in Figure 5.4. In a similar manner the descriptor state space is derived for the transfer function from the compensation DAC to the output. A few approximations are done here. The outputs of the integrators are considered to be grounded. Hence, the schematic has only the adder block which is shown in figure 5.5. The transfer function for this path is denoted by $H_2(s)$.

5.5 Optimization of the NTF

The linearized model of the designed modulator is shown in Figure 5.6. The loopfilter has two paths as is shown. The first path has a delay τ_{d1} and is followed by $H_1(s)$. The other path has a delay of τ_{d2} and is followed by $H_2(s)$. The discrete time equivalent transfer functions $H_1(z)$ and $H_2(z)$ for each path is obtained by the pulse invariance

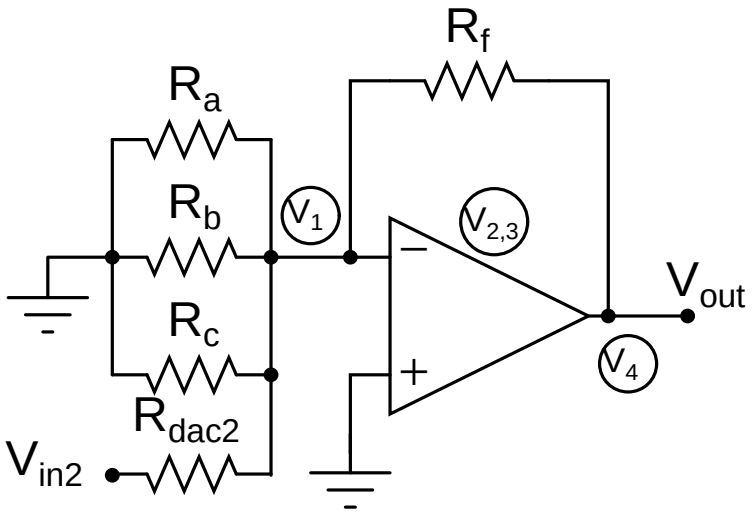


Figure 5.5: Schematic of the adder block with input V_{in2}.

technique (Schreier and Temes (2005)), from which the NTF is obtained as

$$NTF(z) = \frac{1}{H_1(z) + H_2(z)} \tag{5.5}$$

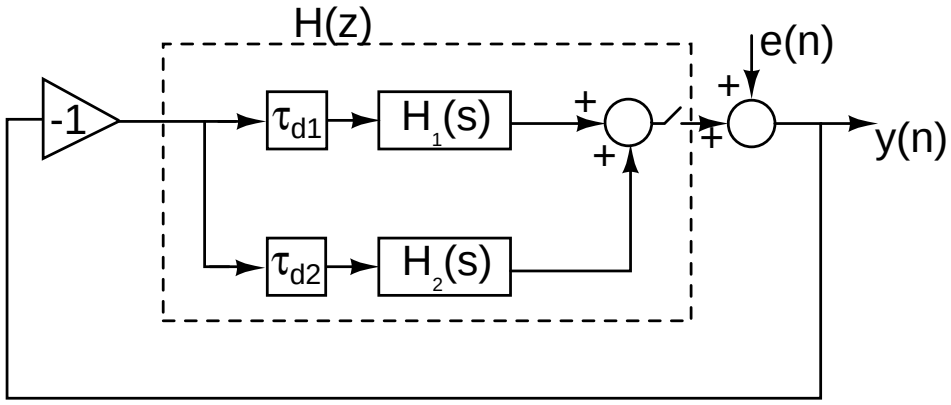


Figure 5.6: Linear model of the architecture discussed.

As discussed earlier, the above NTF would be very different from the desired NTF. The plot of the NTF of the modulator along with the ideal NTF is shown in Figure 5.7. The following steps are followed in the optimization process:

1. The parameters which are to be varied are grouped as a optimization vector. In this case, it is the feedforward resistors and the compensation DAC resistor, R_a, R_b, R_c and R_{dac2} which form the optimization vector.

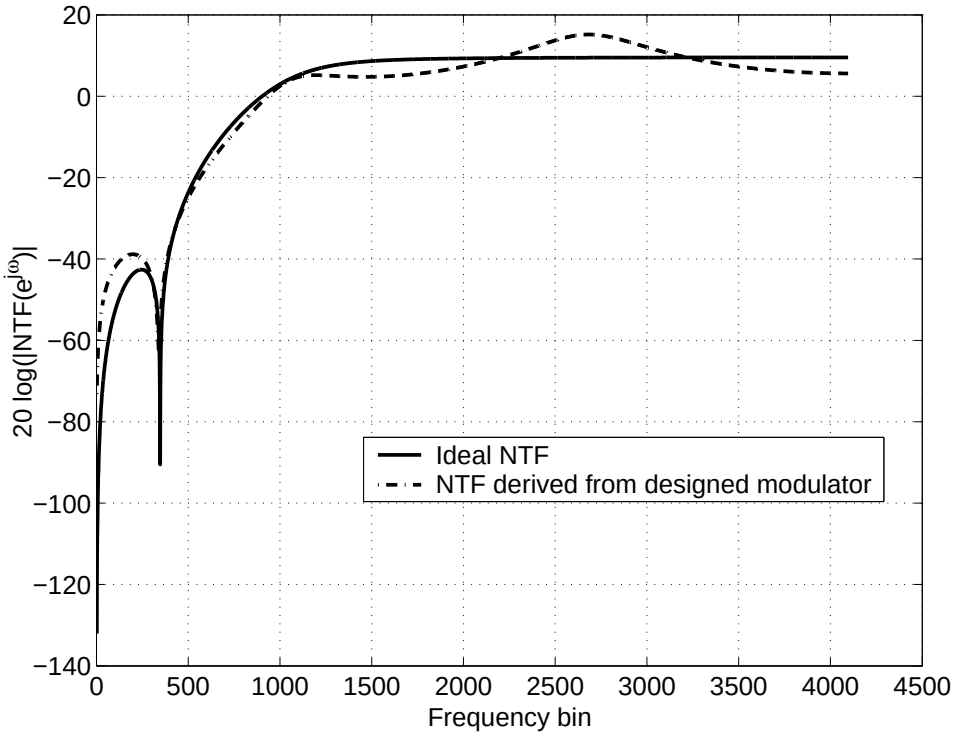


Figure 5.7: NTF plot of the modulator before optimization along with the ideal noise transfer function.

2. The mean square error e_{NTF} between the actual and the ideal NTF response is computed as a function of the optimization vector.

$$e_{NTF}(\cdot) = \frac{1}{\pi} \int_0^{\pi} |NTF_{actual}(e^{j\omega}) - NTF_{ideal}(e^{j\omega})|^2 \, d\omega \tag{5.6}$$

3. The MATLAB function, *fminsearch* minimizes the error by varying the optimization vector.

Figure 5.8 shows the NTF plot after optimization along with the ideal NTF. It could be observed that there is a very good proximity of the optimized NTF with the desired one.

5.6 Summary of the design centering technique

The presence of non-idealities in the loopfilter and the excess loop delay, the actual NTF deviates from the desired one. To obtain the desired NTF, the feedforward

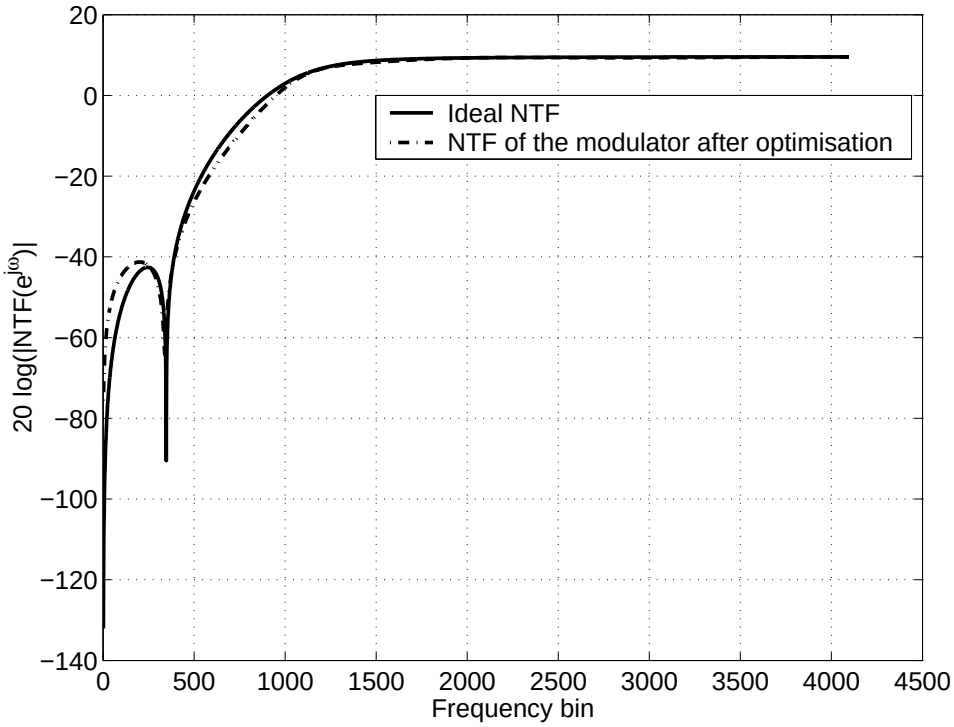


Figure 5.8: NTF plot of the modulator after optimization along with the ideal noise transfer function.

coefficients and the compensation DAC coefficient has to be varied. The systematic process of varying these parameters by minimizing the magnitude error between the actual NTF and the desired NTF is achieved through the MATLAB function *'fminsearch'*. The loopfilter is represented by state space notation to obtain its transfer function and thus the NTF.

CHAPTER 6

Measurement Results

6.1 Die photograph

The die photograph of the chip is shown in Figure 6.1.

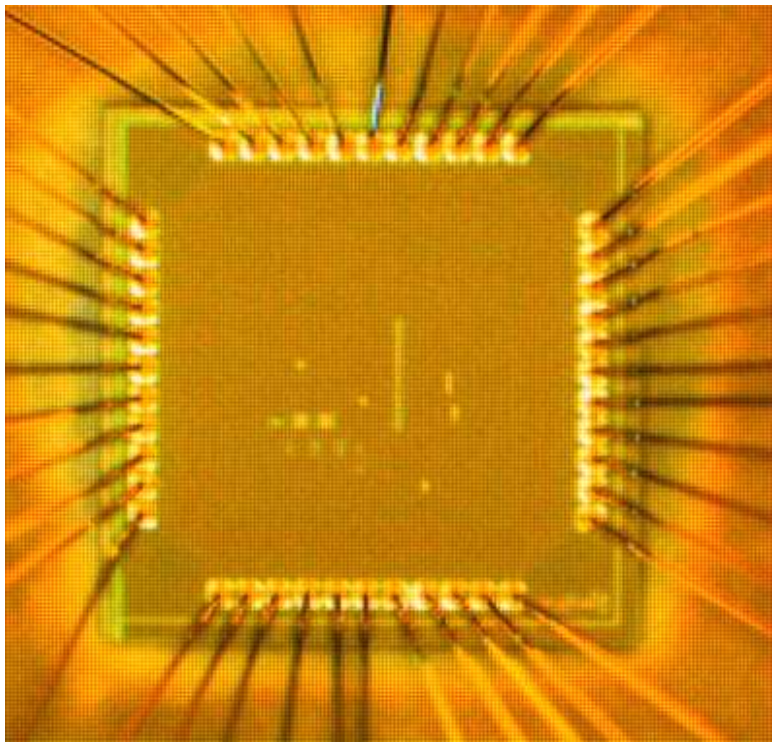


Figure 6.1: The die photograph of the chip

The chip is packaged using a 44 pin JLCC package, and the bonding diagram of the die is shown in Figure 6.2.

6.2 Design of the Printed Circuit Board

The printed circuit board to test the chip was designed in OrCAD. It is a two layer board with the dimensions of 3.4”× 3.7” and the material is FR4 glass epoxy. The

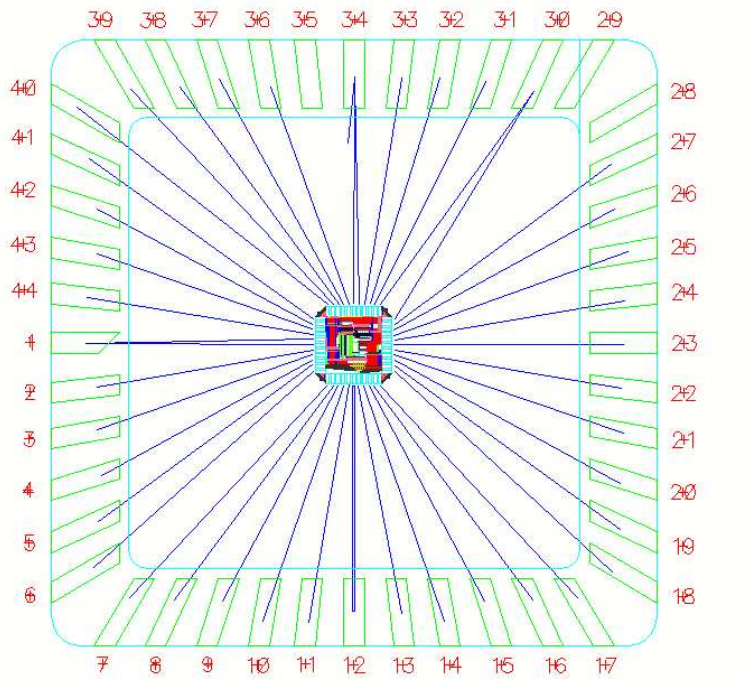


Figure 6.2: The bonding diagram of the die

thickness of the board is 1.6 mm. The snapshot of the board with all the components populated on it shown in Figure 6.6. The snapshot of the test setup is shown in Figure 6.4.

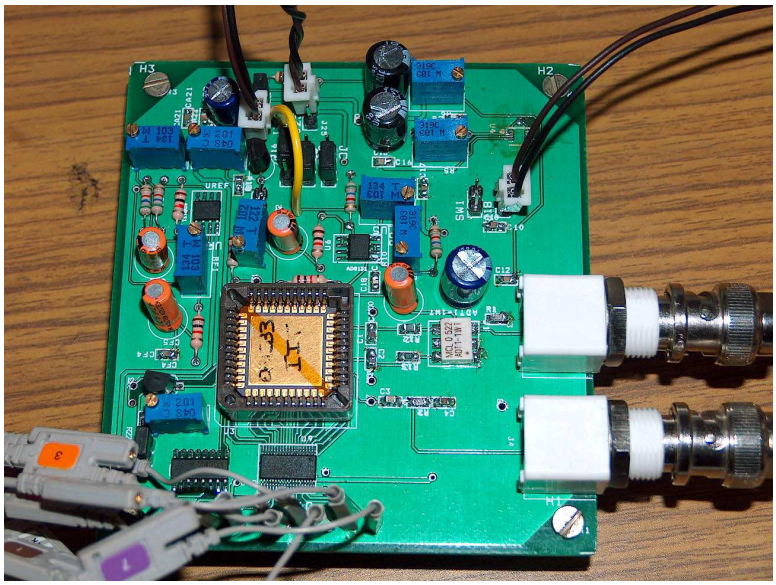


Figure 6.3: Test board, the JLCC package is the chip.

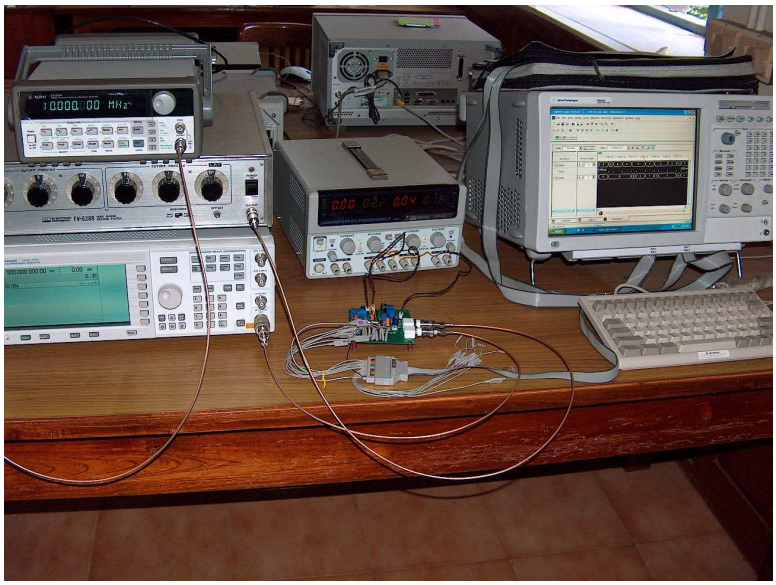


Figure 6.4: Measurement setup, shows the clock and signal generator on the left, the power supply in the centre, the logic analyzer on the right and the test board in the foreground

6.3 Pinout details of the chip

The pins of the chip are classified as follows:

- Power supplies: VDDA, VDDD, VDDC and GNDA
- Input signals: Vinp,Vinm and input clock: CLKin
- LVDS data out and clockout signals: D0-7 and CLKout; LVDS bias current: Ilvds
- Input common mode reference and references to the flash ADC and the DACs: Vcm, Vrefflash, Vrefdac and Vrefdacff
- Bandwidth settings a<0:2>
- Fixed transconductance bias pins: Rp, Rn
- First integrator current input:I_1

6.3.1 Generation of the pin signals on the board

The pin signals can be broadly classified as input, output, control and reference pins.

The generation of the pin signals on the board is shown in Figure 6.6 The three pins

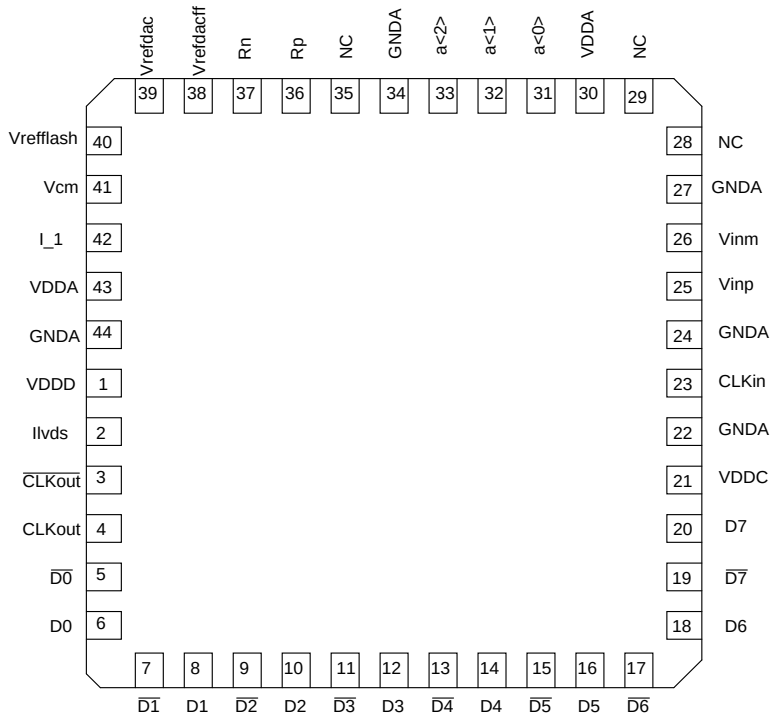


Figure 6.5: Pin details of the test chip

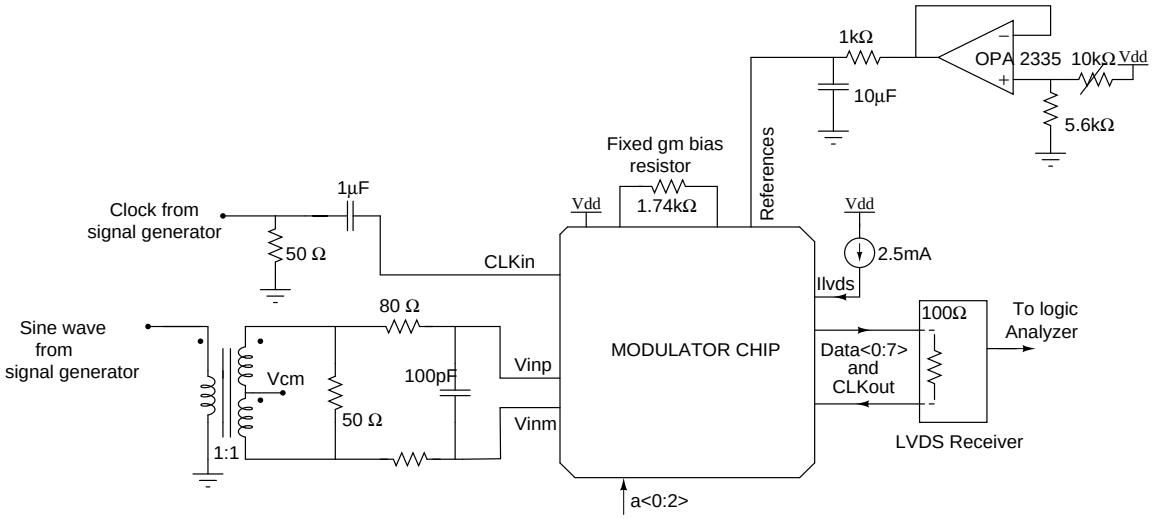


Figure 6.6: Schematic of the board

VDDA, VDDD and VDDC were shorted on the board and were powered by external 1.8 V supply. The input signal is converted from the single ended to differential ended using the centre tapped transformer ADT1-1WT. The centre tap is connected to the input common mode Vcm. The secondary tap is terminated by a $50\,\Omega$ resistor followed by a 20 MHz low pass RC filter of $80\,\Omega$ and 100 pF. The clock input is terminated by a $50\,\Omega$ and is ac coupled to the input through $1\,\mu F$. The references required by the modulator are Vcm, Vrefflash, Vrefdac and Vrefdacff. Vcm is the common mode voltage. Vrefflash is the reference to fix the range of the flash ADC inside the modulator. Vrefdac and Vrefdacff are the reference for the current source generation circuit of the two DACs. The nominal voltages for the references are 0.9, 0.75, 0.9 and 0.9 V for Vcm, Vrefflash, Vrefdac, Vrefdacff respectively. The references are generated by resistor voltage divider circuit from the supply. A trimmable resistor would help us to vary the references from 0.65 to 1.8 V. This is then buffered by OPA2335 by using it in a non-inverting unity feedback configuration. The output of the opamp is low pass filtered and fed to the chip. The data out of the modulator is in the LVDS format. An eight channel LVDS receiver LVDT386A and a four channel receiver LVDT388A are used to receive the 8 bit data and clock respectively. The remaining three channels of the LVDT388A are kept idle. The receiver converts the data to CMOS format which is captured by the logic analyzer. The LVDS transmitter in the chip requires a current of 2.5 mA which is supplied by the external current source LM334. A $1.74\,k\Omega$ is connected between the fixed transconductance bias pins Rp and Rn. The chips OPA2335, LVDT386A and LVDT388A are powered by a 3.3 V supply. The schematic of the board is split into two portions. The schematic of the board with the ADC and the input and output interfaces is shown in Figure 6.7. The schematic of the board with the reference part is shown in

Figure 6.8.

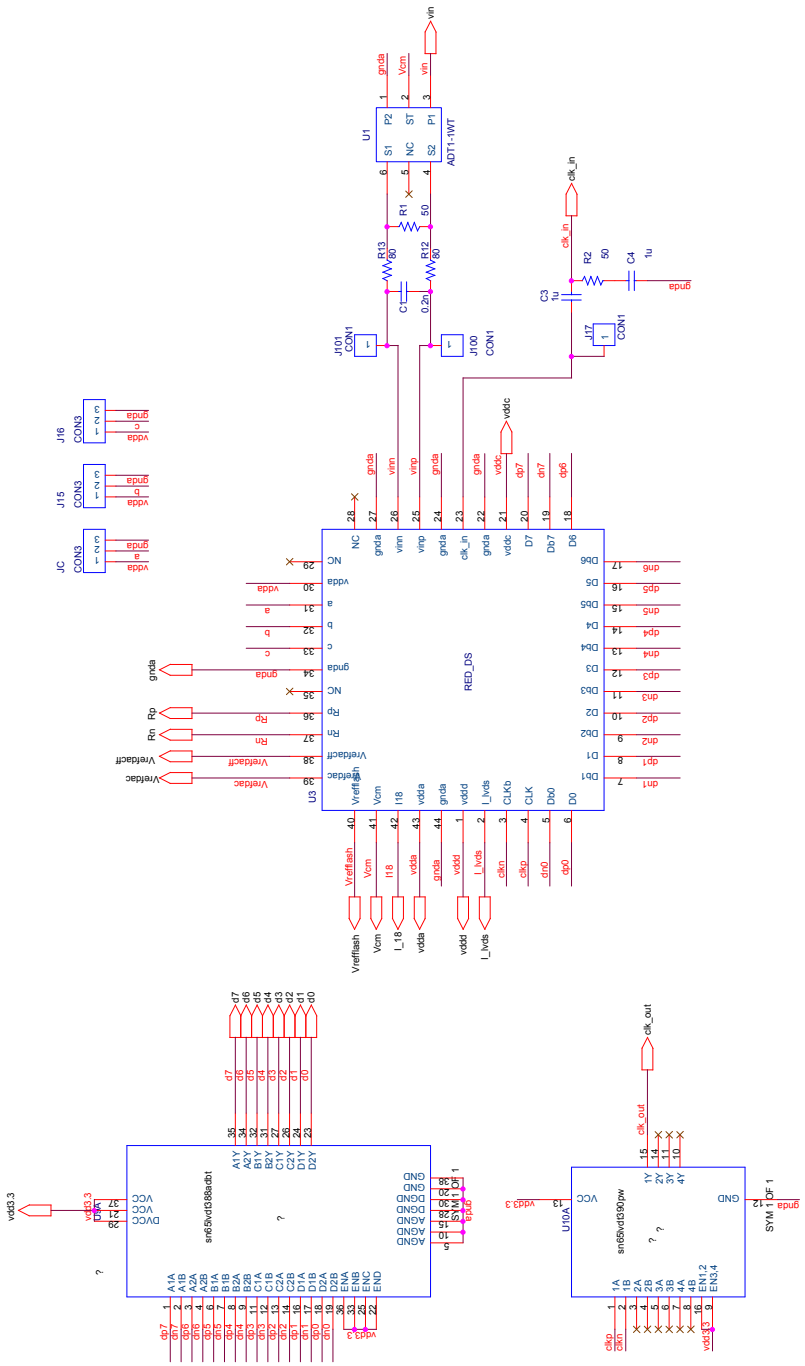


Figure 6.7: Schematic of the board

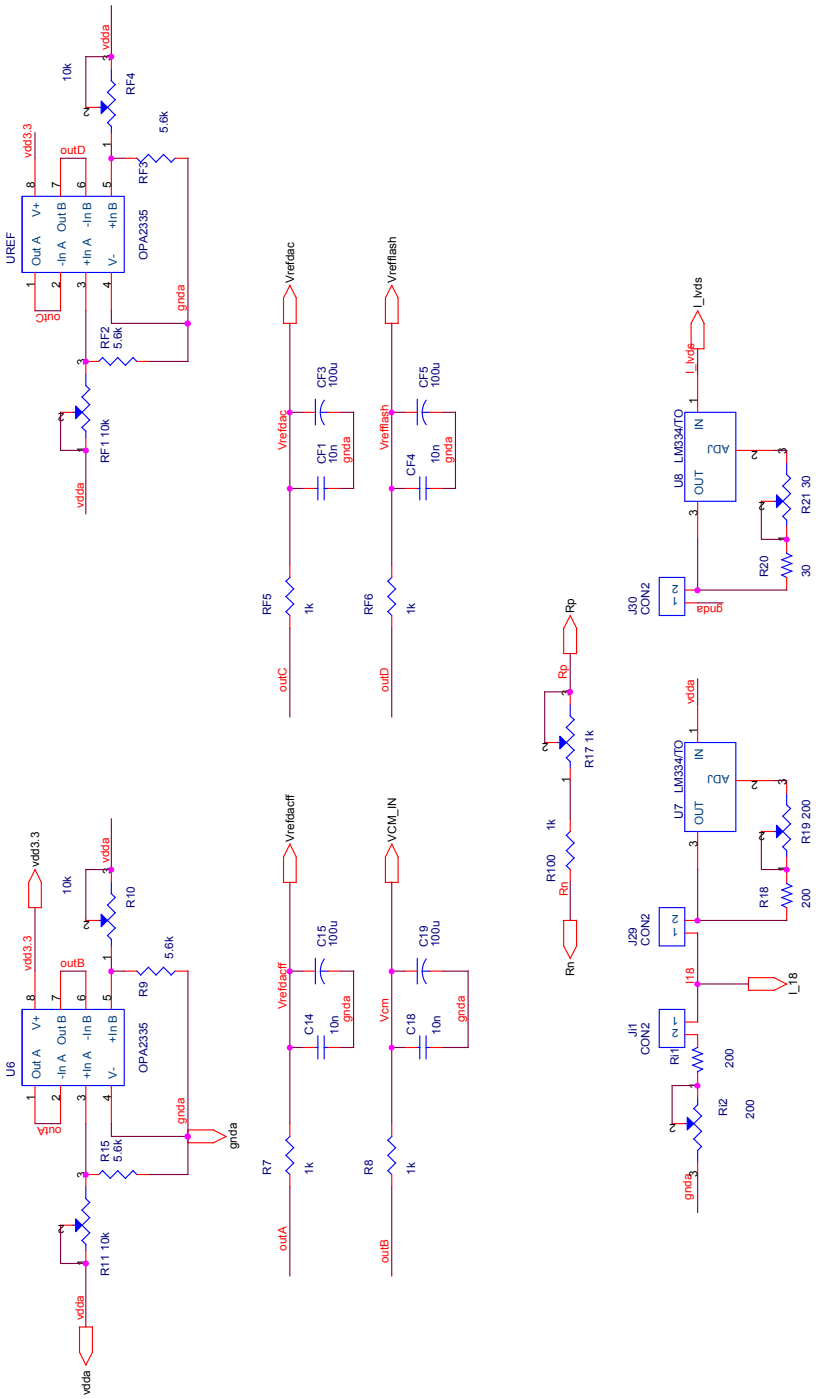


Figure 6.8: Schematic of the board

6.4 Measurement Results

The prototype chip is tested with four frequencies within the signal bandwidth, at 3 MHz, 4.7 MHz, 10 MHz and 14 MHz. The power spectral density plot of the output for -4 dBFS input at 4.7 MHz is shown in Figure in 6.9.

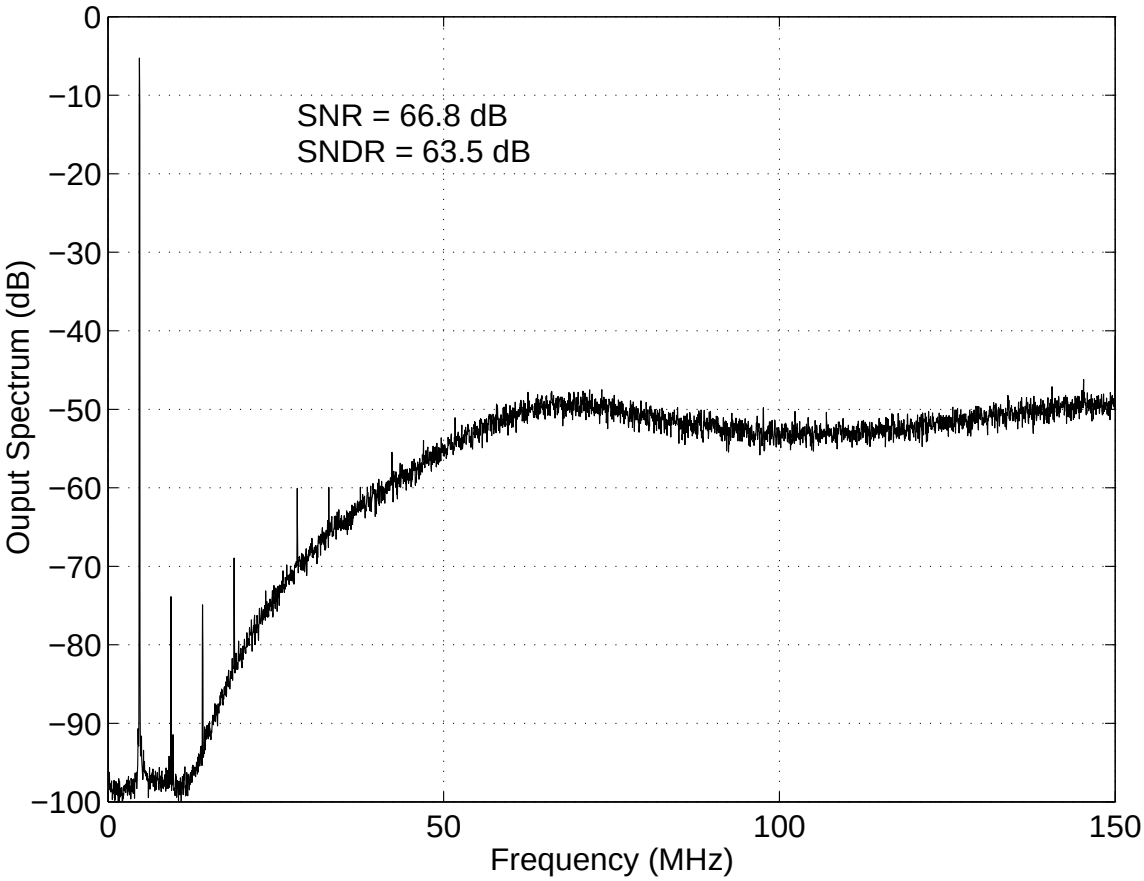


Figure 6.9: Output spectrum for input=-4dBFS at 4.7MHz

The SNR and SNDR plotted against the amplitude for the four different input frequency is shown in Figures 6.10, 6.11, 6.12 and 6.13. The measurement results for the various input frequencies are tabulated in Table 6.1. The peak SNR obtained was 67 dB and the peak SNDR is 63.5 dB. The dynamic range of the modulator is 70.5 dB. The summary of the measurement results is tabulated in Table 6.2.

Input frequency (MHz)	SNR (dB)	SNDR (dB)	Dynamic Range (dB)
3	66.4	63.5	70.5
4.7	66.8	63.3	69.7
10	66	66	68
14	66.2	62	70

Table 6.1: Measured results for different input frequencies

Feature	Details
Technology	$0.18\mu\,m$ CMOS @ 1.8 V
Peak SNR	66.8 dB
Peak SNDR	63.5 dB
Dynamic Range	70.5 dB
Power consumption	20 mW
Active die area	$1\,mm^2$

Table 6.2: Summary of the chip results

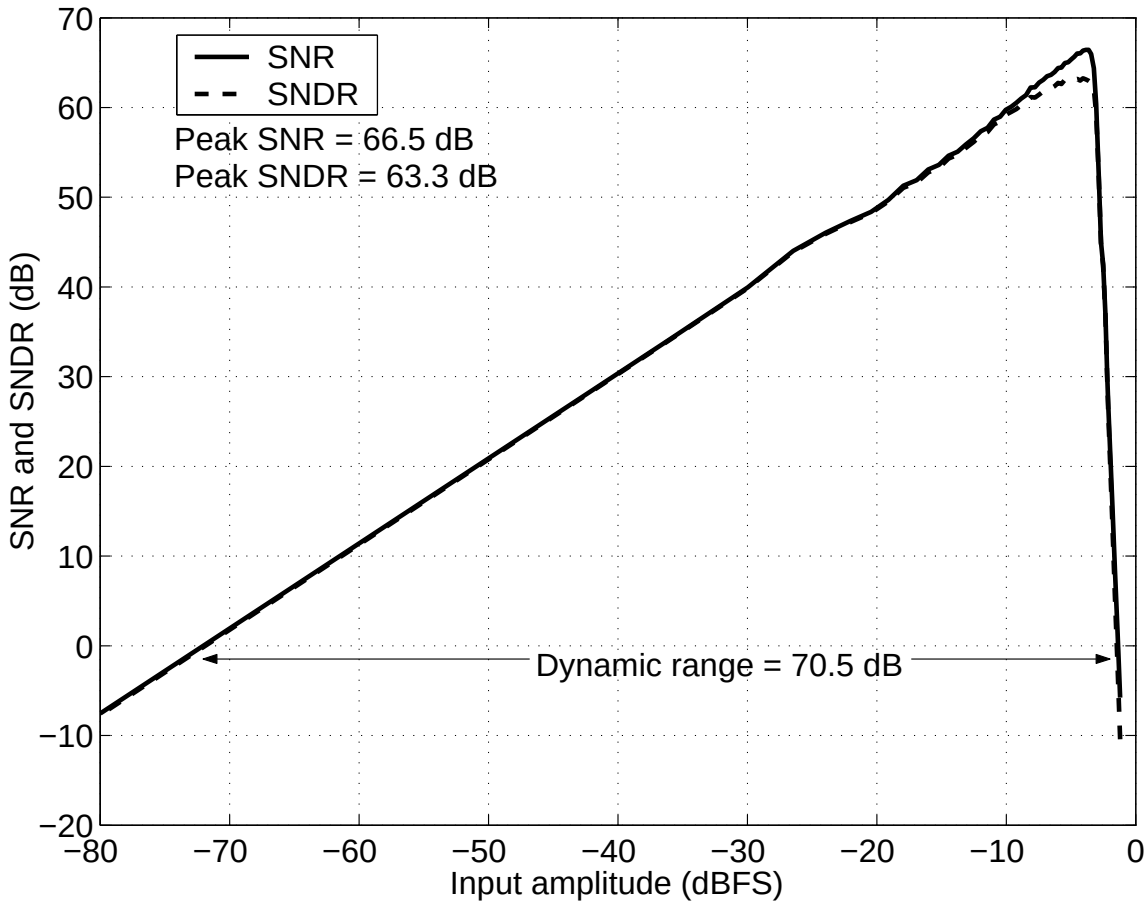


Figure 6.10: SNR and SNDR plots versus input amplitude at 3 MHz tone

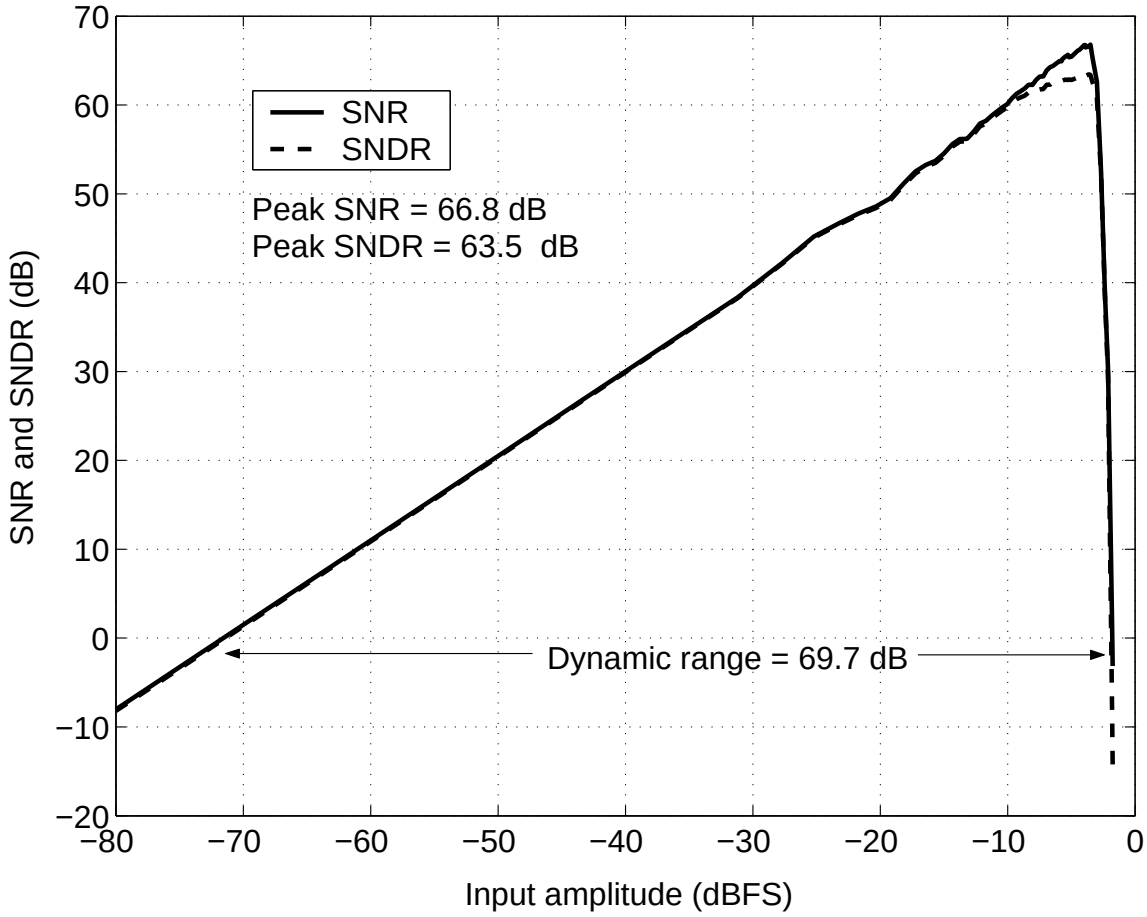


Figure 6.11: SNR and SNDR plots versus input amplitude at 4.7 MHz tone

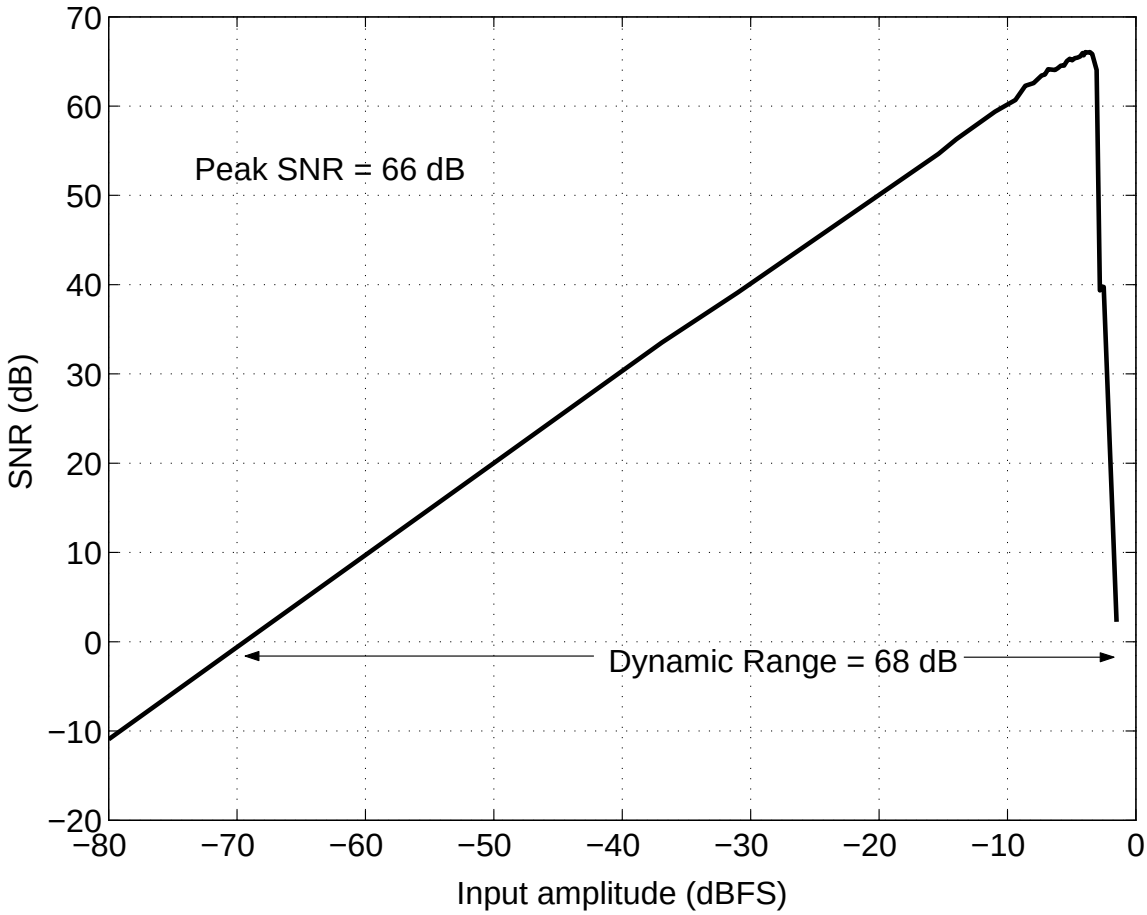


Figure 6.12: SNR plot versus input amplitude at 10 MHz tone

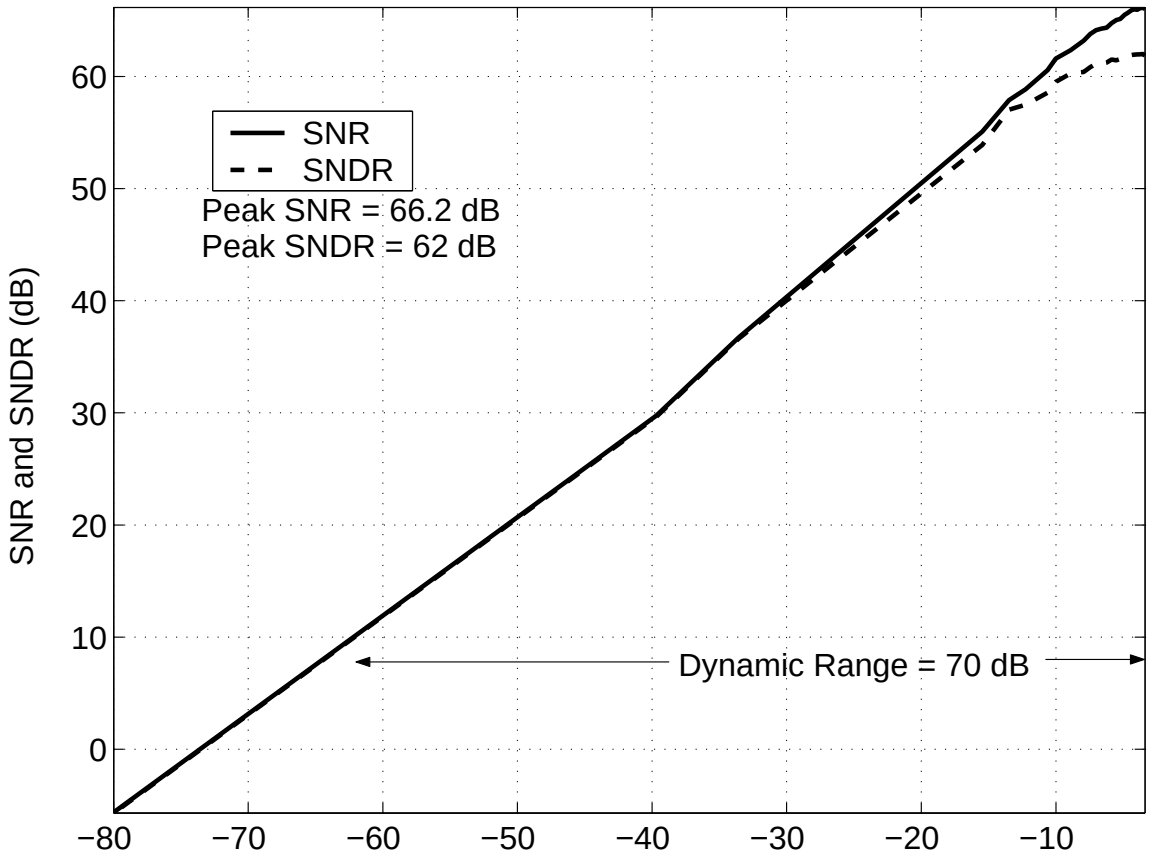


Figure 6.13: SNR and SNDR plots versus input amplitude at 14 MHz tone

CHAPTER 7

Conclusions

The effect of clock jitter in continuous time delta sigma modulators has been studied. A lower bound on the jitter noise in a single-loop CTDSM with white clock jitter has been derived using the Bode sensitivity integral for discrete time systems. An NTF with moderate peaking was shown to have a lower jitter noise than a maximally flat NTF for the same in-band quantization noise, thereby giving intuition to the result in (Hernandez *et al.* (2004)), arrived at using numerical methods. A maximally flat NTF, though not optimal for jitter performance, was shown to be very close to the optimal NTF, provided the right OBG was chosen. As an extension of the work, a third order continuous time modulator has been implemented. The chip was implemented in a 0.18 μm CMOS process. The clock frequency is 300 MHz and the signal bandwidth is 15MHz. The measurement results of the prototype chip shows a peak SNR of 66.8 dB and a dynamic range of 70.5 dB. The power consumption of the chip was 2 0mW at 1.8 V supply.

APPENDIX A

Extension of Arithmetic mean-Geometric mean inequality

Consider a real function $f(x)$ in the interval [a,b]. Since the arithmetic mean is greater than the geometric mean, we have

$$\frac{(b-a)}{L}\sum_{k=0}^{k=L-1}|f(a+k\frac{(b-a)}{L})|^2 \geq (b-a)\left[\prod_{k=0}^{k=L-1}|f(a+k\frac{(b-a)}{L})|^2\right]^{1/L} \quad \text{(A.1)}$$

The RHS of the above equation can be written as follows.

$$(b-a)\left[\prod_{k=0}^{k=L-1}|f(a+k\frac{(b-a)}{L})|^2\right]^{\frac{1}{L}} = (b-a)\exp\left(\frac{1}{L}\sum_{k=0}^{k=L-1}\log(|f(a+k\frac{(b-a)}{L})|^2)\right) \quad \text{(A.2)}$$

Using (A.2) in (A.1), we obtain

$$\frac{(b-a)}{L}\sum_{k=0}^{k=L-1}|f(a+k\frac{(b-a)}{L})|^2 \geq (b-a)\exp\left(\frac{2}{L}\sum_{k=0}^{k=L-1}\log(|f(a+k\frac{(b-a)}{L})|)\right) \quad \text{(A.3)}$$

In the limit when $L \to \infty$, the summation tends to an integral, and we get

$$\int_a^b |f(x)|^2\,dx \geq (b-a)\exp\left(\frac{2}{(b-a)}\int_a^b \log(|f(x)|)\,dx\right) \quad \text{(A.4)}$$

Note that the equality is valid only when $|f(x)|$ is a constant. Equivalently, we see that the lower bound on $\int_a^b |f(x)|^2\,dx$ is $(b-a)\exp\left(\frac{2}{(b-a)}\int_a^b \log(|f(x)|)\,dx\right)$.

APPENDIX B

Analytic expression for jitter noise of maximally flat NTF

The maximally flat NTF (a discrete time Butterworth high pass filter) is given by

$$|NTF(e^{j\omega})|^2 = OBG^2 \frac{\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}}{1+\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}} \tag{B.1}$$

where, ω_c is the 3 dB cut-off frequency. The condition that first sample of the NTF impulse response $h_{NTF}(0) = 1$, relates OBG and ω_c. Representing the NTF in 'z-domain', we have

$$NTF(z) = OBG \left(\frac{\left[\frac{(\frac{1-z^{-1}}{1+z^1})}{\tan(\omega_c/2)}\right]^N}{B_N\left[\frac{(\frac{1-z^{-1}}{1+z^1})}{\tan(\omega_c/2)}\right]} \right) \tag{B.2}$$

where $B_N(x)$ is the butterworth polynomial. For $h_{NTF}(0) = 1$, the coefficient of z^0 in the numerator and denominator have to be same, which are OBG and $B_N \tan(\frac{\omega_c}{2})$ respectively. Hence we have,

$$OBG = B_N\left(\tan\left(\frac{\omega_c}{2}\right)\right) \tag{B.3}$$

Therefore,

$$|NTF(e^{j\omega})|^2 = B_N\left(\tan\left(\frac{\omega_c}{2}\right)\right)^2 \frac{\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}}{1+\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}} \tag{B.4}$$

Now, we have

$$A_J = 4\ B_N^2 \left(\tan\left(\frac{\omega_c}{2}\right)\right) \int_0^{\pi} \frac{\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}}{1+\left(\frac{\tan(\frac{\omega}{2})}{\tan(\frac{\omega_c}{2})}\right)^{2N}} \frac{\tan^2(\frac{\omega}{2})}{\left(1+\tan^2\left(\frac{\omega}{2}\right)\right)}\, d\omega$$

On simplifying the above expression, we have

$$A_J = \frac{4\, B_N^2 \left(\tan(\frac{\omega_c}{2})\right)}{\tan(\frac{\omega_c}{2})} \int_{-\infty}^{\infty} \frac{x^{2N}}{1+x^{2N}} \frac{x^2}{(x^2+a^2)^2}\, dx \tag{B.5}$$

where $a = \frac{1}{\tan(\frac{\omega_c}{2})}$. The method of solving real integrals using Cauchy's Residue theorem is used to evaluate (B.5).

$$A_J = \frac{8\,\pi B_N^2 \left(\tan(\frac{\omega_c}{2})\right)}{\tan(\frac{\omega_c}{2})} \left|(c_1 + c_2)\right| \tag{B.6}$$

where

$$\begin{aligned}
c_1 &= \frac{1}{N} \sum_{l=0}^{\frac{N}{2}-1} \frac{(2a^2-1)\sin\left(\frac{\pi(2\,l+1)}{2\,N}\right) + a^4\ \sin\left(\frac{3\,\pi(2\,l+1)}{2\,N}\right)}{\{1+a^4+2\,a^2\ \cos\left(\frac{\pi(2\,l+1)}{N}\right)\}^2} \\
&\qquad\qquad \textit{for even N} \\
&= \frac{1}{N} \sum_{l=0}^{\frac{N}{2}-\frac{3}{2}} \left[\frac{(2a^2-1)\sin\left(\frac{\pi(2\,l+1)}{2\,N}\right) + a^4\ \sin\left(\frac{3\,\pi(2\,l+1)}{2\,N}\right)}{\{1+a^4+2\,a^2\ \cos\left(\frac{\pi(2\,l+1)}{N}\right)\}^2}\right. \\
&\qquad\qquad \left. -\frac{1}{2(1-a^2)^2}\right] \qquad \textit{for odd N} \\
c_2 &= \frac{a^{2\,N-1}(-1)^{N+1}}{4(1+(-1)^N\, a^{2\,N})}\left(1+\frac{2N}{1+(-1)^N\, a^{2N}}\right)
\end{aligned}$$

The jitter noise is therefore,

$$J = \frac{\sigma_{\Delta T_s}^2}{T^2}\, \frac{\sigma_{lsb}^2}{OSR} \frac{8\, B_N^2 \left(\tan(\frac{\omega_c}{2})\right)}{\tan(\frac{\omega_c}{2})} \left|(c_1 + c_2)\right| \tag{B.7}$$

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1. Reddy, K., and Pavan, S., “Fundamental limitations of continuous-time Delta-Sigma modulators due to clock jitter," in *Proc. IEEE Int. Symp. Circuits and Syst.(ISCAS)*, May 2006.

2. Reddy, K., and Pavan, S., “Fundamental limitations of continuous-time Delta-Sigma modulators due to clock jitter," IEEE Transactions on Circuits and Systems : Regular Papers, October 2007.