Design and Simulation Techniques for Low Distortion Drivers for Analog-to-Digital Converters

A THESIS

submitted by

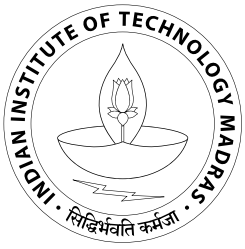
RAKSHITDATTA KIKKERI SHIVADATTA

for the award of the degree

of

MASTER OF SCIENCE

(by Research)



Department Of Electrical Engineering

Indian Institute of Technology Madras, India

June 2014

CERTIFICATE

This is to certify that the dissertation titled **Design and Simulation Techniques for Low Distortion Drivers for Analog-to-Digital Converters** , submitted by **Rakshitdatta Kikkeri Shivadatta**, to the Indian Institute of Technology Madras, for the award of the degree **Master of Science (by Research)**, is a bonafide record of the work done by him under my supervision. The contents of this dissertation, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Associate Professor,
Department of Electrical Engineering,
Indian Institute of Technology Madras,
Chennai 600 036

Place: Chennai
Date:

ACKNOWLEDGEMENTS

I am extremely grateful to Dr. Nagendra Krishnapura for providing me the opportunity to conduct research under him, and for the subsequent guidance. It has been a thoroughly enjoyable and educational experience for me. Through him, I feel I have inculcated the habit of doing things—technical as well as non-technical—the right way. I thank him for that. He is, and will always remain a role model for me.

A significant part of the work was carried out at Texas Instruments India Pvt. Ltd., Bengaluru, under the mentorship of Mitikiri Yujendra. I thank him for all the help he has provided me.

The courses taught by Prof. Shanthi Pavan and Dr. Sankaran Aniruddhan were top-notch and will definitely form the foundation for my career. I thank them for that.

I would like to thank my review committee members—Dr. Shankar Balachandran and Prof. Shanthi Pavan for their precious time and useful suggestions.

The analog group is a big one now and I am indebted to each and every student member—present and several past—for the help, guidance, and support that they have extended. It is only because of them that the labs are fun places to work.

I would like to thank Kamlesh, Sandeep, Ramprasath, Praveen, and Naga for all the fun we had outside the lab. Time spent with the Kannada gang comprising of Dileep, Praveen, Amrut and Vijay was very nice. Thanks to them.

I am also grateful for the people at Texas Instruments: S. Janakiraman, Dipankar

Mandal, and Anand Kannan for their inputs on chip design, P. Rajakumar for the layout design, Sharat Rudrasamudram, Deepak Matthew, and Hemant Deshmukh for their help with the test setup and measurements.

I dedicate this thesis to my parents. Without their love, support, care, and sacrifice none of this would have been possible. I also thank Darshan for the brother he is.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

ADC	Analog-to-Digital Converter
CMOS	Complimentary Metal Oxide Semiconductor
CMFB	Common Mode Feedback
DAC	Digital-to-Analog Converter
HD_2	Fractional Second Harmonic Distortion
HD_3	Fractional Third Harmonic Distortion
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed Circuit Board
PSD	Power Spectral Density
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion

CHAPTER 1

Introduction

1.1 Motivation

Improvements in semiconductor technology have led to drastic increase in the storage and processing capabilities of digital data. For example, it is not uncommon to see personal computers with multi core 64-bit processors running at a few GHz, having tens of gigabytes of memory accompanied by terabytes of storage space. Because of these improvements, it is preferred that most of the signal processing be done in the digital domain. However, most of the real world signals such as speech, light (radiation), temparature, pressure, etc. are analog and mostly non-electrical in nature. Sensors such as microphones, photodiodes, thermocouples, etc. pick up these analog real world signals and convert them into an analog electrical signal (voltage, current, charge, etc.). To utilize the advantages of digital domain, these analog electrical signals must be converted into their digital equivalents. This job is carried out by an analog-to-digital converter (ADC).

1.1.1 SAR based ADCs

Several applications such as test and measurement equipments, high fidelity audio systems, and data acquisition systems require high resolution ADCs. Successive approximation register (SAR) based ADC is a commonly chosen architecture for the implementation of high resolution converters. A block diagram illustrating the architecture is shown in Fig. 1.1. The principle of operation is briefly explained with the help of a 2-bit example. Initially, the ADC takes up

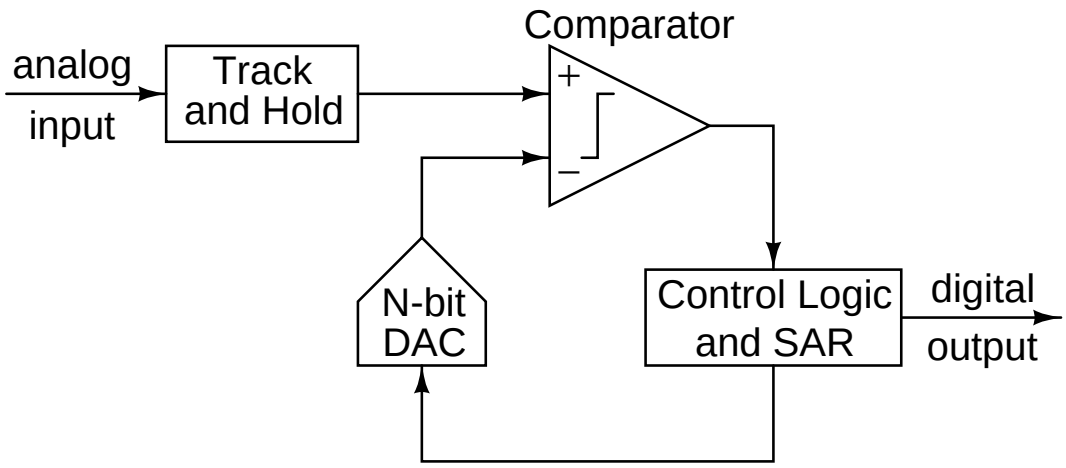


Figure 1.1: Block diagram of a SAR based ADC.

some time to sample the input signal. This is the process of acquisition. After the signal is acquired, the conversion process starts. In the first conversion cycle, input signal is compared with $V_{ref}/2$. This is the generated at the digital-to-analog converter (DAC) output by applying a digital input "10" from the control logic. If the input is greater than $V_{ref}/2$, then the most significant bit (MSB) of the digital code will be set to "1", else "0". Without loss of generality, let us assume that the input signal is greater than $V_{ref}/2$. In the next conversion cycle, the input will be compared with $V_{ref}/2 + V_{ref}/4$ ($V_{ref}/4$ if the input signal was lesser than $V_{ref}/2$). If the input signal is greater than $V_{ref}/2 + V_{ref}/4$, then the least significant bit (LSB) is also set to "1". It is set to "0" otherwise. The same explanation can be easily extended to higher resolutions.

1.1.2 SAR ADCs with capacitive DAC

Although any architecture can be chosen for the implementation of the DAC itself, the choice is usually a capacitive DAC (see [1] and [2]) as it provides the option of inherent track-and-hold of the input signal. With this choice, we can see that most of the circuitry is passive (DAC and the track-and-hold) or digital

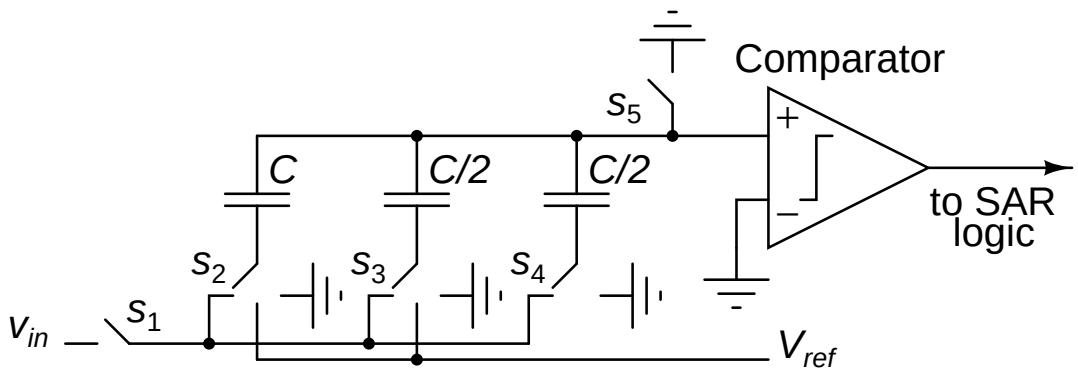


Figure 1.2: Circuit diagram of a 2-bit SAR ADC using capacitive DAC.

(control logic and SAR). This also lends itself to low power and low voltage operation. Fig. 1.2 shows the circuit diagram of a 2-bit SAR based ADC using a capacitive DAC. The digital circuitry is not shown. The converter operation is best explained with the help of modes.

Track Mode: During the track mode, switches s_1 and s_5 are closed. Switches s_2, s_3, and s_4 are connected to the analog input v_{in}. Therefore, the capacitor array will provide a total capacitance of $2C$ to the input and it will get charged to the analog input voltage v_{in}.

Hold Mode: During hold mode, the analog input is first disconnected by opening switch s_1. With this, the capacitor array stores a charge that is proportional to the input voltage v_{in}. We say that the input signal is held. Next, switch s_5 is opened. After that, the switches s_2, s_3 and s_4 are connected to ground. With this, the total voltage at the negative input of the comparator will be -v_{in}.

Charge Redistribution Mode: This is also known as bit cycling. During this phase, the actual conversion takes place. In the first bit cycle, switch s_2 is connected to the reference voltage V_{ref}. Since switches s_3 and s_4 are connected to ground, the reference voltage sees a series combination of capacitors of value C and C. Hence the total voltage at the negative terminal of the comparator will be $-v_{in} + V_{ref}/2$. If this voltage is negative, it implies that v_{in} is larger than $V_{ref}/2$. In that case, the switch s_2 is left as is. Else, it is reconnected to ground. With this,

the most significant bit of the output code is determined. In the next bit cycle switch s_3 is connected to the reference voltage V_{ref}. This will result in a voltage of $-v_{in} + V_{ref}/2 + V_{ref}/4$ at the negative input of the comparator. Based on whether the comparator output is low or high, switch s_3 is either left as is or reconnected to ground.

1.1.3 Total capacitance of the DAC

It should be noted that to realize a high resolution SAR ADC, the DAC within the ADC should also be of comparable resolution. To achieve high resolution in a DAC, it is necessary that all the unit elements within the DAC behave similarly. In the jargon of circuit design, this translates to all the unit elements being matched to each other. In a capacitive DAC, the unit elements are all capacitors and as per the previous arguement, all of them should be matched. It is a well-known fact that increasing the area of capacitors increases the matching between them ([3], [4], and [5]). Increasing the area also increases the capacitance of the unit element. It is because of this reason that the capacitance of the unit element in a high resolution DAC will normally be larger than the smallest possible value that can be realized in a given process. This, coupled with the large number of unit elements (2^n for an n-bit DAC) required for a high resolution capacitive DAC makes the total capacitance large. The total capacitance of the DAC in a high resolution converter can easily reach several tens of pF. These values are considered large inside an integrated circuit.

1.1.4 Switched-capacitor load

From the above explanation, we can see that a SAR ADC employing capacitive DAC presents a switched-capacitor load (series combination of a switch and total capacitance of the DAC) to the input signal source. There is a fundamental

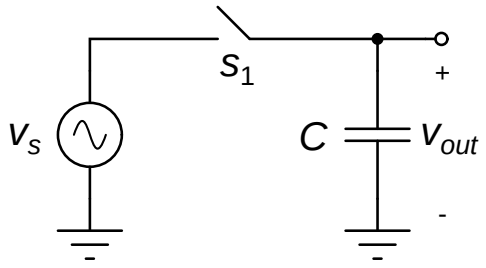


Figure 1.3: Ideal voltage source driving a switched-capacitor load.

problem in driving switched-capacitor loads especially when the input signal is changing. The problem is explained below.

Fig. 1.3 shows an ideal voltage source v_s driving a series combination of switch s_1 and a capacitor C. The voltage across the capacitor is v_{out}. For simplicity, we shall assume that the switch s_1 is ideal. i.e., it has zero ON resistance and infinite OFF resistance. Let us assume that the switch s_1 is intially closed. This makes $v_{out} = v_s$. At time instant t_1, let the switch s_1 be opened. Now, the output voltage will stay constant at $v_s(t_1)$ until the switch closes again. Let us assume that at instant t_2, the switch s_1 is closed again. As a result of closing of the switch, the output voltage will now be $v_s(t_2)$. Clearly, we can see that at the time instant t_2, there is a sudden change in the voltage across the capacitor from $v_s(t_1)$ to $v_s(t_2)$. To induce a sudden change in the capacitor voltage, an impulsive current should flow through it. Fig. 1.4 illustrates the phenomenon. For a given capacitance, higher the value of the step, higher will be the amount of the charge that should be dumped on it. This implies a larger impulsive current. Alternatively, for a given step voltage, as the capacitance increases, the amount of charge that should be dumped on it increases i.e., a larger impulsive current is required.

If an ideal voltage source is driving such a large capacitor, there wouldn't be any problems as the source can easily provide correspondingly larger impul-

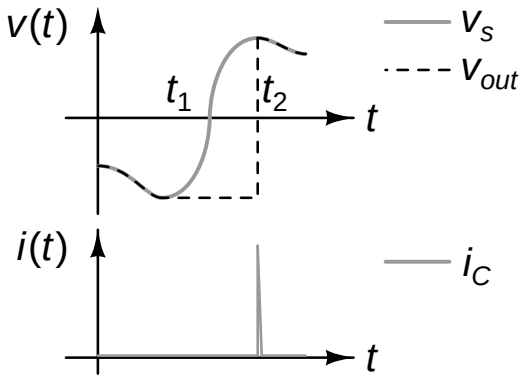


Figure 1.4: Representative waveforms for quantities in Fig. 1.3.

sive currents. However, no real world source is ideal and will have a limit to the maximum current that they can provide. The sensors, which themselves may be integrated circuits, will not be designed to provide (or even handle) such impulsive currents. Hence a separate driver stage which will isolate the sensor and the ADC is required and the addition of driver should not corrupt the signal. This makes the design of ADC driver circuitry a challenging exercise.

Traditionally, general purpose opamps are used for such drivers. The use of general purpose opamps might not be the most power efficient solution just because it is not optimized for the given application. Also, integration of the driver along with the ADC will significantly reduce the board complexity and space. This idea is not new and some commercial parts, which are multi-chip modules, are available which have integrated drivers. ADS8284 serves as an example even though it is presently discontinued. This dissertation will demonstrate the design and implementation of a driver to be used with an 18-bit ADC. Although the designed part is a stand alone driver, the author feels that the integration of the driver along with the ADC should not pose major challenges. In fact, a better performance can be expected as the effect of unnecessary bondwire inductances of the driver as well as the ADC, along with printed circuit board (PCB) trace inductance will be eliminated completely.

1.2 State of the art of ADC driver amplifiers

1.2.1 Evolution

It was mentioned earlier that the ADC manufacturers specify the use of general purpose opamps for the driver. This section shows the evolution of the ADCs and more importantly the driver circuits recommended along with it. The evolution of the devices from three manufacturers are studied separately. Common trends among them are identified. Qualitatively, their advantages and disadvantages are also pointed out. Most of the data in this section come from the datasheets.

The author wishes to bring the following point to the notice of the reader. Datasheets usually do not mention the choice of the technology for the part explicitly. In order to make an educated guess, the assumption that a complimentary metal oxide semiconductor (CMOS) part will have an input bias current smaller than 1 nA is made. For input bias currents greater then 1 nA, it is assumed that the technology used is Bipolar (or BiCMOS).

Texas Instruments: ADS8383 (500 kS/s at 110 mW) and ADS8381 (580 kS/s at 115 mW) were two of the industry's first 18-bit converters. They were released in 2002. The datasheet of ADS8383 does not have any details on driving the input signal. ADS8381 suggests the use of THS4031, a general purpose opamp. The converters support only single-ended inputs. Therefore a simple noninverting unity gain amplifier configuration is recommended. For doing the bipolar to unipolar conversion, an inverting amplifier configuration with a DC voltage applied to the non-inverting input terminal of the opamp is recommended.

ADS8380 (600 kS/s at 115 mW) and ADS8382 (600 kS/s at 115 mW) were released next in 2004. These were advanced versions of the previous devices boasting higher speeds. ADS8382 offered the option of fully-differential in-

put signals. Datasheets recommend the use of THS4031 as the opamp for the driver. For ADS8380, non-inverting unity gain amplifier configuration is recommended as the input is single-ended. A difference amplifier configuration is recommended for bipolar to unipolar conversion. For ADS8382, for converting a single-ended signal to differential signal, a combination of inverting and non-inverting unity gain amplifiers are shown. The non-inverting amplifier gives a buffered version of the input signal at its output while the inverting amplifier gives an inverted version at its output. With this the single-ended signal is converted to a fully-differential version with a gain of 2. The important thing is to note that the input is directly applied to both of the unity gain amplifiers. For fully-differential inputs, the two arms are separately buffered from non-inverting unity gain amplifiers.

ADS8481 (1 MS/s at 225 mW), ADS8482 (1 MS/s at 225 mW), and ADS8484 (1.25 MS/s at 234 mW) were released next. ADS8481 supports single-ended input while ADS8482 supports fully-differential input. THS4031 is the recommended opamp for driver circuitry. Configurations that are recommended with ADS8380 is again recommended with ADS8481. For ADS8482 and ADS8484, for single-ended to differential conversion, cascade of non-inverting and inverting amplifiers are shown. For fully-differential input, two difference amplifiers are used with each arm. This has been done to have the option of adding some common-mode to the input. To add common-mode, a DC voltage is provided on non-inverting input of the opamp.

THS4031 is a 100 MHz , low noise bipolar (input bias current of 3 μA) opamp. The quiescent current consumption is 7.5 mA with a $\pm$5 V supply. This corresponds to a power consumption of 75 mW. For fully-differential operation, use of two such opamps is necessary which doubles the power consumed by the driver circuitry.

Recently, very low power converters were released. They are ADS8881 (1 MS/s

at 5.5 mW), ADS8883 (680 kS/s at 4.2 mW), ADS8885 (400 kS/s at 2.6 mW), and ADS8887 (100 kS/s at 0.7 mW). Datasheets of these devices and related documents recommend the use of OPA250, OPA320 and THS4521. OPA350 and OPA320 are single-ended opamps. For fully-differential input, two of these opamps in non-inverting unity gain amplifier configuration are recommended. THS4521 is a fully-differential opamp and can handle both single-ended and fully-differential signals.

OPA320 is a 20 MHz CMOS (input bias current of 0.2 pA) single-ended opamp. The quiescent current consumption is 1.5 mA with a 5 V supply. This corresponds to a power consumption of 7.5 mW.

OPA350 is a 38 MHz CMOS (input bias current of 0.5 pA) single-ended opamp. The quiescent current consumption is 5.2 mA with a 5 V supply corresponding to a total power consumption of 26 mW. The THD performance of this device is not specified in the datasheet.

THS4521 is a 145 MHz fully-differential opamp in a bipolar process (input bias current of 0.9 μA). The quiescent current consumption is only 1.15 mA.

Analog Devices: AD7674 (800 kS/s at 98 mW), AD7679 (500 kS/s at 76 mW), and AD7678 (100 kS/s at 18 mW) represent the earliest converters from the manufacturer. AD7641 (2 MS/s at 75 mW) and AD7643 (1.25 MS/s at 65 mW) came next which was a speed upgrade on the previously mentioned parts. AD8021 is the recommended opamp in all of the datasheets. For single-ended to differential conversion, the cascade of non-inverting and inverting unity gain amplifiers is recommended while for fully differenial inputs, two non-inverting unity gain amplifiers for the two arms is recommended.

AD8021 is a 200 MHz single-ended opamp in a bipolar process (input bias current of 7.5 μA). The quiescent current consumption is 6.8 mA.

Low power converters AD7690 (upto 400 kS/s) and AD7691 (upto 250 kS/s)

were also released around the same time as AD7643/41. These datasheets recommend the use of ADA4941 as the driver. ADA4941 is a monolithic single-ended to differential converter. Several other parts such as ADA4841, AD8655, AD8021/22, and AD8615 are also specified.

ADA4941 is a 31 MHz single-ended to differential converter in a bipolar process (input bias current of 3 μA). Functional block diagrams of ADA4941 show a cascade of non-inverting and inverting unity gain amplifiers. The quiescent current consumption is 2.3 mA with a 5 V supply.

ADA4841 is an 80 MHz single-ended opamp in a bipolar process (input bias current of 3 μA). It seems that ADA4941 is made out of these opamps as the input bias current is same as ADA4941 with the total quiescent current consumption being exactly half (1.15 mA).

AD8655 is a precision CMOS buffer as mentioned in the datasheet. It has a 28 MHz bandwidth. This part consumes 3.7 mA quiescent current with 5 V supply.

AD7634 (680 kS/s at 180 mW) and AD7631 (250 kS/s at 73 mW) were released later. Datasheets show similar circuits to what was shown in AD7674/78/79. AD8021/22 was the choice specified. They also specify ADA8922 and AD8610.

ADA8922 is a single-ended to differential converter in a bipolar process (input bias current is 1.5 μA.) It has a small-signal bandwidth of 38 MHz. Quiescent power consumption is 70 mW with a $\pm$5 V supply.

AD8610 is a 25 MHz JFET input single-ended opamp. It needs a dual supply of atleast $\pm$5 V. It takes a quiescent current of 2.5 mA.

The parts that were released next were AD7982 (1 MS/s at 7 mW), AD7984 (1.33 MS/s at 10.5 mW), and AD7986 (2 MS/s at 15 mW). ADA4841 in non-inverting unity gain amplifier configuration was recommended for the driver circuitry. Other parts that are recommended are ADA4941, ADA4899, AD8014,

AD8021/22, and AD8655.

ADA4899 is a 600 MHz bipolar (input bias current of 100 nA) single-ended opamp. The quiescent current consumption is 14.7 mA with a 5 V supply.

AD8014 is a 400 MHz bipolar (input bias current of 10 μA) single-ended opamp. It takes a quiescent current of 1.15 mA at 5 V supply. The distortion peformance at low frequenices is not specified.

AD7608 and AD7609 were next released. These are data acquisition systems in themselves, which has input drivers built in. AD7608 is a single-ended input version while AD7609 has facility to handle fully-differential inputs. Functional block diagrams show the use of fully-differential amplifiers for the driver circuitry.

Recently, AD7960 (5 MS/s at 46 mW) was released. ADA4899 is specified with it for the high frequency operation.

Linear Technology: LT2376 (250 kS/s at 3.4 mW), LT2377 (500 kS/s at 6.8 mW), LT2378 (1 MS/s at 13.5 mW), and LT2379 (1.6 MS/s at 18 mW) were the first set of converters released by the manufacturer. For single-ended input signal, each of the datasheets recommend the use of LT6350 which is a single-ended to differential converter. For buffering fully-differential inputs LT6203 is specified. Two single-ended non-inverting amplifiers for each of the arms is suggested.

LT6350 is a 33 MHz single-ended to differential converter in a bipolar process (input bias current is 1.2 μA). Functional block diagram shows a cascade of non-inverting and an inverting unity gain amplifier used to achieve the necessary conversion. The part consumes 24 mW power with a 5 V supply.

LT6202 is a 100 MHz single-ended opamp in a bipolar process (input bias current is 1.3 μA). The part consumes 15 mW power with a 5 V supply.

LT2364 (250 kS/s at 3.4 mW), LT2367 (500 kS/s at 6.8 mW), LT2368(1 MS/s at

13.5 mW), and LT2369 (1.6 MS/s at 18 mW) were also released. These are the single-ended input counterparts of the previously mentioned parts. Each of the datasheets recommend the use of LT6202. The non-inverting unity gain amplifier configuration is recommended.

LT2336 (250 kS/s at 28 mW), LT2337 (500 kS/s at 35 mW), and LT2338 (1 MS/s at 50 mW) were released very recently. These devices have internal references along with reference buffers leading to an increased power consumption. The datasheets specify the use of LT1469, a single-ended opamp for driver circuitry. The cascade on noninverting and inverting unity gain amplifiers is specified for handling single-ended inputs. Two non-inverting unity gain amplifiers are recommended for differential signal driving.

LT1469 is a dual 90 MHz single-ended opamp in bipolar technology (input bias current is around 10 nA). The part consumes a quiescent current of 3.8 mA $\pm$5 V dual supply. Dual supply is necessary for the best performance.

Along with the previously mentioned converters, LT2328 (1 MS/s at 50 mW) was also released. This seems to be a single-ended input version of LT2338. The datasheet shows the usage of LT1468 as the driver. The non-inverting unity gain amplifier is the recommended architecture. LT1468 is a single version of LT1469.

LT2389 (2.5 MS/s at 162.5 mW)is the latest of the converters. It has internal reference and reference buffers. LT6201 is specified. LT6201 is 145 MHz single-ended opamp in a bipolar process (input bias current is 10 μA). It consumes a quiescent current of 15 mA with 5 V supply.

1.2.2 Common trends

The following trends can be seen from the history presented in the previous subsection.

The earliest converters were relatively slow offering speeds of several hundreds of kS/s and supported only single-ended inputs. Such converters typically consumed around a few hundreds of mW. With these converters, high bandwidth low noise general purpose opamps were recommended for driver circuitry. These opamps consumed several tens of mW of power. The power consumption of the driver circuitry was smaller than the power consumed by the converter. Popular architectures for driver included the non-inverting unity gain amplifier for single-ended unipolar input and a difference amplifier for the bipolar to unipolar conversion.

Converters with similar speed and power numbers that started supporting fully-differential input came next. For driving such converters, a combination (cascade as well as parallel) of non-inverting and inverting unity gain amplifiers were recommended for single-ended to differential conversion. For driving fully-differential input signal, two non-inverting unity gain amplifiers was suggested. Two general purpose opamps were required for the driver circuitry which increased the power consumption by a factor of 2. However, even with this increase, the power consumed by the driver circuitry was less or comparable to the power consumed by the converter.

With time, the power consumption of the converters have gradually decreased along with increased speeds. Converters offering $\sim$1 MS/s speeds at a few mW of power are available. With this came the need for reduction in power consumption of the driver circuitry also. Specialized opamps, mostly in bipolar technology which consume a few mW of power themselves are recommended for driving. Monolithic single-ended to differential converters employing a cascade of non-inverting and inverting unity gain amplifiers are also available. These reduce the complexity when compared to the use of two single-ended opamps explicitly.

To reduce the complexity and cost at the board level, effort is now being put into

integrating the reference, reference buffers, and the input buffers along with the converter. Converters with integrated refernces and reference buffers are available in the market. Several complicated techniques like multi chip module were being used to accomplish this. To further reduce the cost of such integrated converter, it is required that the driver circuitry be in the same technology as that of the converter. This dissertation investigates the possibility of low noise and distortion driver amplifiers in CMOS technology with the final aim of integrating them with the converter.

1.3 Overview of the thesis

Chapter 2 is devoted to the architecture of the input driver. Analysis of several possible architectures is given, and based on that, the advantages and shortcomings are pointed out.

Based on the analysis shown in Chapter 2, a fully-differential opamp based driver amplifier is designed in a $0.6\,\mu$m CMOS process. Chapter 3 deals with the design, simulation and layout details of the same. The measurement setup used and the results obtained with prototype chips are presented in Chapter 4.

Chapter 5 deals with a new technique for simulating the per element distortion contributions in an analog circuit. It includes motivation for the work, working principle and related theoretical aspects.

Chapter 6 deals with the analysis of the effect that the common-mode feedback circuitry has on the slew rate in amplifiers. Simulation results corroborating the analysis are also presented. The dissertation concludes in Chapter 7 with a discussion on the achieved results and suggestions for future work.

CHAPTER 2

A Study of Driver Architectures

2.1 Introduction

Circuitry used for driving the input signal to a high resolution ADC will have to usually meet very stringent requirements such as: low noise and distortion—should ideally be lower than, or atleast comparable to, the noise and distortion added by the converter itself (usually, this will amount to a fraction of the LSB), rail-to-rail signal swing at the input and output—to possibly utilise the entire range of converter, high drive capability—to drive the large load presented by the converter, fast response to step like inputs—if they are to be used in time multiplexed systems. These requirements have to be met with the smallest area and power dissipation possible. The focus of this chapter is to zero in on the architectures that are best suited for implementation of a prototype driver that can meet such requirements.

The chapter is organized as follows. Using the non-inverting amplifier configuration in the driver circuitry leads to problems whenever rail-to-rail signal swing at the input side has to be supported. Architectures that employ non-inverting amplifier configuration are first presented in Section 2.2. Section 2.3 presents the details regarding rail-to-rail swing with a brief summary at the end. Although using architectures employing inverting amplifier configuration can alleviate the problems associated with rail-to-rail input signal swing, a design trade off between total noise at the output and gain error (or equivalently, the input impedance) is encountered. Architectures based on the inverting amplifier configuration and the details regarding the trade off are presented in Sections 2.4 and 2.5 respectively.

2.2 Architectures employing non-inverting amplifier configuration

Several commonly used architectures (see [6], for instance) that use the non-inverting amplifier configuration are depicted in Fig. 2.1. The architectures shown are only those that can carry out single-ended to differential conversion with a gain of 2. Slight modifications can make the driver suitable to provide a single-ended output from a single-ended input or a fully-differential output from a fully-differential input.

2.2.1 Cascade architecture

Fig. 2.1(a) shows the cascade of non-inverting and inverting unity gain amplifiers. Because of the non-inverting unity gain amplifer, the input impedance seen is high. However, the input referred noise voltage of the opamp in the non-inverting unity gain amplifier also gets amplified by a factor of 2 because of the inherent gain. The cascade combination can also be realised in the other way where the inverting configuration precedes the non-inverting configuration. This architecture will provide an input impedance of R. Further, the input referred noise voltage of the inverting amplifier, which includes the noise from opamp as well as the input and feedback resistors, gets amplified by a factor of 2. Therefore it is always better to have the non-inverting configuration precede the inverting configuration in a cascade connection.

2.2.2 Parallel architecture

Fig. 2.1(b) shows a parallel combination of non-inverting and inverting unity gain amplifiers. Unlike the cascade architecture, the input referred noise voltage of the opamp in the non-inverting amplifier does not get amplified. How-

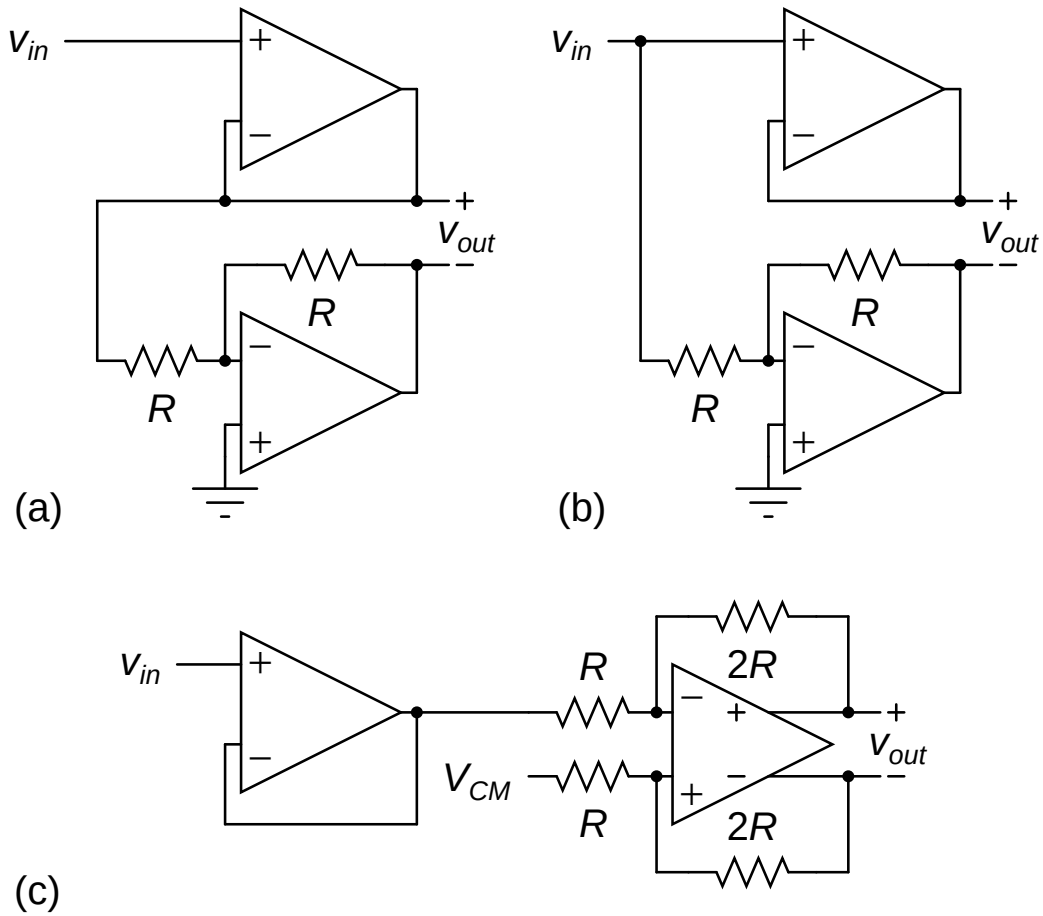


Figure 2.1: Driver architectures involving non-inverting amplifier configuration. (a) Cascade of non-inverting and inverting unity gain amplifiers. (b) Parallel combination of non-inverting and inverting unity gain amplifiers. (c) Cascade of non-inverting unity gain amplifier and a fully-differential amplifier.

ever, the input impedance of this architecture is roughly R because of the inverting amplifier. It is important to note that in both the architectures, cascade and parallel, the two anti-symmetric components of the fully-differential signal are generated separately in a pseudo differential manner. Since the two components travel through significantly different paths, they will experience difference delays. Any delay between the two components of a fully-differential signal will translate to a small gain error[1].

[1]Here the assumption is that the delay between the relevant components is small. Under this condition, the gain error seen will be small.

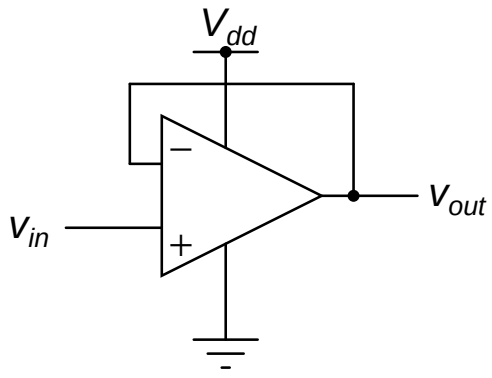


Figure 2.2: Non-inverting unity gain amplifier.

2.2.3 Fully-differential opamp based architecture

Fig. 2.1(c) shows the architecture where the single-ended to differential conversion is carried out by the fully-differential amplifier. This will ensure that there is no delay between the anti-symmetric components of the fully-differential output. The front end unity gain amplifier provides very high input impedance. To maintain the consistency with the other architectures, the fully-differential amplifier is shown to have a gain of 2. As this is essentially yet another cascade architecture, the input referred noise voltage of the opamp in the non-inverting unity gain amplifier will be amplified by a factor of 2 by the following stage.

2.3 Rail-to-rail signal swing

As mentioned in section 2.1, the usage of non-inverting amplifier configuration can lead to significant problems when the requirement of rail-to-rail signal swing at the input is pressed upon. To illustrate the problem clearly, consider the simple case of the non-inverting unity gain amplifier as shown in Fig. 2.2. Let us assume that the driver runs off a single power supply V_{dd} as shown in Fig. 2.2. Let us also assume that the unity gain amplifier has to support a rail-to-rail swing at the input side, i.e., $0 \leq v_{in} \leq V_{dd}$. From the figure, it is clear that if input has a rail-to-rail swing, then the output should also have a rail-

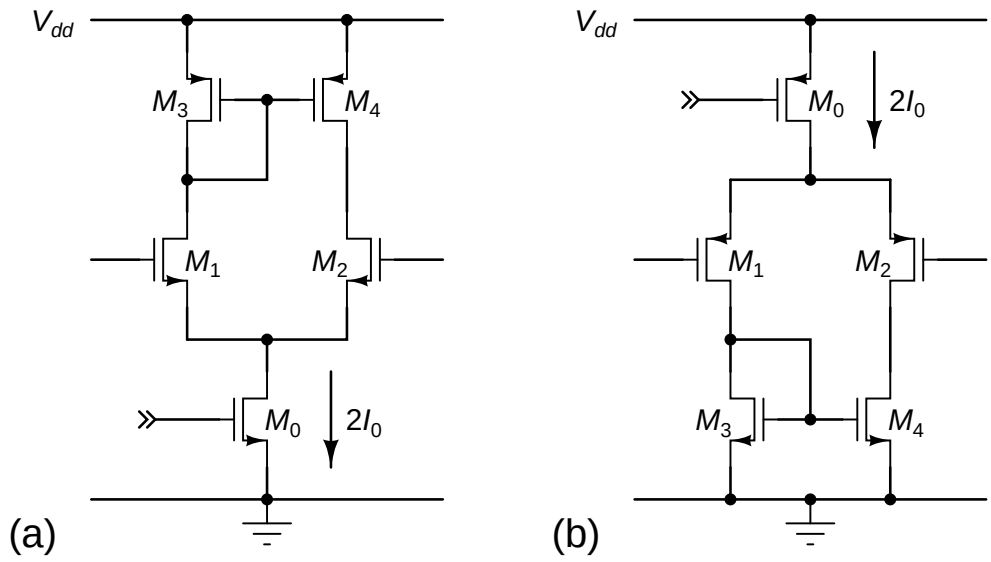


Figure 2.3: Circuit diagram of a differential amplifier with active current mirror load employing (a) nMOS input pair (b) pMOS input pair.

to-rail swing, i.e., $0 \leq v_{out} \leq V_{dd}$. For now, we shall assume that this is true[2]. We consider the various choices available for the implementation of the input stage of an opamp and point out their shortcomings as far as them supporting rail-to-rail input signal swing is concerned.

2.3.1 Differential amplifier with active current mirror load

The most common choice for the input stage of an opamp is the differential amplfier with an active current mirror load ([7], [8], [9], and [10]). Fig. 2.3(a) and (b) show the two possible flavors of the differential amplifier. M_1 and M_2 form the input pair, M_3 and M_4 form the current mirror load, and M_0 is the current source which biases the stage under consideration. Let us assume that $2I_0$ is the value of the tail current source.

Investigating the stage yields the following. For the sake of pithiness, in the following subsections only the case of nMOS input pair is considered for anal-

[2]The assumption probably stems from the fact that in a Bipolar process, the output swing is limited by V_{CEsat} which can be around 0.1 V while the input swing is limited by V_{BE} which is usually around 0.7 V.

ysis. With appropriate changes to the polarity of voltages and currents, similar arguments can be made for the case with pMOS input pair. In order to achieve high DC gain out of this stage,[3] it is necessary that all the transistors operate in the saturation region. This condition limits the possible range of the input signal that can be applied to the stage. The limits are evaluated as follows.

The lowest possible value that the input can take is sum of the minimum drain-source voltage required to keep M_0 in saturation and the gate-source voltage required by M_1 to carry a current I_0. That is,

$$v_{i,min} = V_{DSAT_{M_0}}\Big|_{2I_0} + V_{GS_{M_1}}\Big|_{I_0} \tag{2.1}$$

To get a feel for these quantities, following values of $V_{DSAT} = 100\,\text{mV}$ and $V_T = 600\,\text{mV}$ are assumed. These values are seen to be reasonable in the chosen process. pMOS devices have a higher V_T, however, it is also assumed to be equal to 600 mV for the sake of convenience. With these values, it can be seen that the lower limit for the input signal is 800 mV. This forms a significant fraction of V_{dd} , which is nominally 5 V.

On the upper side, if the input voltage becomes greater than the drain voltage of M_1 by $V_{T_{M_1}}$ (threshold voltage of M_1), then transistor M_1 will operate in the triode region. It can be seen that the drain of the input transistors M_1 and M_2 will be lower than V_{dd} by a value that is equal to the gate-source voltage required by the transistors M_3 and M_4 to carry a current of I_0. Therefore,

$$v_{i,max} = V_{dd} - V_{GS_{M_3}}\Big|_{I_0} + V_{T_{M_1}} \tag{2.2}$$

Plugging in the assumed values for these quantities, the input signal can reach to within 100 mV of power supply. Therefore, from the above analysis, it is clear that the stage under consideration does not support rail-to-rail swing at

[3] In any opamp, the first stage should always provide significant portion of its total gain.

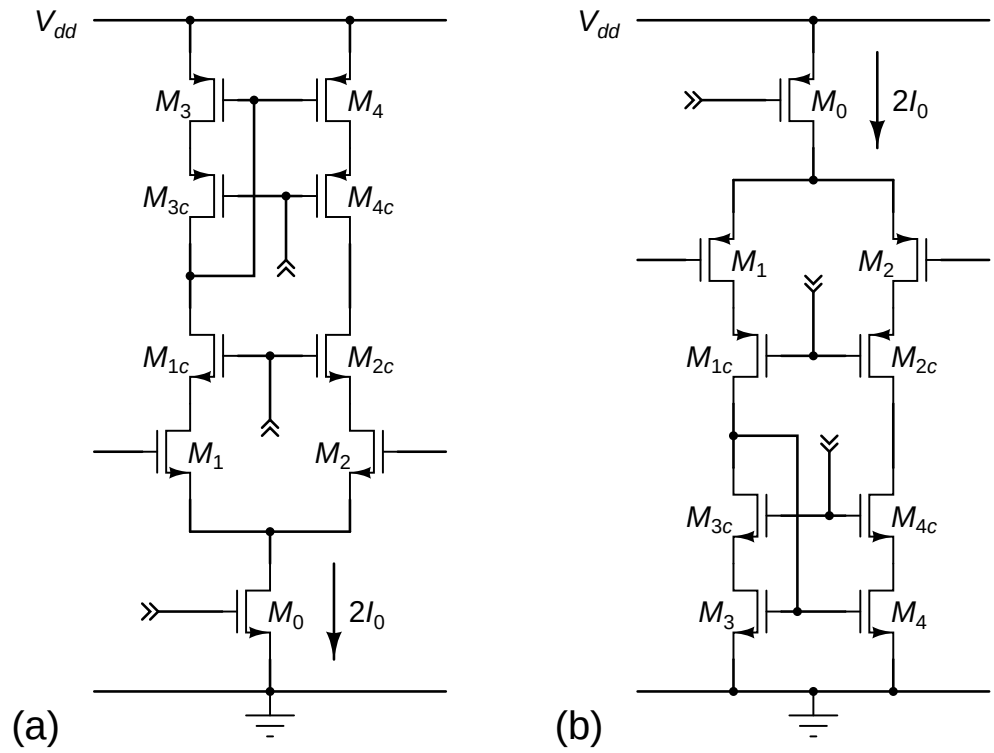


Figure 2.4: Circuit diagram of a telescopic cascode differential amplifier with active current mirror load employing (a) nMOS input pair (b) pMOS input pair.

the input. The available range is limited on both sides, and significantly more on the lower side.

2.3.2 Telescopic cascode

Yet another commonly used structure is what is dubbed as telescopic cascode differential amplifier. Cascoding is carried out for input pair and load transistors in this version. Fig. 2.4 shows the two flavors. M_{1c} and M_{2c} form the cascodes for the input pair transistors. M_{3c} and M_{4c} form the cascodes for the load transistors. Although the main motivation for cascoding is to achieve higher DC gain than the previously considered stage, the swing limits are evaluated here only for the sake of completeness. One added benefit of cascodes, especially for the input pair transistors is the reduction of Miller multiplied input

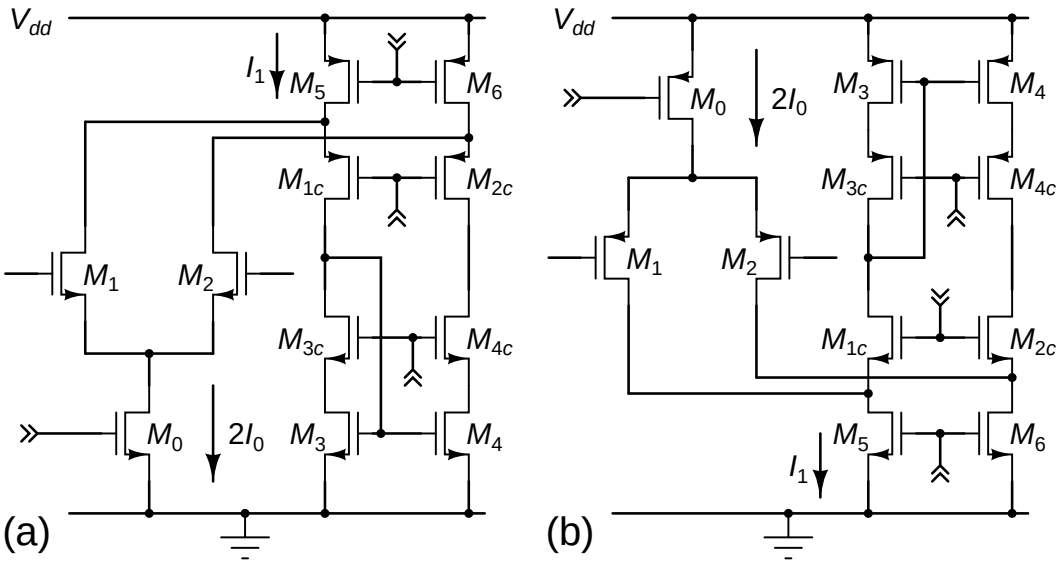


Figure 2.5: Circuit diagram of a folded cascode differential amplifier with active current mirror load employing (a) nMOS input pair (b) pMOS input pair.

capacitance[4].

Proceeding on similar lines for evaluating the swing limits, the lower limit to the input voltage remains the same as was discussed in the previous subsection (relevant circuit topology is the same). However, the higher limit to the input voltage will be smaller than what was calculated earlier because of the need to provide sufficient drain-source voltage for the cascode transistors (M_{1c} and M_{2c}) so that they remain in saturation. From this, we can conclude that the choice of telescopic cascode stage is only worse than the one considered in the previous subsection.

$$v_{i,min} = V_{DSAT_{M_0}}\Big|_{2I_0} + V_{GS_{M_1}}\Big|_{I_0} \tag{2.3}$$

$$v_{i,max} = V_{dd} - V_{GS_{M_3}}\Big|_{I_0} - V_{DSAT_{M_{1c}}}\Big|_{I_0} + V_{T_{M_1}} \tag{2.4}$$

[4]A more subtle advantage is that the difference between the Miller multiplied capacitance seen on the two input terminals is also reduced.

2.3.3 Folded cascode

From the previous subsection, it is clear that introducing cascodes reduces the available signal swing at the input. A technique that is similar in spirit but different in implementation is the use of folded cascodes (using opposite polarity devices for the cascode transistor). Fig. 2.5 illustrates the folded cascode counterparts of those shown in Fig 2.4. pMOS transistors M_{1c} and M_{2c} form the cascodes for the nMOS input pair. As is evident from the figure, only the input pair transistors are cascoded with opposite polarity transistors. The load transistors are cascoded traditionally. Further, M_5 and M_6 are two extra current sources that are necessary for biasing the cascode transistors (M_{1c} and M_{2c}). Let us assume that they carry a current I_1.

From Fig. 2.5 we can find that the lower limit to the input voltage still remains the same as discussed previously (the relevant topology still remains the same). On the upper side, it can be seen that the drain of the input transistors will be one overdrive voltage away from V_{dd}. This is to ensure that the biasing current sources (M_5 and M_6) remain in saturation. We know that the gate voltage of the input transitors can exceed the corresponding drain voltage by a value equal to the threshold voltage of the input transistor. Therefore, the following can be written.

$$v_{i,min} = V_{DSAT_{M_0}}\Big|_{2I_0} + V_{GS_{M_1}}\Big|_{I_0} \tag{2.5}$$

$$v_{i,max} = V_{dd} - V_{DSAT_{M_5}}\Big|_{I_1} + V_{T_{M_1}} \tag{2.6}$$

Using the previously assumed valued for V_{DSAT} and V_T, it can be seen that the upper limit to the input voltage can even be greater than V_{dd} . To summarize, the folded cascode structure in itself will not support rail-to-rail swing at the input. However, it is important to keep in mind that the available swing is limited only on one end. With an nMOS input pair, the limitation is towards the lower rail. Similarly with a pMOS input pair, the limitation will be towards

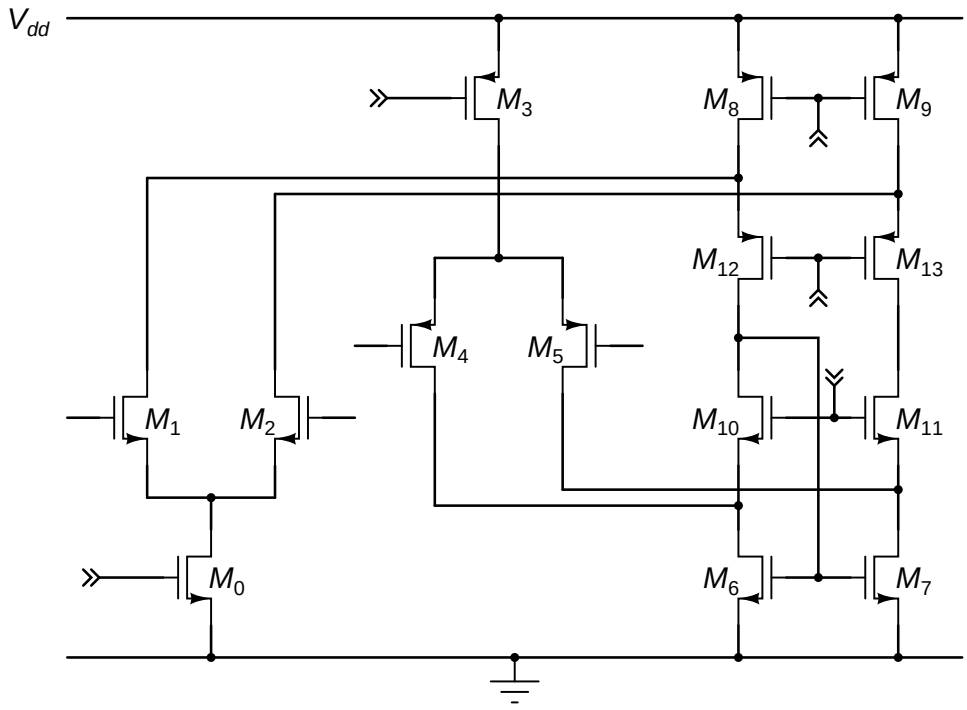


Figure 2.6: Circuit diagram of a differential amplifier with complementary input pairs.

the upper rail.

2.3.4 Complementary input pair

Complementary input pair structure, christened so because of the simultaneous use of opposite polarity devices (nMOS and pMOS)[5] was demonstrated in [11] and [12]. It uses the fact that having an nMOS input pair allows one to apply input signals up to the upper rail while having a pMOS input pair will allow signals up to the lower rail as well. Fig. 2.6 shows such an arrangement. M_1 and M_2 form the nMOS input pair biased from M_0. Similarly, M_4 and M_5 form the pMOS input pair. M_3 forms the corresponding tail current source. These pairs can be thought of as differential transconductor blocks in themselves with the output being currents. Now, as the two pairs appear in parallel, the currents have to be suitably added to form the final output. $M_6 - M_{13}$ forms the sum-

[5]The original demonstration was with NPN and PNP Bipolar transistors.

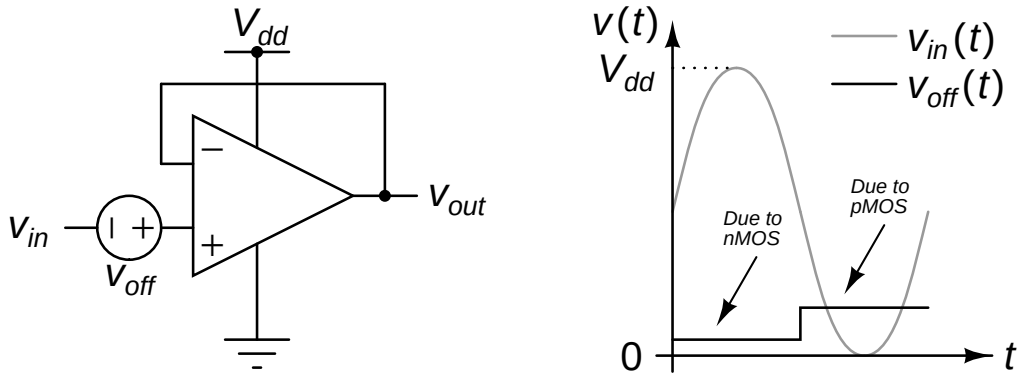


Figure 2.7: (a) Unity gain amplifier with the input referred offset voltage and (b) representative waveforms for input and input referred offset voltage.

ming block. This circuit arrangement will definitely support rail-to-rail input swing.

Although the topology provides the advantage of truly rail-to-rail input swing, it comes with several disadvantages. For input values close to the lower rail, only the pMOS input pair will be active while for values close to the upper rail, only the nMOS input pair will be active. For the intermediate range, both the pairs will be active[6] . Therefore the parameters of the system such as the total transconductance (g_m), gain, and the input referred offset all depend on the signal. This dependency induces significant nonlinear distortion at the final output.

Several techniques have been proposed that ensure that the stage provides a constant g_m and the problem is still attracting considerable interest. See [13] and the references within. These techniques only ensure that the stage provides a constant g_m, and thereby reducing the nonlinear behaviour caused by it. However, the problem of signal dependent input referred offset votlage still persists. As will be shown next, this problem effectively renders the complementary input pair stage useless for use in very low distortion designs.

Consider the unity gain amplifier shown in Fig. 2.7(a). The input referred offset

[6]Suitable biasing can also lead to niether being active as in a typical Class B operation

is shown as an ideal voltage source at the non-inverting input of the opamp. Let us assume that a rail-to-rail input at a frequency f_{in}, as shown in gray in Fig. 2.7(b) is applied. As explained earlier, for input signal close to the lower rail, only the pMOS input pair is active. Therefore the input referred offset is essentially the offset produced by the mismatch in the pMOS input pair[7]. Similarly, for input signals close to the upper rail, only the nMOS input pair is active and the input referred offset is essentially the offset produced by the mismatch in the nMOS input pair. The actual variation of the input referred offset voltage in the presence of an input signal will be complicated. However the following zeroth order approximation is made. For signal values above $V_{dd}/2$, the input referred offset is only because of the nMOS input pair and for signal values below $V_{dd}/2$, the offset is only because of the pMOS input pair. This is pictorially depicted in black solid line in Fig. 2.7(b). The step in the offset voltage is chosen arbitrarily for this figure as the purpose is only of demonstration.

Within the chosen process, the difference in the offset (due to the mismatch) between pMOS input pair and nMOS input pair is seen to be in several tens of μV. For example, the difference in 3σ offset with 100($10\,\mu$m/$1\,\mu$m) transistors biased at $500\,\mu$A current is $\sim 35\,\mu$V[8]. From Fig. 2.7(a), it is clear that the offset voltage directly appears at the output as it is. Therefore, we see harmonics at the output. To find out the strength of these harmonics, the input referred offset signal can be easily represented by a Fourier series as follows. This is based on the approximation made earlier.

$$v_{off}(t) = \frac{2V_{off,diff}}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \cdot \sin(2\pi n f_{in} t) \tag{2.7}$$

where $V_{off,diff}$ denotes the difference in the offset voltage of the two input pairs.

[7]The offset contribution due to the mismatch in the load transistors is neglected.

[8]These results are obtained from a 100 run Montecarlo simulation including process variations.

Substituting the value of 35 μV for $V_{off,diff}$, the first five significant harmonics are evaluated and listed in the table below. It is important to note that the higher

Table 2.1: Harmonics originating from signal dependent input referred offset voltage

Harmonic	Amplitude (μV)
Third	7.4
Fifth	4.45
Seventh	3.18
Ninth	2.47
Eleventh	2.02

harmonics do contribute and cannot be neglected. To get a feel for the distortion that gets introduced because of this effect, it is helpful to recall that for an 18-bit ADC, with 5 V reference and fully-differential operation, 1 LSB will correspond to $\sim$38 μV. Assuming a 10 V signal, with the first five significant harmonics, the THD at the output can be calculated to be around -120 dB. Therefore, the stage cannot be used if the specification is around -120 dB[9] as sufficient margin should be allotted for the nonlinear distortion created by the circuitry itself.

2.3.5 Charge pump based design

[14] demonstrates a technique that circumvents the problems associated with complementary input pair stage. The basic principle is to increase the effective power supply voltage provided to the stage and thereby increase the allowable signal range such that it includes the original rail-to-rail swing expected. For instance, consider the case where V_{dd} is doubled by some scheme (see [15], for instance) and used with the folded cascode stage with pMOS input pair as shown in Fig. 2.5(b). Then, the available signal swing can be evaluated as follows.

$$v_{i,max} = 2V_{dd} - V_{DSAT_{M_0}}\Big|_{2I_0} - V_{GS_{M_1}}\Big|_{I_0} \tag{2.8}$$

[9]It will be seen later that the specification chosen is indeed -120 dB

$$v_{i,min} = V_{DSAT_{M_5}}\Big|_{I_1} - V_{T_{M_1}} \tag{2.9}$$

As explained in subsection 2.3.3, the stage can support input signals as low as the lower rail. With the higher power supply, the stage can now easily support input signals as high as the original upper rail (V_{dd}). A similar scheme of creating $-V_{dd}$ and using it as the lower rail will render rail-to-rail swings for stages with nMOS input pair.

The disadvantages with charge pump based rail-to-rail input stages are the following. The power dissipation of the input stage doubles effectively because of the increased power supply. The charge pump circuit requires a clock for its operation. Clock generation and distribution will complicate the design and further increases the power dissipation. Clock feedthrough and mixing with signal can lead to spurs and intermodulation distortion components at the output respectively thereby reducing the dynamic range and SNR of the circuit. Also, with the higher supply, sufficient care will have to be taken to reduce the possibility of device breakdown.

2.3.6 Summary

In the design of a non-inverting unity gain amplifier with rail-to-rail swing, the traditional differential amplifier and its telescopic cascoded version are not suitable as they cannot support the necessary swing. The folded cascode provides improved performance compared to the other two but still cannot support rail-to-rail swing. Use of complementary input pair structure provides rail-to-rail swing, however brings along with it added distortion at the output because of the dependence of g_m and input referred offset on the input signal. This makes the topology unsuitable for very low distortion designs. Use of a charge pump allows one to use the differential amplifier or its cascoded versions to allow for rail-to-rail swing. Increased power consumption and spurs due to clock

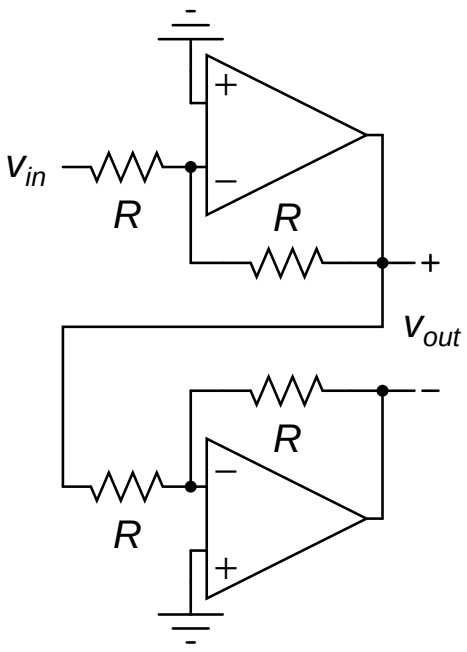


Figure 2.8: Cascade of two inverting unity gain amplifiers

feedthrough render it impractical for low power and low distortion designs. Therefore the non-inverting unity gain amplifier is not suitable for very low distortion designs.

2.4 Architectures employing inverting amplifier configuration

Based on the discussion presented in the previous section, the use of the non-inverting configuration in the driver circuitry is not feasible. Therefore, we have to make do with the inverting configuration. This section deals with the architectures based on inverting configuration. Architectures involving a fully-differential opamp are thought to be similar to inverting configuration as the gain expressions are similar. These are also examined in this section. To maintain consistency with what was described in section 2.2, architectures that pro-

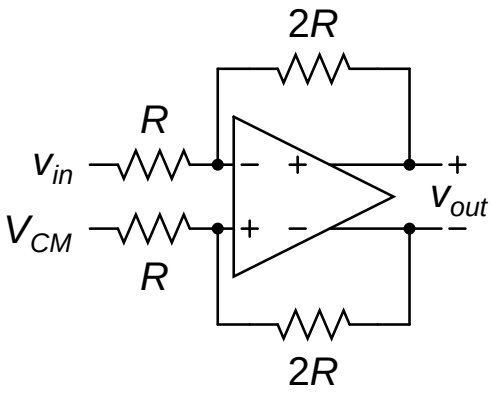


Figure 2.9: Fully-differential amplifier employing a fully-differential opamp.

vide single-ended to differential conversion with a gain of 2 are considered. However, simple manipulations can be done to provide a single-ended output from a single-ended input or a fully-differential output from a fully-differential input.

2.4.1 Cascade of two inverting amplifiers

Fig. 2.8 depicts the cascade of two inverting unity gain amplifiers. The input impedance of this architecture is R. The input referred noise voltage of the first inverting unity gain amplifier, which includes the noise from the opamp, input resistor, and the feedback resistor will get amplified by a factor of 2. The circuit produces a pseudo differential output. As the anti-symmetric components of the fully-differential signal traverse different paths, the delay experienced will definitely be different leading to a gain error. One clear advantage of this topology is that the swing seen by the input terminals of the opamp will be very small leading to a smaller distortion contribution from the input stage of the opamp.

2.4.2 Fully-differential amplifier

Fig. 2.9 shows a fully-differential amplifier employing a fully-differential opamp. For analysing architectures employing fully-differential opamps, we shall make the following assumption. Any fully-differential opamp will need common-mode feedback to keep the quiescent output voltages of every stage in the opamp stable. We assume ideal common-mode feedback loops in this analysis. This implies that the common-mode loop-gain is ideal with infinitely large DC gain and unity loop-gain frequency.

If the input is fully-differential (anti-symmetric), then the analysis exactly corresponds to the differential counterpart of the single-ended inverting amplifier. The key point here is that the input terminals of the opamp do not experience any signal swing. However, as shown in Fig. 2.9, to get the single-ended to differential conversion done, the amplifier is exicted by a single-ended input. The other input of the amplifier is held at a constant value (V_{CM}). With this change, the dynamics of the circuit change slightly.

It is important to note that the gain of the amplifier still remains 2 as the only difference is in the way in which the input is applied. Therefore, if v_{in} is the input, then, we will see v_{in} on the positive node of the output and $-v_{in}$ on the negative side of the output. It is now evident that the non-inverting input terminal of the opamp sees a swing that is $1/3^{rd}$ of the swing seen on the positive node of the output (v_{in}). Therefore, by the principle of virtual short, the inverting input terminal of the opamp should also see a similar swing. This can also be seen if we try to evaluate the node voltage at the inverting input terminal based on superposition and voltage division. Therefore, we can see that applying a single-ended input to a fully-differential amplifier as illustrated in Fig. 2.9 leads to a condition where the input terminals of the opamp experience a swing that is proportional to the input and the feedback factor. The opamp has to be designed to support such swings.

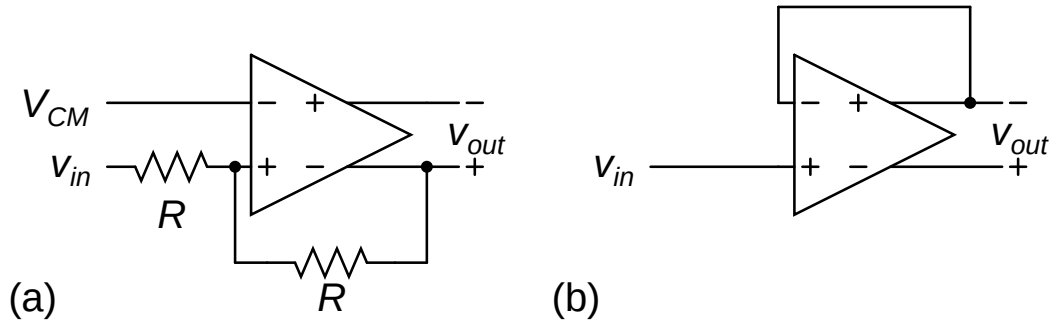


Figure 2.10: Fully-differential opamp with asymmetrical feedback.

2.4.3 Asymmetrical feedback around fully-differential opamp

Fig. 2.10 shows a fully-differential opamp used with asymmetrical feedback. The figure shows two possible configurations. The operation of the circuit in Fig. 2.10(a) can be easily predicted as follows. The reasoning provided is non causal in nature however facilitates a very easy path to the correct prediction the steady state behaviour of the circuit. As the non-inverting input terminal of the opamp does not see any swing, by the principle of virtual short, the inverting input terminal of the opampas should also not see any swing. If v_{in} is the input voltage applied to the amplifier, based on the principles of voltage division and superposition, the positive node of the output should have a voltage of $-v_{in}$. Based on the assumption of ideal common-mode feedback, it can be deduced that the negative node of the output should have a voltage of v_{in}. Therefore, it can be seen that the gain of the amplifier is 2.

The topology only uses a total resistance of $2R$ to achieve a gain of 2 as compared to the $6R$ as shown in Fig. 2.9. Therefore, for a given noise, the input resistance can be thrice as large compared to the other topology. This increases the input impedance of the amplifier. Further this also reduces the load seen by the output stage of the opamp which in turn improves the gain from that stage while simultaneously lowering its distortion contribution. The swing at the input of the opamp is ideally zero. This also helps in reducing the distortion

from the input stage of the opamp.

There are several drawbacks of this topology. The topology cannot handle fully-differential input signals. Clearly, the circuit is not symmetrical. This leads to an increase in the total harmonic distortion seen as the even order harmonics do not cancel out each other[10]. Asymmetrical structure also effectuates reduced immunity to common-mode noise—reduced PSRR and CMRR. Also, it can be proven that the noise from the common-mode feedback circuitry appears at the output. This entails a careful and low noise design of the error amplifier in the common mode feedback circuitry which eventually leads to an increased power dissipation.

Fig. 2.10(b) shows yet another topology for a fully-differential amplifier with asymmetrical feedback. The operation of the circuit can also be easily explained. As the non-inverting input terminal of the opamp sees the entire input signal swing v_{in}, by the principle of virtual short, the inverting input terminal of the opamp should also see the same swing. Because of the complete feedback as in a voltage follower, the negative output also sees the same swing. Based on the assumption of ideal common-mode feedback, it can be deduced that the positive node of the output should have a voltage of $-v_{in}$. Therefore, it can be seen that the gain of the amplifier is 2.

The topology achieves a gain of 2 without the use of any resistors at all. Therefore the opamp is the only source of noise. This will translate to a lower power dissipation in the opamp. Also, the architecture provides an extremely high input impedance.

The key disadvantage in this topology is that the opamp should support rail-to-rail input swing. This requirement effectively renders the architecture unusable in the design of low distortion parts. The problem is dealt in detail in section

[10]It is seen in simulations that the effect of degradation of linearity due to the incomplete cancellation of the even order harmonics is greater than the effect of improved linearity because of the use of larger resistors in the circuit

2.3. As with the other asymmetrical feedback topology, current topology also cannot handle fully-differential input signals, shows higher distortion levels as the even order harmonics do not cancel out each other, shows reduced PSRR and CMRR. Also, noise from the error amplifier in the common-mode feedback circuitry appears at the output.

2.4.4 Summary

The cascade of inverting unity gain amplifier and the fully-differential amplifier are more suitable for implementation compared to those involving the non-inverting configuration. This is mainly because the opamp within these architectures will not have to support a rail-to-rail swing at the input. One extra advantage of this fact is that the distortion contribution from the input stage of the opamp will also be comparatively smaller. However, the major disadvantage is the significantly smaller input impedance.

Asymmetrical feedback around a fully-differential opamp does lead to some interesting structures such as an amplifier with a gain of 2 that independent of the ratio of resistors, it does have its own disadvantages. During the discussion, it is assumed that the common-mode feedback loops are ideal. For practical purposes, the common-mode loopgain should have high enough DC gain and unity loop-gain frequency to ensure that the output common-mode remains stable even in the presence of signal. This entails higher power consumption. Asymmetry in the feedback will not allow for a perfect cancellation of the even order harmonics thereby leading to a higher output distortion. A more delicate disadvantage is that the noise and distortion from the error amplifier in the common-mode feedback loop will appear at the output. Hence we consider the cascade of inverting unity gain amplifiers and the fully-differential amplifier as the only suitable architectures for the implementation of the prototype.

2.5 Noise and gain error

The architectures described in the previous section have a finite input impedance other than that depicted in Fig. 2.10(b). Whenever a designer chooses such architectures where the input impedance of the driver is dependent on a resistor value, he faces a trade off between the total noise and gain error seen at the output. A simple explanation to this trade off is first given. An example scenario is considered and the effect of this trade off is then elucidated.

2.5.1 The trade-off

Any real input source will have a non zero source impedance associated with it. When such a source is used along with the driver, there will be a voltage division between the source impedance and the input impedance of the driver. Because of this division, only a fraction of the source voltage appears as the input to the driver. This leads to a gain error as seen from the output of the driver. As the input impedance of the driver increases, the fraction of the source voltage appearing as the input to the driver increases and therefore the gain error decreases. It is now easy to conclude that to have no gain error because of this division, ideally, the input impedance of the driver should be infinite. It is useful to reiterate here that the topologies depicted in Fig. 2.1(a), Fig. 2.1(b) and Fig. 2.10(b) provide very high input impedance although the requirement of supporting rail-to-rail input swing renders them unfeasible for implementation.

If one has to achieve high input impedance in architectures based on inverting amplifier configuration, the input resistor which controls the input impedance has to be increased to the required value. To achieve the necessary gain, the feedback resistor will also increase proportionally. With the increase in the input and feedback resistors, the total noise contribution from the driver will also

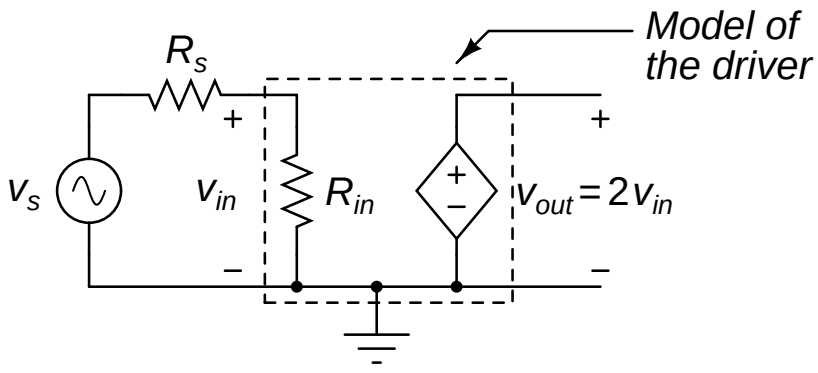


Figure 2.11: Circuit diagram illustrating the voltage division at the input.

increase proportionally. Usually, the bandwidth of operation of the driver will be fixed. Because of the fixed bandwidth and increased noise contribution, the total integrated noise at the output will also increase. If there is a limit on the total integrated noise from the driver, then effectively there will be a limit to the maximum value of the input resistor that can be used. With this limit on the input resistor, we always see a fixed gain error because of the voltage division with the source impedance. Therefore, achieving a low gain error will implicitly bring higher noise at the output and vice versa.

2.5.2 An example

In this section, the total integrated noise and the gain error for architectures depicted in Fig. 2.8 and Fig. 2.9 are evaluated and the trade off is illustrated. In this analysis, we consider the noise contribution from the input and feedback resistors only. Noise contribution from the opamp is not considered as it does not yield any extra information but adds to the complexity of the calculations. To find the total integrated noise at the output, the bandwidth of the driver is assumed to be 25 MHz[11].

For the gain error calculation, the source impedance is assumed to be 100 Ω. Further, the error introduced by the finite DC gain of the opamp is neglected.

[11] This is the specification aimed for the prototype driver.

The error due to the mismatch between the input and feedback resistors is also neglected. It will be seen later that these errors are smaller than the error due to the voltage division at the input by several orders of magnitude. Hence disregarding these errors is justified.

Cascade of inverting amplifiers

Gain error: To find the gain error of the driver, we use the circuit shown in Fig. 2.11. The driver circuitry is replaced by an equivalent model. This model has an input impedance of R_{in} and a voltage controlled voltage source of gain 2. The control voltage to this controlled source is the voltage across R_{in}. Even though the driver output is fully-differential, the output of the model is shown to be single-ended as it does not affect the analysis. v_s represents the source voltage and R_s the source impedance. We can write the following.

$$v_{in} = \left[\frac{R_{in}}{R_s + R_{in}}\right] v_s \tag{2.10}$$

Ideally,

$$v_{in} = v_s \tag{2.11}$$

Therefore, the error (e_{in}) can be calculated as

$$e_{in} = \left[1 - \frac{R_{in}}{R_s + R_{in}}\right] v_s \tag{2.12}$$

Relative to the source voltage, the error is

$$\frac{e_{in}}{v_s} = \left[\frac{R_s}{R_s + R_{in}}\right] \tag{2.13}$$

This is the gain error seen because of the voltage division occuring at the input.

Total integrated noise: To calculate the total integrated noise at the output of the driver, it is useful to first find the total input referred noise voltage of an in-

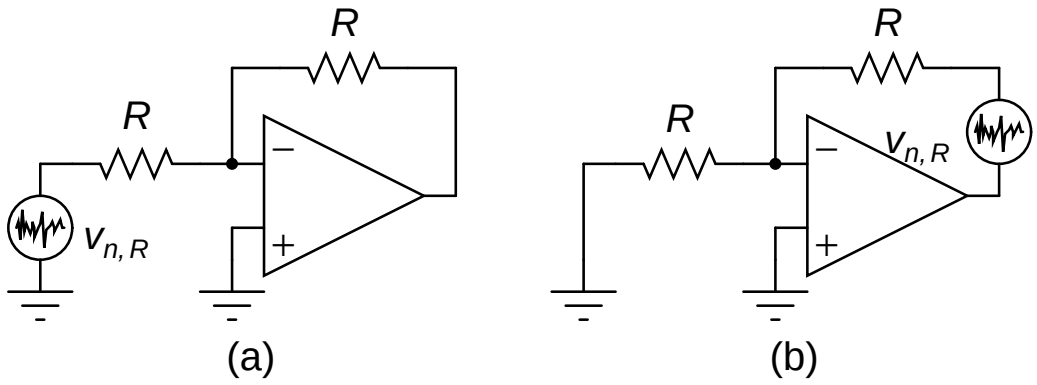


Figure 2.12: Inverting unity gain amplifier illustrating the noise source of (a) the input resistor and (b) the feedback resistor.

verting unity gain amplifier. As stated earlier, the noise from the opamp is neglected. Fig. 2.12(a) and (b) show inverting unity gain amplifier with the noise from the input and feedback resistors respectively. $v_{n,R}$ represents the noise voltage of the resistors. It should also be noted that the original input is grounded.

From Fig. 2.12(a), it is easy to see that the noise voltage associated with the input resistor directly appears at the input of the amplifier.

From Fig. 2.12(b), as the non-inverting input of the opamp is at ground, by the principle of virtual short, we can reason that the inverting input terminal of the opamp is at ground. This implies that the current through the input resistor R is zero as the potential difference across it is zero. We know that zero current flows through the input terminals of the opamp. By applying KCL at the inverting input terminal of the opamp, it can now be seen that the current through the feedback resistor should also be zero. This implies that there will be zero voltage drop across the feedback resistor. Therefore the voltage drop across the feedback branch (series combination of the resistor and its associated noise voltage source) is the same as $v_{n,R}$. It is now evident that the output of the opamp is at a voltage $v_{n,R}$. Alternatively, we say that the entire noise voltage of the feedback resistor also appears at the output of the amplifier. Since the gain

of the amplifier is unity, we can refer it as it is to the input. Therefore,

$$v_{n,in}^2 = v_{n,R}^2 + v_{n,R}^2 \tag{2.14}$$

Here $v_{n,in}$ refers to the total input referred noise voltage. As the two noise sources are uncorrelated, the two power spectral densities can be added directly. Therefore the total input referred noise voltage power spectral density ($S_{v,in}(f)$) of the unity gain amplifier is

$$S_{v_{n,in}}(f) = S_{v_{n,R}}(f) + S_{v_{n,R}}(f) \tag{2.15}$$

$$S_{v_{n,in}}(f) = 4kTR + 4kTR \tag{2.16}$$

where k is the Boltzmann's constant and T is the absolute temparature.

With this background, we can easily calculate the total integrated noise of the architecture depicted in Fig. 2.8. First let us consider the contribution of the resistors in the first unity gain amplifier alone. The input referred noise voltage spectral density is $8kTR$. The transfer function from the input to the differential output is given as follows.

$$H(f) = \frac{1}{\left(1 + \mathrm{j}\frac{f}{BW}\right)^2} + \frac{1}{\left(1 + \mathrm{j}\frac{f}{BW}\right)} \tag{2.17}$$

$$= \frac{2 + \mathrm{j}\frac{f}{BW}}{\left(1 + \mathrm{j}\frac{f}{BW}\right)^2} \tag{2.18}$$

Here, the transfer function of the unity gain amplifier, denoted by $G(f)$, is assumed as shown below. BW refers to its bandwidth in Hz.

$$G(f) = -\frac{1}{\left(1 + \mathrm{j}\frac{f}{BW}\right)} \tag{2.19}$$

The power spectral density of the noise at the output can now be calculated as follows.

$$S_{v_{n,out}}(f) = |H(f)|^2 \cdot S_{v_{n\,in}}(f) \tag{2.20}$$

$$S_{v_{n,out}}(f) = \frac{\left|2 + \mathrm{j}\frac{f}{BW}\right|^2}{\left|\left(1 + \mathrm{j}\frac{f}{BW}\right)^2\right|^2} 8kTR \tag{2.21}$$

The total mean square noise voltage at the output is given by

$$\overline{v_{n,out}^2} = \int_0^\infty S_{v_{n,out}}(f)\, df \tag{2.22}$$

$$\overline{v_{n,out}^2} = \int_0^\infty \frac{\left|2 + \mathrm{j}\frac{f}{BW}\right|^2}{\left|\left(1 + \mathrm{j}\frac{f}{BW}\right)^2\right|^2} 8kTR\, df \tag{2.23}$$

$$= 8kTR \int_0^\infty \frac{4 + \left(\frac{f}{BW}\right)^2}{\left(1 + \left(\frac{f}{BW}\right)^2\right)^2}\, df \tag{2.24}$$

$$= 8kTR \left[\int_0^\infty \frac{4}{\left(1 + \left(\frac{f}{BW}\right)^2\right)^2}\, df + \int_0^\infty \frac{\left(\frac{f}{BW}\right)^2}{\left(1 + \left(\frac{f}{BW}\right)^2\right)^2}\, df \right] \tag{2.25}$$

Substituting (f/BW) by $\tan\theta$ and changing the limits of integration, we obtain

$$= 8kTR \left[\int_0^{\frac{\pi}{2}} \frac{4 \cdot BW \sec^2\theta}{\left(1 + \tan^2\theta\right)^2}\, d\theta + \int_0^{\frac{\pi}{2}} \frac{\tan^2\theta \cdot BW \sec^2\theta}{\left(1 + \tan^2\theta\right)^2}\, d\theta \right] \tag{2.26}$$

$$= 8kTR \left[4BW \int_0^{\frac{\pi}{2}} \cos^2\theta\, d\theta + BW \int_0^{\frac{\pi}{2}} \sin^2\theta\, d\theta \right] \tag{2.27}$$

$$= 8kTR \cdot BW \left[4 \cdot \frac{\pi}{4} + \frac{\pi}{4} \right] \tag{2.28}$$

$$= 8kTR \cdot BW \cdot \left[\frac{5\pi}{4} \right] \tag{2.29}$$

The above equation gives the total mean square noise voltage at the differential output in Fig. 2.8. Note that only the contribution of the resistors—input and

feedback—present in the first unity gain amplifier in the architecture is calculated. The contribution from the resistors in the second unity gain amplifier is still not found. The power spectral density of the input referred noise voltage is $8kTR$. The relevant transfer function from the input of the amplifier to its output is denoted by $G(f)$. Therefore the power spectral density at the output is

$$S_{v_{n,\,out}}(f) = |G(f)|^2 \cdot S_{v_{n\,in}}(f) \tag{2.30}$$

$$= \left| \frac{1}{1 + \mathrm{j}\frac{f}{BW}} \right|^2 8kTR \tag{2.31}$$

Therefore,

$$\overline{v_{n,\,out}^2} = \int_0^\infty \left| \frac{1}{1 + \mathrm{j}\frac{f}{BW}} \right|^2 8kTR\, df \tag{2.32}$$

$$= 8kTR \int_0^\infty \frac{1}{1 + \left(\frac{f}{BW}\right)^2} df \tag{2.33}$$

As was done earlier, subsituting $\tan\theta$ for (f/BW) and changing the limits of integration yields,

$$= 8kTR \int_0^{\frac{\pi}{2}} \frac{BW \sec^2\theta}{1 + \tan^2\theta} d\theta \tag{2.34}$$

$$= 8kTR \cdot BW \cdot \left[\frac{\pi}{2}\right] \tag{2.35}$$

This is the mean square noise voltage seen at the output because of the resistors present in the second unity gain amplifier. From equations 2.29 and 2.35, the total noise seen at the output of the driver depicted in Fig. 2.8 is $8kTR \cdot BW \cdot (5\pi/4 + \pi/2)$.

The gain error and the total mean square noise voltage at the output is evaluated for different values of the input resistors. Table 2.2 shows the details. For this calculation, we assume that the source impedance is $100\,\Omega$.

Table 2.2: Noise and gain error variation with input resistor for driver architecture shown in Fig. 2.8

Input resistor (kΩ)	Root mean square noise (V)	Gain error (%)
10	67.45 μ	1
5	47.64 μ	2
2	30.14 μ	5
0.878	20 μ	10.22

Fully-differential amplifier

The gain error and the total integrated noise seen at the output of the driver illustrated in Fig. 2.9 are calculated here. Together with the calculations done previously, it is easy to quantitatively compare the two architectures.

Gain error: The calculation of gain error because of the finite input impedance is essentially the same as what was done earlier. The gain error is related to the input and source impedances as given below. v_s, R_s, and R_{in} denote the source voltage, source impedance and the input impedance of the driver respectively.

$$\text{error(relative to } v_s) = \frac{R_s}{R_s + R_{in}} \tag{2.36}$$

The only thing that remains to be calculated is that of the input impedance of the architecture. If the applied input was perfectly anti-symmetric, then the calculation of the input impedance is straight forward and will be the fully-differential equivalent of inverting unity gain amplifier. The input terminals of the opamp will not see any signal swing. Therefore, the input impedance is R[12]. However, as discussed earlier in section 2.4.2, with the application of a single-ended input, the dynamics of the circuit change considerably. The key point here is that the input terminals of the opamp will see a signal swing that is proportional to the input and the feedback factor. In our case, the input terminals

[12]Differentially, the input impedance will be $2R$.

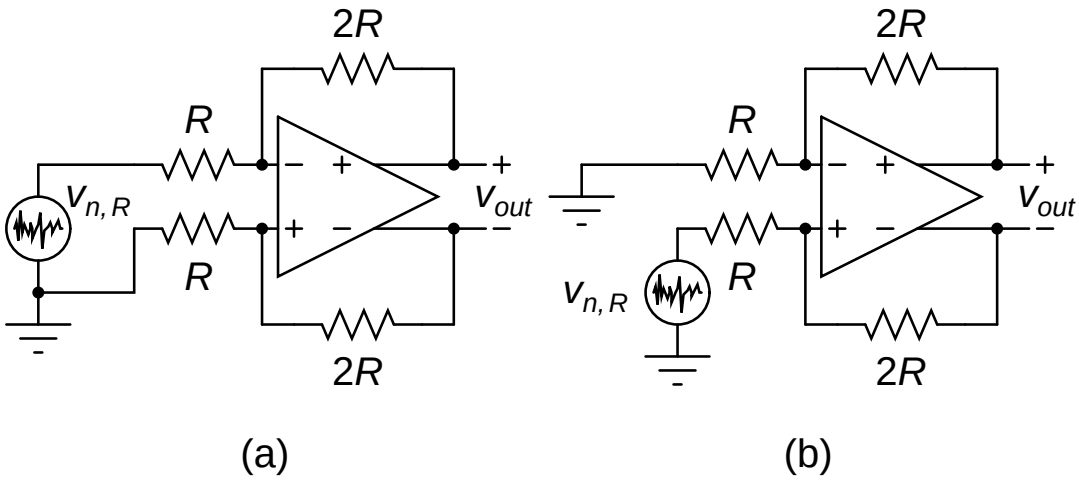


Figure 2.13: Circuit diagram illustrating the noise sources from the input resistors of a fully-differential amplifier.

of the opamp will experience a swing that is $1/3^{rd}$ the input. Therefore,

$$\text{Voltage across the input resistor} = v_{in} - \frac{v_{in}}{3} \tag{2.37}$$

$$\text{Current through the input resistor} = \frac{2v_{in}}{3R} \tag{2.38}$$

$$\text{Therefore, the effective input impedance} = \frac{3R}{2} \tag{2.39}$$

It can be seen that the effective input impedance of the fully-differential amplifier with an anti-symmetric input is smaller than if the input is not anti-symmetric. Also, the factor by which the input impedance increases is dependent to the feedback factor. Smaller the feedback factor, smaller will be the increase in the input impedance seen. This relationship between the input resistor (R) and the effective input impedance of the driver will be used in the subsequent calculation of the gain error.

Total integrated noise: As was done with the previous architecture, to find the total integrated noise at the output of the driver, we first find the total input referred noise voltage. Then, with the knowledge of the transfer function of the

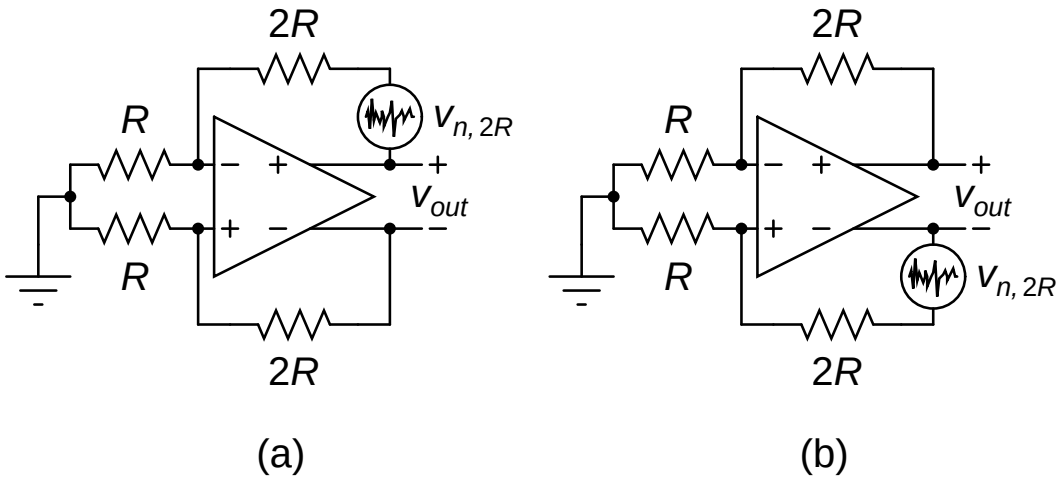


Figure 2.14: Circuit diagram illustrating the noise sources from the feedback resistors of a fully-differential amplifier.

driver, we find the total mean square noise voltage at the output. To calculate the contribution from the different noise sources to the total input referred noise voltage, the original input is grounded.

The noise voltage from the input resistor associated with the inverting terminal of the opamp appears directly at the input of the driver. Hence it is referred as is. This is illustrated in Fig. 2.13(a). Fig. 2.13(b) shows the noise voltage associated with the other input resistor. Since the original input of the driver is grounded, the noise voltage from the input resistor (associated with the non-inverting input terminal of the opamp) acts the effective input to the driver. Therefore it can be thought to have a gain of 2 to the differential output. Furthermore while refering it to the original input of the driver, an attenuation factor of 0.5 is seen. Therefore, the noise voltage from this input resistor also appears as it is when referred to the input of the driver.

The noise voltage from the feedback resistors are shown as voltage sources in series with the corresponding resistors in Fig. 2.14. The contribution from one of the feedback resistor to the total input referred noise voltage is only found out. Similar arguments can be made to find out the contribution from the other

feedback resistor. In particular, we consider the circuit is Fig. 2.14(a) for analysis here. The input to the driver is grounded. The input terminals of the opamp does not experience any swing and hence can be considered as ground for analysis purposes. This implies that no current flows through the input resistors as the voltage drop across them is zero. The input terminals of the opamp will also not carry any current. Therefore by applying KCL at the input terminals of the opamp, we can see that current through the feedback branches is zero. If we now consider the total voltage drop across the feedback branches, it will be equal to zero in the case where the resistor is shown to be noiseless and will be equal to the noise voltage $v_{n,2R}$ in the case where the resistor is shown to be noisy. Therefore the total differential noise voltage seen at the output will be equal to $v_{n,2R}$. When this is referred back to the input of the driver, the attenuation factor of 0.5 comes in and the contribution of the feedback resistor to the input referred noise voltage will be $v_{n,2R}/2$. The contribution from the other feedback resistor will exactly be the same.

$$\text{Total input referred noise voltage} = \underbrace{v_{n,R} + v_{n,R}}_{\text{input resistors}} + \underbrace{\frac{v_{n,2R}}{2} + \frac{v_{n,2R}}{2}}_{\text{feedback resistors}} \tag{2.40}$$

Since the noise sources are all uncorrelated with each other, the power spectral density of the total input referred noise voltage of the driver, denoted by $S_{v_{n,in}}$ will be the sum of the power spectral densities of each of the four contributing sources. $k,\ T,\ and R$ have their usual meaning.

$$S_{v_{n,in}} = 4kTR + 4kTR + \frac{4kT(2R)}{4} + \frac{4kT(2R)}{4} \tag{2.41}$$

$$= 12kTR \tag{2.42}$$

If BW is the closed loop bandwidth of the driver, then the overall transfer func-

tion ($H(f)$) of the driver can be written as below.

$$H(f) = \frac{2}{1 + \mathrm{j}\frac{f}{BW}} \tag{2.43}$$

The power spectral density of the noise voltage at the output of the driver can now be calculated as follows.

$$S_{v_{n,out}} = |H(f)|^2 \, S_{v_{n,in}} \tag{2.44}$$

$$= \frac{4}{1 + \left(\frac{f}{BW}\right)^2} 12kTR \tag{2.45}$$

$$\overline{v_{n,out}^2} = \int_0^\infty \frac{4}{1 + \left(\frac{f}{BW}\right)^2} 12kTR \, df \tag{2.46}$$

$$= 48kTR \int_0^\infty \frac{1}{1 + \left(\frac{f}{BW}\right)^2} \, df \tag{2.47}$$

Substituting $\tan\theta$ for (f/BW) and changing the limits of integration accordingly,

$$\overline{v_{n,out}^2} = 48kTR \int_0^{\frac{\pi}{2}} \frac{BW \sec^2\theta}{1 + \tan^2\theta} \, d\theta \tag{2.48}$$

$$= 48kTR \cdot BW \left[\frac{\pi}{2}\right] \tag{2.49}$$

The gain error and the total mean square noise voltage at the output is evaluated for different values of the input resistors. Table 2.3 shows the details. For this calculation, we assume that the source impedance is $100\,\Omega$.

Comparing Table 2.2 with Table 2.3, we can see that the fully-differential architecture provides an input impedance that is 1.5 times the input impedance provided by the cascade of inverting unity gain amplifier architecture for the same input resistor. However for the same bandwidth the total mean square

Table 2.3: Noise and gain error variation with input resistor for driver architecture shown in Fig. 2.9

Input resistor (k Ω)	Root mean square noise (V)	Gain error (%)
10	88.31 μ	0.66
5	61.80 μ	1.33
2	38.47 μ	3.33
0.128	20 μ	34.24

noise seen at the output is also larger by a factor of 12/7.

CHAPTER 3

Design of the Prototype Driver

3.1 Introduction

This chapter deals with the design of the prototype driver aimed to drive the input signal into an 18-bit 1 MS/s SAR ADC. A proprietary CMOS technology with a drawn minimum length of 0.6 μm from Texas Instruments is used. The nominal power supply voltage is 5 V. The technology provides standard and low threshold voltage flavored nMOS and pMOS devices. The standard nMOS and pMOS have a threshold voltage of 0.6 V and 0.9 V respectively. It is a triple well process-isolated nMOS transistors are also provided.

Section 3.2 tabulates the specifications aimed for the prototype driver. In order to meet these specifications, additional filtering is required to the architectures described in the previous chapter. Details of the filtering and the final architecture chosen for the implementation are presented in Section 3.3 and 3.4. Sections 3.5 and 3.6 give the schematic and layout design and the corresponding simulation results.

3.2 Specifications

The driver is aimed to drive an input signal originating from a source whose specifications are tabulated in Table 3.1. The error tolerable from the driver is as shown in Table 3.2. This includes the DC offset, noise, distortion, gain error,

[1]The architecture allows the input to be truly rail-to-rail. The limitation arrives because of the output stage.

Table 3.1: Input signal source specifications

Mode	Single-ended
Range[1]	0.1 - 0.9V_{dd}
Output impedance (max.)	100 Ω

and settling related errors that the driver can introduce into the signal chain. It should be noted here that an achievable yet rigorous specification combine is chosen for the gain error and noise. In the previous chapter, the trade-off between the gain error and noise was explained.

Table 3.2: Error specifications from the driver

Output offset voltage (3σ)	$\leq$2.5 mV
DC gain error	$\leq$5%
Noise sampled onto the ADC sampling capacitor	$\leq$40 μV
Total harmonic distortion at 10 Hz	-120 dB
Total harmonic distortion at 100 kHz	-100 dB
Settling time for a full scale input step	$\leq$ 1 μs

Table 3.3: ADC load and operating conditions

ADC load	100 pF
Voltage coefficient of the load	0.02 V^{-1}
ADC input mode	Fully differential

The specifications of the converter to be driven are as shown in Table 3.3. The ADC input circuitry is essentially a sample-and-hold circuit. This was illustrated in Chapter 1. The switch that comes in series with the input capacitor adds nonlinearity to the input signal. The nonlinearity is introduced because of the variation of the ON resistance of the switch based on the input signal. Also, the capacitors themselves will have some nonlinearity associated with them. The overall nonlinearity of this switched-capacitor load is specified as a first order voltage coefficient here. It should be noted that even though the coefficient is stated as of a first order, it leads to a second harmonic in the output. The converter is to be used in the fully-differential mode so as to obtain all its

benefits. Therefore, the driver will have to perform single-ended to differential conversion.

Table 3.4: Driver operating conditions

V_{dd}	5 ± 1 V
Temparature range	-40° to +125° C

The expected operating conditions for the driver are as specified in Table 3.4. Since the aim is to integrate the driver with the converter, both blocks running from the same supply[2] will greatly reduce the complexity of such an integrated device. We assume that the converter and the driver both run from the same power supply (= 5 V, nominally).

Several datasheets indicate that the maximum reference input to the converter is close to its nominal analog power supply. It is already mentioned that the ADC will be used in the fully-differential mode. Therefore, it is easy to see that to use the entire range of the converter effectively, the input signal should be amplified by a factor of 2 along with the single-ended to fully-differential conversion.

3.3 Additional filtering

The author wants to bring the following point to the notice of the reader. The total harmonic distortion specification of -120 dB is a very stringent one. This is borne out by the fact that there are only a handful of parts offering such linearity and hardly any literature dealing with systematic design procedures for such circuits, especially with pure CMOS technologies. It is an observation that the circuits that provide comparable distortion performance are implemented

[2]Usually, the analog and digital power supply lines of high resolution converters will be separated to reduce the switching noise from the digital supply line coupling with the critical analog circuitry. Here we refer to the analog power supply of the converter.

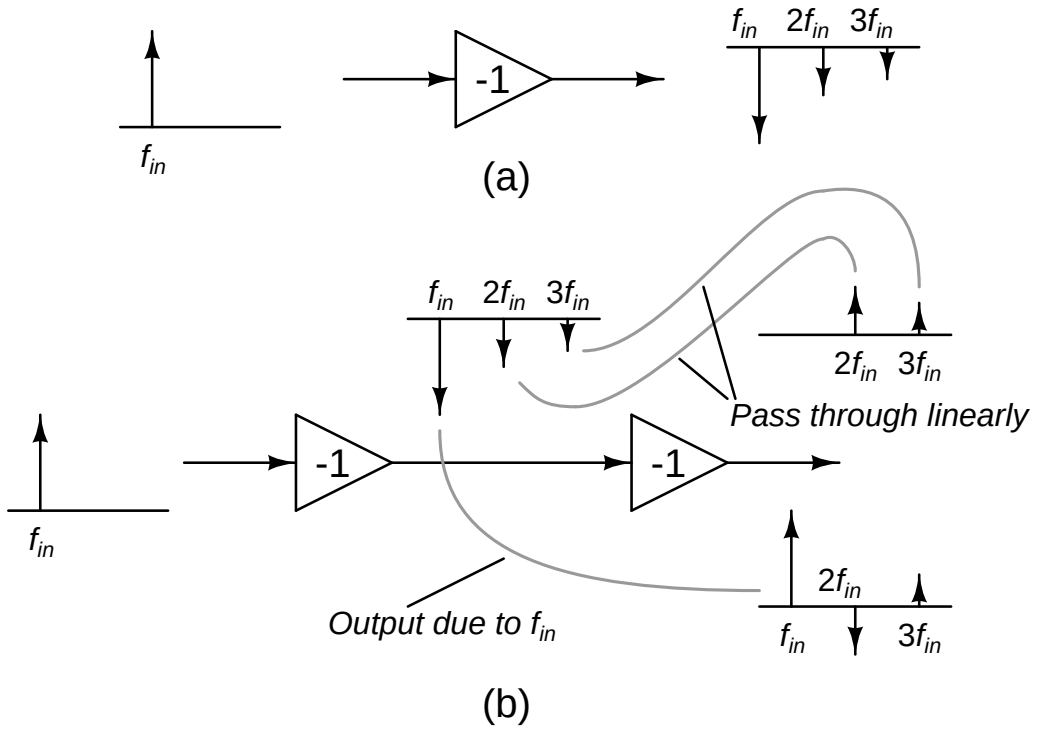


Figure 3.1: Block diagram elucidating the nonlinearity seen in (a) nonlinear unity gain amplifier and (b) cascade of identical nonlinear unity gain amplifiers.

with Bipolar processes. [16] explains the reasons why bipolar transistors lend themselves more easily to highly linear circuits than the MOS transistors.

3.3.1 Filtering at the output

To get a better look at the problem in hand and to find the acheivable level of linearity in the given process, a preliminary design of the driver is first done. The fully-differential amplifier architecture is chosen for the following reason. Among the two architectures, the fully-differential amplifier is more suitable for low distortion design. This is mainly because of the cancellation of all the even order harmonics that comes from the symmetry in the circuit.

Even though the cascade of inverting amplifiers provides a fully-differential output, the even order harmonics on the two anti-symmetric components do not cancel each other. This is explained with the help of Fig. 3.1. Fig. 3.1(a)

shows the inverting amplifier as a block of gain -1. Also shown are the spectra of the input and output assuming that a sinusoidal signal at f_{in} is applied. The output is shown to have components at f_{in}, $2f_{in}$, and $3f_{in}$[3]. Figure shows exaggerated strengths for the second and third harmonic when compared to the fundamental. This is done for the purpose of clarity. The harmonic components will be very small compared to the fundamental in a weakly nonlinear system. The direction of the arrow in the spectra gives an indication of the phase of the frequency components. The choice of the phases in the example is purely arbitrary, but without loss of generality.

Fig. 3.1(b) shows the cascade connection to two identical unity gain amplifiers. The output of the first gain block has components at $f_{in}, 2f_{in}$, and $3f_{in}$. The input to the second gain block can be thought of as the sum of three separate sinusoidal signals. The second gain block will create harmonics for each of these signals. However, the harmonics of $2f_{in}$ and $3f_{in}$ are neglected as they will be extremely small compared to the fundamental at f_{in}. Therefore, it is shown that the components at $2f_{in}$ and 3_{fin} pass through the second gain block linearly with only a change in sign because of the inverting nature of the block.

The fundamental component at the input of the second gain block will have the same strength as the original input signal. However there will be a 180° phase shift because of the inversion. This signal will create harmonics at the output that are similar in strength to the harmonics seen at the output of first stage. The phase of the second harmonic will be the same as the phase of the corresponding second harmonic at the output of the first stage. The phase of the third harmonic will be 180° away from the corresponding phase of the third harmonic at the output of the first stage. The phases associated with the harmonics at $2f_{in}$ and $3f_{in}$ are also shown. If we consider the output of the two unity gain amplifiers to be the two anti-symmetric components of a fully-differential signal, it is clear that the second order harmonics on the two anti-symmetric lines do not

[3]The assumption of weak nonlinearity.

cancel with each other. The strength of the second harmonic will be similar to the strength of the harmonic seen at the output of the first inverting gain block. The same argument can be extended to say that other even order harmonics do not get cancelled. Hence the fully-differential architecture is chosen for the preliminary design.

It is a well-known fact that in a negative feedback amplifier, the high loop-gain will suppress the distortion. Hence having a large enough DC gain will reduce the distortion at low frequencies. This implies that we have a knob to achieve the total harmonic distortion of -120 dB at 10 Hz . Obtaining high DC gain in an opamp running from 5 V supply is not difficult as techniques like cascoding and gain boosting can be used. The opamp designed for the preliminary driver has a DC gain of $\sim$100 dB. Such a large gain could be obtained from a two-stage design with the first stage being a folded cascode differential amplifier and the second stage being a common source amplifier. With a DC gain of $\sim$100 dB, the specification of -120 dB at 10 Hz is found to be achievable.

It is important to note that increasing the DC gain of the opamp while keeping the unity gain frequency constant will only push the dominant pole towards lower and lower frequencies. The loop-gain seen at frequencies higher than the dominant pole frequency will remain the same. Therefore, increasing the DC gain of the opamp will not help in suppressing the distortion at frequencies higher than the dominant pole frequency.

The closed loop bandwidth for the preliminary design is chosen as 2.5 MHz. Reasoning for this choice is given in Section 3.5. With the driver designed to have a bandwidth of 2.5 MHz, the unity loop-gain frequency will also be 2.5 MHz. We also know that the magnitude response should fall at the rate of -20 dB /decade for stability reasons. Therefore, we can calculate the loop-gain at 100 kHz to be equal to $\sim$28 dB. In the preliminary design, it is found that with such a small value of loop-gain, achieving total harmonic distortion of around

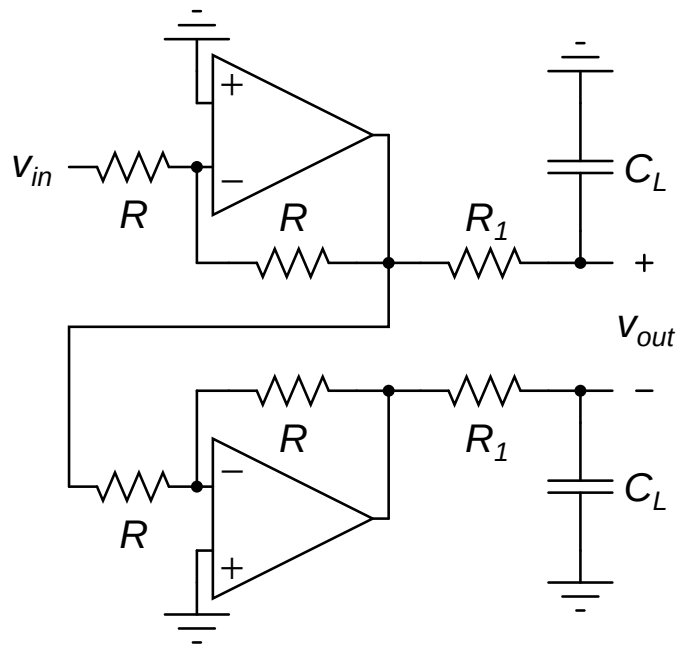


Figure 3.2: Output side filtering with the cascade of inverting amplifiers.

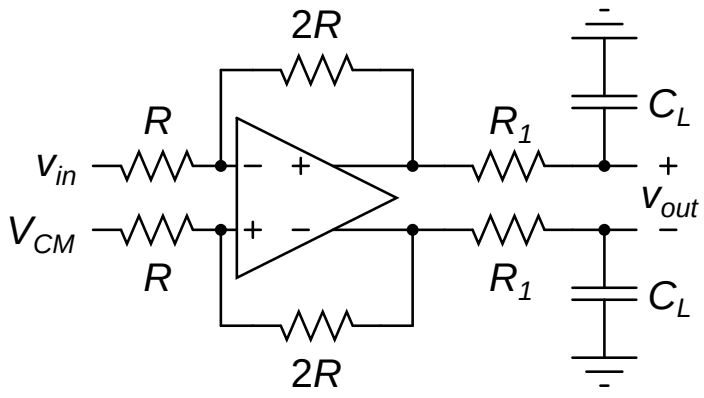


Figure 3.3: Output side filtering with the fully-differential amplifier.

-100 dB is not straightforward.

The distortion at 100 kHz can be improved by increasing the loop-gain at that frequency. The magnitude roll-off at -20 dB/decade ensures that increasing the loop-gain at 100 kHz will increase the unity loop-gain frequency proportionally.

This is essentially the same as increasing the bandwidth of the driver which requires a higher power dissipation. Along with this disadvantage, the integrated noise at the output will also increase. This means that for a specified value of total noise, if the bandwidth of the driver is increased, then the input and feedback resistance will have to decreased proportionally which in turn leads to a larger gain error.

To alleviate these problems, the architectures shown in Fig. 3.2 and 3.3 are proposed. Here R_1 and C_L form first order lowpass filters at the output. The noise from the resistors R_1 do appear at the output and this contribution should also be taken into account while designing the driver. With this arrangement, the bandwidth of the amplifier can be kept as high as required to suppress the distortion while the output side filter clamps the bandwidth of the driver as necessary. This setup provides the designer with another knob to set the high frequency distortion performance. Yet another advantage of this arrangement is that the first order filter directly loads the output stage of the opamp and thereby creating a left half plane zero. This can be effectively used to obtain a higher closed loop bandwidth. This is dealt with in detail in the next section.

Cascade of inverting amplifiers with output filtering

For the architecture depicted in Fig. 3.2, the noise contribution from the input and feedback resistors will not remain the same as what was calculated without the output first order filters. The important difference is that the output of the first inverting amplifier in the above case will not be bandlimited by the filter. This gets fed into the second inverting amplifier and the overall differential output is then bandlimited.

As before, the power spectral density of the total input referred noise voltage of the inverting amplifier is $8kTR$. The transfer function from the input of the driver to the differential output can be written as follows.

$$H(f) = \frac{2}{\left(1 + \mathrm{j}\frac{f}{BW}\right)} \tag{3.1}$$

Following the same lines as before, we can obtain the noise contribution from the input and feedback resistors of the first inverting amplifier as $8kTR \cdot 4BW(\pi/2)$. The extra factor of 4 is due to the conversion to fully-differential output. The contribution from the input and feedback resistors of the second inverting amplifier remains the same as in the case without output side filters. It is equal to $8kTR \cdot BW(\pi/2)$. Therefore, the total contribution from the input and feedback will be equal to $8kTR \cdot 5BW(\pi/2)$. Note that this is larger than that seen in the corresponding architecture without output filters.

The noise contribution from the resistors R_1 themselves have to be added. The contribution from R_1 is a standard result found in textbooks ([8], [9], [10]) and is equal to kT/C_L. Table 3.5 shows the noise contribution from all the sources except for the opamps. It also shows numerical values calculated for an overall bandwidth of 2.5 MHz. Since C_L is specified to be 100 pF, R_1 is chosen to be 636 Ω so that the bandwidth is 2.5 MHz. The value of the input resistor is chosen as 2 kΩ. It should be noted that the gain error performance remains the same as before as there are no changes to the relevant part of the circuit.

Table 3.5: Noise summary for the cascade of inverting amplifiers with output side filtering (Fig. 3.2)

Noise source	Contribution (V^2)	Calculated value (V^2)
Input and feedback resistors	$8kTR \cdot 5BW(\pi/2)$	1.3e-9
Low pass filters	$2(kT/C_L)$	82.83e-12

From the table, we can see that the opamps in total can contribute ∼213e-12 V^2 to the integrated noise at the output. This will have to include both thermal and flicker noise contributions. Alloting a 3:1 ratio[4] for thermal to flicker noise,

[4]This choice was based on the experience with the process.

the g_m requirement for the first stage of the opamp will be $\sim$20 mS. Assuming that we use two-stage opamps[5], roughly, the g_m of the second stage should also be $\sim$20 mS. Since there are two such opamps, the total transconductance required for the driver is 80 mS. Assuming a $g_m\ /I_D$ of 15 V^{-1}, the total current requirement will be $\sim$6 mA.

Fully-differential amplifier with output filtering

Fig. 3.3 illustrates the architecture. The power spectral density of the total input referred noise voltage due to the input and feedback resistors is $12kTR$. This follows similar lines as to what was shown with the fully-differential amplifier. The transfer function from the input to the differential output is also the same as in the fully differntial amplifier case. Therefore the total noise contribution from the input and feedback resistor remains the same. It is given by $12kTR \cdot 4BW(\pi/2)$.

The only difference is that in the case of the fully-differential amplifier, the unity loop-gain frequency of the opamp along with the relevant feedback factor decides the overall bandwidth of the driver, while in this case the output filters decide the bandwidth. The noise contribution of R_1 is straightforward. It is also clear that the gain error of the driver will not change because of the addition of these lowpass filters.

The input resistor R is chosen as 2 kΩ, C_L is specified as 100 pF, and the closed loop bandwidth of the driver (BW) is 2.5 MHz. Therefore R_1 is chosen to be 636 Ω. These values are used to find contribution from various sources. The summary is presented in Table 3.6.

From the above summary, it is evident that the total contribution from the input and feedback resistors and the two lowpass filters itself exceeds the specification. Hence, the above architecture will not be a good choice for the implemen-

[5] Atleast two-stages are required for the necessary swing.

Table 3.6: Noise summary of the fully-differential amplifier with output side filtering

Noise source	Contribution (V^2)	Calculated value (V^2)
Input and feedback resistors	$12kTR \cdot 4BW(\pi/2)$	1.56e-9
Low pass filters	$2(kT/C_L)$	82.83e-12

tation of the prototype.

3.3.2 Filtering the noise from input and feedback resistors

The previous section highlights the advantages of the filters at the output of the driver. The total noise at the output and the gain error is found out for typical values of the components for both the inverting amplifier based configurations. It is seen that the for a 2 kΩ input resistor (R), the fully-differential amplifier architecture is a very bad choice for implementation as the noise from the input, feedback, and the filter resistors exceed the specification. The cascade of two inverting amplifiers is a better option as the total noise from the resistors does not exceed the specification leaving some room for the opamp. A rough calculation yields that nearly 6 mA current is required for the implementation of such a driver. A key point to be noted here is that the fully-differential amplifier gives a lower gain error with a 2 kΩ input resistor compared to the cascade of inverting amplifiers.

One way of reducing the power consumption in the previously discussed architectures is by reducing the noise contribution from any of the sources. The contribution from the output lowpass filter can be reduced only by increasing the load capacitor deliberately which will entail extra power consumption. Therefore it is not considered as a solution at this point.

Reducing noise contribution from any of the input resistor, feedback resistor or the opamp will allow extra margin for the opamp. That is to say that the

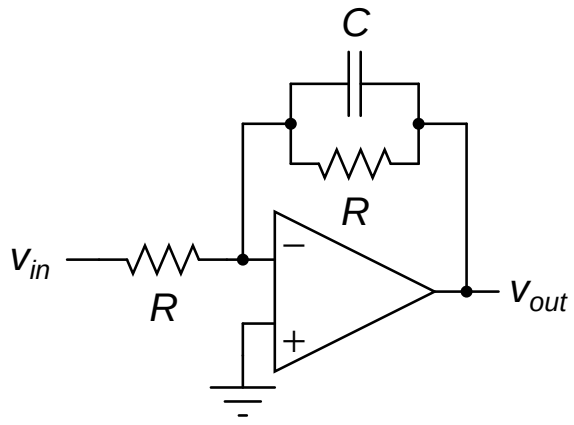


Figure 3.4: Filtering in an inverting unity gain amplifier.

opamp can contribute more noise at the output and this directly reduces the power consumption of the opamp. A more subtle advantage is that with lower current levels in the opamp, choosing transistors to have a small overdrive voltage is easy. [17] demonstrates the fact that if a transistor is biased such that the drain-source voltage is greater than their overdrive voltage ($V_{DS} > V_{DSAT}$) the distortion contribution from the transistor is small. So, with smaller current in the opamp, it is easier to design the opamp for low distortion. In the following paragraphs, a scheme that filters noise from the above mentioned sources is considered.

The filtering scheme is explained with an inverting amplifier as illustrated in Fig. 3.4. The explanation can be easily extended to the fully-differential amplifier. The figure shows a filtering capacitor placed in parallel to the feedback resistor. The effect of this capacitor on the noise from each of the noise sources is considered separately.

First, let us consider the noise from the input resistor alone. The noise source is represented as an ideal voltage source $v_{n,R}$. The original input is shorted as usual. This is shown in Fig. 3.5. Since the non-inverting input terminal of the

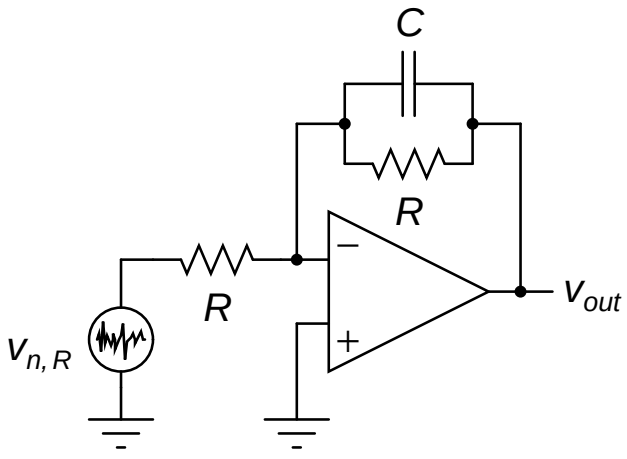


Figure 3.5: Filtering of the input resistor noise in an inverting unity gain amplifier.

opamp is at ground, we can assume that the inverting input terminal of the opamp to be also at ground. This is based on the assumption of virtual short. If the inverting input terminal of the opamp is at ground potential, then there is a current flowing through the input resistor R. The value of this current is $v_{n,R}/R$. Since no current flows through the input terminal of the opamp, all this current has to flow through the feedback path which is a parallel combination of the feedback resistor R and the filtering capacitor C. The noise voltage that appears at the output will be equal to the total voltage drop across the feedback path. Because of the filtering capacitor, the impedance of the feedback path decreases with frequency. This implies that the noise voltage seen at the output will decrease with the frequency. This is how the noise from the input resistor gets filtered. It should be noted that the filteing is of first order and the associated bandwidth is only controlled by the resistor and the capacitor in the feedback path.

Let us now consider the noise from the feedback resistor alone. Fig. 3.6 shows the circuit diagram where the noise voltage from the feedback resistor is shown. Based on the assumption of virtual short, and the fact that the non-inverting

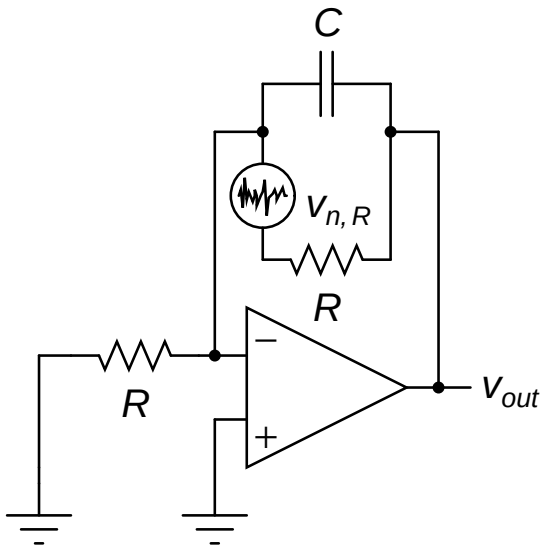


Figure 3.6: Filtering of the feedback resistor noise in an inverting unity gain amplifier.

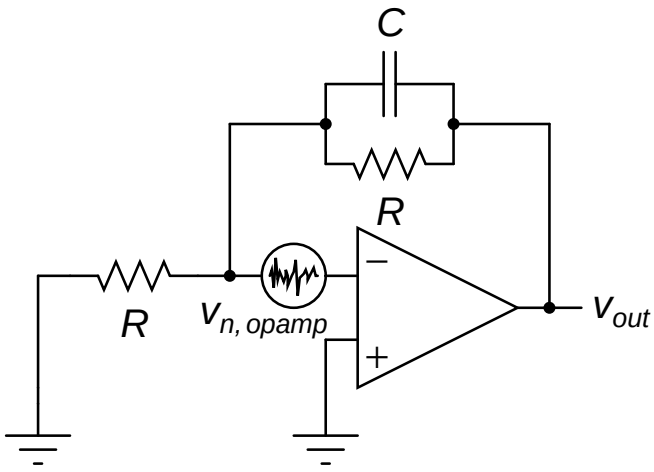


Figure 3.7: Filtering of the opamp noise in an inverting unity gain amplifier.

input terminal of the opamp is grounded we can say that the inverting input terminal is also at ground. It can now be seen clearly that the noise at the output is the lowpass filtered version of the noise of the resistor. It is interesting to note that again the feedback path resistor and capacitor are involved in the filtering process. The input and feedback resistor noise gets filtered by essentially the same filter.

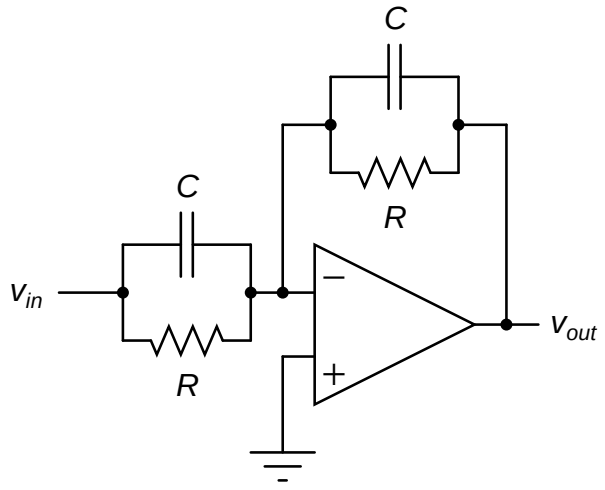


Figure 3.8: Alternative technique for noise filtering of noise in an inverting unity gain amplifier.

Fig. 3.7 shows the input referred noise voltage of the opamp as an ideal voltage source. Again, based on the assumption of virtual short the inverting input terminal of the opamp will be at ground. However the summing node will not be at the ground potential because of the presence of the noise source. The summing node will be at a potential of $v_{n,opamp}$. This implies that a proportional current flows through the input resistor. Applying KCL at the summing node and from the assumption that the input terminals of the opamp do not carry any current, it can be infered that all the current flowing through the input resistor will have to pass through the feedback branch. With this the voltage drop seen across the feedback branch will decrease with an increase in the frequency. It should be noted that the total noise voltage at the output will be equal to the sum of the total input referred noise voltage of the opamp and the voltage drop seen across the feedback path[6]. Therefore only a part of the total noise voltage at the output will be filtered. However the interesting point is to see that again the feedback path resistor and capacitor form the filtering path.

[6]Another way to analyse this is to refer the total input referred noise voltage to the non-inverting input terminal and use the overall transfer function to evaluat the final output. However the author feels that this is not as intuitive as the other method.

To summarize, the effect of having a capacitor in parallel with the feedback resistor is that the noise from the input resistor, feedback resistor and the opamp will get filtered. The bandwidth of this filter will be dependent only on the resistor and the capacitor in the feedback path. The disadvantage of this sort of filtering is that the overall transfer function from the input to the output will also be a lowpass transfer function. This can be easily seen by replacing the noise source of the input resistor in Fig. 3.5 with the actual input. Because of this lowpass transfer function, the response of the amplifier to step inputs will be slow if we choose an aggressive noise filtering option

Fortunately, the solution to overcome this problem is simple and can be conceived very easily. The problem with the arrangement in Fig. 3.4 can be alternatively viewed as follows. The input impedance of the amplifier remains constant with frequency as it is dependent only on the resistor R. However the impedance in the feedback path is frequency dependent because of the presence of the capacitor. Therefore the gain of the circuit, which is dependent on the ratio of the two impedances will also be frequency dependent. To remove this frequency dependence of the gain, one option is to introduce frequency dependence in the input impedance also. Further the dependence should be similar to the feedback impedance. This can be easily achieved by adding a suitable capacitor in parallel to the input resistor. This arrangement is shown in Fig. 3.8.

With this change in the filtering scheme, the contribution from each of the sources is investigated again with the help of Fig. 3.9. First we consider the noise from the input resistor. The relevant circuit diagram is Fig. 3.9(a). The summing node will be at ground potential as per the principle of virtual short. The voltage across the capacitor in the input path is zero and hence no current flows through it. The noise voltage $v_{n,R}$ appears directly across the resistor in the input path and hence a current $v_{n,R}/R$ will flow through it. All of this current will flow through the feedback path as the inverting input terminal of

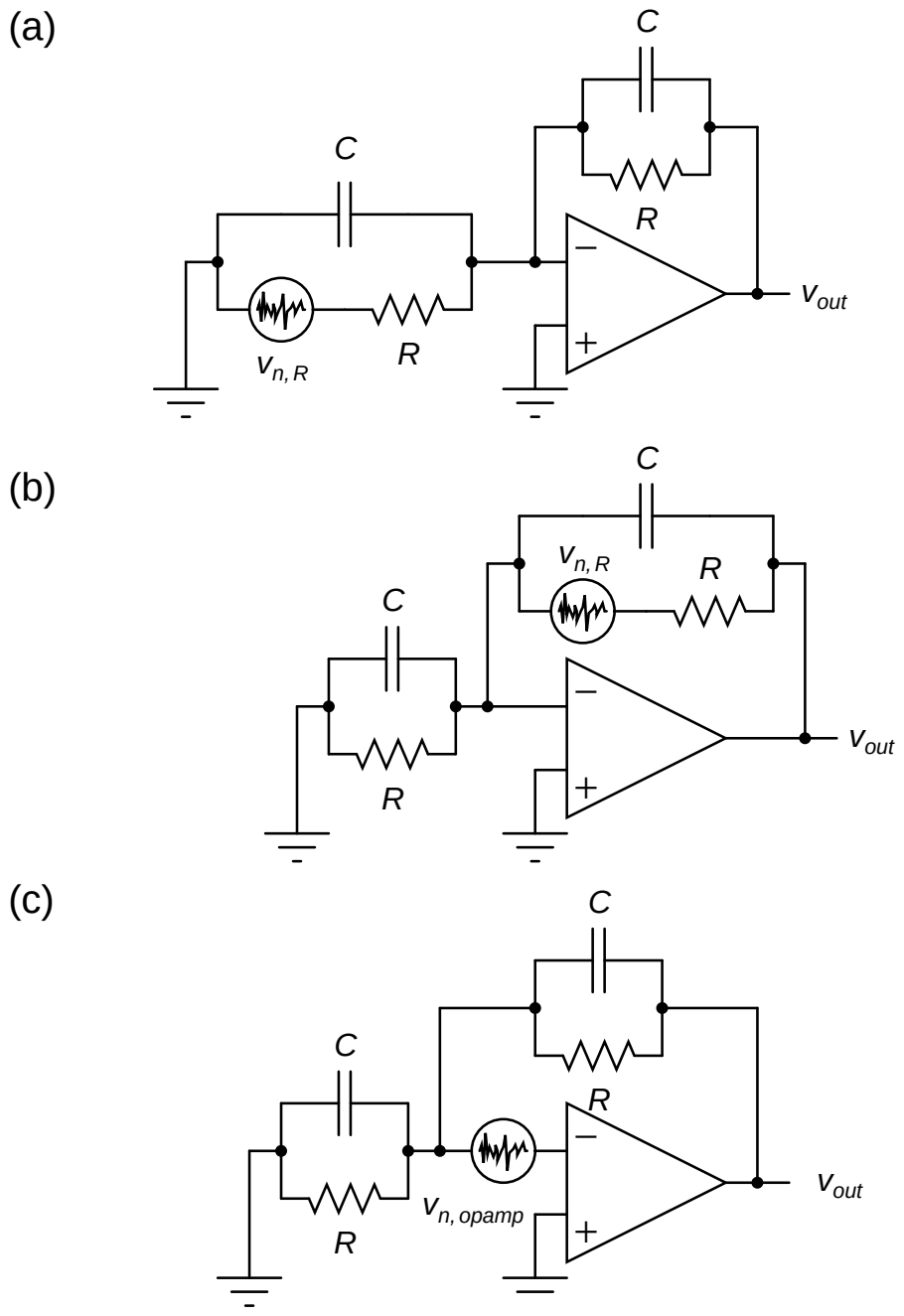


Figure 3.9: Circuit diagram to evaluate the contribution from (a) the input resistor (b) feedback resistor and (c) the opamp in the architecture depicted in Fig. 3.8

the opamp does not support any current. The impedance of the feedback path decreases with frequency and so does the voltage drop across it and thereby filtering the noise. Therefore the presence of the capacitor in the input path does not alter the noise filtering as far as the input resistor is concerned.

We now consider the noise from the feedback resistor. See Fig. 3.9(b) for reference. The virtual short principle tells us that the summing node will be at ground potential. This means that the input path does not carry any current. No current flows through the input terminals of the opamp. Therefore effectively we see a lowpass filtered version of the noise voltage $v_{n,R}$ at the output. The presence of the input path capacitor does not affect the filtering of noise from the feedback resistor either.

The noise from the opamp is shown as an ideal voltage source referred to the inverting input terminal in Fig. 3.9(c). Based on the principle of virtual short, the two input terminals of the opamp will be at ground potential. Because of this, the summing node will see a potential equal to the noise voltage $v_{n,opamp}$. Therefore the input path will carry a current that is equal to $v_{n,opamp}/Z_{in}$. Here, Z_{in} represents the impedance due to the parallel combination of the resistor R and the capacitor C in the input path. This current will have to flow through the feedback path. Since the frequency dependence of the input and the feedback impedances are the same, the voltage drop across the feedback path will also be equal to $v_{n,opamp}$. Therefore, we see $2v_{n,opamp}$ at the output. Therefore the addition of the capacitor in the input path will not allow for the filtering of the noise from the opamp. This is a clear disadvantage of this scheme. The improved step response comes at the cost of higher noise contribution from the opamp when compared to the architecture in Fig. 3.8. Yet another disadvantage of this arrangement is the fact that the input impedance is dependent on the frequency. At higher frequencies, the input impedance will be small and will lead to gain error as described in the previous chapter.

3.4 Final architectures

This section presents the summary of the evolution of the architectures. The final architectures are then presented. It is then followed by a detailed noise analysis and based on the results of this analysis and the choice of the architecture for the implementation of the prototype is justified.

The cascade of inverting amplifiers and the fully-differential amplifier are candidate topologies for low distortion drivers. If they are used as it is, acheiving low distortion and noise simultaneously will be very hard. This is because, to achieve low levels of distortion at high frequencies we need copious amount of loop-gain at those frequencies. Stability concerns ensure that to obtain large loop-gain at higher frequencies the bandwidth of the driver is proportionally large. A large bandwidth translates to larger noise at the output. To mitigate this problem, output side filtering is introduced. This helps one to have low distortion because of the higher loop-gain and low noise because of the bandlimiting offered by the filters.

Further reducing the noise contribution from the input and feedback resistors and the opamp will help in reducing the overall power dissipation. To this end adding a capacitor in parallel to the resistor in the feedback will filter out noise from the input resistor, feedback resistor as well as the opamp. However, the input will also be filtered. This is fatal for step like inputs as the response can be very slow based on the lowpass transfer function. Having a suitable capacitor in the input path will help to solve this problem as the gain is again made independent of frequency. With this arrangement, the input will not see a lowpass transfer function to the output. Along with the input, the input referred noise of the opamp will also not get filtered. Therefore, only the input and feedback resistor noise will be filtered.

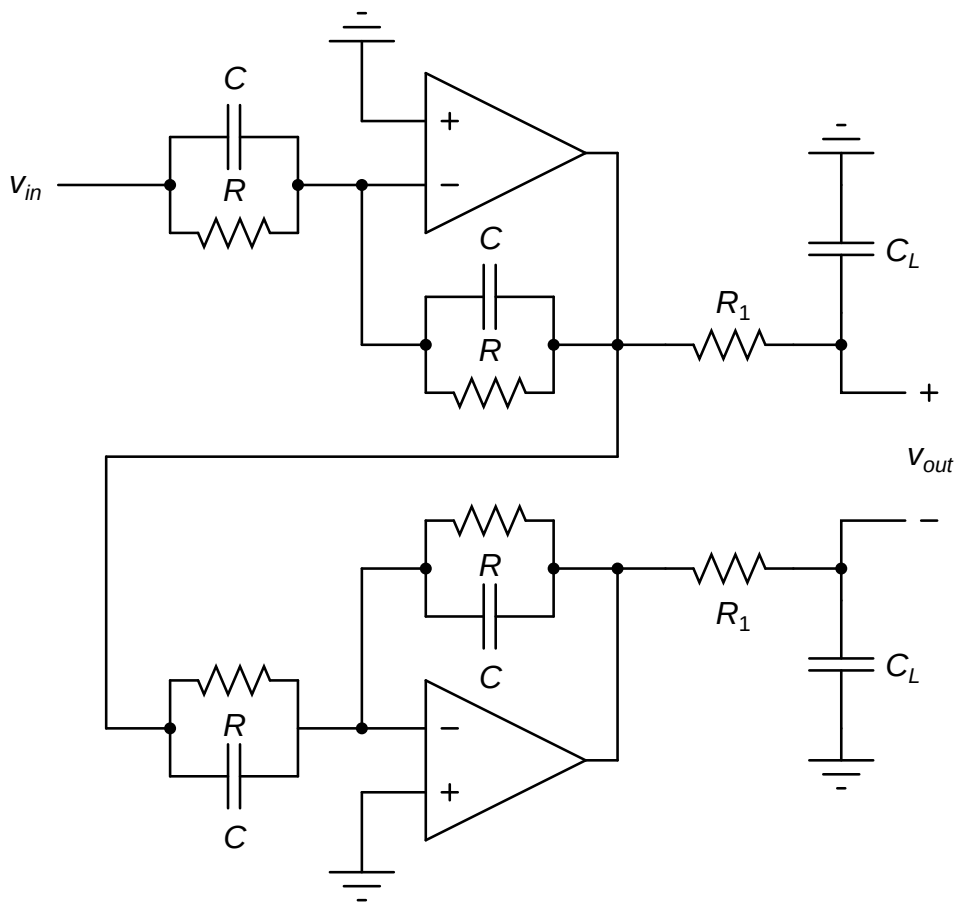


Figure 3.10: Circuit diagram of the cascade of inverting amplifiers with filtering.

3.4.1 Cascade of inverting amplifiers with filtering

Fig. 3.10 shows the architecture with filtering. To keep things consistent with other parts of the dissertation, we again show the single-ended to differential converter with a gain of 2.

The actual bandwidth of the driver will be set by the first order filter created by the series combination of R_1 and C_L. The closed loop bandwidth of each of the individual amplifiers will be kept as high as required to supress the distortion. It can now be seen that the input and the feedback resistors' noise will be first filtered by the RC filter formed in the feedback branch. Further, it will be filtered even more at the output side filter (R_1C_L). In order to obtain meaningful filtering with each of them, the time constants associated should be comparable

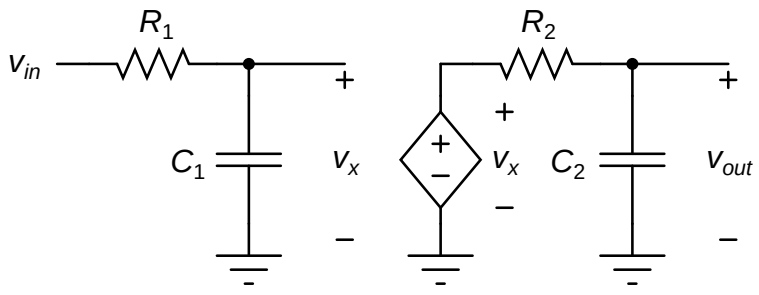


Figure 3.11: Cascade of two RC filters without loading.

to each other. If this is not the case, then the net effect will be almost the same as having only one filter that has the largest time constant. Therefore by design, we have to ensure that these time constants are comparable to each other.

Cascade of two *RC* sections

To find the contribution of the noise from the input and feedback resistors, we will have to take into account the filtering in both the places. One important observation that eases the mathematical calculation is that the net filtering in the architecture is similar to what will be achieved with two independent first order filters in cascade. By independent, we imply that there is no loading or interaction between the two stages. This is illustrated in Fig. 3.11 where an ideal voltage controlled voltage source with unity gain separates the two stages and prevents loading between them.

We first analyse the cascade of two *RC* sections without loading. Then, the results can be used to calculate the noise contribution from input and feedback resistors easily. The same results will be used even in the analysis of fully-differential amplifier architecture. The overall transfer function can be written as follows.

$$H(f) = \frac{v_{out}(f)}{v_{in}(f)} = \frac{1}{1 + \mathrm{j}2\pi f C_1 R_1} \cdot \frac{1}{1 + \mathrm{j}2\pi f C_2 R_2} \tag{3.2}$$

$$|H(f)|^2 = \left| \frac{v_{out}(f)}{v_{in}(f)} \right|^2 = \frac{1}{1 + 4\pi^2 f^2 {C_1}^2 {R_1}^2} \cdot \frac{1}{1 + 4\pi^2 f^2 {C_2}^2 {R_2}^2} \tag{3.3}$$

We calculate the noise contribution from the resistor R_1 to the output of the filter. The power spectral density of the input referred noise voltage can be written as

$$S_{v,in}(f) = 4kTR_1 \tag{3.4}$$

where k and T have their usual meaning. The power spectral at the output can be written as follows.

$$S_{v,out}(f) = 4kTR_1 \cdot |H(f)|^2 \tag{3.5}$$

The mean square noise voltage can be calculated easily as shown below.

$$\overline{{v_{out}}^2} = \int_0^\infty S_{v,out}(f)\, df \tag{3.6}$$

$$\overline{{v_{out}}^2} = \int_0^\infty \frac{4kTR_1}{(1 + 4\pi^2 f^2 {C_1}^2 {R_1}^2) \cdot (1 + 4\pi^2 f^2 {C_2}^2 {R_2}^2)}\, df \tag{3.7}$$

Substituting $f = (\tan\theta / 2\pi R_1 C_1)$ and changing the limits of integration, we obtain the following.

$$\overline{{v_{out}}^2} = \frac{4kTR_1}{2\pi R_1 C_1} \int_0^{\frac{\pi}{2}} \frac{1}{1 + \frac{{C_2}^2 {R_2}^2}{{C_1}^2 {R_1}^2} \cdot \tan^2\theta}\, d\theta \tag{3.8}$$

To solve this integral, we can consider $a = \frac{R_2 C_2}{R_1 C_1}$. The equation is rewritten as below.

$$\int_0^{\frac{\pi}{2}} \frac{1}{1 + \frac{{C_2}^2 {R_2}^2}{{C_1}^2 {R_1}^2} \cdot \tan^2\theta} d\theta = \int_0^{\frac{\pi}{2}} \frac{1}{1 + a^2 \cdot \tan^2\theta}\, d\theta \tag{3.9}$$

Substituting $x = a \cdot \tan\theta$ and suitably changing the limits of integration yields

the following.

$$\int_0^{\frac{\pi}{2}} \frac{1}{1+a^2 \cdot tan^2\theta}\, d\theta = a \int_0^{\infty} \frac{1}{1+x^2} \cdot \frac{1}{a^2+x^2}\, dx \tag{3.10}$$

Resolving this into partial fractions, we obtain the following.

$$a \int_0^{\infty} \frac{1}{1+x^2} \cdot \frac{1}{a^2+x^2}\, dx = \frac{a}{a^2-1} \left[\int_0^{\infty} \frac{1}{1+x^2}\, dx - \int_0^{\infty} \frac{1}{a^2+x^2}\, dx \right] \tag{3.11}$$

$$= \frac{a}{a^2-1} \left[\tan^{-1} x \Big|_0^{\infty} - \frac{1}{a} \tan^{-1} \left(\frac{x}{a} \right) \Big|_0^{\infty} \right] \tag{3.12}$$

$$= \frac{1}{a+1} \cdot \frac{\pi}{2} \tag{3.13}$$

$$= \left[\frac{R_1 C_1}{R_1 C_1 + R_2 C_2} \right] \frac{\pi}{2} \tag{3.14}$$

Therfore,

$$\int_0^{\infty} \frac{1}{(1+4\pi^2 f^2 {C_1}^2 {R_1}^2) \cdot (1+4\pi^2 f^2 {C_2}^2 {R_2}^2)}\, df = \frac{1}{4} \left[\frac{R_1 C_1}{R_1 C_1 + R_2 C_2} \right] \tag{3.15}$$

Substituting this in the original equation,

$$\overline{{v_{out}}^2} = \frac{kT}{C_1} \left[\frac{R_1 C_1}{R_2 C_2 + R_1 C_1} \right] \tag{3.16}$$

This concludes the analysis of the cascade of two RC sections with no loading between them. The result shown in eqn. 3.16 will be used in the noise analysis of the architecture.

Noise analysis

First, we find the contribution of the input and feedback resistor of the first inverting amplifier to the output. A qualitative explanation of the circuit that aids the analysis is given as follows. The noise voltage from both input and

feedback resistors will first get filtered by the capacitor in the feedback branch of the first inverting amplifier. This filtered version of noise passes through the other inverting amplifier and appears at its output as it is with an inversion. Therefore, we see a gain of 2.

Note that the use of output side filters decouple the noise and distortion performance of the driver. The decoupling is achieved as follows. By having a larger bandwidth for the closed loop amplifier (larger loop-gain), we obtain lower distortion at the output but only with higher noise. The output side *RC* filter will then limit the overall bandwidth and reduce the noise seen at the final output. Since the *RC* filter is made only out of passive circuit elements, its addition will not degrade the linearity at the final output. It is not unreasonable to assume that the bandwidth of the inverting amplifier to be large when compared to the bandwidth of the filter[7]. Further, it was mentioned in the previous paragraphs that the bandwidth of the two *RC* sections should be comparable to each other to achieve the advantage of additional filtering. Therefore, the bandwidth of the filter in the feedback branch will also be smaller than the bandwidth of the inverting amplifier. Therefore the noise that appears at the output of the first inverting amplifier will appear as it is at the output of the second inverting amplifier but for an inversion.

The noise at the output of both of the inverting amplifiers will then pass through the output filters. Therefore the overall mechanism can be thought of as a cascade of *RC* section corresponding to the feedback branch filtering, ideal gain block with a gain of 2 corresponding to the cascade of inverting amplifiers, and another *RC* section corresponding to the output filter. Therefore the overall transfer function can be written as follows.

$$H(f) = \frac{2}{1 + \mathrm{j}2\pi f C R} \cdot \frac{1}{1 + \mathrm{j}2\pi f C_L R_1} \tag{3.17}$$

[7] In the actual design, the amplifier bandwidth is nearly 10 times the bandwidth of the output filter

The power spectral density of the total input referred noise voltage is as given below. The expression for this is presented in the previous chapter.

$$S_{v,in}(f) = 8kTR \tag{3.18}$$

Following similar lines to that shown in the analysis of the cascade of two RC sections, we obtain the following.

$$\overline{v_{out}{}^2} = 8kTR \cdot 4 \cdot \frac{1}{2\pi RC}\left[\frac{RC}{RC + R_1C_L}\right]\frac{\pi}{2} \tag{3.19}$$

The contribution from the resistors in the second inverting amplifier is found out. The only difference when compared to the calculation of the contribution from the resistors in the first inverting amplifier is that the noise voltage does not encounter a gain of 2. However it sees the two filters as expected. Therefore, the only change in eqn. 3.19 is that the factor of 4 will be reduced to 1. Therefore the contribution is

$$\overline{v_{out}{}^2} = 8kTR \cdot 1 \cdot \frac{1}{2\pi RC}\left[\frac{RC}{RC + R_1C_L}\right]\frac{\pi}{2} \tag{3.20}$$

The noise contribution from the two output filters can be calculated easily. The noise from the two resistors that appear in the filter on each of the antisymmetric paths will be uncorrelated and will get summed in powers. Therefore,

$$\overline{v_{out}{}^2} = \frac{2kT}{C_L} \tag{3.21}$$

3.4.2 Fully-differential amplifier with filtering

The fully-differential amplifier with filtering is as shown in Fig. 3.12. The amplifier is configured as a single-ended to differential converter with a gain of

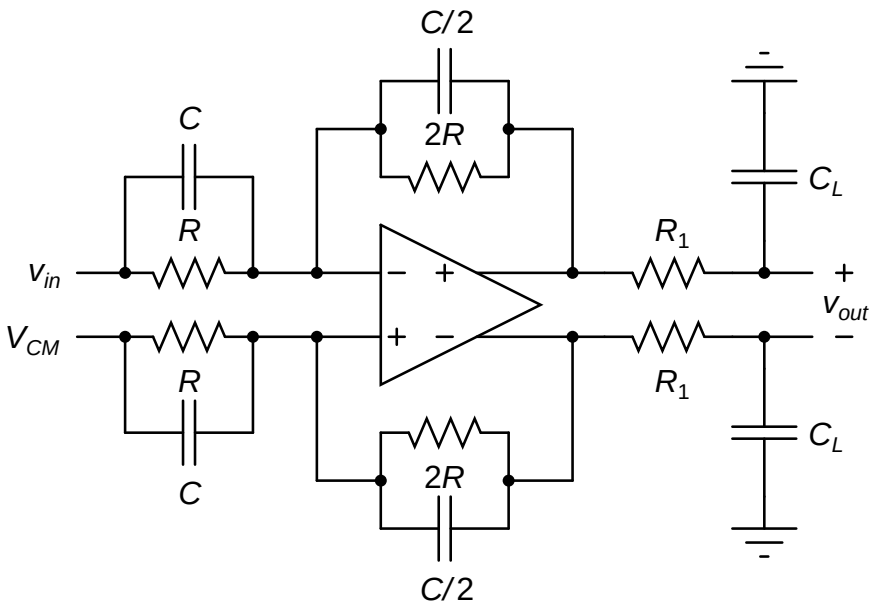


Figure 3.12: Circuit diagram of the fully-differential amplifier with filtering.

2. The impedances in the feedback network are so chosen that we obtain the required gain independent of the input frequency.

Noise analysis

The analysis of noise is very similar to the one that was carried out for the case of cascade of inverting amplifiers. In that topology, we calculate the contribution from the resistors of in each of the inverting amplifiers separately. With the fully-differential amplifier, as there is only one gain stage, the contribution of the resistors in the amplifier is found out in a single step.

The overall transfer function from the input to the output can be written as follows. This is based on the assumption that the closed loop amplifier has a bandwidth that is larger than the bandwidth of the filters employed for noise filtering.

$$H(f) = \frac{2}{1 + \mathrm{j}2\pi f C R} \cdot \frac{1}{1 + \mathrm{j}2\pi f C_L R_1} \tag{3.22}$$

The power spectral density of the total input referred noise voltage is as shown below. The proof is presented in the previous chapter.

$$S_{v,in}(f) = 12kTR \tag{3.23}$$

Based on the results obtained (eqn. 3.16), we can easily calculate the noise at the output to be

$$\overline{v_{out}{}^2} = 12kTR \cdot 4 \cdot \frac{1}{2\pi RC}\left[\frac{RC}{RC + R_1C_L}\right]\frac{\pi}{2} \tag{3.24}$$

The contribution from the output filters is the same as it is for the cascade of inverting amplifier case and is reproduced here for the sake of easy reference.

$$\overline{v_{out}{}^2} = \frac{2kT}{C_L} \tag{3.25}$$

3.4.3 Comparison

In this section, the two architectures are compared for their performance. For the comparison, the following values of $R = 2\,\text{k}\Omega$, $C = 20\,\text{pF}$, $R_1 = 636\,\Omega$, and $C_L = 100\,\text{pF}$ are used. The load C_L comes from the specification. The overall bandwidth required is shown to be equal to 2.5 MHz . Therefore R_1 is set to $636\,\Omega$. R is chosen as $2\,\text{k}\Omega$ based on the gain error specfication. $C = 20\,\text{pF}$ gives a time constant that is close to that of the output filter. This is necessary to obtain useful filtering from both the filters.

Opamp noise

The results obtained in the previous sections for the noise contribution from various sources are used to calculate the respective numerical values. Table 3.7 gives the details for component values as chosen in the above paragraph. With this we get an idea for the available room for the opamp noise. With this, we

can obtain the required g_m for opamps in the two archiectures. This allows us to compare them with respect to their total power consumption.

Table 3.7: Noise contributions from different sources of the two architectures

	Cascade arch.	Fully diff. arch.
Input and feedback resistors (V^2)	800e-12	960e-12
Lowpass filters (V^2)	84e-12	84e-12
Allowable opamp noise (V^2)	716e-12	556e-12

From the table, it is clear that the amount of noise contributed by the resistors is lesser in the case of the cascade of inverting amplifiers architecture.

Opamp noise: Cascade of inverting amplifiers

We first consider the case of cascade of inverting amplifiers. From the analysis in previous subsection, in a unity gain inverting amplifier, it is seen that the input referred noise voltage of the opamp appears at the output with a gain of 2. Since the overall gain is unity, we can effectively refer it as it is to the input of the inverting amplifier.

First we shall calculate the noise contribution from the first opamp. The total input referred noise voltage of the opamp when referred to the input of the driver will see a gain of 2. From the input of the driver to the antisymmetric output as seen at the outputs of the inverting amplifiers will further see a gain of 2. Note that the feedback branch will not filter out any of the noise because of the frequency independent gain. However, the output side filters will filter the noise. The exact calculation should involve the effect of the finite bandwidth of the inverting amplifiers. This is neglected here for the sake of easy calculation. The assumption is reasonable as the bandwidth of the inverting amplifiers is assumed to be larger than the bandwidth of the output filters.

Let us assume that the power spectral density of the total input referred noise voltage of the opamp is denoted by $S_{v_{n,opamp}}(f)$. Then the power spectral density

of the noise voltage when it is referred to the input of the driver, denoted by $S_{v_{n,in}}(f)$, is given as follows.

$$S_{v_{n,in}}(f) = 4S_{v_{n,opamp}}(f) \tag{3.26}$$

Because of the single-ended to differential conversion, we see a gain of 2. This is followed by the output filtering. Therefore the transfer function from the input of the driver to its output can be written equivalently as below. BW refers to the bandwidth of the output filter in Hz .

$$H(f) = \frac{2}{1 + \mathrm{j}\frac{f}{BW}} \tag{3.27}$$

The calculation of the total integrated noise at the output is as shown below.

$$\overline{v_{out}{}^2} = \int_0^\infty |H(f)|^2 \cdot S_{v_{n,in}}(f)\, df \tag{3.28}$$

$$\overline{v_{out}{}^2} = S_{v_{n,in}}(f) \int_0^\infty \frac{4}{1 + \frac{f^2}{BW^2}}\, df \tag{3.29}$$

As usual, substituting $f = \tan\theta / BW$, and chaning the limits of integration, we obtain the following

$$\overline{v_{out}{}^2} = S_{v_{n,in}}(f) \cdot 4 \int_0^{\frac{\pi}{2}} \frac{BW \sec^2\theta}{1 + \tan^2\theta}\, d\theta \tag{3.30}$$

$$= S_{v_{n,in}}(f) \cdot 4 \cdot BW \left[\frac{\pi}{2}\right] \tag{3.31}$$

$$= 4S_{v_{n,opamp}}(f) \cdot 4 \cdot BW \left[\frac{\pi}{2}\right] \tag{3.32}$$

The contribution from the opamp in the second inverting amplifier is straightforward and is given as below. The only change that is seen is that the gain is

unity instead of 2.

$$\overline{v_{out}{}^2} = 4S_{v_{n,opamp}}(f) \cdot 1 \cdot BW \left[\frac{\pi}{2}\right] \tag{3.33}$$

From Eqn. 3.32 and 3.33, we can see that the total noise power due to the two opamps will be $4S_{v_{n,opamp}}(f) \cdot 5 \cdot BW(\pi/2)$.

Opamp noise: Fully-differential amplifier

The analysis is very similar to the cascade architecture. To achieve a gain of 2, we use a feedback factor of $1/3$. With this, the noise gain of the circuit is 3. That is to say that if $v_{n,opamp}$ represents the total input referred noise voltage of the fully-differential opamp, then the noise voltage seen at the output will be amplified by a factor of 3. Since the overall gain of the circuit is 2, the input referred noise voltage of the opamp when referred back to the input of the driver will be $3v_{n,opamp}/2$. Therefore, if $S_{v_{n,opamp}}(f)$ represents the total input referred noise voltage of the opamp, then the power spectral density when it is referred to the input of the driver, denoted by $S_{v_{n,in}}(f)$ can be as follows.

$$S_{v_{n,in}}(f) = \frac{9}{4} S_{v_{n,opamp}}(f) \tag{3.34}$$

Because of the frequency independent gain, the feedback branch will not filter the noise from the opamp. However the output filters do provide filtering. It is assumed that the bandwidth of the closed loop amplifier is larger than the bandwidth of the output filters and therefore the effect of the finite bandwidth of the opamp is not taken into consideration for noise calculations. Therefore the effective transfer function can be written as follows. BW refers to the bandwidth of the output filter.

$$H(f) = \frac{2}{1 + \mathrm{j}\frac{f}{BW}} \tag{3.35}$$

Following the same lines as before, we obtain the total integrated noise at the output as shown below.

$$\overline{v_{out}{}^2} = \frac{9}{4} S_{v_{n,opamp}}(f) \cdot 4 \cdot BW \left[\frac{\pi}{2}\right] \tag{3.36}$$

Therefore, from the results of the two architectures, we can see that for the same g_m in the input stage of the opamps, the fully-differential architecture provides for a lower noise than the cascade of the inverting amplifiers. This is because the total noise power seen at the output (due to the opamp only) in the cascade of inverting amplifiers architecture is more than double the total noise power seen in the case of the fully-differential amplifier. Further, to have the same amount of g_m , we will have to burn twice the power in the cascade of inverting amplifiers architecture just because of the presence of two opamps. Therefore, even though the total resistor noise is smaller in the cascade of inverting amplifiers architecture, the amount of power that has to be dissipated to meet the noise requirement is more. Hence the fully-differential architecture is better suited for implementation as far as the noise performance is concerned.

Distortion

As explained in Section 3.3, the fully-differential amplifier architecture is better suited for low distortion design because the even order harmonics get cancelled perfectly (assuming matching between the transistors). In the cascade of inverting amplifier architecture, it was seen that the even order harmonics do not get cancelled.

A more subtle disadvantage for achieving low distortion in the cascade of inverting amplifiers architecture is that the first inverting amplifier is loaded by the input resistance of the second inverting amplifier in cascade. From the noise analysis, it is seen that this resistance cannot be very high. Therefore the output

stage of the opamp in the first inverting amplifier will have to support a significantly large bias current which will cause extra nonlinearity. Therefore, the distortion performance of the fully-differential amplifier is also expected to be better than that of the cascade of inverting amplifiers architecture.

Output offset

The comparison of the two architectures for their total output offset follows the opamp noise comparison very closely. In the case of fully-differential amplifier architecture, the input-referred offset of the opamp will get amplified by a factor of 3 to the differential output. This is because the feedback factor in use is 1/3. In the case of cascade of inverting amplifiers architecture, the input-referred offset voltage of the opamp in the first inverting amplifier will get amplified by a factor of 2 to its output and will further get amplified by a factor of 2 to the total differential output. Also, the input referred offset voltage of the opamp in the second inverting amplifier will also get amplified by a factor of 2 to the total differential output. Therefore, for the same mismatch between the input pair transistors in the opamps of the two architectures, the total output offset seen in the fully-differential architecture will be smaller.

Gain error

In the previous chapter, it is shown that the for the same value of input resistor, the input resistance of the fully-differential architecture is larger. Therefore the gain error from the fully-differential architecture should be smaller among the two. Yet another disadvantage with the pseudo-differential nature of the output in the cascade architecture is that any delay between the two anti-symmetric components of the output can cause gain error.

Settling time

The pseudo differential nature of the output in the cascade architecture is expected to have a larger settling time when compared with the fully-differential architecture for the same small-signal bandwidth. This is because a part of the signal has to pass through a cascade of two individual amplifiers as opposed to a single amplifier in the fully-differential architecture.

Based on the above arguments, it is clear that the fully-differential architecture is a better option than the cascade of inverting amplifiers. Hence, the fully-differential architecture is chosen for the implementation of the prototype.

3.5 Schematic design

3.5.1 Bandwidth

The closed loop bandwidth of the driver is derived from the settling time specification. It is given in Table 3.2 that the output of the driver should settle to 18-bit accuracy within 1 μs. To arrive at the required closed loop bandwidth specification, we assume that the output of the driver will follow first order behaviour. The assumption is justified because, at the output, we have first order lowpass filters anyway as shown in Fig. 3.12. The settling at the output of the opamp will have some effect to the settling at the final driver output. Since we choose to keep the loop bandwidth to be much larger than the output filter bandwidth, the effect is expected to be smaller. Towards this end, we choose to keep the loop bandwidth to be ten times the bandwidth of the filter at the output. Therefore the closed loop bandwidth as seen at the output of the opamp is 25 MHz.

Assuming first order response at the output, it can be seen that we require 13τ

to reach 18-bit accuracy. The maximum settling time allowed is 1 μs. Therefore τ should be $\leq$ 80 ns. This implies that the bandwidth of the driver should be $\geq$ 2 MHz. With some margin, we choose to implement the driver to have a closed loop bandwidth of 2.5 MHz.

For a 2.5 MHz output filter with the load capacitor being 100 pF, the value of the series resistor R_1 gets fixed to 636 Ω. Also, based on the gain error and total noise specification, a choice of 2 kΩ for the input resistor R is valid. See 2 for details. As discussed in Section 3.3, to get the advantage of additional filtering from the frequency dependent feedback impedance, the time constant of the filter present in the feedback path should be close to the time constant of the filter present at the output. We choose a value of 4 MHz for the bandwidth of the filter in the feedback path. This fixes the value of C to 20 pF. Note that these are exactly the same values that were used for the comparison in Section 3.4.3

3.5.2 Input g_m required

The noise contributions from various sources in the fully-differential amplifier is found out analytically in Section. 3.4. Table 3.8 summarizes the contributions. R =2 Ω, C = 20 pF, R_1=636 Ω, C_L=100 pF, and BW=2.5 MHz are used to find out the numerical contributions. It is seen that the opamp in total can contribute 556e-12 V^2 of noise power to the output.

Table 3.8: Noise summary of the fully-differential amplifier architecture

Noise source	Analytical expression	Calculated value (V^2)
Input & feedback resistors	$12kTR/(RC + R_1C_L)$	960e-12
Output resistors	$2kT/C_L$	84e-12
Opamp	$9S_{v_{n,opamp}} \cdot BW \cdot (\pi/2)$	556e-12 (available)

The thermal noise spectral density of the input referred noise voltage of an opamp which has a differential pair with active load as the first stage is given

as below.

$$S_{v_{n,opamp}}(f) = 8kT\gamma \left[\frac{1}{g_{m_1}} + \frac{g_{m_2}}{g_{m_1}^2} \right] \tag{3.37}$$

Here, k and T have their usual meaning. γ=2/3 for transistors in the long channel operation and is typically found higher under short-channel operation of the transistor. g_{m_1} refers to the transconductance of the input pair transistors and g_{m_3} refers to the transconductance of the load transistors. The noise from the subsequent stages will be insignificant compared to the noise from the first stage and is therefore neglected.

Along with thermal noise, the transistors also contribute frequency dependent flicker noise. A 3:1 ratio is chosen for the thermal noise to flicker noise contribution. Therefore, the opamp should be designed such that its flicker noise contribution is $\leq$139e-12 V^2 and the thermal noise contribution is $\leq$417e-12 V^2. Based on this, we can write the following.

$$\text{417e-12} = 9 \cdot 8kT\gamma \left(\frac{1}{g_{m_1}} + \frac{g_{m_3}}{g_{m_1}^2} \right) BW \cdot \frac{\pi}{2} \tag{3.38}$$

We now assume that g_{m_3} to be half of g_{m_1}. By design, we need to ensure that this condition holds true and this is not an unreasonable assumption. Substituting the values of $\gamma = 2/3$, BW=2.5 MHz, T=273 K, the Boltzmann's constant, and g_{m_1} of 10 mS the contribution from the first stage is close to 300e-12 V^2. With this, we have a room of around 100e-12 V^2 to accomodate for deviations. Therefore, the transconductance of the input pair transistors should be designed to be close to 10 mS and the transconductance of the load transistors in the first stage should be designed to be close ot 5 mS.

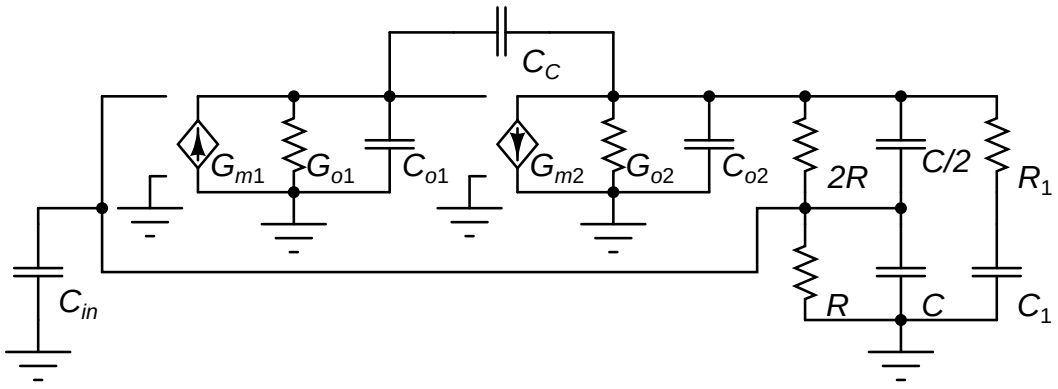


Figure 3.13: Small-signal model of the driver amplifier.

3.5.3 Small-signal details

Since a 0.6 μm CMOS process with a nominal power supply of 5 V is chosen for the implementation of the prototype, obtaining high DC gain will not require many stages. Techniques like cascoding and gain-boosting can be implemented easily. However, the output has to support rail-to-rail swing and because of this, we choose a two-stage architecture for the opamp.

The small-signal model of the feedback amplifier is as shown in Fig. 3.13. G_{m1} represents the transconductance of the input stage. In Section 3.5.2 it is shown that G_{m1} should be $\sim$10 mS. G_{o1} represents the output conductance of the first stage. In the process it is seen that the transistors easily have an intrinsic gain of $\sim$100. With this, if cascoding is employed in the first stage, then we can obtain G_{o1} of $\sim$2 μS. C_1 represents the parasitic load capacitance of the first stage. This is assumed to be $\sim$5 pF.

G_{m2} represents the transconductance of the second stage. With a feedback factor of 1/3, it is shown in Section A that for stability, $G_{m2} \geq 0.5G_{m1}$. Therefore, with some margin, we choose a value of $\sim$10 mS for G_{m2}. As before, assuming an intrinsic gain of 100 and without cascoding, we obtain G_{o1} to be close to $\sim$100 μS. C_{o2} is assumed to be $\sim$5 pF and is the parasitic load of the second stage.

The feedback network comprising of R and C is shown in the model. The output lowpass filters consisting of R_1 and C_L are also shown. C_{in} represents the parasitic capacitor at the input of the opamp. A value of 10 pF is assumed for small-signal bandwidth simulations.

The approximate locations of all the poles and zeros are found out. A 8 pF capacitor is used as the compensation capacitor (C_C). Table 3.9 has the details of the poles and zeros of the small-signal model in question. $p1$, the pole associated with the Miller capacitor is the dominant pole. In the expression for $p1$, $Gain_2$ represents the gain from the second stage alone.

With the presence of the frequency dependent impedances in the feedback path and RC filter at the output of the opamp, two poles—one associated with the C_L and the other associated with $[C_{o2}||(\text{series combination of } C \text{and} 0.5C)]$—are created. The approximate locations are easily evaluated as shown in Section B. In the expressions for $p2$ and $p3$, R'_{o2} represents the parallel combination of G_{o2} and $G_{m2}C_C/(C_C + C_1)$. It is seen that $p2$ is within the attempted unity loop-gain frequency of 25 MHz. It should be noted that the zero $z1$ formed by the output filter is very close to $p2$ and compensates it. $p3$—pole associated with $C_{o2} + C/3$ and $z2$—RHP zero formed due to the feedforward path through the Miller capacitor are seen to be beyond the unity loop-gain frequency and hence are neglected. One important thing that has to be noted here is that the presence of C_{in} creates a closely spaced pole-zero pair at 2.98 MHz. Although this does not cause any degradation in the phase margin in the loop, it can lead to slow settling components as described in [18].

With this small-signal model, the simulated unity loop-gain frequency is seen to be $\sim$35 MHz. The aim was to have a closed loop bandwidth of $\sim$25 MHz. With the above setup, we have enough room to support the parasitic poles that arise from cascode and other circuit additions.

Table 3.9: Pole-Zero summary of the small-signal model

	Expression	Frequency
$p1$	$G_{o1}/2\pi C_C(1+Gain_2)$	$\sim 1\,\text{kHz}$
$p2$	$1/\left(2\pi\left(\left(R'_{o2}\|\|3R\right)+R_1\right)C_1\right)$	$\sim 2\,\text{MHz}$
$p3$	$1/2\pi(R'_{o2}\|\|3R\|\|R_1)(C_{o2}+C/3)$	$\sim 80\,\text{MHz}$
$z1$	$1/2\pi R_1 C_1$	$\sim$2.5 MHz
$z2$	$G_{m2}/2\pi C_C$	$\sim$200 MHz (RHP zero)

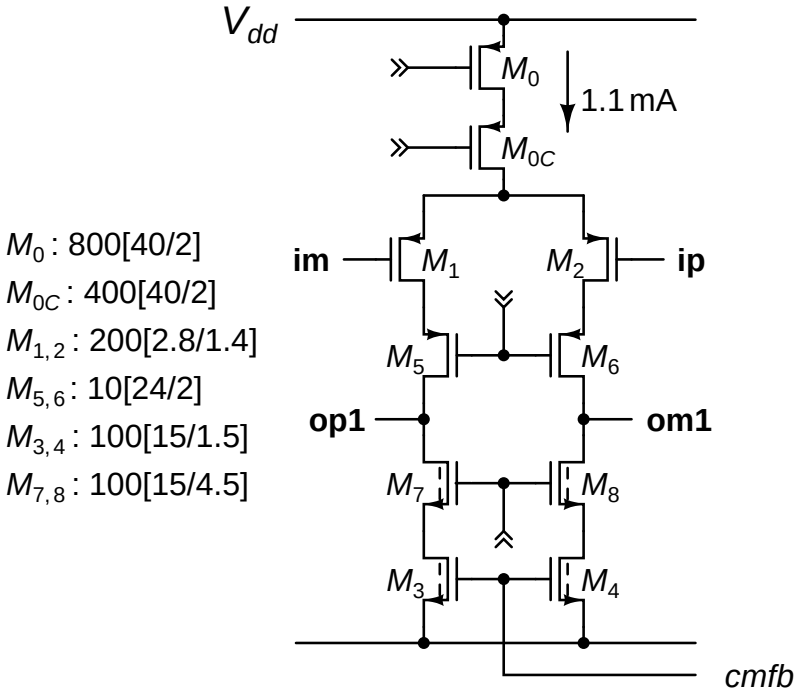


Figure 3.14: Input stage of the opamp.

3.5.4 Opamp design

First stage

We made the assumption of cascodes in the first stage while dealing with the small-signal model of the amplifier so as to obtain a very high DC gain. There are two ways of employing cascodes—telescopic and folded. We choose the telescopic cascode for the implementation. The advantages of this choice over the folded cascode are (a) smaller power consumption as there is no folding arm, (b) higher gain because of the reduced loading, and (c) lesser noise because

of the absence of current sources required to bias the folding arm.

Further, as pMOS transistors contribute lower flicker noise and offset, input pair is made a pMOS input pair. To reduce the noise and offset contribution from the load nMOS transistors, we choose the natural flavor over the standard V_T flavor. The natural transistors are indicated by a dashed line in the symbol.

Based on noise considerations, we have shown that the input stage g_m should be $\sim$10 mS. Assuming a g_m/I_D of 15, the current required through the input transistors is $\sim$667 μA. We choose a current of 550 μA for the input transistors. The transistors are sized so that the g_m obtained is $\sim$9.3 mS. The cascodes are chosen such that the output resistance seen looking into the pMOS side alone is $\sim$3.5 MΩ.

In the discussion on opamp noise, it was also assumed that the g_m of the load transistors in the first stage is half of the g_m of the transistors in the input stage. So, the nMOS load transistors are sized such that they provide a g_m of 5.4 mS. Again, cascodes are sized such that the output resistance looking into nMOS side alone is $\sim$2.5 MΩ. Therefore, the total output resistance seen at the output of the first stage is $\sim$1.5 MΩ and the DC gain of the stage is $\sim$80 dB. The schematic of the first stage is as shown in Fig. 3.14

It can be seen from Fig. 3.14 that a cascode transistor is used in the implementation of the tail current source. The design of this current source is tricky because of the very small headroom available. The available headroom is small because the fully-differential amplifier is configured to be used as a single-ended to differential converter by holding one input of the amplifier at a common-mode value. This configuration causes the input terminals of the opamp to see a swing that is $1/3^{rd}$ of the total swing of the input to the amplifier. With a 5 V power supply, the input terminals of the opamp can see a swing between $\sim$1.8 V to $\sim$3.3 V around 2.5 V common-mode. Allowing for sufficient V_{GS} for the input pair, the worst case headroom available to bias the tail current

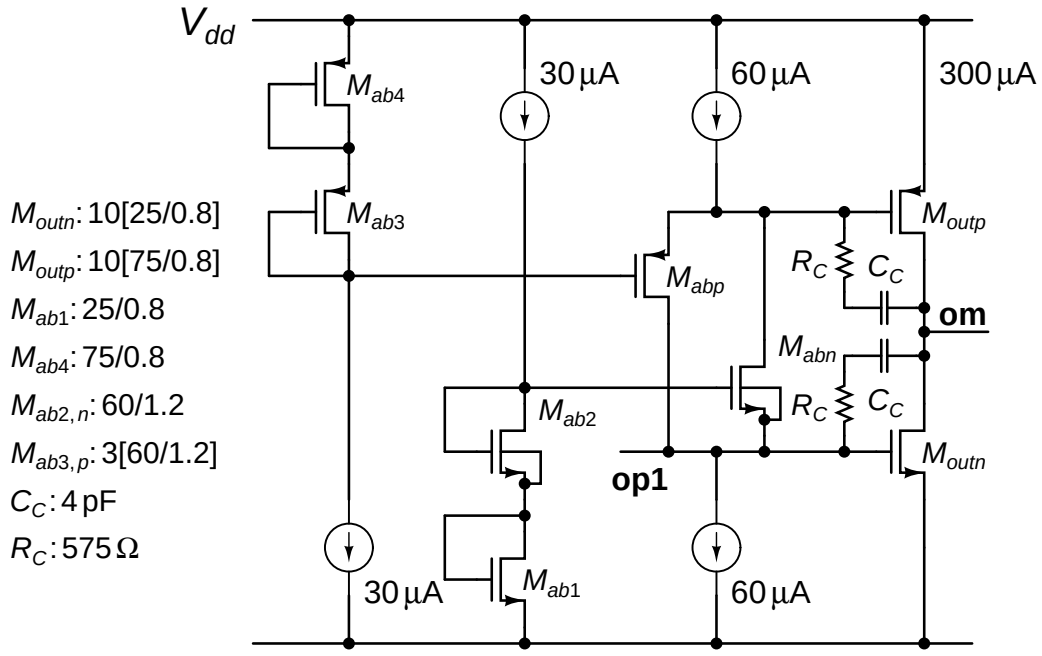


Figure 3.15: Second stage of the opamp.

source is ∼500 mV. Each of the transistors is biased to have overdrive voltage of ∼200 mV. The total output resistance provided by this current source is 640 kΩ.

Second stage

In order to obtain maximum g_m for a given current in the output stage, we choose the class-AB output stage. Fig. 3.15 shows the circuit diagram of the second stage. The biasing setup used to obtain the class-AB operation was first demonstrated in [19]. [20] and [21] provide insight into the operation of the same with more details. Yet another reason to choose a class-AB output stage is because of its superior settling performance compared to the class-A output stages.

From the small-signal model, we know that the second stage should provide a total g_m of 10 mS. Since the design is a class-AB type, we can share the g_m between the output nMOS and pMOS transistors. Therefore, from a single tran-

sistor, we need a g_m of $\sim$5 mS. Assuming a g_m/I_D of 15, the current required in the output branch is $\sim$333 μA. We choose to bias the output transistors at 300 μA.

M_{ab1-4} form the bias transistors for the stage and $M_{abn,\,p}$ form the control transistors. The stage is based on the translinear loops formed (see [22]). M_{ab1}, M_{ab2}, M_{abn}, and M_{outn} form one loop and a similar loop consisting of pMOS transistors can also be seen. To ensure that the biasing is stable, the V_T of M_{ab1} and M_{outn} should match well. This can taken care by having them close to each other and having dummy fingers around them. Simulatenously, the V_T of M_{ab2} and M_{abn} should also match. Achieving this is not as straightforward as the previous case because of the presence of the signal. With the presence of the signal at the source of M_{abn}, the body effect of that transistor comes into play and because of that the threshold voltage of M_{abn} gets modulated. The bias transistor M_{ab2} does not experience this effect. Therefore, the output stage current gets modulated and will lead to significant nonlinear distortion. To ensure good matching between these transistors, we use "isolated" nMOS transistors (comes with a triple well process). With this flavor, the body of the devices can be connected to their respective sources and thereby mitigating the problem. Similar arguments can be made with the pMOS side of the output stage as well. The fact that the body of the pMOS transistors is easily available helps in achieving the necessary matching.

We use a ratio of 1:10 between M_{ab1} and M_{outn}. This will ensure that the current through the output stage will be 10 times the current through M_{ab1}. Since we need the output stage current to be equal to 300 μA, we bias the M_{ab1} transistor with 30 μA. A 1:10 ratio is also maintained between M_{ab4} and M_{outp} and M_{ab4} is also biased to carry a current of 30 μA. With this arrangement, the other bias transistors M_{ab2} and M_{ab3} will also carry 30 μA. Therefore, we bias each of the control transistors M_{abn} and M_{abp} with 30 μA.

A disadvantage of using class-AB operation is that the g_m of the output stage varies with the input signal. In order to keep the modulation of g_m of the output stage small, the biasing is done such that even with peak signal, both the output transistors remain in saturation. This is achieved by suitably choosing the g_m and the bias current of the control transistors. The choice should be such that even at peak signal operation, none of the control transistors should completely turn off. Effectively, the arrangement is the same as two class-A common source amplifiers in parallel. Further it is seen that the distortion performance of the output stage is better if the two control transistors have the same g_m . In order to ensure this, we size the pMOS three times as large as the nMOS control transistor.

The g_m of the M_{outn} is seen to be $\sim$4.8 mS and that of M_{outp} is $\sim$4.6 mS . Also, the output resistance seen from the stage is around 20 kΩ.

The Miller-compensation capacitor of 8 pF is realised as two 4 pF capacitors and are connected across the two output transistors. Further, series resistors (R_C) are also used to bring the RHP zero formed because of the Miller-compensation to the left half plane to improve the phase margin. The zero is now placed at 1.5 $\times$ the unity loop-gain frequency.

Common-mode feedback

A single error amplifier scheme is used to set the output common-mode voltage of both the stages. Fig.3.16 shows the common-mode detector, error amplifier and the load of the first stage of the opamp. The second stage is not shown in the figure to avoid clutter. Since the swing at the output is rail-to-rail, a highly linear common-mode detector is required. Hence, a resistive common-mode detector is used. 250 kΩ resistors are used so that the gain of the second stage of the opamp is not reduced. However, this large resistor along with the input capacitance of the error amplifier creates a low frequency pole and reduces the

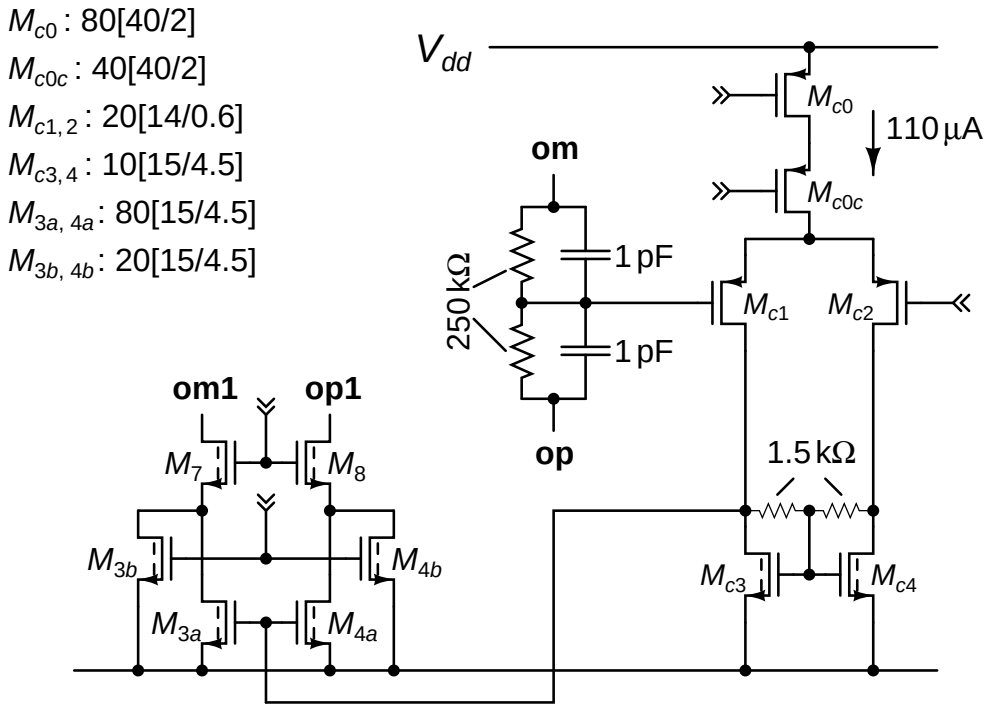


Figure 3.16: Common-mode feedback circuitry.

phase margin. In order to overcome the effect of phase margin degradation due to this pole, additional capacitors of 1 pF are placed in parallel to the resistors.

It can be seen that the common-mode loop is effectively a three-stage structure including the error amplifier. The compensation capacitor which is used to compensate the differential loop itself also acts as the compensation capacitor to the common-mode loop. Since, there is no freedom in changing the compensation capacitors, the gain of the three-stage structure should be controlled such that the loop is stable. This requires the error amplifier to have a very low gain. The error amplifier in Fig. 3.16 is a low gain amplifier. The error amplifier itself can be interpreted as a fully-differential single stage amplifier with resistive common-mode feedback. Low valued resistors (1.5 kΩ) are used to bring down the differential gain of this single stage amplifier. Without the resistors, the gain obtained from the error amplifier is found to be large enough to reduce the phase margin.

The output of the error amplifier is fed to the load of the first stage (M_3 and M_4 in Fig. 3.14) of the opamp. The g_m of these transistors decides the gain of the this stage as far as the common-mode loop is concerned. The load transistors M_3 and M_4 have a g_m of $\sim$5 mS. Such a high value rendered the common-mode loop unstable. In order to reduce the g_m seen by the common-mode feedback signal, transistors M_3 (and M_4) are split into two parts M_{3a} and M_{3b} (M_{4a} and M_{4b}) such that M_{3a} (M_{4a}) carries 440 μA and M_{3b} (M_{4b}) carries only 110 μA. Note that originally M_3 carried a current of 550 μA. The common-mode feedback signal is now only fed to M_{3a} and M_{4a} as shown in Fig. 3.16. Since they carry much lower current, the g_m offered by them to the common-mode feedback signal is proportionally smaller and this helps us achieve stability.

M_{3a} and M_{4a} are explicitly biased to carry 440 μA each. The error amplifier is biased to carry a tail current of 110 μA. This current source is obtained from the same source that controls the first stage tail current. Replica biasing is used to match M_{c3} with M_{3b} (and M_{c4} with M_{4b}). A 11.5 pF capacitor is placed in parallel to the tail current source of the error amplifier. Doing this will create a pole-zero pair at the associated tail node and the pole is found to be at twice the frequency of the zero. Therefore, the phase lead provided by this zero is used to improve the phase margin of the common-mode feedback loop.

The intuition on the zero creation is as follows. At low frequencies, the tail node of the error amplifier will be at $v_{in}/2$, where v_{in} is the voltage at the input of the error amplifier. Now, the gain of the error amplifier can be calculated to be $g_m\ R_L/2$, where R_L is the effective load resistance. At high frequencies, the capacitor shunts the current source and the tail node will be effectively at ground and the corresponding gain will be $g_m\ R_L$. We can see that the setup has created a left half plane zero at $g_m\ /\mathrm{C}$, where C is the capacitor is used in parallel to the current source.

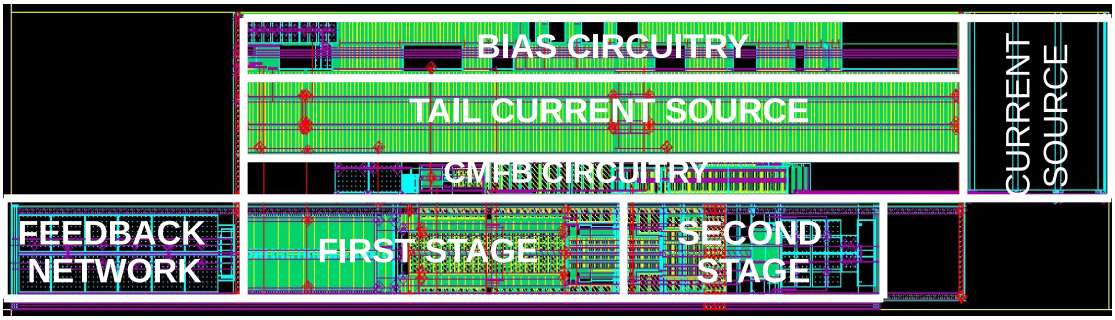


Figure 3.17: Snapshot of the layout view of the prototype driver.

3.6 Layout and Simulation results

3.6.1 Layout

Fig. 3.17 shows the layout of the prototype driver. The various blocks are also annotated. It should be noted that to obtain very good matching between the input pair transistors, the fingers are interleaved.

3.6.2 Simulation results

Unless otherwise mentioned, the simulation results are obtained from the extracted netlists from the layout. For extracting the netlist with parasitics, minimum R setting of 0.1 Ω and a minimum C setting of 1 fF is used. Further, 5 nH inductances are also used with relevant nodes to include the effect of the bond-wire inductance. Simulations are done at three different temperature settings of -40°, 25°, and 125° C and at three different power supply voltage settings of 4, 5, and 6 V and across the three different process corners.

Differential loop-gain

Figures 3.18 and 3.19 shows the loop-gain magnitude and phase response for the 27 different combinations respectively. In these simulations, the output filters (636 Ω + 100 pF) with 2.5 MHz bandwidth are present as load to the fully-

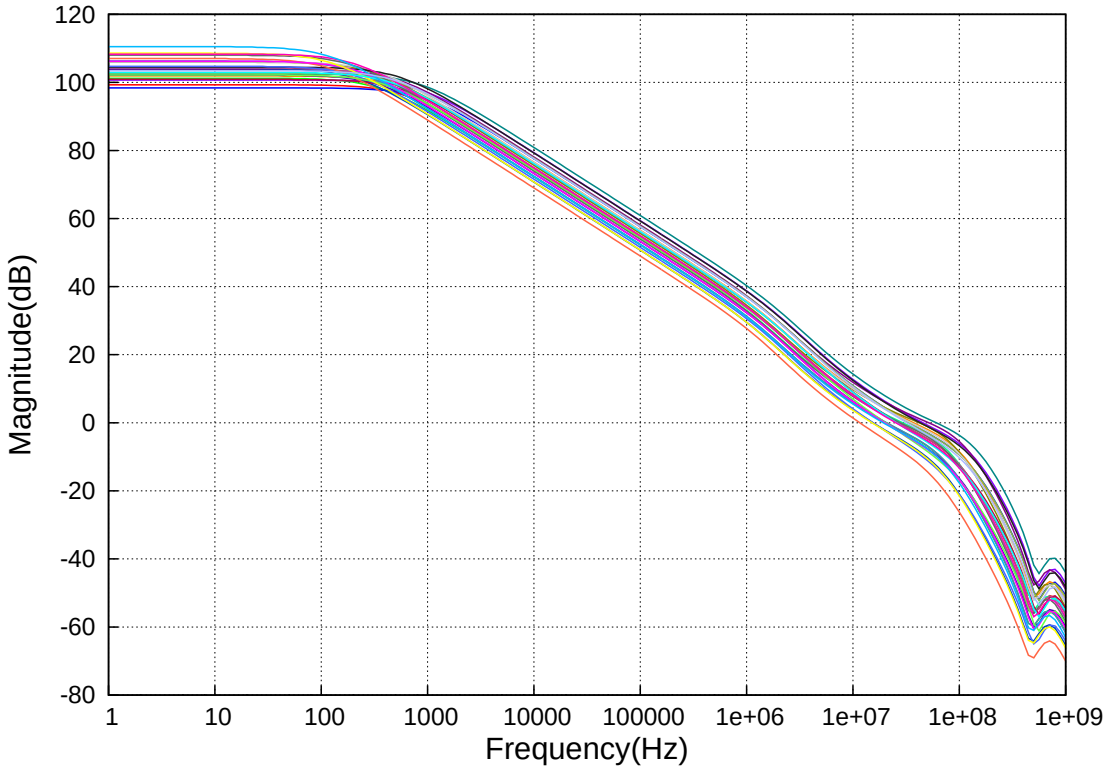


Figure 3.18: Magnitude response of the differential loop-gain over PVT variations.

differential amplifier.

In the nominal corner, the unity loop-gain frequency obtained is 26.76 MHz with 71° phase margin. Across the PVT corners a minimum phase margin of 62° is maintained. The minimum unity loop-gain frequency obtained is ∼11.6 MHz. This occurs with weak corner, 135° C and with 4 V power supply.

Common-mode loop-gain

Figures 3.20 and 3.21 shows the common-mode loop-gain magnitude and phase response for the 27 different combinations respectively. In these simulations, the output filters (636 Ω + 100 pF) with 2.5 MHz bandwidth are present as load to the fully-differential amplifier.

In the nominal corner, the unity loop-gain frequency obtained is 8.5 MHz with 65.6° phase margin. Across the PVT corners a minimum phase margin of 58° is

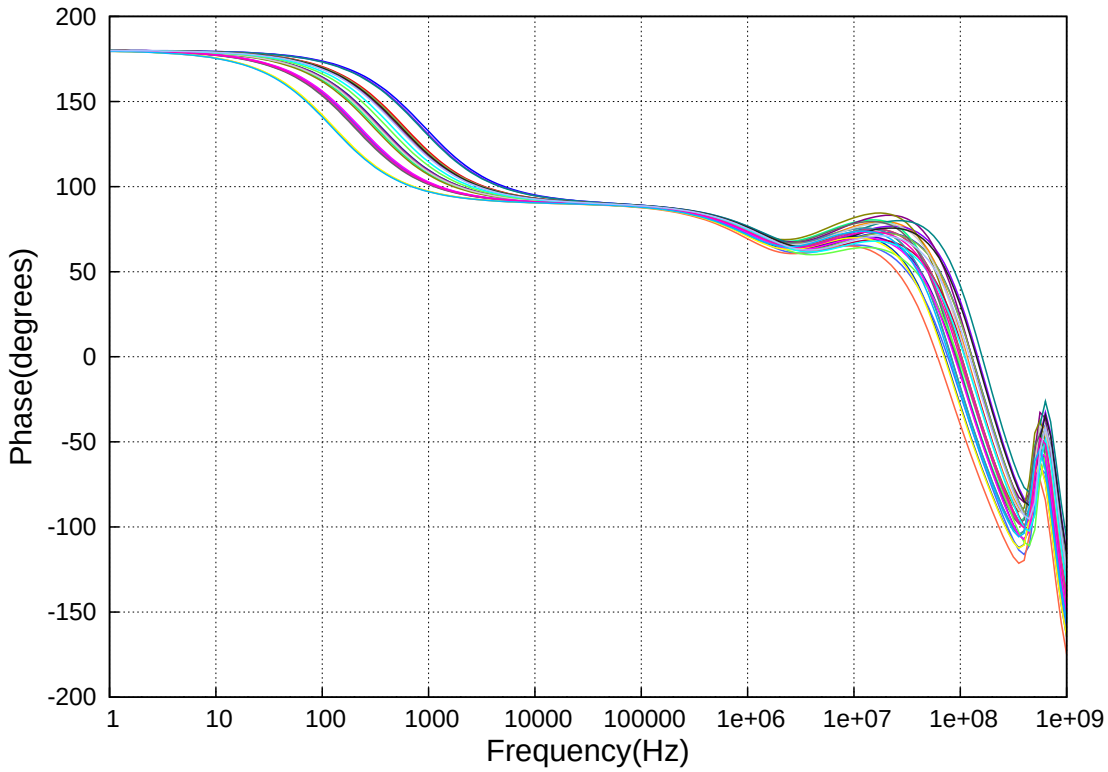


Figure 3.19: Phase response of the differential loop-gain over PVT variations.

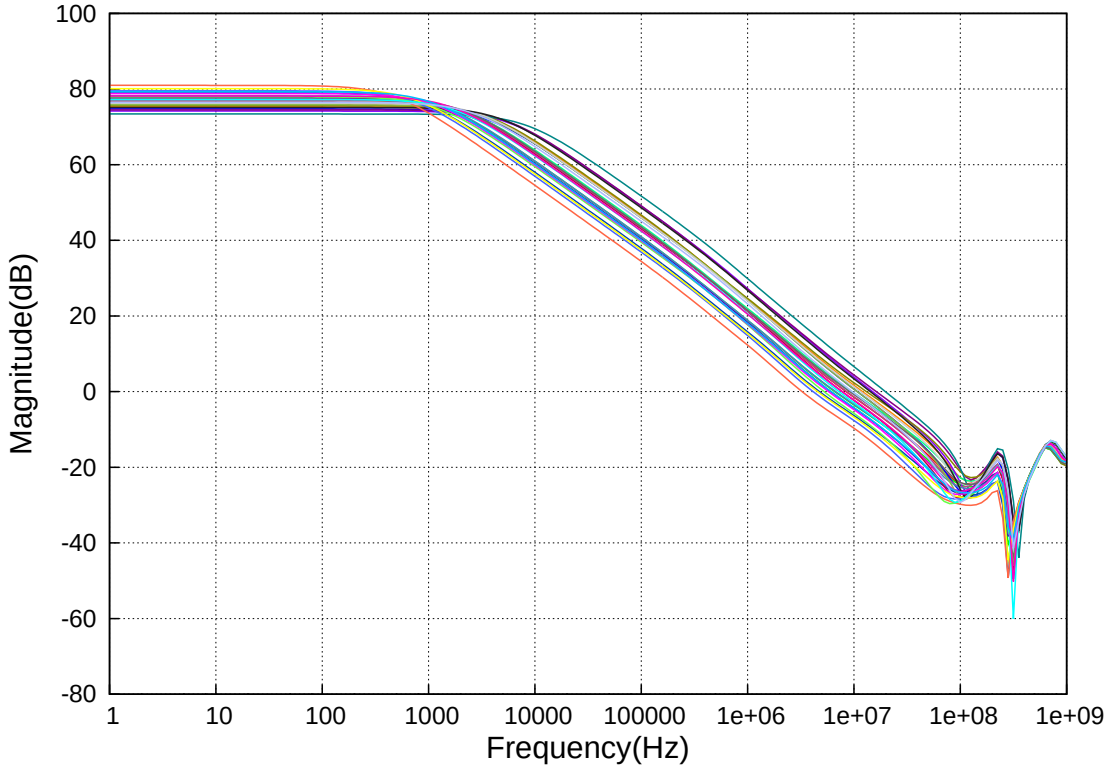


Figure 3.20: Magnitude response of the common-mode loop-gain over PVT variations.

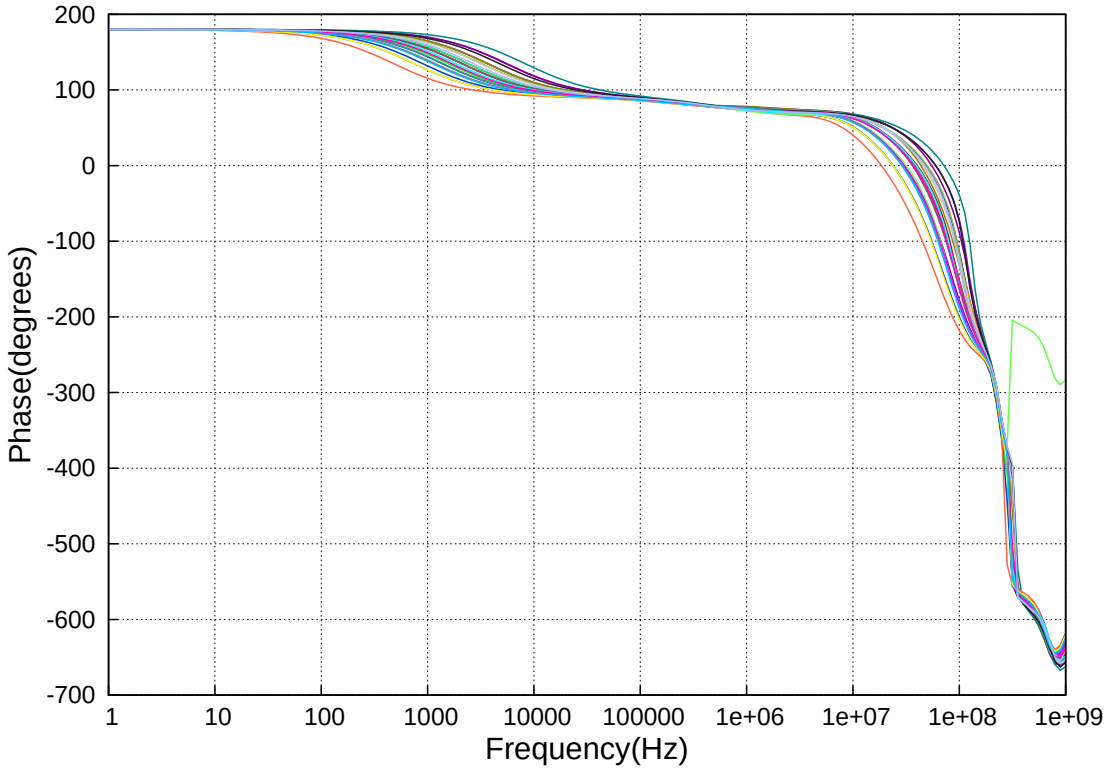


Figure 3.21: Phase response of the common-mode loop-gain over PVT variations.

maintained. The minimum unity loop-gain frequency obtained is ∼3.25 MHz. This occurs with weak corner, 135° C and with 4 V power supply.

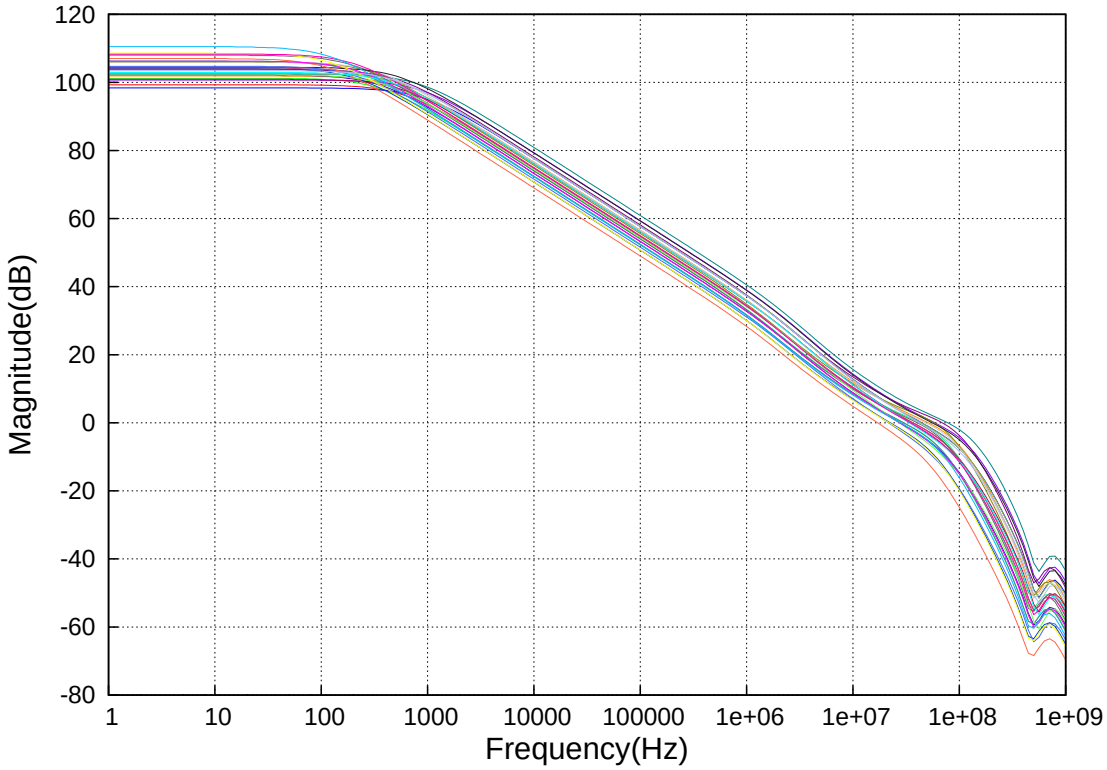


Figure 3.22: Magnitude response of the differential loop-gain over PVT variations in no load condition.

Differential loop-gain without load

Figures 3.22 and 3.23 shows the loop-gain magnitude and phase response for the 27 different combinations respectively. In these simulations, the output filters (636 Ω + 100 pF) with 2.5 MHz bandwidth are removed. This is important because the driver amplifier should remain stable even when the SAR ADC is in the conversion mode.

In the nominal corner, the unity loop-gain frequency obtained is 26.76 MHz with 71° phase margin. Across the PVT corners a minimum phase margin of 47° is maintained. The minimum unity loop-gain frequency obtained is ∼18.5 MHz. This occurs with weak corner, 135° C and with 4 V power supply.

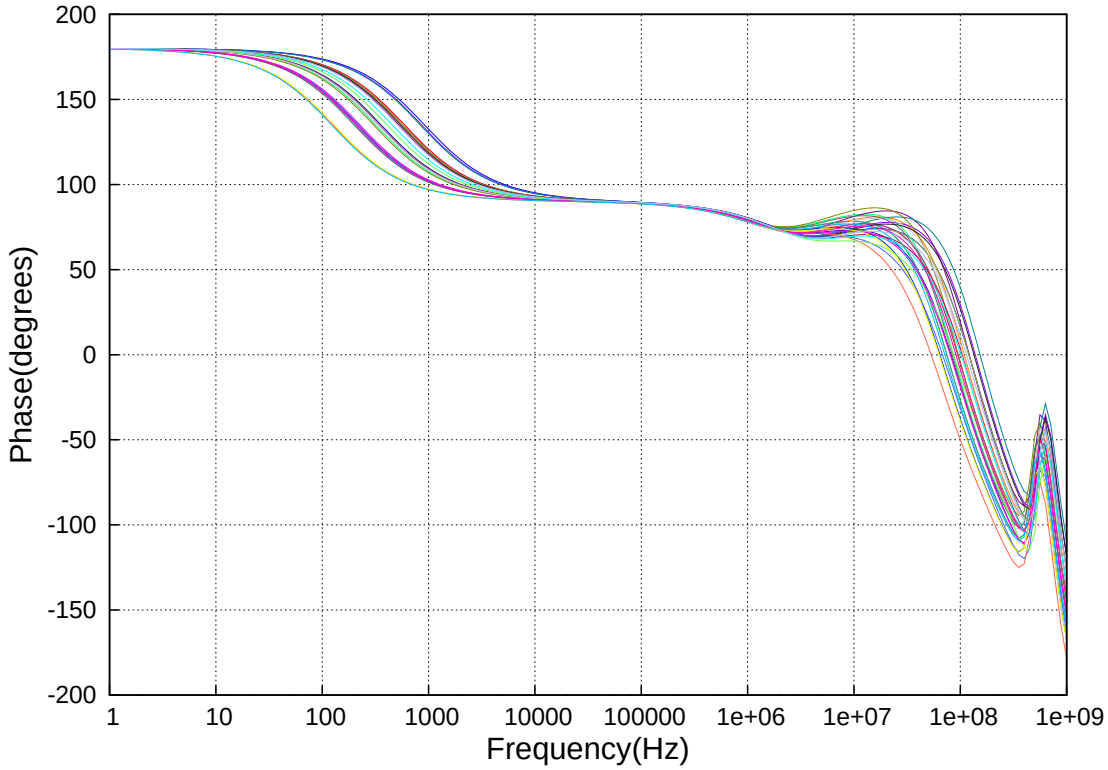


Figure 3.23: Phase response of the differential loop-gain over PVT variations in no load condition.

Common-mode loop-gain without load

Figures 3.24 and 3.25 shows the common-mode loop-gain magnitude and phase response with no load for the 27 different combinations respectively. In the nominal corner, the unity loop-gain frequency obtained is 8.5 MHz with 65.6° phase margin. Across the PVT corners a minimum phase margin of 55.5° is maintained. The minimum unity loop-gain frequency obtained is ∼4.5 MHz.

Closed loop response

Figures 3.26 and 3.27 show the magnitude and phase response of the driver in the presence of the output filter load. It can be seen that the gain is equal to two and is constant over the 100 kHz bandwidth. The phase response is also flat up to 100 kHz . It should also be seen that the bandwidth of the driver is close to 2.5 MHz. This can be seen by the magnitude plot where the gain reduces by

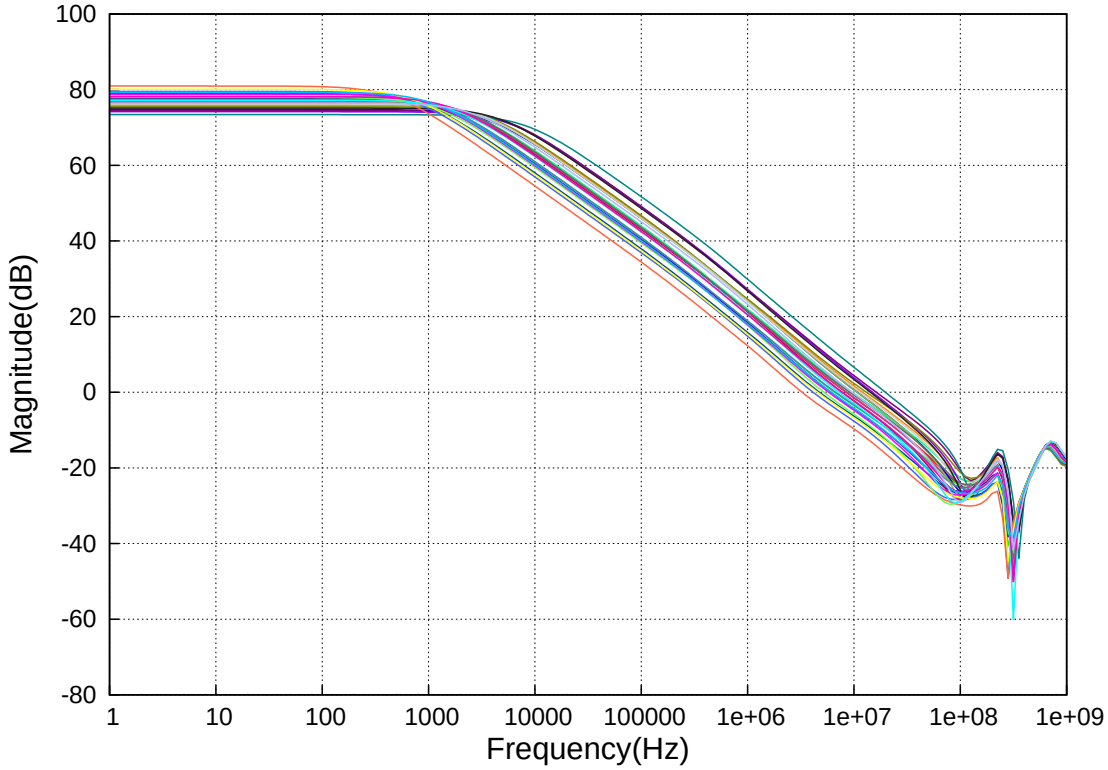


Figure 3.24: Magnitude response of the common-mode loop-gain over PVT variations in no load condition.

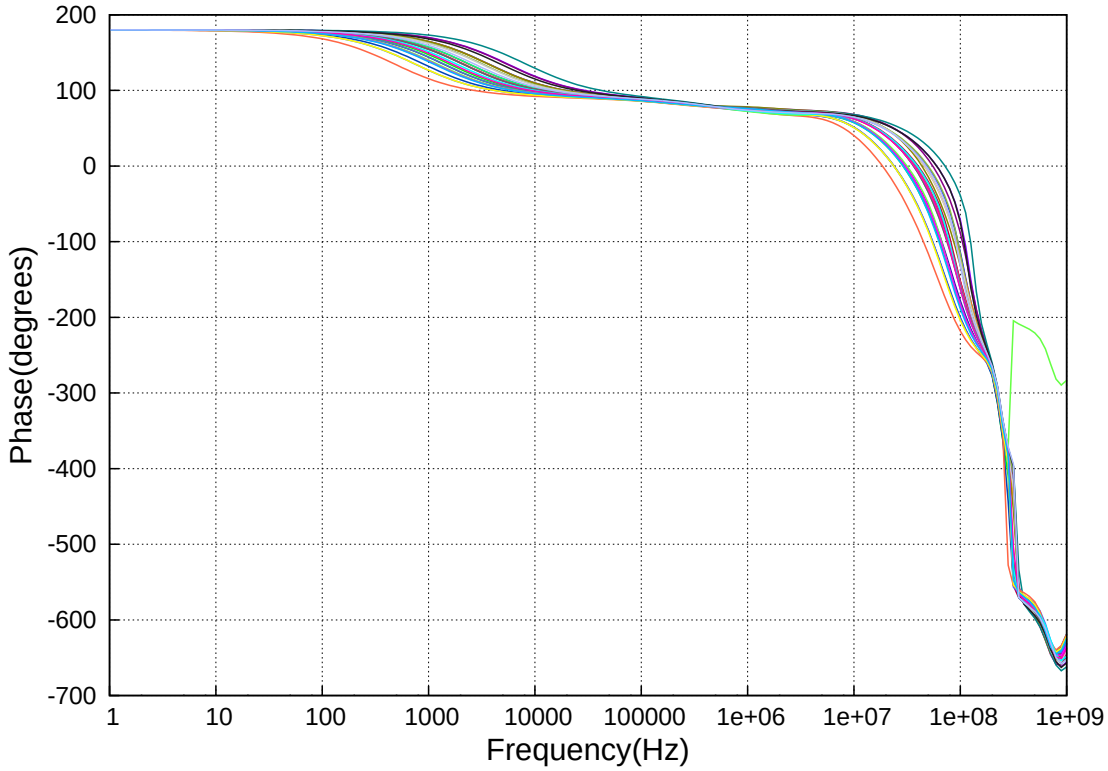


Figure 3.25: Phase response of the common-mode loop-gain over PVT variations in no load condition.

3 dB as well as in the phase plot where is a phase lag of 45° is seen.

Figures 3.28 and 3.29 show the magnitude and phase response of the driver in the absence of the output filter load. It can be seen that the gain is equal to two and is constant over a 1 MHz bandwidth. The phase response is also flat up to 1 MHz. Without the load, the bandwidth of the driver is above 25 MHz. Peaking in the response is also seen. This should not be a cause of concern as we are interested in signal frequencies up to 100 kHz only.

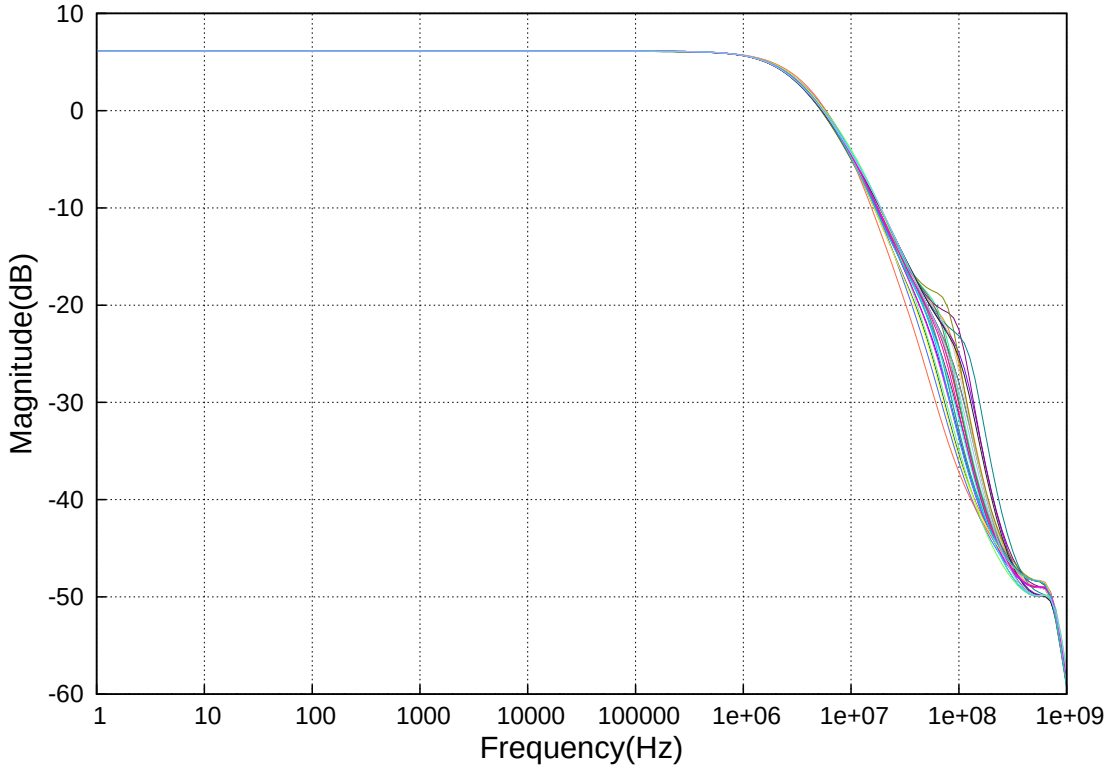


Figure 3.26: Magnitude response of the closed loop transfer function over PVT variations.

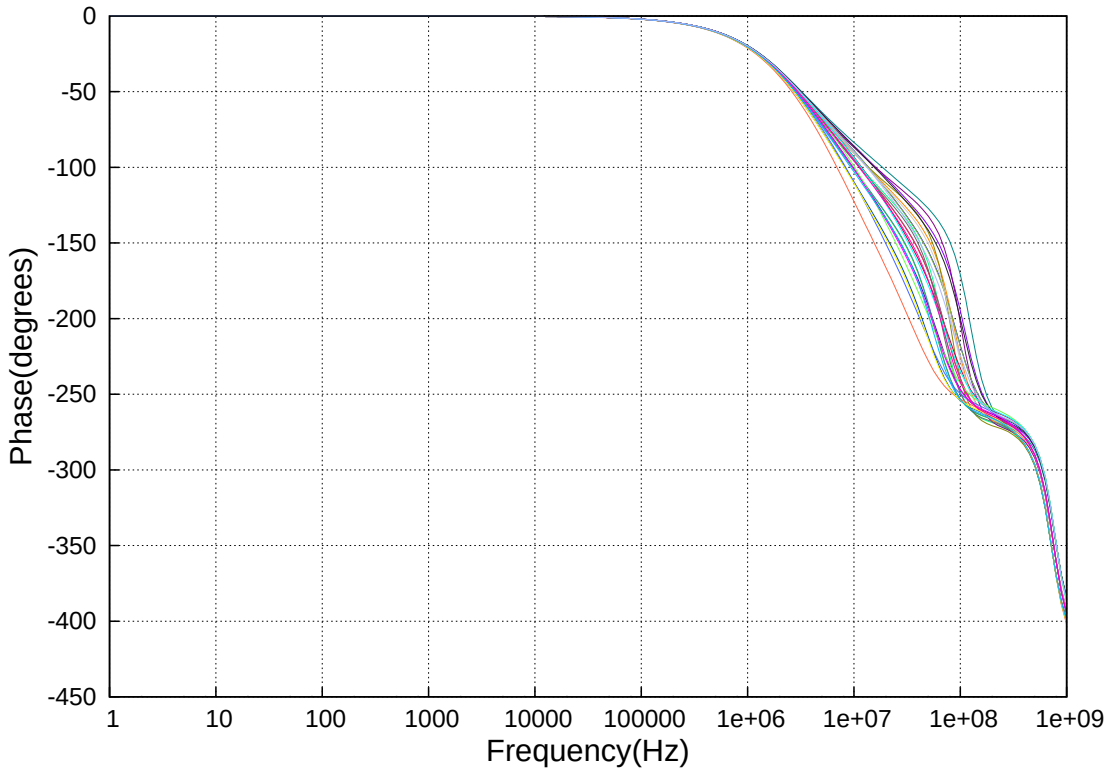


Figure 3.27: Phase response of the closed loop transfer function over PVT variations.

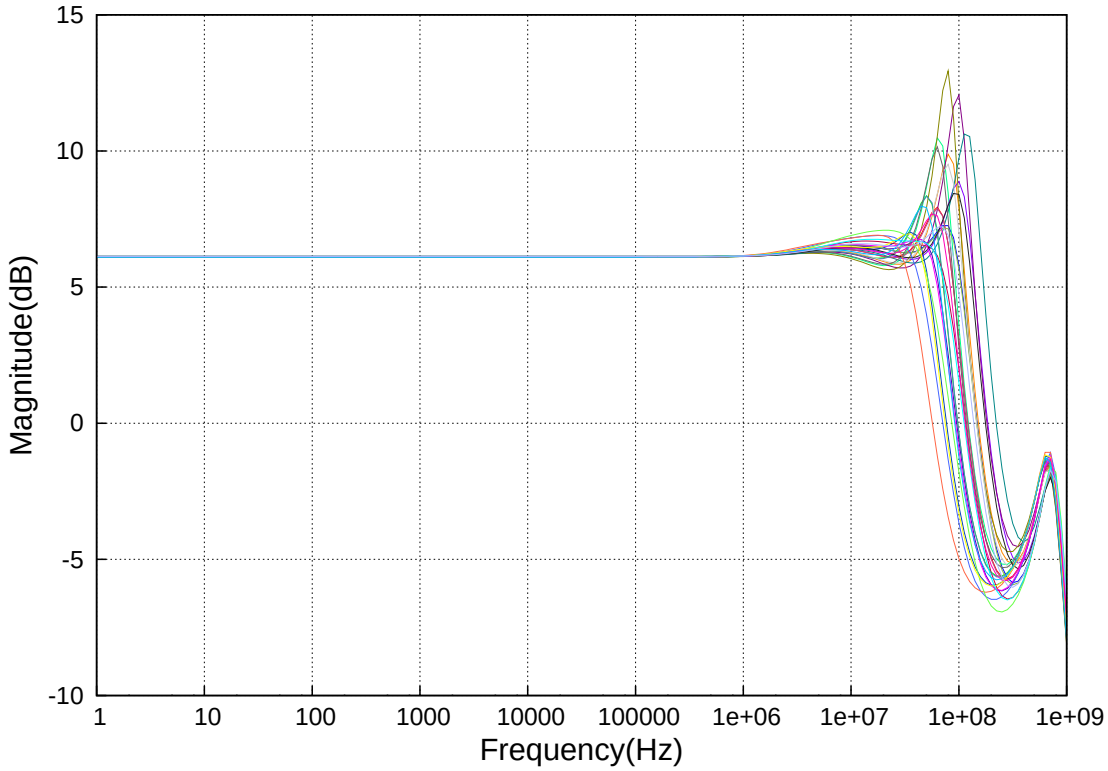


Figure 3.28: Magnitude response of the closed loop transfer function over PVT variations under no load condition.

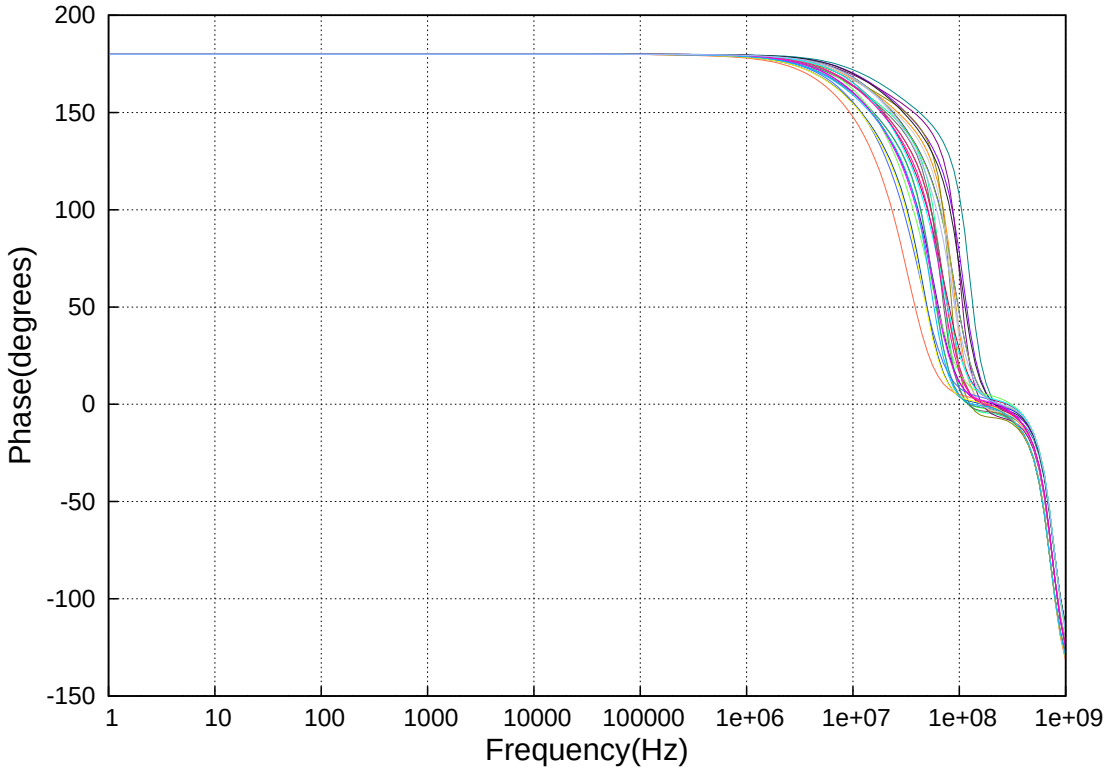


Figure 3.29: Phase response of the closed loop transfer function over PVT variations under no load condition.

Table 3.10: Lookup table for RRMOD

RRMOD	Temp.	V_{dd}	Corner	RRMOD	Temp.	V_{DD}	Corner
1	-40°	4	Nominal	15	30°	5	Strong
2	-40°	4	Weak	16	30°	6	Nominal
3	-40°	4	Strong	17	30°	6	Weak
4	-40°	5	Nominal	18	135°	6	Strong
5	-40°	5	Weak	19	135°	4	Nominal
6	-40°	5	Strong	20	135°	4	Weak
7	-40°	6	Nominal	21	135°	4	Strong
8	-40°	6	Weak	22	135°	5	Nominal
9	30°	6	Strong	23	135°	5	Weak
10	30°	4	Nominal	24	135°	5	Strong
11	30°	4	Weak	25	135°	6	Nominal
12	30°	4	Strong	26	135°	6	Weak
13	30°	5	Nominal	27	135°	6	Strong
14	30°	5	Weak				

Lookup table

Table 3.10 shows the PVT corners associated with each of the RRMOD value. The results of noise, distortion and step response simulations are shown with reference to RRMOD.

Noise

Table 3.11: Integrated output noise across PVT variations

RRMOD	Noise power (V^2)
1	1.135e-9
2	1.197e-9
3	1.053e-9
4	1.089e-9
5	1.143e-9
6	1.016e-9
7	1.057e-9
8	1.105e-9
9	988.6e-12
10	1.542e-9
11	1.637e-9
12	1.423e-9
13	1.469e-9
14	1.549e-9
15	1.364e-9
16	1.417e-9
17	1.488e-9
18	1.321e-9
19	2.220e-9
20	2.384e-9
21	2.029e-9
22	2.081e-9
23	2.214e-9
24	1.918e-9
25	1.986e-9
26	2.100e-9
27	1.840e-9

Table 3.11 shows the total integrated noise power at the output of the driver in the presence of output filters. It can be seen that RRMOD = 13 corresponds to

the nominal corner and in this case, the specification is met. The bandwidth over which integration is carried out is 1 mHz to 1 THz.

Step response

Large-signal:

A full scale (0.1V_{dd} -0.9V_{dd}) input step is applied to the driver and the settling time for an 18-bit accurate response is found out. The simulated results across the PVT corners are shown in Fig. 3.30 and 3.31. The results are shown for rising as well as falling step inputs. For these simulations, the nonlinearity of the 100 pF capacitor in the output load is modeled. Further an overall mismatch of 1% is explicitly added to the output filter sections. This is to account for the mismatch seen at the board level. From the plots, it is seen that driver meets the specification of $\leq$1 μs.

Small-signal:

Fig. 3.32 and 3.33 depict the settling time for 18-bit accurate response with small-signal rising and falling step at the input respectively. A 10 mV input step is used for the simulations. The error band is also made proportionally smaller while calculating the settling time. The variation of the settling time with PVT changes is very small indicating a very good small-signal performance of the driver.

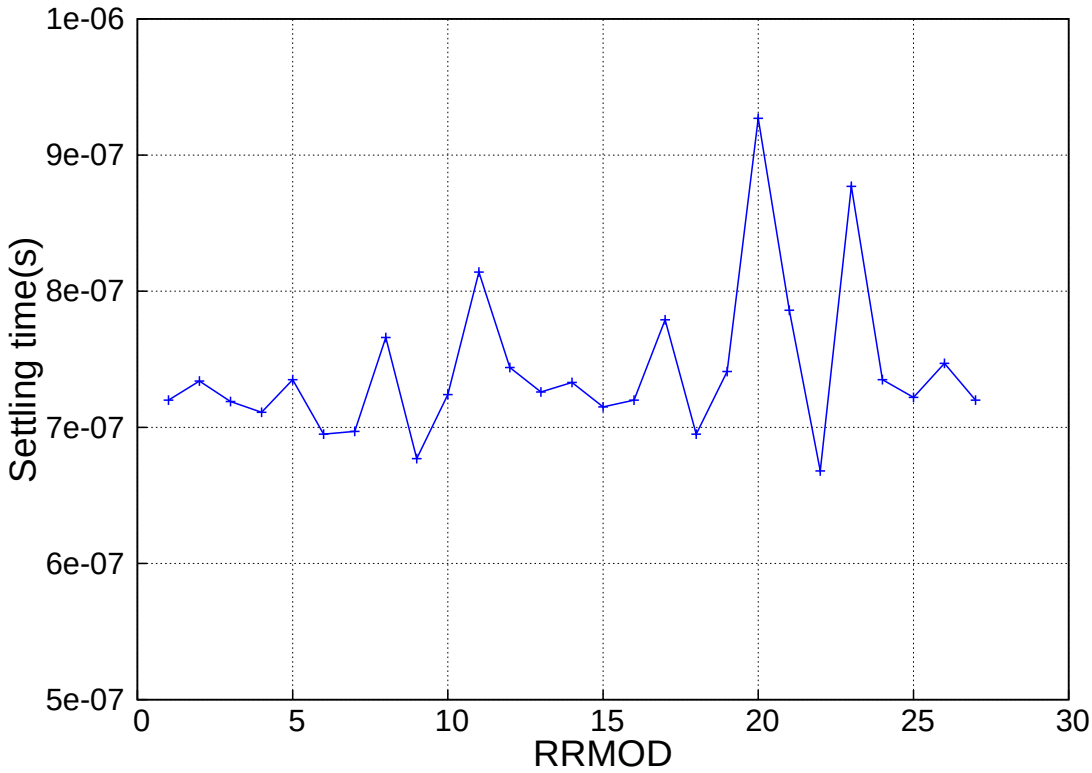


Figure 3.30: Settling time for 18-bit accurate response over PVT variations for rising input step.

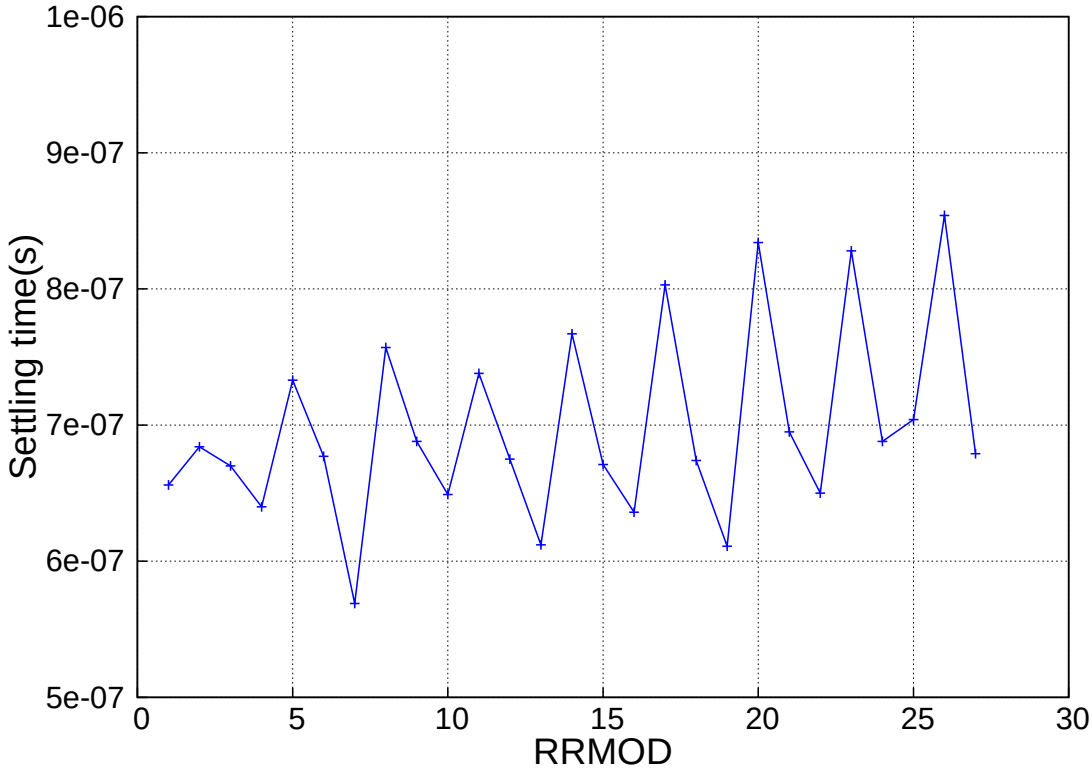


Figure 3.31: Settling time for 18-bit accurate response over PVT variations for falling input step.

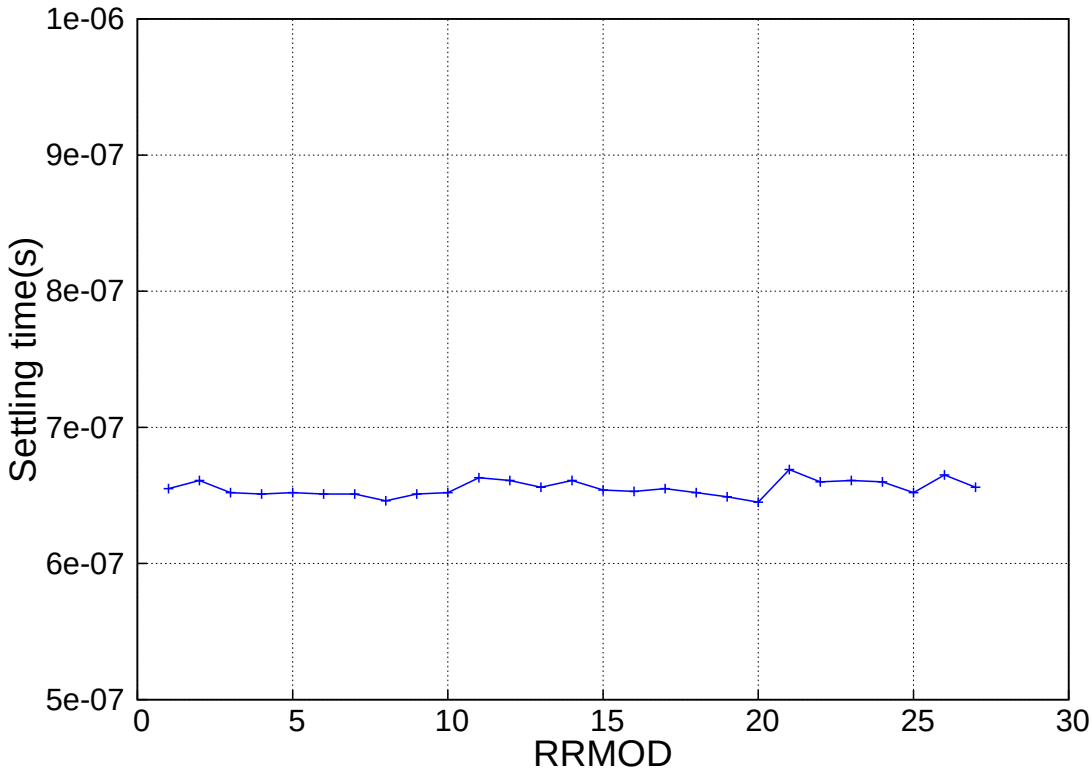


Figure 3.32: Settling time for 18-bit accurate response over PVT variations for rising small-signal input step.

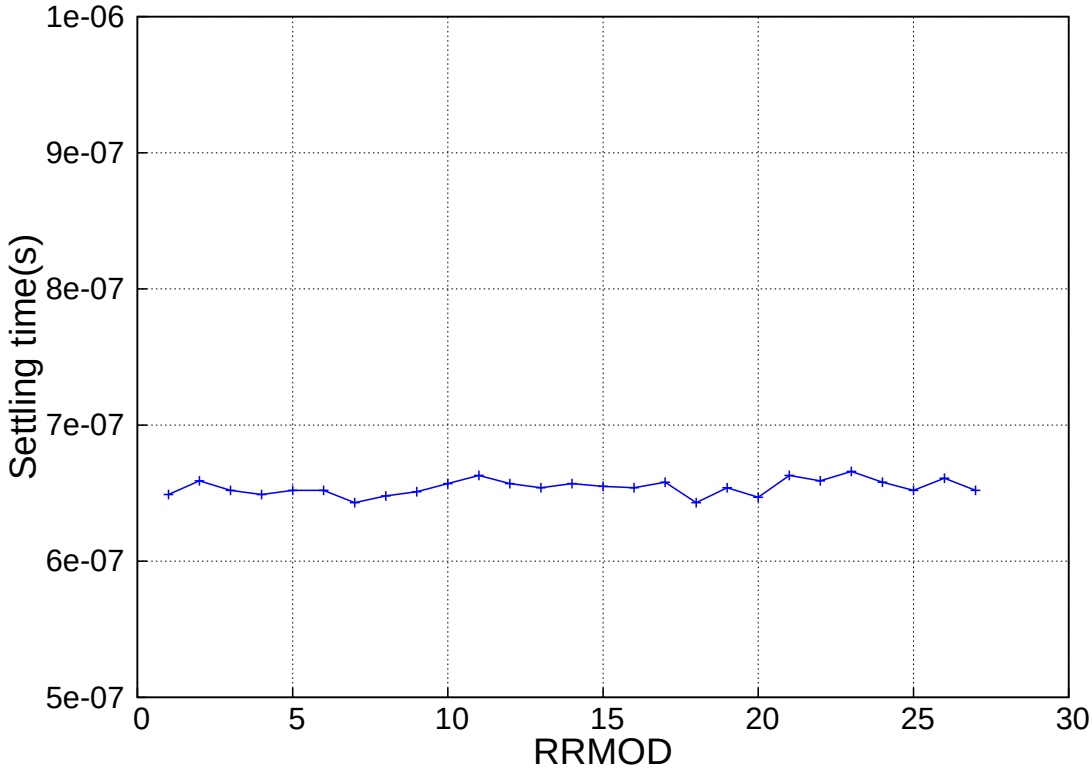


Figure 3.33: Settling time for 18-bit accurate response over PVT variations for falling small-signal input step.

Distortion

Table 3.12 shows the total harmonic distortion seen at the output of the driver for 10 Hz as well as 100 kHz . Simulations are carried out with the presence of the lowpass filters at the output. A peak-to-peak of $0.8V_{dd}$ input signal is used for the simulation. Also, the load nonlinearity is modeled along with 1% mismatch introduced in the output filters. From the table, it is seen that the driver meets the low frequency THD specification while the high frequency linearity is slightly off from the original specifications.

Table 3.12: Total harmonic distortion across PVT variations

RRMOD	THD @ 10 Hz (dB)	THD @ 100 kHz (dB)
1	-123.697	-99.749
2	-125.015	-96.3625
3	-123.906	-101.244
4	-127.45	-99.224
5	-128.898	-98.0279
6	-127.575	-99.431
7	-130.239	-97.4531
8	-131.786	-97.0971
9	-130.378	-97.6143
10	-127.797	-96.7554
11	-129.005	-93.7421
12	-127.745	-98.6105
13	-131.286	-96.6045
14	-132.477	-95.1183
15	-131.21	-97.4628
16	-134.425	-95.5645
17	-135.476	-94.7776
18	-134.721	-96.1787
19	-130.758	-95.2616
20	-132.429	-91.363
21	-129.162	-98.0924
22	-133.109	-96.2561
23	-134.726	-93.788
24	-130.458	-97.5142
25	-135.879	-95.3898
26	-137.576	-94.047
27	-131.143	-96.1339

Offset

To find the output offset of the driver, a 100-run monte carlo simulation with process variation and mismatch is carried out. Table 3.13 shows the simulation results at different V_{DD}. The results show the 3σ number. It is to be noted that the simulation is done using the schematic and not on the extracted netlist as monte carlo simulation on the extracted netlist was extremely resource intensive.

Table 3.13: Output offset across power supply variation

V_{DD}(in V)	Output offset(in mV)
4	1.82
5	2.16
6	1.75

3.7 Conclusions

In this chapter, the specifications chosen for the implementation of the prototype driver is presented. Detailed noise analysis of architectures based on the inverting amplifier configuration with output side filtering are given. Output side filtering is used to remove the trade-off between the distortion and noise performance of such drivers. Additional filtering scheme to reduce the noise contribution from the input and feedback resistors in such architectures is presented. The noise analysis of the architectures with additional filtering is redone. In depth performance comparison between the cascade of inverting amplifiers and the fully-differential amplifier is presented. It is shown that the fully-differential amplifier outperforms the cascade of inverting amplifier in all aspects and is therefore made the choice for the implementation of the prototype driver. The design procedure is dealt with thoroughly. This is followed by simulation results which prove the performance of the design. The simulated

performance summary of the design is as shown in Table 3.14

Table 3.14: Performance summary of the driver

Specification	**Simulated performance**	**Comment**
Offset $< 2.5\,\text{mV}$	$< 2.5\,\text{mV}$	
Gain error $< 5\%$	$< 5\%$	
THD at 10 Hz $<$ -120 dB	-131.2 dB	spec. at nominal condition
THD at 100 kHz $<$ -100 dB	-96.6 dB	spec. at nominal condition
Sampled noise $< 40\,\mu\text{V}$	$< 38.07\,\mu\text{V}$	spec. at nominal condition
18 bit settling in 1 μs	$< 1\mu$s	
$V_{DD} = 5 \pm 1$ V	works satisfactorily	
Temp range -40° to 135°	works satisfactorily	
Power	14.5 mW	at nominal condition

CHAPTER 4

Measurement Results

4.1 Frequency response

Fig. 4.1 shows the setup used to measure the frequency response of the driver amplifier. A single-ended input signal from the signal generator is applied to the driver. The other input of amplifier is held at common-mode voltage. To facilitate this, we have used a dual power supply for the chip. With this arrangement, directly connecting the relevant input terminal to the ground plane will set the necessary common-mode voltage. At the output of the driver, a series combination of 636 Ω in series with 100 pF capacitor is used as the load. The output is fully-differential and to probe the signal a high impedance active differential probe is used. The probed signal is then fed into an oscilloscope to make the measurements. For the measurement of the small-signal frequency response, a 100 mV peak-to-peak signal is used.

The measured frequency response at room temperature and across three different power supplies is as shown in Fig. 4.2. From the response, it can be seen that the gain of the driver is 2. The gain remains flat for frequencies upto 100 kHz and this ensures satisfactory performance of the device over the frequency range of interest. Further, this matches with the simulated results. However, we see that there is high frequency peaking that is unexpected. We expect it to be an artefact of the measurement setup. One possible cause could be that of the board trace inductance interfering with the active probe circuitry. In the current setup, the output traverses through a long trace (with a 0 Ω resistor in the path) before it is picked up by the probe through Berg connectors.

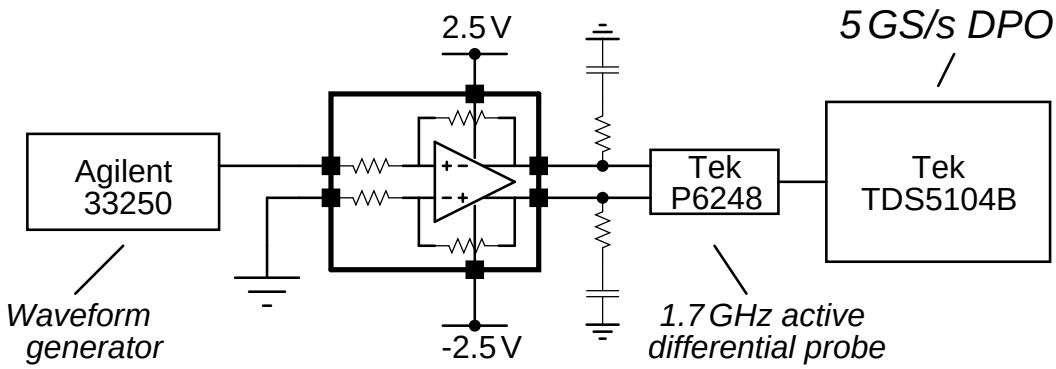


Figure 4.1: Measurement setup used for frequency response.

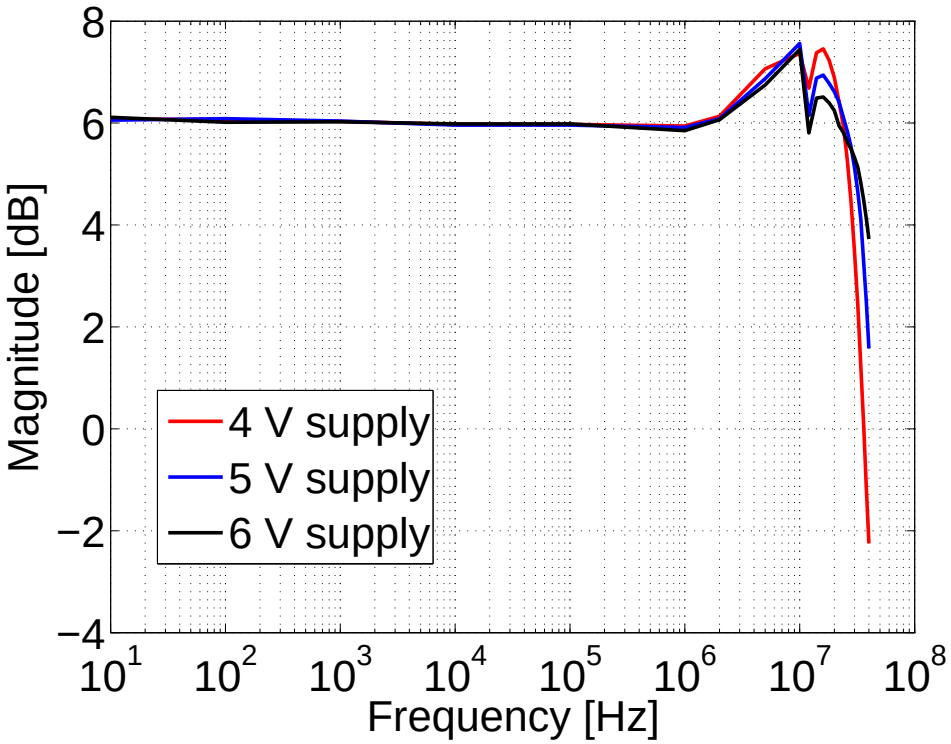


Figure 4.2: Measured small-signal frequency response across different power supplies.

4.2 Output offset

Fig. 4.3 shows the setup used to measure the output offset of the driver amplifier. To measure the output offset, the inputs of the driver are hard connected to the ground plane of the board through 0 Ω resistors. To ensure compatibility with the input common-mode voltage, dual power supplies are used for the measurement. At the output of the driver, a series combination of 500 Ω in se-

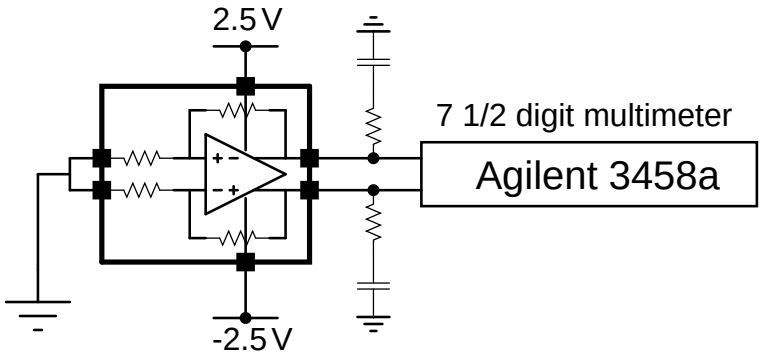


Figure 4.3: Setup used for output offset measurement.

ries with 100 pF capacitor is used as the load. Output pins are accessed on the board with Berg pins. A Berg to Banana adapter cable is used and the signal is fed into a multimeter using Banana connectors for measurement.

Measurements were done across 8 chips. Further, for each of the chips, measurements were done at 3 different power supply voltage settings (4, 5, and 6 V) and 3 different temperature settings (-40°, 25°, and 125° C). The measured output offset was always found to be less than 1.36 mV. This indicates satisfactory performance of the driver in terms of output offset.

4.3 Output noise

Fig. 4.4 shows the setup used to measure the output noise of the driver amplifier. Similar to the offset measurement, the inputs of the driver are hard connected to the ground plane of the board through 0 Ω resistors. To ensure compatibility with the input common-mode voltage, dual power supplies are used for the measurement. To measure the noise, we use the AP2722 audio analyzer from Audio Precision. The input impedance of this analyzer is specified as 100 kΩ ||185 pF. To drive this high capacitive load provided by the analyzer, we use 500 Ω resistors in series with the output.

The analyzer provides some standard filtering options for the measurement of

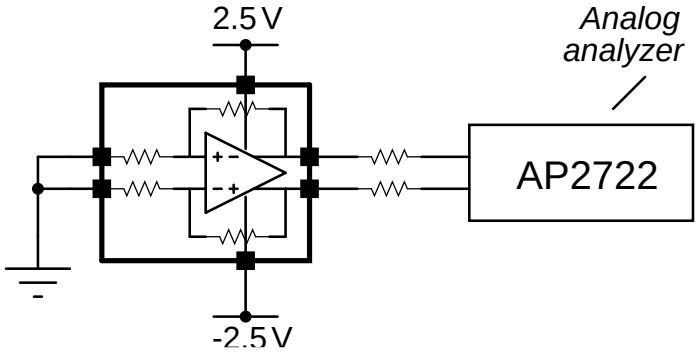


Figure 4.4: Setup used for output noise measurement.

noise. 20 Hz to 80 kHz is the largest bandwidth over which the measurements can be made and is therefore the choice in our measurements. The equivalent circuit is used to simulate the noise for comparison. One important thing that has to be ensured is that the cable carrying the signal from the board to the analyzer should be twisted nicely so that any environmental common-mode noise is rejected completely.

Two measurements are made to find out the contribution from the driver. The first measurement is made using the setup as shown in Fig. 4.4. This measures the noise from driver amplifier along with the noise from measurement equipment. To determine the noise contribution from the measurement equipment, a large capacitor (10 μF) is placed across the input terminals of the analyzer. This filters the noise from the driver almost completely and the measurement reading will correspond to the noise contribution from the measurement equipment alone. The contribution from the measurement equipment is calibrated out to find the exact contribution of the driver.

The simulated and measured noise performance of a driver at three different temperature settings are given in Table 4.1. The simulated and the measured values match closely. The matching seems to be better with increased temperature. The reason for this discrepancy could be due to the die temperature being established to value that is different than the read temperature on the temperature source (especially for lower values).

Table 4.1: Measured noise performance of the driver

Temperature	Measured (μV)	Expected (μV)
-40°	5.61	5.36
25°	6.29	6.12
125°	7.17	7.14

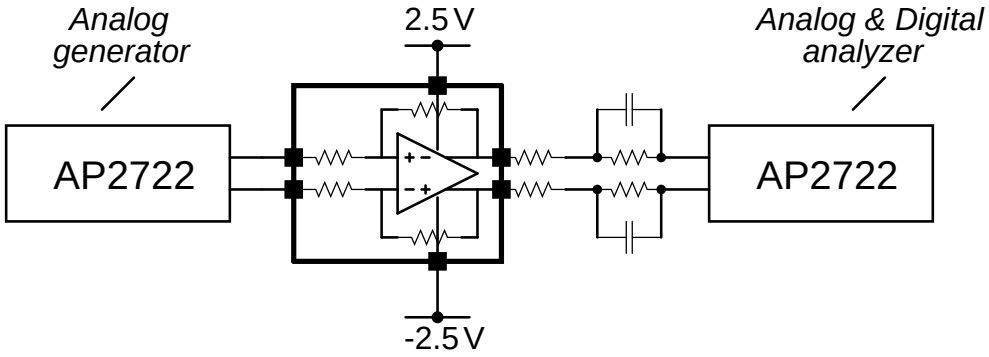


Figure 4.5: Setup used for THD measurement.

4.4 Total harmonic distortion

Fig. 4.5 shows the setup used to measure the distortion at the output of the driver amplifier. The low distortion analog sinewave generator available in AP2722 from Audio Precision is used as the input signal for the measurements. By default, the output common-mode voltage of the sinewave generator is zero. In order to obtain a sine signal with a different common-mode, an extra DC voltage source needs to be used in conjunction with the generator. To reduce the complexity of the test setup, we choose a common-mode voltage of zero by the use of dual power supply.

To measure the distortion in the output signal from the driver, we use the analyer from the same device AP2722. To drive the analyzer without any problems, we use a series resistor of 500 Ω. Internally, a 24-bit $\Delta - \Sigma$ ADC with a sampling rate of 65.536 kS/s is used to measure the frequency response of the output signal. To reduce the nonlinearity introduced by the analyzer itself, we try to reduce the swing of the signal at the input of the analyzer itself by adding

a parallel combination of 180 pF and 100 kΩ in series with the analyzer. This is to mock the input impedance of the analyzer so that the analyer sees only half the signal swing at the output of the driver by voltage division. To further reduce the nonlinearity contribution from the ADC, the internal notch filter that is available in AP2722 is also used. The notch is set at the fundamental frequency itself so that the swing at the input of the ADC is very small. With this setup, the harmonics seen in the signal generator output for a 1.414 V peak signal were below -130 dB.

The THD performance of the driver is measured using this setup. Since the ADC sampling rate is 65.536 kS/s, it is impossible to characterize signals beyond 32.768 kHz with this setup. Since we are interested in finding out the nonlinearity of the amplifier, we can characterize the THD performance upto only 10 kHz (3^{rd} harmonic at 30 kHz).

Table 4.2 shows the strengths of the second and third harmonics at the output with a 4 V peak-to-peak signal at the input. These measurements were made at room temperature with 5 V power supply voltage. The results for three different frequency settings are shown. It is seen that only the second and third harmonics have significant strengths. The THD performance at 300 Hz is ∼118.5 dB . This confirms the satisfactory linearity performance of the driver. Fig. 4.6 shows the spectrum of the output signal measured with this setup. The input signal frequency is 1 kHz. The use of the notch filter can be easily seen. From the spectrum, it is clear that only the second and third harmonics are significant.

Table 4.2: Measured linearity performance of the driver across input frequency

Fund. freq.	Second harmonic (dB)	Third harmonic (dB)
300 Hz	-128	-115.7
1 kHz	-133.65	-116.5
10 kHz	-123.13	-127.5

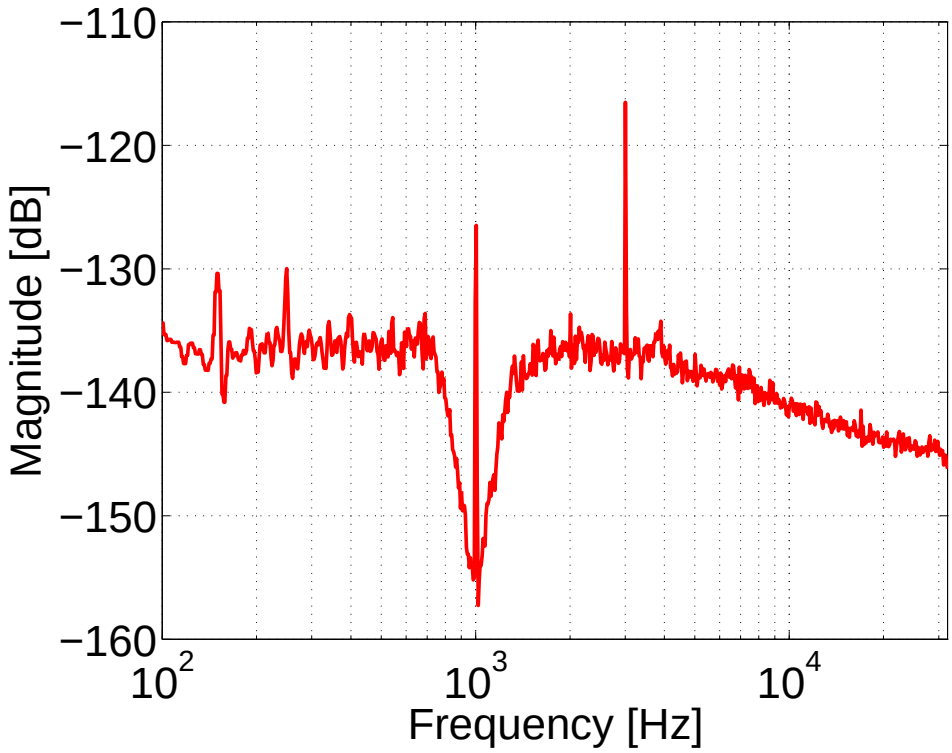


Figure 4.6: Output spectrum with notch filter at the fundamental.

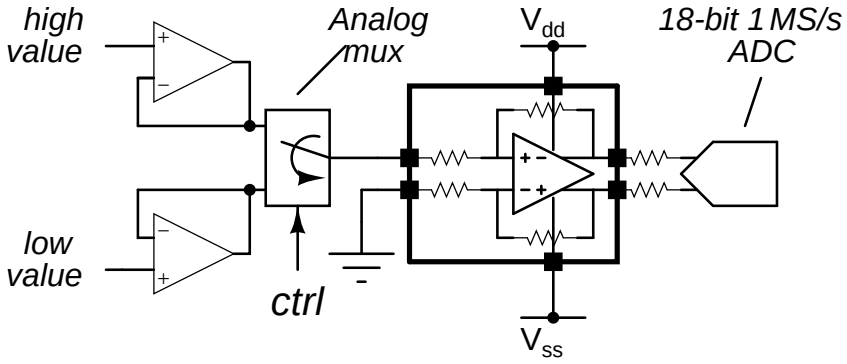


Figure 4.7: Setup used for setting time measurement.

4.5 Step response

Fig. 4.7 shows the setup used to measure the settling time of the driver amplifier. The step input required to excite the amplifier is also created on the board and is shown in the figure. A reference IC is used to the high and low values (using resistive divider) of the step input. These high and low values are buffered using THS4031 opamps. An analog mux TS5A3159 is used to switch between the buffered high and low values to create the step input.

An 18-bit ADC is used to make the measurements. A scheme similar to equivalent time sampling is used. The scheme is explained in detail in [23]. To measure the settling time to 18-bit accuracy, it is seen that the switch used to create the step should have very good isolation between the two channels and the output. This is to ensure that transients due to the load switching does not get coupled to the other channel and thereby reducing the quality of the input step itself. An alternative way to reduce the effect of load switching is to have a replica step generation circuit with the switching happening in the opposite way. With this arrangement, the total load seen by the opamps buffering the high and low values remains constant and eliminates transients due to switching.

The low distortion analog sinewave generator available in AP2722 from Audio Precision is used as the input signal for the measurements. By default, the output common-mode voltage of the sinewave generator is zero. In order to obtain a sine signal with a different common-mode, an extra DC voltage source needs to be used in conjunction with the generator. To reduce the complexity of the test setup, we choose a common-mode voltage of zero by the use of dual power supply.

In our setup we use ADS8881 for the measurements. The reference voltage of the ADC is set at 4 V. The ADC has an ESD diode between the input pins and the reference pin. Therefore to not turn on the ESD diode, the voltage on the input terminals cannote exceed 4 V. Therefore we choose a 1 V input step with suitable common-mode such that the voltage on the input terminals are well below 4 V even in the case of overshoot. The results for 0.1% and 0.01% accurate settling times are measured for three different temperature settings. Table 4.3 shows the details. Fig. 4.8 shows the corresponding waveforms.

Table 4.3: Measured settling times across temperature

Accuracy	Cold	Room	Hot
0.1%	160 ns	160 ns	200 ns
0.01%	240 ns	280 ns	360 ns

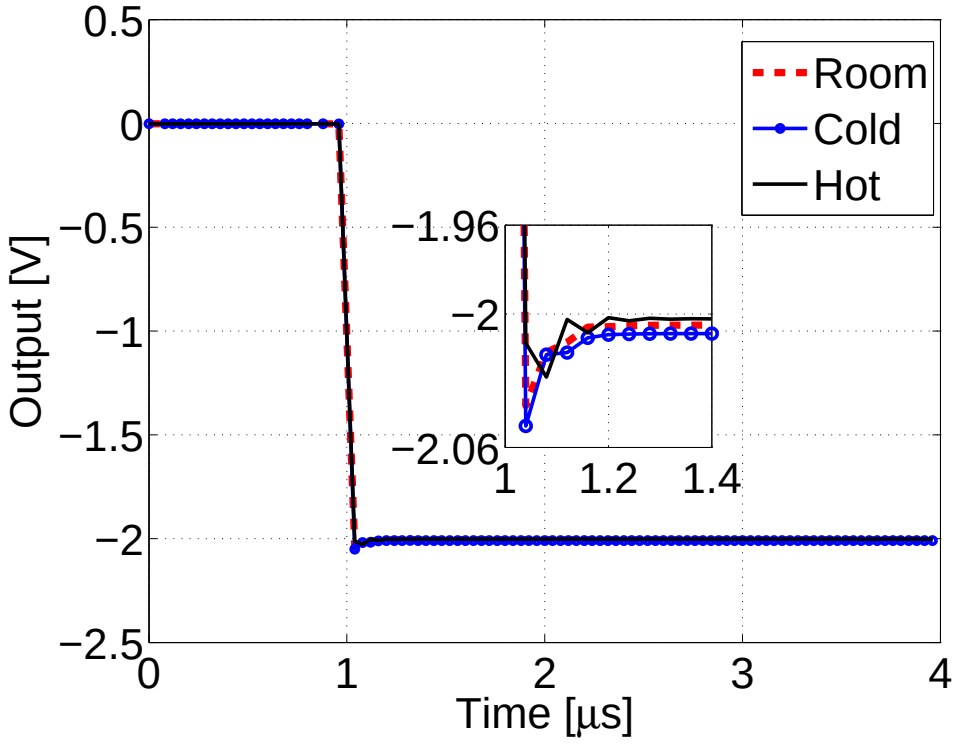


Figure 4.8: Measured response of the driver for 1 V input step.

CHAPTER 5

A Model-Agnostic Technique for Simulating Per-Element Distortion Contributions

5.1 Introduction

Distortion due to nonlinearity and noise due to inherent randomness are the most important disturbances in signal processing circuits. Circuits must be designed such that these are kept below certain specified levels. Knowing individual contributions of these disturbances from different elements to the overall output is useful for optimizing circuits. Determining noise contributions from individual elements is routinely done in standard circuit simulators. For distortion though, such facility is not usually available. The total output distortion can however be determined easily by running a transient or periodic steady state analysis with nonlinear device models.

To determine the distortion or noise contribution of each element, we need to know the equivalent nonlinear distortion or noise source in that element, and the transfer function from that source to the output. The difficulty in resolving individual distortion contributions is that, unlike in the case of noise, it is not straightforward to calculate the equivalent distortion source of the element. If the nonlinear device were described by a Taylor or Volterra series in the port variables, the nonlinear source would consist of the higher order terms in the series. In practice, the device models are a lot more complicated and not described in simple closed form. Also, unlike noise, equivalent distortion source strongly depends on the signal levels in the element.

We present a technique that bypasses both these steps of explicitly computing the distortion source of the device or the transfer functions to the output [24]. To do this, we first simulate the output distortion of the original circuit. We then replace the element whose contribution we want to determine by another element whose operating point and first order terms are exactly the same as the original, but whose nonlinear terms are changed by known factors. We show that such a device can be constructed *based on elementary circuit theory and without any knowledge of the device model*. We simulate the output distortion of the modified circuit as many times as there are significant nonlinear terms, with the scaling factors of nonlinear terms changed each time. The relationship between the output distortion in these simulations and distortion contributions from different nonlinear terms is a set of linear equations whose coefficients are the (known) scaling factors of nonlinear terms in the modified element. We extract the contributions from different terms by solving this set of equations. For weakly nonlinear circuits, the extracted contribution of an element is the reduction in distortion when nonlinear terms disappear from that element. For circuits with high distortion, the extracted contributions are sensitivities of output distortion to nonlinear terms of the element.

In the rest of this section, we first briefly discuss techniques which are frequently used by designers or have been published in the literature for determining distortion contributions from different elements of a circuit and then provide an outline for the rest of the chapter.

In case of a cascade of open loop stages, the difference in distortion between the input and output of a stage can be attributed to that stage. Loading of one stage by another makes it harder to isolate contributions from a stage. For closed loop systems, this technique cannot be used. Alternatively, distortion contribution from an element can be determined by replacing it by its linear equivalent (e.g. opamp by a voltage controlled voltage source) and the observing the change

in distortion. This typically oversimplifies the circuit and misses many details such as loading.

Using the probing and nonlinear current injection method (also called the perturbation method) described in [25], and suitable Taylor or Volterra series models for nonlinear elements, numerical values or symbolic expressions for output distortion components can be derived (e.g. [26, 27, 28, 17, 29]). The distortion contribution of an element is obtained by selectively injecting nonlinear currents or by identifying terms containing constants belonging to that element. Key difficulties here are finding suitable models and extracting numerical values of model parameters (which has to be manually carried out at the relevant operating point). Algebraic complexity is an additional difficulty with symbolic calculations.

[30] circumvents the extraction of nonlinear device models by using an appropriate multi-sine excitation with which one can determine the equivalent additional distortion source of each element. This is essentially a missing tone test, and it may not be easy to relate this to conventional single-tone harmonic distortion and two-tone intermodulation distortion tests. It also involves choosing an appropriate multi-tone input signal which entails additional labor.

[31] describes an efficient technique that finds the nonlinear contribution of an element by subtracting the operating point and first order terms from the nonlinear function describing the element. But, this algorithm has to be coded into the simulator and cannot be used by a circuit designer running a conventional SPICE-like simulator.

Recent versions of Virtuoso Spectre ([32, 33]) provide small signal distortion summary based on the perturbation method and small signal transfer functions around a dc or periodic operating point. The contribution of each element is calculated as the output distortion of the circuit when only that element is nonlinear. Consequently, distortion arising from interaction between different

nonlinear elements are not identified in per-element contributions.

Compared to these, the proposed technique eliminates the need for symbolic analysis or model (and parameter) extraction, does not oversimplify or otherwise alter the circuit to first order, can identify contributions arising from interaction between nonlinearities of different elements, and can be run on a conventional SPICE-like simulator. All these come at the expense of having to run multiple simulations.

In the next section, we show how to synthesize a new nonlinear element which has the same operating point and linear characteristics as a given element, but different nonlinear characteristics. We start with the simplest realization of such an element, discuss its limitations, and describe a more elaborate realization which is usable in all cases. Such nonlinearity scaling is illustrated with an example in Section 5.3. In Section 5.4, additional scaling factors that come into play when the nonlinear element is embedded in a circuit are discussed. In Section 5.5, we show how to use this element with scalable nonlinear terms to obtain individual distortion contributions. The interpretation of per-element distortion contributions and its contrasting features with noise are discussed in Section 5.6. In Section 5.7 the proposed technique is verified by applying it to several examples. Section 5.8 compares our technique to other published techniques for computing per-element distortion contributions. Section 5.9 concludes the chapter.

5.2 Obtaining a device with scaled nonlinearity

5.2.1 Scaling nonlinearity using two copies of the element

For simplicity, the principle is first illustrated with a memoryless one-port element. Fig. 5.1(a) shows a nonlinear element E with a current-voltage relation-

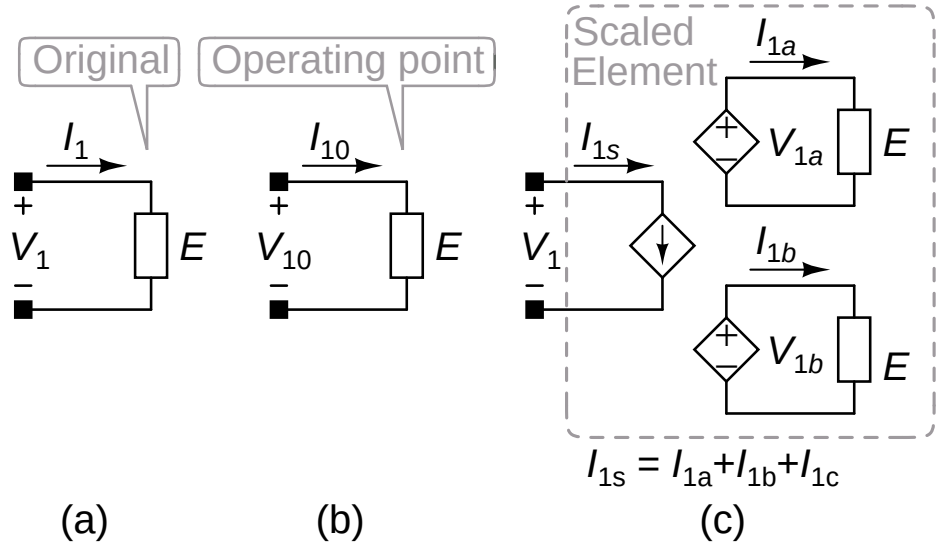


Figure 5.1: (a) Nonlinear one-port element E, (b) Operating point, (c) Nonlinear one-port element constructed from two instances of E driven by V_{1a} and V_{1b}.

ship $I_1 = f(V_1)$. Fig. 5.1(b) shows the same element E at a certain operating point (V_{10}, I_{10}). Defining incremental voltage v_1 and current i_1 respectively as $v_1 = V_1 - V_{10}$ and $i_1 = I_1 - I_{10}$ and expanding the nonlinear relationship in a Taylor series around the operating point, we get

$$I_1 = \underbrace{f(V_{10})}_{I_{10}} + \underbrace{f^{(1)}_{V_{10}} v_1 + \frac{f^{(2)}_{V_{10}}}{2!} v_1^2 + \frac{f^{(3)}_{V_{10}}}{3!} v_1^3 + \ldots}_{i_1} \tag{5.1}$$

where $f^{(k)}_{V_{10}}$ is the k^{th} derivative of f evaluated at the operating point V_{10}. The first term is the operating point, the second term is the linear part, and successive terms are nonlinearities of corresponding orders.

Now consider the one-port in Fig. 5.1(c) which is constructed from two instances of elements E driven with voltages V_{1a} and V_{1b}. These voltages are related to V_1, the voltage across the one-port, as follows:

$$V_{1a} = V_{10} + a_1 (V_1 - V_{10}), \quad V_{1b} = V_{10} + (1 - a_1)(V_1 - V_{10}) \tag{5.2}$$

where a_1 is a scaling factor. In other words, the two copies of E experience

differently scaled versions of the incremental voltage $v_1 = V_1 - V_{10}$ around the same operating point (V_{10}) as the original. The current I_{1s} in the new one-port element is defined as $I_{1s} = I_{1a} + I_{1b} - I_{10}$. Using (5.1) and (5.2), we get the Taylor series representation for I_{1s}.

$$\begin{aligned} I_{1s} &= f(V_{10}) + f^{(1)}_{V_{10}} v_1 + \left(a_1^2 + (1-a_1)^2\right) \frac{f^{(2)}_{V_{10}}}{2!} v_1^2 \\ &\quad + \left(a_1^3 + (1-a_1)^3\right) \frac{f^{(3)}_{V_{10}}}{3!} v_1^3 + \ldots \end{aligned} \tag{5.3}$$

It is clear from (5.1) and (5.3) that I_{1s}, the current in the nonlinear one-port element in Fig. 5.1(c), has the same operating point and linear terms as I_1 in the original one-port element in Fig. 5.1(a), but scaled nonlinear terms. The N^{th} order term in the series is scaled by $\alpha^{(N)} = a_1^N + (1-a_1)^N$. The scaled element reduces to the original when $\alpha^{(N)} = 1$ for all N ($a_1 = 0$ or $a_1 = 1$).

This reasoning can be easily extended to a two-port element. Fig. 5.2(a) shows a two-port element E with voltages V_1, V_2 and currents I_1, I_2. Fig. 5.2(b) shows the operating point condition. Fig. 5.2(c) shows a new two-port network constructed from two instances of E which receive scaled versions of the incremental voltages above the operating point. The voltages applied to the copies of the two-port are given by the following relationships:

$$\begin{aligned} V_{1a} &= V_{10} + a_1 (V_1 - V_{10}), \quad V_{1b} = V_{10} + (1-a_1)(V_1 - V_{10}) \\ V_{2a} &= V_{20} + a_2 (V_2 - V_{20}), \quad V_{2b} = V_{20} + (1-a_2)(V_2 - V_{20}) \end{aligned} \tag{5.4}$$

The currents $I_{1a,1b}$ and $I_{2a,2b}$ in the two networks are combined with the operating point currents I_{10} and I_{20} to obtain I_{1s} and I_{2s} in Fig. 5.2(c). These are given by

$$I_{1s} = I_{1a} + I_{1b} - I_{10}, \quad I_{2s} = I_{2a} + I_{2b} - I_{20} \tag{5.5}$$

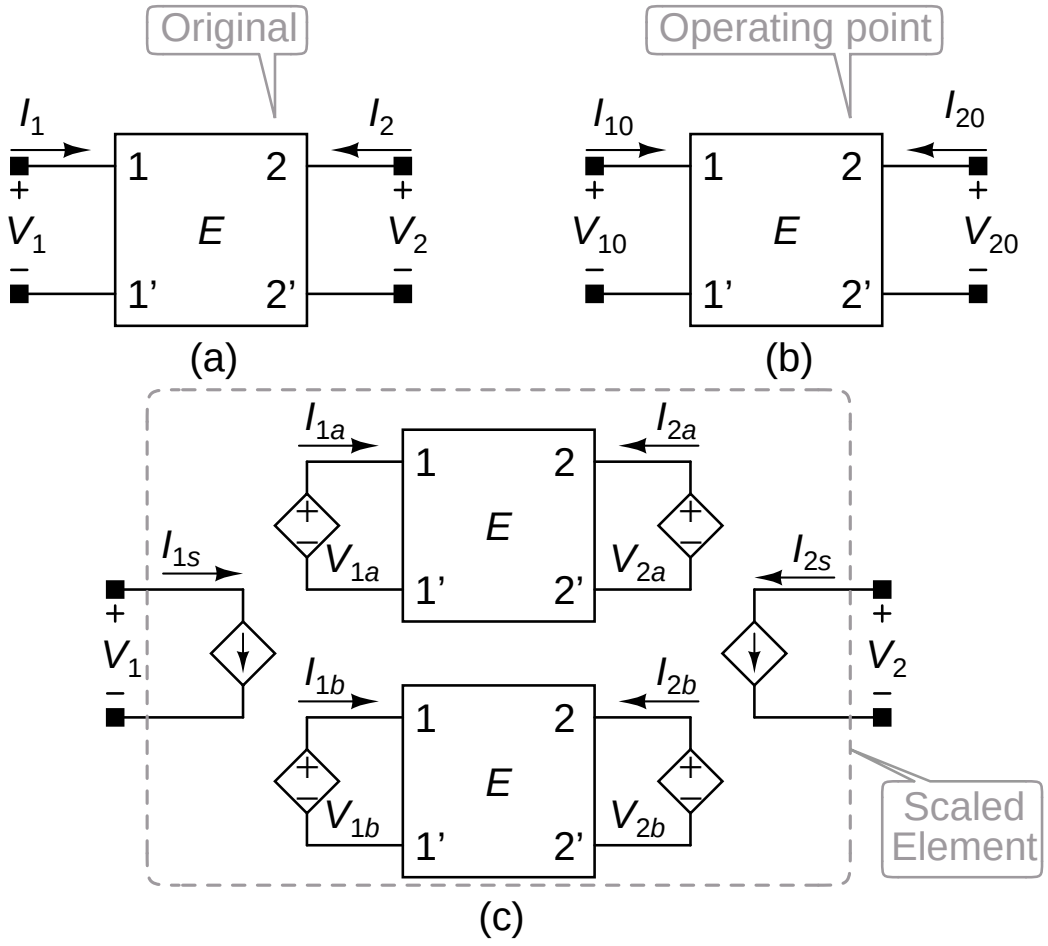


Figure 5.2: (a) Nonlinear two-port element E, (b) Operating point, (c) Nonlinear two-port constructed from two instances of E driven by $V_{1a,2a}$ and $V_{1b,2b}$.

Using similar reasoning as with the one-port, it is clear that I_{1s} and I_{2s} of the composite two-port network in Fig. 5.2(c) consist of the same operating point and first order terms as I_1 and I_2 in the original two-port in Fig. 5.2(a), but have scaled higher order terms. Table 5.1 lists the scaling factors for second and third order terms in I_1 and I_2. The pattern for higher order terms is obvious. Different nonlinear terms of a given order are scaled differently, ensuring that their contributions can be distinguished from one another.

If we use the same scaling factor a_1 for both ports instead of different factors a_1, a_2, the scaling factor for all nonlinear terms of a given order will be the same as in the one port case. These are also shown in the table. In general, the scaling factor for the N^{th} order term is $\alpha^{(N)} = a_1^N + (1 - a_1)^N$.

Table 5.1: Scaling factors for the two-port of Fig. 5.2(c)

Second order	Differently scaled ports	Identically scaled ports
v_1^2	$\alpha^{(2,0)} = a_1^2 + (1-a_1)^2$	$\alpha^{(2)} = a_1^2 + (1-a_1)^2$
$v_1 v_2$	$\alpha^{(1,1)} = a_1 a_2 + (1-a_1)(1-a_2)$	
v_2^2	$\alpha^{(0,2)} = a_2^2 + (1-a_2)^2$	
Third order		
v_1^3	$\alpha^{(3,0)} = a_1^3 + (1-a_1)^3$	$\alpha^{(3)} = a_1^3 + (1-a_1)^3$
$v_1^2 v_2$	$\alpha^{(2,1)} = a_1^2 a_2 + (1-a_1)^2(1-a_2)$	
$v_1 v_2^2$	$\alpha^{(1,2)} = a_1 a_2^2 + (1-a_1)(1-a_2)^2$	
v_2^3	$\alpha^{(0,3)} = a_2^3 + (1-a_2)^3$	

The concept can be easily generalized to an M-port element. In an M-port element, we need M scaling factors $a_1, \ldots a_M$ to scale the incremental port voltages $v_1, \ldots v_M$. Each N^{th} order nonlinear term in the scaled network will be of the form $\prod_{k=1}^{M} v_k^{l_k}$ where $0 \leq l_k \leq N$ and $\sum_{k=1}^{M} l_k = N$. The scaling factor for this term would be $\alpha^{(l_1,\ldots,l_M)} = \prod_{k=1}^{M} a_k^{l_k} + \prod_{k=1}^{M}(1-a_k)^{l_k}$. If all ports are scaled by the same factor a_1, the scaling factor for all N^{th} order terms would be $\alpha^{(N)} = a_1^N + (1-a_1)^N$.

5.2.2 Dependence of coefficients under simultaneous presence of both even and odd order nonlinearities

The scaling factors $\alpha^{(k)}$ for k^{th} order nonlinear term in the scaled one-port of Fig. 5.1(c) are given below for $1 \leq k \leq N_e + 1$. N_e is even.

$$
\begin{aligned}
\alpha^{(1)} &= 1 \\
\alpha^{(2)} &= a_1^2 + (1-a_1)^2 \\
&= 2a_1^2 - 2a_1 + 1 \\
\alpha^{(3)} &= a_1^3 + (1-a_1)^3 \\
&= 3a_1^2 - 3a_1 + 1
\end{aligned}
\qquad
\begin{aligned}
\alpha^{(N_e)} &= a_1^{N_e} + (1-a_1)^{N_e} \\
&= 2a_1^{N_e} - N_e a_1^{N_e-1} + \ldots \\
& \\
\alpha^{(N_e+1)} &= a_1^{N_e+1} + (1-a_1)^{N_e+1} \\
&= (N_e+1)a_1^{N_e} - \frac{(N_e+1)N_e}{2} a_1^{N_e-1} + \ldots \\
&= \frac{N_e+1}{2}\left(2a_1^{N_e} - N_e a_1^{N_e-1}\right) + \ldots
\end{aligned}
$$

In the expression for $\alpha^{(3)}$, a_1^3 terms cancel out and the highest power term is a_1^2. Also, the terms containing a_1^2 and a_1 are in the same proportion in $\alpha^{(3)}$ and $\alpha^{(2)}$. By inspection, it is clear that $\alpha^{(3)} = 1.5\alpha^{(2)} - 0.5\alpha^{(1)}$. Similarly, for any even N_e, the highest power in both $\alpha^{(N_e+1)}$ and $\alpha^{(N_e)}$ will be $a_1^{N_e}$ because $a_1^{N_e+1}$ terms cancel out in the former. Again, the terms containing $a_1^{N_e}$ and $a_1^{N_e-1}$ are in the same proportion in $\alpha^{(N_e+1)}$ and $\alpha^{(N_e)}$. There is a similar dependence between lower power terms of $\alpha^{(N_e+1)}$ and $\alpha^{(N_e)}$. Therefore, $\alpha^{(N_e+1)}$ can be written as a linear combination of $\{\alpha^{(N_e)}, \alpha^{(N_e-1)}, \ldots, \alpha^{(2)}, \alpha^{(1)}\}$. This causes the linear equations that will be set up (described in the next section) to extract the contribution of the nonlinear element to be linearly dependent and consequently unsolvable. Therefore, the composite element realized using two copies of the original element as shown in Fig. 5.1 or 5.2, though it scales the nonlinear terms in a predictable and distinct manner, cannot be used when the nonlinear element has terms with both an even power N_e and the next odd power $N_e + 1$. It can be used when only odd or only even nonlinear terms are present.

5.2.3 Scaling nonlinearity using three copies

Dependence between scaling factors can be eliminated by constructing the composite element using three copies of the original element. Fig. 5.3(c) shows a composite one-port network so constructed. The three copies in the composite one-port element are driven by voltages V_{1a}, V_{1b}, and V_{1c} as defined below ($v_1 = V_1 - V_{10}$):

$$V_{1a} = V_{10} + a_1 v_1, \quad V_{1b} = V_{10} + b_1 v_1, \quad V_{1c} = V_{10} + c_1 v_1 \tag{5.6}$$

The scaling factors a_1, b_1, and c_1 are chosen such that their sum is unity. The current I_{1s} in the new one-port is defined as

$$I_{1s} = I_{1a} + I_{1b} + I_{1c} - 2I_{10} \tag{5.7}$$

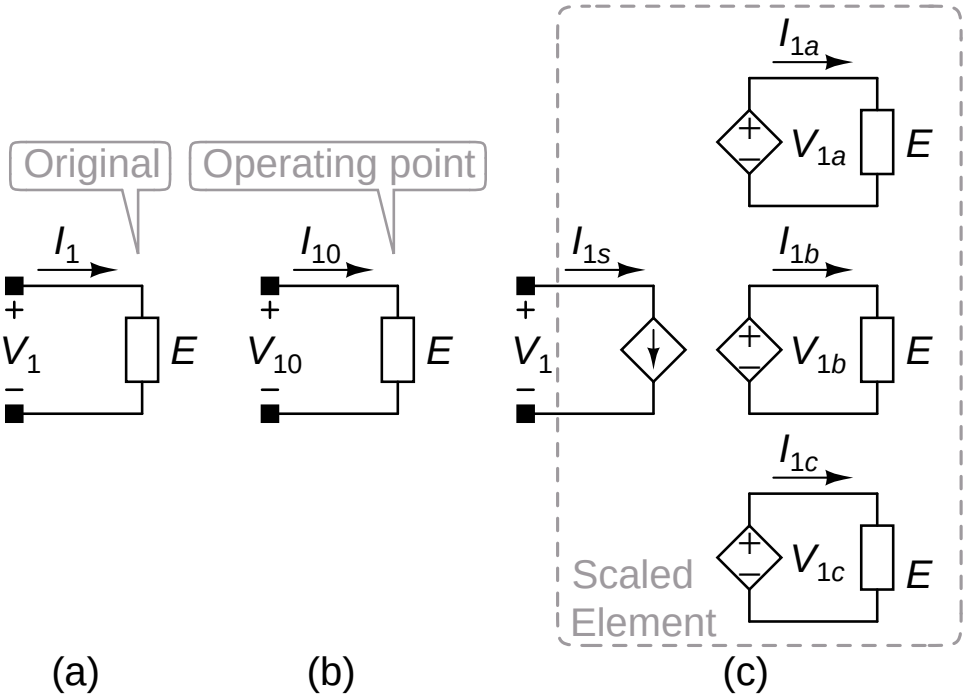


Figure 5.3: (a) Nonlinear one-port element E, (b) Operating point, (c) Nonlinear one-port element constructed from three instances of E driven by V_{1a}, V_{1b}, and V_{1c}.

Summing the three individual one-port currents and subtracting twice the operating point current ensures that the operating point of the new one-port element is exactly the same as that of the original. The sum of scaling factors being unity ensures that the new one-port element has exactly the same first order behavior as the original. The scaling factor for the N^{th} order term is given by $\alpha^{(N)} = a_1^N + b_1^N + c_1^N$. These scaling factors can be chosen to be independent for all N.

Generalization to two or more ports is straightforward. An M-port element with scaled nonlinearity and independent scaling factors can be similarly constructed using three copies of the original M-port. For port k, the scaling factors for the three copies would be a_k, b_k, c_k with $a_k + b_k + c_k = 1$. The scaling factor for N^{th} order nonlinear term of the form $\prod_{k=1}^{M} v_k^{l_k}$ ($0 \leq l_k \leq N$ and $\sum_{k=1}^{M} l_k = N$) would be $\alpha^{(l_1,\ldots,l_M)} = \prod_{k=1}^{M} a_k^{l_k} + \prod_{k=1}^{M} b_k^{l_k} + \prod_{k=1}^{M} c_k^{l_k}$. As before, scaling factors

for all ports can be chosen to be identical ($a_k = a, b_k = b, c_k = c$ for all k), if one is not interested in distinguishing between different nonlinear terms of each order. In this case, all N^{th} order terms would be scaled by $\alpha^{(N)} = a_1^N + b_1^N + c_1^N$.

5.2.4 Generalization to nonlinearity with memory

Memoryless nonlinear elements are chosen above for simplicity, however, the method is equally applicable to nonlinearity with memory. Such elements are described using a Volterra series, which is similar in spirit to the Taylor series. Instead of the k^{th} order term containing v_1^k as in the latter, the former has k integrals under which v_1 is time shifted and multiplied k times. The first and second order terms in Taylor and Volterra series are shown below for illustration.

$$\begin{aligned} f_{V_{10}}^{(1)} v_1 &\leftrightarrow \int h_{V_{10}}^{(1)}(\tau_1)\, v_1(t-\tau_1) d\tau_1 \\ \frac{f_{V_{10}}^{(2)}}{2!} v_1^2 &\leftrightarrow \iint h_{V_{10}}^{(2)}(\tau_1, \tau_2)\, v_1(t-\tau_1) v_1(t-\tau_2) d\tau_2 d\tau_1 \end{aligned} \tag{5.8}$$

$h_{V_{10}}^{(1)}$ is the first order Volterra kernel (impulse response of the linearized element) and $h_{V_{10}}^{(2)}$ is the second order Volterra kernel, both evaluated at the operating point V_{10}. The pattern continues for higher order terms.

Though the terms in the series expansion appear more complicated, it must be noted that v_1 appears only once under the integral (a linear operation) in the first order term, it is multiplied by itself under the integral in the second order term and so on. Therefore, it is easy to see that, when three such series in which the incremental voltage v_1 is scaled by a_1, b_1, and c_1 respectively (with $a_1 + b_1 + c_1 = 1$) are added together, the first order term is retained as is, the second order term is scaled by $a_1^2 + b_1^2 + c_1^2$ and so on. Generalization to more ports is similar to earlier cases. Therefore the proposed technique for scaling nonlinearity works equally well for nonlinear elements with memory.

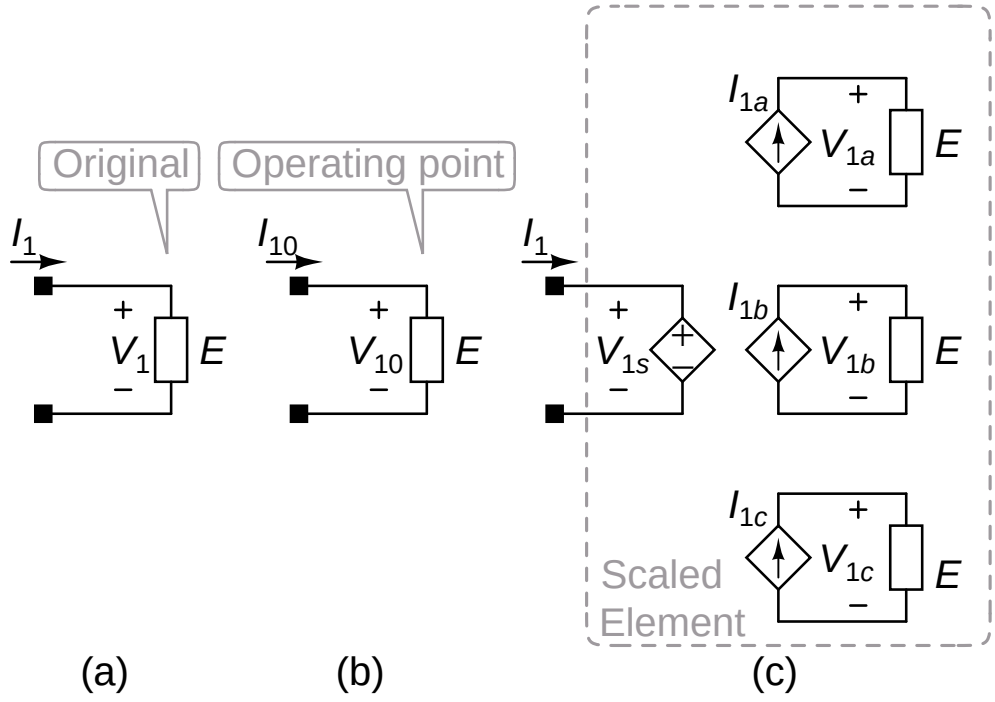


Figure 5.4: Scaling of the Nonlinear one-port element E in impedance form. (a) Nonlinear element E (b) Operating point, (c) Nonlinear one-port element constructed from three instances of E driven by I_{1a}, I_{1b}, and I_{1c}.

5.2.5 Generalization to other representations

In the description above, the admittance form (current as a function of voltage) has been used. This is the most convenient form for frequently used nonlinear elements such as the MOS or bipolar transistor and diodes. Nonlinearity scaling can equally well be accomplished in impedance form. For this, the voltage controlled voltage sources used to apply port voltages to the copies of the element in Fig. 5.3(c) are replaced by current controlled current sources to apply port currents. The current controlled current source that sets the port current in Fig. 5.3(c) is replaced by a voltage controlled voltage source that sets the port voltage. The controlled sources are defined as in (5.6) with the roles of voltage and current interchanged. This representation may sometimes be necessary, for instance, with inductors. Generalizing further, a multi-port network could have some or all ports driven by current sources instead of voltage sources.

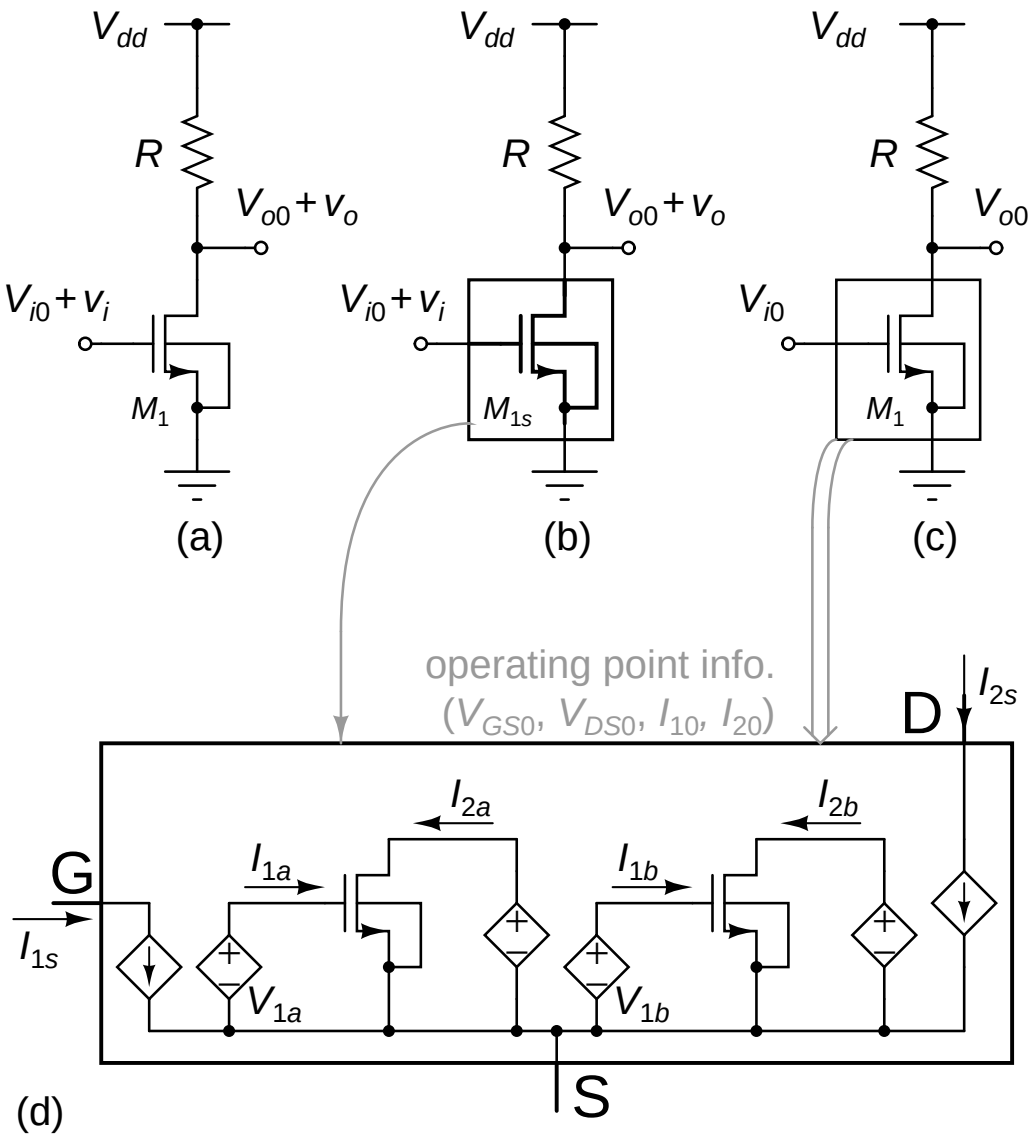


Figure 5.5: (a) Common source amplifier, (b) With M_1 replaced by its scaled version M_{1s}, (c) Amplifier in its quiescent condition, (d) Scaled transistor.

5.3 Verification of nonlinearity scaling

Nonlinearity scaling is illustrated using the common source amplifier circuit in Fig. 5.5(a). It has a single nonlinear element M_1. This circuit is simulated to determine the contribution from the first five terms of its Taylor series. The input signal is a single sinusoid whose amplitude is such that the dominant contribution to the N^{th} harmonic is from the N^{th} order nonlinear term, i.e. the transistor is in the weakly nonlinear regime. In Fig. 5.5(b), the transistor M_1 is replaced

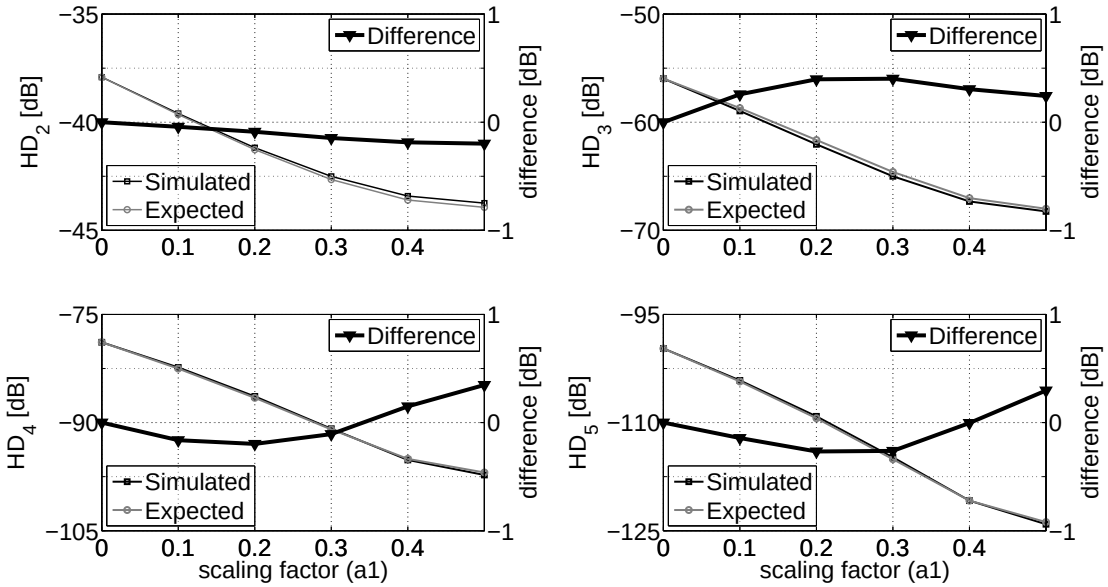


Figure 5.6: Illustration of nonlinearity scaling. Simulated values are distortion components in Fig. 5.5(b) for different scaling factors of M_{1s}. Expected values are distortion in Fig. 5.5(a) multiplied by expected scaling factors. Difference between simulated and expected values are shown in thick black lines against y-axes on the right.

by its scaled version M_{1s}. Fig. 5.5(c) shows the amplifier in its quiescent condition. The scaled transistor M_{1s} is shown in Fig. 5.5(d). For simplicity, only two copies are used as in Fig. 5.2. Also, since the bulk is tied to source in Fig. 5.5(a), the transistor is treated as a three terminal two-port element instead of a four terminal three-port element. The two ports (gate-source and drain-source) use identical scaling factors a_1. The controlled sources in the scaled transistor use the operating point information from Fig. 5.5(c). The N^{th} harmonic in Fig. 5.5(b) is expected to be $\alpha^{(N)} = a_1^N + (1 - a_1)^N$ times the N^{th} harmonic in Fig. 5.5(a). Fig. 5.6 shows the simulated and expected values of the second, third, fourth, and fifth harmonics in Fig. 5.5(b). The harmonics scale as expected. The simulated and expected values are very close to each other. The difference between them is plotted against expanded y-axis on the right, and is seen to be smaller than 0.5 dB in all cases. The fundamental component (not shown here) is seen to be constant with scaling factor a_1. These results validate the scaling technique.

5.4 Scaling of terms with embedded elements

Table 5.2: Scaling factors for an embedded nonlinear one-port element

Order	Scaling factor	Interacting terms	Additional factors from interaction
2	$\alpha^{(2)}$	—	—
3	$\alpha^{(3)}$	$(2,1)^{(2)}$	$\alpha^{(2)^2}$
4	$\alpha^{(4)}$	$(3,1)^{(2)}$, $(2,1,1)^{(3)}$, $(2,2)^{(2)}$	$\alpha^{(2)}\alpha^{(3)}$, $\alpha^{(2)^3}$
5	$\alpha^{(5)}$	$(4,1)^{(2)}$, $(2,1,1,1)^{(4)}$, $(3,1,1)^{(3)}$, $(3,2)^{(2)}$, $(2,2,1)^{(3)}$	$\alpha^{(2)}\alpha^{(4)}$, $\alpha^{(3)^2}$, $\alpha^{(2)^2}\alpha^{(3)}$

Table 5.3: Scaling factors for an embedded nonlinear two-port element

Order	Scaling factor	Interacting terms	Additional factors from interaction
2	$\alpha^{(2,0)}, \alpha^{(1,1)}, \alpha^{(0,2)}$	—	—
3	$\alpha^{(3,0)}, \alpha^{(2,1)}$, $\alpha^{(1,2)}, \alpha^{(0,3)}$	$(2,1)^{(2)}$	$\alpha^{(2,0)^2}$, $\alpha^{(0,2)^2}$, $\alpha^{(1,1)^2}, \alpha^{(0,2)}\alpha^{(2,0)}$, $\alpha^{(2,0)}\alpha^{(1,1)}$, $\alpha^{(1,1)}\alpha^{(0,2)}$

The previous section described a technique to alter the nonlinear terms of an element by known factors. If a nonlinear element is driven by an independent voltage source, the k^{th} order nonlinear term in the current is scaled by $\alpha^{(k)}$. When the element is embedded in a network, the voltage across the element is influenced by the current in the element, which in turn is a nonlinear function of the voltage across it. This interaction results in additional scaling factors for terms of each power in the nonlinear function. It is possible to derive these scaling factors by going through iterative steps of analyzing the effect of nonlinearity of an element, e.g., by the probing and nonlinear current injection method in [25]. Due to lack of space, we only give an intuitive justification and the final results. Table 5.2 summarizes the results for a one-port element. The second and third columns show the order of terms and corresponding scaling factors arising from scaling the nonlinearity. The fourth column shows possi-

ble interactions between lower order terms which can give rise to terms of a given order. For instance, a third order term (v^3) can be generated by a second order interaction (= number of terms being multiplied) of second and first order terms ($v^2 \times v$). This is indicated as $(2,1)^{(2)}$. The number in the superscript indicates the order of interaction and the numbers in the lower parentheses indicate the order of interacting terms. The scaling factor for this term would be the product of scaling factors for each of the interacting terms and the scaling factor for the order of interaction, i.e. $\alpha^{(2)} \times \alpha^{(1)} \times \alpha^{(2)} = \alpha^{(2)^2}$. By construction, $\alpha^{(1)} = 1$. Different interactions can give rise to the same scaling factor, e.g., $(3,1)^{(2)}$ and $(2,1,1)^{(3)}$ both result in $\alpha^{(2)}\alpha^{(3)}$. Since we are dealing with weakly nonlinear systems, a component arising from interaction between two or more higher order terms would be weaker than that arising from interaction between first order terms and a single higher order term. The former are shown in gray in Table 5.2 and can usually be ignored.

Table 5.3 shows the scaling factors for the two-port case. They are many more in number, but conceptually similar to those for a one-port element. In place of $\alpha^{(2)^2} = \alpha^{(2)} \times \alpha^{(2)}$ for the third order case we have all possible pairwise products of $\{\alpha^{(2,0)}, \alpha^{(1,1)}, \alpha^{(0,2)}\}$. As usual, if both ports of a two-port are scaled identically, the scaling factors are same as in the one-port case. These additional factors have to be accounted for when extracting the contributions (described in the next section). Depending on the circuit configuration, some of the interaction terms maybe absent.

5.5 Determining an element's contribution

Fig. 5.7(a) shows a circuit with a nonlinear element E whose contribution to distortion has to be determined. For clarity of discussion, we consider a single input voltage v_s, an output voltage v_o, and an element E which has nonlinear

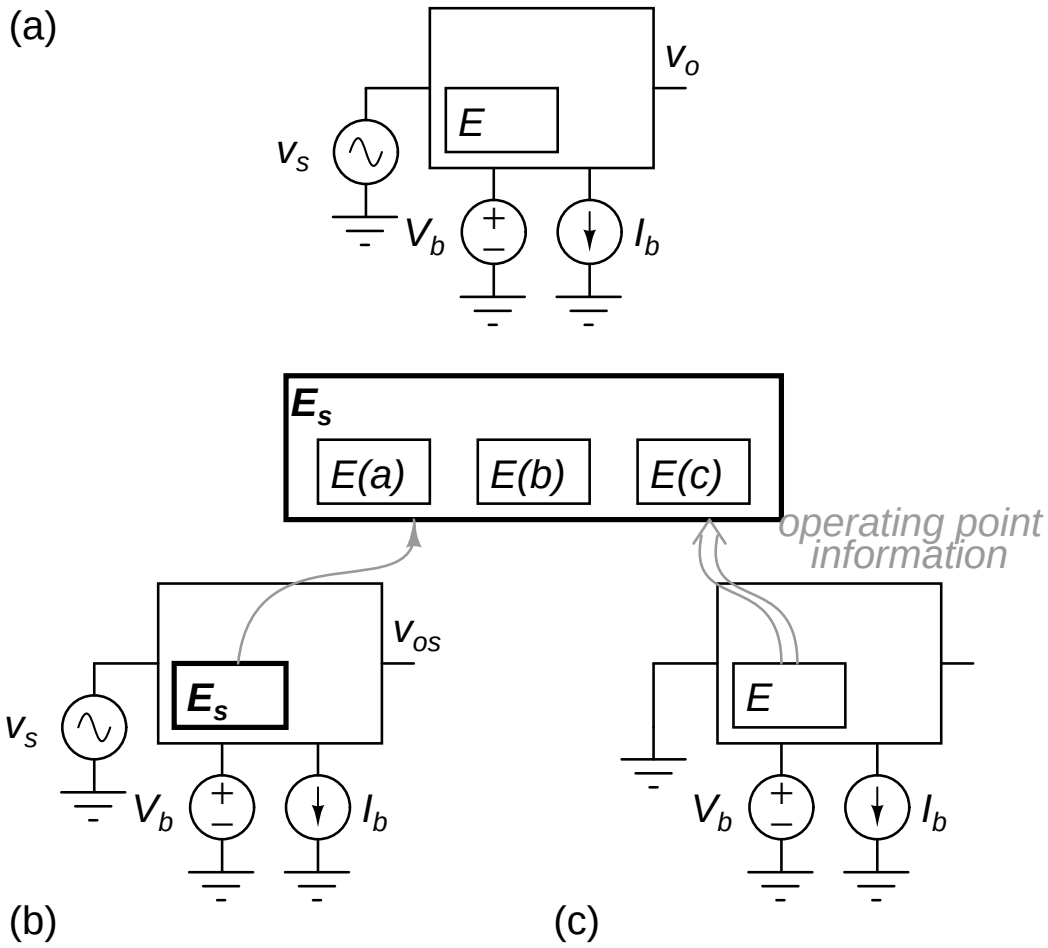


Figure 5.7: (a) Original circuit with element E, (b) Circuit with E replaced by its scaled version E_s, (c) Original circuit at its operating point. This information is used in the scaled element E_s.

terms only up to the second order. But the technique is general and works in the same way for multi-tone inputs, currents instead of voltages, and elements with higher order nonlinearity. V_b and I_b represent sources used to setup the operating point.

First, the output voltage $v_{o,sim1}$ of the circuit in Fig. 5.7(a) is simulated. Then, the schematic in Fig. 5.7(b) is generated from the original schematic. It consists of the circuit with the nonlinear element E replaced by its scaled version E_s comprising three copies[1] of E. For simplicity, we initially assume that either E is a one-port element, or a multi-port element with all ports scaled by the same

[1]If a nonlinear element is known to have terms only up to the second order, scaled elements with only two copies can be used as in Section 5.2.1. To be general, this discussion uses three copies.

factor. The scaling factor for the second order nonlinearity $\alpha^{(2)} = a_1^2 + b_1^2 + c_1^2$, where a_1, b_1, c_1 are the scaling factors for the incremental voltages in the three copies. The scaled element E_s requires the original operating point information. Therefore, a copy[2] of the original circuit in quiescent condition is included in the schematic (Fig. 5.7(c)) to provide this. The output voltage $v_{os,sim2}$ is simulated in this modified circuit. The linear equations below relate different contributions to the output voltages in the two simulations.

$$\begin{bmatrix} 1 & 1 \\ 1 & \alpha_{sim2}^{(2)} \end{bmatrix} \begin{bmatrix} v_o^{(rest)} \\ v_{oE}^{(2)} \end{bmatrix} = \begin{bmatrix} v_{o,sim1} \\ v_{os,sim2} \end{bmatrix} \tag{5.9}$$

In the above, $v_{oE}^{(2)}$ is the contribution from the second order nonlinear term of E. $v_o^{(rest)}$ is due to everything other than the second order nonlinear term. This comprises of contributions from the rest of the circuit and also from the linear term of E. The first equation simply states that the output is the sum of all these contributions. In the second equation, only $v_{oE}^{(2)}$ is scaled differently, because the scaled element E_s is designed that way, and the contribution of the rest of the circuit is assumed to remain unchanged. Solving this set of linear equations results in $v_{oE}^{(2)}$ and $v_o^{(rest)}$.

In the above description, $v_{o,sim1}$ and $v_{os,sim2}$ are assumed to be time domain voltages. The method is general and works with any type of input. One could, for instance, compute the contribution of nonlinear terms to the step response. Most often though, distortion analysis is carried out with sinusoidal inputs at one or more frequencies. In that case, the output voltages could be, say, for one period of the fundamental signal, obtained from transient or periodic steady-state simulations. It is clear that any linear transformation of the output voltages can be used equally well in (5.9), and the result would be the same linear

[2]For convenience, the technique is illustrated with a duplicated circuit for the operating point. But this duplication is not essential. As an alternative, the operating point could be simulated first (in the same simulation or a separate one) and appropriate information could be fed to the scaled network E.

transformation of $v_{oE}^{(2)}$ and $v_{o}^{(rest)}$. This enables us to work directly with the distortion component of interest. For example, one could rewrite the above in terms of phasors corresponding to the second harmonic as follows:

$$\begin{bmatrix} 1 & 1 \\ 1 & \alpha_{sim2}^{(2)} \end{bmatrix} \begin{bmatrix} H_{o2}^{(rest)} \\ H_{oE2}^{(2)} \end{bmatrix} = \begin{bmatrix} H_{o2,sim1} \\ H_{os2,sim2} \end{bmatrix} \tag{5.10}$$

$H_{o2,sim1}$ and $H_{os2,sim2}$ are the output second harmonic phasors in the two simulations and $H_{oE2}^{(2)}$ and $H_{o2}^{(rest)}$ are respectively the output second harmonic contributed by the second order term of E and the rest of the circuit. In general, one could choose the time or frequency domain representation of a single harmonic or intermodulation distortion component or a combination of several components and extract the contribution of nonlinear terms of E to those components. One can also extract the contribution to the fundamental component, which denotes compression or expansion, and contribution to dc, which denotes offset due to nonlinearity. Working directly with harmonics is convenient, for instance, when using Fourier integral based distortion analysis. This analysis is built into SPICE-like circuit simulators and avoids aliasing. It is calculated on the fly as the simulation is running. Its outputs are the phasors at different harmonics.

If E is a two-port and one is interested in extracting contributions from its different second order terms (see Table 5.1) one needs four simulations instead of two, but the procedure is essentially the same. The linear equations relating the contributions from different terms to the output voltages in different simula-

tions are given below:

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & \alpha_{sim2}^{(2,0)} & \alpha_{sim2}^{(1,1)} & \alpha_{sim2}^{(0,2)} \\ 1 & \alpha_{sim3}^{(2,0)} & \alpha_{sim3}^{(1,1)} & \alpha_{sim3}^{(0,2)} \\ 1 & \alpha_{sim4}^{(2,0)} & \alpha_{sim4}^{(1,1)} & \alpha_{sim4}^{(0,2)} \end{bmatrix} \begin{bmatrix} v_o^{(rest)} \\ v_{oE}^{(2,0)} \\ v_{oE}^{(1,1)} \\ v_{oE}^{(0,2)} \end{bmatrix} = \begin{bmatrix} v_{o,sim1} \\ v_{os,sim2} \\ v_{os,sim3} \\ v_{os,sim4} \end{bmatrix} \tag{5.11}$$

$v_{oE}^{(2,0)}$, $v_{oE}^{(1,1)}$, $v_{oE}^{(0,2)}$ respectively denote contributions from v_1^2, $v_1 v_2$, and v_2^2 terms (v_1 and v_2 are the port voltages of E). $\alpha^{(2,0)}$, $\alpha^{(1,1)}$, and $\alpha^{(0,2)}$ are the corresponding scaling factors and are given in Table 5.1. For each simulation, these values must be chosen such that the equations above are independent. A simple way to ensure this is to choose a, b, and c (scaling factors for the incremental voltages in the three copies) to be different from each other in each simulation, and to be different from any of the a, b, or c values used in previous simulations.

In the above, the element E had nonlinear terms only up to the second order. For higher orders, more simulations have to be carried out. The number of simulations equals one plus the number of relevant scaling factors α (Table 5.2). For instance, if both second and third order nonlinearity are present, and the total distortion contribution of the element is to be extracted, four simulations are required[3] and a set of linear equations analogous to (5.9) is setup as given below

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & \alpha_{sim2}^{(2)} & \alpha_{sim2}^{(3)} & \alpha_{sim2}^{(2)^2} \\ 1 & \alpha_{sim3}^{(2)} & \alpha_{sim3}^{(3)} & \alpha_{sim3}^{(2)^2} \\ 1 & \alpha_{sim4}^{(2)} & \alpha_{sim4}^{(3)} & \alpha_{sim4}^{(2)^2} \end{bmatrix} \begin{bmatrix} v_o^{(rest)} \\ v_{oE}^{(2)} \\ v_{oE}^{(3)} \\ v_{oE}^{(2)^2} \end{bmatrix} = \begin{bmatrix} v_{o,sim1} \\ v_{os,sim2} \\ v_{os,sim3} \\ v_{os,sim4} \end{bmatrix} \tag{5.12}$$

The terms above have the usual meaning. $v_{oE}^{(2)^2}$ is the nonlinear contribution

[3]By choosing a, b, c such that $\alpha^{(3)} = \alpha^{(2)^2}$, we can eliminate one simulation. Then it will not be possible to distinguish between these two contributions.

due to mixing of first and second order voltages in the second order term of E. The number of significant nonlinear terms has to be initially determined by trial and error. A priori knowledge that some terms are insignificant (e.g. even order terms in a fully differential two-port) can reduce the number of simulations.

The steps required to extract the distortion contribution from an element E are summarized below.

1. Simulate the original circuit to obtain its operating point
2. Simulate the original circuit to obtain its output (transient waveform or periodic steady-state waveform or distortion phasor as desired)
3. Create E_s, the scaled counterpart of the desired element E with the scaling factors a, b, c as parameters and the operating point information (from step 1) as additional inputs.
4. Make a copy of the circuit with the desired element E replaced by its scaled counterpart E_s.
5. Determine K, the number of significant nonlinear terms from which the distortion contribution has to be determined. For many nonlinear circuits, accounting for nonlinear terms up to third order is sufficient.
6. Choose K sets of $\{a, b, c\}$ to be used in E_s and construct the matrix $[A]$ of scaling factors (e.g. on the left hand side of (5.12)) such that it is not singular.
7. Simulate the new circuit (with the result from step 1 as operating point inputs to E_s) to obtain its output (transient waveform or periodic steady-state waveform or distortion phasor as desired). This step has to be repeated K times with new scaling factors (chosen in the above step) each time. Form $\overline{v}_{o,sim}$, the vector of simulated outputs from the results in step 2 and this step.
8. The equation relating the vector of contributions $[v_o^{(rest)}\ \overline{v}_E^T]^T$ to the vector of simulation results $\overline{v}_{o,sim}$ is $[A][v_o^{(rest)}\ \overline{v}_E^T]^T = \overline{v}_{o,sim}$ (e.g. see (5.12)). Extract the vector of contributions $[v_o^{(rest)}\ \overline{v}_E^T]^T = [A]^{-1}\,\overline{v}_{o,sim}$.

A note of caution is in order here. If an element has significant nonlinear terms up to, say, fifth order, and we are interested only in the contribution from the second order term, we must still extract the contributions from all nonlinear terms up to fifth order. This is because, a key assumption in (5.9), (5.11), or

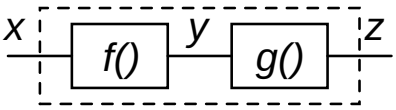


Figure 5.8: Cascade of two nonlinear stages.

(5.12) is that the contribution of $v_o^{(rest)}$ to the output remains the same when the nonlinear element is scaled. Choosing not to extract the contribution of a nonlinear term means that it is clubbed with $v_o^{(rest)}$. Because all nonlinear terms are scaled when the element is scaled, ignoring significant nonlinear terms violates the above assumption.

5.6 Interpretation

Consider a cascade of two stages as shown in Fig. 5.8, each nonlinear up to third order: $y = x + \beta_2 x^2 + \beta_3 x^3$, $z = y + \gamma_2 y^2 + \gamma_3 y^3$. The overall nonlinearity from x to z is given by

$$z = x + (\beta_2 + \gamma_2)x^2 + (\beta_3 + 2\beta_2\gamma_2 + \gamma_3)x^3 + \ldots \tag{5.13}$$

The third order term in the overall nonlinearity consists of three components:

- Third order output of the first stage going through first order term of the second stage ($\beta_3 x^3$).
- First order output of the first stage going through third order term of the second stage ($\gamma_3 x^3$).
- First and second order outputs of the first stage mixing in the second order term of the second stage ($2\beta_2\gamma_2 x^3$).

Applying the technique described in this chapter, the contribution of the two stages to the third order nonlinearity of the overall function can be identified as

$(\beta_3 + 2\beta_2\gamma_2)x^3$ and $(\gamma_3 + 2\beta_2\gamma_2)x^3$ respectively. The former has all terms containing βs and the latter, those containing γs. The component arising from the interaction of the two nonlinearities, $2\beta_2\gamma_2 x^3$, is counted against both stages.

To interpret these results correctly, it is first useful to recall the possible interpretations of the random noise contribution $S_{oE}(f)$ of an element E to the output noise (assuming as usual that noise from different elements are uncorrelated).

- If E became noiseless, the total output noise would reduce by S_{oE}.
- If all elements other than E became noiseless, output noise would be S_{oE}.
- The sum of noise contributions S_{oEk} of all elements E_k in the circuit equals the total output noise.

Inspection of the calculated nonlinear contributions of the two stages quickly reveals that only the first of the above interpretations holds true for distortion. That is to say, if v_{oE} is the distortion contribution of an element E, it means that, if E magically became linear, the output distortion reduces by v_{oE}. But, if E were the only nonlinear element, distortion products which are solely due to interaction between nonlinearities ($2\beta_2\gamma_2 x^3$ in the example above) won't be produced at all and the output distortion would not be necessarily equal to v_{oE}. Also, if contributions from individual elements were summed together, the terms due to interaction between nonlinearities are "double counted" and the sum would not equal the total distortion. This introduces a subtlety in the interpretation of $H_{o2}^{(rest)}$ in (5.11). It is not the same as the second harmonic contribution of the rest of the circuit. It is the difference between the total distortion and the sum of extracted contributions.

A common circuit where distortion is generated only by interaction between nonlinearities is a differential pair consisting of purely square law devices and an ideal tail current source. The drain voltages have only odd order distortion, though each device has only second order nonlinearity.

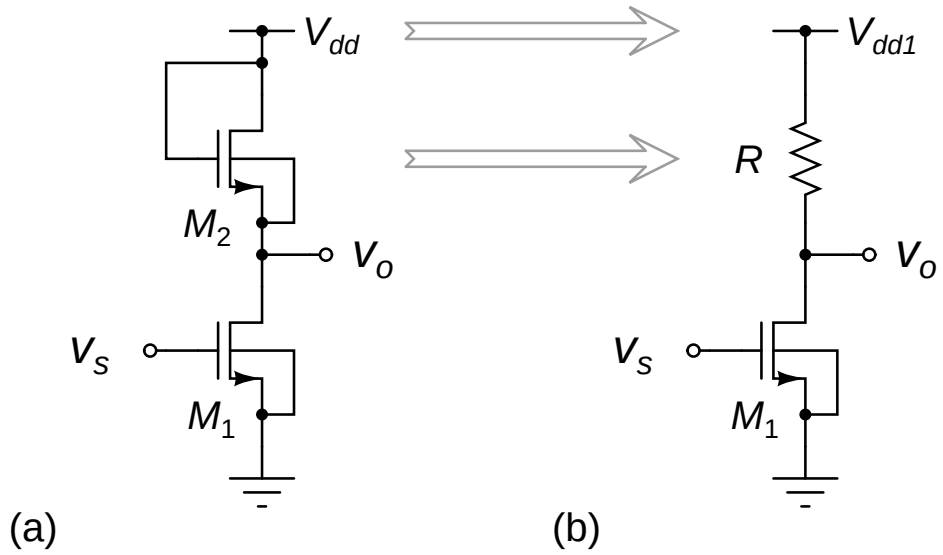


Figure 5.9: Circuits used to verify the extraction procedure. (a) nMOS common source amplifier with an nMOS diode connected load, (b) Diode load in (a) replaced by a resistor.

The sum of contributions from different elements does not equal the total distortion. However, if the contribution from an element is large, it means that the output distortion is very sensitive to the nonlinear terms of that element. This points designers to where their distortion optimization efforts must be focussed.

5.7 Examples

5.7.1 Common source amplifier with a MOS transistor load

Fig. 5.9(a) shows an nMOS common source amplifier with an nMOS diode connected load. Since the load nonlinearity is a replica of the amplifier's, nonlinearities should cancel. The circuit is simulated with a 1 kHz input and distortion contributions from the amplifier and the load are calculated using the method in Section 5.5. Fig. 5.10(a) shows the contributions from each transistor and Fig. 5.10(b) shows the distortion at the output. It can be seen that the contri-

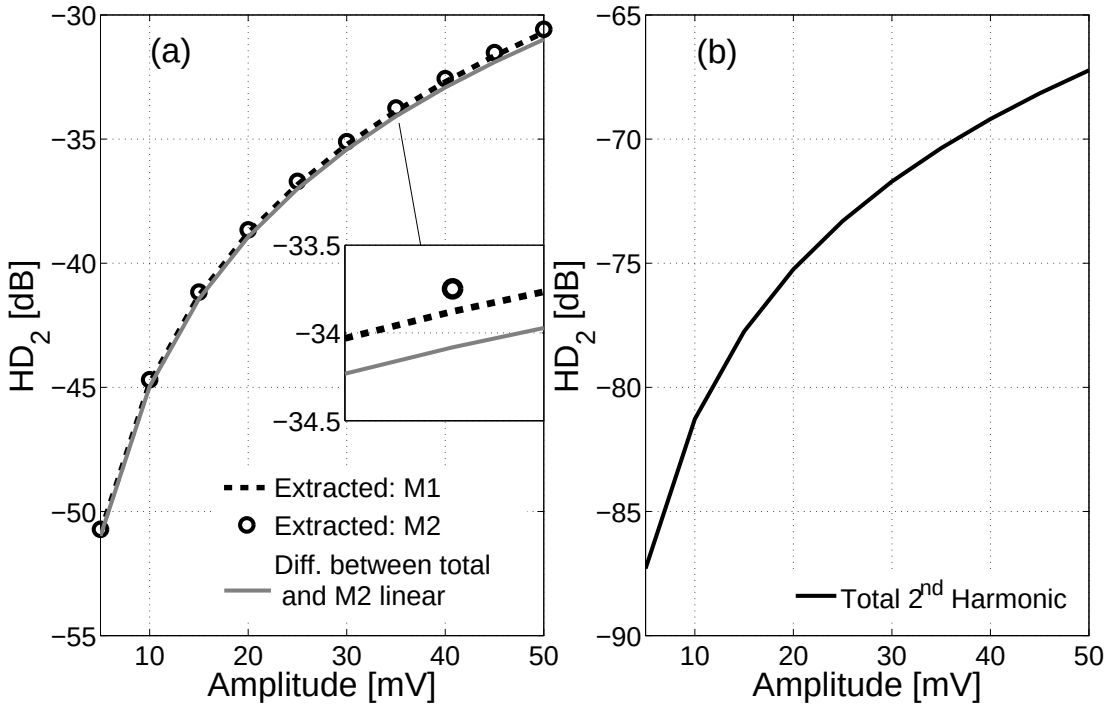


Figure 5.10: (a) Extracted contributions from M_1 and M_2 in Fig. 5.9(a) and the reduction in distortion when M_2 turns linear (Fig. 5.9(b)), (b) Output second harmonic distortion in Fig. 5.9(a).

butions from the two components are almost equal in magnitude. They turn out to have opposite phase, leading to cancellation. This can also be seen from the fact that the output second harmonic distortion is about 35 dB below the contribution from either device.

To verify that the extracted values are correct, the nMOS load is replaced by a resistor (of value $1/g_m + g_{ds}$of nMOS load) as shown in Fig. 5.9(b). The supply voltage is changed to maintain the same operating point for the amplifier device. As discussed in the previous section, when the load is made linear, the distortion reduces by an amount equal to the contribution of the load in the original circuit in Fig. 5.9(a). That reduction is also plotted in Fig. 5.10(a) and is seen to be the same as the extracted contribution of M_2 in Fig. 5.9(a).

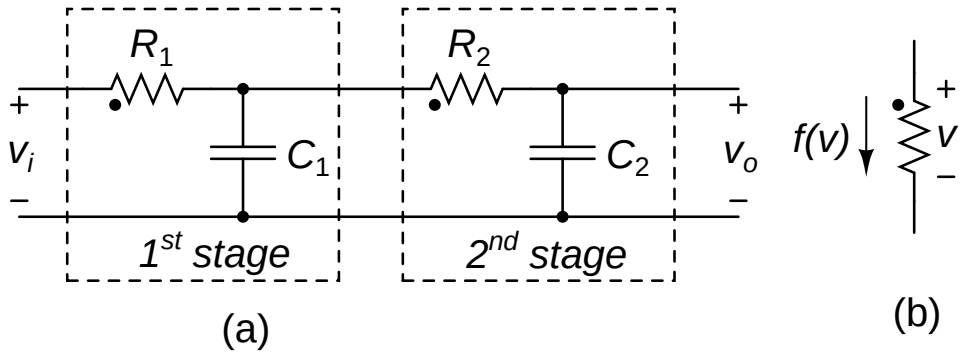


Figure 5.11: (a) Second order RC filter with nonlinear resistors, (b) Resistor model.

5.7.2 Lowpass filter with nonlinear resistors

Fig. 5.11(a) shows a second order RC filter with nonlinear resistors. The resistors are modeled (Fig. 5.11(b)) as $i = (v + K_2 v^2 + K_3 v^3)/R$. $R_1 = R_2 = R$ and $C_1 = C_2 = C$. $K_{2R1} = K_{2R2} = 0.2\,\mathrm{V}^{-1}$, $K_{3R1} = K_{3R2} = 0.1\,\mathrm{V}^{-2}$. The total distortion and the distortion contribution of each stage can be calculated using the probing and current injection method ([25, 26, 27, 28, 17]). The expression for the output second harmonic phasor when the input is $V_p \cos(\omega\, t/RC)$ is given below (ω is the signal frequency normalized to $1/RC$).

$$H_{o2} = \frac{V_p^2\omega^2(\overbrace{K_{2R1}\left(-\omega^2 + j4\omega + 4\right)}^{R_1\ /\ \text{First stage}} + \overbrace{K_{2R2}\,(j2\omega + 1)}^{R_2\ /\ \text{Second stage}}\ )}{8\omega^6 - j60\omega^5 - 162\omega^4 + j192\omega^3 + 102\omega^2 - 24j\omega - 2} \tag{5.14}$$

The corresponding expression for the third harmonic is much longer and is not given here. From these expressions, the second and third harmonic distortion of this circuit are calculated for $V_p = 0.3\,\mathrm{V}$. The contribution of each resistor is evaluated by collecting the terms containing nonlinear coefficients of that resistor as shown in (5.14). The calculated values are shown as solid lines in Fig. 5.12.

The distortion contribution of each nonlinear resistor is extracted using the proposed technique. For this, we use the schematic in Fig. 5.7 with the element E

being R_1 or R_2 in Fig. 5.11(a) and solve (5.12). The distortion contributions are plotted in Fig. 5.12 using the symbols "$+$" and "$\times$" for R_1 and R_2 respectively. It is seen that the extracted and calculated contributions match very closely.

The circuit can also be thought of as two RC stages in cascade, as shown in Fig. 5.11(a). The contributions of these stages are extracted. For this, the element E in Fig. 5.7 is the two-port corresponding to the first or second stage in Fig. 5.11(a). The contributions of the first and second stage are plotted in Fig. 5.12 using the symbols "$\Diamond$" and "$\Box$" respectively. Since the only nonlinear element in each stage is the resistor, the corresponding stage and resistor contributions must be identical, and the results show them to be so. The insets show slight differences between the calculated and the two extracted contributions. These may be attributed to various approximations and numerical errors. Each stage in Fig. 5.11(a) is a nonlinear two-port with memory and these results also validate the reasoning in Section 5.2.4.

5.7.3 Closed loop amplifier using an opamp

Fig. 5.13(a) shows an inverting amplifier of gain 4 with a bandwidth of $\sim$3 MHz. Fig. 5.13(b) shows the opamp architecture. It has two gain stages with local common mode feedback (CMFB) for each stage. Fig. 5.14 shows the transistor-level schematic of the opamp[34]. The first stage has a nonlinear common mode detector formed by splitting the transistors of the CMFB error amplifier. The feedback is applied to the gates of the first stage load transistors. The second stage has a linear resistive common mode detector followed by an error amplifier. The feedback currents are added to the output nodes.

The distortion in the differential output of Fig. 5.13(a) is simulated for a 40 mV peak-to-peak differential input across a range of frequencies, and distortion contributions from the two gain stages A1 and A2, and the two CMFB stages

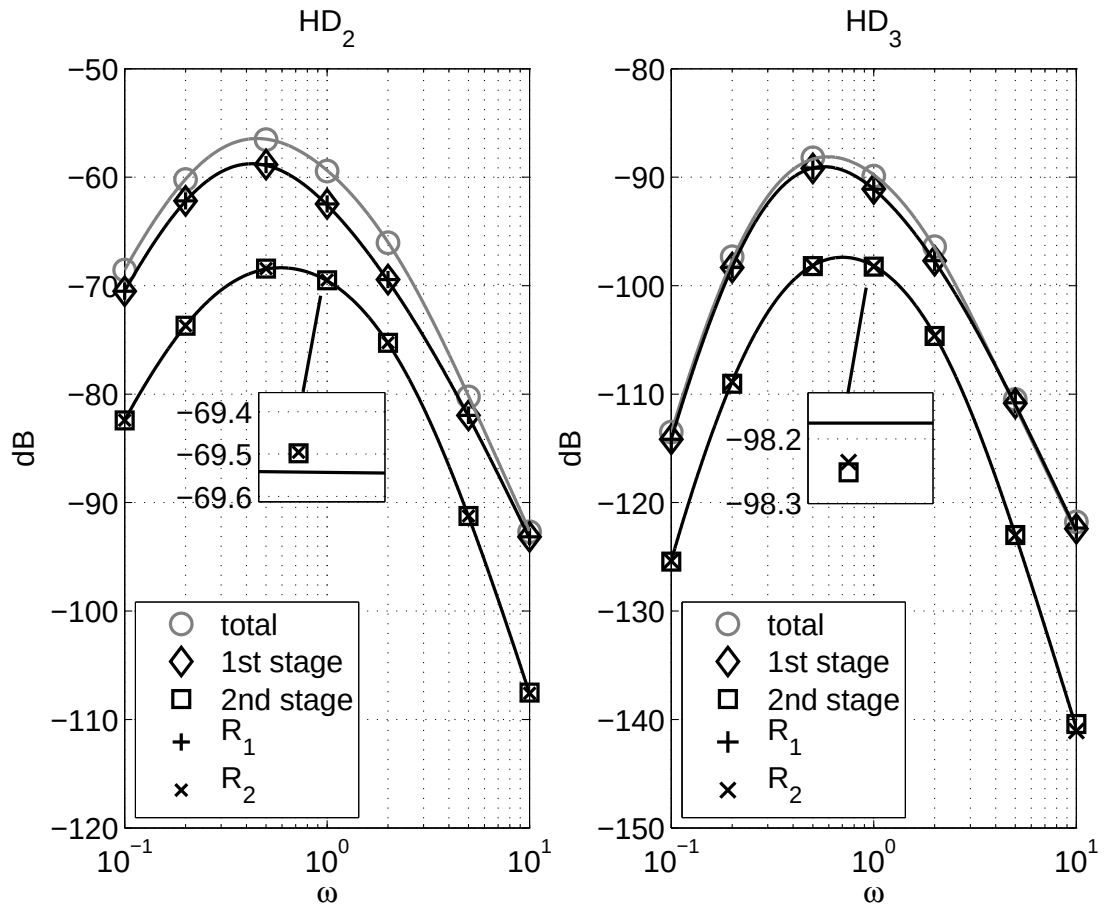


Figure 5.12: Output HD_2 and HD_3 of the filter in Fig. 5.11(a). Lines are from calculations (e.g. (5.14)). Markers are from simulations.

CMFB1 and CMFB2 are extracted using techniques outlined earlier. For this, the gain stages are treated as four-port networks and the CMFB stages as two-port networks. These stages and the ports are marked in Fig. 5.13(b) and 5.14. For purposes of extraction, all ports of each stage are scaled by the same factor. Fig. 5.16 shows the total distortion and contributions from different stages. Contributions from the second gain stage (A2) and the first stage CMFB dominate. The contribution from the first gain stage is very small because of its small input swing, and the contribution from the second stage CMFB is very small because of linear common mode detection. Fig. 5.17(a) and (b) show the composition of contributions from A2 and CMFB1. It is seen that the second order nonlinear term (scaled by $\alpha^{(2)}$) is dominant in both cases.

We can draw the following conclusions with the aid of Fig. 5.15. The first

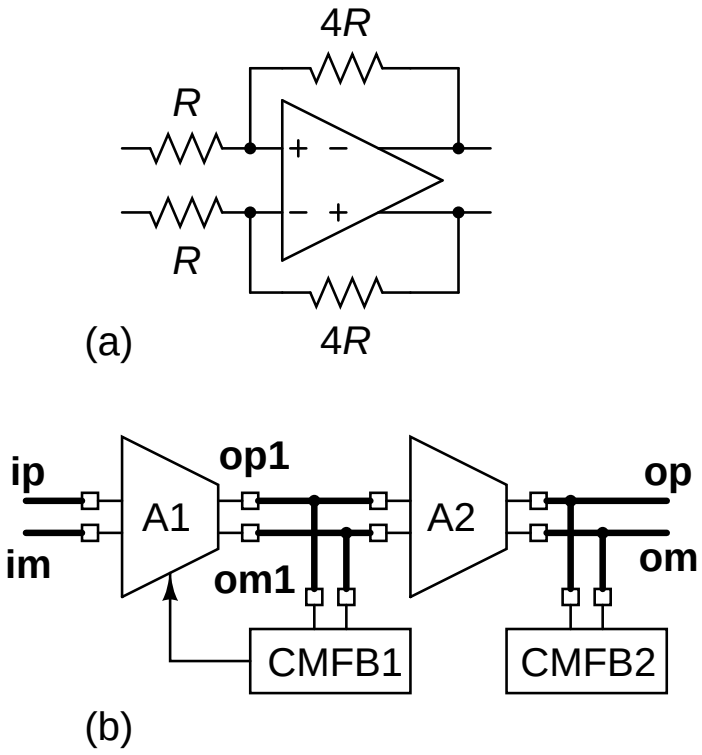


Figure 5.13: (a) 4× inverting amplifier (b) Opamp architecture.

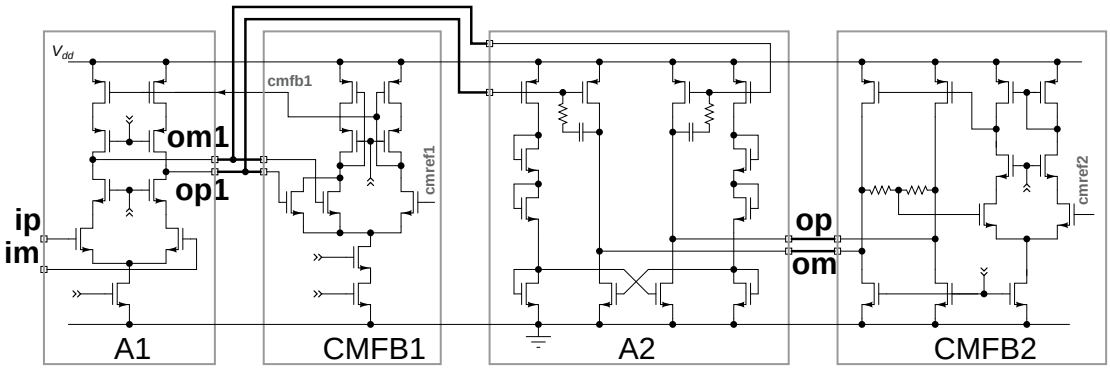


Figure 5.14: Opamp schematic [34]

stage CMFB generates second harmonic common mode at the output of the first stage. The fundamental and second harmonic mix in the second order nonlinearity (scaled by $\alpha^{(2)}$) of the second stage to generate differential third harmonic components. The third harmonic distortion in this opamp is therefore predominantly caused by interaction between the second order nonlinearities in the first stage CMFB and the second gain stage. This example underscores the utility of decomposing distortion from different stages, and from different sources in each stage. It points the designer to the part of the circuit that needs im-

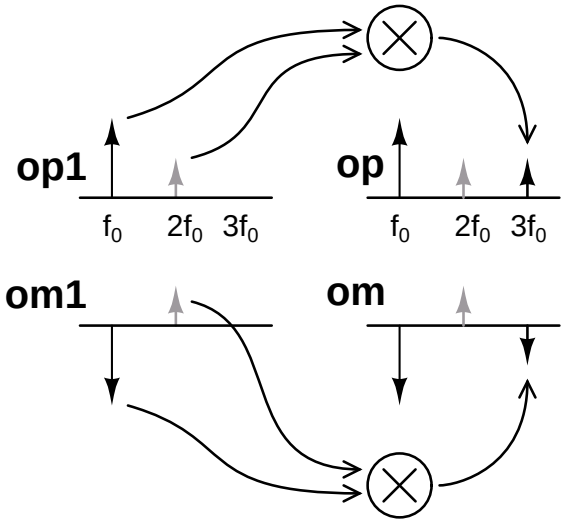


Figure 5.15: Dominant distortion products

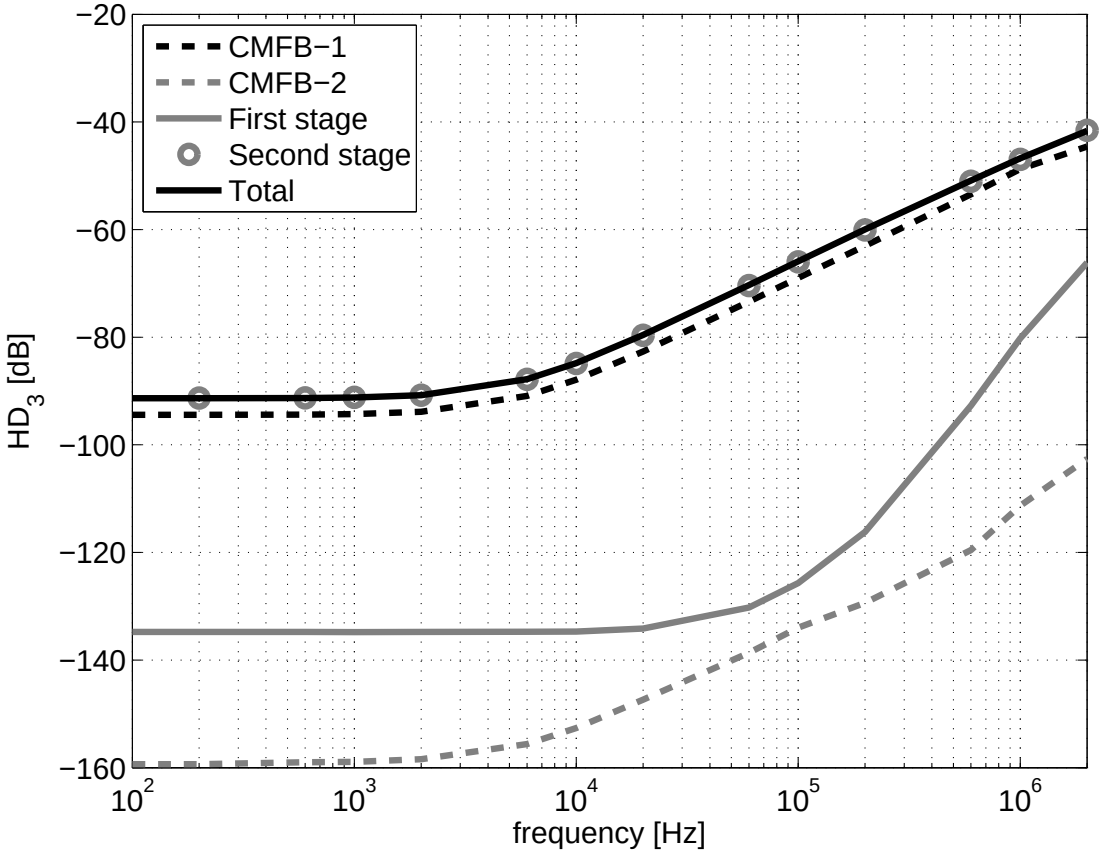


Figure 5.16: Distortion contributions for the amplifier in Fig. 5.13 versus frequency. Second gain stage (A2) and the first stage CMFB dominate.

provement. In this example, linearizing the first stage common mode detector can improve the distortion performance of the opamp.

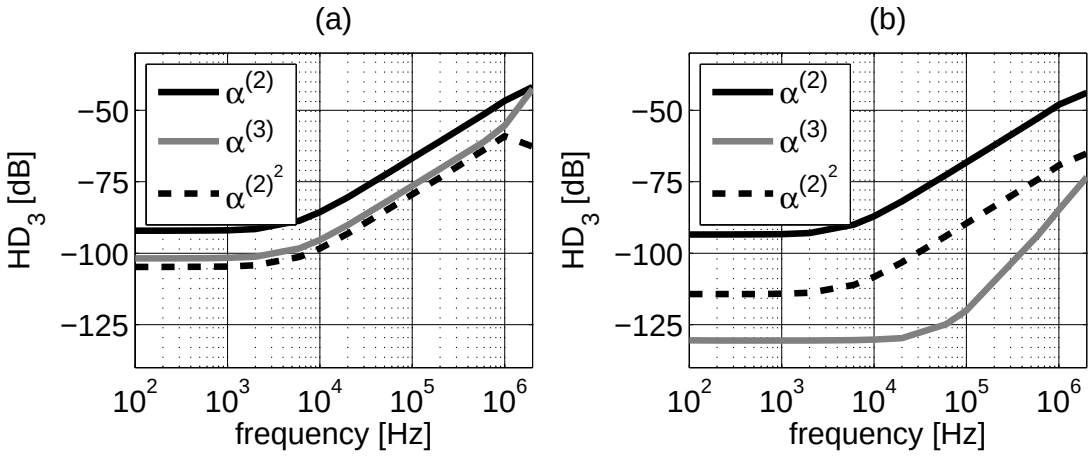


Figure 5.17: Composition of distortion contributions from (a) A2, (b) CMFB1.

The examples above consisted of signals applied over a dc operating point. The technique can equally well be applied to circuits such as mixers which have large-signal operating point excursions. In such cases, the time varying large signal source (such as the local oscillator in a mixer) must be considered as part of the operating point setup (like V_b and I_b in Fig. 5.7(c)) and retained in operating point simulations.

5.8 Comparison to other techniques

In Section 5.1, we briefly discussed a few existing techniques used to determine per-element distortion contributions. The proposed technique is similar in spirit to replacing an element by its linear counterpart (e.g. an opamp by a voltage controlled voltage source), and observing the change in distortion. But, by construction, the linear behavior including loading are exactly the same as the original, and the circuit is not oversimplified in any way. Also, the procedure for constructing the modified element is systematic and not ad hoc.

Calculating the distortion components using the probing method in [25] is very quick since it consists of linear analysis used iteratively. The difficult part is deriving suitable models for the components, extracting their parameters at the

desired operating points, and complexity of calculations if symbolic analysis is used. Also, changes made to the circuit require re-derivation of such expressions.

The method in [31] specifically addresses the calculation of per-element distortion contributions, and is an efficient technique. But, it appears that this algorithm is not presently implemented on commonly used circuit simulators and cannot be used by a circuit designer running a conventional SPICE-like simulator. A shortcoming of this technique is that it is not possible to identify the distortion coming from different nonlinear terms of each element.

The implementation in Virtuoso Spectre ([32, 33]) identifies per-element contributions as the output distortion when only the relevant element is nonlinear. Because of this, distortion arising from interaction between two nonlinear elements are not identified. For instance, when applied to third order nonlinearity in the two-stage system described in Section 5.6, interaction term $2\beta_2\gamma_2 x^3$ will be omitted and the contribution of the two stages would be predicted as $\beta_3 x^3$ and $\gamma_3 x^3$ respectively.

[30] describes a method that is model-agnostic in the same sense as the proposed method. But, choosing an appropriate multi-sine excitation, interpolating as required in case of odd order distortion, and interpreting the results is a lot more complicated than in the proposed method.

The proposed technique does not require model extraction and can be implemented on conventional circuit simulators in a simple manner. It can be applied not only to basic elements but also composite circuit blocks (such as the stages of the opamp in Section 5.7.3). Therefore, the proposed technique can also be used to construct nonlinear models for arbitrary circuits. A disadvantage of the proposed technique is that it requires multiple simulations, with a corresponding increase in simulation time. A minimum of three simulations (See (5.12) and footnote 3) are required for extraction of *total* nonlinear contributions (which is

usually the requirement) up to third order of a given element. To further resolve the contributions from different cross terms, more simulations are required—A total of 13 simulations for a two-port, up to third order terms, as listed in Table 5.3. On the other hand, during the exploratory phase, circuits are not very large, and simulation times with today's computers are very short. Therefore we feel that this is not always a severe shortcoming, and is more than balanced by its model agnostic nature, ability to be implemented on any simulator, and applicability to arbitrary circuit blocks and analysis types.

5.9 Conclusions

We have proposed a method by which a circuit designer can conveniently determine distortion contributions from different elements and from different terms of each element without going into device model details. It does not require the designer to extract Taylor or Volterra series models for individual circuit elements. The method is based on changing only the nonlinear characteristics of the element in a known manner and observing changes in output distortion. We have demonstrated the technique on a number of examples.

Since the modified element is based on instances of the original element, and not an abstracted model, the proposed technique also allows us to determine distortion contributions with process or temperature variations. This is in contrast to the methods where Taylor/Volterra models are used in which case these models have to be generated at each corner. The technique can be applied to blocks (e.g. stages of an opamp, or the entire opamp) as well as to individual transistors to produce a hierarchical summary of distortion contributions.

The published literature on distortion analysis falls into two categories: Those that describe algorithms that can be implemented in a circuit simulator (e.g. [30, 31, 32, 33]), and those that analyze specific circuits (e.g. [28, 29, 35, 36, 37]). The

former are not implemented in most circuit simulators. The latter are usually too cumbersome to be used quantitatively for arbitrary circuits. The approach presented here mitigates both these difficulties. It can be used in a conventional circuit simulator to accurately determine distortion contributions. The results can point to parts of the circuit that need optimization. Then, if warranted, one can resort to symbolic analysis to get a qualitative understanding. This is akin to how noise summary listing is typically used by the circuit designer. Because of its ease of use, the proposed technique can serve as a convenient tool for optimizing distortion or investigating the robustness of distortion cancellation and predistortion schemes.

CHAPTER 6

Effect of CMFB on the Slew Rate in Class-A Fully-Differential Amplifiers

6.1 Introduction

Several applications such as switched-capacitor filters, input buffers for ADCs, or output buffers for DACs require operational amplifiers which can drive large capacitive loads. Such opamps should ideally have high DC gain and slew rate. A high DC gain will ensure the accuracy of the settled values. A high slew rate will ensure that the settling time is as small as possible for a given small-signal bandwidth. This is because, typically, for large output steps, settling is dominated by slewing.

Because of the associated low supply voltage, obtaining high DC gain with a large output swing in fine-line CMOS technologies requires the use of multi-stage architectures as opposed to techniques such as cascoding and gain boosting. It is a well-known fact that fully differential architectures are highly tolerant to common-mode noise sources, and are therefore the automatic choice in many designs. One complication with the implementation of the fully differential high DC gain opamps is the need to set the output common-mode voltages. This is in contrast with single-ended opamps where the external feedback network provides the necessary DC negative feedback for stable operating point ([8], [10], and [9]).

[38] classifies the different schemes of common-mode feedback into two general categories. One which employs dual loops and the other employing single

loop. We refer to the dual loop scheme as local common-mode feedback and the single loop scheme as global common-mode feedback. Opamps in [39] and [40] serve as examples for the local and global common-mode feedback schemes respectively.

[41] demonstrates the use of local common-mode feedback to achieve high slew rates in single-ended opamps—local common-mode feedback is used to implement a fully differential high DC gain first stage and subsequently the anti-symmetric outputs are used to obtain a class-AB output stage which provides a high slew rate. Compared to class-A output stages, class-AB output stages provide higher slew rates. With lower supply voltages, biasing the class-AB output stage is not straightforward [42].

In this chapter, we present an analysis of the effect of two schemes of common-mode feedback on the slew rate of the closed loop amplifier using a fully differential class-A opamp. It is shown that slew rate is higher with local common-mode feedback than with global common-mode feedback. Class-A opamps with local common-mode feedback can be a convenient alternative to class-AB stages for providing high slew rates with capacitive loads.

In the next section, we review the slewing behavior in a fully differential two-stage Miller-compensated opamp with global common-mode feedback. In Section 6.3, we analyze the slewing behavior with local feedback around each stage. In Section 6.4, we present simulation results corroborating the analysis. It is demonstrated that the architecture with local feedback settles faster for both continuous-time and discrete-time amplifiers. Section 6.5 concludes the chapter.

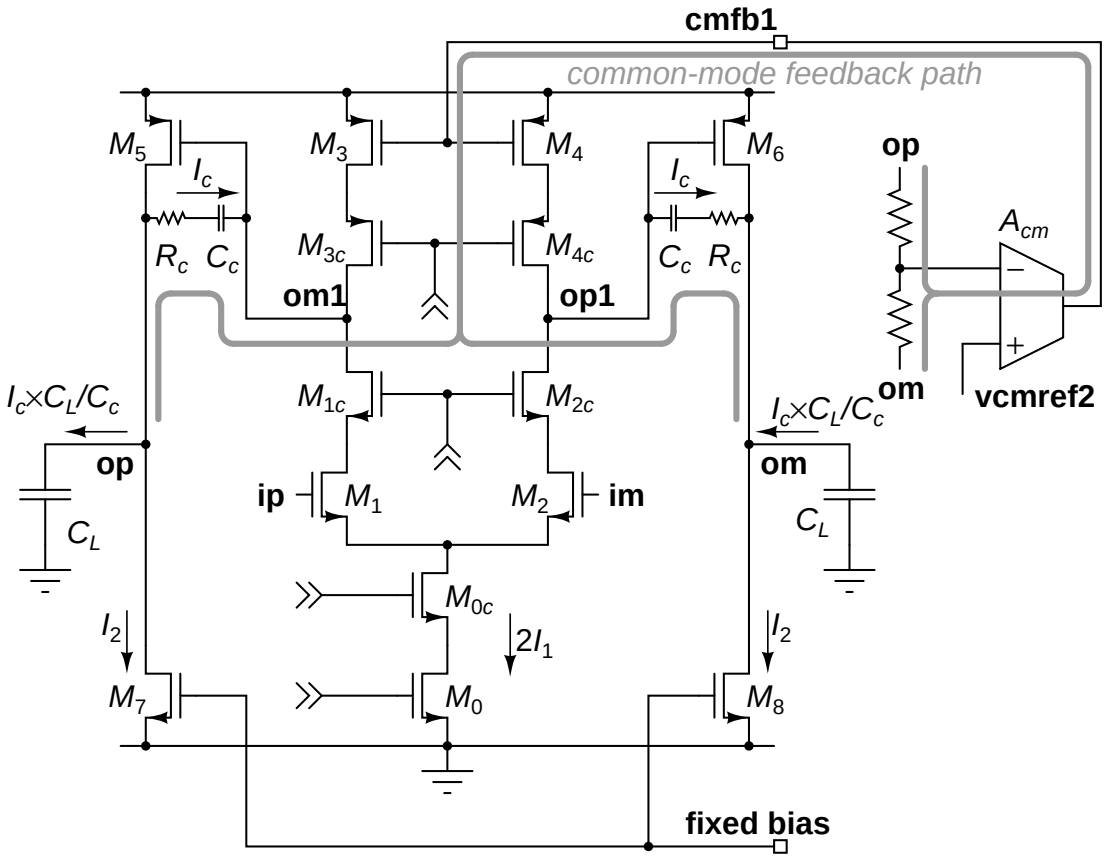


Figure 6.1: Two stage opamp with global common-mode feedback. Thick gray line indicates common-mode feedback path.

6.2 Analysis with global CMFB

Fig. 6.1 shows a two stage Miller-compensated opamp with global common-mode feedback. The first stage is a telescopic cascode stage with a tail current $2I_1$. The second stage has common source amplifiers M_5 and M_6 biased at a current I_2 from current sources M_7 and M_8. The series RC branch R_c-C_c stabilizes the opamp. The output common-mode voltage is sensed and fed back through the error amplifier A_{cm} to the gates of M_3 and M_4, the load transistors of the first stage. The common-mode feedback loop is shown in gray. Negative feedback around this loop will set the output common-mode of the second stage to **vcmref2** and the output common-mode of the first stage such that M_5 and M_6 carry a current I_2.

When a differential input is applied to the opamp, the currents in M_1 and M_2

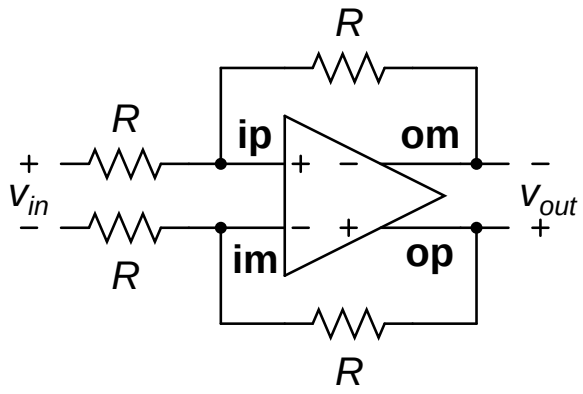


Figure 6.2: Unity gain amplifier using the opamp in Fig. 6.1.

differ from each other, and differential currents are pumped out of the first stage. These are shown as currents I_c flowing through compensation capacitors. Assuming the second stage inputs (**op1** and **om1**) to be virtual shorts to ground, the outputs **op** and **om** will respectively rise and fall at a rate I_c/C_c[8]. This implies that the load capacitors C_L carry a current $I_c \times C_L/C_c$. With this background, slewing in a closed loop amplifier is analyzed below.

Fig. 6.2 shows the unity gain amplifier used for the slew rate analysis. When a differential step is applied to the input, the output does not change instantaneously, and a fraction (half in this case) of the input step is applied across the input terminals **ip** and **im** of the opamp. For a sufficiently large input step, transistor M_2 (in Fig. 6.1) turns OFF and M_1 carries all of the tail current $2I_1$. Under these conditions, the current I_c through the Miller-compensation capacitors equals I_1. From the analysis in the previous paragraph, we infer that the outputs **op** and **om** start respectively rising and falling at I_1/C_c and the load capacitors carry a current $I_1 \times C_L/C_c$. This means that, under these conditions, the currents through M_5 and M_6 will be $I_2 + I_1\,(1 + C_L/C_c)$ and $I_2 - I_1\,(1 + C_L/C_c)$. But the latter can be valid only if $I_2 > I_1\,(1 + C_L/C_c)$. If this is not the case, M_6 cuts off and the negative slew rate will be limited to $I_2/(C_L + C_c)$. That is, **op** rises faster than the rate at which **om** falls. Consequently, their common-mode voltage rises. The common-mode feedback attempts to keep the output nodes symmetrical by changing the currents in M_3 and M_4 in accordance with the

output common-mode. In this case, the currents in M_3 and M_4 increase, which results in reducing the rate of increase of **op**. Both outputs settle to a slew rate of $I_2/\left(C_L + C_c\right)$ which is smaller than I_1/C_c.

In applications where large capacitive loads are to be driven—cases where C_L is an order of magnitude greater than C_C—I_2 should be almost an order of magnitude greater than I_1 for the negative slew rate to be limited by the first stage current. This entails a larger power dissipation in the circuit. In the next section, it will be shown that the usage of local common-mode feedback will help relax this condition. That is, a smaller bias value for I_2 can be chosen, while still obtaining a slew rate that is limited by the first stage current.

6.3 Analysis with local CMFB

Fig. 6.3 shows a two stage Miller-compensated opamp with local common-mode feedback around each stage. The output common-mode voltage of the first stage is sensed[1], amplified by the error amplifier A_{cm1}, and fed back to the gates of load transistors of the first stage M_3 and M_4. Under steady state, they supply a current I_1. The common-mode feedback loop is shown using a dashed gray line. The negative feedback around the loop will ensure that the output common-mode voltage of the first stage is same as **vcmref1**.

Transistors M_5 and M_6 form the common source class-A output stage. **vcmref1**, the nominal output common-mode voltage of the first stage, is derived from a replica circuit such that M_5 and M_6 are biased at a current I_2 when this voltage is applied to their gates. The output common-mode of the second stage is sensed and fed back through the error amplifier A_{cm2} to the gates of load transistors M_7 and M_8. Under steady state, they carry a current I_2. The second stage common-mode feedback loop is shown using a solid gray line. Negative feedback around

[1]For simplicity, a resistive common-mode detector is shown for both stages. The actual implementation for the first stage is shown in Section 6.4.3.

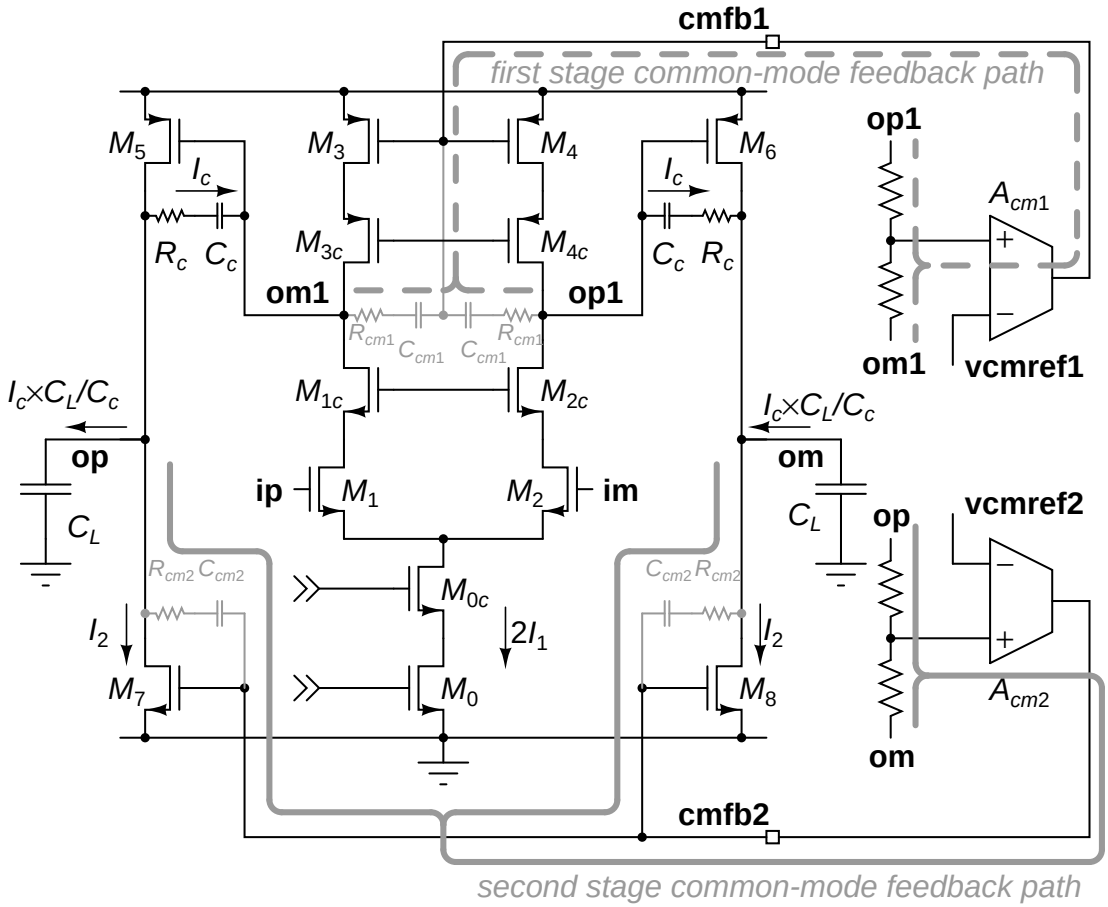


Figure 6.3: Two stage opamp with local common-mode feedback. Dashed gray line shows common-mode feedback around the first stage. Solid gray line shows common-mode feedback around the second stage. Series RC branches shown in gray may be needed depending on the implementation of common-mode feedback amplifiers A_{cm1} and A_{cm2}.

the loop ensures that the output common-mode voltage is set to **vcmref2**, which is typically at half the supply voltage.

Analyzing the circuit in the same manner as the previous section, we obtain the positive slew rate to be the same as I_1/C_C. This is based on the fact that the drain current of transistor M_5 will get adjusted such that a current I_1 flows through the compensation capacitor. Further, if we assume that I_2 is not sufficiently large ($I_2/(C_C + C_L) < I_1/C_C$), then the negative slew rate will be $I_2/(C_L + C_C)$. With this, we can see that net common-mode voltage at the output of the second stage increases. Because of this, the output voltage of the error amplifier A_{cm2} in the second stage common-mode feedback loop starts to

increase. This increases the currents in M_7 and M_8 thereby effectively increasing I_2 and consequently, the negative slew rate. We can see that the use of two loops has effectively made the output stage behave similar to a class-AB stage under slewing conditions. Both outputs settle to a slew rate of I_1/C_c.

6.4 Verification of slew rate enhancement

The analysis in the previous sections are verified by simulating amplifiers using two stage Miller-compensated opamps in a $0.18\,\mu$m process with a 1.8 V supply. The same opamp is implemented with local and global common-mode feedback and tested in a closed loop setting.

6.4.1 Common-mode feedback circuits

Fig. 6.4 shows the common-mode feedback circuitry used for global feedback with Fig. 6.1. Fig. 6.4(a) shows the common-mode detector and error amplifier. A resistive detector is used for linearity. The feedback **cmfb1** is given to the gates of M_3 and M_4 in Fig. 6.1. The loop includes three stages—$M_{3,4}$, second stage of the opamp $M_{5,6}$, and error amplifier A_{cm}. Therefore, a low gain error amplifier with a diode connected pMOS load is used. R_c and C_c used for stabilizing the opamp in Fig. 6.1 also stabilize the common-mode feedback loop.

Fig. 6.4(b) shows the switched capacitor counterpart [45]. Since there are two stages of the opamp in the common-mode feedback loop, an inverting stage is necessary to provide negative feedback. This is provided by the stage formed by M_{c11} and M_{c13}. A capacitive common-mode detector using two identical capacitors C_1 is used to drive the gate of M_{c11}. The charge on C_1 is periodically refreshed by placing a capacitor C_2 charged to the difference between **vcmref2** (the desired common-mode output of the first stage) and **vbiasn11** (the voltage

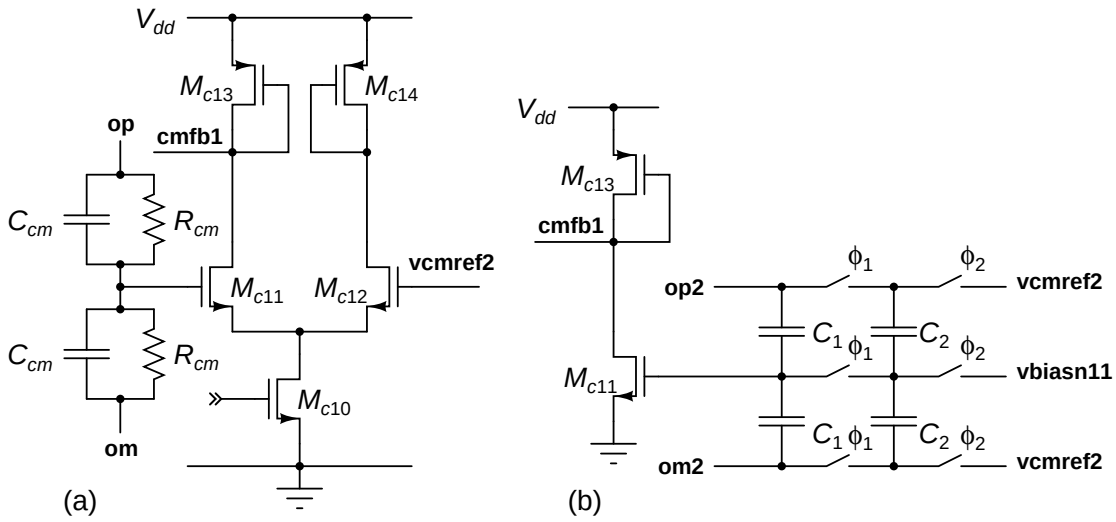


Figure 6.4: Circuitry used for global common-mode feedback (Fig. 6.1): (a): Continuous-time common-mode detector and error amplifier, (b): Switched-capacitor common-mode detector followed by an inverting stage.

required at the gate of M_{c11}) across them. The net effect is similar to placing a battery with an appropriate voltage between the output common-mode and the gate of M_{c11}. As with Fig. 6.4(a), R_c and C_c used for stabilizing the opamp also stabilize the common-mode feedback loop.

Fig. 6.5 shows the common-mode feedback circuitry used for local feedback with Fig. 6.3. Fig. 6.5(a) shows the common-mode detector and error amplifier A_{cm1} for the first stage. A single differential pair with a current mirror load is used as the error amplifier. The input transistor of the error amplifier is split into M_{c11a} and M_{c11b} to form the common-mode detector with a high input resistance so that the dc gain of the first stage is not affected. The feedback **cmfb1** is given to the gates of M_3 and M_4 in Fig. 6.3. Since the common-mode feedback loop around the first stage consists of two gain stages (the error amplifier in Fig. 6.5(a) and $M_3, 4$ in Fig. 6.3), series RC networks R_{cm1}-C_{cm1} are used for stability. Fig. 6.5(b) shows the common-mode detector and error amplifier for the second stage. A resistive divider with parallel RC branches is used for linearity. A high resistance ensures no loading and parallel capacitors ensure that there is no phase shift at high frequencies. The feedback **cmfb2** is provided to the gates of M_7 and M_8 in Fig. 6.3. Again, there are two gain stages in feedback

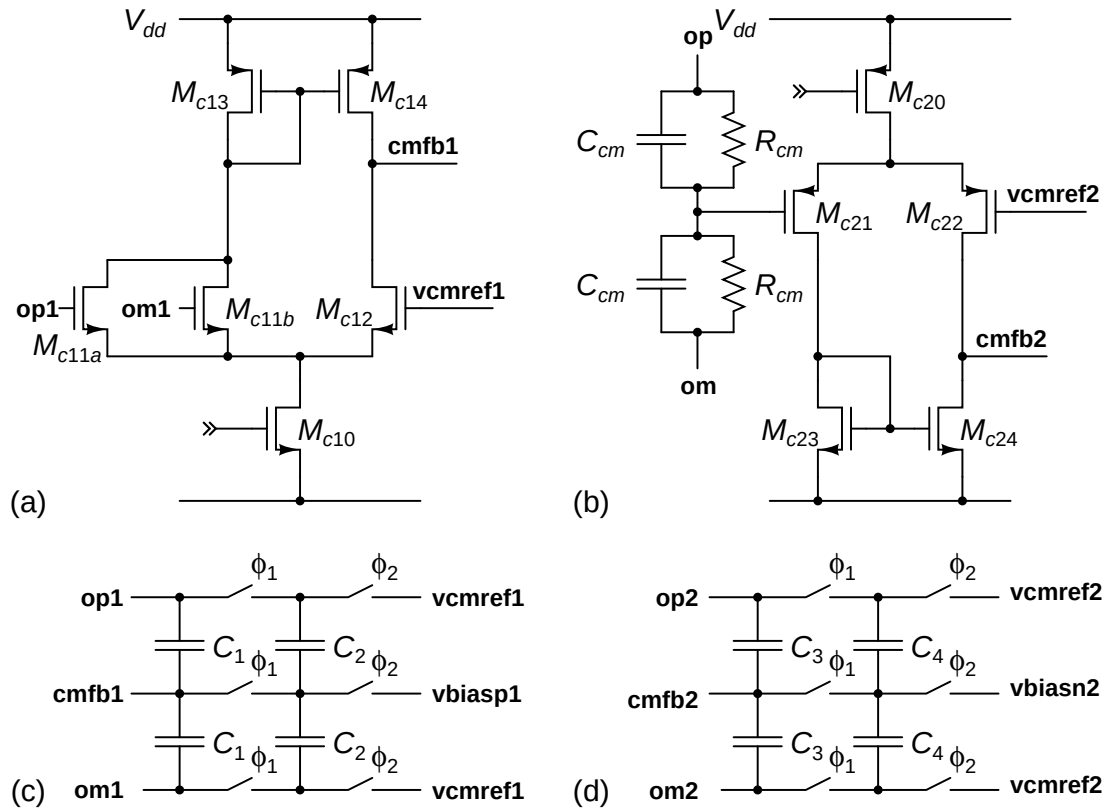


Figure 6.5: Circuitry used for local common-mode feedback (Fig. 6.3): (a, b): Continuous-time common-mode detector and error amplifier, (c, d): Switched-capacitor common-mode detector.

and series RC networks R_{cm2}-C_{cm2} are used for stability.

Fig. 6.5(c, d) show the switched capacitor counterparts of Fig. 6.5(a, b). The common-mode feedback structure used around the first stage is as shown in Fig. 6.5(c). A capacitive divider using two identical capacitors C_1 detects the common-mode and provides feedback to the gates of M_3 and M_4. The charge on C_1 is periodically refreshed by placing a capacitor C_2 charged to the difference between **cmref1** (the desired common-mode output of the first stage) and **vbiasp1** (the voltage required at the gate of M_3 and M_4 in Fig. 6.3 for them to be biased at a current I_1) across them. In this case, there are no error amplifiers, and the common-mode loop gain is provided by M_3 and M_4. This results in a lower dc loop gain and higher loop bandwidth compared to the continuous time common-mode feedback case shown in Fig. 6.5(a). R_{cm1} and C_{cm1} in Fig. 6.3 are not necessary. Fig. 6.5(d) shows the common-mode feedback struc-

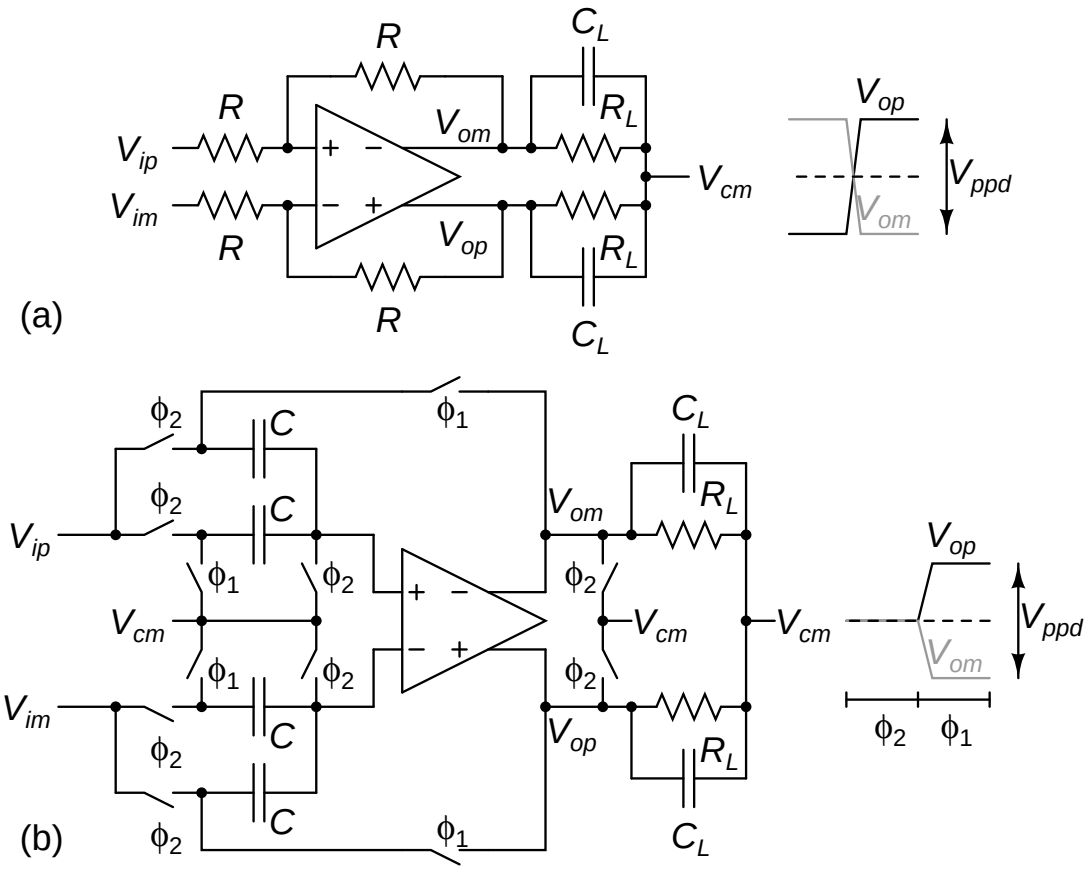


Figure 6.6: Closed loop amplifier examples: (a) Continuous-time amplifier, (b) Switched capacitor amplifier and inverting low gain stage.

ture used around the second stage. It is similar to that used for the first stage and provides feedback to M_7 and M_8 in Fig. 6.3. Again, there is a single gain stage in feedback and R_{cm2} and C_{cm2} are not required.

6.4.2 Closed loop amplifier examples

The amplifiers in Fig. 6.6 were used to verify the slewing behavior with global and local common-mode feedback. Fig. 6.6(a) shows a continuous-time amplifier with a differential gain of 1. The input and feedback resistors are 20 kΩ each. The amplifier is tested with differential step inputs of up to 2.8 V peak-to-peak around a common-mode voltage of 0.9 V. This amounts to the single ended signals swinging up to 200 mV off the supply rails.

Fig. 6.6(b) shows a switched capacitor amplifier with a differential gain of 2. In

ϕ_2, the opamp's input and output are reset to the common-mode and the input is sampled on both capacitors C. In ϕ_1, the total charge is transferred to one of the capacitors by connecting it in feedback and connecting the other capacitor across the virtual short input of the opamp. This is a structure typically used in pipelined ADCs[44]. The capacitor $C = 4\,\text{pF}$. In this case, the amplifier is tested for step-like outputs of 1.4 V from the reset state. In ϕ_1, the amplifier in Fig. 6.6(b) has a feedback fraction of 0.5, the same as that in Fig. 6.6(a). Therefore, the amplifiers are expected to have a similar settling behavior.

Both of the amplifiers in Fig. 6.6 are tested with (a) Purely capacitive load of 100 pF and a parallel RC load of 100 pF——2 kΩ , and (b) Continuous-time and switched capacitor common-mode feedback.

The two-stage Miller-compensated opamps in Figs. 6.1 and 6.3 used for these simulations have a quiescent current of 400 μA $(2I_1)$ in the differential pair and 550 μA ,(I_2) in each common source amplifier of second stage. In the global feedback case, the error amplifier consumes 120 μA . In the local feedback case, the first and second stage error amplifiers consume 40 μA and 100 μA respectively. The opamp characteristics are summarized in Table 6.1. The unity loop gain frequency $(f_{u,loop})$ and phase margin (ϕ_M) of different feedback loops are calculated for the continuous-time amplifier (Fig. 6.6(a)) with continuous-time common-mode feedback circuits (Fig. 6.4(a) or Fig. 6.5(a,b)) under quiescent condition. It is seen that $I_2/(C_c + C_L)$ is nearly 4$\times$ smaller than I_1/C_c. For the second stage not to limit the slew rate with global common-mode feedback a I_2 is required to be 2.2 mA, increasing the total current in the opamp to 4.92 mA.

6.4.3 Simulation results

Fig. 6.7 shows the step response of the continuous-time amplifier in Fig. 6.6(a). For this comparison, continuous-time common-mode feedback circuits shown

Table 6.1: Opamp characteristics

	Global	Local	
First stage I_1	200 μA	200 μA	
Second stage I_2	560 μA	560 μA	
Error amplifiers	120 μA	140 μA	
Total	1.62 mA	1.64 mA	
I_1/C_c	20 V/ μs	20 V/ μs	
$I_2/(C_c + C_L)$	5.1 V/ μs	5.1 V/ μs	
Differential loop	11.4 MHz,	11 MHz,	
$(f_{u,loop}, \phi_M)$	60°	57°	
Common-mode	11.8 MHz,	12.7 MHz,	10.6 MHz,
feedback loop	68°	71°	72°
$(f_{u,loop}, \phi_M)$		(first stage)	(second stage)

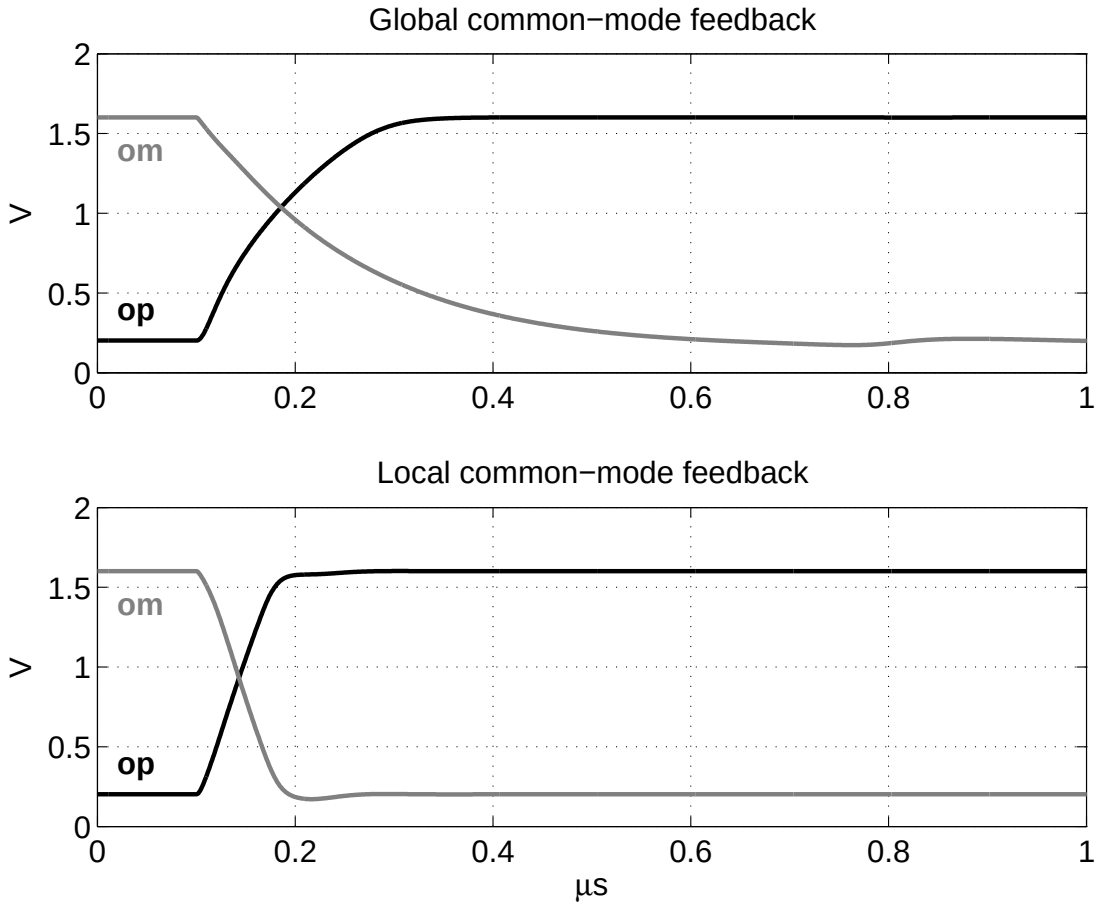


Figure 6.7: Output voltages of the amplifier in Fig. 6.6(a) for a 2.8 V differential output step and 100 pF||2 kΩ load.

in Fig. 6.4(a) (global feedback) and Fig. 6.5(a,b) (local feedback) were used. Also, a 2 kΩ||100 pF load is used. The differential output step seen is 2.8 V. It is clearly seen that the amplifier with local common-mode feedback settles much

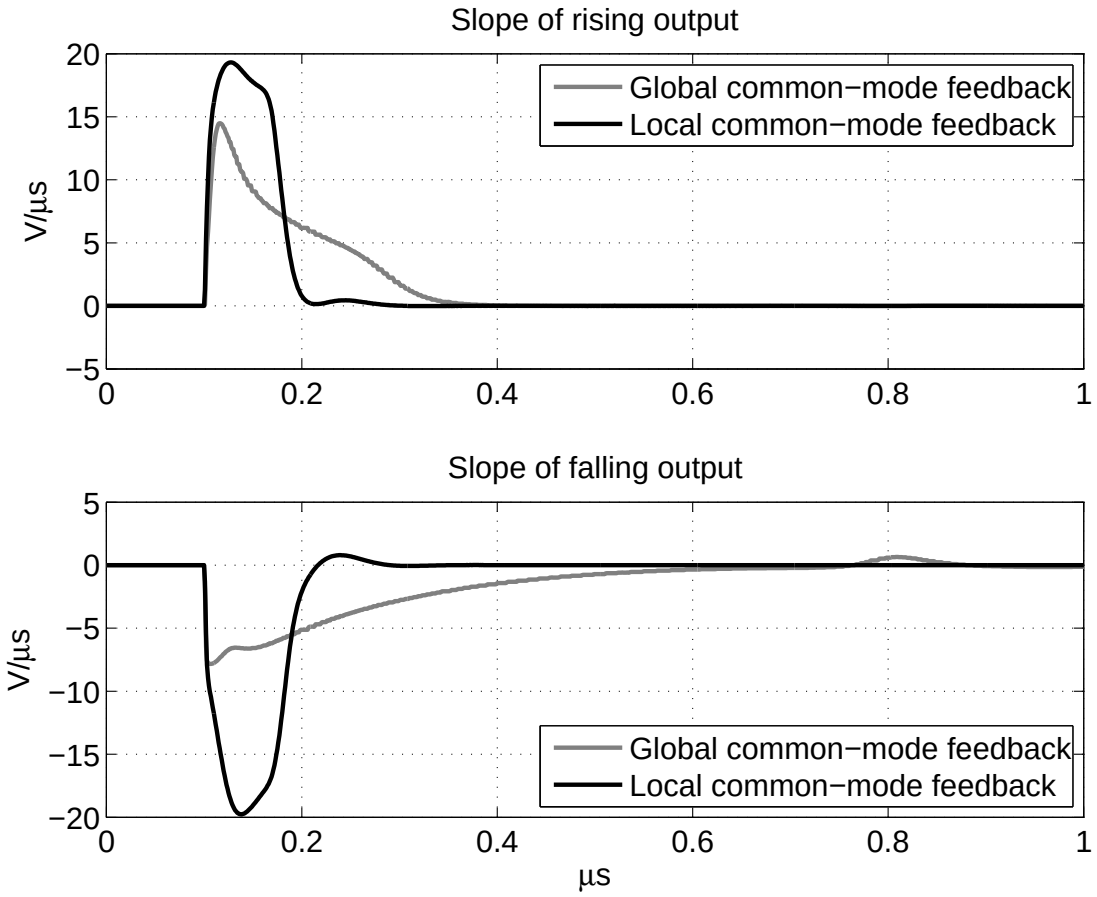


Figure 6.8: Output slopes of the amplifier in Fig. 6.6(a) for a 2.8 V differential output step and 100 pF||2 kΩ load.

faster and has a more symmetric settling of **op** and **om**. With global common-mode feedback, **om** settles much slower than **op**.

It is is also evident that **op** follows a piecewise linear profile while slewing. i.e. it begins to rise rapidly, and settles to a slower slew rate. Fig. 6.8 shows the slopes of **op** and **om** under the same conditions. With local feedback, both **op** and **om** slew nearly at $I_1/C_c = 20\,\mathrm{V}/\,\mu\mathrm{s}$. With global common-mode feedback, the slope of **om** is significantly lower and close to $I_2/(C_c + C_L) = 5.1\,\mathrm{V}/\,\mu\mathrm{s}$. **op** starts off with a higher slope and, and settles to the lower value after a short interval. This behavior is because it takes a little time for the common-mode feedback loop to kick in and restore symmetry on the two sides.

Table 6.2 shows the settling time (in nanoseconds) to 0.1% accuracy for the continuous-time amplifier in Fig. 6.6(a). For the continuous-time amplifier, all

Table 6.2: Settling time (in ns) for the continuous-time amplifier with local and global CMFB

		CT cmfb		SC cmfb	
	o/p step	100 pF || 2 kΩ	100 pF	100 pF || 2 kΩ	100 pF
Global feedback	25%	197	187	248	244
	50%	286	257	347	309
	75%	466	332	515	360
	100%	1149	416	782	451
Local feedback	25%	96	108	163	170
	50%	120	139	150	172
	75%	114	159	176	159
	100%	144	192	250	202

combinations of common-mode feedback—global continuous-time (Fig. 6.4(a)), local continuous-time (Fig. 6.5(a & b)), global discrete-time (Fig. 6.4(b)), local discrete-time (Fig. 6.5(c & d))—are used. All these combinations are simulated for two different loads (100 pF and 100 pF||2 kΩ). Further, simulations are done for different values of output steps and the results are shown. For the case under consideration, 100% corresponds to 2.8 V differential output step (-1.4 V to 1.4 V).

Table 6.3: Settling time (in ns) for the discrete-time amplifier with local and global CMFB

		CT cmfb		SC cmfb	
	o/p step	100 pF || 2 kΩ	100 pF	100 pF || 2 kΩ	100 pF
Global feedback	25%	185	170	166	160
	50%	315	231	236	211
	75%	455	275	323	250
	100%	1636	327	612	294
Local feedback	25%	115	160	130	128
	50%	157	184	146	136
	75%	159	193	159	133
	100%	147	208	201	139

The simulations are run for the case of discrete-time amplifier in Fig. 6.6(b). Again, all possible combinations of common-mode feedback circuits, load con-

ditions, and output steps are used for the simulations. For this case, a 100% output step corresponds to 1.4 V differential output step. Table 6.3 shows the settling times.

In every case it is seen that local common-mode feedback results in quicker settling—more than 1.5× better with a purely capacitive load, and more than 3× better with an additional resistive load. The settling and slopes of the outputs are similar to that seen in Fig. 6.7 and Fig. 6.8 in all cases.

6.5 Conclusions

We have analyzed the slewing behavior of two stage Miller-compensated opamps with global and local common-mode feedback loops. We have shown that, while slewing, both pull-up and pull-down currents in the output stage are signal dependent when local common-mode feedback is used. This effectively makes a class-A output stage act like a class-AB output stage. Simulations under various conditions show at least a 2× quicker settling with local common-mode feedback for the same quiescent current in the opamp. Achieving a similar reduction with global common-mode feedback entails an increase in current of more than 2×. We therefore conclude that, to achieve a given settling time, using local common-mode feedback is more power efficient than using global common-mode feedback, especially in opamps which are required to drive large capacitive loads. This is in spite of the extra error amplifier or switched capacitor feedback stage that is required for local common mode feedback.

CHAPTER 7

Conclusions and Suggestions for Future Work

7.1 Conclusions

There has been a continuous effort to reduce the power consumption of high resolution converters. Chapter 1 deals with the history and evolution of such high resolution converters and the associated driver circuitry. The past decade has seen a tremendous reduction (nearly two orders of magnitude) in the power consumption of the converter. However there was very little effort into reducing the power consumption of the driver circuitry. With this, the current scenario is that the driver circuitry consumes more power than the converter itself. This dissertation is aimed at bridging this gap.

A detailed study of possible architectures for the driver circuitry is given in Chapter 2. It is shown that architectures based on inverting amplifier configuration are best suited for this problem. Based on the results obtained in Chapter 2, a driver based on the fully-differential amplifier architecture is fabricated. The design and simulation details of the same are presented in Chapter 3. The measurement results given in Chapter 4 confirms satisfactory performance of the driver.

In Chapter 5, we propose a technique to determine the distortion contributions from individual elements or sub-blocks. The technique is based on elementary circuit theory and does not require the designer to have the knowledge of models. Further, the technique can be easily used with SPICE-like simulators and is therefore a very handy tool to optimize circuits for low distortion and to explore several distortion cancellation/reduction schemes. Further, it can be used

to understand the distortion behaviour of circuits.

Chapter 6 dealt with the effect that the common-mode feedback scheme has on the slew rate of a fully-differential amplifier. The advantages obtained by having local common-mode feedback instead of global common-mode feedback are presented.

7.2 Suggestions for future work

In this dissertation, the possibility of charge pump based design was not investigated in depth. To reduce the problems of clock feedthrough and mixing, one could choose a pulse position modulated clock in the charge pump as demonstrated in [46]. With this arrangement, the power of the feedthrough tone will not appear at a single frequency but will be spread over the entire range over which the clock frequency varies. The scheme trades SNR for a better SFDR. Another solution to prevent the aforementioned problems is to use the ADC clock itself in the charge pump circuitry. With this arrangement, the feedthrough tone will be seen at $f_s/2$ at the output of the ADC while the mixing tone will be seen on the signal bin itself.

The fabricated driver is not integrated with the converter. Integrating the driver with the converter will alleviate problems related to bondwire inductances along with those associated with board traces. Further, it will greatly reduce the complexity and area of the board.

The simulation technique for determining the individual distortion contributions can also be used to extract Volterra-type models for individual elements or circuit subblocks. Then, with these extracted models, in principle, ac-type simulations can be performed on the circuits while capturing their nonlinear behaviour. This can be a convenient alternative to the otherwise time consuming transient simulation.

APPENDIX A

Relationship Between G_{m1} and G_{m2} for Stability in Two-Stage Opamp

Fig. A.1 shows the small-signal model of a two-stage opamp. The compensation scheme is also shown. G_{m1}, G_{o1}, and C_1 represent the first stage transconductance, output conductance and output capacitance respectively. Similarly, G_{m2}, G_{o2}, and C_2 represent the second stage transconductance, output conductance and output capacitance respectively. C_C represents the Miller compensation capacitor.

The transfer function of the opamp ($A(s)$) is found out and is as given below.

$$A(s) = \frac{G_{m1}(G_{m2} - sC_c)}{G_{o1}G_{o2} + s(C_C + C_2)G_{o1} + s(C_C + C_1)G_{o2} + sC_CG_{m2} + S^2(C_1C_2 + C_1C_C + C_2C_C)} \tag{A.1}$$

If we use this opamp to make a closed loop amplifier of gain 2, we will use a feedback factor of 0.5. We can calculate the transfer function of the closed loop

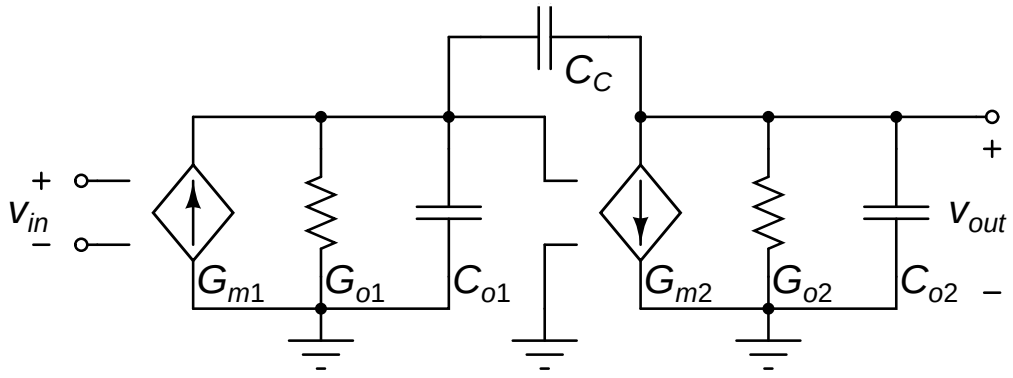


Figure A.1: Small-signal model of a two-stage opamp.

amplifier ($CLTF(s)$) as shown below.

$$CLTF(s) = \frac{2A(s)}{2 + A(s)} \tag{A.2}$$

The denominator of the above transfer function is as shown below.

$$2\big(G_{o1}G_{o2} + s(C_C + C_2)G_{o1} + s(C_C + C_1)G_{o2} + sC_CG_{m2} + S^2(C_1C_2 + C_1C_C + C_2C_C)\big) + G_{m1}(G_{m2} - sC_c) \tag{A.3}$$

For left half plane roots, all the coefficients must be positive. If we now consider the coefficient of the term in s, then it can be seen that the coefficient is mainly dominated by the terms involving G_{m1} and G_{m2}. This is because by design, G_ms will be larger than G_os by several orders of magnitude. Based on this assumption, if we consider only the significant terms in s, we can see that

$$2G_{m2} > G_{m1}$$

is required for the coefficient to be positive.

APPENDIX B

Pole Zero Estimation

R_2 and C_2 in Fig. B.1 are representative of the series resistor R_1 and load capacitor C_L in the original small-signal model depicted in Fig. 3.13 respectively. R_1 in the above circuit is representative of the parallel combination of the G_{o2} (output conductance of the second stage), $G_{m2}C_C/(C_C + C_{o1})$ (conductance due to the feedback through the compensation capacitor), and $3R$ (feedback network). C_1 in the above network is representative of the parallel combination of C_{o2} (load capacitance of the second stage) and $C/3$ (feedback network). From the values that were seen, we assume that $C_2 > C_1$ and $R_1 \approx R_2$.

Based on the above approximation, we can see that there will be widely separated poles with the low frequency pole associated with C_2 and high frequency pole associated with C_1. To determine the low frequency pole, we see that C_1 will present a very high impedance. R_1 dominates the parallel combination of R_1 and C_1. Therefore, the pole associated with C_2 will be $\frac{1}{2\pi(R_1+R_2)C_2}$.

Similarly, to determine the high frequency pole associated with C_1, we see that

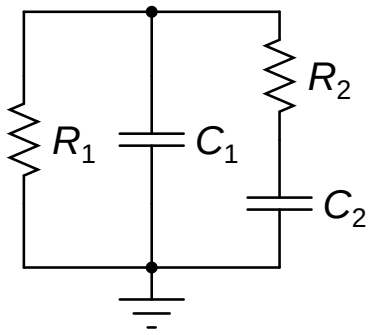


Figure B.1: Equivalent circuit used to find out the pole zero locations of the small-signal model shown in Fig. 3.13.

the impedance of the series combination of R_2 and C_2 will be dominated by R_2. With this, the pole associated with C_1 will be $\frac{1}{2\pi(R_1||R_2)C_1}$.

REFERENCES

[1] J. L. McCreary and Paul R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371-379, Dec. 1975.

[2] Ricardo E. Suarez et al., "All-MOS charge-redistribution analog-to-digital conversion techniques. II," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 379-385, Dec. 1975.

[3] K. R. Lakshmikumar et al., "Characterisation and modeling of mismatch in MOS transistors for precision analog design," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 6, pp. 1057-1066, Dec. 1986.

[4] Marcel Pelgrom et al., "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433-1440, Oct. 1989.

[5] Peter Kinget, "Design mismatch and tradeoffs in the design of analog circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1212-1224, Jun. 2005.

[6] C. P. Hurrell et al., "An 18 b 12.5 MS/s with 93 dB SNR," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2647-2654, Dec. 2010.

[7] R. Widlar et al., "A monolithic power Op Amp," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 2, pp. 527-534, Apr. 1988.

[8] D. Johns and K. Martin, *Analog Integrated Circuit Design*, 1st ed., Wiley India Pvt. Ltd., 2008.

[9] Nagendra Krishnapura, "EE5390: Analog Integrated Circuit Design," Available: http://www.ee.iitm.ac.in/∼nagendra/videolectures

[10] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2000.

[11] Robert A. Blauschild et al., *Differential amplifier circuit with rail-to-rail capability*, United States Patent 4 532 479, Jul. 30, 1985.

[12] Johan H Huijsing and D. Linebarger, "Low voltage operational amplifier with rail-to-rail input and output ranges," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 6, Dec. 1985.

[13] Shouli Yan et al., "Constant-g_m techniques for rail-to-rail CMOS amplifier input stages: a comparative study," *Proceedings of the International Symposium on Circuits and Systems*, pp. 2571-2574, May 2005.

[14] T. A. F. Duisters and E. C. Dijkmans, "A -90 dB THD Rail-to-Rail Input Opamp Using a New Local Charge Pump in CMOS," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, Jul. 1998.

[15] Y. Nakagome et al., "Experimental 1.5V 64Mb DRAM," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp-465-472 Apr. 1995.

[16] David J. Comer and Donald T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps", *IEEE Transactions of Circuits and Systems II: Express Briefs*, vol. 51, no. 1, pp. 8-14, Jan. 2004.

[17] B. Hernes and T. Saether, *Design Criteria for Low Distortion in Feedback Opamp Circuits*, Kluwer, 2003.

[18] Kamath, B. Y. T. et al., "Relationship between frequency response and settling time of operational amplifiers", *IEEE Journal of Solid-State Circuits*, vol. 9, no. 6, pp. 347-352, Dec. 1974.

[19] D. M. Monticelli, "A quad CMOS single-supply opamp with rail-to-rail output swing ," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 6, Dec. 1986.

[20] R. Hogervorst et al, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries ," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, Dec. 1994.

[21] K. de Langen and J. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, Oct. 1998.

[22] Barrie Gilbert, "Translinear circuits: a proposed classfication," *Electronics Letters*, vol. 11, no. 1, pp. 14-16, Jan. 1975.

[23] Rajiv Mantri et al., "Accurately measuring ADC-driving circuit settling time," Available: http://www.ti.com/lt/an/slyt262/slyt262.

[24] Nagendra Krishnapura and Rakshitdatta K. S., "A model-agnostic technique for simulating per-element distortion contributions," *Proc. 2013 IEEE Custom Integrated Circuits Conf.*, San Jose, 2013.

[25] J. J. Bussgang et al., "Analysis of nonlinear systems with multiple inputs," *Proc. IEEE*, vol. 62, pp. 1088-1119, Aug. 1974.

[26] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Boston, MA: Kluwer, 1998.

[27] P. Wambacq et al., "Symbolic simulation of harmonic distortion in analog integrated circuits with weak nonlinearities," *Proc. 1990 International Symp. on Circuits and Systems*, New Orleans, 1990, pp. 536-539.

[28] B. Hernes and W. Sansen, "Distortion in single-, two- and three-stage amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, pp. 846-856, May 2005.

[29] S. O. Cannizzaro et al., "Distortion analysis of miller-compensated three-stage amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, pp. 961-976, May 2006.

[30] A. Cooman et al., "Determining the dominant nonlinear contributions in a multistage op-amp in a feedback configuration", *Proc. 2012 SMACD*, Sep. 2012, pp. 205-208.

[31] P. Li and L. T. Pileggi, "Efficient per-nonlinearity distortion analysis for analog and RF circuits," *IEEE Trans. Comput.-Aided Des. Integr. Integrated Circuits and Systems Circuits Syst.*, vol. 22, pp. 1297-1309, Oct. 2003.

[32] *Virtuoso® Spectre® Circuit Simulator and Accelerated Parallel Simulator RF Analysis User Guide*, Product Version 12.1, Cadence Design Systems, October 2012.

[33] *Virtuoso® Spectre® Circuit Simulator RF Analysis Theory*, Product Version 12.1, Cadence Design Systems, October 2012.

[34] S. Pavan et al., "A power optimized continuous-time delta-sigma modulator for audio applications," *IEEE J. Solid-State Circuits*, vol. 43, pp. 351-360, Feb. 2008.

[35] Y. Miao and Y. Zhang, "Distortion modeling of feedback two-stage amplifier compensated with miller capacitor and nulling resistor", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, pp. 93-105, Jan. 2012.

[36] G. Palumbo and S. Pennisi, "High-frequency harmonic distortion in feedback amplifiers: analysis and application," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, pp. 328-340, Mar 2003.

[37] J. Chun and B. Murmann, "Analysis and Measurement of Signal Distortion due to ESD Protection Circuits," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2354-2358, Oct. 2010.

[38] Y. Papananos et al., "Design and implementation of a CMOS operational amplifier architecture with dual common-mode feedback loop," *Proc. 1996*

IEEE International Conference on Electronics, Circuits, and Systems, May 1990, pp. 904-907.

[39] N. Krishnapura et al., "A high-IIP3 third-order elliptic-filter with current-efficient feedforward-compensated opamps," *IEEE Transactions of Circuits and Systems II: Express Briefs*, vol. 58, no. 4, pp. 205-209, Apr. 2011.

[40] W. G. Garrett et al, "A monolithic differential-output operational amplifier," *Proc. 1972 IEEE International Solid State Circuits Conference*, pp. 174-175, 1972.

[41] J. Ramirez-Angulo et al., "High slew rate two stage A/AB and AB/AB op-amps with phase lead compensation at output node and local common mode feedback," *Proc. 2008 IEEE International Symposium on Circuits and Systems*, pp. 288-291, May 2008.

[42] K. de Langen and J. H. Huijsing, *Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Amplifiers*, Springer, 1999.

[43] M. Banu et al., "Fully differential operational amplifiers with accurate output balancing," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, June 1988.

[44] O. Rajaee and U. Moon, "Highly Linear Noise-Shaped Pipelined ADC Utilizing a Relaxed Accuracy Front-End", *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 502-515, Feb. 2013.

[45] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit", *IEEE Transactions of Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 12, pp. 906-917, Dec. 2003.

[46] Chembiyan Thambidurai and Nagendra Krishnapura, "On pulse position modulation and its application to PLLs for spur reduction", *IEEE Transactions of Circuits and Systems I: Regular Papers*, vol. 58, no. 7, pp. 1483-1496, July 2011.

List of publications based on thesis

International Journals

1. Nagendra Krishnapura and Rakshitdatta K. S., "A Model-Agnostic Technique for Simulating Per-Element Distortion Contributions," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, Vol. 61, no. 8, Aug. 2014 (to appear).

International Conferences

1. Nagendra Krishnapura and Rakshitdatta K. S., "A Model-Agnostic Technique for Simulating Per-Element Distortion Contributions," *Proceedings of the 2013 IEEE Custom Integrated Circuits Conference*, San Jose, Sep. 2013.