INVESTIGATION OF HYBRID FILTER BANK BASED ANALOG-TO-DIGITAL CONVERSION

A THESIS

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THESIS CERTIFICATE

This is to certify that the thesis titled **INVESTIGATION OF HYBRID FILTER BANK BASED ANALOG-TO-DIGITAL CONVERSION** , submitted by **RAJESH INTI**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Science**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

High sampling rate and high resolution analog-to-digital converters (ADCs) are required in a variety of applications, like wide band radio receivers, oscilloscopes and spectrum analyzers. Sample rates of hundreds of MSamples/sec and 10-12 bits of resolution is desirable. Traditionally, high speed converters have been implemented using time interleaving techniques, where an array of converters are used to sample the input data using skewed clocks. Circuit non-idealities like the deviation of skew between clocks from their intended value, gain and offset error in the ADC degrade the performance of this class of converters.

To circumvent the aforementioned problems in time interleaved converters, a hybrid filter bank (HFB) based approach is investigated in this thesis. In the HFB approach, all the converters sample using a single clock, but the input to each of these converters is separated in frequency domain by using continuous time analog filters. One way of separating the input signal in the frequency domain was proposed by Velazquez [Velazquez *et al.* (1998)]. In Velazquez's implementation, analog filters with a very sharp roll off were used mandating high order analog filters. Since integrating high order analog filters is a challenge in itself, we investigate the use of simpler filter transfer functions for signal separation. A 2-channel HFB with 10-bit resolution sampling at 80 MSamples/sec was designed in AMS (Austria Microsystems) 0.35 μm CMOS process. The IC was fabricated and characterized. Measured results are presented.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Analog-to-Digital Converters (ADCs) are key design blocks in modern communication systems. With tremendous advances in CMOS fabrication technology, most signal-processing functions are being moved to the digital domain for a low power, low cost, high yield and highly reconfigurable implementation. Many communication standards like Bluetooth and IEEE 802.11 a/b require ADCs with a resolution of 8-10 bits sampling at around 10-100 MSamples/sec [Xia *et al.* (2006)].

The achievable sampling rate and resolution of an ADC in a particular technology is dictated by the rate at which switched-capacitor circuits in the ADC can be operated. To achieve higher sampling rates, many ADCs sampling at lower rates can be used in parallel. Exploiting parallelism in A/D conversion can be done either in the time or frequency domains.

Traditionally, high speed converters have been implemented using time interleaving techniques, where an array of converters are used to sample the input data using skewed clocks. Non-idealities in the realization of multiple skewed clocks degrades the performance of this class of converters. To circumvent the problem of multiple clock generation in time interleaved converters, a new technique called hybrid filter bank (HFB) based A/D conversion was proposed in [Velazquez *et al.* (1998)]. As shown in Fig 1.1, the continuous time analog input signal V_{in} whose bandwidth is $\frac{Mf_s}{2}$ is

split into M frequency bands with bandwidth $\frac{f_s}{2}$ using analog continuous time filters $H_0(s)$, $H_1(s)\ldots$, $H_{M-1}(s)$. The effective bandwidth of the signal after filtering is only $\frac{f_s}{2}$, which is suitable for conversion by AD_0, $AD_1\ldots$, AD_{M-1} whose sampling rates are f_s. FIR filters $F_0(z)$, $F_1(z)\ldots$, $F_{M-1}(z)$ are used to reconstruct the digitized samples provided by AD_0, $AD_1\ldots$, AD_{M-1}. In Velazquez's implementation, analog filters with

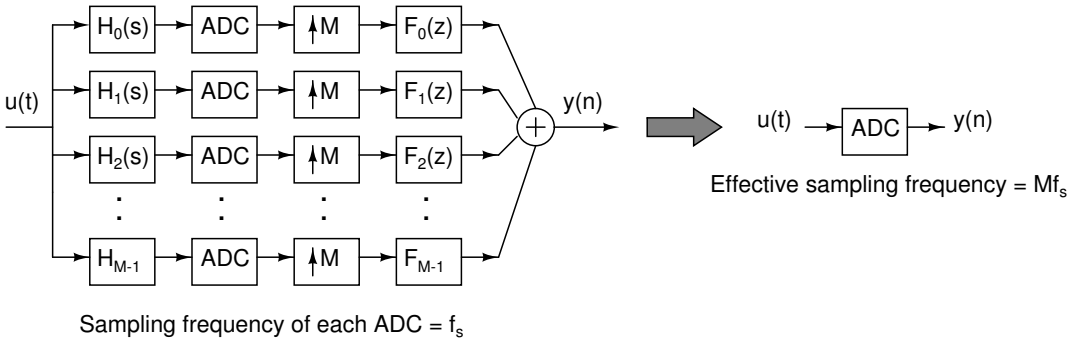


Figure 1.1: Velazquez's M-channel HFB implementation

sharp roll off are used mandating higher order analog filters. Designing such high order filters is a challenge in itself. High order filters are also sensitive to component variations. In this work, we will investigate the use of simpler analog filters. We investigate the use of simpler filters to accomplish the task of frequency domain A/D conversion. Specifically, we explore the possibility of building a 10-bit, two channel ADC sampling at 80 MSPS (Mega Samples Per Second) using the frequency domain approach.

1.2 Organization

Chapter 2 introduces the concepts and terminology in A/D conversion circuits. Dynamic and static characteristics of an ADC are discussed.

Chapter 3 describes HFB based A/D conversion. The procedure for the design of HFB based ADCs are outlined. Details regarding the design specifications of a 10-bit,

2-channel HFB based 80 MSPS ADC are provided.

Chapter 4 presents the design of a 10-bit, 40 MSPS pipeline ADC. The design of the multiplying DAC (MDAC) stage, the 3-bit termination Flash ADC and the digital error correction (DEC) logic will be dealt with.

Chapter 5 gives the design of an opamp-RC based band-pass filter with center frequency at 40 MHz. Techniques employed to measure the frequency response of the on-chip band-pass filter are discussed.

Chapter 6 presents details regarding printed circuit board (PCB) design, prototype IC characterization and measured results.

Chapter 7 gives the possible reasons for the observed error sources in the prototype IC. The differential nonlinearity (DNL) characteristic has been used to extract information pertaining to the multiplying DAC stages.

Chapter 8 concludes the thesis.

CHAPTER 2

ADC PERFORMANCE METRICS

In this chapter, we review the important metrics involved in the performance measurement of ADCs [AN748 (2001)] like integral/differential nonlinearity (INL/DNL), signal-to-quantization noise ratio (SNR), signal-to-quantization noise+distortion ratio (SNDR), spurious free dynamic range (SFDR), effective number of bits (ENOB) and figure of merit (FOM).

2.1 Analog-to-Digital Converter (ADC)

An ADC converts real time analog signals into digital codes. An ADC has a reference voltage or current against which the analog input is compared. The N-bit digital output word indicates what fraction of the reference quantity V_{ref} the input quantity V_{in} is. The input-output transfer function is described by

$$\text{Output-code } D_{\text{out}} = \frac{2^n V_{in}}{V_{ref}} \text{ (or) } \frac{2^N I_{in}}{I_{ref}}$$

where N is the number of bits that can be resolved by the ADC, V_{in} or I_{in} correspond to the input quantity and V_{ref} or I_{ref} correspond to the reference value against which the input will be compared. In the sections henceforth, we will look at the metrics involved in performance characterization of ADCs.

2.1.1 Resolution (N)

The resolution of an ADC is the number of bits in the digital output code. Alternatively, it can be defined as the size of the least significant bit (LSB). In a N-bit ADC, we will have 2^N possible levels. If the full scale range of the ADC is FSR, then

$$1\ LSB = \frac{FSR}{2^N}$$

2.1.2 Sampling rate (f_s)

Sampling frequency defines the number of samples per second taken from a continuous signal to obtain a discrete version of the signal. The common notation for sampling frequency is f_s.

2.1.3 Integral Nonlinearity (INL) / Differential Nonlinearity (DNL)

Each code width (LSB) of an ADC's transfer function should be uniform in size. Deviations of the code width from the ideal value of 1 LSB can be accounted using DNL/INL.

Differential nonlinearity (DNL)

Ideally, the voltage difference between each code transition should be equal to one LSB. Deviation of each code from an LSB is measured as DNL. For an ideal ADC, in which the differential nonlinearity coincides with DNL = 0 LSB, each analog step equals 1 LSB and the transition values are spaced exactly 1 LSB apart. It is defined as

follows:

$$DNL(n) = \frac{V_{actual}(n) - V_{actual}(n-1)}{LSB} - 1$$

where V_{actual}(n) is the voltage corresponding to input at which the ADC transitions from code (n-1) to n. A DNL error specification of less than or equal to 1 LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) with an increasing input signal. DNL is specified after gain error correction and offset error correction.

Integral nonlinearity (INL)

Integral Non-linearity, INL, describes the deviation from an ideal linear transfer curve for an ADC . The size and distribution of the DNL errors will determine the integral linearity of the converter. It is defined as follows:

$$INL(n) = \frac{V_{actual}(n) - V_{ideal}(n)}{LSB}$$

2.1.4 THD, SFDR, SNR, SNDR

An ADC's dynamic performance is specified using parameters obtained via spectral analysis and is measured by performing a Discrete Fourier transform (DFT) on the output codes of the ADC. In Fig 2.1, the fundamental frequency is the input signal frequency. This is the signal measured with the ADC. Contributors to noise include harmonic distortion, thermal noise, 1/f noise, and quantization noise. Nonlinearity in

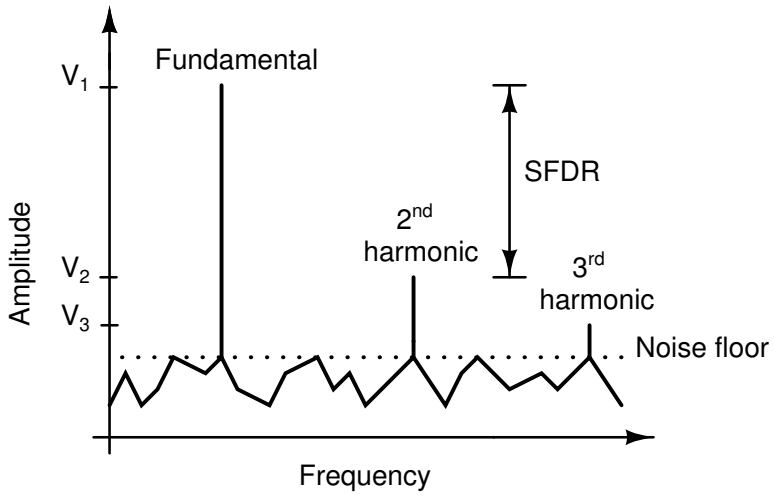


Figure 2.1: Spectrum of the output of an ADC to a single-tone input

the ADC results in harmonic distortion (HD). Such distortion is observed as "spurs" in the FFT at harmonics of the measured signal as showing in Fig 2.1. This distortion is referred to as total harmonic distortion (THD), and its power is calculated using

$$THD = 10 \log \left[\frac{V_2^2 + V_3^2 + \ldots + V_n^2}{V_1^2} \right] \text{ dB}$$

Spurious-free dynamic range (SFDR) is the difference between the magnitude of the measured signal and its highest spur peak. This spur is typically a harmonic of the measured signal. SFDR measurement is shown in Fig 2.1.

The signal-to-noise ratio (SNR) is the ratio of the root mean square (RMS) power of the input signal to the RMS noise power (excluding harmonic distortion), expressed in dB. SNR can be computed using,

$$SNR = 20 \log \left[\frac{V_{signal,rms}}{V_{noise,rms}} \right] \text{ dB}$$

For a N-bit ADC, the theoretical peak SNR = 6.02N + 1.76 dB for a full-scale sinusoidal

input.

Signal-to-noise plus distortion ratio (SNDR) gives a description of how the measured signal will compare to the noise and distortion. SNDR can be computed using

$$SNDR = 10 \log \left[\frac{V_1^2}{V_2^2 + V_3^2 + \ldots + V_n^2 + V_{noise}^2} \right] \text{ dB}$$

2.1.5 Effective number of bits (ENOB)

SNDR is often converted to effective-number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC. It is a measure of the effective resolution of the ADC accounting for quantization noise and distortion.

$$ENOB = \frac{\text{SNDR} - 1.76}{6.02} \text{ bits}$$

2.1.6 Figure of Merit (FOM)

FOM is used as an universal measure of ADC performance [Walden (1999)]. It enables us to compare the performances for ADC irrespective of the architecture, effective resolution (ENOB), sampling rate (f_s) and power dissipation (P_{diss}). It is computed using

$$FOM = \frac{P_{diss}}{2^{ENOB} f_s}$$

2.2 Characterization techniques

Any ADC prototype needs to be characterized to determine its static (INL, DNL) and dynamic (SNR,SNDR, SFDR and THD) specifications. Fig 2.2 shows the setup used for characterization of an ADC. In the sections that follow, techniques that are adopted for static and dynamic characterization are described.

To avoid spectral leakage, the clock and signal input sources should be synchronized. An bandpass/lowpass filter should be used in the signal path to suppress the second and third harmonics corresponding to the input signal, such that the harmonics do not limit the SNR measurement of the device under test (DUT).

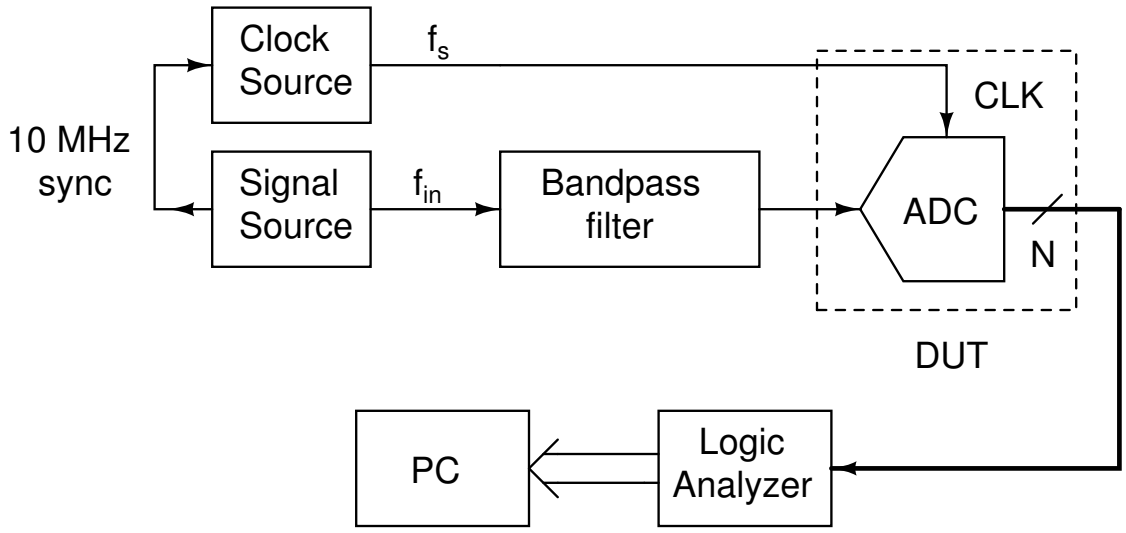


Figure 2.2: Setup for characterizing an ADC

2.2.1 Static characteristics INL / DNL

The histogram technique has been widely used for characterizing the static characteristics of an ADC [Doernberg *et al.* (1984), AN2085 (2003)]. This approach, also

referred to as the code density test, is performed in the amplitude-domain of a data converter. In a histogram test, a sine-wave signal is applied to the ADC, generating a corresponding distribution of digital codes at the output of the converter. Deviation from the corresponding output code distribution from the ideal distribution is used to estimate the INL/DNL.

2.2.2 Dynamic characteristics SNDR / SNR / SFDR / THD

Typically, single-tone inputs are used to compute the SNDR, SFDR and THD of an ADC prototype. To ensure that the 2^{nd} and 3^{rd} order distortion terms of the signal source does not affect the measurements, the harmonic suppressing filter should be a bandpass filter centered around the input frequency f_{in} and should provide sufficient attenuation of the distortion components.

CHAPTER 3

FILTER BANK BASED A/D CONVERSION

In this chapter, we briefly review time-interleaving A/D conversion. An alternative architecture i.e. the hybrid filter bank (HFB) based A/D conversion that overcomes the problems with the time-interleaved architecture is discussed. System level design aspects like choice of optimal analysis filters and computing the synthesis filters in a HFB based ADC are provided. The degradation of SNR due to the HFB technique in a generic M-channel ADC is derived.

3.1 Time-Interleaving based A/D conversion

Time interleaving in A/D conversion was introduced in [Black and Hodges (1980)]. Time-interleaved ADC systems employ the concept of running M ADCs at a sample rate that is 1/M of the overall system sample rate. Each channel is clocked at a phase that enables the system as a whole to sample at equally spaced increments of time, imitating the behavior of a single A/D converter sampling at full speed. In a two-converter example as shown in Fig 3.1, both ADC channels are clocked at one-half of the overall system's sample rate, and are 180^o out of phase with one another.

Matching between the individual channels has a direct impact on the dynamic range (DR) performance of a time-interleaved ADC system. Mismatches between the ADC channels result in DR degradation that in the output spectrum (to a single tone sine wave input) show up as spurious frequency components called image spur and offset

spur. The image spur associated with time-interleaved ADC systems are a direct result of gain and phase mismatches between the ADC channels. The offset spur is generated by offset differences between the ADC channels. The offset spur is independent of the input signal unlike the image spur.

Time interleaved ADCs with M-channels require clocks which are separated in phase by $\frac{360^o}{M}$ degrees. Clock skew degrades the performance of the system. For a detailed study of the behavior of the gain, phase and offset mismatches in time-interleaved ADC systems, the reader is referred to [Kurosawa *et al.* (2001)].

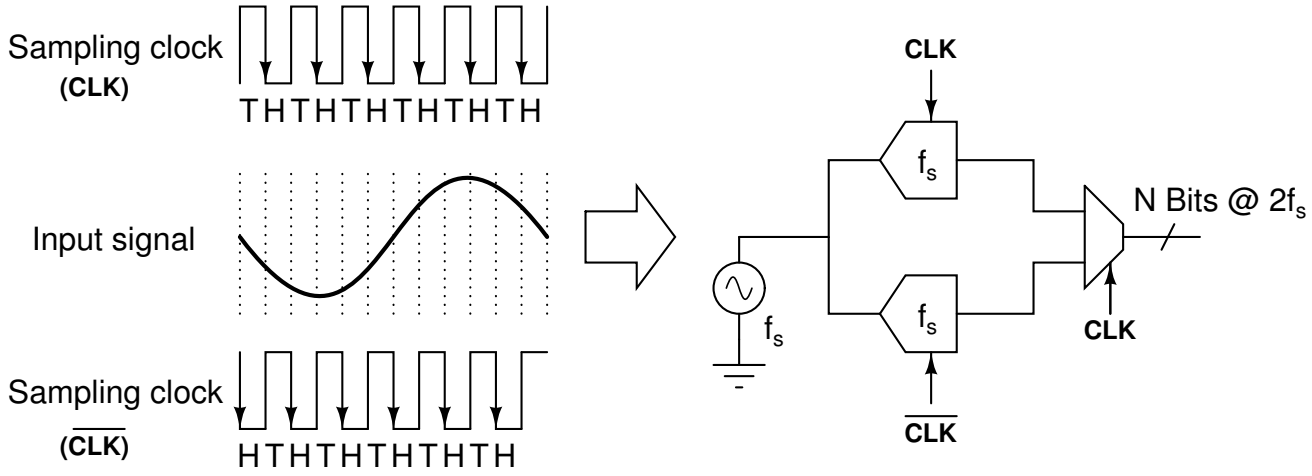


Figure 3.1: 2-channel time interleaved ADC

3.2 Hybrid Filter Bank based A/D conversion

Filter banks are used in a wide range of communication applications like sub-band coding, digital audio and image coding. The operation operation of a filter bank depicted in Fig 3.2 can be outlined as follows. Assume that the input signal has a bandwidth of f_B. The analysis filters $H_k(z)$ channelize the input signal u[n] into M sub-band each with a bandwidth of $\frac{f_B}{M}$. The sub-band signals are further down sampled by a

factor M. Sub-band processing (operations like coding, compression, quantization etc.) now happens at a rate which is $\frac{f_B}{M}$, which is M times smaller than the Nyquist frequency corresponding to u. After sub-band processing, the signal is upsampled by a factor M. Digital interpolation filters are used to generate the output.

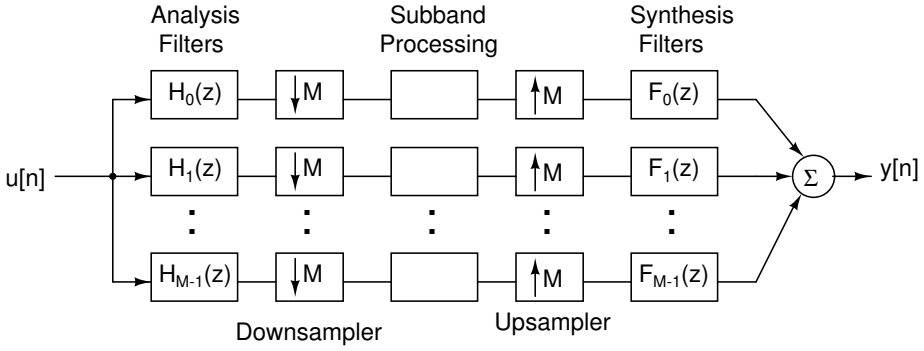


Figure 3.2: M-channel discrete-time filter bank

[Petraglia and Mitra (1992)] have reported a discrete-time filter bank based 2-channel ADC. The ADC uses 12-bit successive approximation ADCs sampling at 10 kHz to build a system whose effective sampling rate is 20 kHz. One of the disadvantages of a discrete time implementation is that it requires an up-front sample and hold circuit which operates the systems effective sampling rate i.e. 20 kHz in this example. Implementation of the discrete time analysis filters requires switched capacitor (SC) circuits whose maximum frequency of operation is limited.

Unlike the discrete-time filter bank, the hybrid filter bank (HFB) [Velazquez *et al.* (1998)] uses analog analysis filter $H_k(s)$ to allocate a frequency band to each ADC in the array and digital synthesis filters $F_k(z)$ to reconstruct the digitized signal. As will be seen in the sections that follow, HFB improves the speed and resolution of the conversion by attenuating the effects of mismatches between the converters, which would otherwise limit the maximum resolution achievable by the system [Velazquez *et al.* (1998)].

3.3 System level design aspects of a HFB based ADC

In this section, we will examine a generic M-channel HFB ADC. We assume analog analysis filters $H_k(s)$ and digital synthesis filters $F_k(z)$ as shown in the Fig 3.3. The sampling rate of each ADC shown is Fig 3.3 is denoted as is f_s Hz. The whole system emulates an ADC sampling at Mf_s Hz.

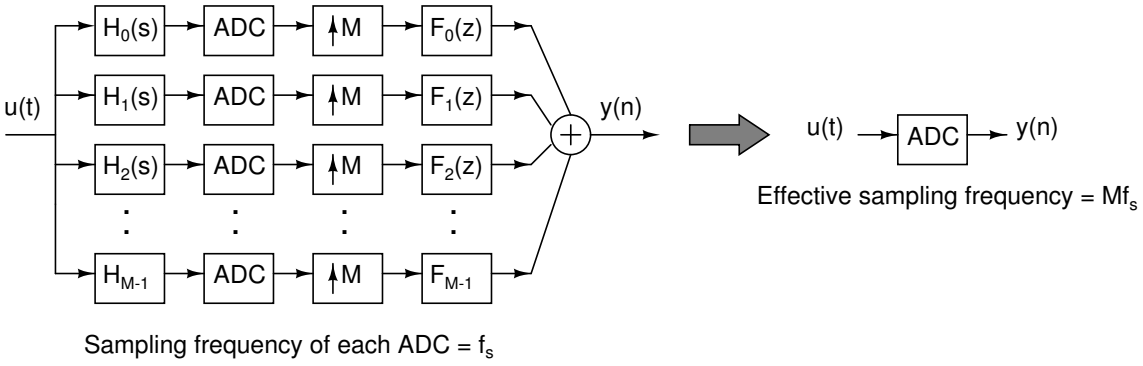


Figure 3.3: M-channel HFB based ADC

3.3.1 Operation of the M-channel HFB

For operation of the M-channel discrete time FB, the reader is referred to [Vaidyanathan (1993)]. In the M-channel HFB case, the outputs after each stage are as shown below -

After each analysis filter:

$$X_k(j\Omega) = U(j\Omega)H_k(j\Omega)$$

where Ω denotes the frequency in the continuous-time domain (in radians/sec).

After A/D conversion in each sub-band channel: Using $\omega = \Omega T_s$

$$V_k(j\omega) = \sum_{m=-\infty}^{m=+\infty} U(j(\omega - 2\pi m)/T_s) H_k(j(\omega - 2\pi m)/T_s)$$

After upsampling by M and the synthesis filter section:

$$W_k(j\omega) = \sum_{m=0}^{m=M-1} F_k(j\omega) U(j(M\omega - 2\pi m)/T_s) H_k(j(M\omega - 2\pi m)/T_s)$$

After the summer, the output is:

$$Y(j\omega) = \sum_{k=0}^{k=M-1} \sum_{m=0}^{m=M-1} F_k(j\omega) U(j(M\omega - 2\pi m)/T_s) H_k(j(M\omega - 2\pi m)/T_s)$$

Rearranging the output equation

$$Y(j\omega) = \sum_{m=0}^{m=M-1} U(j(M\omega - 2\pi m)/T_s) \sum_{k=0}^{k=M-1} H_k(j(M\omega - 2\pi m)/T_s) F_k(j\omega)$$

The desired output is $U(Mj\omega/T_s)$, which is the input $U(j\Omega)$ sampled at $f_s' = Mf_s = \dfrac{M}{T_s}$. The components $U(j(M\omega - 2\pi)/T_s), U(j(M\omega - 4\pi)/T_s) \ldots U(j(M\omega - (M-1)\pi)/T_s)$ are the aliasing components. To achieve perfect reconstruction, the scaling functions for the desired output should be a ideal delay element and the aliasing components should be zero. We use the the following definitions for the aliasing and distortion functions.

Distortion function :

$$T_0(j\omega) = \sum_{k=0}^{k=M-1} H_k(Mj\omega/T_s)F_k(j\omega) = Me^{-j\omega d} \tag{3.1}$$

Aliasing functions :

$$T_m(j\omega) = \sum_{k=0}^{k=M-1} H_k(j(M\omega - 2\pi m)/T_s)F_k(j\omega) = 0 \text{ for m = 1,2,3 ... M-1} \tag{3.2}$$

Equations [3.1,3.2] form a set M linear equations which can solved over the frequency range $0 < \omega \leq \pi$ to obtain the frequency response of the synthesis filters for pre-defined set of analysis filters $H_k(s)$. Using the standard Matlab **ifft** routine, we can obtain the impulse response for each $F_k(z)$.

3.3.2 Two-channel HFB

All our discussions henceforth will be based on the 2-channel HFB. In the sections that ensue, we will look into how to choose the continuous time analog filters $H_k(s)$, the computation of filter taps by solving for the synthesis filters $F_k(z)$, the maximum achievable SFDR and the SNR at the output of a 2-channel HFB ADC for the chosen analog filters.

The generic 2-channel HFB system shown in Fig 3.4 can be described by

$$\begin{bmatrix} H_0(2j\omega/T_s) & H_1(2j\omega/T_s) \\ H_0(j2(\omega-\pi)/T_s) & H_1(j2(\omega-\pi)/T_s) \end{bmatrix} \begin{bmatrix} F_0(j\omega) \\ F_1(j\omega) \end{bmatrix} = \begin{bmatrix} 2e^{-j\omega d} \\ 0 \end{bmatrix} \tag{3.3}$$

The synthesis filters $F_0(z)$ and $F_1(z)$ can be solved using Eqn 3.3. The variable **d** is the

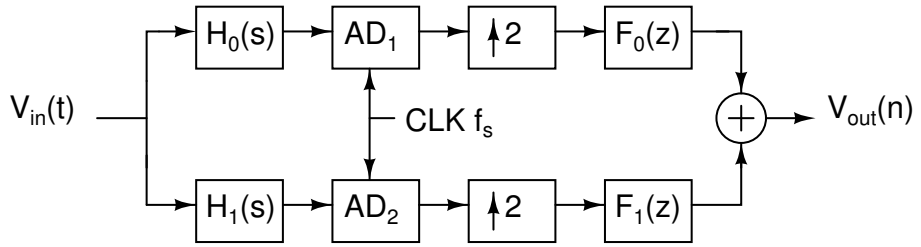


Figure 3.4: 2-channel HFB based ADC

delay of the system (typically an integer number of clock cycles). It is usually chosen to be approximately equal to half the length of the FIR filter i.e. if each of $F_k(z)$ are realized using 32 taps then d = 16. The desired distortion and aliasing functions T_0 and T_1 are given by -

$$T_0(j\omega) = H_0(2j\omega/T_s)F_0(j\omega) + H_1(2j\omega/T_s)F_1(j\omega) = 2e^{-j\omega d}$$

$$T_1(j\omega) = H_0(2j(\omega-\pi)/T_s)F_0(j\omega) + H_1(2j(\omega-\pi)/T_s)F_1(j\omega) = 0$$

3.3.3 System specifications

We aim to build a 10-bit 80 MSPS ADC using the 2-channel HFB architecture described above. The important building blocks are the analog analysis filters, the sub-band ADCs with a sampling rate of 40 MHz. The digital synthesis filters are implemented in software.

In the following sections, we will describe how the analog analysis filters are chosen, methods for computing the synthesis filter taps and the SNR computation of a HFB system.

3.4 Maximum achievable SFDR in a 2-channel HFB system

The resolution of the ADC to be used in an HFB system is limited by the maximum achievable SFDR of the HFB system. To compute SFDR, the ADCs are replaced by sample and hold (SAH) blocks which do not add quantization noise to the system. The value of SFDR can be computed by feeding a single tone input and measuring the power in the input tone to that of the aliasing tone. In a 2-channel HFB, SFDR is given by

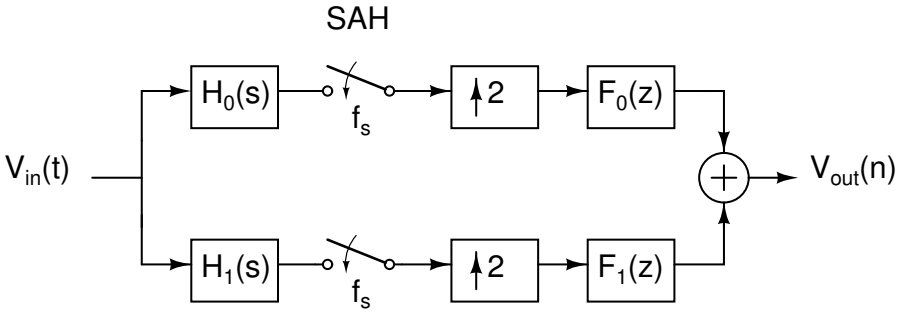


Figure 3.5: Setup to measure SFDR in a 2-channel HFB based ADC

$$SFDR\,(\text{dB}) = 20\log\left|\frac{T_0(j\omega)}{T_1(j\omega)}\right|_{\omega=\omega_{in}}$$

Table 3.1 shows the simulated and theoretically computed SFDR for three different cases of analog analysis filters.

Analysis Filters H_0 & H_1	FIR length L	$SFDR_{theoretical}$	$SFDR_{simulation}$
All pass & Biquad	32	112.1	112.5
3^{rd} order Butterworth LPF & HPF	128	144.2	144.9
5^{th} order Butterworth LPF & HPF	128	153.2	152.6

Table 3.1: Achievable SFDR in a 2-channel HFB measured at $\frac{f_{in}}{f_s} = \frac{7371}{8192}$

3.5 Choice of Optimal Analysis filters

High order analog analysis filters have a sharp roll off and result in synthesis filters which require a large number of taps for realization [Velazquez *et al.* (1998)]. RLC circuit based 2^{nd} order filter banks have been studied in [Petrescu *et al.* (2005)]. Lower order analysis filters result in synthesis filters with smooth roll off thereby requiring lesser number of taps. In this work, we use simple second order active-RC filters.

We will have to trade off SNR with the complexity of the analysis filters and number of taps in the synthesis filters. Use of lower order analysis filters implies that the quantization noise added by each ADC is will now be shaped by a synthesis filter with smoother roll off. The loss in SNR in HFB based ADCs is illustrated below.

We use two second order filter for $H_0(s)$ and $H_1(s)$ and optimize (ω_{LP}, ω_{BP}, Q_{LP}, Q_{BP}) to minimize the error constraint (which accounts for the deviation of the distortion function from a delay d cycles, and a scaled version of the aliasing function) given by

$$\epsilon = \int_0^{\pi} \left[\left| T_0(j\omega) - 2e^{-j\omega d} \right|^2 + 100 \left| T_1(j\omega) \right|^2 \right] d\omega$$

The generic $H_0(s)$ and $H_1(s)$ are given as

$$H_0(s) = \frac{b_0 + b_1 s}{a_0 + a_1 s + a_2 s^2}, \;\; H_1(s) = \frac{c_0 + c_1 s}{d_0 + d_1 s + d_2 s^2}$$

We use **fminsearch** in Matlab to minimize ϵ which is a function of (ω_{LP}, ω_{BP}, Q_{LP},

Q_{BP}). The transfer functions of the optimized filters are

$$H_0(s) = 1, \quad H_1(s) = \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

where $\omega_0 = 2\pi \times 40$ Mrad/sec, Q = 0.5. The frequency responses of the optimized analog analysis filters are shown in Fig 3.5 and the digital synthesis filters in Fig 3.5.

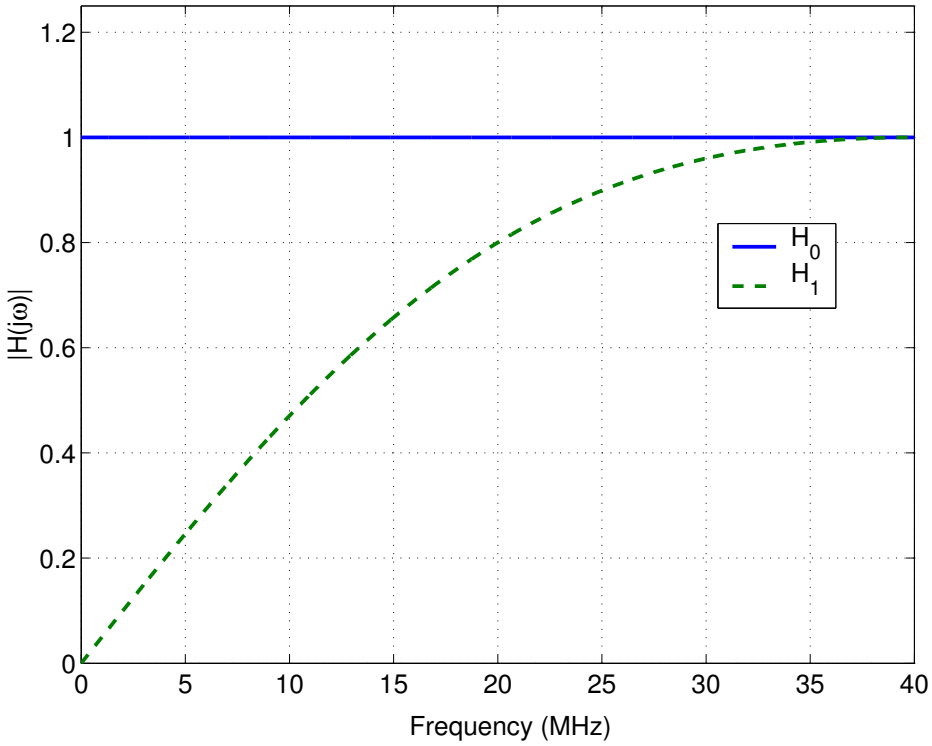


Figure 3.6: 2 channel HFB analysis filters

3.6 Computing the Synthesis filters

3.6.1 Delay optimization by minimizing energy loss due to synthesis filter truncation

Calculating the **ifft** of the ideal frequency response expressions obtained by solving equations [3.1,3.2] over N-points yields synthesis filters whose length is equal to N. By

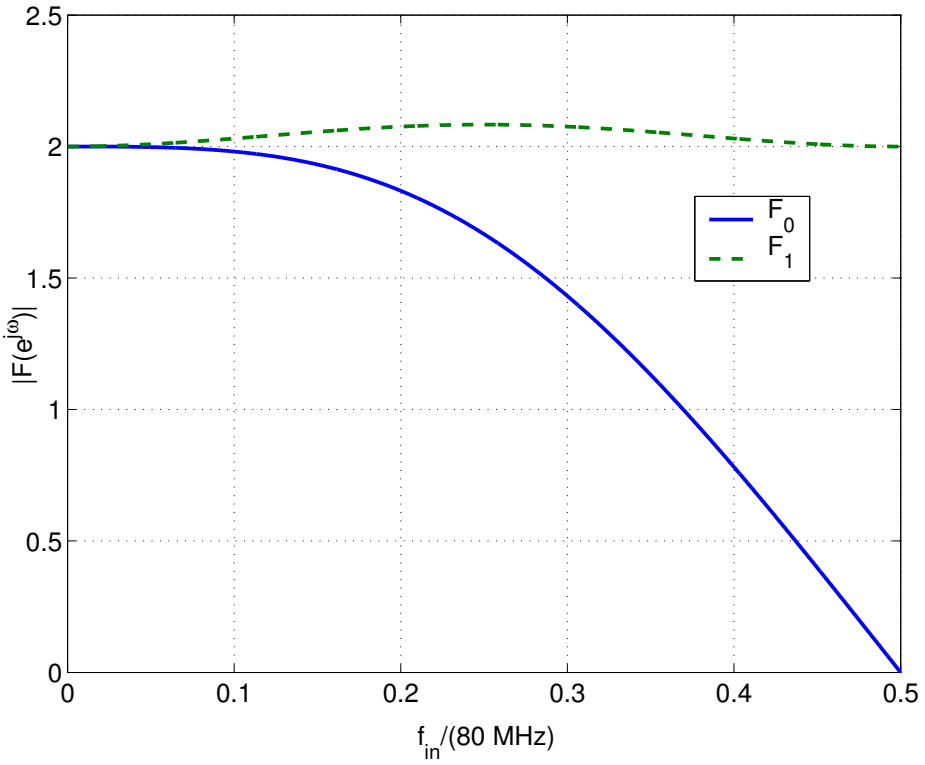


Figure 3.7: 2 channel HFB synthesis filters for 32-tap filters

using Parseval's theorem, the energy loss due to filter windowing to length L is given by

$$\epsilon = \sum_{k=0}^{1} \epsilon_k = \sum_{k=0}^{1} \int_0^{\pi} \left[\left| \overline{F}_k(j\omega) \right|^2 - \left| F_k(j\omega) \right|^2 \right] d\omega = \sum_{k=0}^{1} \sum_{n=L}^{N-1} (f_k(n))^2$$

. where $\overline{F}_k(j\omega)$ is the frequency response of the truncated filter of length L. The standard Matlab routine **fminsearch** is used to iteratively adjust delay d in equation [3.2] which will minimize energy loss ϵ .

3.6.2 Synthesis filters satisfying the LMSE criterion for white noise input

A white noise input sequence is generated and is band-limited to $f_{in,max} = f_s$ Hz using a high order Butterworth filter. We assume a length L for all the FIR synthesis filters. The length of the input sequence to the system is M. The length of the resulting output sequence will be $M + L - 1$.

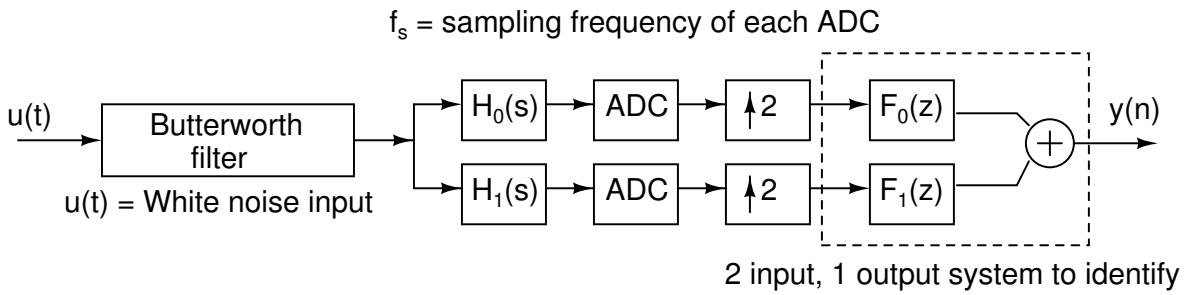


Figure 3.8: Synthesis filter identification using LMSE criteria

Since we have chosen the input sequence length as M and synthesis filter with L taps, the length of output y will be $M+L-1$. Denoting the inputs to the system shown in hashed lines as $x_0(n), x_1(n)$ of length M, we can express the output as

$$y(n) = \sum_{i=0}^{M+L-1} x_0(i) f_0(n-i) + \sum_{i=0}^{M+L-1} x_1(i) f_1(n-i)$$

The resultant output sequence y(n) can be represented in vector form as

$$Y = \sum_{k=0}^{1} X_k F_k$$

where the dimensions of Y, X, F [1] are $(M+L-1) \times 1$, $(M+L-1) \times (M+L-1)$, $(M+L-1) \times 1$. The class of filters f_k which result in the least reconstruction error E^2 can be obtained by solving

$$\frac{dE^2}{dF} = 0 \text{ where } E^2 = (Y - \sum_{k=0}^{1} X_k F_k)^T (Y - \sum_{k=0}^{1} X_k F_k) \tag{3.4}$$

[1] Y,X,F are used to denote vectors and should not be confused with frequency response.

The solution to equation [3.4] can be written as

$$\begin{bmatrix} X_1^T X_1 & X_1^T X_2 \\ X_2^T X_1 & X_2^T X_2 \end{bmatrix}_{dxd} \begin{bmatrix} F_1 \\ F_2 \end{bmatrix}_{dx1} = \begin{bmatrix} X_1^T Y \\ X_2^T Y \end{bmatrix}_{dx1}$$

where the dimension $d = 2(M + L - 1)$. Solving the above equation will yield the synthesis filters satisfying LMSE criteria for white noise input.

3.6.3 SNR degradation in HFB based ADCs

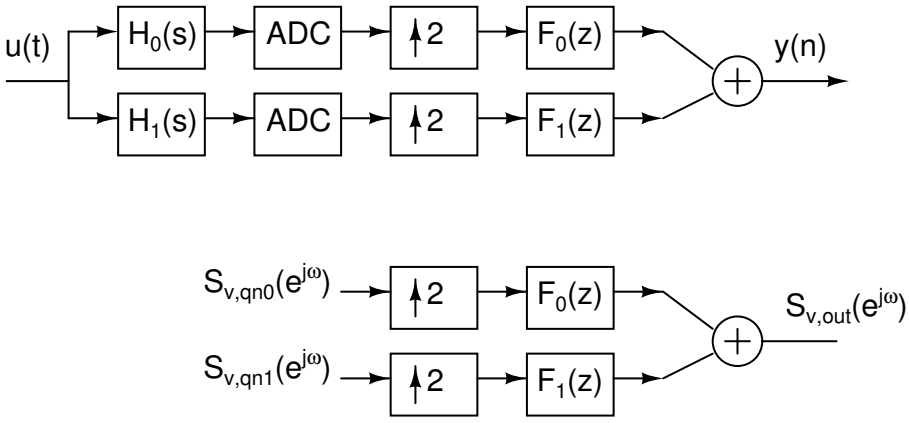


Figure 3.9: Computing SNR at the output in a 2-channel HFB based ADC

Fig 3.9 shows a two channel HFB based ADC. The quantization noise signal path is also shown in the figure. We need to compute $S_{v,out}(e^{j\omega})$ as a function of $S_{v,qn0}(e^{j\omega})$, $S_{v,qn1}(e^{j\omega})$ and integrate over frequency to compute the quantization noise power at the output. We will first look at the effect of upsampling on quantization noise power.

Effect of upsampling on $S_{v,qn}(e^{j\omega})$

Fig 3.10 shows examples of the input and output spectrum's of two different inputs when passed through an upsample by 2 block. From Fig 3.10 it can be seen that the

integrated quantization noise power comes down by a factor 2 due to upsampling. But there will be no change in SNR due to upsampling because the signal power will also come down by a factor 2. Assuming that the input sequence length is N,

$$\begin{aligned} X(e^{j\omega}) &= x[0] + x[1]e^{-j\omega} + x[2]e^{-j2\omega} \ldots + x[N-1]e^{-j(N-1)\omega} \\ &= \sum_{n=0}^{N-1} x[n]e^{-j\omega n} \end{aligned}$$

After upsampling by a factor 2,

$$\begin{aligned} X_{up}(e^{j\omega}) &= x[0] + x[1]e^{-j2\omega} + x[2]e^{-j4\omega} \ldots + x[2N-2]e^{-j(2N-2)\omega} \\ &= \sum_{n=0}^{N-1} x[n]e^{-j2\omega n} = X(e^{j2\omega}) \end{aligned}$$

From Fig 3.10, it can be seen that upsampling compresses the discrete time fourier transform (DTFT) by a factor of 2 along with the ω axis.

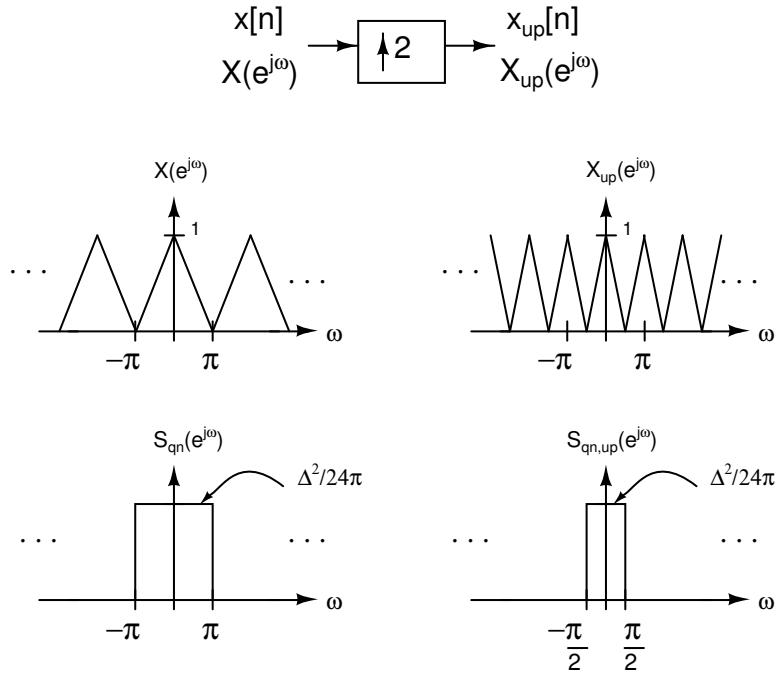


Figure 3.10: Interpolation by factor 2

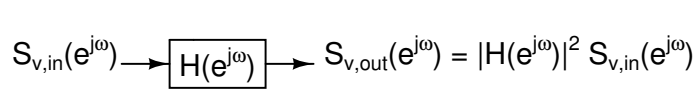


Figure 3.11: Effect of filtering on $S_{v,qn,up}(e^{j\omega})$

Effect of filtering on $S_{v,qn,up}(e^{j\omega})$

Fig 3.11 shows the effect of filtering of process with spectral density $S_{v,in}(e^{j\omega})$ with a filter H($e^{j\omega}$). From Fig 3.9, the integrated quantization noise power at the output can be written as

$$\begin{aligned}
P_{qn,out} &= \int_{\frac{-\pi}{2}}^{\frac{\pi}{2}} S_{v,qn0,up}(e^{j\omega})|F_0(e^{j\omega})|^2\, d\omega + \int_{\frac{-\pi}{2}}^{\frac{\pi}{2}} S_{v,qn1,up}(e^{j\omega})|F_1(e^{j\omega})|^2\, d\omega \\
&= \frac{\Delta^2}{24\pi}\Big[\int_{\frac{-\pi}{2}}^{\frac{\pi}{2}} |F_0(e^{j\omega})|^2\, d\omega + \int_{\frac{-\pi}{2}}^{\frac{\pi}{2}} |F_1(e^{j\omega})|^2\, d\omega\Big] \\
&= \frac{\Delta^2}{24\pi} \times \pi\Big[\sum_{i=0}^{L-1} f_0(i)^2 + \sum_{i=0}^{L-1} f_1(i)^2\Big] \qquad \text{(By using Parseval's theorem)} \\
&= \frac{\Delta^2}{12}\Big[\frac{1}{2} \times \sum_{k=0}^{1}\sum_{i=0}^{L-1} f_k(i)^2\Big]
\end{aligned}$$

In general, for a M channel HFB, the integrated quantization noise power is given by

$$P_{qn,out} = \frac{\Delta^2}{12}\Big[\frac{1}{M} \times \sum_{k=0}^{M-1}\sum_{i=0}^{L-1} f_k(i)^2\Big]$$

and the SNR for a M channel HFB is given by

$$\text{SNR}_{out}[\text{dB}] = 6.02N + 1.76 - 10\log_{10}\Big[\frac{1}{M} \times \sum_{k=0}^{M-1}\sum_{i=0}^{L-1} f_k(i)^2\Big]$$

Simulation results on various 2-channel HFBs are shown in in Table 3.2. The simulation SNR is in close agreement with the theoretically computed SNR.

Analysis Filters H_0 & H_1	FIR length L	$SNR_{theoretical}$	$SNR_{simulation}$	ENOB
All pass & Biquad	32	56.7	56.5	9.1 bits
3^{rd} order Butterworth LPF & HPF	128	58.9	59.1	9.5 bits
5^{th} order Butterworth LPF & HPF	128	58.8	58.5	9.4 bits

Table 3.2: SNR results on a 2-channel HFB

Fig 3.12 shows the simulated SNDR for a 2-channel HFB realized using "All pass & Biquad" analog filters. The resolution of the ADC used in the simulations was 10-bits.

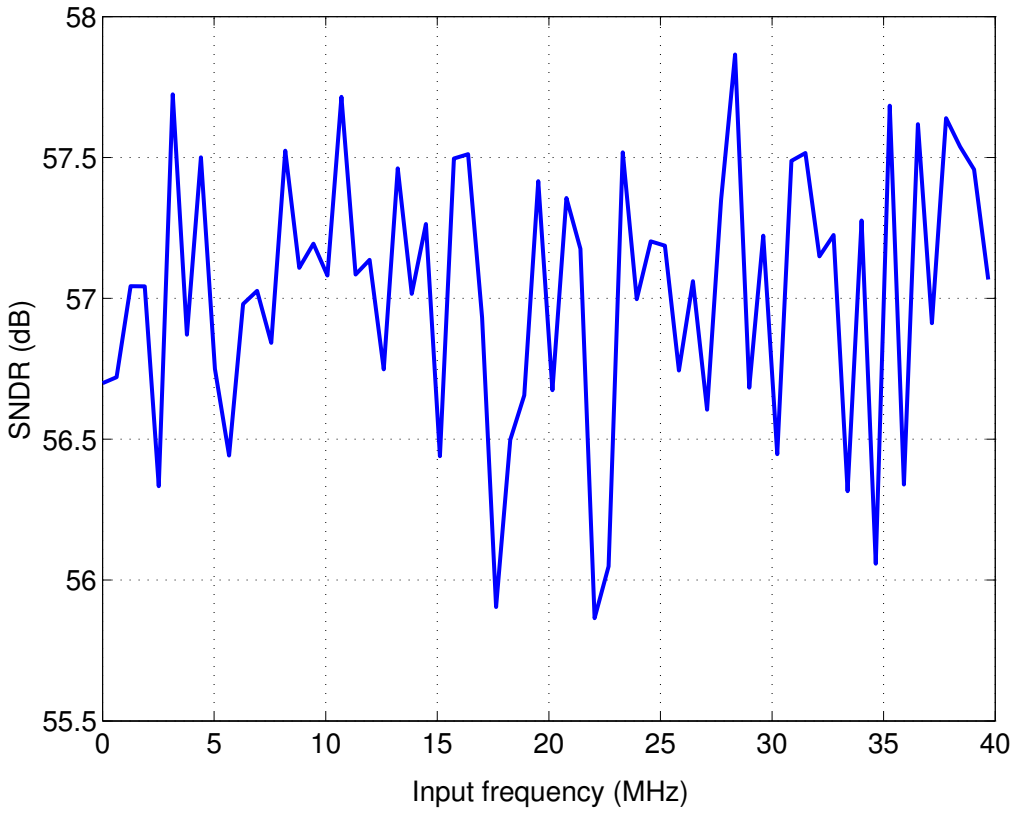


Figure 3.12: SNR simulation for a 2-channel HFB realized using "All pass & Biquad" analog filters

CHAPTER 4

DESIGN OF A 10-BIT, 40 MSPS PIPELINE ADC

In this chapter we discuss the design details of a 10-bit 40 MSPS pipeline ADC in a 0.35 μm CMOS process.

4.1 Architecture of the pipelined ADC

Pipeline ADCs are being employed in a wide range of applications, including digital receiver, base station, CCD imaging, ultrasonic medical imaging, digital video (e.g. HDTV), xDSL, cable modem and fast Ethernet. Pipeline ADCs provide high resolutions at high throughput rates at the expense of latency.

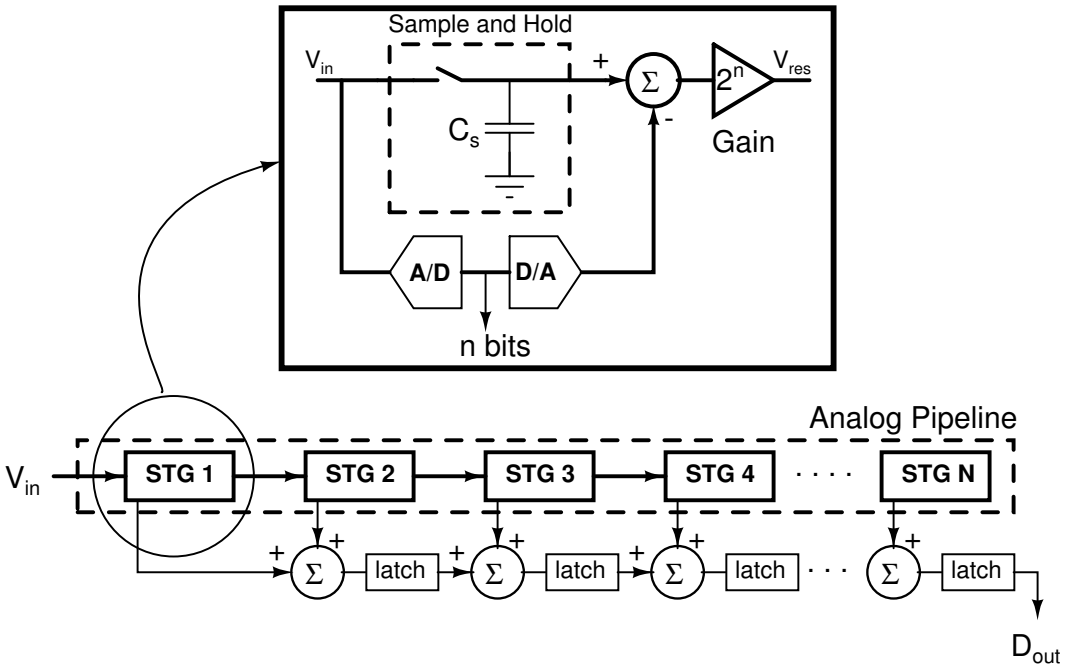


Figure 4.1: Architecture of a generic pipelined ADC

The sample and hold in the first stage is used to sample the input. Subsequent stages sample the residue of the previous stage. Thus the throughput rate is independent of the

number of stages in the pipeline. The amplifier with gain 2 is used to amplify the residue before passing it onto the next stage [Cho *et al.* (1994)]. By doing this, the resolution requirements for the subsequent stages can be relaxed. The DAC and gain 2 amplifier together will be termed as Multiplying-DAC (MDAC).

Fig 4.1 shows the block diagram of a generic pipeline ADC with N-bit resolution. Comparator offsets for the architecture shown in Fig 4.1 needs to be atleast one bit better than the overall resolution of the ADC. The use of the 1.5 bits/stage architecture [Lewis *et al.* (1992)] alleviates the offset requirements on the MDAC comparators.

Fig 4.2 shows the architecture of the 10-bit pipelined ADC. The ADC is designed for 10-bit resolution (capacitors chosen for 10-bit resolution) but utilizes 11-bit arithmetic. The opamp sharing technique is used to reduce the number of opamps [Nagaraj *et al.* (1997)]. By using opamp sharing, two stages as shown in Fig 4.1 can be merged into a single stage and the number of required opamps can be halved.

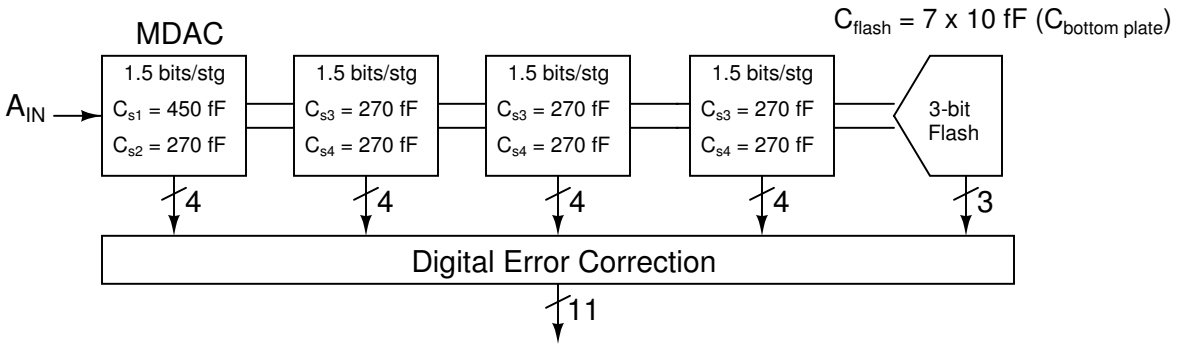


Figure 4.2: Architecture of the 10-bit pipelined ADC

4.2 MDAC stage input-output characteristics

The input-output characteristic of each 1.5 bits/stage MDAC is defined below :

$$V_{\text{RES}} = \begin{cases} 2V_{\text{IN}} + V_{\text{REF}} & \text{if } V_{\text{IN}} < -\dfrac{V_{\text{REF}}}{4} \\ 2V_{\text{IN}} & \text{if } |V_{\text{IN}}| \leq \dfrac{V_{\text{REF}}}{4} \\ 2V_{\text{IN}} - V_{\text{REF}} & \text{if } V_{\text{IN}} > \dfrac{V_{\text{REF}}}{4} \end{cases}$$

In the above equations, $2\,V_{\text{REF}}$ denotes the peak-peak swing of the input signal to be quantized. As shown in Fig 4.3, the three important blocks in each MDAC stage are:

- Closed amplifier with gain = 2
- Bootstrapped sampling switches
- Comparators which generate the V_{dac}

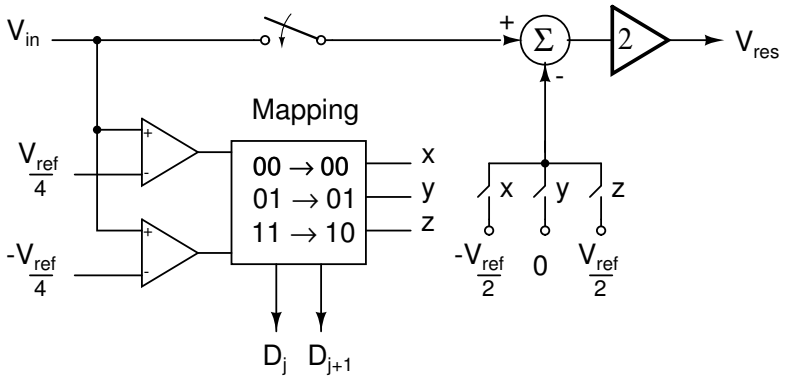


Figure 4.3: Important sub-blocks in a MDAC stage

Implementation details of each of the constituent blocks are described in subsequent sections. Fig 4.4 shows the input/output characteristics of a single MDAC stage. Using the opamp sharing technique, two MDAC stages can be realized using only opamp rather than two. Fig 4.5 shows the implementation of two MDAC stages in which the hold phase for first stage is ϕ_h and the hold phase for the second stage is ϕ_s. Clocks ϕ_{sd} and ϕ_{hd} are delayed versions of ϕ_s and ϕ_h.

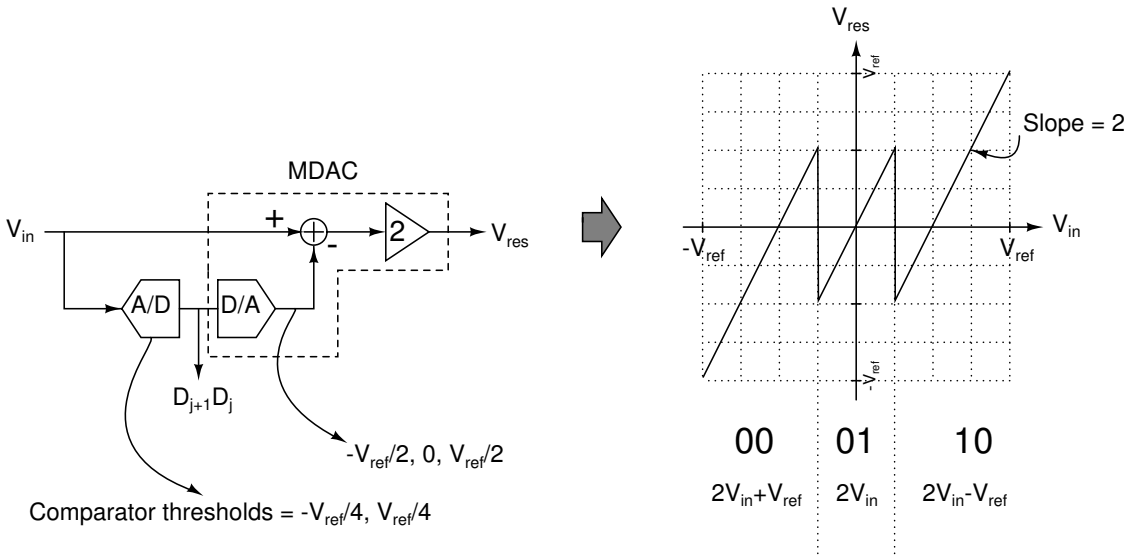


Figure 4.4: MDAC stage input-output characteristic

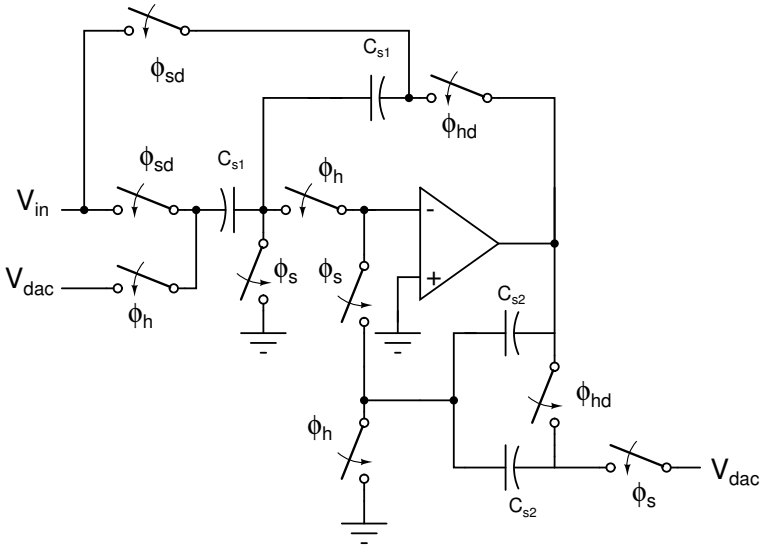


Figure 4.5: Opamp shared MDAC stage

4.3 Design of MDAC stage

MDAC stage is the most critical block. Before starting the design of the MDAC stage, the specifications for all the following parameters need to fixed. They are -

- Value of sampling capacitor C_{sample}.
- Open loop DC gain of the opamp.
- Unity-Gain Bandwidth (UGB) of the opamp.

4.3.1 Arriving at the opamp specifications

Value of C_{sample}

The choice of a particular C_{sample} is constrained by two parameters - thermal noise and capacitor matching. Poly-Poly capacitors are used for realizing the capacitors. Constraining the noise contribution due to the sampling capacitor to be 0.1 LSB, we get

$$\sqrt{\frac{kT}{C_{sample}}} < 0.195 \text{ mV} \Rightarrow C_{sample} > 108 \text{ fF}$$

The matching between the capacitors should be of 10-bit accuracy.

$$\sigma_{\frac{\Delta C}{C}} = \frac{1.2}{\sqrt{WL}}\%\mu m \Rightarrow WL \geq 151\mu m^2$$

We will choose a sampling capacitor of 450 fF which will require an area of 380 μm^2.

Value of A_{dc}, Unity-gain Bandwidth f_u

The open loop dc gain of the first MDAC opamp has to atleast 2^{n+1} where n is the effective resolution of the opamp.

$$A_{dc} \geq 2^{11} = 2048 \approx 66 \text{ dB}$$

The UGB of the opamp is determined the required setting time and the feedback factor of the MDAC stage. The MDAC stage has an ideal feedback factor β = 0.5, but due to the presence of parasitic capacitances at the opamp inputs, we will see a degradation in the β factor. Assuming a settling error in half a clock period (12.5 ns) for the first stage $\leq \frac{V_{LSB}}{2}$ of 10-bit ADC,

$$V_{FS}.e^{-\frac{t}{\tau}} \leq \frac{V_{LSB}}{2}$$

$$\frac{1}{\tau} = \beta w_u \Rightarrow f_u \geq 200 \text{ MHz}$$

The opamp to be designed should have minimum dc gain of 66 dB and UGB of 200 MHz.

4.3.2 Opamp topology

A gain boosted telescopic opamp is used in the MDAC stage [Bult and Geelen (1990)]. The schematic of the gain boosted amplifier is shown in Fig 4.6. The gain boosted amplifier consists of 5 individual amplifiers to achieve the entire gain - one main telescopic cascode opamp, 2 nMOS folded cascode amplifiers and 2 pMOS folded

cascode amplifiers.

Assuming that the overdrive of each device in the telescopic cascode opamp is chosen as Δ, the gain-boost amplifier (GBA) for device M_2 will sense voltages of the order of 2Δ and drive outputs in the order $V_T + 3\Delta$. Hence a pMOS folded cascode is used as the GBA for device M_2. Similarly the GBA for device M_3 will sense voltages of the order of $V_{DD} - \Delta$ and drive outputs in the order V_{DD} - V_T - 2Δ. Hence a nMOS folded cascode is used as the GBA for device M_3.

We study the design of each of the 3 opamps (telescopic cascode, nMOS folded cascode and pMOS folded cascode) independently and finally arrive at the gain boosted telescopic opamps specification. Sizes of the transistors shown in Fig 4.6 are shown in the telescopic cascode amplifier section.

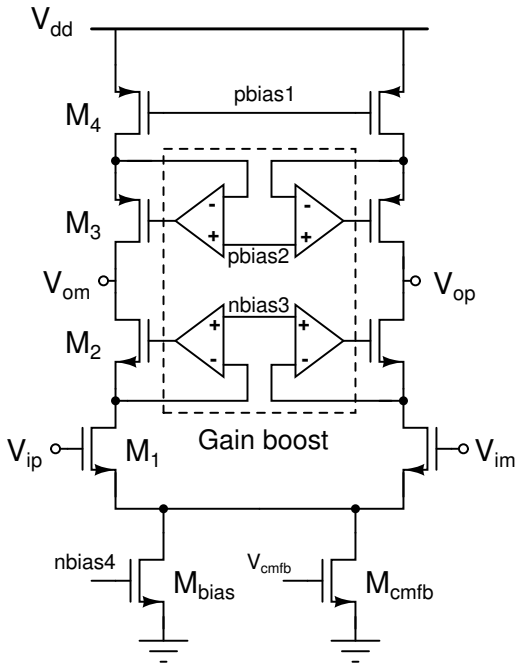


Figure 4.6: MDAC stage opamp architecture

4.3.3 Design of the telescopic opamp

Fig 4.7 shows the schematic of the telescopic opamp without the gain boosting amplifiers. Table 4.7 shows the device dimensions, the g_m and r_o of the devices used. The output common mode is controlled by having a tunable tail current source whose value is $\frac{1}{32}$ of the entire tail current. The dominant pole is determined by the load capacitor and g_{m1}. The DC gain of the opamp is given by

$$A_{ol} = g_{m1}(R_{n,cascode}||R_{p,cascode})$$

$$= g_{m1}(g_{m2}r_{o2}r_{o1}||g_{m3}r_{o3}r_{o4})$$

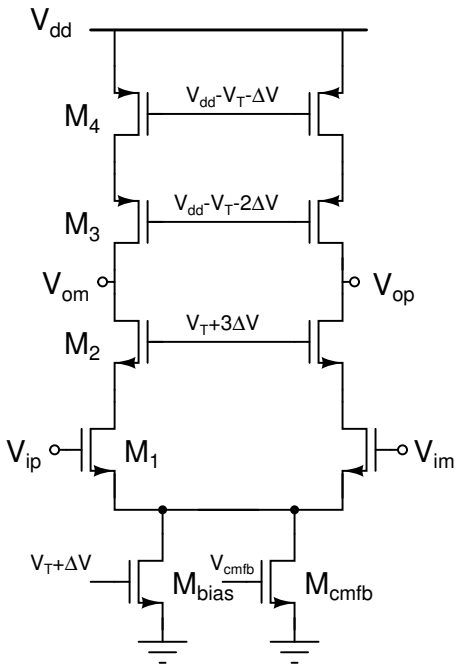


Figure 4.7: Telescopic opamp without the gain boosting amplifiers

Tab.4.1 shows the simulated open loop response of the telescopic cascode opamp.

	M_{bias}	M_{cmfb}	M_1	M_2	M_3	M_4
Size	$62(\frac{2}{0.5})$	$2(\frac{2}{0.5})$	$64(\frac{2}{0.5})$	$64(\frac{2}{0.5})$	$96(\frac{2}{0.35})$	$96(\frac{2}{0.35})$
I (mA)	1.966	0.052	1.009	1.009	1.009	1.009
ΔV (mV)	232	223.2	237.7	238.4	320	330
g_m (mS)	5.726	0.172	6.1	6.387	5.67	5.27
r_o (kΩ)	2.56	114.1	4.16	13.36	4.49	3.33

Feature	Achieved response
DC gain	52 dB
Phase Margin (PM)	81^o
UGB with C_L = 1.2 pF	700 MHz

Table 4.1: Achieved open loop response of the telescopic cascode opamp

4.3.4 Design of the gain boosting amplifiers - nMOS folded cascode opamp

Fig 4.8 shows the schematic of the nMOS folded cascode opamp. Table 4.2 shows the device dimensions, the g_m and r_o of the devices used. The frequency response of the gain boosting amplifier is not crucial compared to the response of the telescopic cascode itself [Bult and Geelen (1990)].

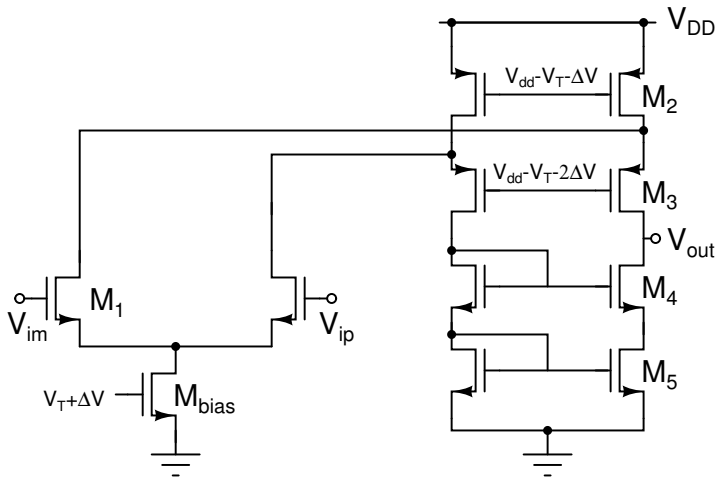


Figure 4.8: nMOS folded cascode gain boosting amplifier

The small signal DC gain is given by

$$A_{ol} = g_{m1}(R_{n,cascode}||R_{p,cascode})$$

$$= g_{m1}(g_{m3}r_{o3}r_{o2}||g_{m4}r_{o4}r_{o5})$$

The load capacitance seen by the opamp will be equal to the parasitic capacitances at the gate of M3 in Fig 4.7.

	M_{bias}	M_1	M_2	M_3	M_4	M_5
Size	$32(\frac{1}{1})$	$16(\frac{1}{0.35})$	$36(\frac{1.5}{0.75})$	$36(\frac{1.5}{0.75})$	$12(\frac{1}{0.5})$	$12(\frac{1}{0.5})$
I (μA)	97.1	48.5	93.7	45.1	45.1	45.1
ΔV (mV)	196	145	271	198	175	166
g_m (mS)	0.706	0.563	0.645	0.453	0.411	0.403
r_o (kΩ)	591.3	84.67	88.1	281.5	260..6	257.5

Table 4.2: Transistor sizes of the nMOS folded cascode opamp

Feature	Achieved response
DC gain	69.5 dB
Phase Margin (PM)	67^o
UGB with C_L = 1 pF	75 MHz

Table 4.3: Achieved open loop response of nMOS folded cascode opamp

4.3.5 Design of the gain boosting amplifiers - pMOS folded cascode opamp

Fig 4.9 shows the schematic of the pMOS folded cascode opamp. Table 4.4 shows the device dimensions, the g_m and r_o of the devices used.

The small signal gain is given by

$$A_{ol} = g_{m1}(R_{n,cascode}||R_{p,cascode})$$

$$= g_{m1}(g_{m3}r_{o3}r_{o2}||g_{m4}r_{o4}r_{o5})$$

The load capacitance seen by the opamp will be equal to the parasitic capacitances at the gate of M2 in Fig 4.7.

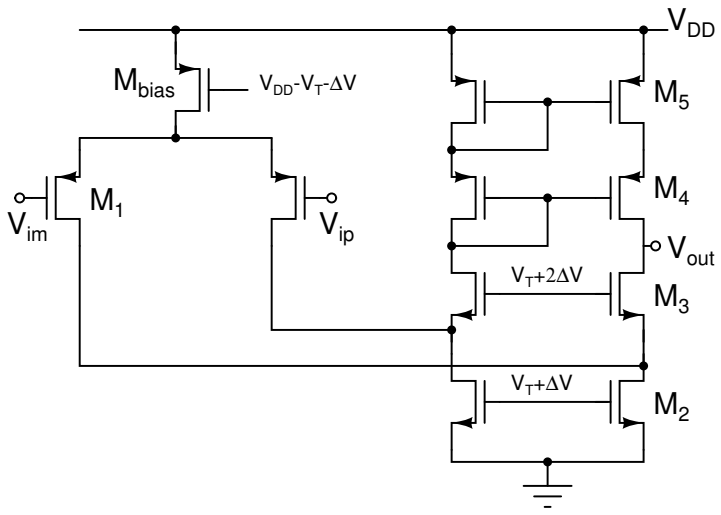


Figure 4.9: pMOS folded cascode gain boosting amplifier

	M_{bias}	M_1	M_2	M_3	M_4	M_5
Size	$32(\frac{1}{1})$	$16(\frac{1}{0.35})$	$12(\frac{1}{0.5})$	$12(\frac{1}{0.5})$	$36(\frac{1.5}{0.75})$	$36(\frac{1.5}{0.75})$
I (μA)	96.3	48.1	97.3	49.1	49.1	49.1
ΔV (mV)	388	271	236	181	210	200
g_m (mS)	0.43	0.36	0.57	0.43	0.47	0.47
r_o (kΩ)	236.7	78.7	84.31	220.2	257.8	237.5

Table 4.4: Transistor sizes of the pMOS folded cascode opamp

Feature	Achieved response
DC gain	63 dB
Phase Margin (PM)	70^o
UGB with C_L = 1 pF	47 MHz

Table 4.5: Achieved open loop response of pMOS folded cascode opamp

4.3.6 Biasing the opamp

5 important bias voltages need to generated for biasing the opamp. They are vcmi ($\approx V_T+2\Delta V$), pbias1 ($\approx V_{DD}-V_T-\Delta V$), pbias2 ($\approx V_{DD}-\Delta V$), nbias3 ($\approx 2\Delta V$) and nbias4 ($\approx V_T+\Delta V$), where $\approx \Delta V$ is the assumed overdrive of the tail current source.

Figs 4.10, 4.11 and 4.12 show the generation of each of these voltages respectively. The opamp along with the bias circuit is shown in each figure for sake of clarity.

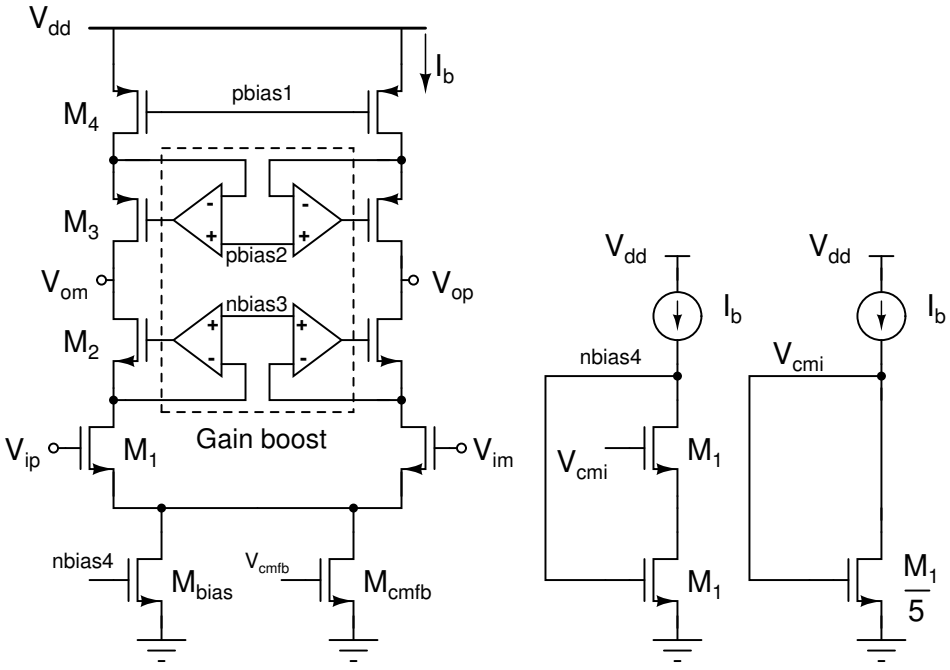


Figure 4.10: Biasing - Generation of vcmi, nbias4

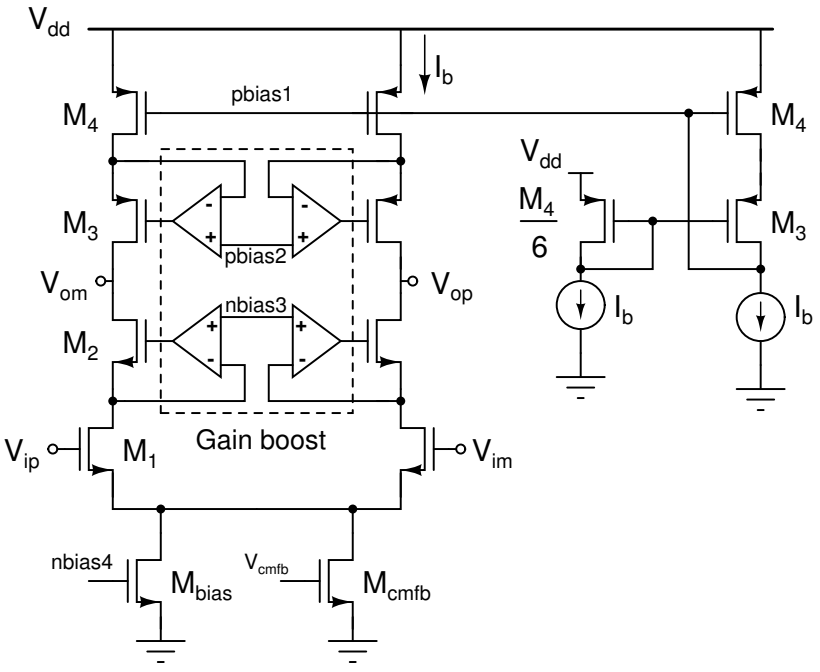


Figure 4.11: Biasing - Generation of pbias1

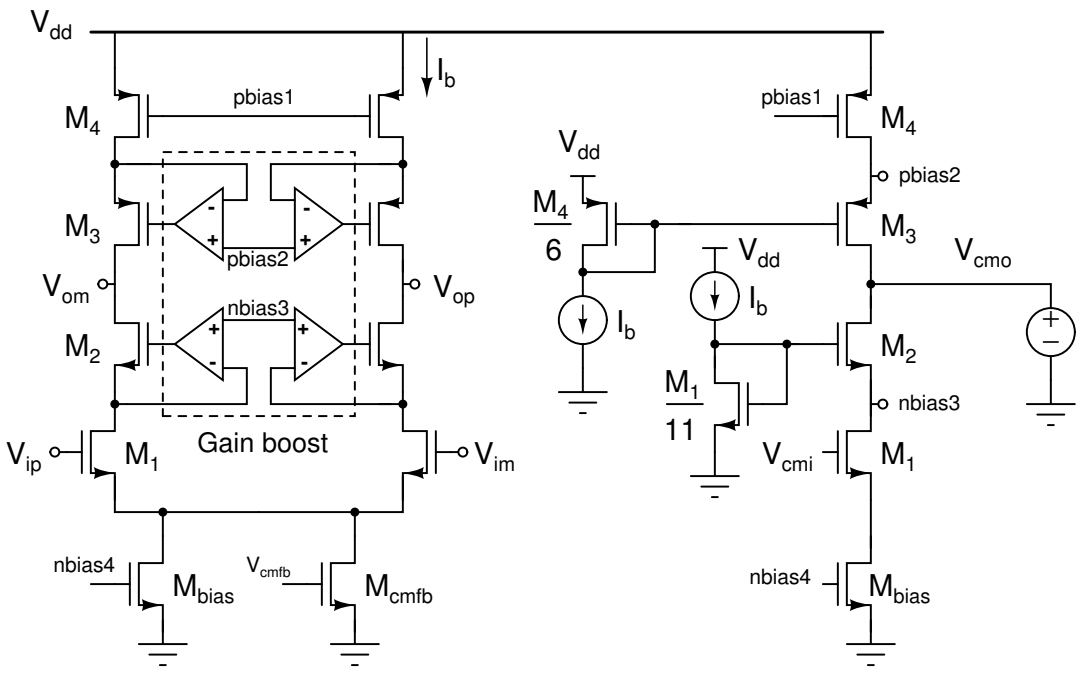


Figure 4.12: Biasing - Generation of pbias2, nbias3

4.3.7 Common-mode feedback loop

A switched capacitor common feedback loop [Choksi and Carley (2003)] is used to control the output common mode. The desired output common mode is 1.5 V. Each of the switches were nMOS with dimensions $2(\frac{0.5}{0.35})$. With the inputs tied to input common mode, the output common mode was verified to settle to 99% V_{cmo} in 12.5 ns.

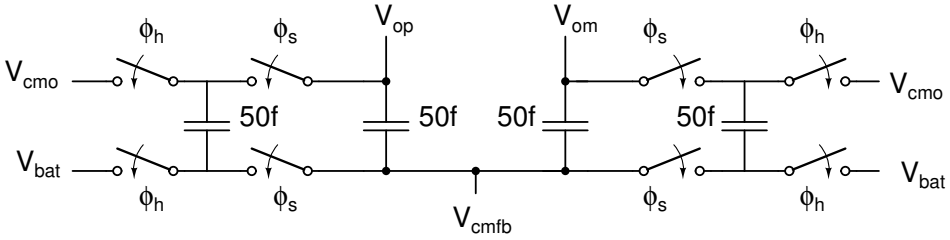


Figure 4.13: Switched capacitor CMFB

4.3.8 Opamp noise analysis

For noise analysis, the equivalent half circuit is shown in Fig 4.14. The tail current source is not shown as it does not contribute to noise at the output. All the nodes whose gate values are at DC are grounded in the incremental equivalent circuit.

Let the equivalent resistance of the gain-boosted cascode be denoted as R_{out}.

$$
\begin{aligned}
R_{out} &= (R_{n,cascode} || R_{p,cascode}) \\
&= (\ A_n g_{m2} r_{o2} r_{o1}\ ||\ A_p g_{m3} r_{o3} r_{o4}\ ) \\
v_{n,out} &= g_{m1} R_{out} v_{n1}\ +\ g_{m4} R_{out} v_{n4} \\
S_{vn,out} &= g_{m1}^2 R_{out}^2 S_{v,n1}\ +\ g_{m4}^2 R_{out}^2 S_{v,n4}
\end{aligned}
$$

The major noise contributors are transistors M_1 and M_4. The equivalent input referred noise integrated over 10 KHz to 1 GHz is 90.1 μV ($\approx$ 0.1 LSB).

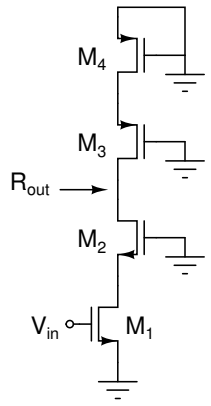


Figure 4.14: Equivalent circuit for noise analysis

4.3.9 Summary of simulated results

Tab.4.6 shows the simulated open loop response of the gain-boosted opamp.

$$A_{ol} = g_{m1}(R_{n,cascode}||R_{p,cascode})$$

$$= g_{m1}(A_n g_{m2} r_{o2} r_{o1}||A_p g_{m3} r_{o3} r_{o4})$$

Feature	Achieved response
DC gain	118 dB
Phase Margin (PM)	80^o
UGB with C_L = 1.2 pF	700 MHz

Table 4.6: Achieved open loop response

4.3.10 Design of bootstrapped sampling switches

In the first MDAC stage, bootstrapped switches are used to achieve lower distortion. Bootstrapping the sampling switch ensures a constant gate-source voltage across the switch. Bootstrapping techniques reported in [Nagaraj *et al.* (2000)] are used to realize a sampling switch with 3 dB bandwidth of 330 MHz with a 1 pF capacitive load.

Fig 4.15 shows the implementation of the sampling switch along with the circuit for the bootstrapped clock generator. The Nakagome charge pump [Nakagome *et al.* (1991)] used for generating a clock which switches from 3.0 V to 5.2 V is shown in dotted lines in Fig 4.15. The third order harmonic distortion is 80 dB for 2 V_{pp}, 19.375 MHz sinusoidal input. Fig 4.16 shows the output spectrum of the switch.

During layout, attention should be paid to minimize the value of parasitic capaci-

tance between the input and output terminals of the sampling switch. Signal feedthrough from the input pin to the output pin during the hold phase degrades the distortion performance of the sampling switch. For a fully differential implementation of the MDAC stage, 4 bootstrapped switches are required. Only one clock level shifter circuit was used for driving the boosted clock to all the 4 sampling switches.

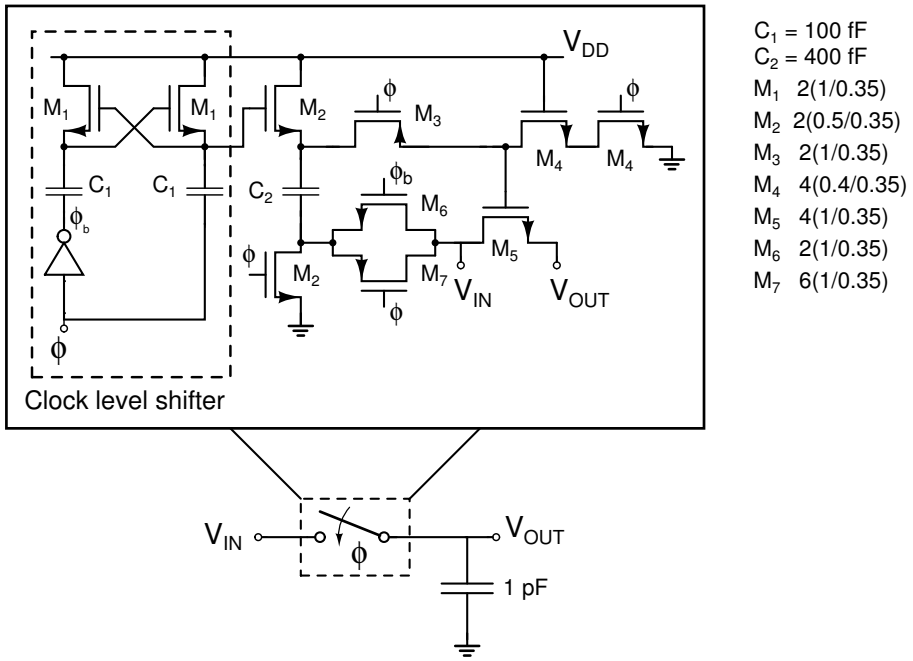


Figure 4.15: Schematic of bootstrapped switch

4.3.11 Comparator design

The A/D converter in each MDAC stage requires 2 comparators, with comparator thresholds at $\frac{V_{\text{REF}}}{4}$ and $\frac{-V_{\text{REF}}}{4}$. The need to generate two different references $\frac{V_{\text{REF}}}{4}$ and $\frac{-V_{\text{REF}}}{4}$ can be avoided by using the comparator topology in [Cho and Gray (1995)]. Fig 4.18 shows the circuit implementation of the comparator used in MDAC stage. The bottom NMOS device pairs (M_{1a}, M_{2a}) and (M_{1b}, M_{2b}) operate in triode region and act as resistances R_1, R_2. The values of R_1, R_2 depend on the input voltages V_{IP}, V_{IM}. The values of R_1, R_2 are given by the equations shown below. The input common mode

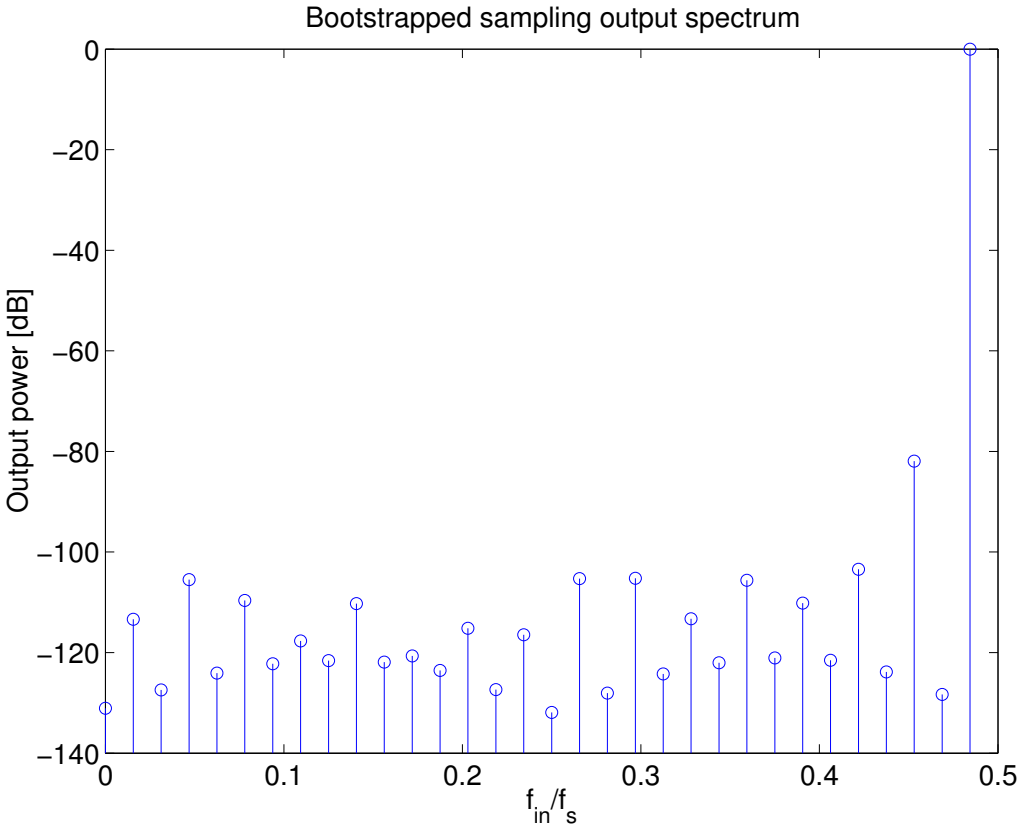


Figure 4.16: Output spectrum of the bootstrapped switch

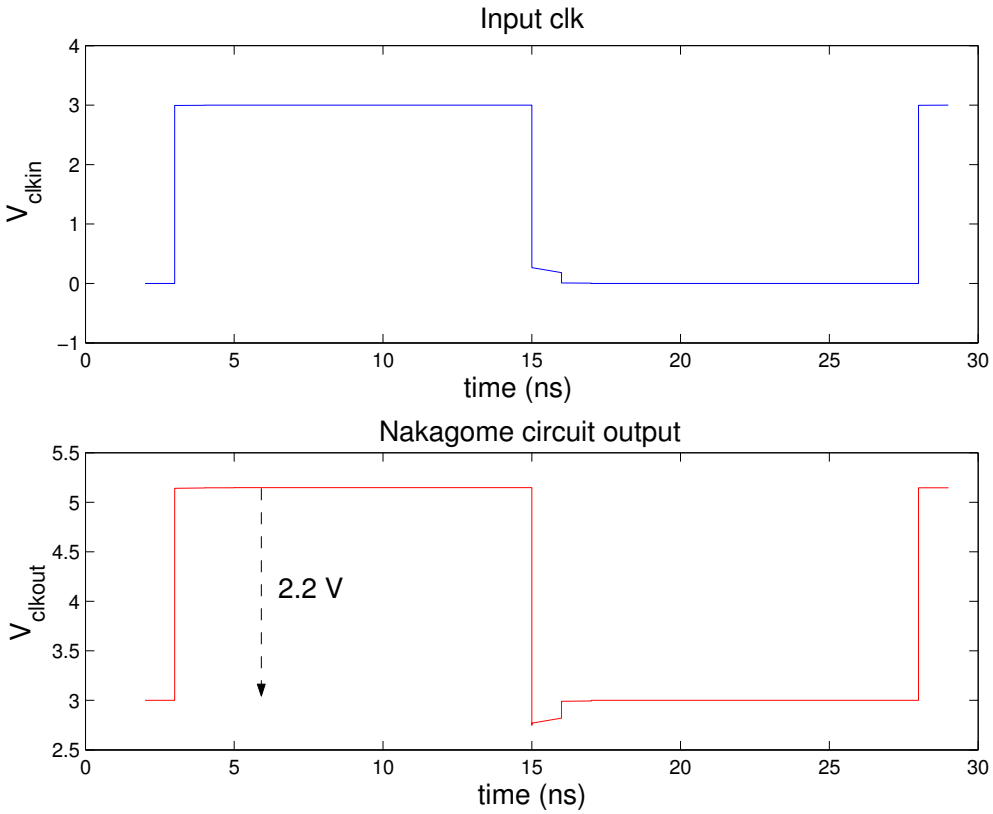


Figure 4.17: Nakagome charge pump output

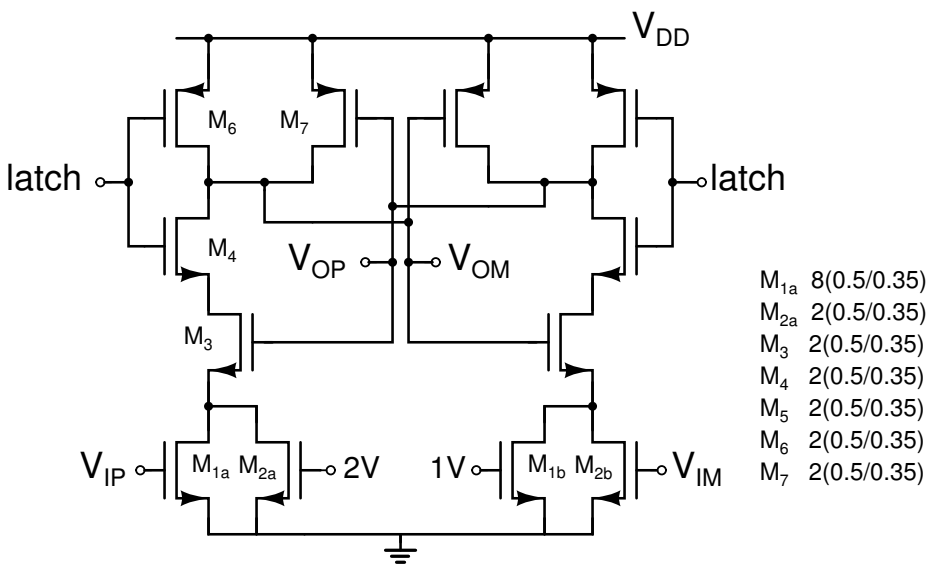


Figure 4.18: MDAC stage comparator

voltage V_{cmo} is 1.5V and V_{REF} is 1V.

$$\frac{1}{R_1} = K_n\Big[\frac{W_{1a}}{L}(V_{\text{IP}} - V_T) + \frac{W_{2a}}{L}(V_{cmo} + \frac{V_{\text{REF}}}{2} - V_T)\Big]$$
$$\frac{1}{R_2} = K_n\Big[\frac{W_{1b}}{L}(V_{\text{IM}} - V_T) + \frac{W_{2b}}{L}(V_{cmo} - \frac{V_{\text{REF}}}{2} - V_T)\Big]$$

The regeneration of the comparator is shown in Fig 4.19. To regenerate from V_{dd} to the correct decisions, the comparator takes around 1.2 ns.

The decisions from the first MDAC stage comparators are needed by the rising edge of ϕ_h. The rising edge of latch signal shown in Fig 4.18 should occur at t-Δt so as to accommodate the delay of the comparator. The earliest instant at which the edge of latch signal occurs can be computed from the input-output characteristic of the MDAC stage. In duration Δt, the input can at most change in within one segment of the characteristic.

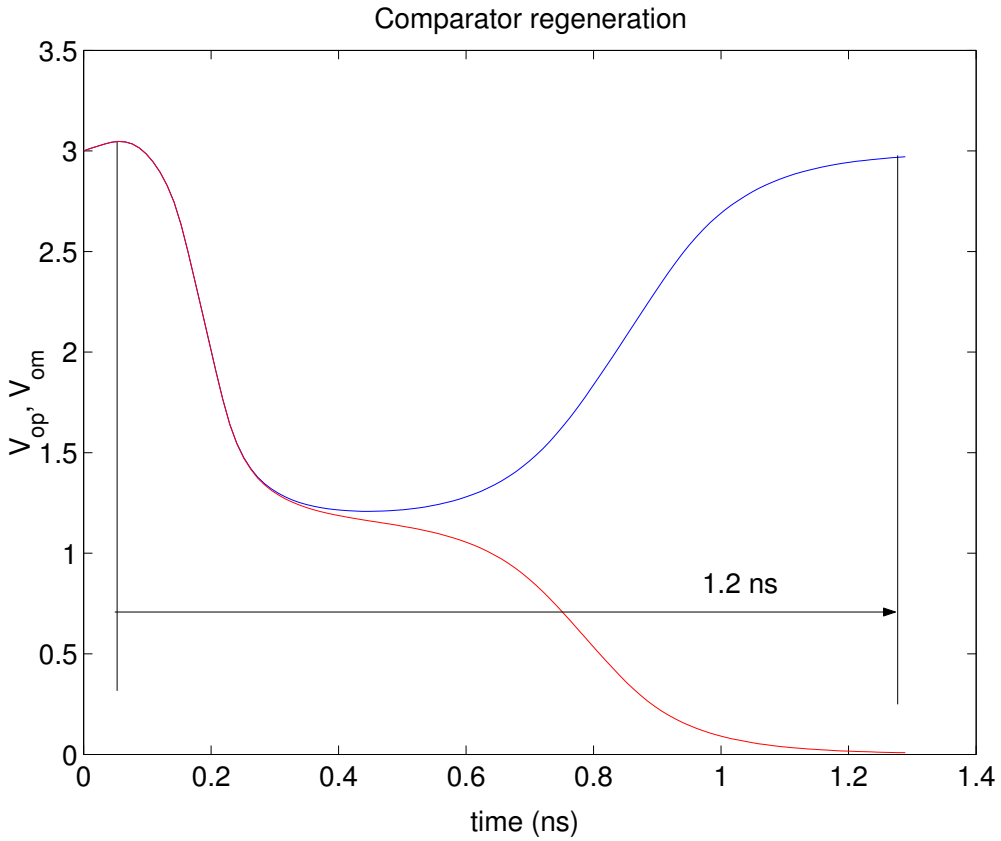


Figure 4.19: MDAC stage comparator regeneration

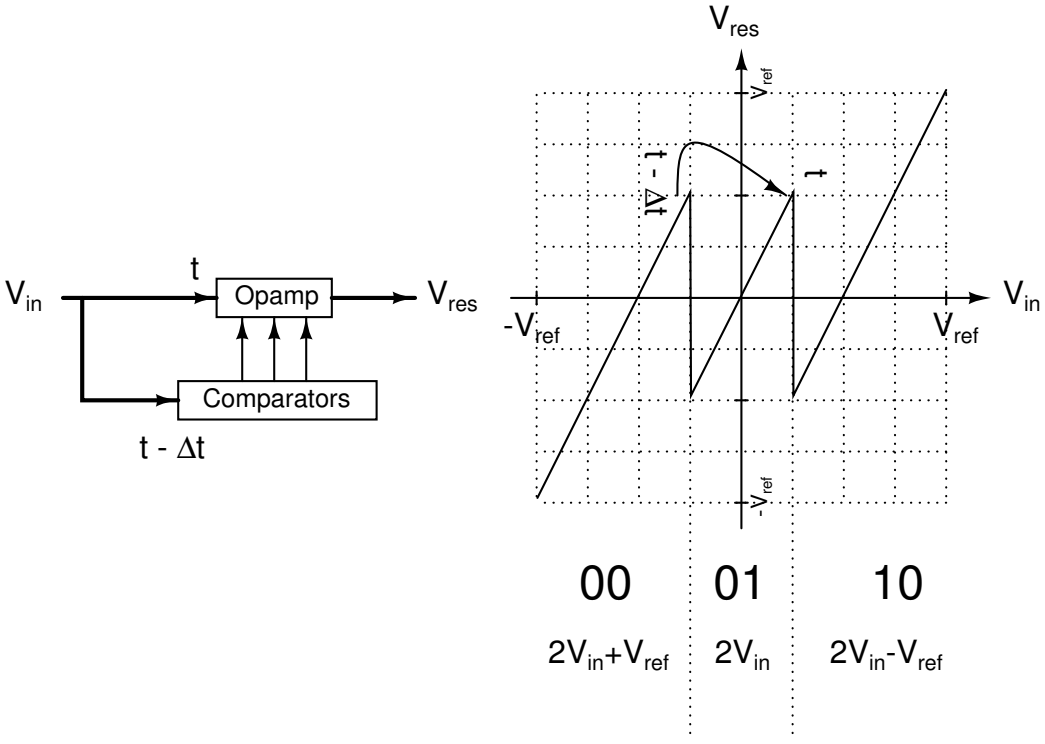


Figure 4.20: Latch signal timing

$$\text{For } V_{in} = A.sin(\omega t),\ (\frac{\Delta V_{in}}{\Delta t})_{max} = A\omega \Rightarrow \Delta t_{max} = 3.97\text{ns}$$

4.4 Design of a 3-bit Flash ADC

The important building blocks of the 3-bit flash ADC are the resistor ladder and the comparators. The resistor ladder is a string of eight 2 KΩ resistors that generates the differential voltage references for the comparators. Two resistor ladders are used to generate the differential references as shown in Fig 4.21. Large (area wise) resistors minimize the power consumption and improve matching between resistors, but degrade the transient response of the ladder. Bypass capacitors of 1 pF are provided at each node of the resistor ladder. In Fig 4.21 the value of V_{REFP} is 2 V and V_{REFM} is 1 V. These differential references (with a common mode of 1.5 V) are generated externally.

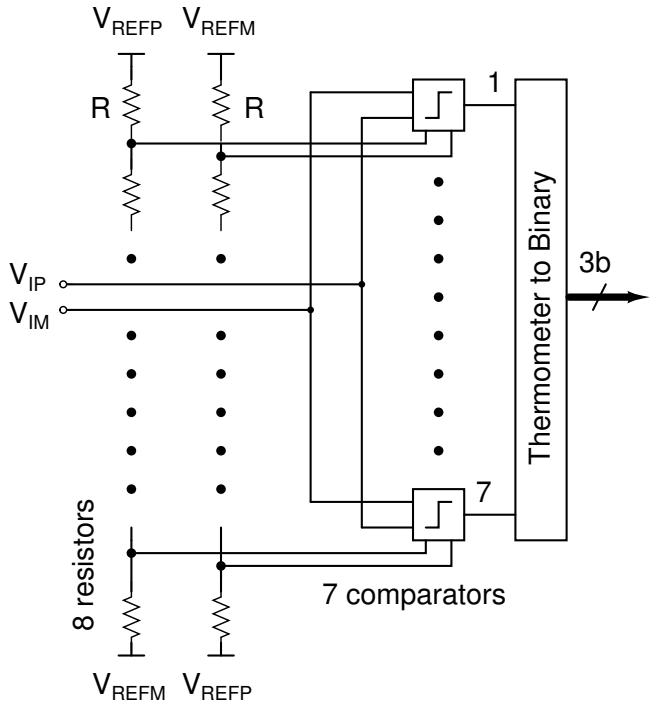


Figure 4.21: 3-bit Flash architecture

4.4.1 Flash comparator design

Fig 4.22 shows the implementation of the comparator and the clocking scheme used in the flash ADC. All the switches shown are transmission gates. The value of C is 50 fF.

The comparator has a three phased operation: the track phase, the regeneration phase and reset phase. In the track phase, LC is high and the parasitic capacitances at the input nodes of the latch are charged to v_{ip}-V_{REFP} and v_{im}-V_{REFM} respectively, where V_{REFP}, V_{REFM} are the differential reference voltages (with a common mode component V_{cmo}) corresponding to a particular comparator.

In the regeneration phase, LATCH is high and two operations are performed. The latch and capacitor portions are disconnected by the transmission gate operating on LC. The capacitors are charged to the corresponding references V_{REFP}-V_{cmo} and V_{REFM}-V_{cmo}, and the latch goes into regeneration mode. The value to which the latch outputs D_{OP}, D_{OM} regenerate to depend on the value of the voltage established on the parasitic capacitances at the input nodes.

In the reset phase, the output D_{OP}, D_{OM} are shorted through LRST switch. In this phase, LATCH is low, and there will be no current drawn from the supply by the back to back connected inverter pair to return to its common mode voltage at D_{OP}, D_{OM}. The average dynamic power dissipation of each comparator is around 70 μW/comparison cycle.

The input referred offset of the latch is computed using common mode conditions

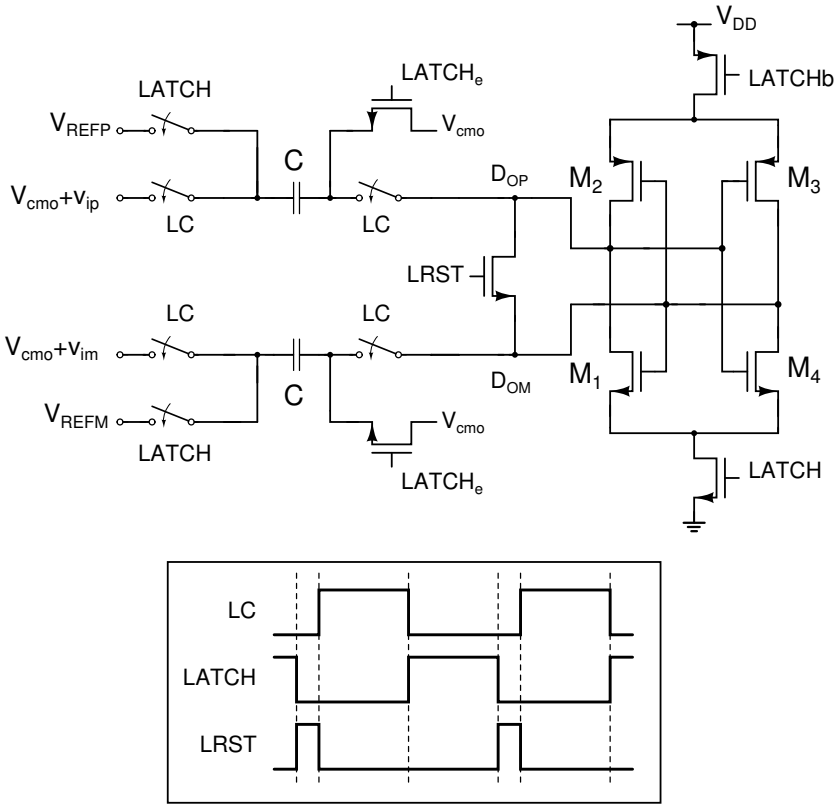


Figure 4.22: Flash comparator

on the latch input as shown in Fig 4.23. The offset is given by

$$\sigma_{offset} = \sqrt{(\frac{g_{m,n}}{g_{m,n}+g_{m,p}}\Delta V_{tn})^2 + (\frac{g_{m,p}}{g_{m,n}+g_{m,p}}\Delta V_{tp})^2}$$

For the device dimensions used, $g_{m,n} = 122.9\ \mu S$, $g_{m,p} = 65.1\ \mu S$ and $\Delta V_{tn} = 13.9\ \mathrm{mV}$, $\Delta \mathrm{V_{tp}} = 25.2\ \mathrm{mV}$. Using the above parameters, the offset is computed to be $\sigma_{offset} = 12.31\ \mathrm{mV}$.

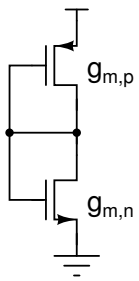


Figure 4.23: Equivalent circuit for latch offset calculation

4.4.2 Thermometer to binary converter

Thermometer to binary code conversion is achieved using addition of all the 7 output bits of the 7 comparators. This technique does not rely on detecting the 0→1 transition in the thermometer code. As opposed to the 0→1 transition detection technique, the addition technique will always result in an error of 1 LSB irrespective of the position of where the single bubble occurs. The error in LSBs will be equal to the number of bubbles in the thermometer code. Standard cell library full adders have been used to implement this conversion. Fig 4.24 shows the realization of the thermometer to binary converter using full adders (FA).

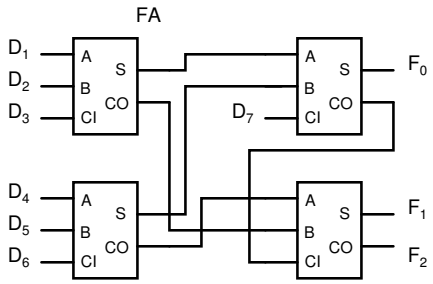


Figure 4.24: Thermometer to binary converter for 3-bit Flash ADC

4.5 Digital error correction (DEC)

DEC technique reported in [Lewis *et al.* (1992)] has been used. DEC is performed on 16 MDAC A/D output bits from 4 MDAC stages and 3 flash ADC outputs. Overlapped addition is performed using the circuitry shown in Fig 4.27. The 11-bit output (10-bit accuracy) of the DEC circuitry is latched using a 11-bit register. The 11-bit registers clock is feeds an external pin D_{clkout} which will serve as a synchronization signal for data capture by the logic analyzer.

Signal flow from each of the 4 MDAC stages (effective 8 MDAC stages after opamp

sharing) is shown in Fig 4.25. When MDAC stage goes in hold mode, the output voltage is sampled onto another set of capacitors and the same opamp is reused for the hold mode of MDAC stage 2. The conversion time for the ADC is 125 nS (5 clock cycles). Appropriate synchronization is require before overlapped addition. The flip flop requirements is explored further in this section.

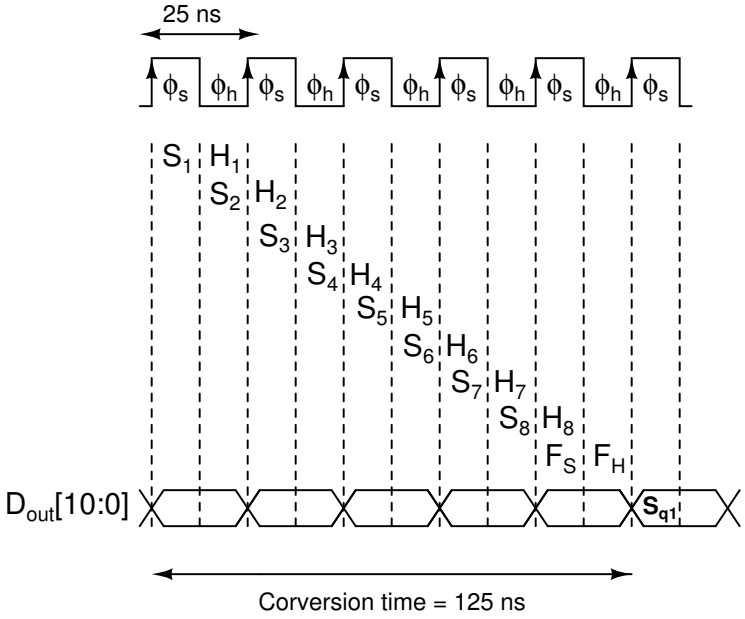


Figure 4.25: Signal flow in the DEC block

The overlapped-addition algorithm is shown in Fig 4.26. This implementation will require 8 full adders and 1 XOR gate. The 4 output bits of the MDAC stage 1,2,3,4 and 3-bit flash ADC need to be delayed by 5,4,3,2,1 cycles appropriately. This will need 20 + 16 + 12 + 8 + 3 = 59 flip flops totally.

The implementation of the DEC algorithm is shown in Fig 4.27. The flip flop array consists of 59 flip flops which delay each of the 4-bits of each MDAC stage appropriately before addition.

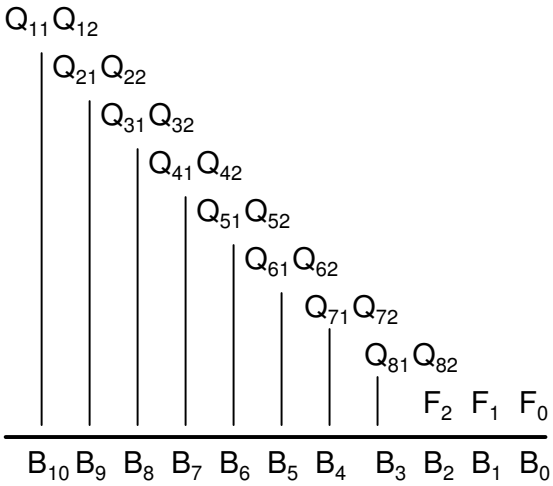


Figure 4.26: DEC addition algorithm

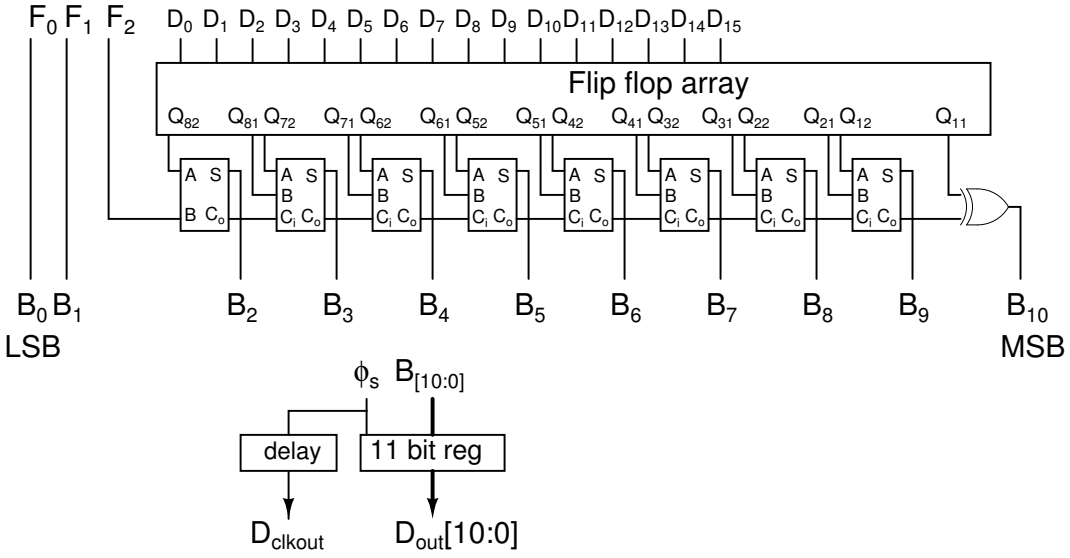


Figure 4.27: DEC addition

4.6 Clock generator design

Clock input to the ADC will be a sine wave at 40 MHz. It should be recalled that each of the subband ADCs operate at 40 MHz effectively realizing a 80 MHz sampling ADC. The circuit for converting the sine wave to square wave is shown in Fig 4.28. The clock is ac coupled to the IC pin. The transmission gate across inverter I1 acts a large resistance. The inverter biased at its common needs a small voltage change at its input to steer the output to 0 or V_{DD}. The 20 pF capacitor serves to attenuate any disturbance coupled onto the sine wave input.

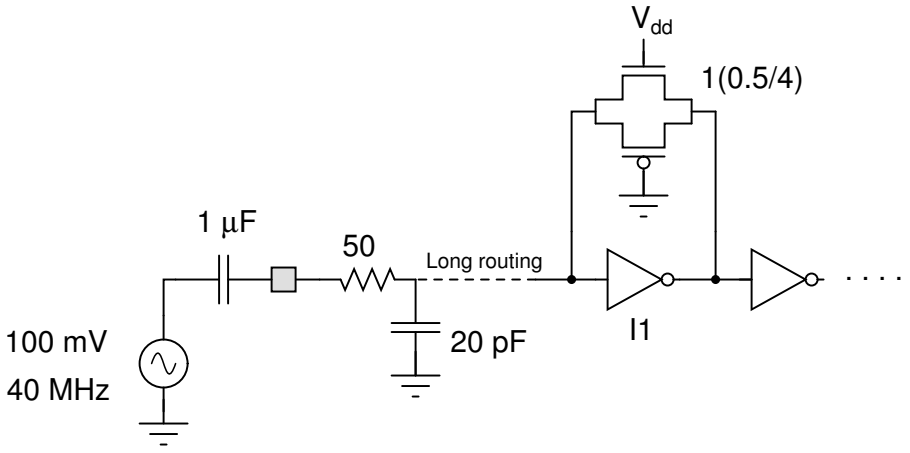


Figure 4.28: Converting sine wave clock to square wave

Non overlapping clocks are generated by first generating overlapping clocks using the NAND clock generator and then inverting the outputs CK_a and CK_b. The schematic and the timing diagram of the non overlapping clock generator is shown in Fig 4.29. The non overlap period can be adjusted by adjusting t_{d1} and t_{d2}. Buffer chain can be used after the NAND gates to realize the delay elements.

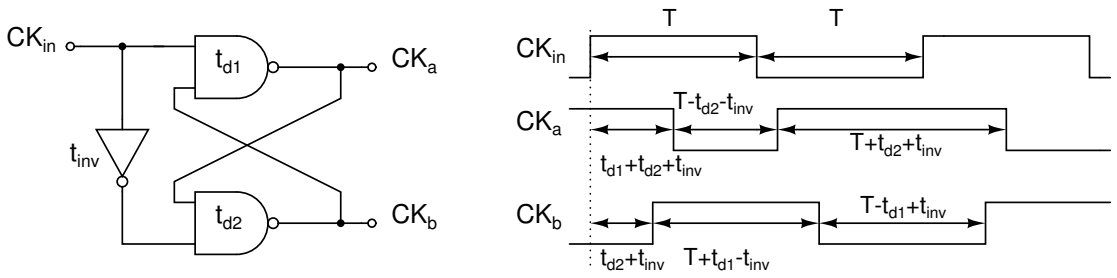


Figure 4.29: Non-overlapping clock generator

4.7 Voltage references

External voltage references are used for this ADC. Differential references are generated on-board using an AD8138 differential amplifier and REF3125 bandgap reference voltage. Since bond wire inductance leads to disturbances in the ADC internally, the model shown in Fig 4.30 is used for simulations. To dampen the oscillation due the LC tank formed by bond wire inductance and the on-chip bypass capacitance, a damping resistor of 10 Ω is used in conjunction with the bypass capacitance located close to the input pads. A total of 250 pF bypass capacitance is used on each of the differential reference input lines.

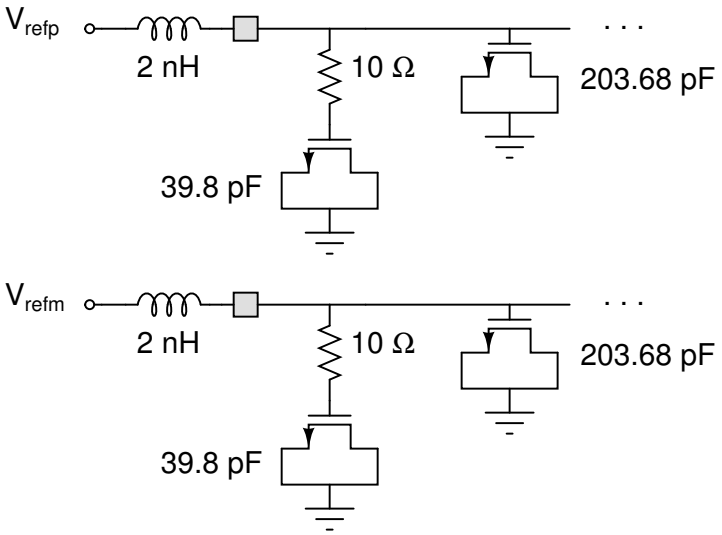


Figure 4.30: Bypass capacitor on external voltage references

4.7.1 MDAC stage Layout

Fig 4.31 shows the layout of the single MDAC stage. While doing the layout, care should be taken to avoid any clocks or supply signals crossing the virtual ground nodes of the gain boosted opamp. The layout shows the individual blocks in the ADC - the telescopic opamp, the nMOS folded cascode and the pMOS folded cascode opamps. The loop includes the capacitor elements and the 4 comparators.

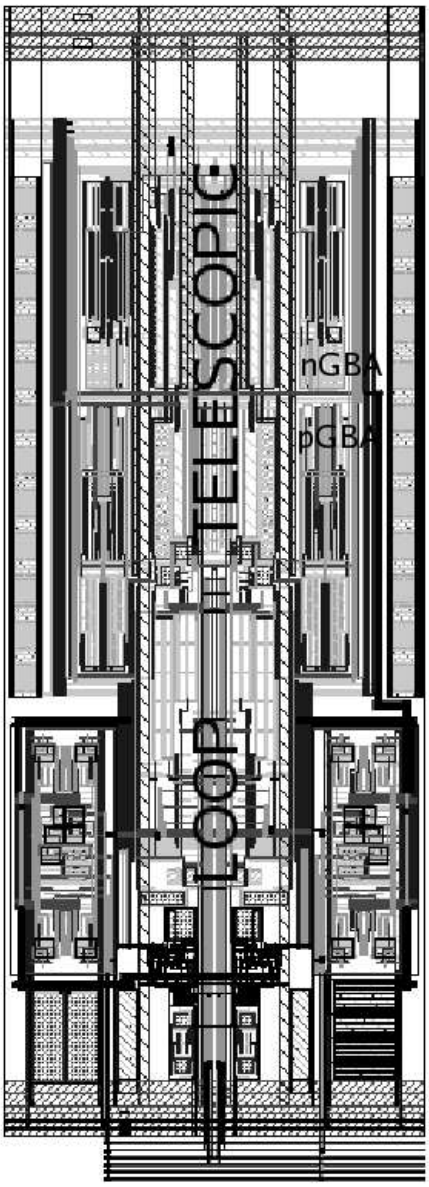


Figure 4.31: Layout of the MDAC stage

4.7.2 Pipelined ADC Layout

Fig 4.32 shows the complete layout of the pipelined ADC. The MDAC stage, 3-bit Flash ADC and the DEC blocks are marked. The power supply rails of the MDAC stages and the DEC block are separated to avoid power supply noise corrupting the individual MDAC stage outputs. To avoid IR drop across the the supply lines, the power rails are made wide (20 μm) enough, and routed in two metal layers (METAL 1 and METAL 3) to further decrease the resistance.

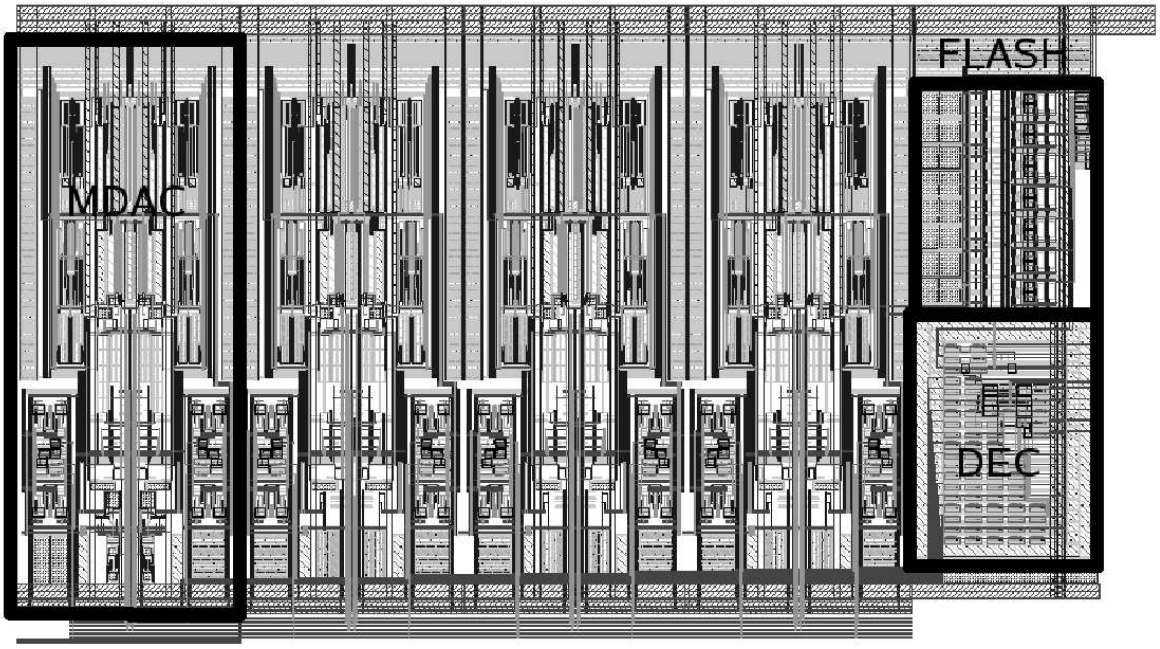


Figure 4.32: Layout of the sub band ADC

4.8 Simulation results for the entire 10-bit ADC

Fig 4.33 shows the output spectrum of the ADC to a 10 MHz full scale sine wave input (2048 points). The SNDR to such an input was found to 60.7 dB. For Nyquist rate performance, the designed ADC was simulated with a full scale input (2 V_{pp}) at 20 MHz. The SNDR variation across corners is shown in Table 4.7. The degradation in

SNDR in worst speed corner is due to improper settling of the first MDAC stage output.

The final simulated response of the ADC are shown in Table 4.8.

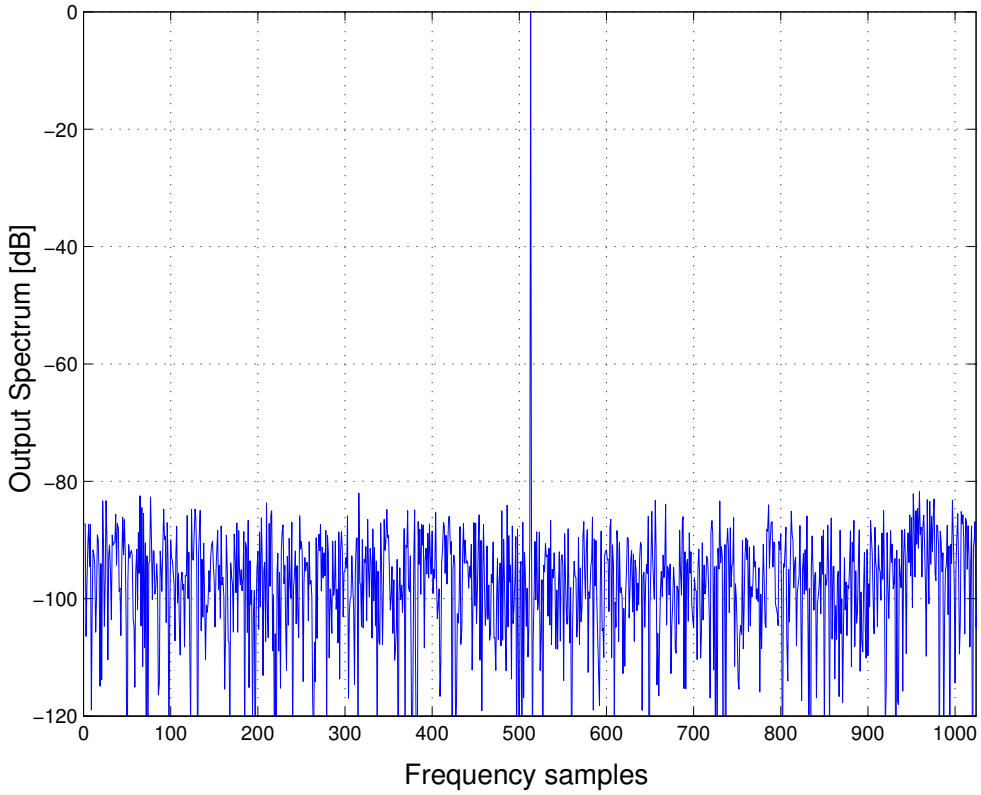


Figure 4.33: ADC output spectrum for a 10 MHz input

Corner	SNDR
cmostm	60.4
cmosws	57.3
cmoswp	59.4
cmoswo	61.3
cmoswz	59.8

Table 4.7: Corner simulations

Feature	Achieved results
Accuracy	10 bits
SNDR	60.4 dB (typical mean)
Sample rate	40 MSa/s
Signal bandwidth	40 MHz
Power dissipation	50 mW

Table 4.8: Pipeline ADC simulated results

CHAPTER 5

FILTER DESIGN

In this chapter we discuss details pertaining to the design of a biquad with f_c = 40 MHz and Q=0.5.

5.1 Biquad topology

A biquad is an active filter consisting of two-integrators in a feedback loop. As shown in Fig 5.1, it can be used as either a low-pass or band-pass filter, depending on where the output signal is taken from.

For the biquad in Fig 5.1, the low pass and band pass transfer function are given by

$$H(s) = \frac{G_{lpf}\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

$$H(s) = \frac{G_{bpf}\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

where, $G_{lpf} = \frac{R_4}{R_1}$, $G_{bpf} = \frac{R_2}{R_1}$ and $f_c = \frac{1}{2\pi\sqrt{R_3R_4C_1C_2}}$, $Q = R_2C_1\sqrt{\frac{1}{R_3R_4C_1C_2}}$

The important block in the biquad is opamp. The details relating to the design of the opamp are discussed in the next section. It can be seen that the gain of the biquad for the low pass and band pass sections is a ratio of resistors. Deviation of the R, C from the expected values will not alter the gain of the biquad but will alter the f_c and Q. Provision for fine tuning the center frequency should be provided. The can be achieved

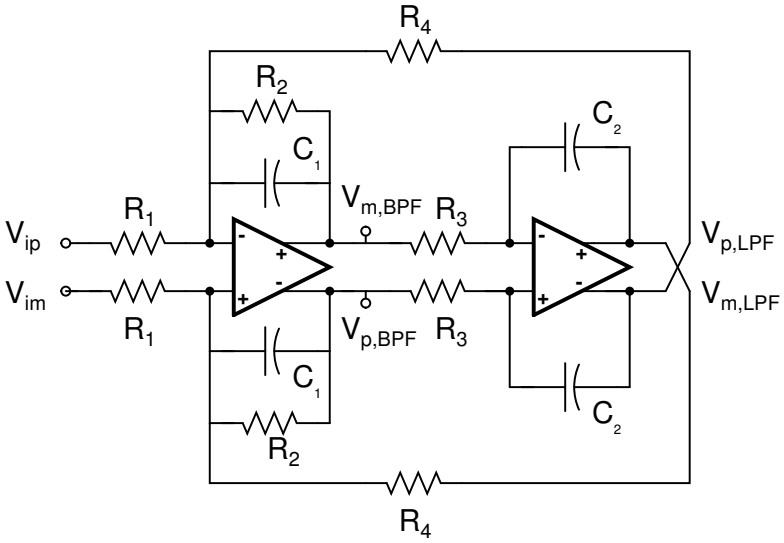


Figure 5.1: Biquad schematic

either by tuning the resistors or the capacitors. In this implementation, we choose to adjust the capacitors.

5.2 Arriving at the opamp specifications

The two important specifications of the biquad that need to computed are the open loop DC gain and the unity gain bandwidth (UGB). For a fixed UGB, decreasing the open loop DC gain of the opamp decreases the stop band attenuation. Variation of the stop band attenuation as the opamp gain changes from 50 to 1000 V/V can be seen in Fig 5.2. For a stop band attenuation of 60 dB, the minimum opamp gain required is around 200.

For a fixed opamp DC gain, varying the UGB of the opamp alters the pass band response i.e. the f_c and Q of the filter. Variation of the f_c as the opamp UGB changes from 40 to 400 MHz can be seen in Fig 5.3. Peaking in the pass band response can be seen which is a result of the low UGB. The UGB of the opamp is chosen to be approximately 10 times the center frequency f_c such that the filter characteristic matches

the ideal response. The minimum specifications that the opamp should meet are - an open loop DC gain of 200, and UGB of 400 MHz.

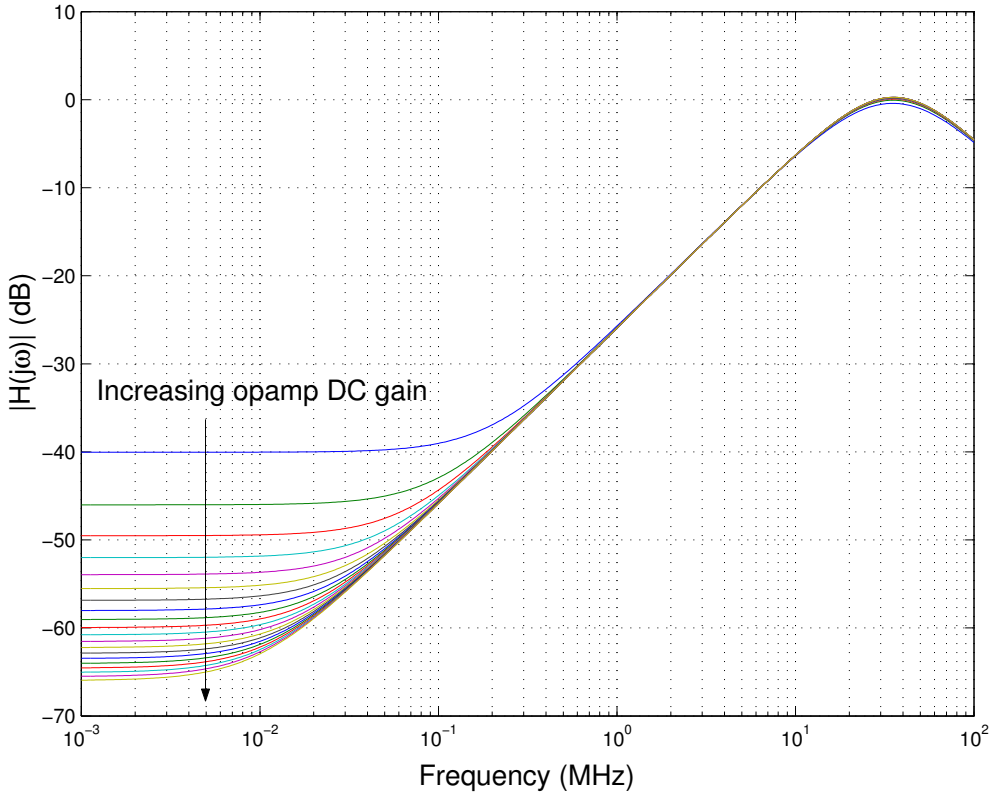


Figure 5.2: Variation of stop band response in a biquad with varying opamp DC gain

5.3 Opamp topology

A simple two stage opamp [Razavi (2002)] is used in this design. The opamp topology is shown in Fig 5.4. In the two stage opamp, both the output node of the first and second stages contribute poles. This opamp should be frequency compensated to move the interstage pole towards origin and the output pole away from the origin. This can be achieved by pole-zero compensation as shown in Fig 5.5.

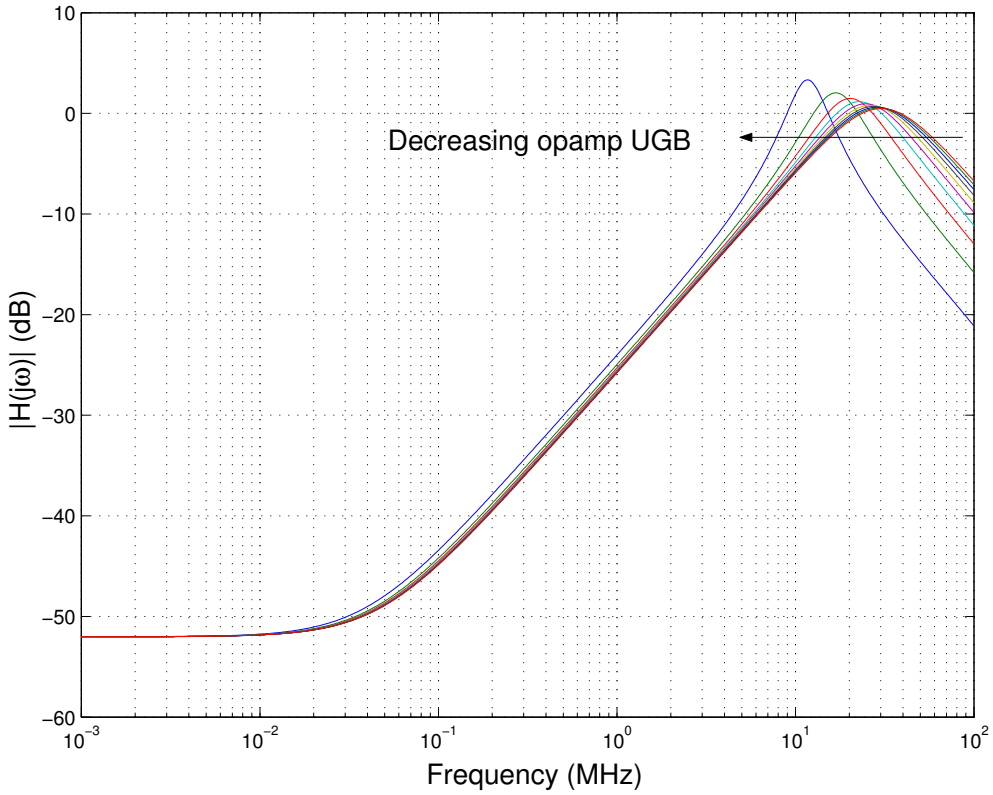


Figure 5.3: Variation of stop band response in a biquad with varying opamp UGB

The criteria for compensation is that

$$\frac{1}{C_c(\frac{1}{g_{m3}} - R_z)} = \frac{-g_{m3}}{C_L}$$

and to ensure that the zero introduced is in the left half plane always, the following constraint must be satisfied.

$$R_z \geq \frac{1}{g_{m3}}$$

By frequency compensating the opamp, we get the UGB to be independent of the load

capacitor C_L. The UGB of the opamp after compensation is

$$UGB = \frac{g_{m1}}{2\pi C_c}$$

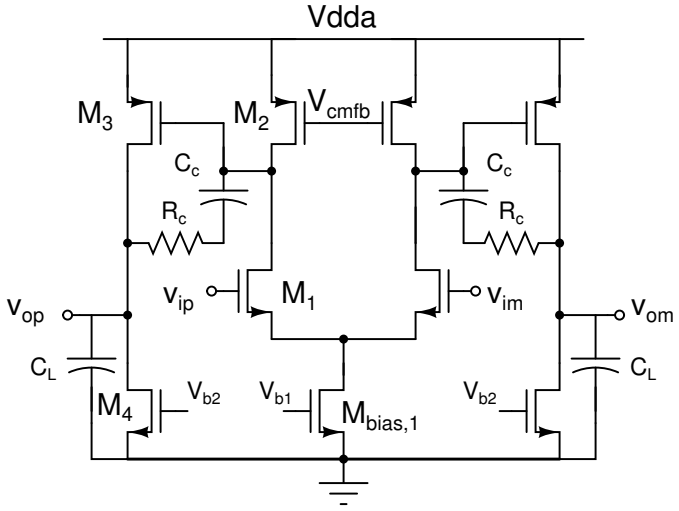


Figure 5.4: Opamp topology used in the biquad realization

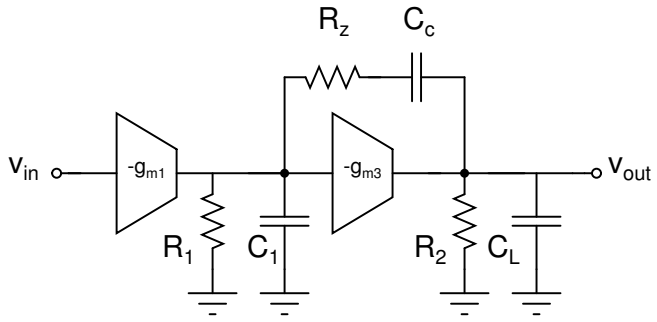


Figure 5.5: Small signal equivalent showing pole-zero compensation

The transistor sizes, bias currents and small signal parameters of the opamp shown in Fig 5.4 are shown in Table 5.1.

The specification of the designed opamp are shown in Table 5.2.

	$M_{bias,1}$	M_1	M_2	M_3	M_4
Size	$32(\frac{2}{2})$	$16(\frac{2}{0.35})$	$16(\frac{2}{0.35})$	$20(\frac{3}{0.35})$	$20(\frac{3}{0.50})$
I (mA)	0.2492	0.1246	0.1246	1.49	1.49
ΔV (mV)	290	152	323	836	324
g_m (mS)	1.15	1.325m	0.707	4.34	9.51
r_o (kΩ)	151.2	45.9	67.9	3.58	7.2

Table 5.1: Transistor sizes and operating point.

Feature	Achieved specification
DC gain	52.5 dB
UGB	700 MHz
Phase margin	50^o
Input referred noise	255 μV
Output swing	1.92 V
V_{cmi}	1.5 V
V_{cmo}	1.495 V
I_{total}	3.25 mA

Table 5.2: Achieved specifications

5.3.1 Common mode feedback loop

The common mode loop shown in Fig 5.6 is used to fix the output common mode of the opamp. The operating point, transistor sizes used in the common mode feedback loop are shown in Table 5.3. Since the opamp itself provides a large gain in the common mode loop path, the common mode opamp is chosen to have a low gain (≈ 1) configuration.

	$M_{bias,1}$	M_1	M_2
Size	$32(\frac{2}{2})$	$4(\frac{2}{0.35})$	$16(\frac{2}{0.35})$
I (mA)	0.262	0.131	0.131
ΔV (mV)	317	320	339
g_m (mS)	1.13	0.58	0.7
r_o (kΩ)	58.5	89	55.7

Table 5.3: Transistor sizes and operating point of the CMFB loop.

The common mode loop stability is tested by connecting both the input and output nodes of the opamp to input common mode and applying a 1μA test current into the

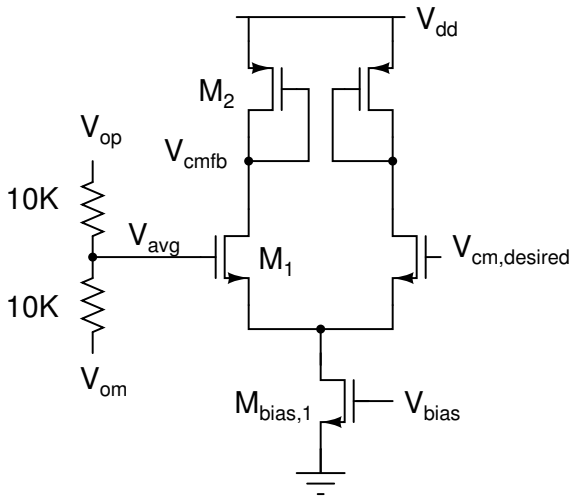


Figure 5.6: Common mode feedback loop

output nodes. The output common mode should settle to the desired value (1.5 V) in less that 25 ns. The common mode step response is shown in Fig 5.7.

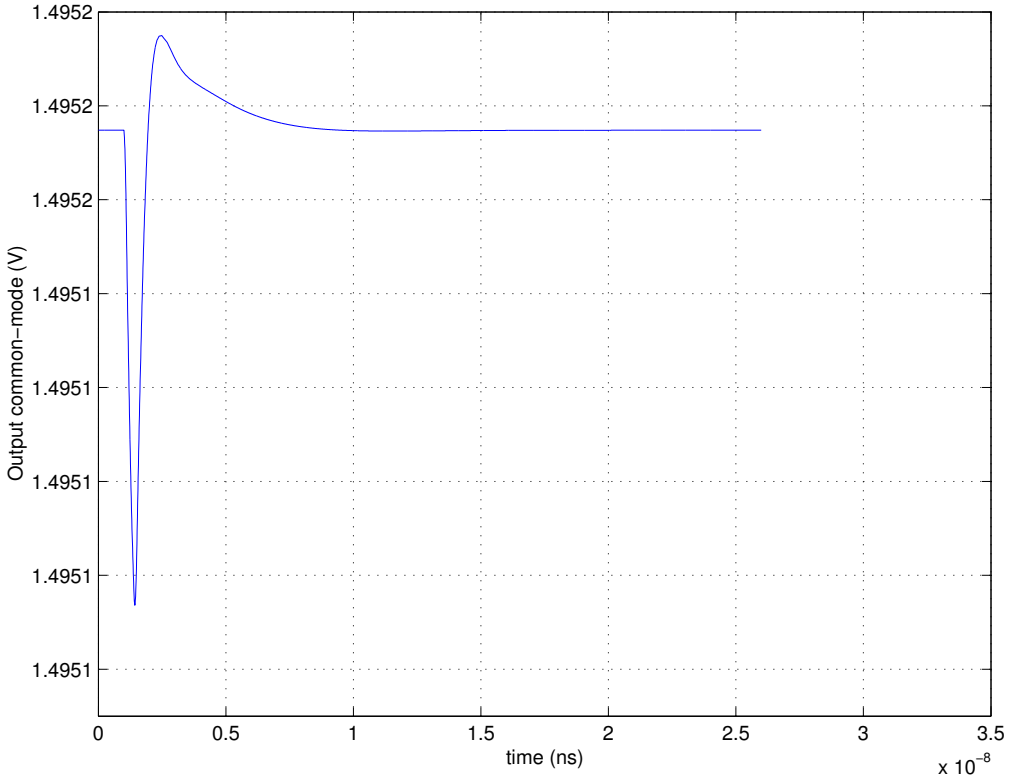


Figure 5.7: Common mode feedback loop stability

5.4 Biquad implementation

The implementation of the biquad is shown in Fig 5.8. Theoretically resistors R_1 and R_2 should be equal, but different values are chosen so as to accommodate for achieving gain at f_c to be 1 (0 dB) in the face of parasitic capacitance at each opamp input and output nodes. Provision for tuning the center frequency is achieved using a bank of capacitors parallel to C which can be turned ON/OFF.

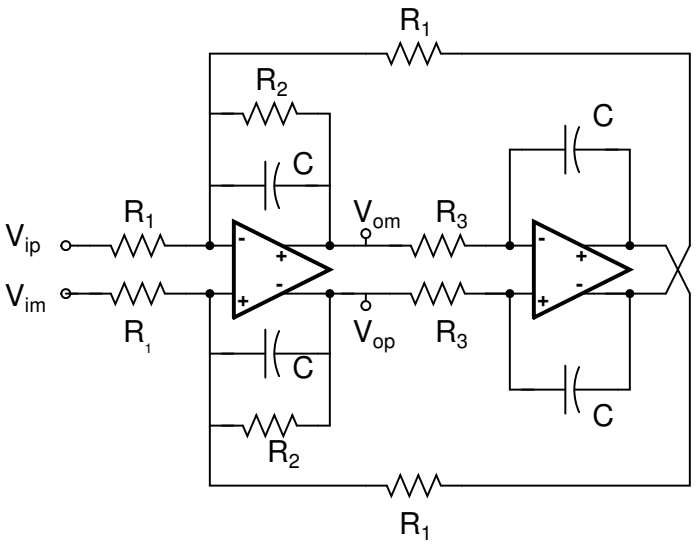


Figure 5.8: Biquad schematic

The values of [R_1,R_2,R_3,C] should be optimized accounting for all the parasitic capacitances introduced for both the opamps. The algorithm for tuning the values of [R_1,R_2,R_3,C] is elaborated in the next section.

5.5 Procedure for obtaining the integrating R,C values

In the face of parasitic capacitances, finite DC gain and UGB in the opamps used in the biquad, the band pass frequency response deviates from the ideal response. In order to obtain the values of [R_1,R_2,R_3,C], we first need to precisely model the opamp used

in the biquad. The procedure detailed below elaborates on how to obtain the values of [R_1,R_2,R_3,C]. The design centering approach is same as elaborated in [Laxminidhi and Pavan (2007)].

Step 1: First, the state space model of the opamp needs to be developed. The general representation of the state space model is

$$H\dot{\mathbf{v}}(t) = A\mathbf{v}(t) + B\mathbf{u}(t)$$

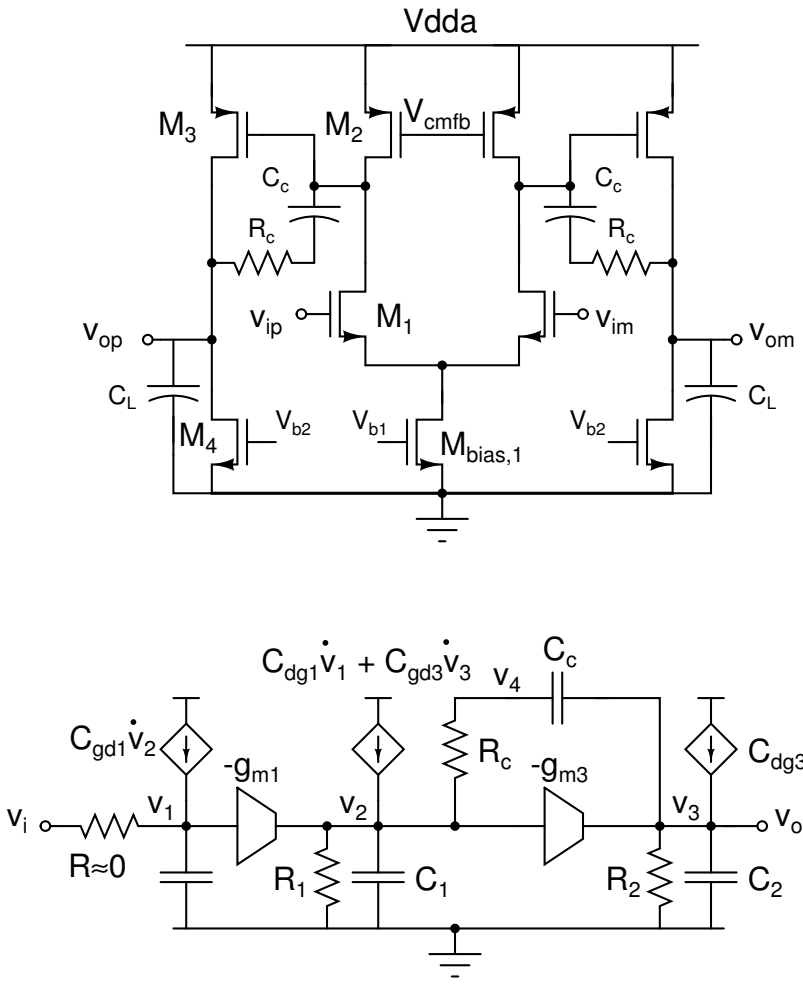
$$\mathbf{y}(t) = C\mathbf{v}(t) + D\mathbf{u}(t)$$

$\mathbf{x}$(t) is the state vector which usually comprises of voltages across capacitors and current flowing through inductors in the circuit. For the small signal model in Fig 5.9, the state space model is given by

$$[H_{opamp}] = \begin{bmatrix} C_{gg1} & -C_{gd1} & 0 & 0 \\ -C_{dg1} & C_1 & -C_{gd3} & 0 \\ 0 & -C_{dg3} & C_2 + C_c & -C_c \\ 0 & 0 & -C_c & C_c \end{bmatrix}, [A_{opamp}] = \begin{bmatrix} \frac{-1}{R} & 0 & 0 & 0 \\ -g_{m1} & -\frac{1}{R_1} - \frac{1}{R_c} & 0 & \frac{-1}{R_c} \\ 0 & -g_{m3} & \frac{-1}{R_2} & 0 \\ 0 & \frac{1}{R_c} & 0 & \frac{-1}{R_c} \end{bmatrix}$$

$$[B_{opamp}] = \begin{bmatrix} \frac{1}{R} \\ 0 \\ 0 \\ 0 \end{bmatrix}, [C_{opamp}] = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix}, [D_{opamp}] = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{ and } [v_{opamp}] = \begin{bmatrix} \mathbf{v_1} \\ \mathbf{v_2} \\ \mathbf{v_3} \\ \mathbf{v_4} \end{bmatrix}$$

Step 2: Next, using the state space model shown above, the opamp frequency response is obtained and verified that the small signal model in Matlab and AC simulation



$$R_1 = \frac{1}{g_{ds1} + g_{ds2}} \qquad R_2 = \frac{1}{g_{ds3} + g_{ds4} + (1/R_{cm})}$$

$$C_1 = C_{dd1} + C_{dd2} + C_{gg3} + C_{jd1} + C_{jd2}$$

$$C_2 = C_{dd3} + C_{dd4} + C_{load} + C_{jd3} + C_{jd4}$$

Figure 5.9: Opamp and its small signal equivalent circuit

in Cadence show the same frequency response.

Step 3: With the knowledge of the opamp state space model, the state space model of the biquad is developed i.e. H_{biquad}, A_{biquad}, B_{biquad}, C_{biquad}, D_{biquad} are obtained.

Step 4: Using the state space model of the biquad, the transfer function from the input to output can obtained. Using $\epsilon = \left|\mathrm{H}_{obtained}(j\omega) - \mathrm{H}_{ideal}(j\omega)\right|^2$ as an error criteria, **fminsearch** routine in Matlab is used to adjust the values of [R_1,R_2,R_3,C] to minimize error ϵ.

Fig 5.10 shows the response of the biquad after optimization using the algorithm detailed above. The values of the optimized [R_1,R_2,R_3,C] = [8.2 KΩ, 7.4 KΩ, 54.3 KΩ, 150 fF].

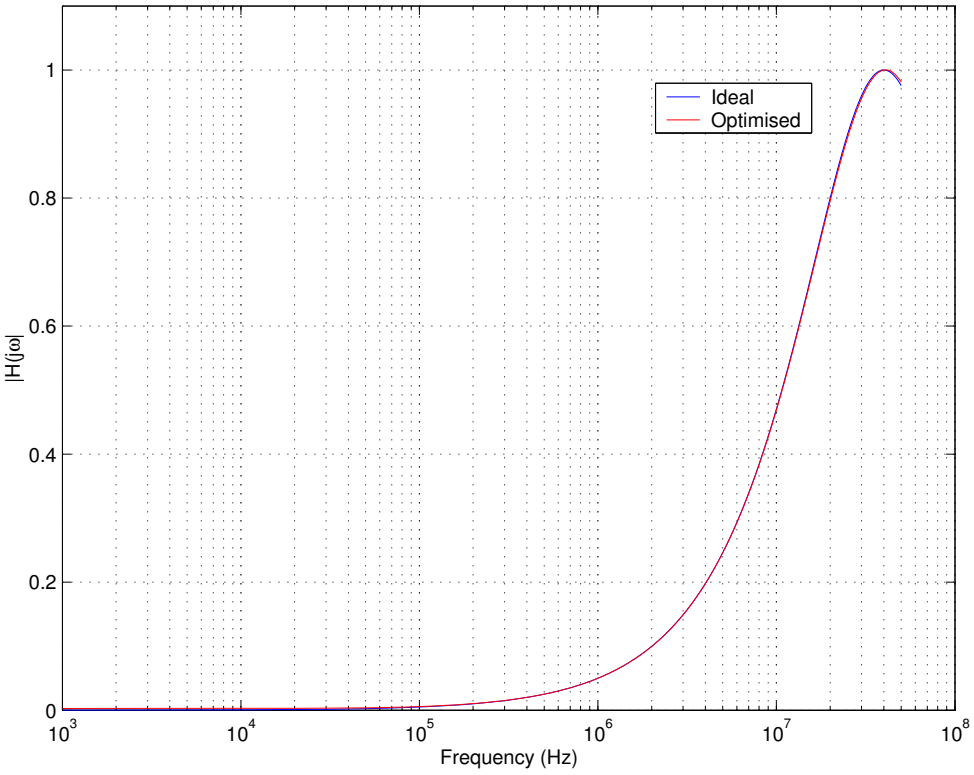


Figure 5.10: Ideal, Obtained responses after [R_1,R_2,R_3,C] optimization

5.6 Integrated noise at the filter output

The contribution of each of the resistive noise sources for the single ended biquad shown in Fig 5.11 is tabulated in Table 5.4. It can be seen from the table that the noise contributed by resistors R_1 and R_2 is band pass filtered but the noise contributed by R_3 i.e. noise source v_{n2} is low pass filtered. It is seen in noise simulation that the major noise contributor is resistor R_3. Integrated noise at the output over 1 kHz to 1 GHz is 520 μV.

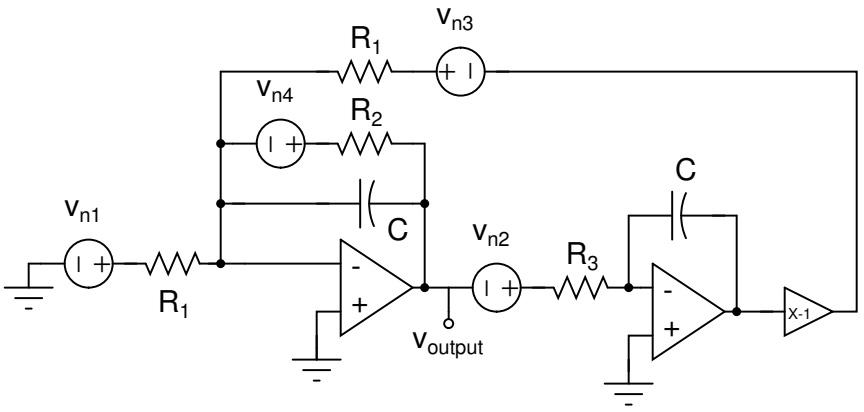


Figure 5.11: Noise contributors

5.7 Tuning the center frequency f_c of the biquad

Deviation of the R,C's from their intended values will result in a different value of f_c and Q. To be able to get back to the desired biquad response, capacitor tuning is employed. Using the capacitor bank shown in Fig 5.12, the center frequency of the filter f_c is tunable by $\pm 10\%$. The switching of the capacitors in the capacitor bank is based on thermometer code. The capacitance can be tuned from it nominal value of 125 fF till 181 fF in steps of 8 fF. The simulated tuning range of the biquad was from 33 MHz to 48 MHz. The simulated tunable frequency responses are shown in Fig 5.13.

Source	Transfer function	Nature
v_{n1}	$\left\lvert \frac{v_o}{v_{n1}} \right\rvert = \frac{\frac{s}{R_1 C}}{s^2 + \frac{s}{R_2 C} + \frac{1}{R_1 R_3 C^2}}$	Band pass
v_{n2}	$\left\lvert \frac{v_o}{v_{n2}} \right\rvert = \frac{\frac{1}{R_1 R_3 C^2}}{s^2 + \frac{s}{R_2 C} + \frac{1}{R_1 R_3 C^2}}$	Low pass
v_{n3}	$\left\lvert \frac{v_o}{v_{n3}} \right\rvert = \frac{\frac{s}{R_1 C}}{s^2 + \frac{s}{R_2 C} + \frac{1}{R_1 R_3 C^2}}$	Band pass
v_{n4}	$\left\lvert \frac{v_o}{v_{n4}} \right\rvert = \frac{\frac{s}{R_2 C}}{s^2 + \frac{s}{R_2 C} + \frac{1}{R_1 R_3 C^2}}$	Band pass

Table 5.4: Noise contribution

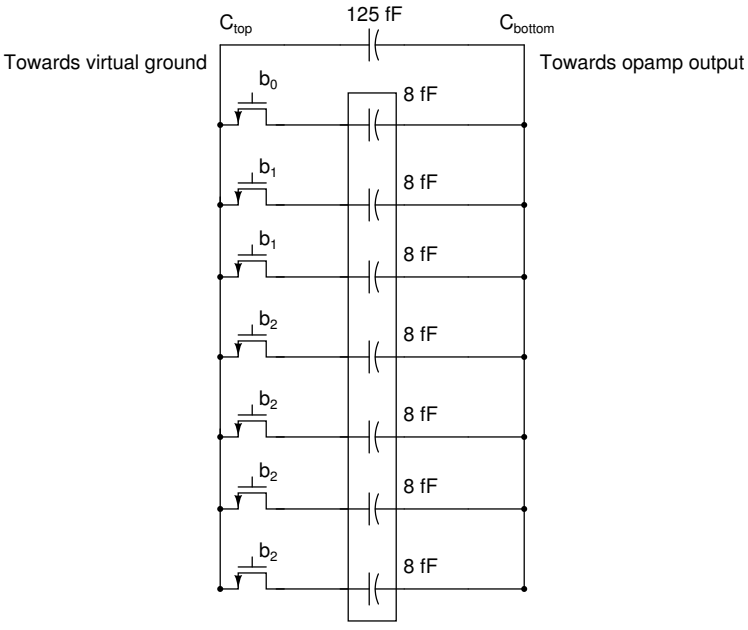


Figure 5.12: Capacitor tuning

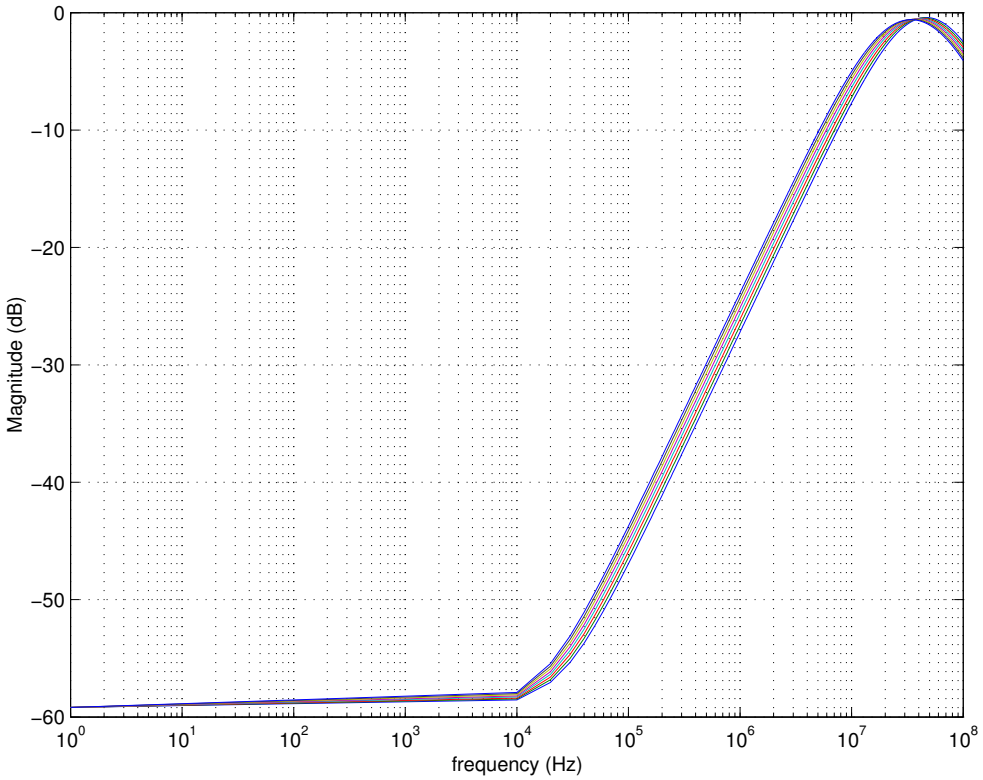


Figure 5.13: Tunable frequency response. Simulated f_c ranges from 33 to 48 MHz

5.8 Measurement of the frequency response

To measure the frequency response of the filter H_{fil} alone, test buffers capable of driving the pad capacitance + differential 50 Ω load are needed. The frequency response H_{fil} is de-embedded using two measurements - direct path measurement, and filter path measurement [Pavan and Laxminidhi (2007)]. In the first measurement, H_{tb}, the frequency response of the test buffere is measured and in the second measurement $H_{tb}H_{fil}$ is measured. Fig 5.14 shows the setup for measuring the frequency response H_{fil}. H_{fil} is obtained using

$$H_{fil} = \frac{H_{tb}H_{fil}}{H_{tb}}$$

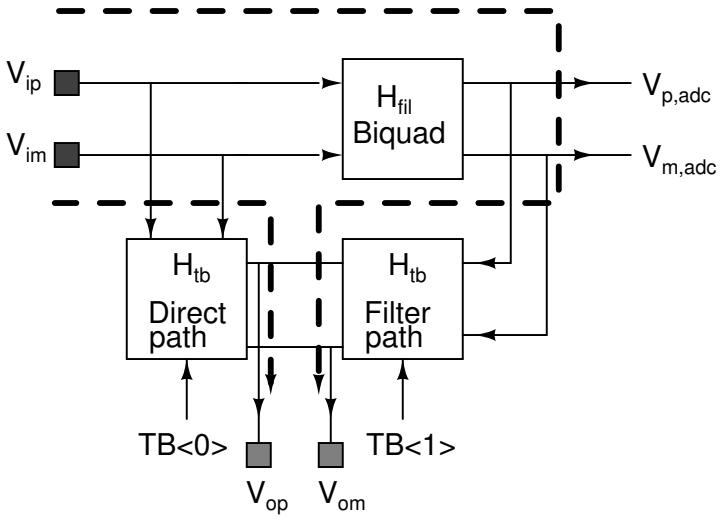


Figure 5.14: Setup for measuring frequency response of the biquad

5.8.1 Test buffer design

The test buffer described in the section above needs to designed to drive a differential 50 Ω load. Fig 5.15 shows the circuit implementation of the test buffer. The test buffer has a 3-dB bandwidth of 500 MHz, when loaded differentially with a 50 Ω load. Table 5.5 shows the transistor sizes and the operating points of the test buffer.

The output swing of the biquad at f_c is 2 V_{pp}. To be able to measure the distortion introduced by the biquad alone, the test buffer needs to linear for the entire output swing of the biquad. To avoid the test buffer from distorting the output of the biquad, only $\frac{1}{8}^{th}$ of the biquad voltage output is fed to the test buffer.

	M_1	M_3	M_5
Size	$16(\frac{10}{0.35})$	$12(\frac{3.1}{0.35})$	$12(\frac{9.3}{0.35})$
I (mA)	1.561	1.939	1.939
ΔV (mV)	376	439	261
g_m (mS)	7.177	5.324	10.8
r_o (kΩ)	3.88	54.7	43.1

Table 5.5: Transistor sizes and Operating point of the Test buffer

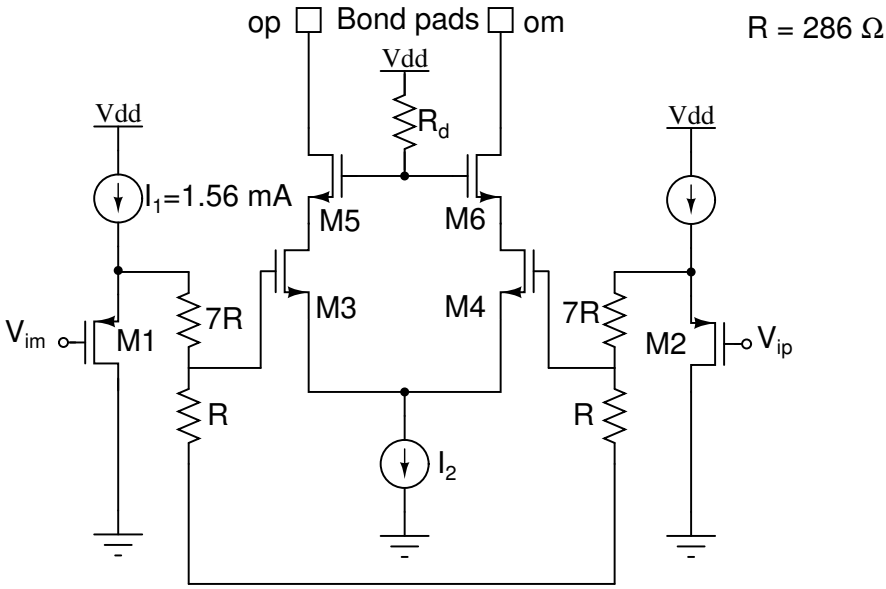


Figure 5.15: Test buffer schematic

5.8.2 Simulation results

The simulated performance of the biquad is summarized in Table 5.6. It is important that the distortion at the output of the biquad does not limit the noise floor of the preceding stage. When loaded with the first MDAC stage, the distortion at various corners was found to be sufficiently lower than the intended SNR. The distortion measurements for full scale input (2 V_{pp}) at two different input frequencies were carried out and the distortion was observed.

Observations regarding distortion are tabulated in Table 5.7.

Feature	Achieved specification
f_0	40.27 MHz
Output integrated noise (V)	520 μV
HD3 @ f = 13 MHz, 2V_{pp}	77.2 dB
HD3 @ f = 40 MHz, 2V_{pp}	69.8 dB
Power consumption	7 mA $\times$ 3 V

Table 5.6: Achieved specifications

Fig 5.16 shows the simulated response of the biquad. With the capacitance value

Corner	f_{in} = 13 MHz	f_{in} = 40 MHz
cmostm (typical mean)	77.2	69.8
cmosws (worst speed)	78.7	68.7
cmoswp (worst power)	74.2	67.2
cmoswo (worst one)	80.7	69.3
cmoswz (worst zero)	72.1	66.5

Table 5.7: HD_3 for 2 V_{pp} input signal

of the capacitor bank set to 149 fF, the simulated $f_c = 10^{7.605}$ = 40.27 MHz. It can be seen that the stop band attenuation is around 59 dB. The pass band response variation to the 7 possible capacitor setting is shown in Fig 5.17. It can be seen that with all the 8 fF capacitors turned OFF, the integrators are least "lossy" and the passband response droops and f_c shifts left by turning ON each of the 8 fF capacitor.

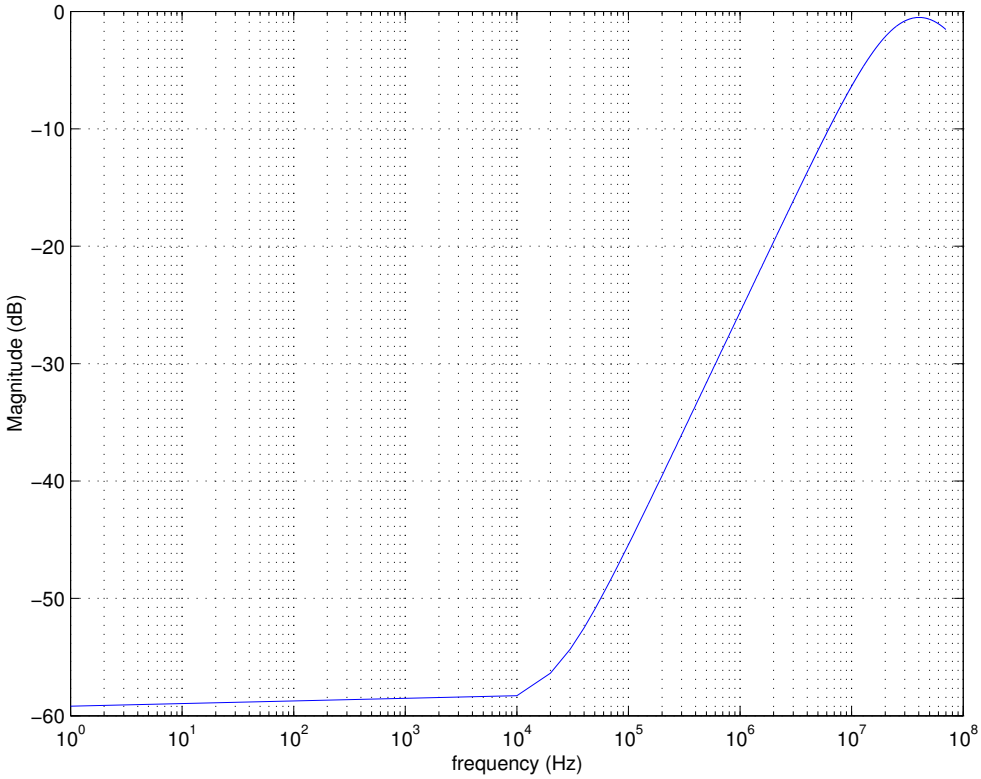


Figure 5.16: Frequency response. Simulated $f_c = 10^{7.605}$ = 40.27 MHz

Finally, the response of the biquad to temperature variation if shown in Fig 5.18. With temperature changed from 0 to 70^{o}C, the pass band gain changes by around 0.1

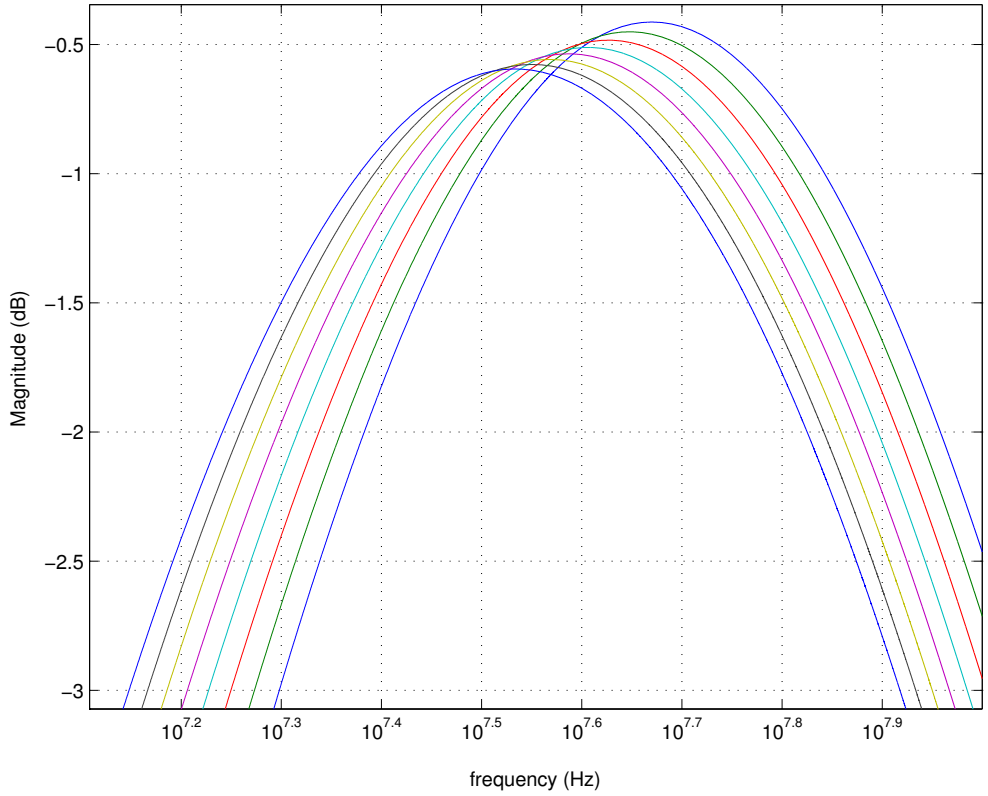


Figure 5.17: Passband details

dB.

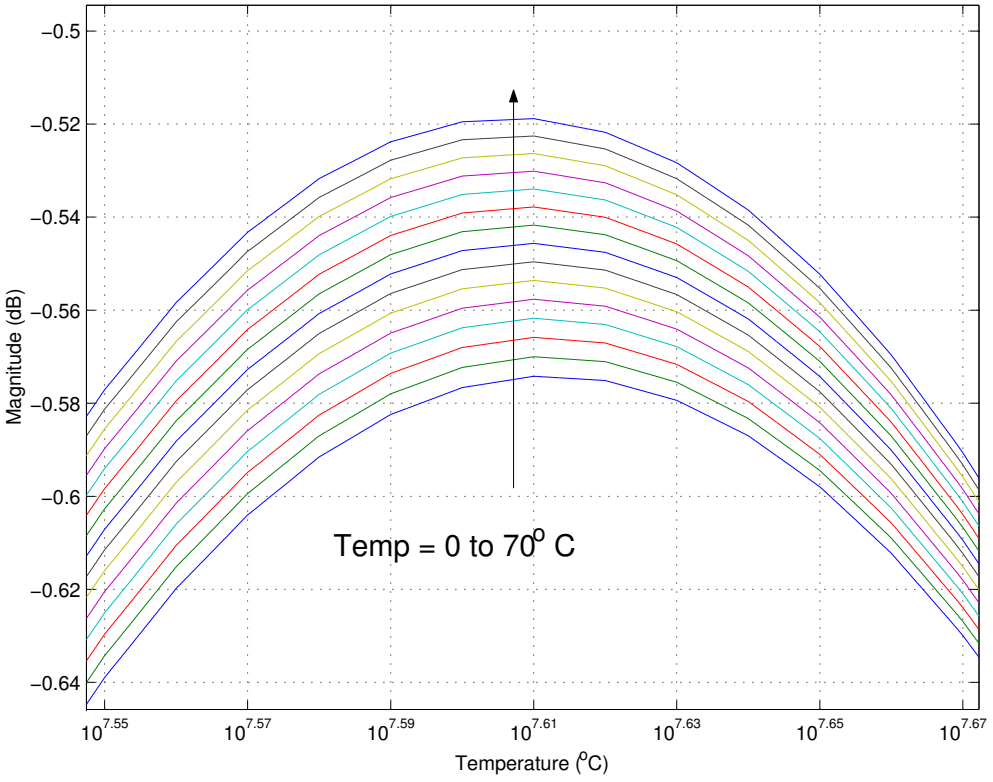


Figure 5.18: Frequency response variation across temperature

5.8.3 BPF Layout

Fig 5.19 shows the layout of the BPF. Two test buffers (direct path buffer and the filter path buffer) to facilitate the measurement of the frequency response are also shown. A separate V_{DD} is used for the BPF alone to provide a less noisier supply to the BPF compared to the BPF.

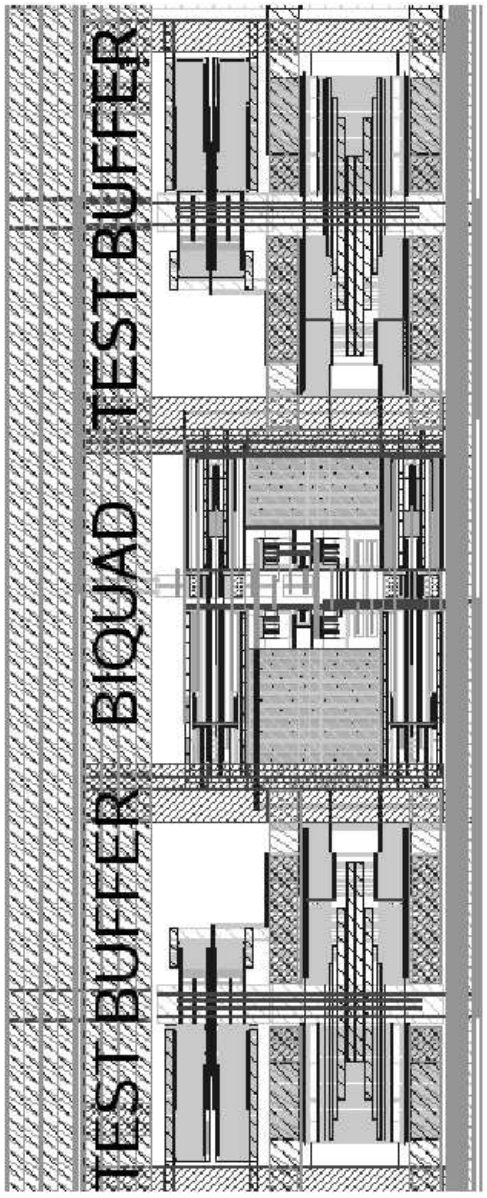


Figure 5.19: Layout of the BPF

5.9 System integration

Fig 5.20 shows the 2-channel HFB implementation. Both the ADC's share common clock generator and reference voltages. As shown in Fig 5.20 after integrating the filter and 2 ADC's together, it has been ensured in simulation that the SNDR across 2 channels is 60 dB. Fig 5.21 shows the layout of the 2-channel HFB ADC layout.

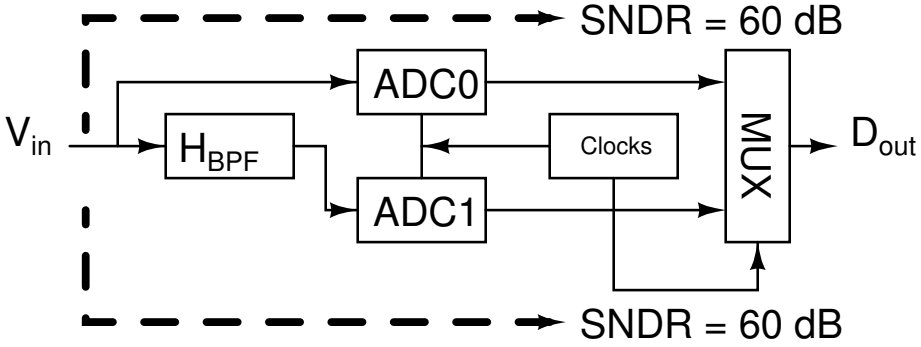


Figure 5.20: 2-channel HFB system

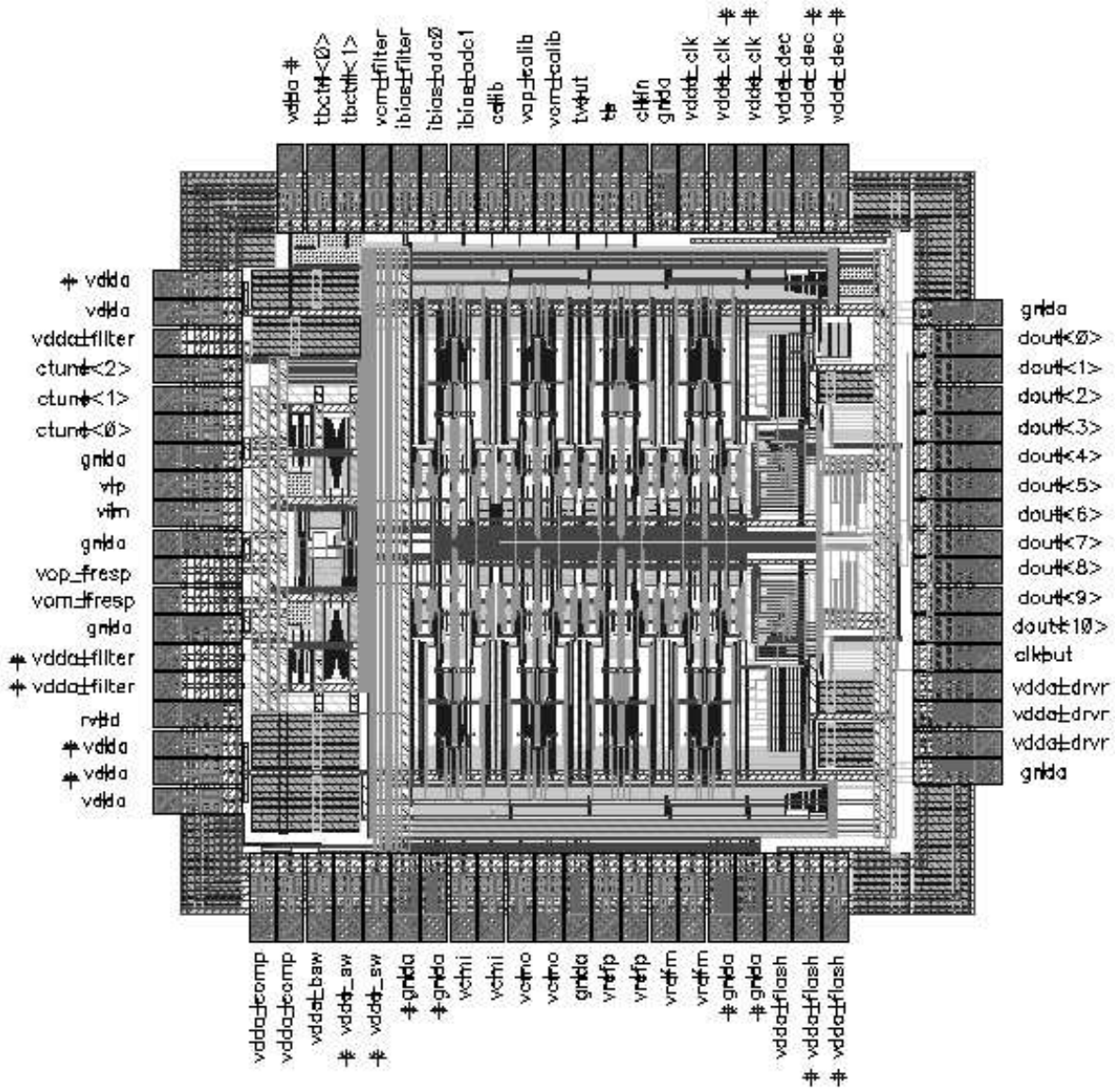


Figure 5.21: 2-channel HFB ADC layout.

CHAPTER 6

PCB DESIGN AND IC CHARACTERIZATION

The IC designed in 0.35 μm CMOS process was fabricated using Europractice foundry services. The photograph of the die is shown in Fig 6.1 and the test PCB designed for characterization of the prototype is shown in Fig 6.2.

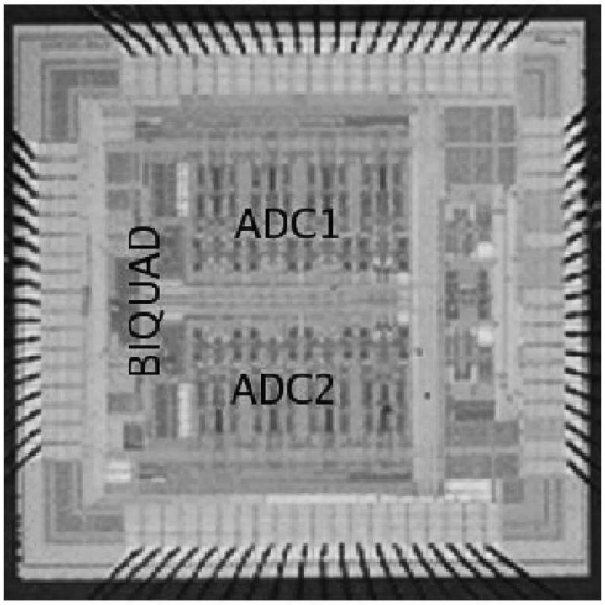


Figure 6.1: Die photograph

6.1 PCB Design

The PCB top level schematic is shown in Fig 6.3. The single ended input source is converted to differential input using a differential transformer. Being a passive element, the same transformer is employed for differential to single-ended conversion of the test buffer output. The reference voltages V_{refp}, V_{refm} are generated on the board. Specific details of the PCB design are provided in the Appendix.

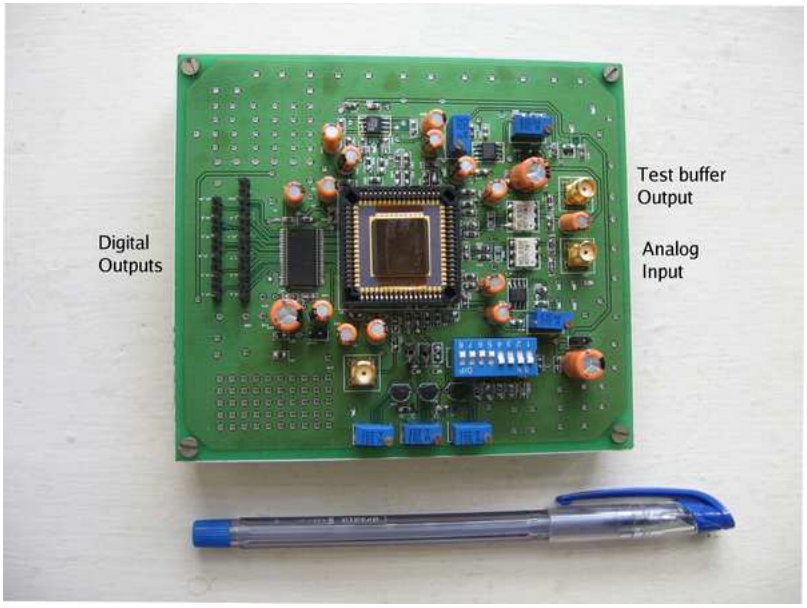


Figure 6.2: PCB designed for prototype characterization

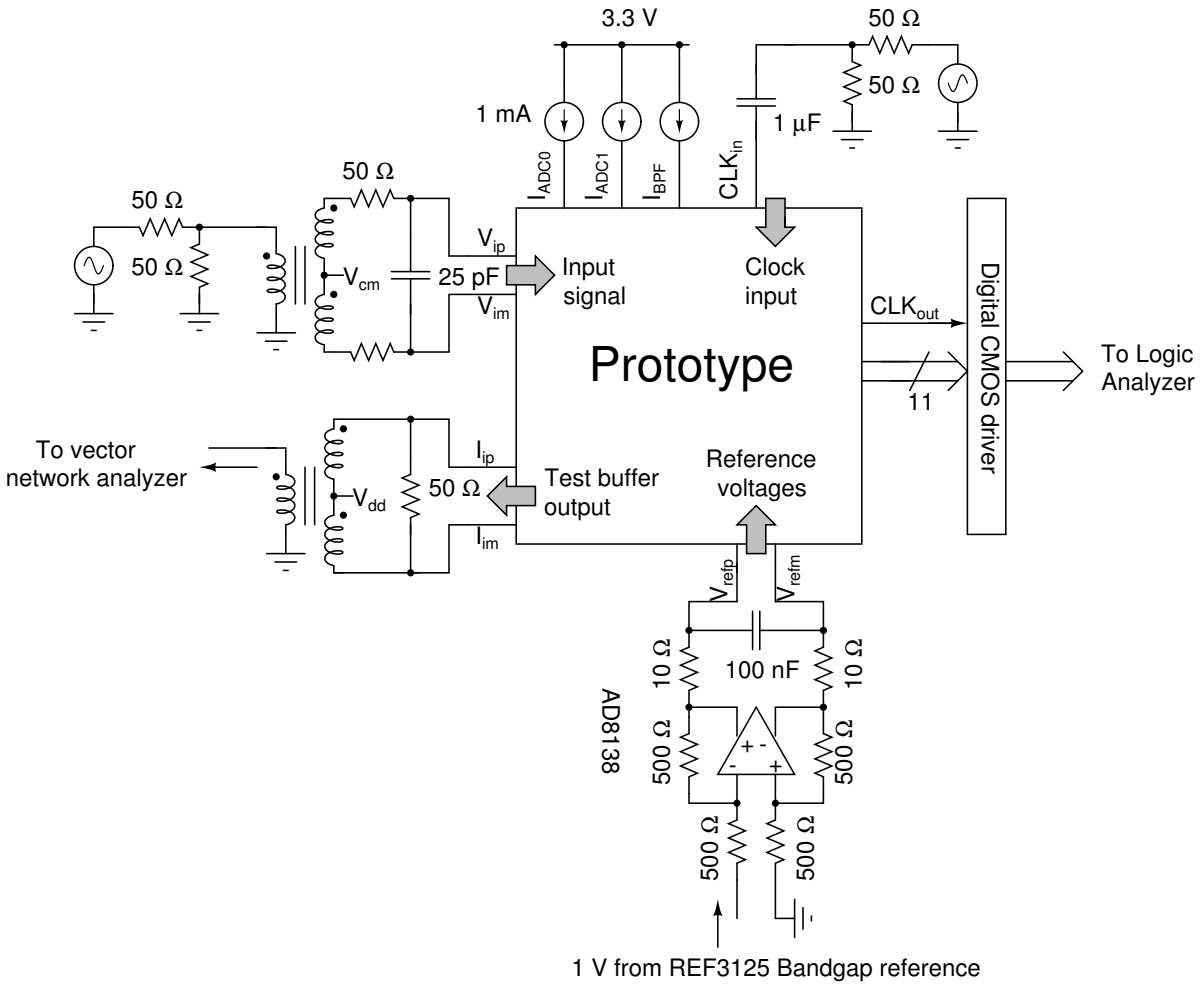


Figure 6.3: PCB top level schematic

6.2 IC Characterization

The following tests on the prototype IC have been carried out.

- Characterization of sub band ADC
  - DNL/INL using histogram technique
  - SNR/SNDR measurement
- Characterization of the Bandpass filter (BPF)
  - Obtaining the frequency response for various bandwidth settings
  - Obtain the distortion of the filter for inputs at f_{in} = 15 MHz, 40 MHz
  - Estimation of IIP3

6.3 Characterization of the sub band ADC

The static/dynamic characteristics of the ADC need to evaluated. The static characteristics include DNL/INL and the dynamic characteristics include SNR, SNDR and SFDR.

6.3.1 DNL/INL using histogram technique

The histogram technique [Doernberg *et al.* (1984)] was employed to compute the DNL/INL of the channel 0 ADC. Most likely due to fabrication problems (as discussed later), there was 8 LSB noise at the ADC output. Hence the ADC was characterized at 8-bit level. DNL/INL of channel 0 ADC is done at two different sampling rates - 20 MHz and 40 MHz. The code density plots are shown in Fig 6.4 and 6.5. DNL plots at two different sampling rates are shown in Fig 6.6 and 6.7. INL plots are shown in Fig 6.8 and 6.10. At 20 MHz the maximum DNL/INL was 0.49/1.8 LSB. At 40 MHz the

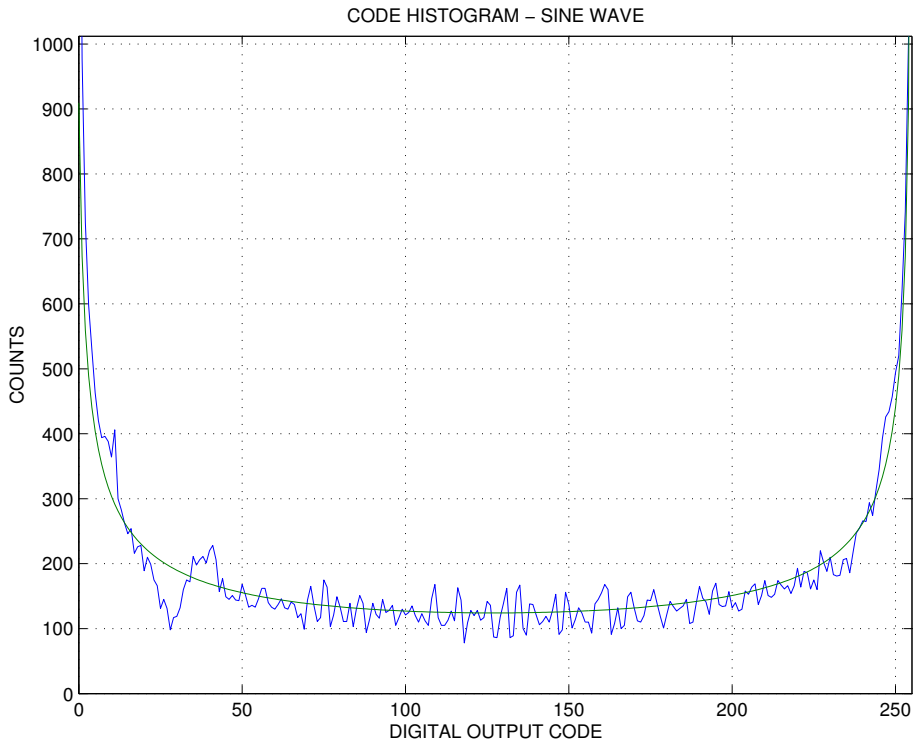


Figure 6.4: Output histogram for full scale input at 20 MHz sampling rate

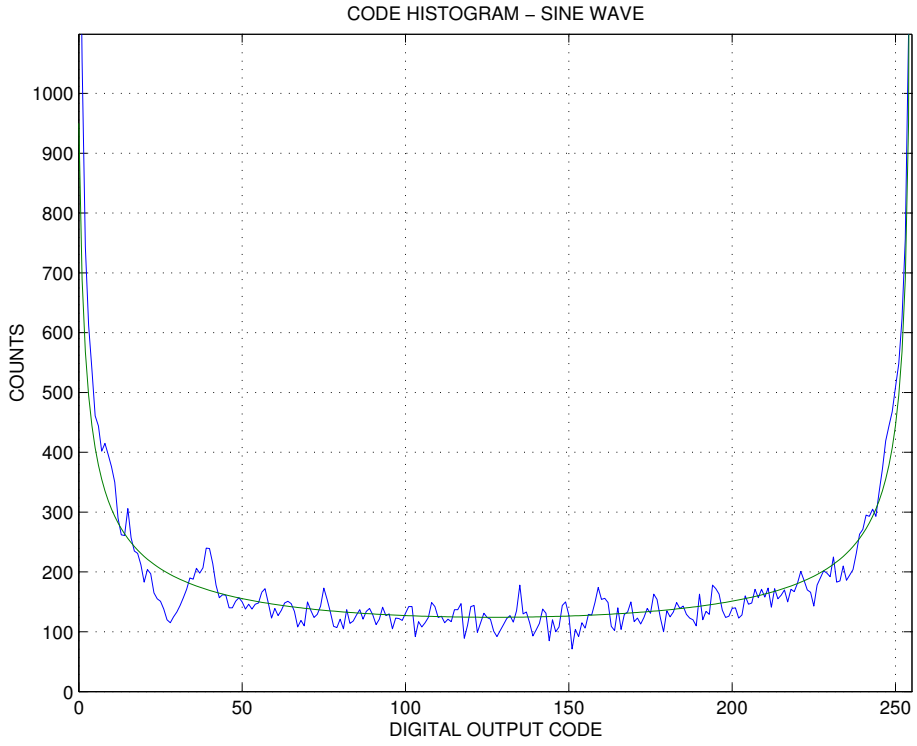


Figure 6.5: Output histogram for full scale input at 40 MHz sampling rate

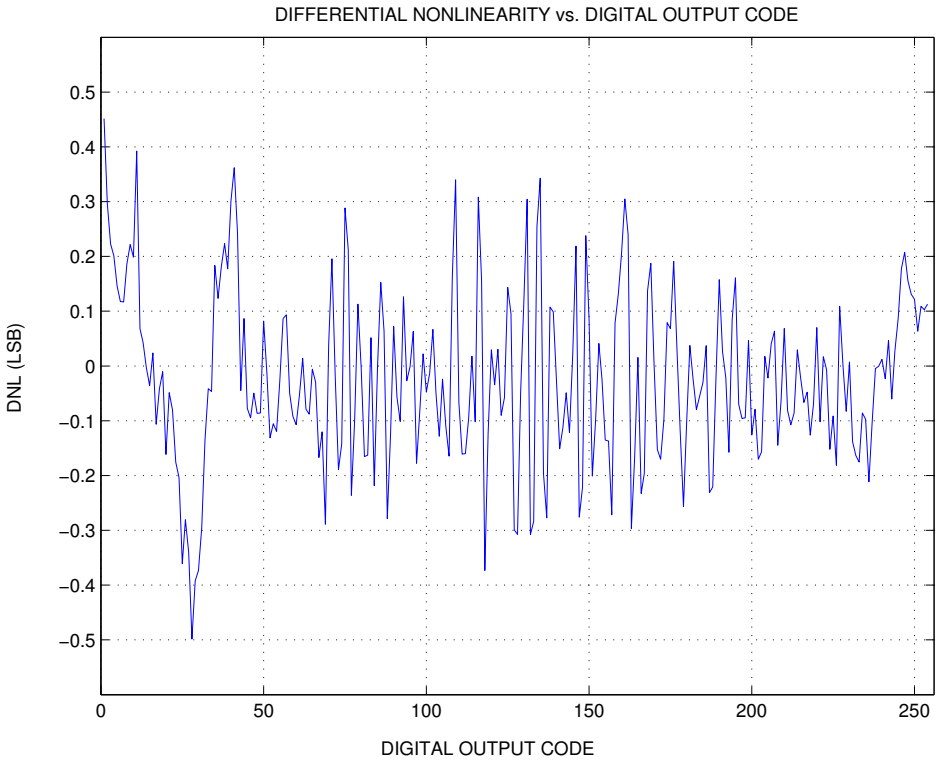


Figure 6.6: DNL plot for full scale input at 20 MHz sampling rate

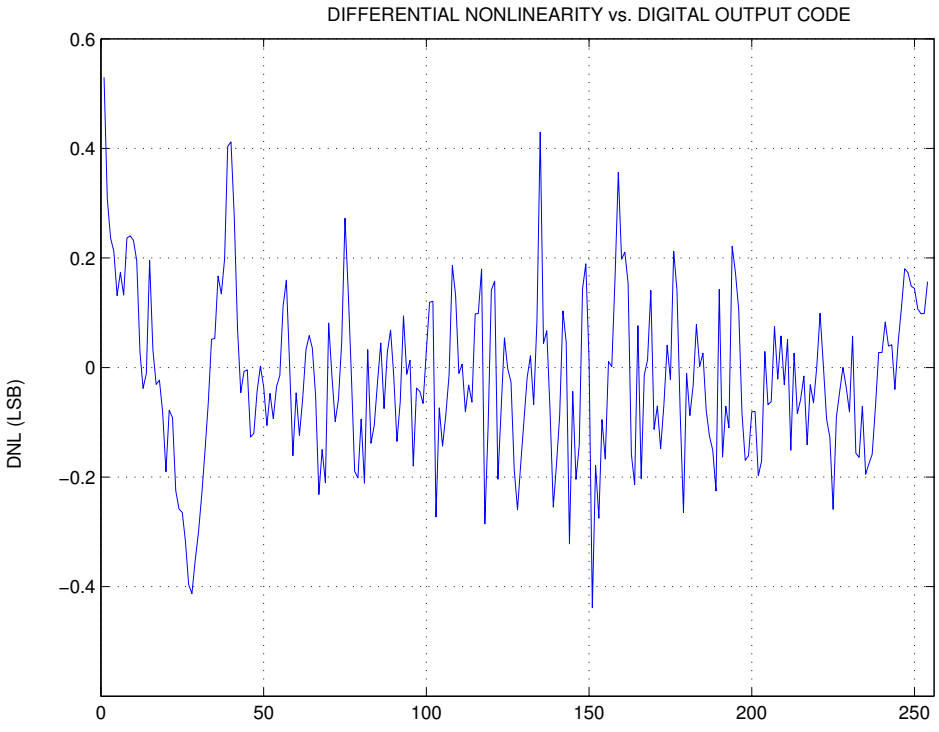


Figure 6.7: DNL plot for full scale input at 40 MHz sampling rate

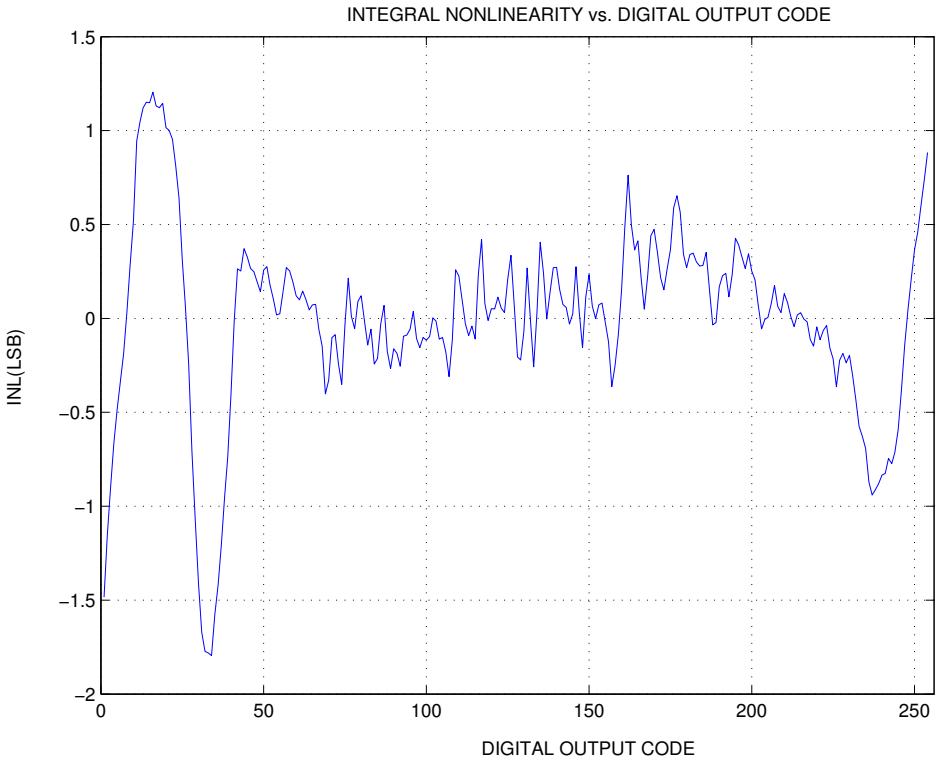


Figure 6.8: INL plot for full scale input at 20 MHz sampling rate

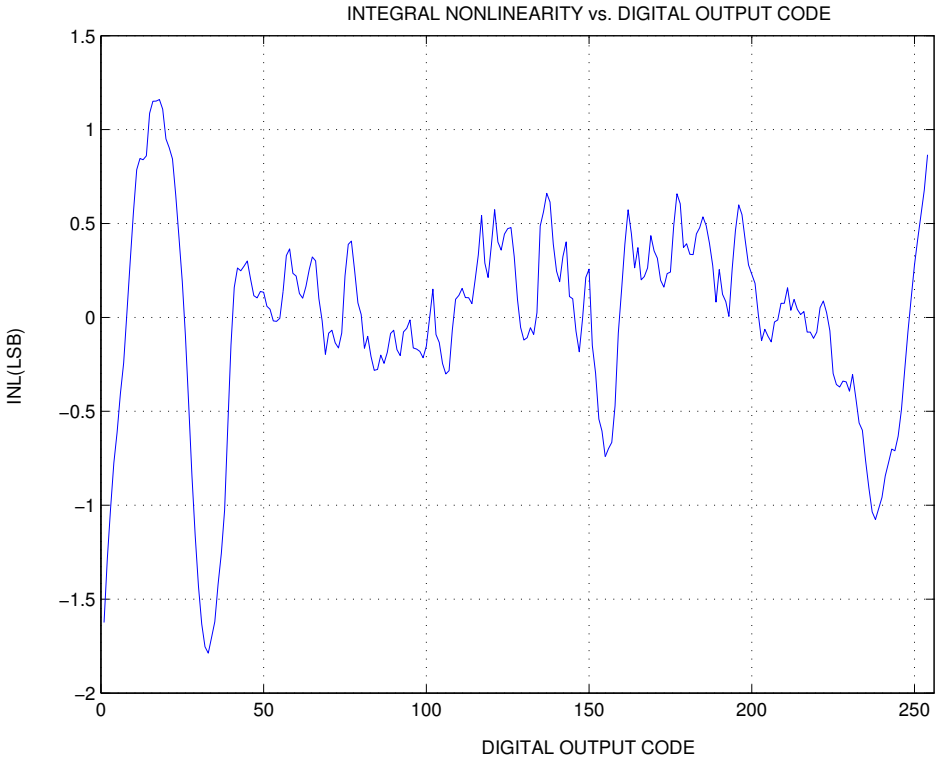


Figure 6.9: INL plot for full scale input at 40 MHz sampling rate

maximum DNL/INL was 0.53/1.82 LSB. The DNL/INL look very similar at 20 and 40 MHz indicating that the opamp outputs are settling comfortably.

6.3.2 SNR/SNDR measurement

The SNR and SNDR measurements were done on the channel 0 ADC (using all the 11-bits) for an input with $\frac{f_{in}}{f_s} = \frac{4011}{4000}$. The SNDR was found to be 42.4 dB and the SNR was 56 dB. Significant HD2 and HD3 were observed. The HD2 was -50 dB and HD3 was -54 dB. The second order distortion can be attributed due the nonlinearity in the input-output characteristic caused by the MDAC stage comparator offset (as will be discussed later).

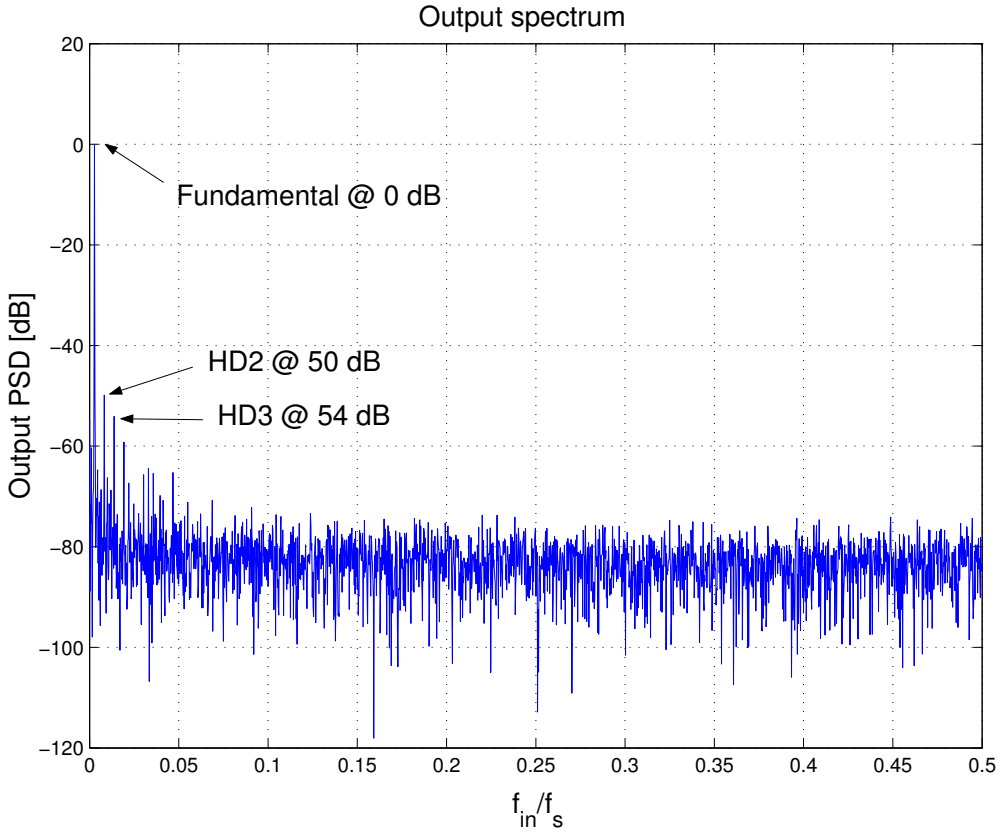


Figure 6.10: Output spectrum for Channel 0 ADC using 4K point FFT

6.4 Characterization of the Bandpass filter (BPF)

6.4.1 Frequency response of the BPF

The frequency response of the BPF measured using a vector network analyzer for various tuning capacitor settings is shown in Fig 6.11. The desired center frequency was 40 MHz and the obtained center frequency after tuning was 44.5 MHz.

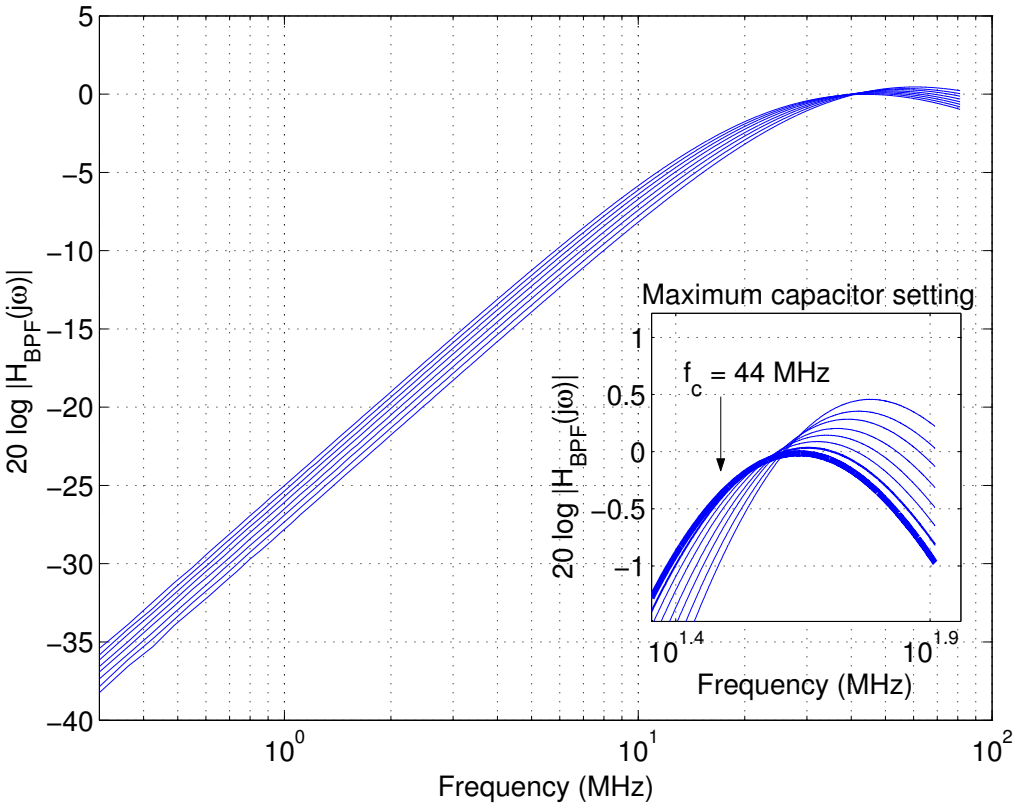


Figure 6.11: Frequency response of the bandpass filter for 7 capacitor settings

6.4.2 Distortion of the BPF

The distortion of the bandpass filter has been characterized at 2 different frequencies i.e. 15 MHz and 40 MHz. The input signal strength was set at 4 dBm ($\approx 1V_{pp}$). Table 6.4.2 shows the results. The significant HD2 at the output filter has been justified

Setting	f_c MHz	Gain at f_c
000	60.30	1.05
001	57.68	1.04
010	54.88	1.03
011	52.39	1.02
100	49.15	1.01
101	47.53	1.00
110	45.66	1.00
111	44.47	0.99

Table 6.1: Center frequency f_c, Gain at f_c for various capacitor settings

because of the offset (600 mV) present at the differential output of the BPF.

f_{in} MHz	Fundamental [dBm]	HD2 [dB]	HD3 [dB]
15	3.1	-37.5	-47.3
40	4.4	-38.7	-54.3

Table 6.2: Distortion measurement

6.4.3 IIP3 characterization of the BPF

At resonance frequency f_c = 44.4 MHz, the gain of the BPF has been found to be 0.99. Third-Order Intercept Point (IP3) is a figure-of-merit for linearity. Higher IP3 means better linearity and less distortion. IP3 is commonly tested with two input tones In the BPF, at the center frequency f $_c$, the output IP3 and input IP3 will be the same.

Two input tones at 43.5 MHz and 44.5 MHz are mixed and fed to the BPF. Due to 3^{rd} order distortion, there will be tones at 45.5, 42.5 MHz. Since the test buffer attenuates the input signal by 8, an wide band RF amplifier with a gain of 30 dB is used amplify the output of test buffer. Non-linearity of the RF amplifier has not been accounted due the wide input range (12 V_{pp}).

IIP3 can be computed using the formula

$$IIP3 = P_{in} + \frac{IM3}{2} = -6 + \frac{54}{2} = 21\ dBm \approx 2.51\ V_{rms}$$

Fig 6.12 shows the output spectrum to two-tone inputs.

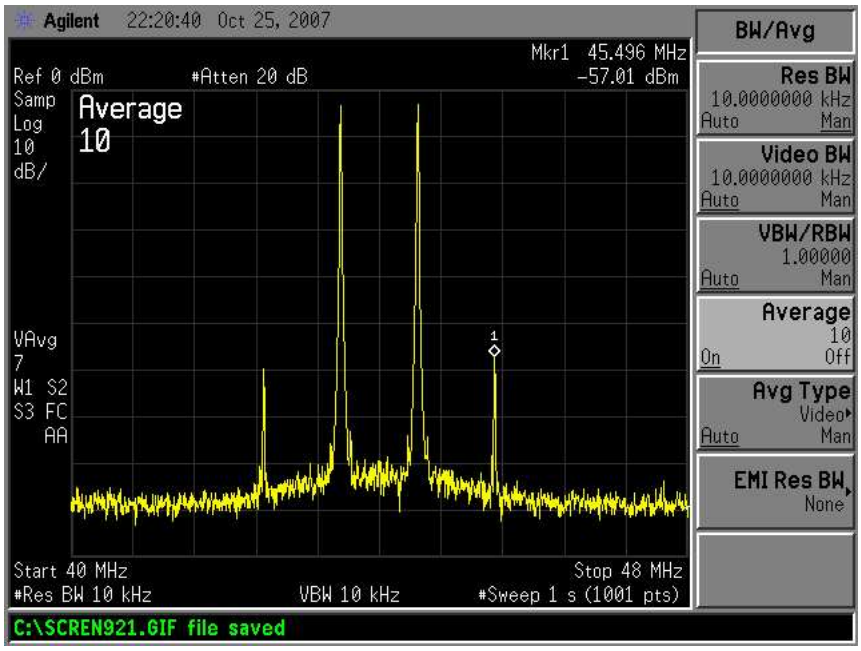


Figure 6.12: IIP3 measurement of the filter

6.5 Problems encountered during IC characterization

- The offset voltage of each ADC is measured using zero-input condition. The channel with the BPF shows large offsets ($\approx$ 600 mV). Due to this characterization of DNL/INL of the channel with BPF (channel 1) is not possible.
- Due to output offset in the filter path, the BPF shows significant second order distortion.
- The ADCs in both the channels show 3-bit toggles around the envelope of the input signal. Due to this, the characterization results are shown for 8-bit resolution only.
- Due to offset in the filter path, complete characterization of the system to estimate the SNR/SNDR was not possible. The SNDR of the complete system is limited due to the distortion introduced in the BPF channel. With reduced swing to avoid

clipping, the system characterization was done and the characterization results are shown in next section.

The offsets observed at the filter output are much larger than the maximum random offset calculated for the device sizes used. This was observed across several chips. This was unusual, as several filters with excellent repeatable performance have been designed by other group members in the same technology[Pavan and Laxminidhi (2007), Pavan and Laxminidhi (2006)].

These filters are based on the Gm-C architecture, which are a lot more sensitive to device mismatch compared to the active-RC filter used in this design. Analysis of the ADC DNL/INL indicates that random mismatch in the comparator exceeds the large margin inherent to the ADC architecture, leading us to believe that this particular IC run was probably defective.

6.6 HFB system characterization.

Due to the subband ADC not being to achieve full resolution, the HFB system has been characterized at 8-bit accuracy level. Fig 6.13 shows the equivalent system that will be used for characterization. The ADC has been designed for an input range of 2 V_{pp}. Due to the offset of 600 mV at the BPF output, the maximum input that can be applied such that there will be no clipping at the output of the filter path channel ADC is 800 mV_{pp} only.

To obtain the impulse responses of the synthesis filter $F_0(z)$ and $F_1(z)$, is is necessary to know the frequency response of the bandpass filter from DC to 40 MHz (in increments of 78.125 kHz to be able to solve the synthesis filters to atleast 512 points). But

the operating range differential transformer used on the PCB is from 400 kHz to 800 MHz. The approximate magnitude response from DC to 400 kHz is obtained using the low frequency path on the PCB. The phase information is extrapolated from the phase response obtained from 400 kHz to 40 MHz. After obtaining the frequency response of the BPF, the synthesis filter taps are computed using **ifft** routine in Matlab.

Figs 6.14 and 6.15 show the impulse responses obtained by using the procedure outlined in Chapter 3. Another important observation is that the system can be characterized with full swing at very low input frequencies but at high frequencies (as $f_{in} \rightarrow f_s$), the bandpass filter starts distorting due to the offset in the filter path. When characterized at a low input frequency as shown in Fig 6.16, the SNDR was found to be 37.5 dB. The measured noise floor is 41 dB. The ideally expected noise floor in the implementation of a 2 channel HFB with 8-bit ADCs is 44 dB.

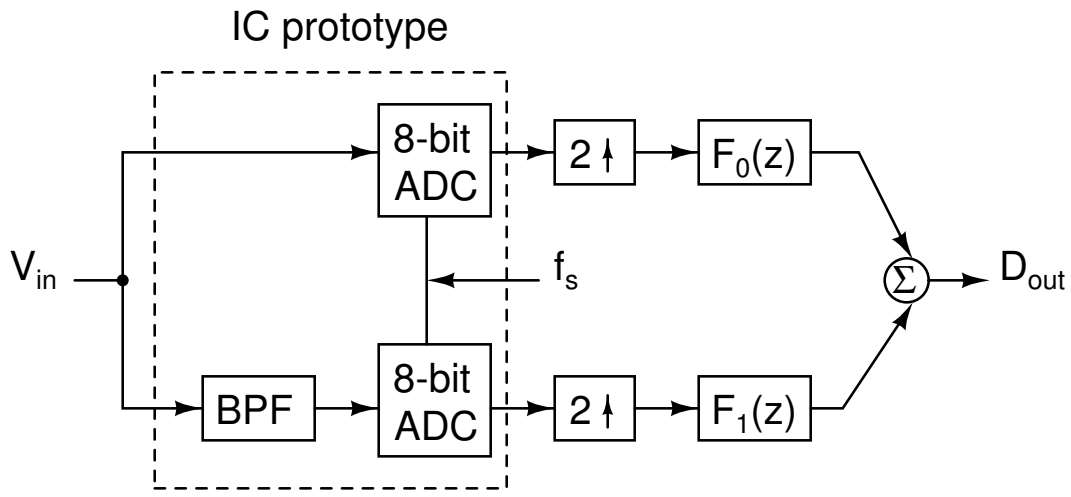


Figure 6.13: Equivalent model at 8-bit accuracy level

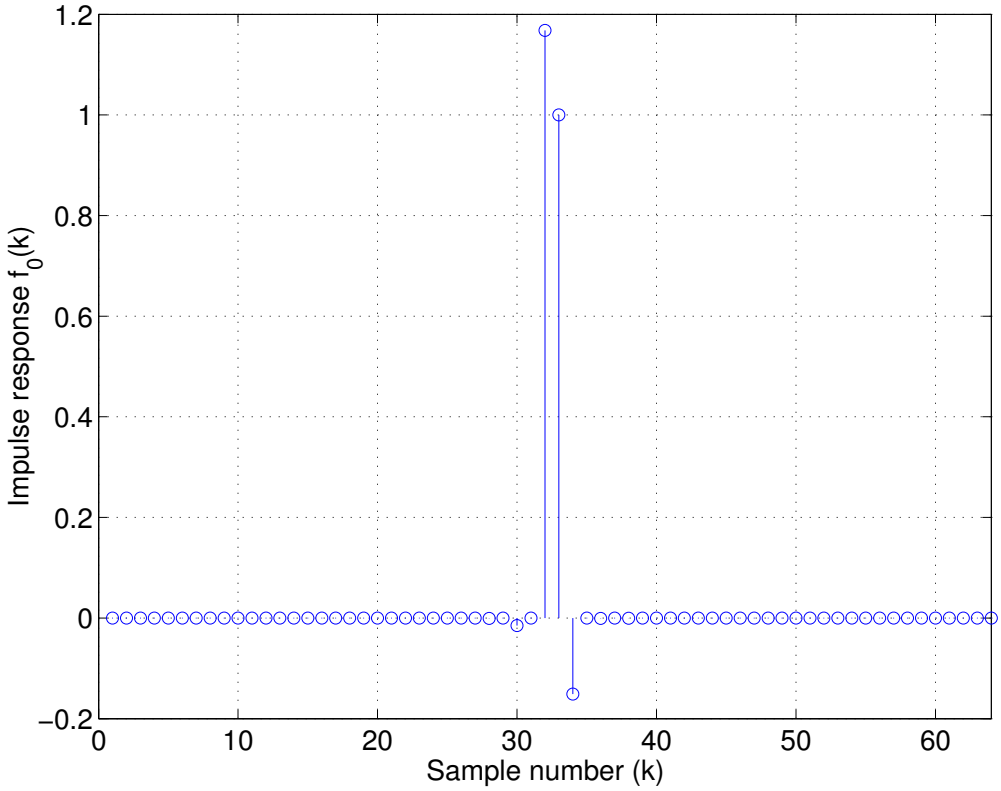


Figure 6.14: 64 tap impulse response of $F_0(z)$

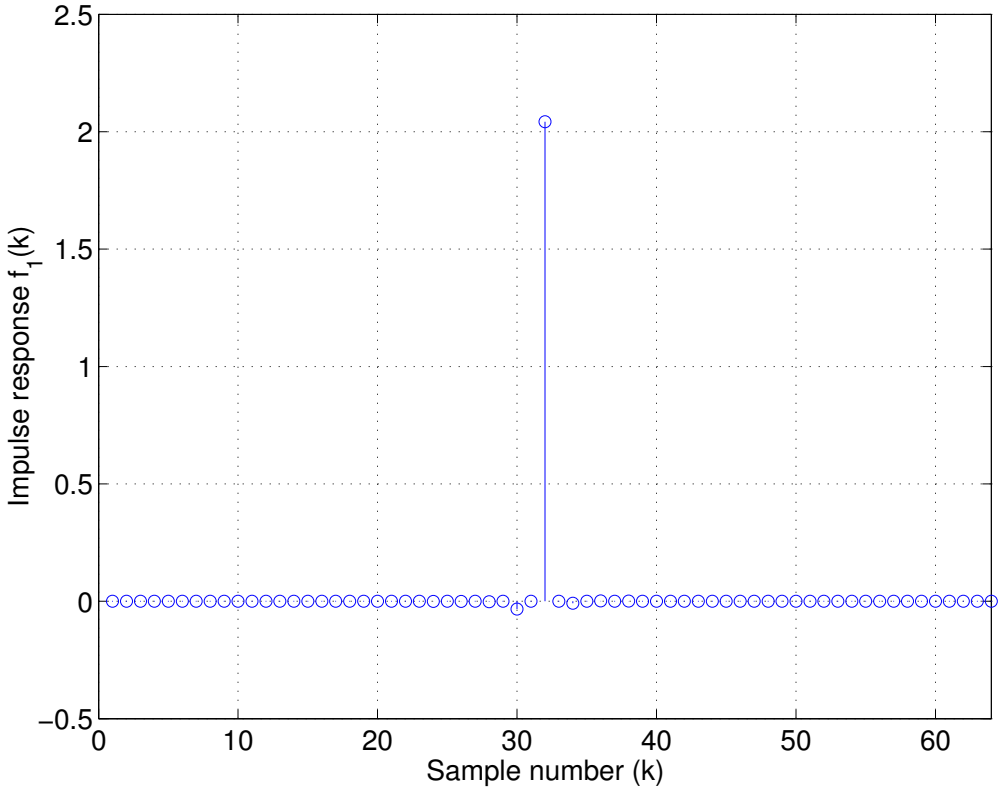


Figure 6.15: 64 tap impulse response of $F_1(z)$

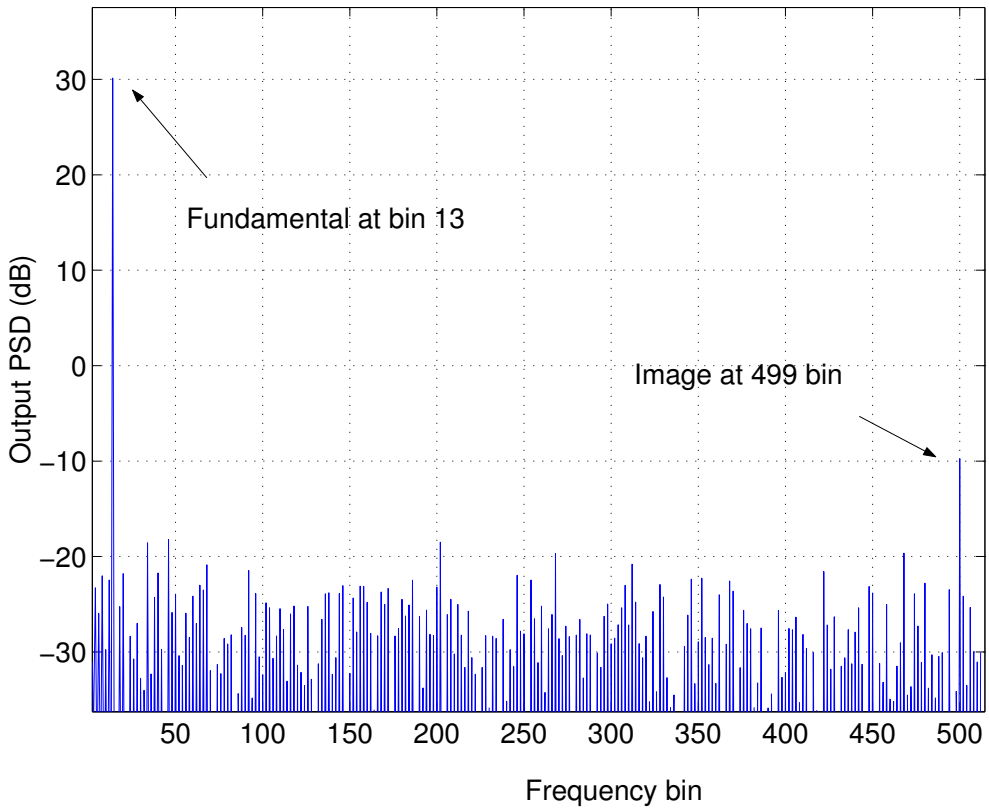


Figure 6.16: Output spectrum to input of $f_{in} = \frac{13}{512} f_s$

CHAPTER 7

DEBUG OF ERROR SOURCES IN THE PROTOTYPE

The two major impairments observed in the fabricated prototype were - the sub band ADC not achieving its full resolution (due to missing codes at the 10-bit level) and the significant second/third order distortion in the BPF (due to offset). Possible error sources were identified for these artifacts. They are discussed in this chapter. A technique to model (in Matlab) all important parameters of the pipelined ADC from the static characterization results (DNL/INL) is discussed.

7.1 Explaining missing codes in pipeline ADC at 10-bit level

At 10-bit resolution, the pipeline ADC was exhibiting missing codes (around 80 missing codes). There was around 3-bit toggles (± 8 code jumps) when the channel 0 ADC was fed with a very low frequency ramp input signal. To debug such behavior, one needs to fit the static characteristics of the ADC to a Matlab model and find out which could the possible error causing block. Since the ADC itself comprises repeated MDAC stages, we first look at the important MDAC stage parameters. Dynamic problems (like opamp settling) were ruled out because the DNL & INL characteristics were very similar at 20 & 40 MSPS rates.

7.1.1 MDAC stage parameters (gain, opamp offset, comparator offset)

The typical architecture of a 1.5 bits/stage MDAC is shown in Fig 7.1. The four important parameters of a MDAC stage are - gain (nominally 2), two comparator thresh-

olds (nominally V_{ref}/4, -V_{ref}/4) and input referred offset of the opamp (nominally 0). When opamp sharing technique [Nagaraj *et al.* (1997)] is used, each stage will comprise of 1 opamp, 2 switched capacitor loops and 4 comparators. Effectively each stage can be characterized by the following 7 parameters - 2 gains, 4 comparator thresholds and 1 input referred opamp offset.

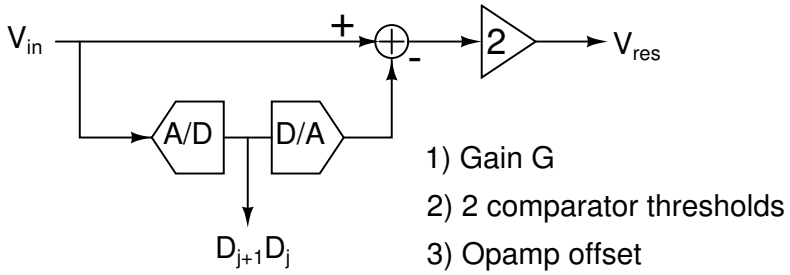


Figure 7.1: 3 MDAC stage parameters that affect the stage characteristic

7.1.2 ADC model parameters (gain, opamp offset, comparator offset, flash comparator thresholds)

Extending the same to a pipeline ADC, the number of MDAC stages employed will determine the number of parameters to be estimated. As shown in Fig 7.2, this particular IC implementation uses 4 MDAC stages and a 3-bit Flash ADC. The total number of parameters are 35 (28 MDAC stage parameters + 7 comparator thresholds in the 3-bit Flash ADC).

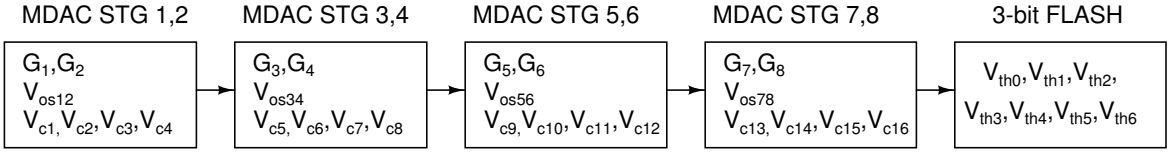


Figure 7.2: 35 ADC parameters that need to estimated

7.1.3 Estimating ADC model parameters

Rrom the measurement results it is possible to fit the DNL data to an ideal ADC with 35 programmable parameters. The error criteria used is the sum of the squared difference between DNLs of the ADC with 35 tunable parameters and the IC prototype. The technique is illustrated in Fig 7.3.

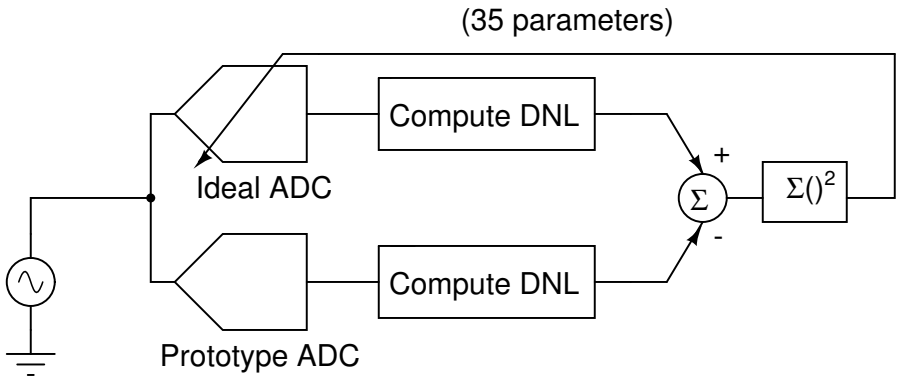


Figure 7.3: Estimation technique to fit prototype behavior to ideal ADC with programmable parameters using histogram test

7.1.4 Missing codes in the IC prototype

When a low frequency sine wave input is fed to the ADC to exercise the full output range, the output shows jumps only in the negative going cycle. Fig 7.4 shows the ADC output and the inset provides a clearer picture of the code jump around code 50 to 150. To exercise the complete range of output codes, the input to the ADC is made to swing a little above the input range. Hence, clipping in the sine wave output can be noticed in Fig 7.4. The histogram of the sine wave output is shown in Fig 7.5. All the measurements shown in this chapter are at the 10-bit level. The DNL plot shows ± 1 LSB, an indication of missing codes.

Using the estimation technique described above, a Matlab model of the ADC is

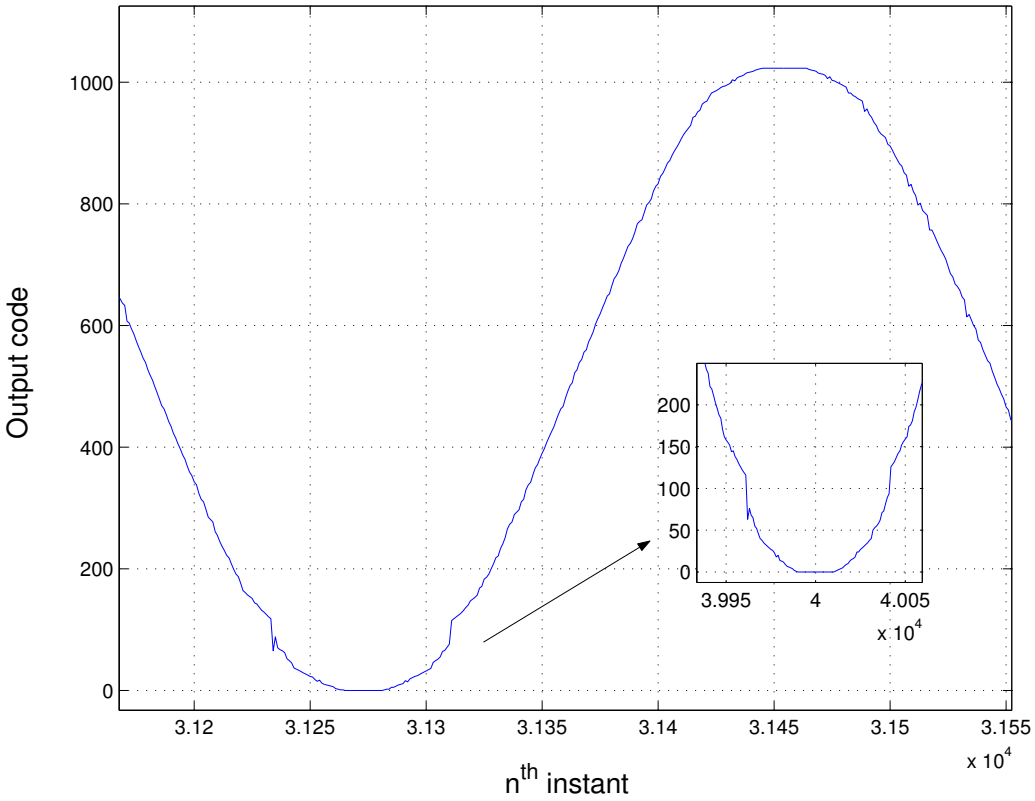


Figure 7.4: Distortion introduced in sine wave in negative cycle only indicative of errors in MDAC comparator thresholds

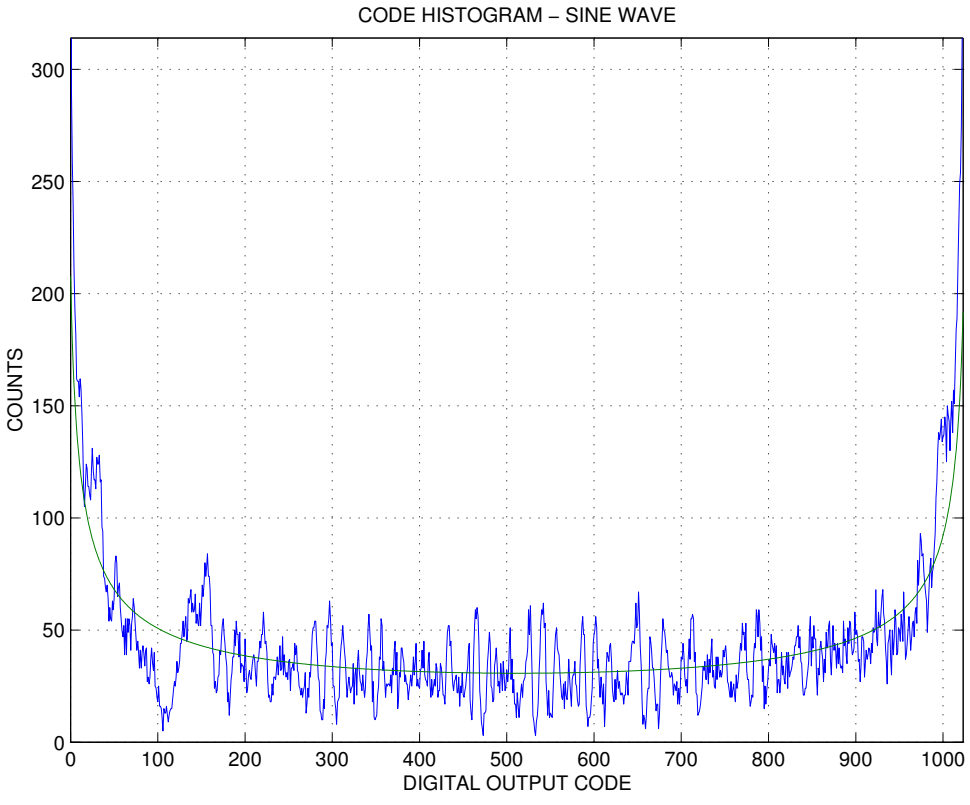


Figure 7.5: Measured Histogram at 10-bit level

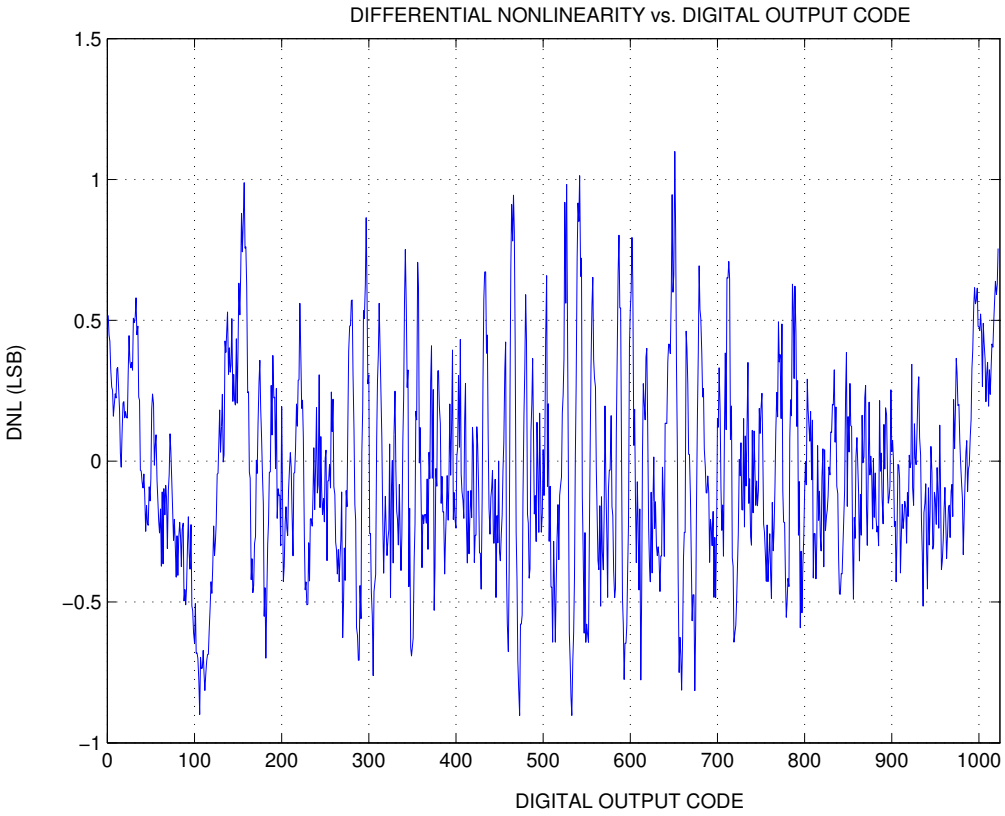


Figure 7.6: Measured DNL at 10-bit level

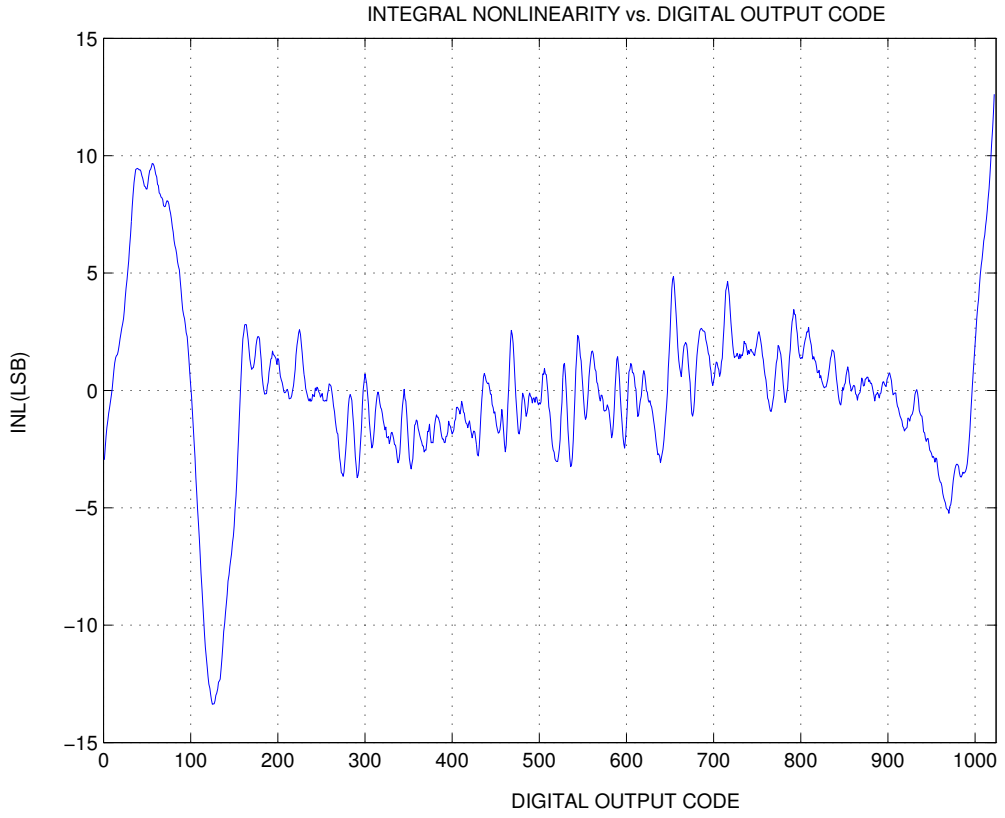


Figure 7.7: Measured INL at 10-bit level

developed which exhibits approximately the same DNL characteristic as the IC prototype. Fig 7.6 and 7.7 shown the DNL and INL plots. The DNL plots of the IC prototype and the Matlab model are shown in Fig 7.8. A linearly increasing/decreasing trend in the INL is a signature of deviation in MDAC comparator thresholds [Kuyel and Bilhan (1999)]. This is reiterated by the value of comparator thresholds obtained from the Matlab model. The various MDAC stage thresholds obtained from the model are shown in Fig 7.9. It can be seen clearly that the MDAC stage 4 (i.e. sub stage 7) comparators shown threshold voltages close to the 450 mV. The maximum tolerable offset in the 1.5 bits/stage architecture is 250 mV (assuming no other non idealities). **The MDAC stage comparators offset is therefore one of the most probable reason for missing codes.** To overcome this limitation, the ADC was characterized at only 8-bit level and the results were shown in the previous chapter.

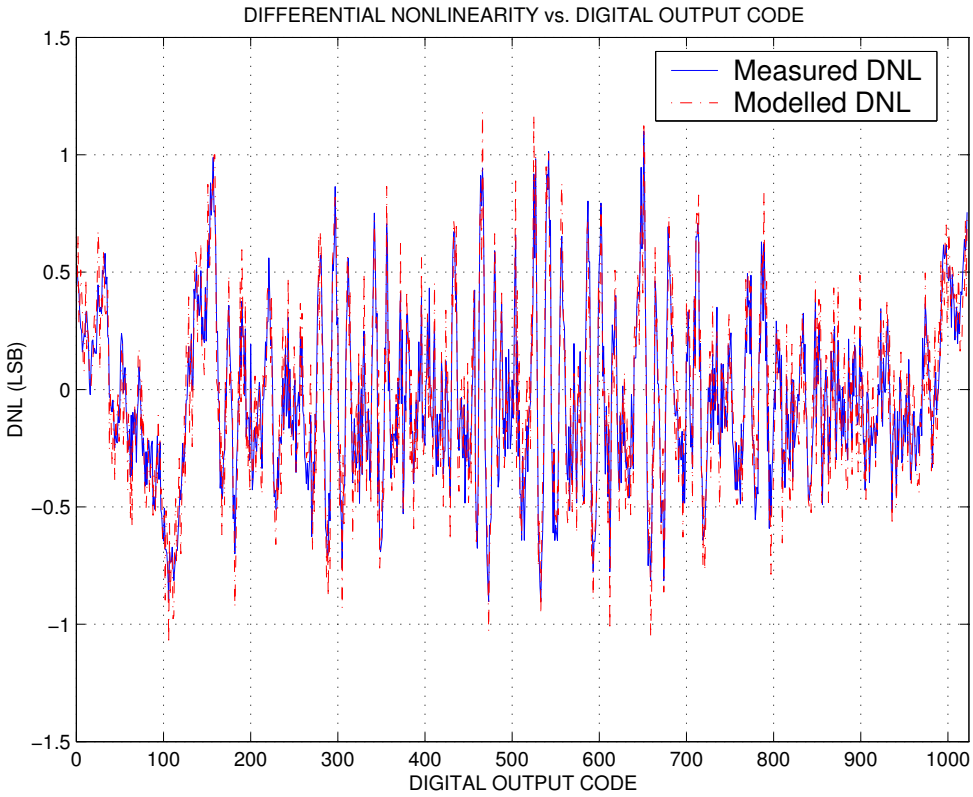


Figure 7.8: Measured and Estimated DNL at 10-bit level

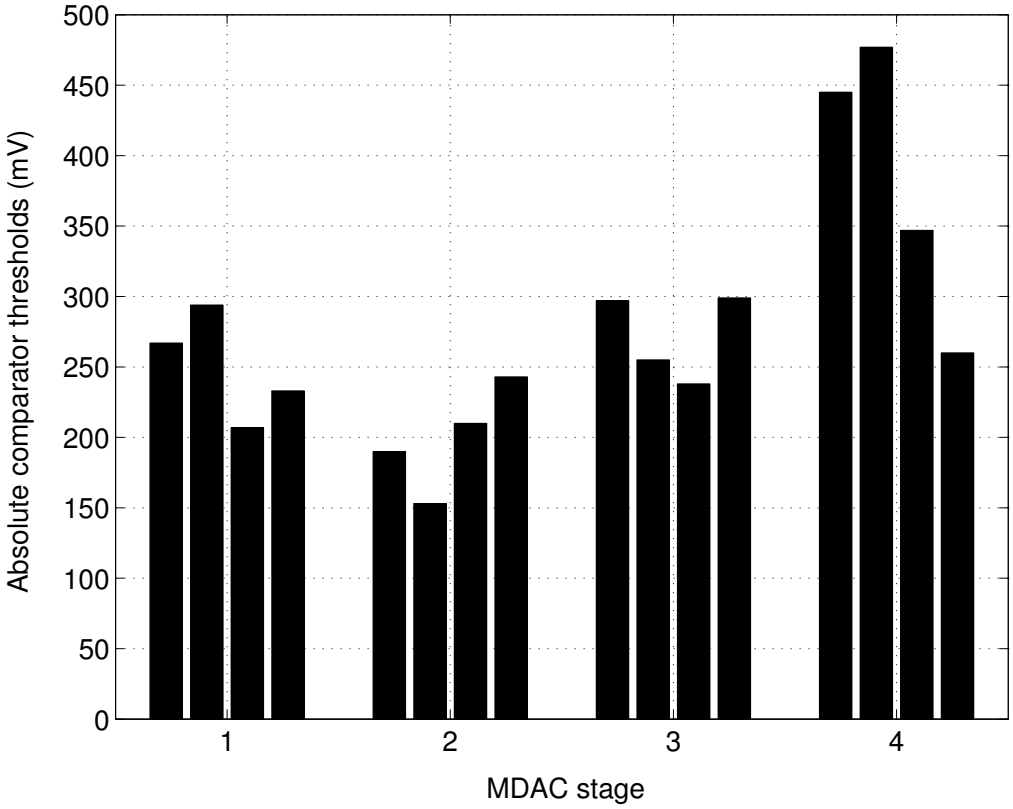


Figure 7.9: Absolute comparator thresholds in the 4 MDAC stages

7.2 BPF offset and its effect on distortion

The single ended implementation of the biquad with equivalent input referred offsets is shown in Fig 7.10. V_{os1} is the input referred offset of opamp 1 and V_{os1} is the input referred offset of opamp 2. It should be recalled that the differential implementation will not require the '-1' gain element.

As it can be seen from Table 7.1, the offset of the second opamp directly reflects at the bandpass output node. It is likely that the offset of opamp 2 is likely contributor to the bandpass offset. In the presence of such an offset, the differential swing output of opamp 1 will get limited and when a full scale input is fed to the opamp, distortion occurs. In the case of unbalanced differential outputs, we will see significant second order and third order distortion terms.

Offset source	Transfer function	Gain at DC
V_{os1}	$\left\lvert\frac{V_{out}}{V_{os1}}\right\rvert = \frac{s^2 + s\left(\frac{1}{R_2C} + \frac{2}{R_1C}\right)}{s^2 + \frac{s}{R_2C} + \frac{1}{R_1R_3C^2}}$	0
V_{os2}	$\left\lvert\frac{V_{out}}{V_{os2}}\right\rvert = \frac{\frac{s}{R_1C} + \frac{1}{R_1R_3C^2}}{s^2 + \frac{s}{R_2C} + \frac{1}{R_1R_3C^2}}$	1

Table 7.1: Effect of opamp offsets

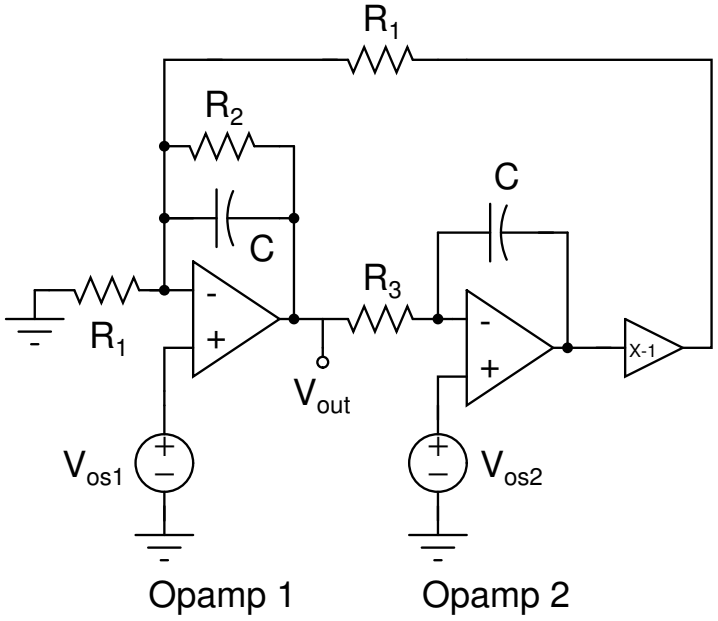


Figure 7.10: Effect of input referred opamp offsets

7.2.1 Input referred offset of the opamp

The first stage of the opamp used in the biquad is shown in Fig 7.11. For the differential pair shown in Fig 7.11, the input referred offset is given by

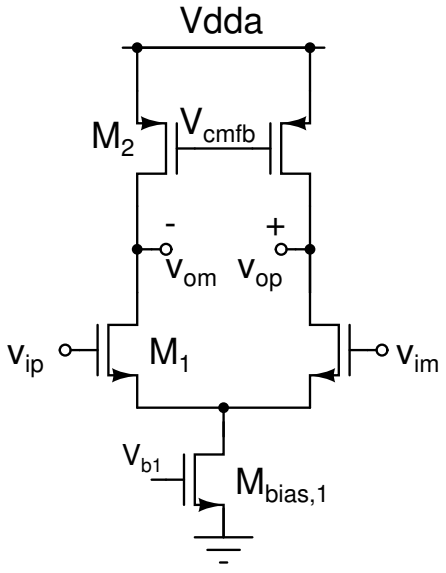


Figure 7.11: Opamp first stage

Using g_m values and device sizes from Table 5.1,

$$\Delta V_{tn} = \frac{A_{V_{T,nMOS}}}{\sqrt{WL}} = \frac{9\,\mathrm{mV} - \mu\mathrm{m}}{\sqrt{32 \times 0.35}} = 2.7\,\mathrm{mV}$$

$$\Delta V_{tp} = \frac{A_{V_{T,pMOS}}}{\sqrt{WL}} = \frac{15\,\mathrm{mV} - \mu\mathrm{m}}{\sqrt{32 \times 0.5}} = 4\,\mathrm{mV}$$

$$\sigma_{offset} = \sqrt{\Delta V_{tn}^2 + (\frac{g_{m,M2}}{g_{m,M1}})^2 \Delta V_{tp}^2} = 3.3\,\mathrm{mV}$$

From the above offset calculation due to mismatch, it can be seen that the maximum random offset ($3\sigma_{offset}$) cannot exceed 10 mV. But from measurements, it was seen that across prototype samples, the offset varied from 200 to 600 mV. **Such large variations in the offset suggest the possibility of fabrication errors**.

CHAPTER 8

CONCLUSIONS

8.1 Work done

In this work, we have explored an alternative to time interleaved A/D conversion. An optimized 2 channel HFB architecture was developed and expressions pertaining to the SNR loss in a M-channel HFB topology were derived. After arriving at the top level specifications of the 2-channel HFB ADC, the design was implemented in a 0.35 μm CMOS process. The schematic, layout was done and prototype of the IC was fabricated using Europractice IC services. A PCB was designed to test the IC prototype. Due to two problems in the prototype (i) ADC not meeting full resolution and (ii) offset at the filter output, it was not possible for the prototype to achieve the intended specifications.

8.2 Further work

Errors corresponding to the MDAC stage comparator offsets can be avoided using an alternate comparator topology with lesser input referred offsets or a preamp+comparator topology can be explored. An important observation was that the frequency measurement technique used in this implementation is susceptible to errors when encountered with offsets in the filter path (the input signal seen by the filter path test buffer and the direct path test buffer differ in the DC content when the filter output has an offset voltage). An improved frequency response measurement technique which avoids the above problem can be used.

APPENDIX A

PCB DESIGN SCHEMATICS

A.1 PCB Design

The top level schematic is segmented into the following sub-schematics

- ADC Chip schematic shown in Fig A.2.
- Analog inputs schematic shown in Fig A.3.
- Bias & References schematic shown in Fig A.4.
- Digital Buffer schematic shown in Fig A.5.
- Supply input & Bypass capacitors schematic shown in Fig A.6.
- Test logic schematic shown in Fig A.7.

Important details regarding the design of each of the sub-schematics is discussed in the sections that follow.

A.1.1 ADC Chip schematic

At the supply inputs of the ADC, a combination of 1 μF through-hole (TH) capacitor and 100 nF surface mount (SM) capacitor are used bypass capacitances. The analog and digital supply pins are named as A_VDD_3P and D_VDD_3P. The TOP and BOTTOM plane copper pour areas are connected to GND to ensure uniform GND across the PCB. Multiple VIAS uniformly spread across the PCB are used to connect the TOP and BOTTOM GND planes.

A.1.2 Analog inputs & outputs schematic

The ADC inputs are differential and the output of the test buffer which will be used for measuring the bandpass filter response are also differential. For single ended to differential conversion and vice versa, ADT1WT differential transformer will be used. The common mode input signal to ADT1WT is bypassed using a 100 nF SM capacitor. Analog inputs to the ADC are low pass filtered using a first order RC filter (50 Ω, 50 pF) whose 3-dB frequency is approximately 60 MHz. The input signal bandwidth is 40 MHz only. The clock to the ADC is AC coupled using a 100 nF SM capacitor.

A.1.3 Bias & References inputs schematic

The ADC requires 3 different bias currents - for ADC0, ADC1 and the BPF. Each of the bias currents are generated using LM334 IC. The supply to all the 3 LM334 ICs should by appropriately bypassed. The differential voltage references V_{refp} and V_{refm} are generated us AD8138. The single ended reference input of 1 V to AD8138 is generated using a REF3125 (2.5 V bandgap reference) and is set to 1 V using a voltage divided. VCMO is also generated in a similar fashion.

A.1.4 Digital Buffer schematic

ALB16244 IC is used as a digital buffer to be able to drive the logic analyzer probes. The input and output levels of this IC are fully CMOS compatible (3.3 V).

A.1.5 Supply input & Bypass capacitors schematic

The supply points corresponding to A_VDD_3P and D_VDD_3P are bypassed using a 100 μF TH capacitor. The supply rail routing on the PCB is made 25 mil wide to ensure minimal IR drop across the board.

A.1.6 Test logic schematic

A 8 switch DIP is used to cset the various control pins to VDD/GND. When the switch is OFF, a pull down resistor should be used to bring the control pin voltage back to GND. This is achieved by using 20 kΩ resistors for pull down.

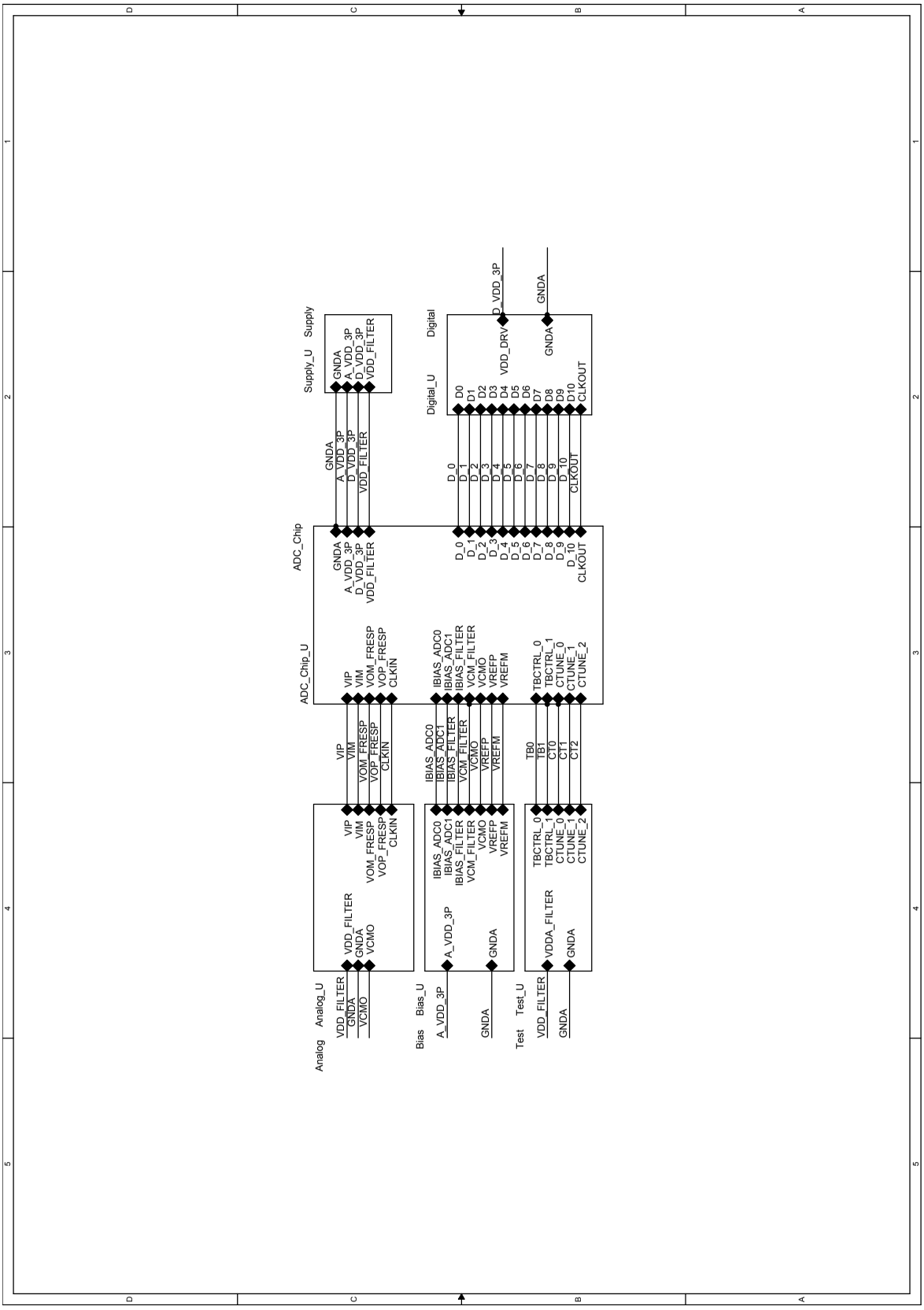


Figure A.1: PCB top level schematic

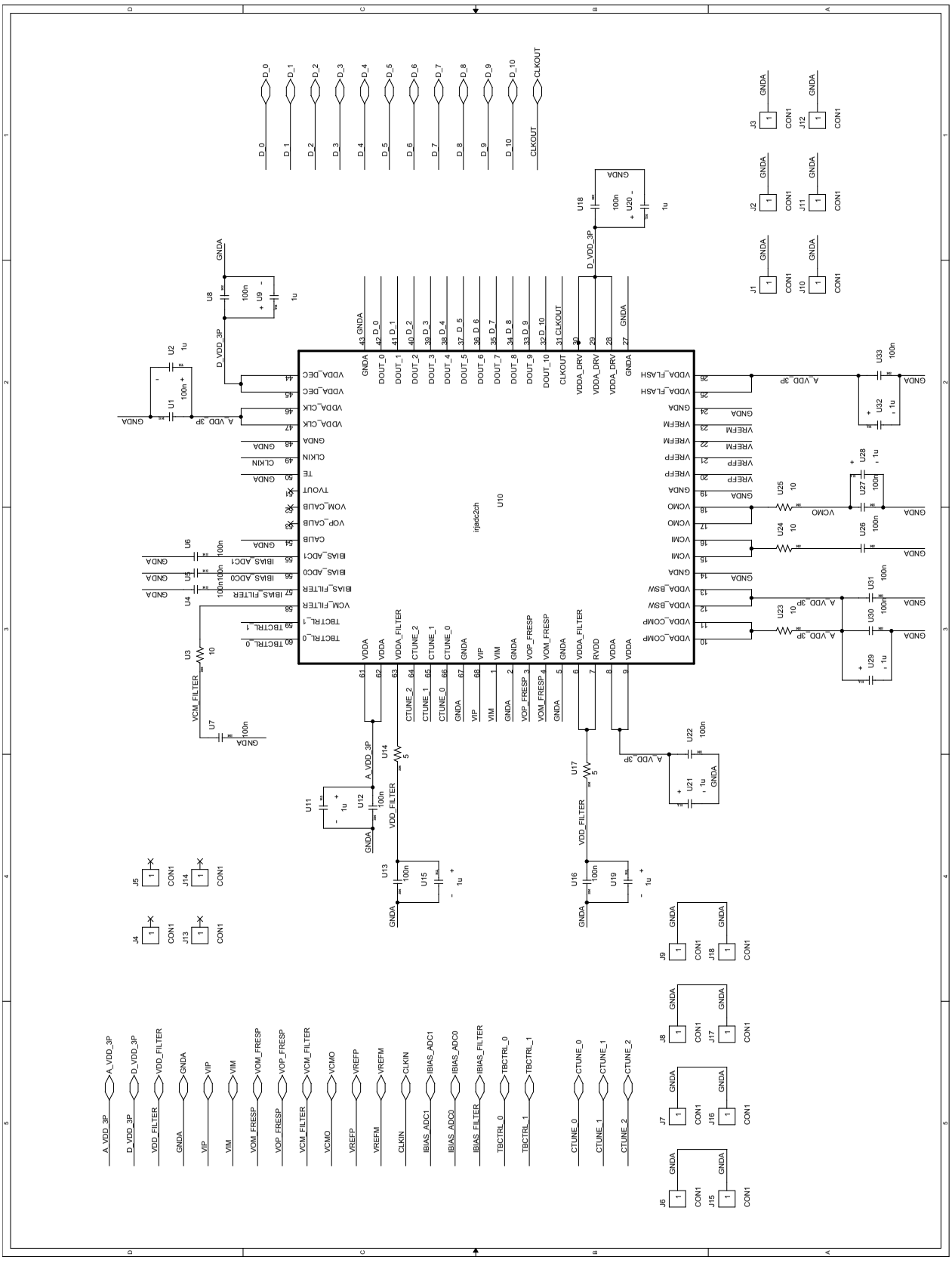


Figure A.2: ADC Chip schematic

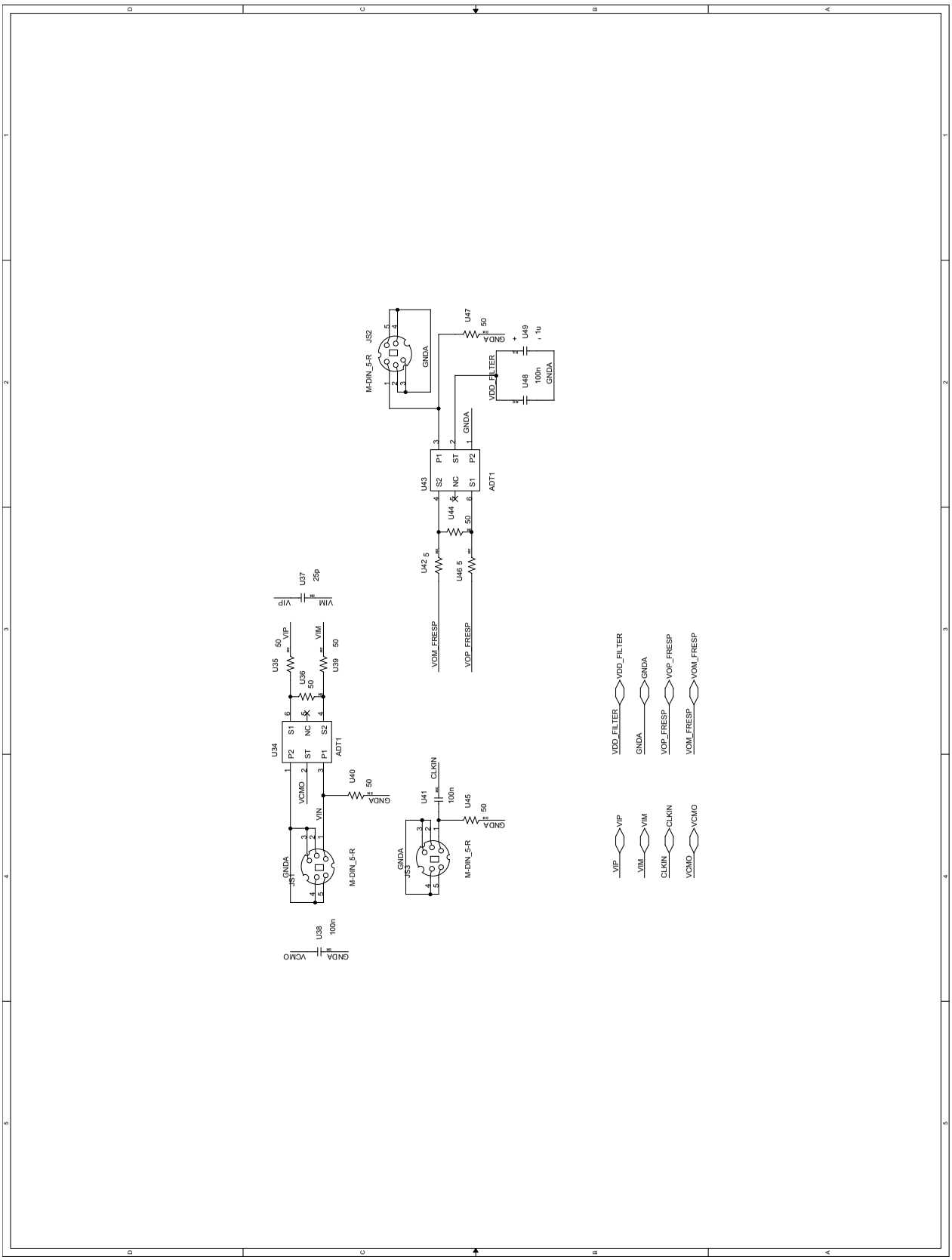


Figure A.3: Analog inputs schematic

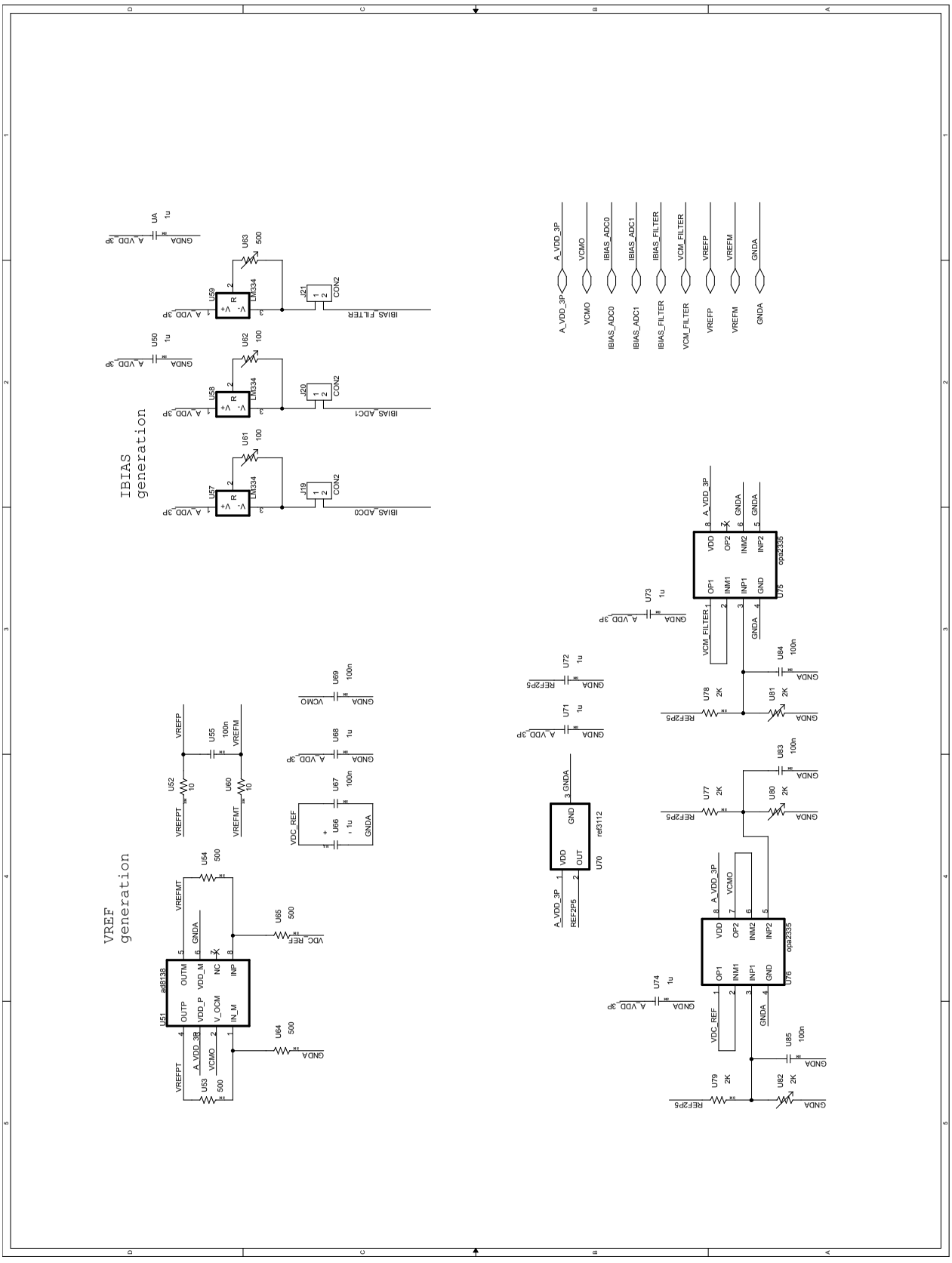


Figure A.4: Bias & References schematic

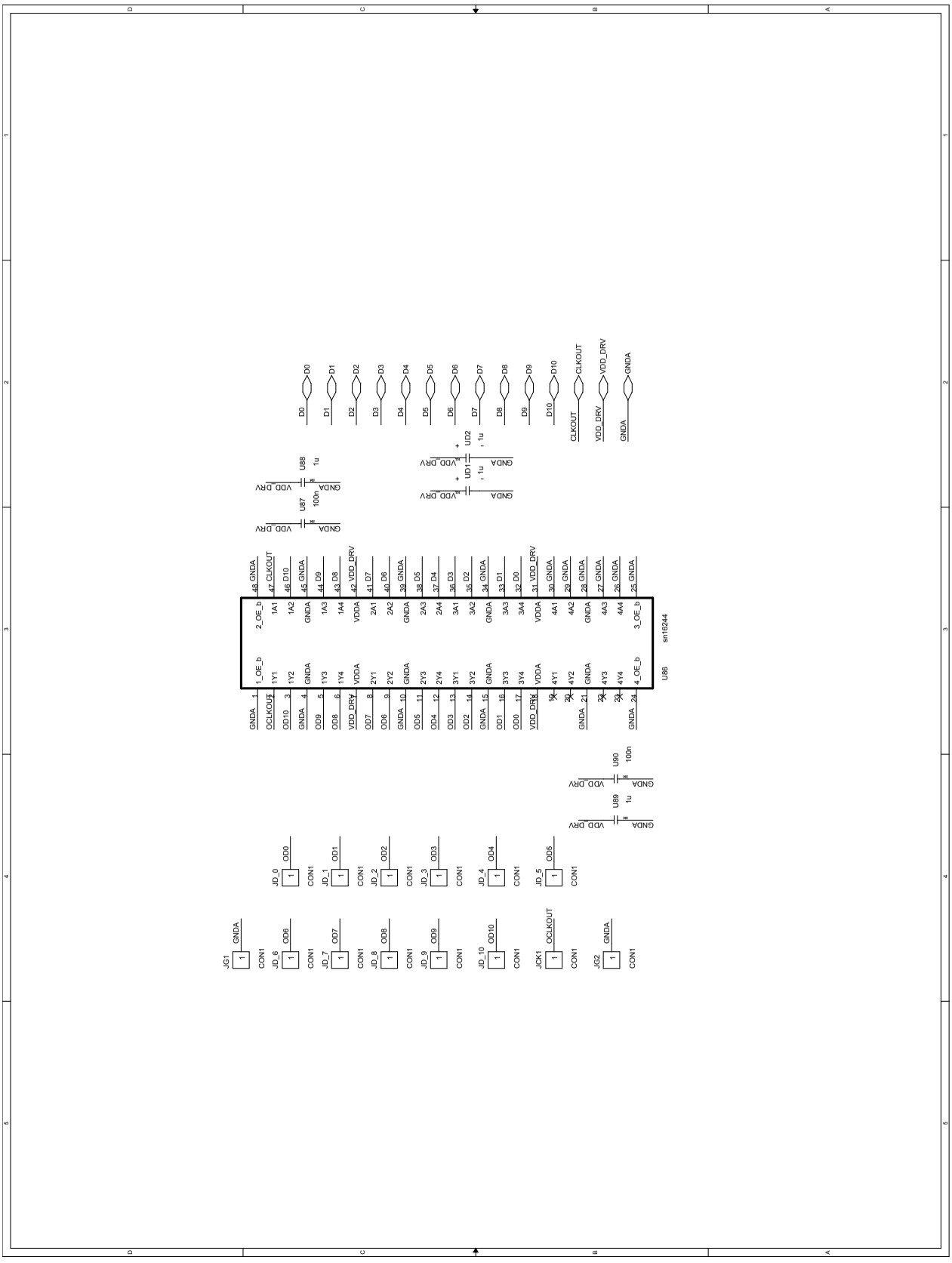


Figure A.5: Digital Buffer schematic

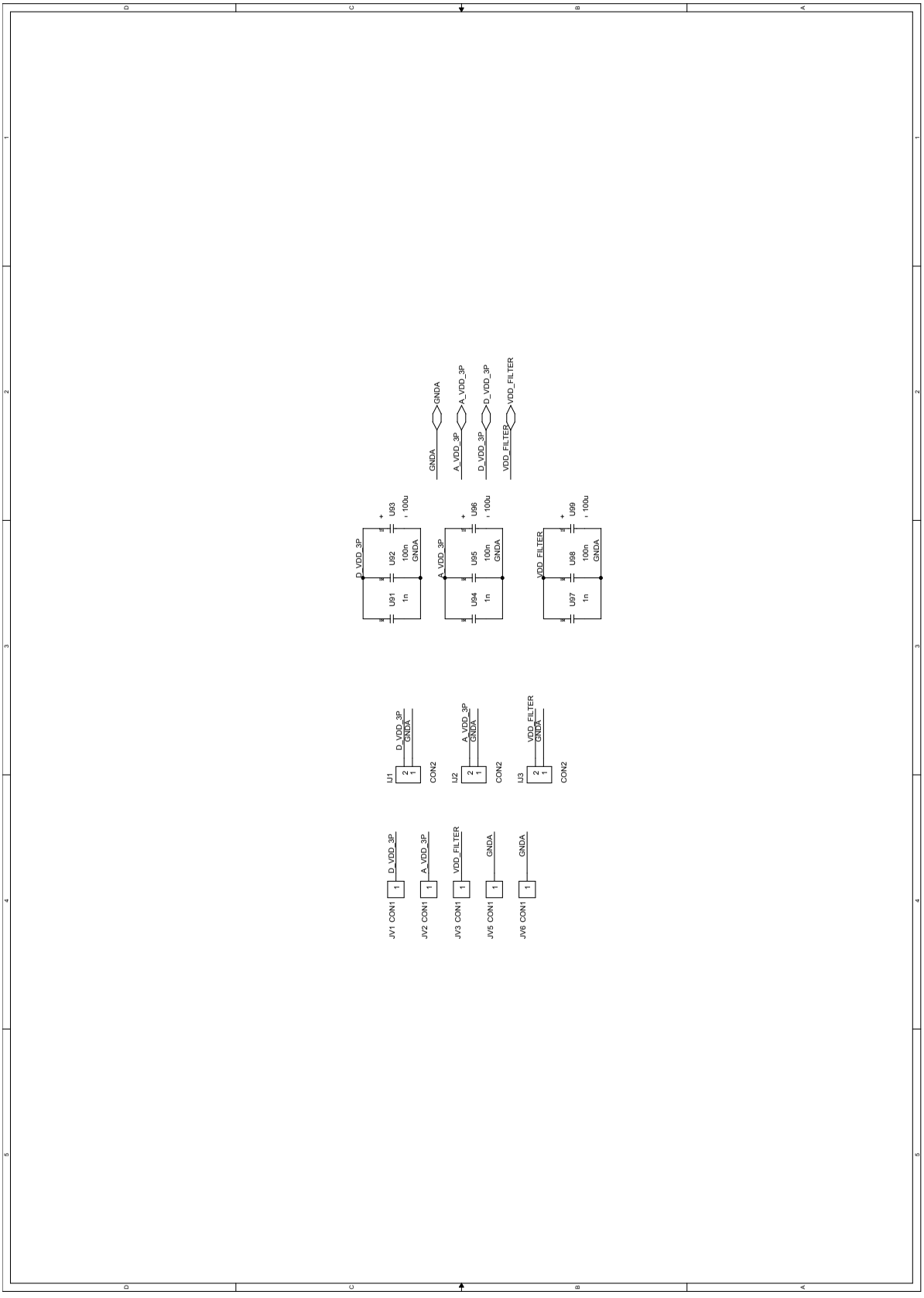


Figure A.6: Supply input & Bypass capacitors schematic

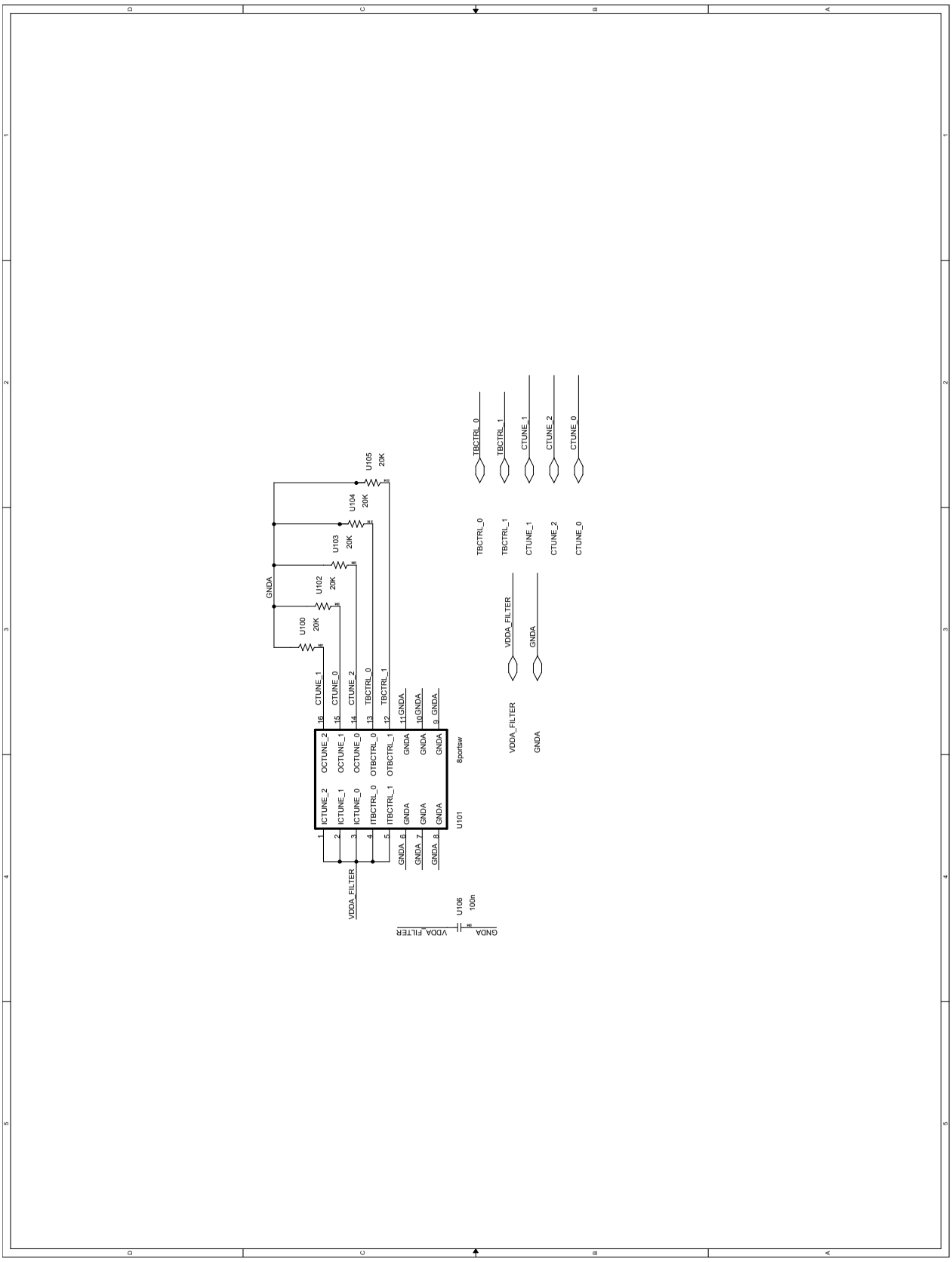


Figure A.7: Test logic schematic

REFERENCES

1. **AN2085** (2003). http://www.maxim-ic.com/appnotes.cfm/an_pk/2085.

2. **AN748** (2001). http://www.maxim-ic.com/appnotes.cfm/appnote_number/748/.

3. **Black, W.** and **D. Hodges** (1980). Time Interleaved Converter Arrays. *IEEE Journal of Solid-State Circuits*, **15**(6), 1022–1029.

4. **Bult, K.** and **G. Geelen** (1990). A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. *IEEE Journal of Solid-State Circuits*, **25**(6), 1379–1384.

5. **Cho, T.**, **D. Cline**, **C. Conroy**, and **P. Gray** (1994). Design considerations for low-power, high-speed CMOS analog-to-digital converters. *IEEE Symposium on Low Power Electronics*, 70–73.

6. **Cho, T.** and **P. Gray** (1995). A 10 b, 20 Msample/s, 35 mW pipeline A/D converter. *IEEE Journal of Solid-State Circuits*, **30**(3), 166–172.

7. **Choksi, O.** and **L. Carley** (2003). Analysis of switched-capacitor common-mode feedback circuit. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **50**(12), 906–917.

8. **Doernberg, J.**, **H. Lee**, and **D. Hodges** (1984). Full-speed testing of A/D converters. *IEEE Journal of Solid-State Circuits*, **19**(6), 820–827.

9. **Kurosawa, N.**, **H. Kobayashi**, **K. Maruyama**, **H. Sugawara**, and **K. Kobayashi** (2001). Explicit analysis of channel mismatch effects in time-interleaved ADC systems. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **48**(3), 261–271.

10. **Kuyel, T.** and **H. Bilhan** (1999). Relating Linearity Test Results to Design Flaws of Pipelined Analog to Digital Converters. *IEEE International Test Conference*, 772–779.

11. **Laxminidhi, T.** and **S. Pavan** (2007). Efficient design centering of high-frequency integrated continuous-time filters. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **54**(7), 1481–1488.

12. **Lewis, S. H.**, **H. S. Fetterman**, **G. F. Gross**, **R. Ramachandran**, and **T. R. Viswanathan** (1992). A 10b, 20 MSamples/s Analog-to-Digital Converter. *IEEE Journal of Solid-State Circuits*, **27**(3), 351–358.

13. **Nagaraj, K.**, **H. Fetterman**, **J. Anidjar**, **S. Lewis**, and **R. Renninger** (1997). A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers. *IEEE Journal of Solid-State Circuits*, **32**(3), 312–320.

14. **Nagaraj, K.**, **D. A. Martin**, **M. Wolfe**, **R. Chattopadhyay**, **S. Pavan**, **J. Cancio**, and **T. R. Viswanathan** (2000). A Dual-Mode 700-MSamples/s 6-bit 200-MSamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS Process. *IEEE Journal of Solid-State Circuits*, **35**(12), 1760–1768.

15. **Nakagome, Y.**, **H. Tanaka**, **K. Takeuchi**, **E. Kume**, **Y. Watanabe**, **T. Kaga**, **Y. Kawamoto**, **F. Murai**, **R. Izawa**, **D. Hisamoto**, *et al.* (1991). An experimental 1.5-V 64-Mb DRAM. *IEEE Journal of Solid-State Circuits*, **26**(4), 465–472.

16. **Pavan, S.** and **T. Laxminidhi** (2006). A 70-500MHz Programmable CMOS Filter Compensated for MOS Nonquasistatic Effects. *Proceedings of the 32nd European Solid-State Circuits Conference*, 328–331.

17. **Pavan, S.** and **T. Laxminidhi** (2007). Accurate Characterization of Integrated Continuous-Time Filters. *IEEE Journal of Solid-State Circuits*, **42**(8), 1758–1766.

18. **Petraglia, A.** and **S. Mitra** (1992). High-speed A/D conversion incorporating a QMF bank. *IEEE Transactions on Instrumentation and Measurement*, **41**(3), 427–431.

19. **Petrescu, T.**, **J. Oksman**, and **P. Duhamel** (2005). Synthesis of hybrid filter banks by global frequency domain least square solving. *IEEE International Symposium on Circuits and Systems, 2005*, 5565–5568.

20. **Razavi, B.** (2002). Design Of Analog CMOS Integrated Circuits. *Tata McGraw-Hill Edition*.

21. **Vaidyanathan, P.**, *Multirate systems and filter banks*. Prentice-Hall, Inc. Upper Saddle River, NJ, USA, 1993.

22. **Velazquez, S.**, **T. Nguyen**, and **S. Broadstone** (1998). Design of hybrid filter banks for analog/digital conversion. *IEEE Transactions on Signal Processing*, **46**(4), 956–967.

23. **Walden, R.** (1999). Analog-to-digital converter survey and analysis. *IEEE Journal on Selected Areas in Communications*, **17**(4), 539–550.

24. **Xia, B.**, **A. Valdes-Garcia**, and **E. Sanchez-Sinencio** (2006). A 10-bit 44-MS/s 20-mW configurable time-interleaved pipeline ADC for a dual-mode 802.11b / Bluetooth receiver. *IEEE Journal of Solid-State Circuits*, **41**(3), 530–539.