ACCURATE DESIGN AND CHARACTERIZATION OF HIGH FREQUENCY CONTINUOUS-TIME FILTERS

A THESIS

submitted by

LAXMINIDHI T.

for the award of the degree

of

DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

NOVEMBER 2007

This thesis is
dedicated to
my parents

Tonse Laxmikanta
and
Tonse Laxmidevi

THESIS CERTIFICATE

This is to certify that the thesis titled **ACCURATE DESIGN AND CHARACTERIZATION OF HIGH FREQUENCY CONTINUOUS-TIME FILTERS**, submitted by **Laxminidhi T.**, to the Indian Institute of Technology, Madras, for the award of the degree of **Doctor of Philosophy**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Y. Shanthi Pavan
Research Guide
Asst. Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date:

ACKNOWLEDGEMENTS

I would like to express sincere and heartfelt gratitude to my research advisor Dr. Shanthi Pavan. I thank him for the constant guidance and support he has provided throughout my research. I am inspired by his dedication to research and teaching. I also thank him for the time he spent in putting this thesis in the present form. Words are not enough to express my indebtedness to him, for all the guidance and support.

I am grateful to the heads of the EE department. I thank Prof. Venkatasheshaiah, the head of the department (HoD) at the time of my enrollment to the Ph.D. Program; Prof. Srinivasan, the next HoD and Prof. Jagadeesh Kumar, the present HoD.

I thank Prof. K. Radhakrishna Rao, Professor (Retd.), EE department, IIT Madras. His short term course on Analog and Mixed Signal IC Design at IIT Madras inspired me to pursue my research in the field of analog integrated circuits. I admired his teaching style. Thanks to him for introducing me to Dr. Shanthi Pavan.

I am grateful to the Directors of my parent intitution National Institute of Technology Karnataka (NITK), Surathkal, for deputing me to carry my research through the Quality Improvement Program (QIP).

My heartfelt thanks to the heads of the E&C department, NITK surathkal: Prof. Subbanna Bhat, for forwarding my application, Prof. Sumam David, the next HoD and Prof. Shankarananda, the present HoD for their support. I also take this opportunity to thank all the faculty and staff of E&C department, NITK surathkal.

I am indebted to Mr. Girish Navada and Mr. Annappa, faculty at NITK for standing as surety for the bond I executed at NITK. I thank them whole heartedly for accepting to be the surety, with no hesitation.

I am thankful to the members of the doctoral committee - Prof. Vinita Vasudevan, Dr. Anil Prabhakar from the EE department, Prof. T.S. Natarajan from the Physics department and Dr. Manu Santhanam from the Civil department, for their comments and suggestions.

My thanks are also to the co-ordinator (QIP), IIT Madras for the support extended for my stay at IIT Madras. I thank Mr. Thomas for all the help he rendered in the QIP office with a friendly behaviour.

I also thank the staff in the Academic Section, Administration Section and Estate Section of IIT Madras as well as the Administrative staff of NITK Surathkal.

I would like to thank the supporting staff of the lab Mrs. Janaki and Mrs. Sumathi. I also thank the office staff, in the EE department for their help in the office related matters.

I thank Mr. Prabakar Rao and Mr. Jayachandran for lending the Spectrum Analyzer for testing the fabricated chips. My thanks are also to Mr. Rohit and Ms. Chella for lending me the RF amplifiers and populating the printed circuit board with surface-mount components respectively.

I acknowledge National Semiconductors, Bangalore for providing their lab facility to test the robustness of the fabricated filter chip under varying temperature.

I thank all my friends in the TI lab where I carried my research for the last three and a half year - V.V. Srinivas, Reddy Karthikeyan, Saravanan, T.Tajesh, Mohan, I.Rajesh, Murali, Prabhu Sankar, Ramalingam, M.N.V. Prasadu, Nanda Govind, Chembian. Special thanks to V.V. Srinivas for solving the CAD related problems and clearing the design doubts in the initial days at TI Lab; I.Rajesh giving the precious time of him to correct the first draft of my papers and for giving me company in exploring the Non-veg hotels at Chennai; Reddy and Murali for all the fun and discussion in and out the lab; M.N.V. Prasadu for all the discussion related to the design of active-RC filter.

My thanks to Mr. Somashekhara Bhat, Mr. Jayadeva, Mr. Rameshaiah, Mr. Jaibir Sharma and their family for making the campus life lively.

I take this opportunity to express my gratitude to my sister Laxmiprabha and brother-in-law Mr. Chetan for their support. I also thank my in-laws Mr. Aithappa and Mrs. Rohini for their blessings throughout the research. Thanks to Sachin, and all relatives and friends for their support.

My wife Savitha has been beside me in course of my research and supported me in all respects. Thanks to her for sharing all my happiness and sorrows I had in the course of my research. Thanks to my son Gagandeep, whose innocent actions were the source of relief from all the tensions (but of-course sometimes he was a tension creator).

My parents, Tonse Laxmikanta and Tonse Laxmidevi, have been the pillars of support for what I am today. The constant advice from my father right from my school days till date, though not related to any technical matters, helped me in each and every aspect of the life. My mother, who is a teacher by profession, is the source of inspiration for me to be in teaching profession. Thanks to her mathematics classes that laid the foundation in me. I am in short of words for the scarfices they have made in their life to make my life smoother. The best way to express my gratitude is to dedicate this thesis to them.

(Laxminidhi T.)

ABSTRACT

KEYWORDS: Continuous-time filters; Design centering; Non-quasi-static effects; Characterization; Active-RC filters; Constant-C scaling.

This research addresses some of the issues in the design and characterization of widely programmable high frequency continuous-time filters. An optimization technique known as “space-mapping” is applied to efficiently design center the high frequency continuous time filters. A graphical intuition is given for the design centering scheme adopted to the filter. The results are shown for a fifth order transconductor-capacitor ladder filter having wide programmability of bandwidth from 71.4-500 MHz.

An analysis on the influence of non-quasi-static (NQS) effects of MOS transistors on the performance of high frequency transconductor-capacitor filters is presented. A simple technique to compensate for these effects is proposed.

The thesis also presents efficient techniques to accurately characterize the frequency response and noise spectral density of continuous-time filters by de-embedding the package and test-setup characteristics. One technique uses a vector network analyzer for the measurements and the other uses a spectrum analyzer.

A 71.4-500 MHz fifth order Gm-C Chebyshev ladder filter designed in a 0.35 μm CMOS process is used as a test-vehicle to validate the techniques presented in this thesis. The proposed NQS compensation scheme is found to be effective in compensat-

ing the MOS NQS effects. The proposed frequency response measurement techniques, when compared to the conventional techniques, show a significantly enhanced measurement accuracy in the stopband while being less sensitive to package characteristics. The filter has a dynamic range of 52 dB for 1% THD and consumes a power of 100 mW while operating with a 3.3 V supply.

A constant-C scaled active-RC integrator is proposed and used as a building block in a 44-300 MHz fifth order active-RC Chebyshev ladder filter designed in a 0.18 μm CMOS process. Through the results of the fabricated integrated circuit, it is shown that the consant-C scaling applied to active-RC filter, allows to realize widely programmable high frequency active-RC filters while maintaining the frequency response shape across the tuning range.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS **i**

ABSTRACT **iii**

LIST OF TABLES **ix**

LIST OF FIGURES **xv**

ABBREVIATIONS **xvi**

NOTATION **xvii**

CHAPTER 1 INTRODUCTION **1**

1.1 MOTIVATION 1

1.2 PRIOR WORK 4

1.3 ORGANIZATION OF THE THESIS 6

CHAPTER 2 DESIGN OF A WIDELY PROGRAMMABLE TRANSCONDUCTOR-CAPACITOR FILTER **8**

2.1 FILTER ARCHITECTURE 9

2.1.1 LC Ladder 9

2.1.2 Leapfrog Implementation 10

2.1.3 Node Scaling The Filter 11

2.2 CONSTANT-C SCALED TRANSCONDUCTOR 14

2.3 COMMON-MODE FEEDBACK CIRCUIT 17

2.4 FIXED TRANSCONDUCTANCE BIAS GENERATION 19

2.5 BIAS DISTRIBUTION SYSTEM 22

2.6 INTEGRATING CAPACITORS 25

2.7 FILTER LAYOUT 26

2.7.1 Programmable Transconductor 26

2.7.2 Filter Layout 28

CHAPTER 3 FILTER DESIGN CENTERING 32

3.1 THE NEED FOR DESIGN CENTERING IN INTEGRATED ANALOG FILTERS 32

3.2 PREVALENT METHODS 34

3.2.1 Brute-Force Tweaking 34

3.2.2 Using a Circuit Optimizer 35

3.3 SPACE MAPPING : AN OVERVIEW IN THE CONTEXT OF FILTER DESIGN 36

3.3.1 Graphical Example 38

3.3.2 Generalization to a practical filter 41

3.4 SPACE-MAPPING APPLIED TO THE 71.4-500 MHz FIFTH ORDER Gm-C LADDER FILTER OF CHAPTER 2 42

3.4.1 Transconductor Nonidealities 42

3.4.2 Model 43

3.4.3 Design Centering 44

CHAPTER 4 ANALYSIS AND COMPENSATION OF MOS NON-QUASI-STATIC EFFECTS IN HIGH FREQUENCY TRANSCONDUCTOR–CAPACITOR FILTERS 48

4.1 INFLUENCE OF NQS EFFECTS ON CONSTANT-C SCALED Gm-C FILTERS 50

4.1.1 A Simple QS Model for the Programmable Transconductor . 50

4.1.2 A Complete QS Model for the Programmable Transconductor 52

4.1.3 Non-quasi-static model for the programmable transconductor 57

4.2 COMPENSATING FOR MOS NQS EFFECTS - A BIQUAD EXAMPLE 63

4.2.1 Biquad - Compensating for NQS effects 65

4.3 SIMULATION RESULTS 69

CHAPTER 5 ACCURATE CHARACTERIZATION OF ON-CHIP INTEGRATED FILTERS 71

5.1 LIMITATIONS OF THE CONVENTIONAL MEASUREMENT TECHNIQUE 75

5.2 PROPOSED MEASUREMENT TECHNIQUES 79
5.2.1 Method - 1 : Using a Vector Network Analyzer (VNA) . . . 79
5.2.2 Method - 2 : Using a Spectrum Analyzer 82
5.3 A MODIFIED TEST-SETUP FOR THE PROPOSED MEASUREMENT TECHNIQUES 86
5.4 MEASUREMENT OF NOISE SPECTRAL DENSITY 87
5.4.1 Measurement of $|H_{b1}|$ 90
5.5 SIMULATION RESULTS 92

CHAPTER 6 EXPERIMENTAL RESULTS 94
6.1 DESIGN OF THE TEST BOARD 94
6.2 RESULTS ON NQS EFFECTS AND ITS COMPENSATION . . . 97
6.3 RESULTS ON PROPOSED CHARACTERIZATION SCHEMES . 100
6.3.1 Frequency Response Measurement Using a VNA 100
6.3.2 Frequency Response Measurement Using Spectrum Analyzer Method 103
6.3.3 Noise Spectral Density Measurement 104
6.4 DISTORTION MEASUREMENT 105

CHAPTER 7 CONSTANT-C SCALED ACTIVE-RC FILTERS 109
7.1 CONSTANT-C SCALED ACTIVE-RC INTEGRATORS 111
7.1.1 Programmable OTA 112
7.1.2 Programmable Integrating Resistor (R_{int}) 113
7.1.3 Programmable Zero-Compensating Resistor (R_z) 115
7.2 DESIGN OF A FIFTH ORDER ACTIVE-RC LADDER FILTER . 116
7.2.1 Common-Mode Feedback circuit 118
7.2.2 Resistor Servo Circuit 121
7.2.3 Test Buffers 122
7.3 SIMULATION RESULTS 125
7.4 EXPERIMENTAL RESULTS 126

CHAPTER 8 CONCLUSIONS AND FUTURE DIRECTIONS 133
8.1 FUTURE DIRECTIONS 134

CHAPTER A EFFECT OF THE PARASITIC POLE OF A TRANSCONDUCTOR ON ω_o AND Q OF A Gm-C BIQUAD 135

CHAPTER B PIN DETAILS OF THE Gm-C FILTER CHIP 137

CHAPTER C LM334 BASED CURRENT SOURCE/SINK 139

CHAPTER D PIN DETAILS OF THE ACTIVE-RC FILTER CHIP 141

LIST OF TABLES

4.1 Example for the strategy to find ΔC to compensate for the MOS NQS effects. 67

5.1 Mutual coupling between the bondwire inductances used for the simulation 92

6.1 Summary of measurement results 108

7.1 Choices for implementing the unit resistor 113

7.2 Summary of measurement results of active-RC filter chip 130

7.3 Comparison with some of the published filters 132

B.1 Functionality of pins of Gm-C filter chip 138

C.1 Jumper settings 140

D.1 Functionality of pins of the active-RC filter chip 142

LIST OF FIGURES

1.1 Simplified block diagram of a hard-disk drive read channel. 1

2.1 Block diagram of the test-chip 8

2.2 Prototype LC ladder with (a) 1 Ω termination and a band-edge of 1 rad/sec (b) 250 Ω termination and a band-edge of 500 MHz. 9

2.3 (a) Floating inductor to be realized. (b) Gyrator-capacitor based realization of floating inductor. 10

2.4 Realizing source-end terminating resistor (R) using transconductors of value G=1/R. 11

2.5 Gm-C implementation of the LC ladder shown in Figure 2.2(b). . . . 11

2.6 Frequency response at each integrating node - before node scaling. . 12

2.7 Schematic of a node scaled filter. 13

2.8 Frequency response at each integrating node - after node scaling. . . 13

2.9 3-bit digitally programmable transconductor realized using constant-C scaled unit transconductors. 15

2.10 Unit constant-C Gm-Cell. 16

2.11 Common mode feedback circuit. 18

2.12 Fixed transconductance bias generation circuit. 19

2.13 Schematic of the complete fixed-Gm bias circuit used in this work. . 21

2.14 (a) and (b) Conventional bias distribution schemes. 22

2.15 Proposed bias distribution technique with the advantages of schemes shown in Figure 2.14. 24

2.16 (a) Schematic of the unit transconductor g_m (b) Floorplan of the programmable transconductor (G_m) layout. 26

2.17 Demonstration of area efficient layout - (a) Schematic to be laid out (b) Simple layout, where M5 and Ms3 are laid separately (c) Layout with fingers of M5 and Ms3 merged together (d) Optimized layout, with unnecessary contacts removed. 27

2.18 (a) Scheme of filter layout (b) Fully differential schematic of the filter. 29

2.19 Screen-shot of completely laid filter 30

3.1 Ideal and nonideal Gm-C integrators. 33

3.2 Space mapping : the model design space is offset from the filter design space. (a) The filter, with the explicit capacitance, as well as a parasitic C_p. (b) The model (c) Step 1 - finding $F(C_1)$, (d) Step 2 - finding $M^{-1}(F(C_1))$, (e) Step 3 - finding $M^{-1}(B_{des})$, (f) Step 4 - finding C_{des}. 38

3.3 Space mapping when the model space is not just a translated version of the filter space : (a) & (b) - first iteration, (c) & (d) second iteration. . 40

3.4 Small signal model of the digitally programmable transconductor. k is the bandwidth programming code, settable between 1-7. 42

3.5 Design centering : comparison of $F(\mathbf{C}_1)$ and H_{des}. 45

3.6 The actual and desired responses match after one iteration. 46

3.7 Passband detail of Figure 3.6. 46

4.1 (a) Simplified single-ended schematic of the integrator used by Shi *et al.* (1986) (b) Distributed RC small signal model of the transistor M1 and (c) First order approximation for (b). R_T and C_T are the total channel resistance and capacitance respectively 49

4.2 Programmable transconductor (a) Unit g_m-cell and (b) Realization of programmable Gm using unit g_m-cells. 50

4.3 A simple quasi-static small signal model of a MOSFET operating in saturation 51

4.4 A simple quasi-static small signal model of the programmable transconductor of Figure 4.2. N is the number of unit cells per transconductor and k is an integer that sets the filer bandwidth ($1 \leq k \leq N$). 51

4.5 Complete QS small signal model of a MOSFET operating in saturation 53

4.6 Intrinsic small signal model of the programmable transconductor. A complete QS model is assumed for the transistors 53

4.7 Evaluation of (a) $TF_i(j\omega)$ and (b)$TF_{nqs}(j\omega)$ of a fifth order all-pole filter 55

4.8 A 3-D plot illustrating the Q-enhancement in the filter when the QS model is considered 56

4.9 An intrinsic small signal model of a MOSFET operating in saturation with bulk and source terminals at the same potential, valid for high frequencies 57

4.10 The intrinsic model of the programmable transconductor considering NQS effects 58

4.11 Effect of R_{gs} and L_{ds} in the NQS model of the transistor on the magnitude response of the fifth order Chebyshev ladder filter. The complete NQS model includes the effect of R_{gs} and L_{ds} in addition to the pole in transconductance, while in the simplified model R_{gs} and L_{ds} are neglected. 59

4.12 Shift in the $j\omega$-axis due to the QS behaviour and the NQS behaviour of transconductors 60

4.13 Comparison of the magnitude responses of the fifth order Chebyshev ladder filter model considering the complete QS model and NQS model for the programmable transconductor. 61

4.14 Passband detail of Figure 4.13 61

4.15 Stopband detail of Figure 4.13 plotted up to 10 GHz 62

4.16 Magnitude response of the filter model across the bandwidth settings when NQS effects are considered - Passband details 62

4.17 Simplified schematic of an integrator incorporating MOS NQS effects. 63

4.18 Gm-C biquad 64

4.19 Gm-C biquad: compensating strategy 66

4.20 (a) Unit NMOS capacitor used for the ΔC (b) C-V curve of the unit NMOS capacitor in (a), showing the operating regions 66

4.21 Normalized magnitude response of the layout-extracted filter without NQS compensation. 70

4.22 Normalized magnitude response of the layout-extracted filter with NQS compensation. 70

5.1 Conventional on-chip filter measurement test setup. 71

5.2 Signal flow graph of the conventional test setup. 73

5.3 Isolation of the filter path with and without the packaged IC. 76

5.4 Isolation of the direct path with and without the packaged IC. 76

5.5 Isolation between the output ports with and without the packaged IC. 77

5.6 Signal flow graph with finite package isolation. 77

5.7 On-chip portion of proposed technique. 79

5.8 Simplified schematic of the test buffer and polarity reversal switches. 82

5.9 Signal flow graph of the setup with gain control. 83

5.10 Simplified schematic of the test buffer with variable gain and constant bandwidth. 85

5.11 On-chip portion of improvement to the proposed technique. 86

5.12 Signal flow graph for the improved method when (a) TB2 is on (filter path measurement) and (b) TB1 is on (direct path measurement). . . 87

5.13 (a) & (b) Test setup for the measurement of noise spectral density of the filter. (c) Block diagram of the test setup. 88

5.14 Test setup for finding H_{b1} 90

5.15 Schematic of the test bench used for validating the proposed measurement technique. The mutual inductance used for the test-setup is given in Table 5.1 92

5.16 Simulation results for the proposed measurement technique using a VNA 93

6.1 Chip die photograph. 95

6.2 Bonding Diagram 95

6.3 Snap-shot of the populated PCB 96

6.4 Magnitude response of the filter without correcting for NQS effects. 97

6.5 Magnitude response of the filter with NQS compensation. 98

6.6 Comparison of the frequency response of 20 chips measured under identical conditions, with and without NQS compensation. In both cases, the filter is set to the highest bandwidth. 98

6.7 Measured filter response is compared with that of the simulated filter considering the channel resistance of MOS capacitors and interconnect resistances, for the NQS uncompensated and the NQS compensated filters. The responses are plotted for both the highest and the lowest bandwidth settings. 99

6.8 Measured frequency response variation with ambient temperature. . 99

6.9 Comparison of the responses obtained for the conventional technique and proposed VNA based method. The inset shows the passband detail - the responses measured using the conventional and proposed techniques are virtually identical, since package isolation is high in the filter passband. Notice that the stopband attenuation measured using the proposed technique is less sensitive to package variations. 101

6.10 Photograph of the package A and B used for investigating the sensitivity of the proposed measurement technique. Package A is a 40 pin DIP and Package B is the same 40 pin DIP but with a copper strip pasted on it. 102

6.11 Magnitude responses measured using the conventional method and proposed spectral analyzer method. 103

6.12 Measured and simulated output noise spectral density of the filter for the lowest bandwidth setting. 104

6.13 Measured output noise spectral density of the filter when the filter bandwidth is tuned over its range. 105

6.14 Third harmonic distortion of the filter as a function of the input voltage. The filter is set to the lowest bandwidth and the test-tone is given at one-third of the filter band-edge. 106

6.15 Third harmonic distortion of the filter as a function of the input frequency for an input signal of 0.5 V peak-to-peak. The filter is set to the lowest bandwidth. 107

7.1 (a) The programmable integrator of Harrison and Weste (2003) and (b) single-ended block diagram of the OTA. 109

7.2 Schematic of constant-C scaled (a) active-RC integrator and (b) OTA. 111

7.3 (a) Unit constant-C Gm-Cell and (b) Binary weighting of unit cells to realize a 3-bit programmable constant-C transconductor. 112

7.4 Programmable integrating resistor 114

7.5 Programmable compensating resistor 115

7.6 Floor-plan of the test chip. 116

7.7 Single ended schematic of the filter - component values are for the highest bandwidth setting. 117

7.8 Fixed-Gm bias circuit 119

7.9 Current distribution circuit 120

7.10 Common-mode feedback circuit 121

7.11 Simplified schematic of the resistor servo loops. 121

7.12 Charge pump based battery generator 122

7.13 Schematic of the test buffer 123

7.14 Simulated filter response (a) without constant-C scaling, only R_{int} is varied to change bandwidth and (b) with constant-C scaled OTA, R_{int} and R_z. 125

7.15 Die photograph and top-level layout. 126

7.16 Photograph of the test board. 127

7.17 Measured frequency response across all bandwidth settings. 128

7.18 Passband detail for 15 chips at the highest and lowest bandwidth setting. 128

7.19 Measured IIP3 of the filter as a function of frequency for the lowest bandwidth setting 129

7.20 Measured noise spectral density of the filter 129

B.1 Pinout of the packaged chip 137

C.1 Basic current source using LM334 139
C.2 Schematic of the current source/sink circuit 140

D.1 Pinout of the packaged active-RC chip 141

ABBREVIATIONS

SoC	Systems-on-chip
THD	Total harmonic distortion
Gm-C	Transconductor-Capacitor
QS	Quasi-static
NQS	Non-quasi-static
VNA	Vector network ananlyzer
SA	Spectrum ananlyzer
DIP	Dual-in-line package
OTA	Operational transconductance amplifier
DR	Dynamic range

NOTATION

English symbols

C_{gb}	Gate-body intrinsic capacitance of the MOSFET
C_{gs}	Gate-source intrinsic capacitance of the MOSFET
C'_{ox}	Gate oxide capacitance per unit area
g_m	Small signal transconductance of the MOSFET
g_{ds}	Output small-signal conductance of the transistor
L	Channel length of the MOSFET
V_T	Threshold voltage of the MOSFET
V_{GS}	Gate-source voltage
W	Channel width of the MOSFET

Greek symbols

μ_o	Surface mobility of the channel charge

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

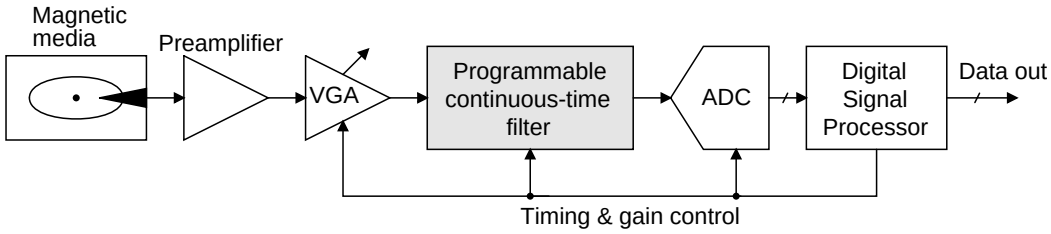


Figure 1.1: Simplified block diagram of a hard-disk drive read channel.

Widely programmable high frequency continuous-time (CT) filters are integral parts of systems-on-chip (SoC) like hard-disk drives and CD/DVD read channel electronics. A simplified block diagram the hard-disk drive read channel is shown in Figure 1.1 (Gopinathan *et al.* (1999)). The preamplifier and the Variable Gain Amplifier (VGA) amplify the signal from the magnetic storage media. The amplified signal is then filtered by a programmable continuous time filter. The Analog to Digital Converter (ADC) digitizes the filtered signal. The Digital Signal Processor (DSP) processes the digital signal further and does the data detection. The rate at which the data is read varies with the location from where it is being read on the disc, necessitating the programmability of the filter bandwidth. Higher data density increases the rate at which the data is read from the storage device. This calls for higher bandwidth of the filters. The focus of this thesis is on the programmable continuous time filters. The primary tasks of such filters are anti-aliasing and partial channel equalization.

Design centering such high frequency integrated filters is a challenging task. In this work, *design centering* means the following. It refers to the process of ensuring that the filter response *including the layout parasitics* is indeed the desired one. The prevailing methods of design centering are brute-force tweaking or the use of a circuit optimizer. In the former method, the designer tweaks the optimizing parameters (usually capacitor values) till the desired frequency response is achieved. This requires that the designer have good intuition about the filter building blocks, and becomes virtually impossible for complicated topologies like ladder filters.

Using a circuit optimizer requires minimal intervention of the designer. But this approach consumes inordinate amounts of time, since the optimizer has to compute the frequency response of the layout extracted netlist of the filter many times (1000 is not uncommon). Each computation of the frequency response is very time consuming (for example a frequency response evaluation of a filter presented in Chapter 2 takes 25 minutes). Thus there is a need for an efficient design centering technique that involves very few simulations of the complete layout extracted netlist. Surprisingly, this practical problem does not seem to have received the attention it deserves.

In CMOS technologies, the transconductor-capacitor (Gm-C) architecture is the one of choice for realizing very high frequency filters. In such filters, when the bandwidth becomes a significant fraction of the transition frequency (f_T) of the MOS transistors, the finite response time of the channel charges (non-quasi-static effects (NQS)) makes the transconductor slower, resulting in excess phase lag in the integrator. This leads to Q-enhancement of the filter. Since the excess phase lag is bandwidth dependent, the shape of the frequency response varies as the bandwidth of the filter is programmed.

Such variations are unacceptable in several practical applications. It is thus seen that low power and hardware efficient techniques to mitigate the effects of non-quasi-static behaviour are necessary.

Another challenging task associated with on-chip filters is the characterization of the fabricated prototypes. The difficulties associated with measurement are the following-

- Filters are part of an SoC and are not intended to drive package parasitics.
- The test procedure has to be as "non-invasive" of the main signal path as possible.
- Wafer probing techniques are not attractive, since these require additional probe pads on the chip, which occupy extra area and add large parasitics in the signal path.
- When the chip is packaged, the effects of the package must be de-embedded from the response of the filter.
- The usual "microwave" practice of having dedicated calibration structures (which must be on-chip) for de-embedding the package response is not practical due to space and pin-count considerations.

A commonly used technique that addresses several of the issues discussed above was proposed by Nauta (1992). Using this technique, the authors (and other researchers) have found that measurements made in the filter passband are generally accurate. However, the response in the stopband usually doesn't fall below 55-60 dB, and is very sensitive to the test setup. To date there seems to be no explanation as to why stopband measurements are erroneous. There is also a need to make accurate measurements of the stopband frequency response.

Another problem addressed in this work is the design of high performance programmable active-RC filters. It can be shown that active-RC filters are fundamentally more power efficient when compared to their Gm-C counterparts. However, such filters are mostly avoided in high frequency applications because of the difficulties in realizing

an opamp with adequate gain and bandwidth. These issues are exacerbated when the bandwidth has to be programmed over a wide range.

This thesis aims to solve the practical problems (described above) arising during the design and characterization of high frequency CMOS analog filters.

1.2 PRIOR WORK

The first integrated continuous-time filter was reported by Moulding and Wilson (1978). It was a Gm-C filter in bipolar technology for video applications, designed to replace bulky LC filters. Another Gm-C filter was reported by Voorman *et al.* (1982) for viewdata modems. This was also implemented in bipolar technology. Continuous-time filters for read-channel applications were reported in the early 90s (Khoury (1991), De Veirman and Yamasaki (1992), Alini *et al.* (1992)).

The filter presented by Khoury (1991) is a Gm-C filter with bandwidth tunable from 6-15 MHz, designed in a 0.9 μm CMOS process. The filter bandwidth was tuned using a voltage-controlled oscillator (VCO) based master-slave tuning circuit. De Veirman and Yamasaki (1992) presents a 2-10 MHz tunable bandwidth fifth order bipolar equiripple linear phase filter. It shows how a careful one-time frequency trim and use of DC current through an external precise resistor can avoid master-slave tuning in filters with moderate Q. The filter by Alini *et al.* (1992) was a second order Gm-C filter designed in a 2 μm BiCMOS process, with bandwidth tunability of 8-32 MHz. The emphasis was on the fully differential BiCMOS transconductor using a MOS transistor. The filter had a dynamic range of 72 dB for -40 dB total harmonic distortion (THD) at a supply voltage of 5 V.

Nauta (1992) reported a low-pass Gm-C filter tunable in the range of 22-98 MHz. He also described a technique to characterize packaged integrated filters. Gopinathan *et al.* (1999) presented a 30-100 MHz Gm-C filter in a 0.25 μm CMOS process. A variable gain amplifier (VGA) was embedded into the filter. Pavan *et al.* (2000) presented a Gm-C filter in a 0.25 μm CMOS process with bandwidth tunability from 60-350 MHz. They proposed the constant capacitance (constant-C) scaling technique for the transconductor, that makes the parasitic capacitances of the transconductor independent of the bandwidth setting. They showed that the constant-C technique avoids the severe linearity and noise trade-offs commonly encountered in realizing programmability. We make extensive use of this technique in this thesis. A 550 MHz Gm-C filter in a 0.35 μm CMOS process was reported by Panday *et al.* (2006). It did not incorporate any tuning. The achieved dynamic range is only 40 dB for a total harmonic distortion (THD) of -40 dB. Harrison and Weste (2002) presented a 350 MHz active-RC filter in a 0.18 μm CMOS process. They used a feed-forward compensation technique for the operational transconductance amplifier (OTA) making it suitable for high frequency filtering. Fundamentally the design is power efficient since it avoids the conventional Miller compensation. They also presented a 500 MHz active-RC filter in a 0.18 μm CMOS process (Harrison and Weste (2003)). It is seen in both these filters that the shape of the frequency response varies when the bandwidth of the filter is varied over its tuning range.

The filters in the references cited above constitute the state of the art in high frequency integrated filter design. Most of these are realized as a cascade-of-biquads, apparently due to the difficulty associated with design centering ladder filters, especially at high speeds.

Upon careful observation of the measured frequency responses in the above mentioned works, one sees that the rejection of filters in their stopband is poor - an effect attributed to the "quality of the test setup". Another aspect of the filters published in the literature is that most of them use Gm-C architecture. Active-RC filters have largely been avoided, inspite of their potential advantages.

1.3 ORGANIZATION OF THE THESIS

In this thesis, a fifth order Gm-C lowpass filter with a bandwidth digitally programmable from 71.4-500 MHz is used to validate the ideas proposed for design centering, compensation of NQS effects and accurate characterization. The proposed widely programmable active-RC filter technique is validated using a fifth order Chebyshev low-pass filter with a bandwidth programmable from 44-300 MHz.

The rest of the thesis is organized as follows - Chapter 2 explains the design and layout of the fifth order low-pass Gm-C Chebyshev ladder filter. The transistor level realization of each block of the filter is given in detail. Layout considerations are discussed.

Chapter 3 focusses on the difficulties faced by the designer while design centering the netlist extracted filter. A technique known as "space-mapping" is effectively adapted to optimize the filter. The chapter gives an overview of space-mapping in the context of filter design with graphical intuition.

Chapter 4 analyzes the influence of MOS non-quasi-static effects on the widely programmable Gm-C filters. A simple hardware efficient technique to compensate for NQS effects is proposed.

Chapter 5 is dedicated to the issue of characterizing high frequency filters. The chapter gives an overview of conventional techniques of measuring the frequency response and noise spectral density of on-chip continuous-time filters. The limitations of these methods when applied for high frequency filters are highlighted. Improved techniques are proposed with in-depth analysis.

Chapter 6 discusses the measurement results of the 71.4-500 MHz Gm-C filter designed in a 0.35 μm CMOS process. The efficacy of the techniques proposed in Chapters 3, 4 and 5 are borne out by the measurement results.

Chapter 7 deals with widely programmable active-RC filter design. An active-RC technique that maintains the shape of the filter frequency response when the bandwidth is programmed over a wide range is proposed. Experimental results from the ICs fabricated in a 0.18 μm CMOS process are given.

Chapter 8 gives the conclusions and suggestions for future work.

CHAPTER 2

DESIGN OF A WIDELY PROGRAMMABLE TRANSCONDUCTOR-CAPACITOR FILTER

To validate some of the ideas proposed in this research, a fifth order Gm-C low-pass Chebyshev ladder filter was designed in a 0.35 μm CMOS process. The filter bandwidth is digitally programmable from 71.4-500 MHz using a 3-bit control word. The pass-band ripple was chosen to be 1 dB. The filter is fully differential, as it has become routine to have fully differential circuits owing to their inherent advantages over their single ended counterparts. This chapter describes the design of filter and the supporting circuits. Figure 2.1 shows the block diagram of the filter test-chip. The design details of each block will be given in this chapter.

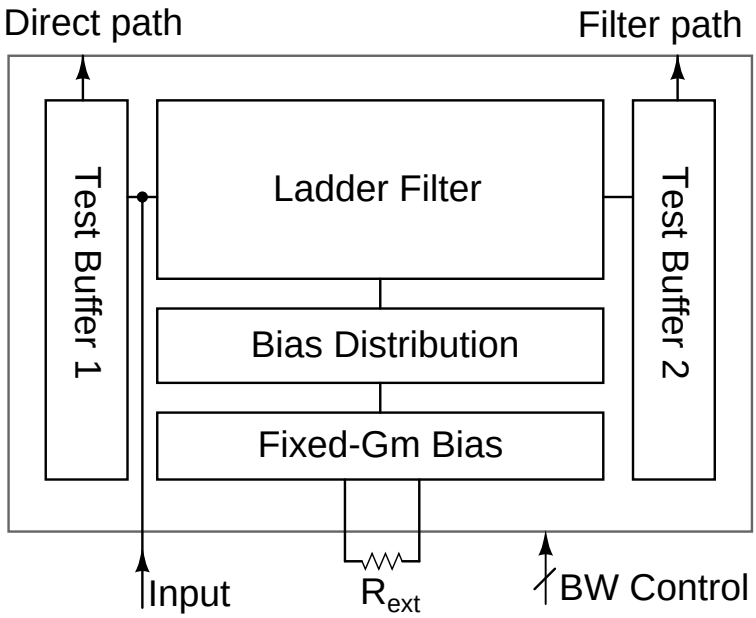


Figure 2.1: Block diagram of the test-chip

2.1 FILTER ARCHITECTURE

2.1.1 LC Ladder

The filter is realized as a singly terminated ladder. To start with the design, a prototype of the fifth order low-pass Chebyshev LC filter with pass-band ripple of 1 dB is taken. Figure 2.2(a) shows this prototype. The element values shown are for a 1 Ω terminating resistance and a band-edge of 1 rad/sec. The prototype is then scaled to realize a filter with a 250 Ω (conductance = 4 mS) terminating resistance and a band-edge of 500 MHz (the highest bandwidth to be realized). The scaled ladder is shown in Figure 2.2(b).

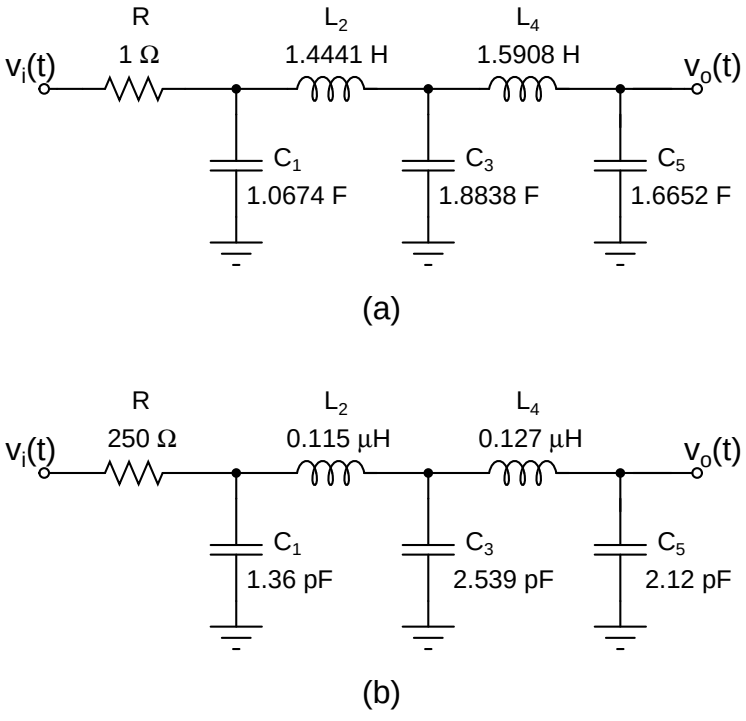


Figure 2.2: Prototype LC ladder with (a) 1 Ω termination and a band-edge of 1 rad/sec (b) 250 Ω termination and a band-edge of 500 MHz.

2.1.2 Leapfrog Implementation

To arrive at the Gm-C architecture, the inductors L_2 and L_4 of the ladder filter in Figure 2.2(b) are emulated using a gyrator-capacitor circuit. Though the concept is well known, realization of the floating inductor using a gyrator-capacitor circuit is shown in Figure 2.3(b).

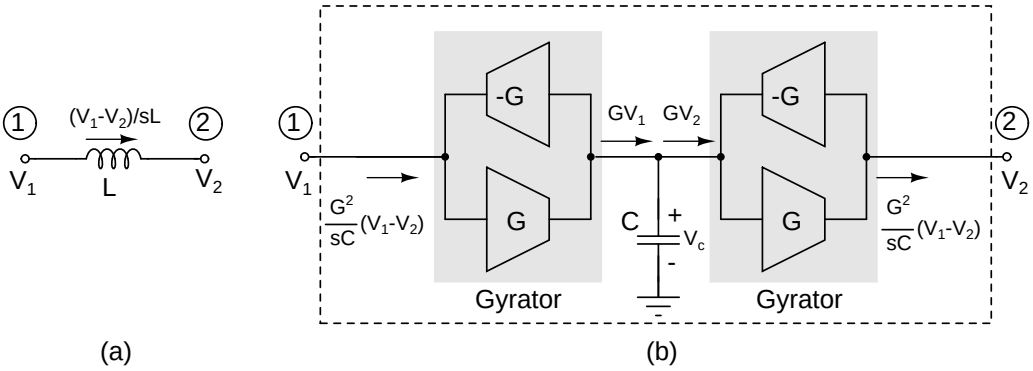


Figure 2.3: (a) Floating inductor to be realized. (b) Gyrator-capacitor based realization of floating inductor.

In Figure 2.3(b), the impedance seen between the nodes 1 and 2 (Z_{12}) is purely inductive and is given by -

$$Z_{12} = \frac{sC}{G^2} \tag{2.1}$$

Thus a grounded capacitor C is transformed to a floating inductor $L = \frac{C}{G^2}$.

The terminating resistor (R=250 Ω) at the source end is also realized using a transconductor of value G=1/R. A step-by-step realization is shown in Figure 2.4. Note that with this realization of R, the filter offers a high input impedance.

Replacing the resistors and inductors of the LC ladder with their equivalent Gm-C structures, one arrives at the active ladder filter as shown in Figure 2.5.

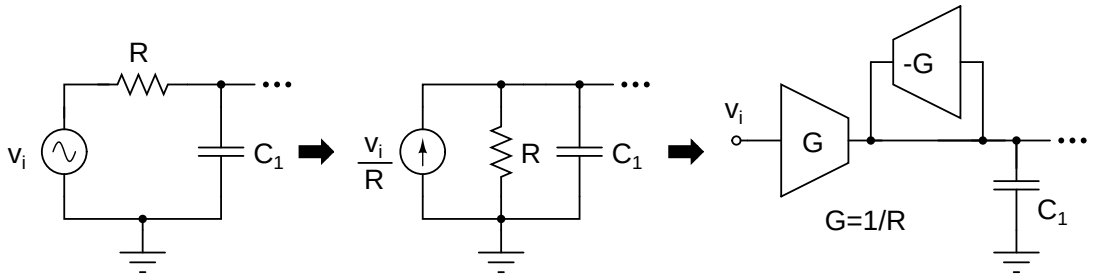


Figure 2.4: Realizing source-end terminating resistor (R) using transconductors of value G=1/R.

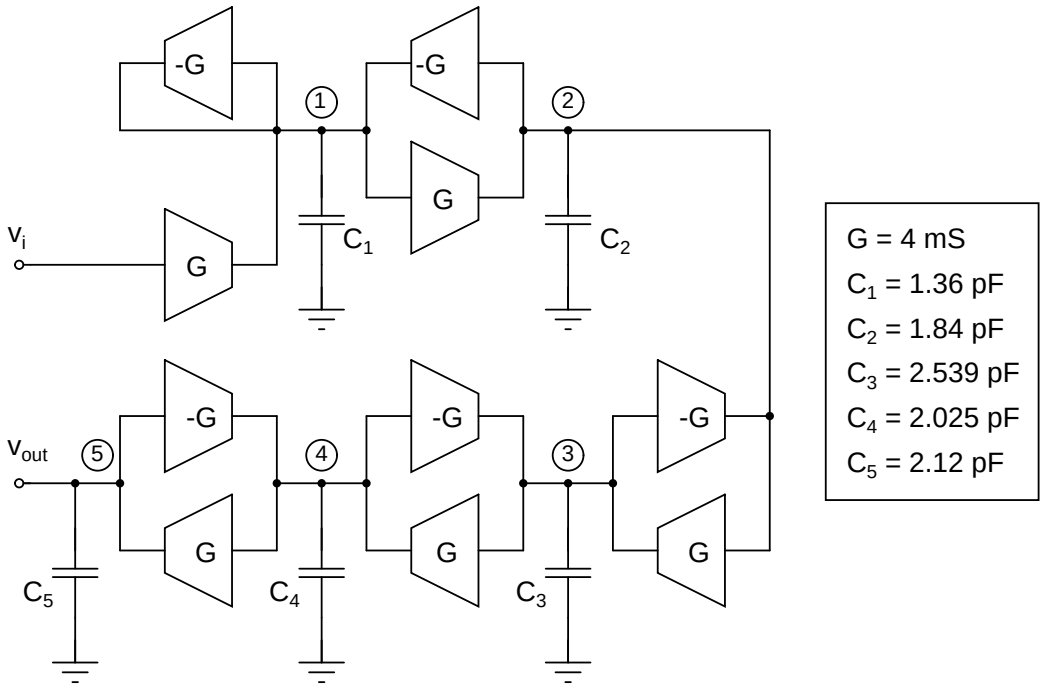


Figure 2.5: Gm-C implementation of the LC ladder shown in Figure 2.2(b).

2.1.3 Node Scaling The Filter

The voltage gain (as a function of frequency) at all the internal nodes (node-1 to node-5) of the filter of Figure 2.5 are plotted in Figure 2.6. It can be seen that the maximum swing at node-2 and 3 is about 50% more than that at the output (i.e. node-5) and at node-4, it is 60% more than the output. Therefore, the linearity of the filter is limited by the transconductors sensing the voltages at nodes 2, 3 and 4. To maximize the dynamic range, the maximum voltage gain at all the internal nodes must match that of the output. Therefore the nodes-2, 3 and 4 should be scaled down. The procedure of

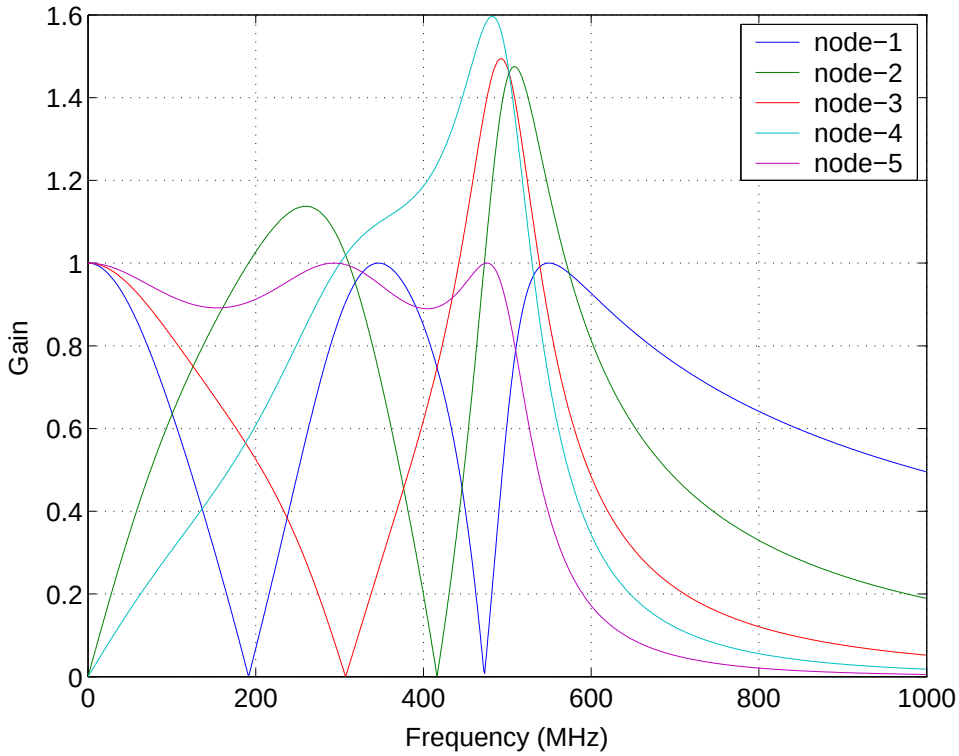


Figure 2.6: Frequency response at each integrating node - before node scaling.

"node scaling" the voltage at a given node by 'α' can be described as follows -

- Scale the integrating capacitor of that node, by $1/\alpha$.
- Scale all the transconductors sensing this node voltage by $1/\alpha$. This is done to keep the input-to-output transfer function unaltered.

On an integrated circuit, good matching can be achieved between the transconductors if the scaling of the transconductors is done in integer multiples. This also makes implementation easy as it can be done just by connecting the required number of transconductors in parallel. Hence, nodes 2, 3 and 4 have to be scaled down by a factor of two (rather than 1.5 or 1.6). The single-ended schematic of the filter, after node scaling, is shown in Figure 2.7 and the node scaled responses are shown in Figure 2.8.

Now that the top-level schematic of the filter is designed for the highest bandwidth, the next task is to achieve bandwidth programmability. With 3-bits for bandwidth programmability, the filter bandwidth can be set to 7 different values. With 500 MHz being

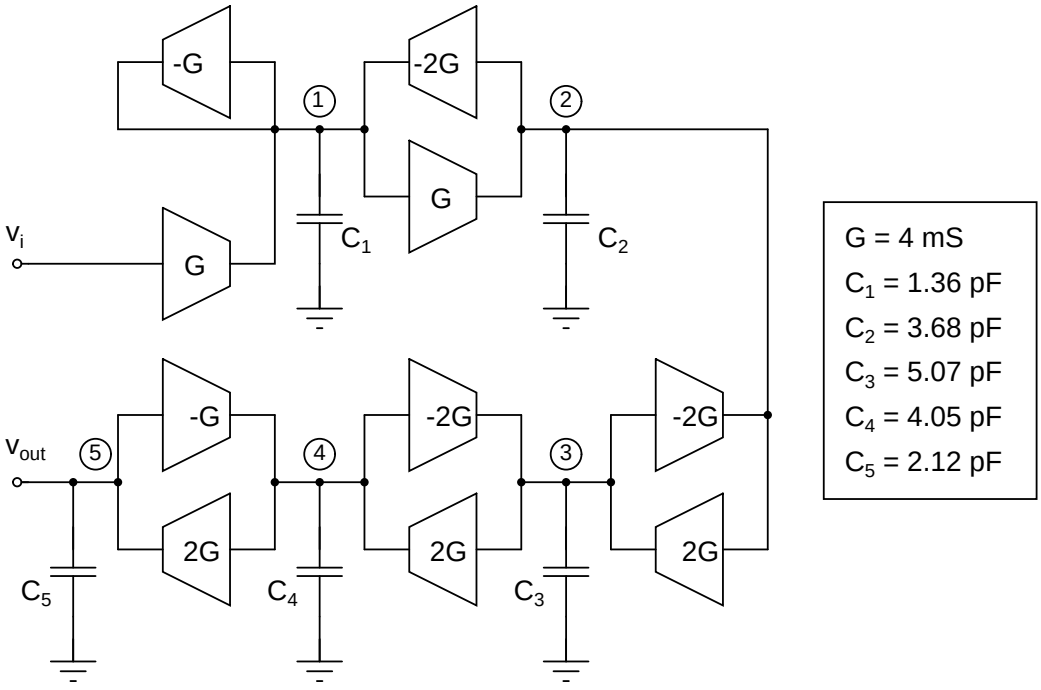


Figure 2.7: Schematic of a node scaled filter.

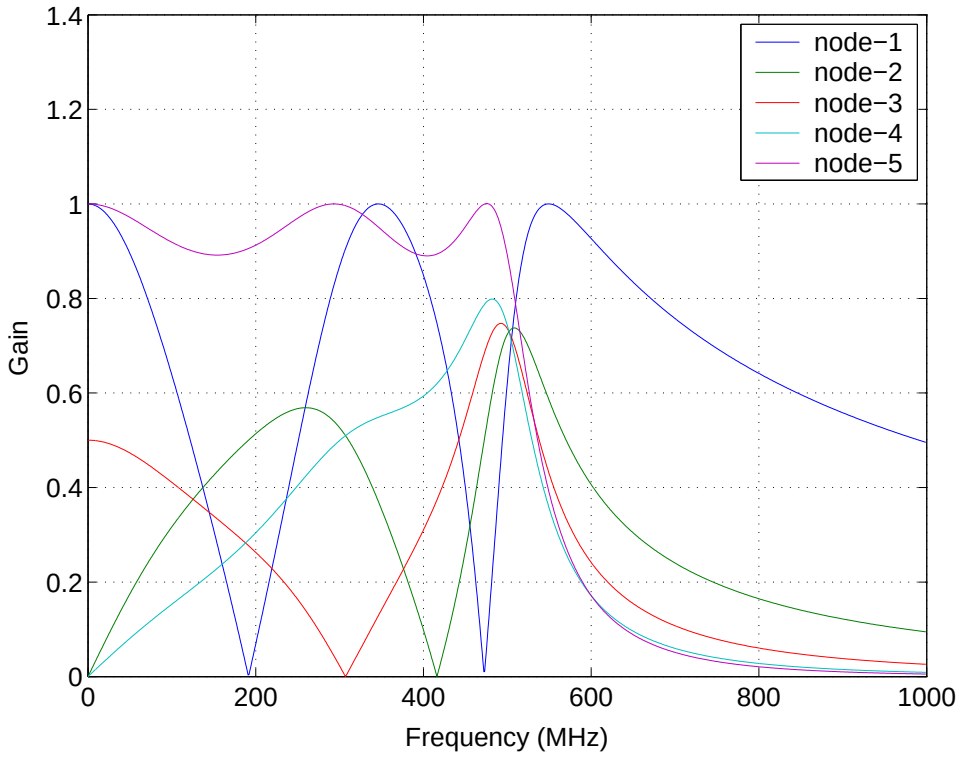


Figure 2.8: Frequency response at each integrating node - after node scaling.

the highest bandwidth, the lowest bandwidth would be 71.4 MHz (i.e. 500 MHz/7). Therefore the filter bandwidth should be programmable from 71.4 MHz to 500 MHz in

steps of 71.4 MHz.

Fundamentally, programmability can be achieved in one of the two ways viz.

1. Constant-Gm scaling: All capacitors are programmed while keeping all the transconductances/conductances constant.
2. Constant-C scaling: All the transconductances/conductances of the network are scaled with all capacitances kept constant.

The latter technique has been shown to be (Pavan *et al.* (2000)) an efficient technique for implementing programmable bandwidth filters, as it avoids severe linearity and noise trade-offs usually associated with realizing programmability. For a rigorous discussion on the advantages of constant-C scaling, the reader is referred to Pavan and Tsividis (2000).

With constant-C scaling being the choice, the transconductors of the filter have to be programmed. A practical transconductor has parasitic capacitances at both its input and output. As per the principle of constant-C scaling, *all* the transconductor parasitic capacitances must be kept constant when the transconductance is scaled. The next section describes the design of a constant-C scaled programmable transconductor.

2.2 CONSTANT-C SCALED TRANSCONDUCTOR

In the constant-C scaled programmable transconductor proposed by Pavan *et al.* (2000), the transconductor is programmed in a manner as to keep all parasitic capacitances constant irrespective of the transconductance being realized. A digitally programmable constant-C scaled transconductor is realized by connecting binary weighted transconductors in parallel. This work borrows the above idea to realize a 3-bit digitally programmable transconductor.

Figure 2.9 shows the way in which a 3-bit digitally programmable transconductor is realized using unit constant-C scaled transconductors. g_m is the transconductance. The binary weighted transconductances $2g_m$ and $4g_m$ are realized by connecting the required number of g_ms in parallel. $b_0 - b_2$ are the control bits. A '0' on these bits turn off the corresponding transconductor, where a '1' on these bits turns the transconductor on.

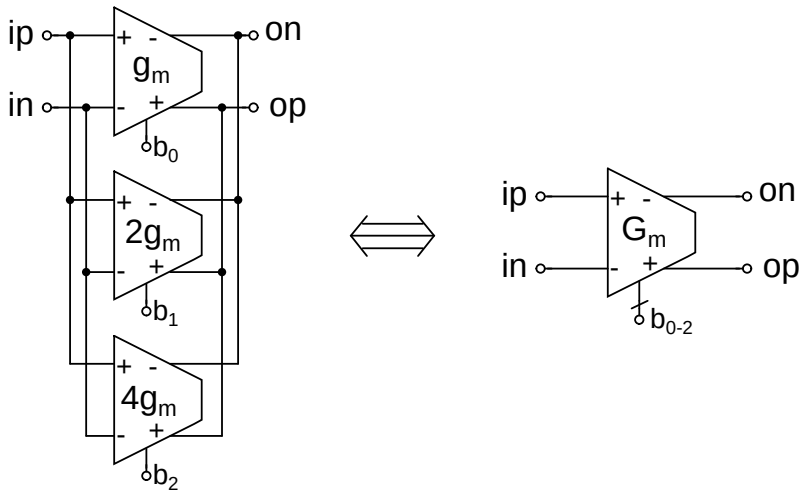


Figure 2.9: 3-bit digitally programmable transconductor realized using constant-C scaled unit transconductors.

The schematic of a unit constant-C transconductor is shown in Figure 2.10. M1 & M2 form the main differential pair. M5, Ms3, M6 & Ms4 form its tail current source. The PMOS loads are cascoded current sources formed by M9, M10, M11, M12, Ms1 & Ms2. M3 & M4 form the dummy differential pair, whose tail current source is formed by M7, M8, Ms5 & Ms6. The dummy differential pair is in parallel with the input of the main differential pair and its drains are connected to a voltage equal to the common-mode voltage. Ms1 through Ms6 are switches which turn the corresponding current sources "on" or "off". When the main differential pair is off, the dummy pair is switched on in order to keep the input capacitance of the transconductor a constant. Note that a

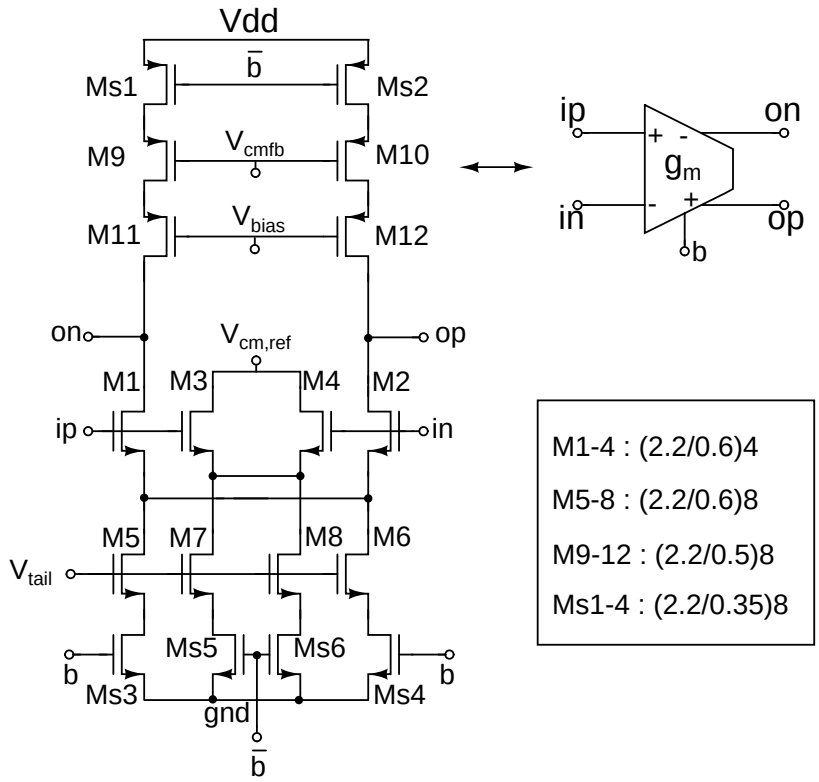


Figure 2.10: Unit constant-C Gm-Cell.

physical capacitor, rather than a differential pair could be switched in to save power (at the expense of robustness). Common-mode feedback (CMFB) is applied at the gates of M9 & M10.

The value of g_m needed for the unit transconductor is $\frac{4\,\mathrm{mS}}{7} = 571.4\,\mu\mathrm{S}$. Simulations show that a differential pair with transistor size $4\left(\frac{2.2\,\mu}{0.6\,\mu}\right)$ biased with a tail current of $230\,\mu$A has the required transconductance. This corresponds to a gate overdrive of $300\,$mV. The other transistors of the unit-cell are sized appropriately and sizes are shown in Figure 2.10, where the width (W) and length (L) given in the figure are in microns.

The bias V_{tail} for the tail current sources is derived from a fixed transconductance bias circuit that servos the transconductance of the differential pair to an off-chip stable resistor, thereby keeping the transconductance intact over process and temperature variations. The details of the fixed transconductance bias circuit and the bias distribution

scheme are given in sections 2.4 and 2.5 respectively.

The transconductor has a DC gain of about 100 and a unity gain frequency (with only the parasitics of the transconductor) of 4.7 GHz.

2.3 COMMON-MODE FEEDBACK CIRCUIT

The common-mode voltage at the output of each transconductor is servoed to an internally generated reference voltage ($V_{cm,ref}$). The schematic of the common-mode feedback system is shown in Figure 2.11. A PMOS differential pair formed by M1 and M2, whose input comes from the transconductor outputs is used as the common-mode detector. M4 forms the current source of the differential pair. The source coupled node of the differential pair senses the common-mode variations. Since the input impedance of this common-mode detector is capacitive, it can be absorbed into the integrating capacitors for design centering the filter. The detected common-mode is compared with the common-mode reference. The error is amplified using the NMOS error amplifier formed by M6-M10. M12 is a low output impedance source follower that drives the compensating capacitor Cc. Ms1 and Ms2 are the replicas of the switches Ms1 and Ms2 in Figure 2.10. The reference current (I_{bias}) is obtained from the bias distribution system. Note that one common-mode feedback circuit is needed to stabilize the common-mode level at each set of differential nodes. The filter, therefore, requires five common-mode feedback loops.

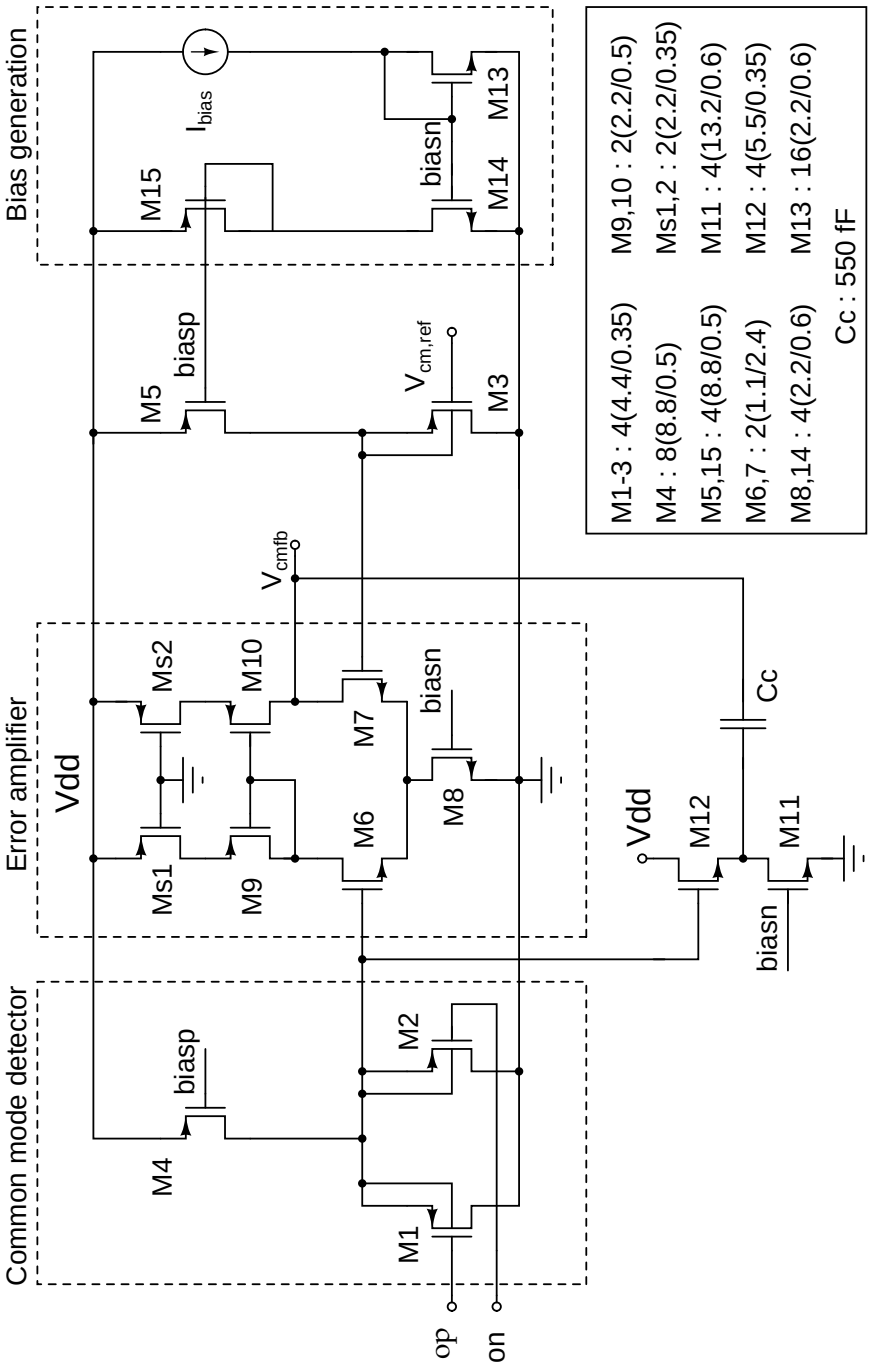


Figure 2.11: Common mode feedback circuit.

2.4 FIXED TRANSCONDUCTANCE BIAS GENERATION

A fixed transconductance bias generator that is robust with respect to supply voltage and ambient temperature is needed to stabilize the transconductances in the filter. Figure 2.12 shows the fixed transconductance bias generator employed in this design (Pavan (2004*a*)).

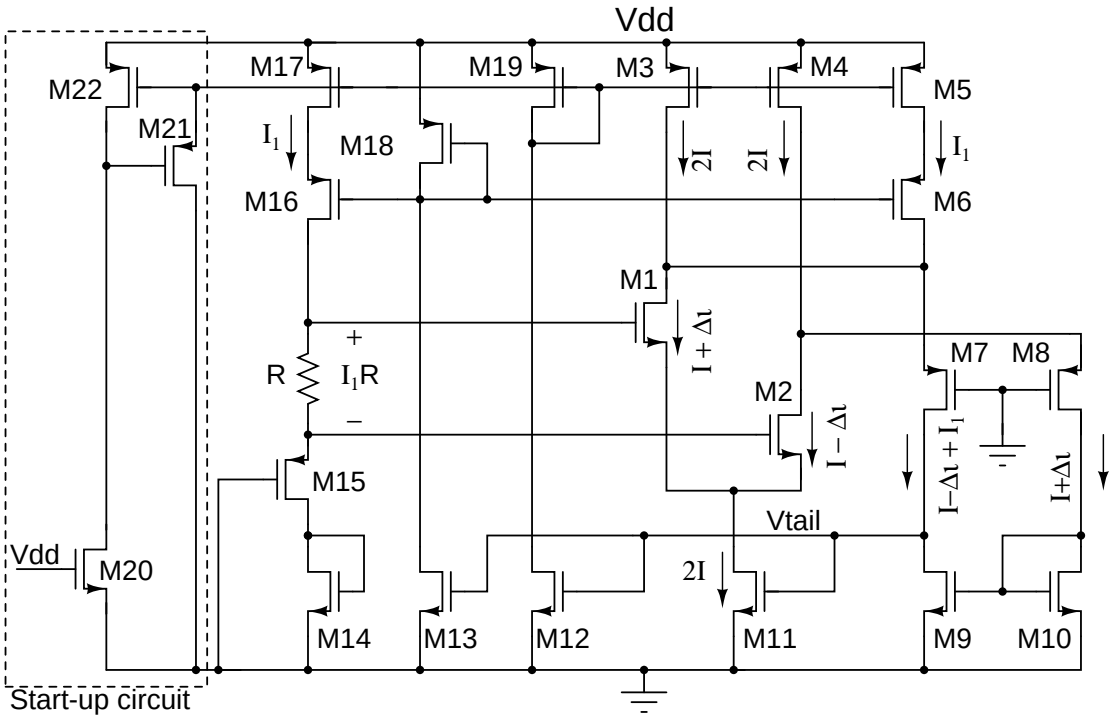


Figure 2.12: Fixed transconductance bias generation circuit.

In the figure, M1 and M2 are the devices whose transconductance needs to be stabilized. The currents in the important branches are marked. In steady state, M9 and M10 will carry equal currents as they form a current mirror. Therefore,

$$I - \Delta i + I_1 = I + \Delta i \tag{2.2}$$

$$I_1 = 2\Delta i \tag{2.3}$$

For the differential pair formed by M1 and M2,

$$\Delta i = g_{m|,M1}\left(\frac{I_1 R}{2}\right) \tag{2.4}$$

Substituting (2.4) in (2.3) for Δi we obtain,

$$g_{m|,M1} = \frac{1}{R} \tag{2.5}$$

Thus, the transconductances of M1 and M2 are servoed to the conductance $1/R$. R is a stable off-chip resistor. Therefore, $g_m|_{M1,M2}$ would be stable over process and temperature.

Circuit operation can be understood as a negative feedback system. Any deviation of $g_{m|,M1}$ from $1/R$ causes negative feedback to adjust the current through M11 to bring $g_{m|,M1}$ back to $1/R$. The drain potentials of M1 and M2 are identical and independent of the supply voltage.

The salient features of this bias generator are the following :

- The generator does not rely on the MOSFET square law, unlike more traditional circuits (Steininger (1990), Zele and Allstot (1996)).
- The generated bias current is very tolerant of the large output conductances of short channel MOSFETs.
- The circuit is robust with power supply variations.

Figure 2.13 shows the schematic of the fixed-Gm bias circuit used for the Gm-C filter designed in this work. The current in M11 is mirrored to the current distribution circuit that distributes the tail current to all transconductors. Simulations (in the absence of mismatch) show that g_m's of M1,2 vary by less than 0.1% for a Vdd varying between

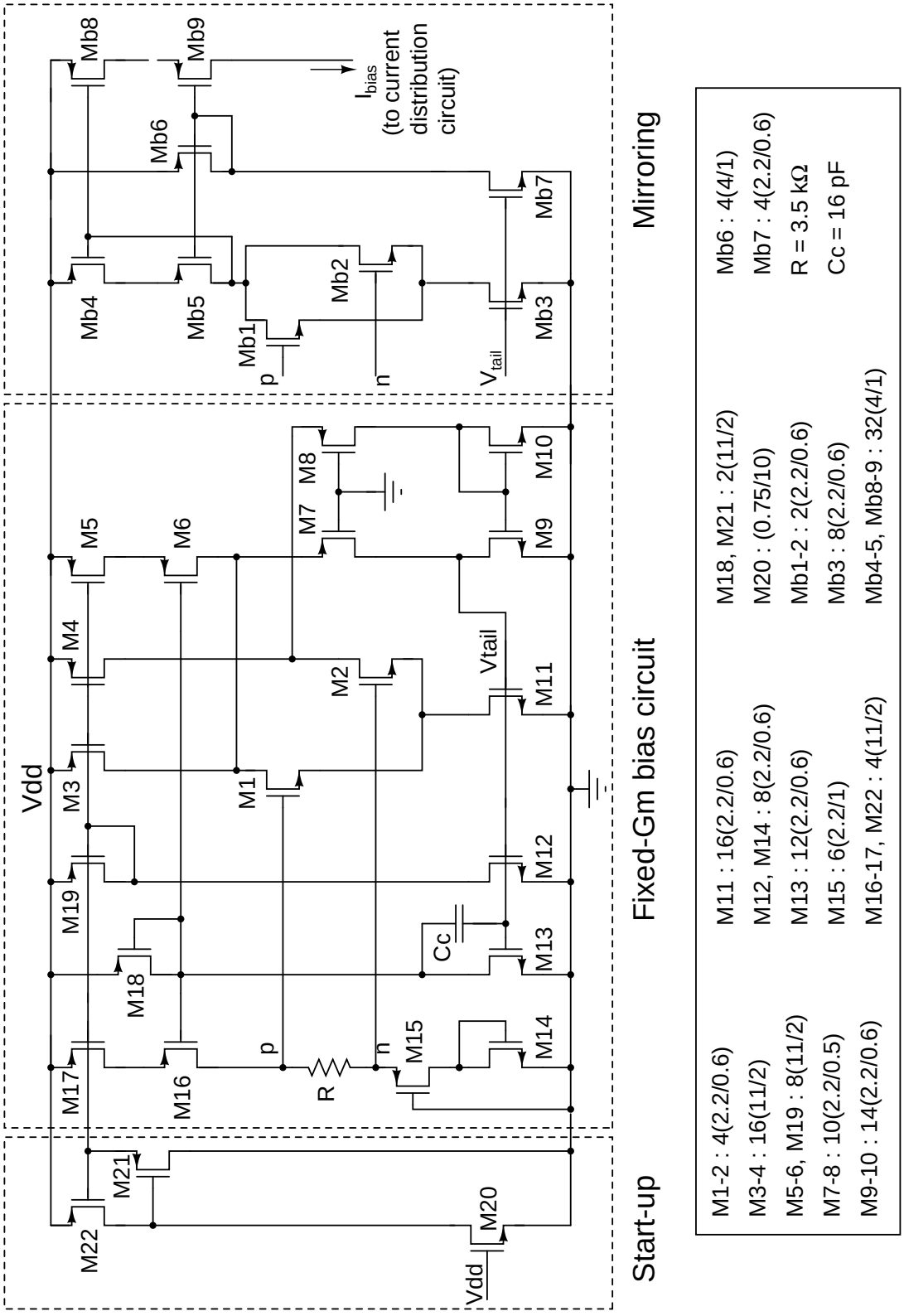


Figure 2.13: Schematic of the complete fixed-Gm bias circuit used in this work.

2.5 & 3.6 V. M11's drain current is distributed to all transconductors on the chip using the precision bias distribution circuit explained in the next section, which is a CMOS version of the bipolar system proposed in Pavan *et al.* (2005).

2.5 BIAS DISTRIBUTION SYSTEM

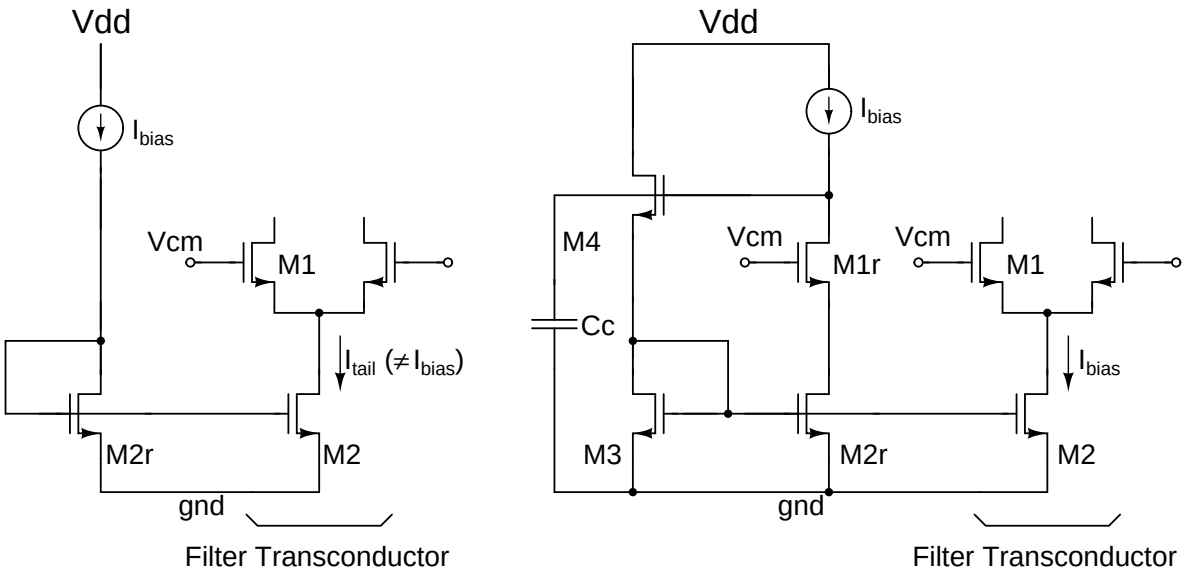


Figure 2.14: (a) and (b) Conventional bias distribution schemes.

The current generated by the fixed-Gm bias circuit should be mirrored to all the filter transconductors as accurately as possible. Figure 2.14(a) shows the simplest circuit that can be used to do this. I_{bias} is generated in the fixed-Gm bias block and routed to the filter transconductor, where it is converted into a voltage by M2r. M2 represents the tail current source of the filter transconductor. For simplicity, the switches used to switch the current source is not shown. Notice that the V_{DS} of M2 is dependent on V_{cm}, the input common-mode voltage of the filter. Note that M2r and M2 should be placed in

close proximity, which is easy to accomplish. One problem with this approach is that the current in M2 no longer equals $\mathrm{I_{bias}}$ due to the different drain-source voltages of M2r and M2. Assuming equal sizes for M2r and M2, the percentage error in the drain current of M2 is seen to be

$$\frac{I_{tail}}{I_{bias}} = \frac{1 + \lambda V_{DS,M2}}{1 + \lambda V_{GS,M2r}} \tag{2.6}$$

To mitigate this problem, a common solution is to employ the precise current mirror shown in Figure 2.14(b). M1r is sized so that it has the same current density as M1 in the filter. Hence, M2 and M2r have the same V_{DS} thereby ensuring that the transconductor current is $\mathrm{I_{bias}}$. Cc compensates the negative feedback loop formed by M2r, M1r, M3 and M4. While this approach certainly eliminates systematic error in the drain current of M2, it poses a layout problem due to the following - four devices (M1r, M2r, M3 and M4) need to be placed in close proximity to M1 and M2. Cc is also usually larger than these devices. Since M1 is a part of the high speed signal path of the filter, it is preferable that the layout be compact. It is therefore seen that while the simple technique of Figure 2.14(a) is advantageous with respect to layout, it has poor accuracy. On the other hand the circuit in Figure 2.14(b) results in an accurate reproduction of current, while resulting in a sub-optimal layout.

A careful look at the techniques shown in Figure 2.14(a) and (b) reveals that it is possible to arrive at a circuit that combines the advantages of both circuits, while avoiding their disadvantages. The basic idea is the following. Precision of the circuit of Figure 2.14(a) could be improved by deliberately modifying I_{bias} to $I'_{bias} = I_{bias}\frac{1+\lambda V_{GS,M2r}}{1+\lambda V_{DS,M2}}$. Since I'_{bias} is a predistorted version of I_{bias}, the percentage error in the drain current

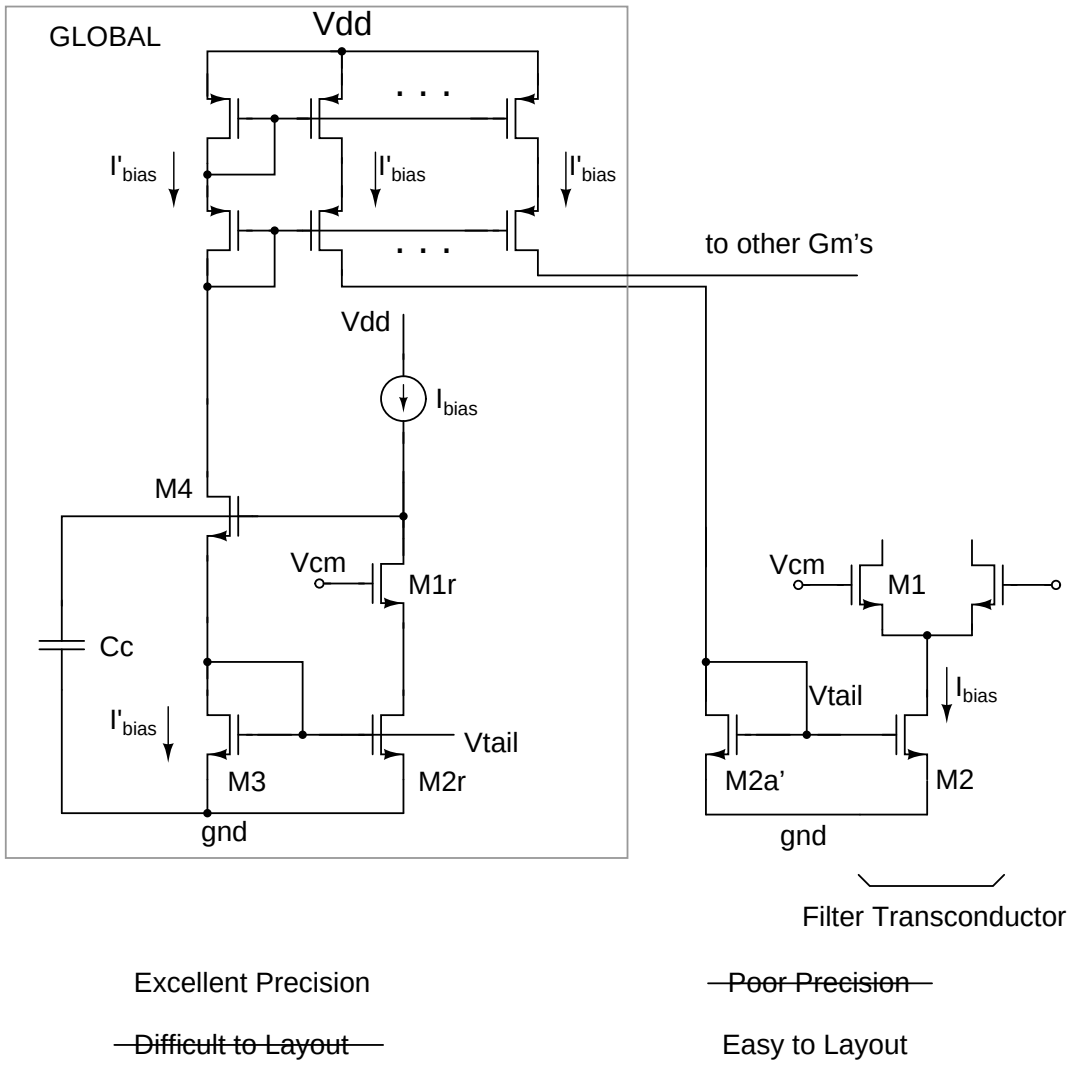


Figure 2.15: Proposed bias distribution technique with the advantages of schemes shown in Figure 2.14.

of M2 is seen to be zero. Now, to generate the predistorted current I'_{bias}, the biasing scheme used in Figure 2.14(b) is used. A circuit that implements this improved scheme is shown in Figure 2.15. The devices shown in the box are global. They are laid out far away from the high speed signal path. M3 and M2r have identical sizes. We see that

$$I'_{bias} = I_{bias}\frac{1+\lambda V_{GS,M2r}}{1+\lambda V_{DS,M3}} \tag{2.7}$$

I'_{bias} is sensed by precision PMOS mirrors and multiple copies of I'_{bias} are routed to

the individual transconductors. At the transconductor, I'_{bias} is mirrored by M2a'-M2, generating I_{bias} in M2. Notice that the layout near the transconductors (the high speed signal path) is very simple and compact. In practice, M2a' and M2 are merged into the same multi-finger structure. While the proposed technique is discussed here in the context of continuous-time filters, it is generic and can be applied to a whole range of analog circuit blocks.

2.6 INTEGRATING CAPACITORS

The technology used in this work provides three alternatives for realizing integrating capacitors.

1. Poly-poly capacitors
2. MOS accumulation capacitors
3. MOS inversion capacitors

In our process, the poly-poly capacitors have excellent linearity but a low specific capacitance of about 0.9 fF/μm^2. MOS capacitors have a density of about 4.8 fF/μm^2 in our technology, which is about five times that of poly-poly capacitors.

It is well known (Behr *et al.* (1992)) that MOS accumulation capacitors are more linear when compared to their inversion counterparts. Therefore, MOS accumulation capacitors are used as integrating capacitors in this filter.

The technology poses a limitation on the minimum size of the MOS accumulation device, which is 6.6 μm/0.65 μm. Therefore the minimum realizable capacitance in this process is about 20.6 fF. This is not a serious issue since the integrating capacitors to be realized are much higher than 20.6 fF.

2.7 FILTER LAYOUT

2.7.1 Programmable Transconductor

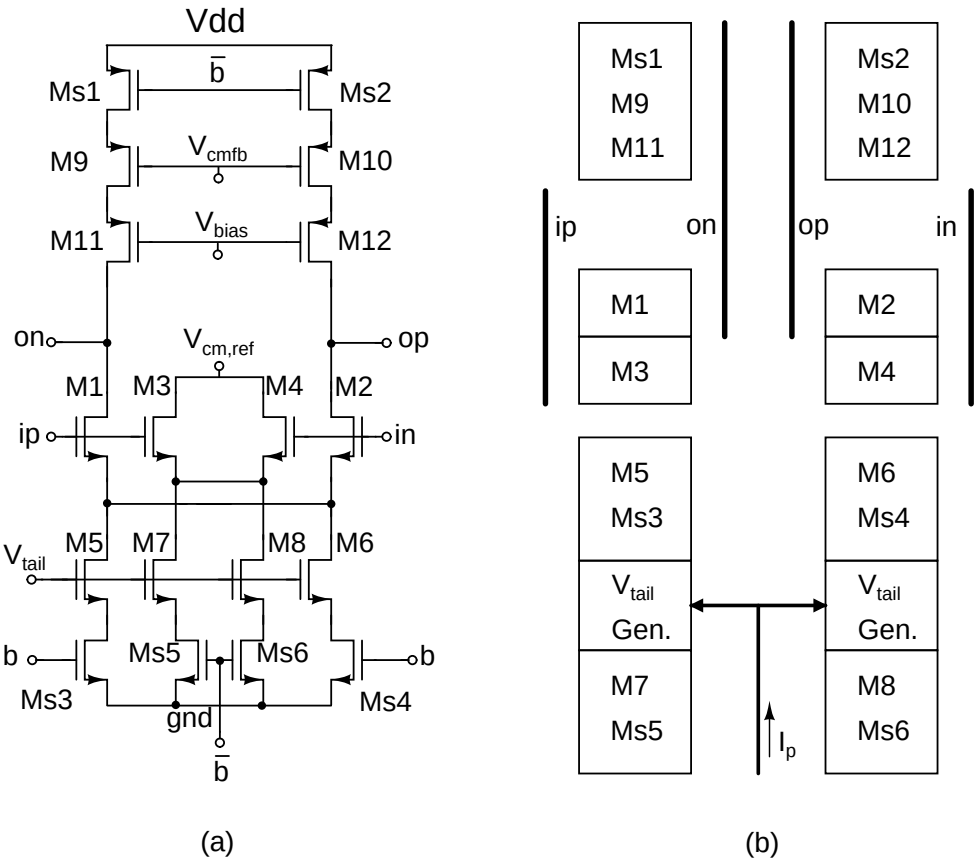


Figure 2.16: (a) Schematic of the unit transconductor g_m (b) Floorplan of the programmable transconductor (G_m) layout.

As mentioned earlier in this chapter, the filter is constructed using identical programmable transconductors. Therefore, only one programmable transconductor has to be laid out. Figure 2.16(a) & (b) show the schematic and floorplan of the programmable transconductor. To explain the correspondence between the layout and the schematic, consider the PMOS load. The left leg of the differential load is formed by M9, M11 and Ms1. In the layout, the PMOS load (left leg) of all the unit transconductors forming the programmable transconductor are laid out together. The block on the top left of Figure 2.16(b) shows this. Other transistors are labelled in a similar fashion.

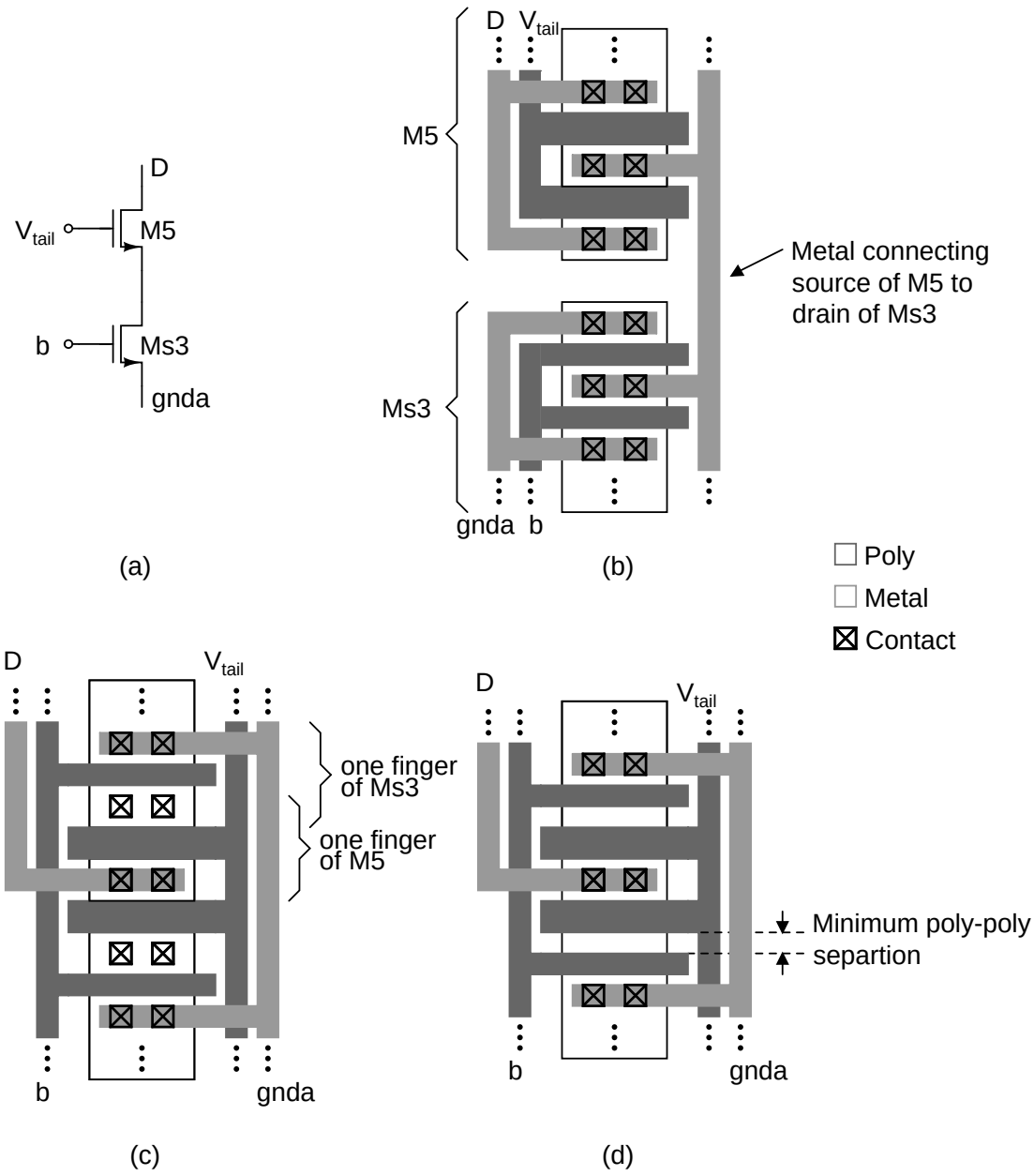


Figure 2.17: Demonstration of area efficient layout - (a) Schematic to be laid out (b) Simple layout, where M5 and Ms3 are laid separately (c) Layout with fingers of M5 and Ms3 merged together (d) Optimized layout, with unnecessary contacts removed.

For laying out series connected (cascoded) transistors like those in the tail current sources (for example M5 and Ms3) and cascoded PMOS loads (for example M9, M11 and Ms1) of the transconductor, a simple method is to lay the transistors separately and then interconnect them. This is shown in Figure 2.17(b), where the tail current source formed by M5 and Ms3 is taken as an example. The source of M5 is routed

to the drain of Ms3 using a metal wire. A compact alternative, if M5 and Ms3 have the same finger width and same number of fingers, is to share the drain diffusion of Ms3 with the source diffusion of M5. These fingers are then connected in parallel to realize the complete current source. This is shown in Figure 2.17(c). Notice that the source-drain contacts of M5 and Ms3 are not connected together. This layout is area efficient compared to that in Figure 2.17(b), since the transistors are merged. Further optimization of the area is possible. The source-drain contacts of M5 and Ms3 are not necessary and can be omitted. The separation between the gates of M5 and Ms3 can be kept to the minimum allowed poly-to-poly separation. This is shown in Figure 2.17(d), and has been extensively used in this work. The PMOS loads are also laid out in a similar fashion.

2.7.2 Filter Layout

The scheme used for the layout of the filter is shown in Figure 2.18(a). Each transconductor is represented by a simple block with input and output lines, ip, in and op, on respectively. The capacitors are also represented by simple box, but coloured gray, with only the integrating nodes shown (i.e op, on). Figure 2.18(b) shows the fully differential schematic of the filter. The schematic is drawn in such a way to have a one-to-one correspondence with the layout.

Figure 2.18(a) emphasizes the routing between the blocks. All the vertical routing is made in *metal2* and the horizontal routing is made in *metal3*. The interconnection is accomplished by inserting a via between these metal lines. In the figure, interconnection of lines is shown by a black bubble. Notice carefully that while interconnecting two

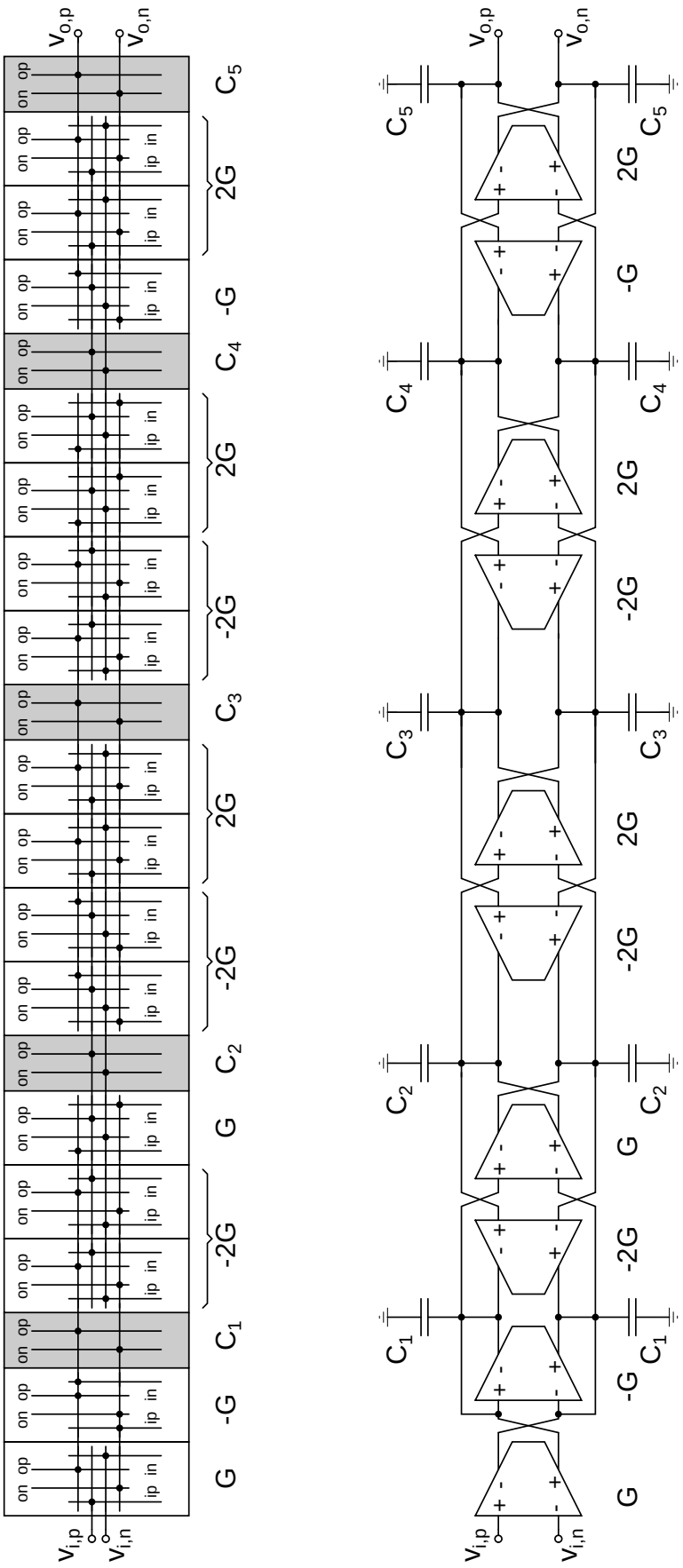


Figure 2.18: (a) Scheme of filter layout (b) Fully differential schematic of the filter.

wires, both the wires are extended beyond the junction (Pavan (1999)). This ensures that the interconnect parasitic capacitances on the differential lines are equal. A shield of grounded *metal1* is used below the long routing lines. This serves two purposes-

1. It reduces the coupling between the line and the substrate.
2. The parasitic capacitances will have a path to ground (through $metal1$) and are well defined. These are small capacitances, referenced to ground and can be absorbed into the integrating capacitors.

Figure 2.19 shows the screen-shot of the complete filter layout with all the main building blocks marked. The empty space available in the chip is filled with supply bypass capacitors. NMOS and PMOS capacitors are used for bypassing. The total on-chip bypass capacitance is about 1.3 nF.

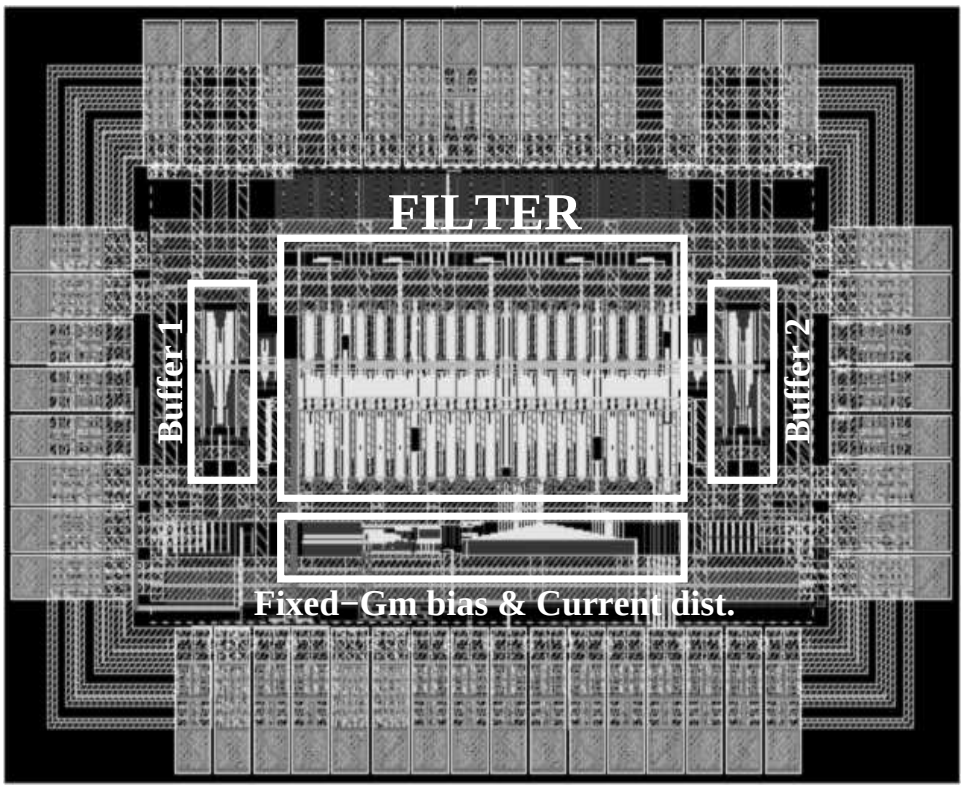


Figure 2.19: Screen-shot of completely laid filter

After the complete layout of the filter, interconnect parasitics are extracted. These parasitics, along with the non-idealities of the transconductor, cause the filter response

to deviate significantly from the desired response, thereby necessitating a “design centering” procedure that modifies the integrating capacitor values and brings the response back to the desired one. The next chapter (Chapter 3) discusses the design centering technique in detail.

CHAPTER 3

FILTER DESIGN CENTERING

The term “design centering” used in this thesis refers to the procedure for ensuring that the filter response *including layout parasitics* is indeed the desired one (at the nominal process corner & ambient temperature). With process & temperature variations, the filter performance will deviate from the nominal, and steps should be taken to ensure that the variations in the response are within prespecified bounds. Commonly, automatic tuning loops are used to keep the nominal time constants in the filter stable across process and temperature (Schaumann and Tan (1989)). These techniques are not the focus of this work and are not discussed here. The word “design centering” is not to be confused with statistical design centering. The latter term is used for yield optimization, where an attempt is made to select the nominal values of the design parameters so as to ensure that the behavior of the circuit remains within specifications with the highest manufacturing yield.

3.1 THE NEED FOR DESIGN CENTERING IN INTEGRATED ANALOG FILTERS

Active analog filters are networks of integrators. Without loss of generality we consider the case of Gm-C integrators. An ideal integrator shown in Figure 3.1(a) has a transfer function $\frac{G_m}{sC_i}$. A real integrator has several nonidealities. They are -

1. Finite DC gain.

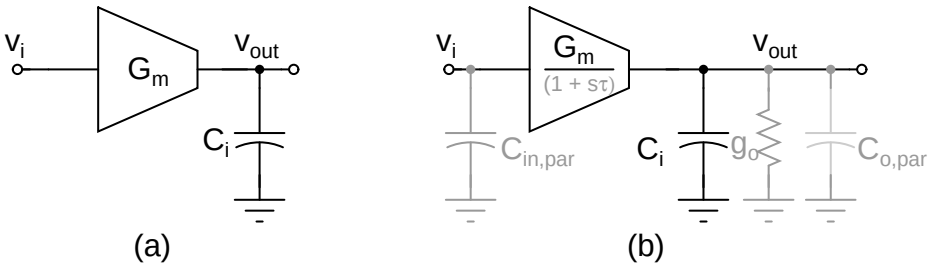


Figure 3.1: Ideal and nonideal Gm-C integrators.

2. Finite bandwidth and parasitic poles/zeros.
3. Parasitic capacitances associated with the input and output terminals. These capacitances are from the devices used to realize the transconductor, as well as routing capacitances.

The integrator with the above mentioned non-idealities is shown in Figure 3.1(b). $1/\tau$ and g_o are the bandwidth and output conductance of the transconductor respectively. $C_{in,par}$ and $C_{o,par}$ are the parasitic capacitances at the input and output terminals of the transconductor.

In any practical Gm-C filter, an attempt is made to keep the transconductor DC gain sufficiently high. Further, $1/\tau$ is chosen to be significantly higher than the $\omega_p Q_p$ product of the filter. Even still, along with input/output parasitic capacitances, these nonidealities can significantly alter the filter transfer function. It is therefore necessary to correct the design for all these effects. This is done by varying the capacitors and/or transconductor values. This constitutes the design centering process.

Design centering high frequency filters is a challenge due to the following. The total parasitic capacitance at a node can be a significant fraction of the intended integrating capacitance (in the filter described in the previous chapter, the parasitic capacitances at the integrating nodes were between 25% to 65% of the intended integrating capacitances). These parasitic capacitances can significantly alter the frequency response of

the filter, and some way of accounting for these capacitors is necessary.

3.2 PREVALENT METHODS

It is more convenient to use capacitors as design variables rather than transconductors, since the former can be individually and easily adjusted. Commonly used methods of design centering are the following -

1. Brute-force tweaking.
2. Using a circuit optimizer.

The following subsections briefly explain these procedures and their limitations.

3.2.1 Brute-Force Tweaking

The designer, based on experience and circuit intuition, varies capacitor values until the response is close to the desired response. As can be easily appreciated, this approach is time consuming, since an AC simulation has to be run after each such “tweak”. Each AC simulation of the extracted netlist in a SPICE like simulator can take a very long time, due to the large number of active devices and interconnect parasitics.

Further, most circuit designers are only likely to have intuition about simple filter building blocks like second order sections. The “tweak and simulate” approach can be seen to be hopeless when a more complicated topology - like a ladder filter has to be designed. This difficulty is one of the reasons why a cascade-of-biquads structure is preferred over a ladder filter in spite of the latter having lower sensitivity to component variations.

Some CAD tools allow a designer to back-annotate the parasitic capacitances extracted from the layout onto the schematic. The explicit capacitances in the filter could then be reduced by these parasitics. While this approach can help to some degree, it is still not satisfactory, since many parasitics could be to nodes other than small signal ground - for example, a parasitic capacitance C_p between two balanced nodes is equivalent to having a capacitance of $2\,C_p$ from each of the nodes to ground. It is thus seen that this would need significant designer intervention in interpreting each of the parasitic capacitances at a node. The brute-force tweaking of design variables, therefore, would require significant amount of designer and simulation time.

3.2.2 Using a Circuit Optimizer

Many commercial simulation packages have circuit optimizers built into them. These optimizers can be used for design centering. This is a less "cut-and-try" method, in which the layout extracted netlist is input into the optimizer and the design variables are varied until the filter response matches the desired response. Traditional SPICE simulator based optimizers work in the following manner. The circuit to be optimized is simulated at the transistor level with an initial guess of the design parameters. The objective function (derived from a set of specifications) is evaluated and the design parameters are modified in an attempt to minimize it. The circuit optimizer is simply an optimization "framework" built around a circuit simulator.

While this method of design centering works, it can be problematic due to the following. The optimization algorithm (for example, the Nelder-Mead simplex method) has to compute the response of the filter several times (1000 is not uncommon), before

the difference between the actual and desired response is sufficiently small. Each frequency response evaluation of the complete layout extracted filter netlist is very time consuming (for the Gm-C filter presented in chapter 2, one such evaluation took 20 minutes on a PC with a 3.2 GHz processor). Thus, the entire optimization process may take several hours (if not days) to converge.

From the above discussion, we see that there is a need for a time-efficient design centering technique that involves very few simulations of the complete layout extracted netlist. The "Space mapping" technique, originally introduced by Bandler *et al.* (1994) for optimizing electromagnetic structures was adopted in this thesis. Space mapping is now in use in a variety of applications (Bandler *et al.* (2004), Bakr (2000)) from RF and Microwave implementation to non-linear device modeling to structural design (in civil engineering). Surprisingly this body of literature does not seem to have been appreciated by active-filter designers. In this chapter we show that a simplified form of space mapping is an effective technique to design-center continuous-time filters.

3.3 SPACE MAPPING : AN OVERVIEW IN THE CONTEXT OF FILTER DESIGN

Space mapping was originally intended for the optimization of electromagnetic structures which involve time-intensive simulations. The basic idea is to come up with a less accurate model which approximately represents the expensive model to be optimized, but takes a little time to simulate. In space mapping terminology, the expensive model (to be optimized) is called the "fine" model and the less accurate, cheaper model is termed the "coarse" model.

A mapping is established between the design spaces of the fine and coarse models. The optimum design variables are computed for the coarse model. This optimal solution obtained in the coarse design space is interpreted or *mapped* into the fine space. This process involves many computations of the coarse model. However, this is not a problem since these computations are inexpensive.

The original space mapping algorithm assumes a linear mapping between the two parameter spaces, which might not be accurate if significant misalignment exists between the two spaces. Several improvements, like Aggressive Space Mapping (ASM), Trust Region Aggressive Space Mapping (TRASM) were subsequently introduced (Bakr (2000)).

The design centering problem for high frequency filters is similar to that of electromagnetic structure optimization - the computation of the frequency response of the layout extracted filter is CPU intensive. Therefore, the space mapping technique can be applied to these filters, by introducing a “coarse” model for the layout extracted transistor level circuit.

In high frequency filters, parasitic capacitances are the dominant nonideality. Note that if they were the only nonideality, the design space of a “coarse” model comprising of ideal integrators would simply be offset from the design space of the actual filter. Since other nonidealities (like finite gain and bandwidth) are made small by design, it is seen that a simplified version of the space mapping technique should be adequate for this class of problems. This is explained with an example in the next subsection.

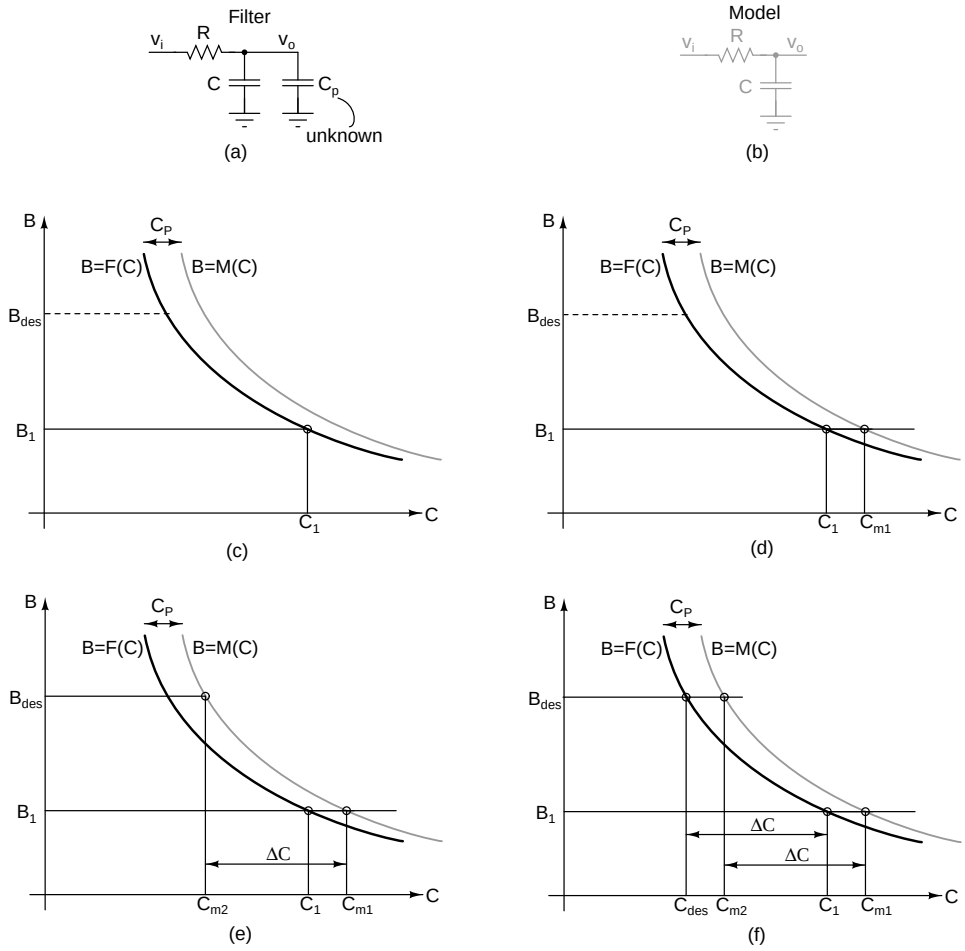


Figure 3.2: Space mapping : the model design space is offset from the filter design space. (a) The filter, with the explicit capacitance, as well as a parasitic C_p. (b) The model (c) Step 1 - finding $F(C_1)$, (d) Step 2 - finding $M^{-1}(F(C_1))$, (e) Step 3 - finding $M^{-1}(B_{des})$, (f) Step 4 - finding C_{des}.

3.3.1 Graphical Example

We now provide intuition for the space mapping technique as applied to filter design, using a graphical approach. For simplicity, consider the design of a first order RC lowpass filter, shown in Figure 3.2(a). The design centering problem is to determine C so that the 3 dB bandwidth of the filter is set to a desired value B_{des}. R is fixed. A parasitic capacitance C_p occurs in parallel with C. *Assume* that the circuit of Figure 3.2(a) is a layout extracted netlist, which takes very long to simulate. We form a simplified *model* of the filter, shown in Figure 3.2(b). We postulate that it is possible to simulate

the model extremely fast. The bandwidths of the filter and the model as a function of C are depicted by the dark ($F(C)$) and light ($M(C)$) curves in Figure 3.2(c) respectively. Note that $M(C)$ is simply a translated version of $F(C)$. The space mapping method of determining C_{des} which results in a filter bandwidth B_{des} is as follows :

1. Choose an initial guess for C in the filter, say C_1. Simulate the filter with this value. The resulting bandwidth is B_1. Notice that $B_1 = F(C_1)$ will be lower than B_{des} due to the parasitic capacitance C_p (Figure 3.2(c)).
2. Divert the optimization task to the *model*. Determine the value of $C = C_{m1}$ required in the *model* that results in a bandwidth of B_1 (Figure 3.2(d)). This is an inverse problem, in the sense that we are required to find C that results in a given response (i.e. $C_{m1} = M^{-1}(B_1)$). In general, the solution is arrived at through an iterative process requiring several simulations of the model. This is not an issue, since the model can be rapidly simulated. In the space mapping parlance, this process is called Single Point Extraction (SPE). In the trivial example under consideration, the answer is seen to be $C_{m1} = C_1 + C_p$. Knowing C_{m1} and C_1, one can have an estimate of the unknown parasitic capacitance C_p.
3. For the *model*, determine the value of $C = C_{m2}$ that results in a bandwidth of B_{des} (i.e. $C_{m1} = M^{-1}(B_{des})$). This is also an iterative process requiring several simulations of the model.
4. The capacitance required in the filter is seen to be $C_{des} = C_1 + C_{m2} - C_{m1}$, since $M(C)$ is a translated version of $F(C)$.

In conventional design centering, $F(C)$ would have to be computed several times to determine $C_{des} = F^{-1}(B_{des})$. Observe that in the space mapping technique, the filter is simulated only once. The model is simulated many times in the process of finding $C_{m1} = M^{-1}(B_1)$ and $C_{m2} = M^{-1}(B_{des})$. Therein lies the efficiency of the technique. The name "space-mapping" makes sense, since the design *space* of the filter is *mapped* onto the design space of the model.

In the example considered above, the model design space is simply a translated version of the filter space - thus only one (time consuming) filter simulation (to determine $B_1 = F(C_1)$) is necessary to determine C_{des}. This need not be the case always. The

following example explains the space mapping when the model design space is not just a translated version of the filter design space.

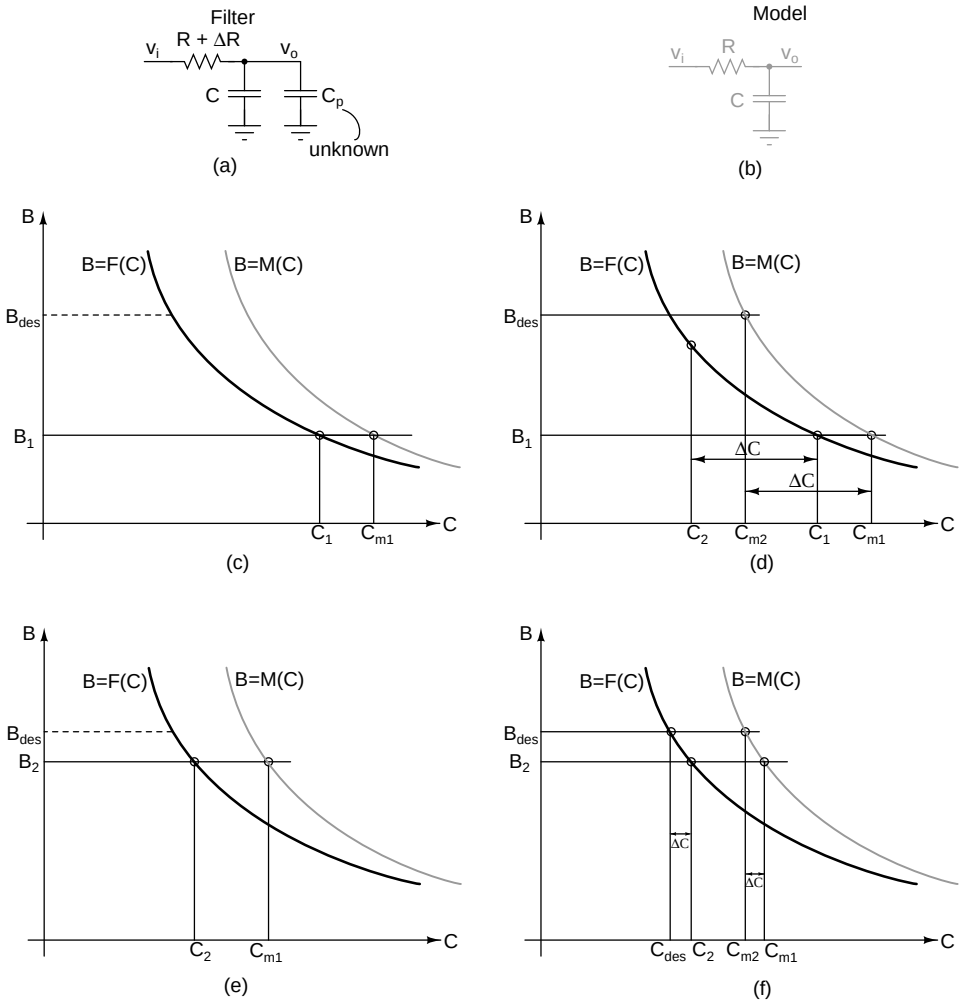


Figure 3.3: Space mapping when the model space is not just a translated version of the filter space : (a) & (b) - first iteration, (c) & (d) second iteration. .

Figure 3.3(a) & (b) show the filter and model respectively. The filter Figure 3.3(a), in addition to an unknown parasitic capacitance, has an unknown offset ΔR for the resistor R. But the goal of design centering is still the same i.e. determine C so that the 3 dB bandwidth of the filter is set to the desired value B_{des}.

We proceed for the design centering in the same way as we did for the earlier example. Figure 3.3(c) & (d) show the first iteration. Since $M(C)$ is not a translated version of $F(C)$, the output of the first iteration will not lead to C_{des}. Let C_2 be the output of the

first iteration. $F(C_2) \neq B_{des}$, but C_2 is very close to C_{des}. C_2 is used as the initial guess for the second iteration, which is shown in Figs. 3.3(e) & (f). Again, note that only two simulations of the filter were necessary (to determine $B_1 = F(C_1)$ and $B_2 = F(C_2)$).

3.3.2 Generalization to a practical filter

Now that space-mapping is understood using a simple example, we generalize the procedure for a practical filter, where the frequency response is a complex function of many variables. Since the filter capacitors are modified due to interconnect parasitics, it is common practice to modify the explicit capacitors to obtain the desired frequency response. Hence, these capacitors are chosen as the design variables and are denoted in vector form as $\mathbf{C}$. Let $F(\mathbf{C})$ be the filter frequency response for the set of capacitors $\mathbf{C}$ evaluated over a desired frequency grid. H_{des} is the desired frequency response, evaluated over the same frequency grid. The response of the model is denoted by $M(\mathbf{C})$. If the model is chosen appropriately, the model space is almost a translated version of the filter space, and the design centering process to correct for the effect of layout parasitics can be simplified as follows :

1. Choose an initial value of capacitors $\mathbf{C}_1$. The values used in the schematic is a good starting point. Evaluate $F(\mathbf{C}_1)$.
2. Determine $\mathbf{C}_{m1}$ needed in the model, so that $M(\mathbf{C}_{m1}) = F(\mathbf{C}_1)$. This is done by finding $\mathbf{C}$ that minimizes $||M(\mathbf{C}) - F(\mathbf{C}_1)||_2$.
3. Determine $\mathbf{C}_{m2}$ needed in the model, so that $M(\mathbf{C}_{m2}) = H_{des}$. This is done by finding $\mathbf{C}$ that minimizes $||M(\mathbf{C}) - H_{des})||_2$.
4. Form $\mathbf{C}_2 = \mathbf{C}_1 + \mathbf{C}_{m2} - \mathbf{C}_{m1}$.
5. Evaluate $F(\mathbf{C}_2)$. If this is not sufficiently close to H_{des}, repeat steps 1 through 4 above, with $\mathbf{C}_2$ as the initial guess.

The above procedure works well, since offset is the major component of the difference in the filter and model spaces. In experience of the author, just one or two filter computations are usually sufficient if the model is chosen appropriately, as described in the next section.

3.4 SPACE-MAPPING APPLIED TO THE 71.4-500 MHz FIFTH ORDER Gm-C LADDER FILTER OF CHAPTER 2

This section shows the effectiveness of space-mapping employed to design center a 71.4-500 MHz fifth order Chebyshev Gm-C ladder filter designed in Chapter 2. Design centering is attempted at the highest bandwidth. Constant-C scaling ensures that the shape of the frequency response remains the same over all bandwidth settings.

3.4.1 Transconductor Nonidealities

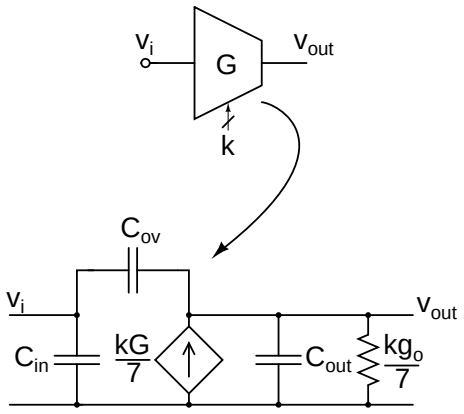


Figure 3.4: Small signal model of the digitally programmable transconductor. k is the bandwidth programming code, settable between 1-7.

Each programmable transconductor of the filter is associated with several nonidealities. The small signal model of the digitally programmable transconductor is shown in Figure 3.4. Apart from parasitic capacitances C_{in} and C_{out} which appear in parallel

with the integrating capacitors, a small overlap capacitance C_{ov} couples the input to the output. Another nonideality is the finite DC gain of the transconductor. A single 3-bit programmable transconductor used in the filter has about 1000 transistors.

The entire design flow uses Cadence tools. The layout extracted schematic has about 21000 transistors and 8400 capacitors. On a computer with a 3.2 GHz processor and 256 MB RAM, evaluating the DC operating point of the chip takes 15 minutes and frequency response computation at 1001 points in the frequency range (0-1000 MHz) takes 25 minutes. It is apparent that optimizing the filter with a circuit optimizer (the conventional method) is not a practical option.

3.4.2 Model

The next step is to have a model that approximately represents the actual filter and takes a little time to simulate. A model whose frequency response can be computed rapidly is a state-space representation of Figure 2.7. The transconductor finite output impedances are included in the model, since these are readily available from a DC operating point analysis of a single transconductor. The differences between the model and the filter are the following. Input/output capacitances and routing parasitics of the transconductors are not accounted for in the model. Overlap capacitance of the transconductors is also not a part of the model. If overlap capacitances are neglected, the model space is a translated version of the filter design space. As usual, the state variables are the five capacitor voltages denoted by $\mathbf{v}$.

The state space model of the filter is

$$\dot{\mathbf{v}} = \mathbf{A}\mathbf{v} + \mathbf{B}v_i \tag{3.1}$$

$$v_o(t) = [\ 0 \quad 0 \quad 0 \quad 0 \quad 1\ ]\mathbf{v} \tag{3.2}$$

where

$$\mathbf{A} = \begin{bmatrix} -\frac{(G+4g_o)}{C_1} & -\frac{2G}{C_1} & 0 & 0 & 0 \\ \frac{G}{C_2} & -\frac{3g_o}{C_2} & -\frac{2G}{C_2} & 0 & 0 \\ 0 & \frac{2G}{C_3} & -\frac{4g_o}{C_3} & -\frac{2G}{C_3} & 0 \\ 0 & 0 & \frac{2G}{C_4} & -\frac{3g_o}{C_4} & -\frac{G}{C_4} \\ 0 & 0 & 0 & \frac{2G}{C_5} & -\frac{2g_o}{C_5} \end{bmatrix}$$

$$\mathbf{B} = [\ \frac{G}{C_1} \quad 0 \quad 0 \quad 0 \quad 0\ ]^T \tag{3.3}$$

The model is coded in MATLAB. G and g_o are obtained from a DC operating point analysis of a single transconductor. A frequency response calculation over a 1001 point grid from 0-1000 MHz takes less than 100 ms (recall that it is about 40 minutes for layout extracted filter).

3.4.3 Design Centering

As mentioned in the beginning of this section, design centering is attempted at the highest bandwidth setting of 500 MHz.

1. The initial capacitor values are chosen to be those corresponding to the "ideal" ladder of Figure 2.7, $\mathbf{C}_1$ = [1.36, 3.68, 5.07, 4.05, 2.12] pF. The layout extracted

filter is simulated with $\mathbf{C}_1$. The resulting frequency response $F(\mathbf{C}_1)$ is compared with the desired response in in Figure 3.5. Notice that the bandwidth is significantly lower than the ideal response. The shape of the response is also modified due to the parasitics.

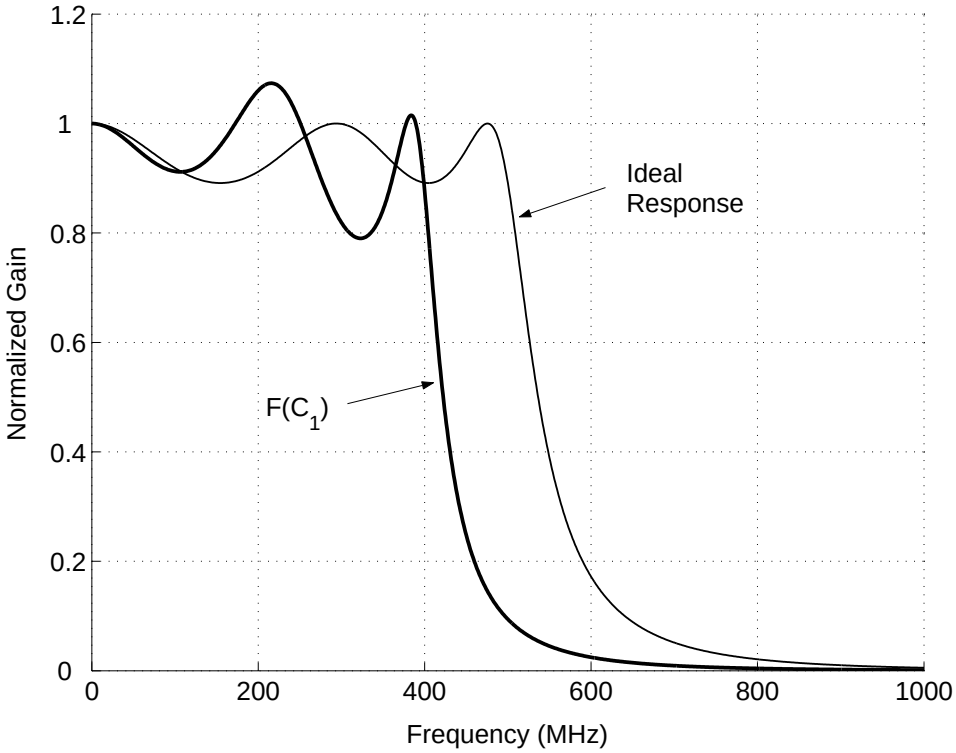


Figure 3.5: Design centering : comparison of $F(\mathbf{C}_1)$ and H_{des}.

2. $\mathbf{C}_{m1}$ needed in the model, to obtain $F(\mathbf{C}_1)$ is determined. The *fminsearch* optimization routine in MATLAB, which employs the Nelder-Mead simplex optimization process is used to do this. The objective function used for the minimization is $||M(\mathbf{C}) - F(\mathbf{C}_1)||_2$. The resulting $\mathbf{C}_{m1}$ = [2.225, 4.84, 6.35, 5.225, 2.703] pF.

3. The capacitor values in the model ($\mathbf{C}_{m2}$) that would result in the desired (ideal) response H_{des} are found, as in step 2 above. $\mathbf{C}_{m2}$ = [1.497, 3.632, 5.38, 3.92, 2.157] pF.

4. The capacitance vector that must be used in the filter to obtain the ideal response is calculated from $\mathbf{C}_{des} = \mathbf{C}_1 + (\mathbf{C}_{m2} - \mathbf{C}_{m1})$. Thus, $\mathbf{C}_{des}$ = [0.632, 2.472, 4.1, 2.744, 1.575] pF

It takes about 20 seconds to complete steps 2 & 3.

Figure 3.6 shows the design centered frequency response of completely extracted filter and Figure 3.7 shows the passband detail. See the excellent matching between the

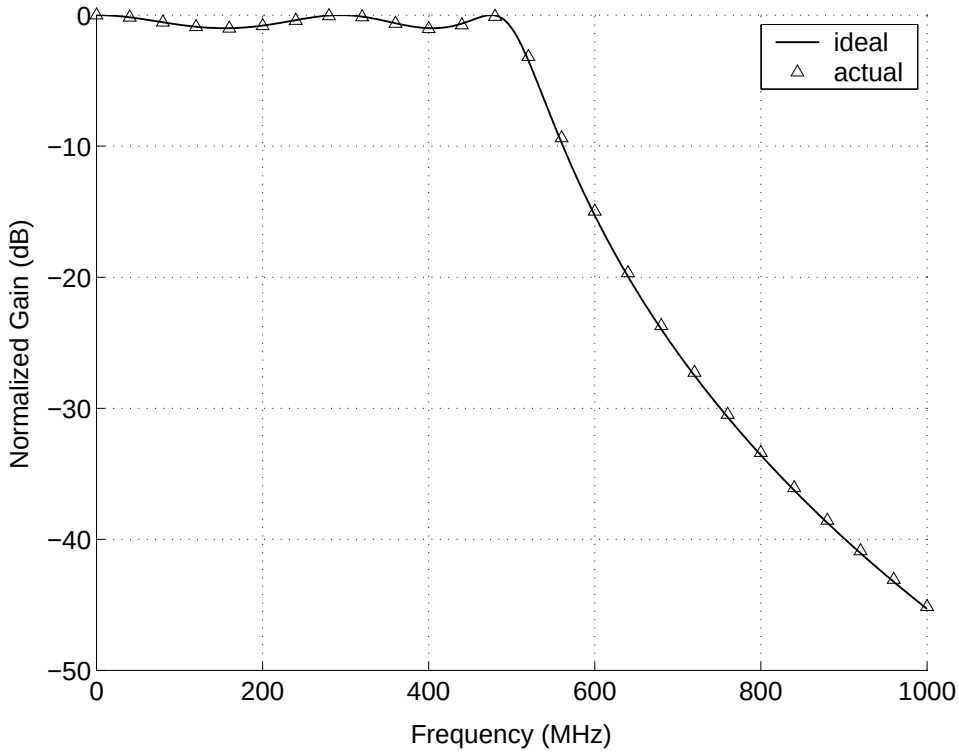


Figure 3.6: The actual and desired responses match after one iteration.

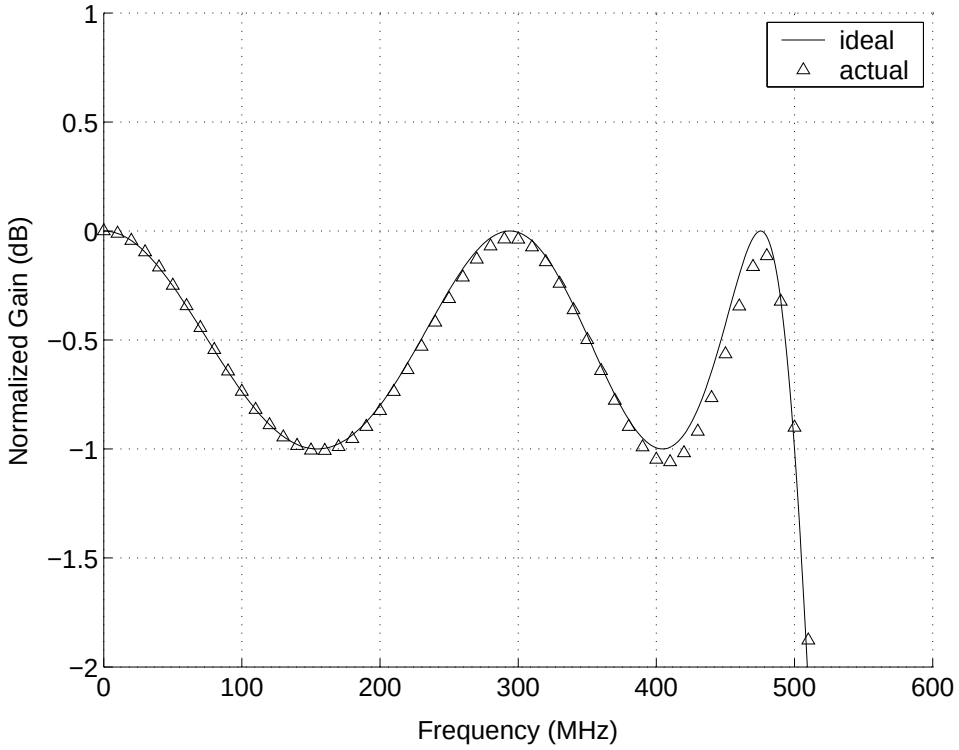


Figure 3.7: Passband detail of Figure 3.6.

design centered and the desired responses. The small deviation in the response after design centering is due to the size of the smallest unit-capacitor (20.6 fF) used in the design. This technique of design centering is thus found to be efficient and has been extensively used in our work, especially for correcting the frequency response in the face of MOS non-quasi-static effects, the details of which are discussed in the next chapter.

CHAPTER 4

ANALYSIS AND COMPENSATION OF MOS NON-QUASI-STATIC EFFECTS IN HIGH FREQUENCY TRANSCONDUCTOR–CAPACITOR FILTERS

Simple small signal models of semiconductor devices are derived using the quasi-static (QS) approximation, where the following assumption is made. *When the device is excited with time varying terminal voltages, for example* $v_T(t)$ *at terminal* T*, the charge concentration at any position of the device at any time* t_1 *is identical to that obtained when a dc voltage* $V_T = v_T(t_1)$ *is applied at the corresponding terminal* (Tsividis (1999)). This is a valid assumption if the terminal voltages vary sufficiently slowly so that the charge carriers in the device respond with negligible inertia. The quasi-static assumption makes device analysis (and hence the circuit analysis) simple. However, when the terminal voltages are varying fast, the quasi-static approximation breaks down since, charges in the device fails to respond instantaneously. It is difficult to quantitatively define the term "fast" and it depends on the type of the analysis and the accuracy one seeks. It becomes necessary to consider the non-quasi-static (NQS) operation of the devices to understand the actual behaviour of the device (and circuit).

In high frequency continuous-time filters, if the bandwidth becomes a significant fraction of the limiting frequency of the active devices, the quasi-static assumption for the devices will lead to a filter response that is in deviation from the desired. It is therefore necessary to understand the non-quasi-static behaviour of the devices, analyze

their influence on the filter response and correct for these effects in order to get the desired response.

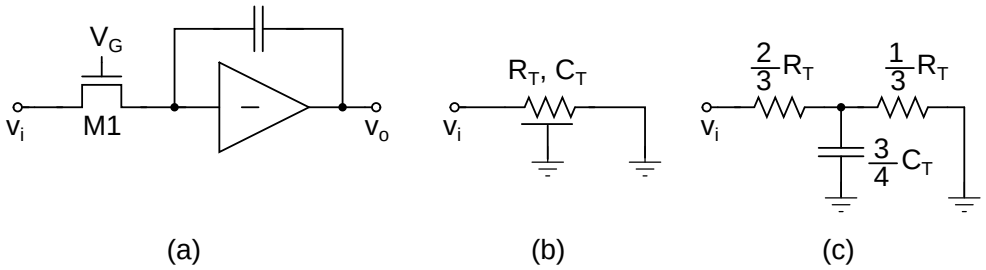


Figure 4.1: (a) Simplified single-ended schematic of the integrator used by Shi *et al.* (1986) (b) Distributed RC small signal model of the transistor M1 and (c) First order approximation for (b). R_T and C_T are the total channel resistance and capacitance respectively

Since the filter designed in this thesis uses MOS devices as the active element, we focus on the influence of non-quasi-static behaviour of the MOS transistors on filter performance. Shi *et al.* (1986), Pu and Tsividis (1990) report filters exploiting the distributed RC nature of the MOSFET in the triode region. Figure 4.1 shows the integrator used in the filter of Shi *et al.* (1986). M1 is the MOSFET operated in triode region. The distributed nature of channel was taken in to account by modeling M1 with a distributed RC line approximated to the first order as shown in Figure 4.1(b). An excellent analysis on the high frequency effects in such filers is given by Khoury and Tsividis (1987).

The MOSFETs used in the transconductors of the filter designed in this thesis operate in saturation. In this chapter, we examine the effects of MOS NQS effects on the performance of constant-C scaled Gm-C filters. A hardware and power efficient compensation technique is proposed to compensate for MOS NQS effects.

4.1 INFLUENCE OF NQS EFFECTS ON CONSTANT-C SCALED Gm-C FILTERS

In this section we examine the quasi-static and non-quasi-static behaviour of the constant-C scaled programmable transconductor and thereby analyze the influence of QS and NQS effects on the constant-C scaled Gm-C filters. The constant-C scaled programmable transconductor presented in chapter 2 is redrawn in Figure 4.2.

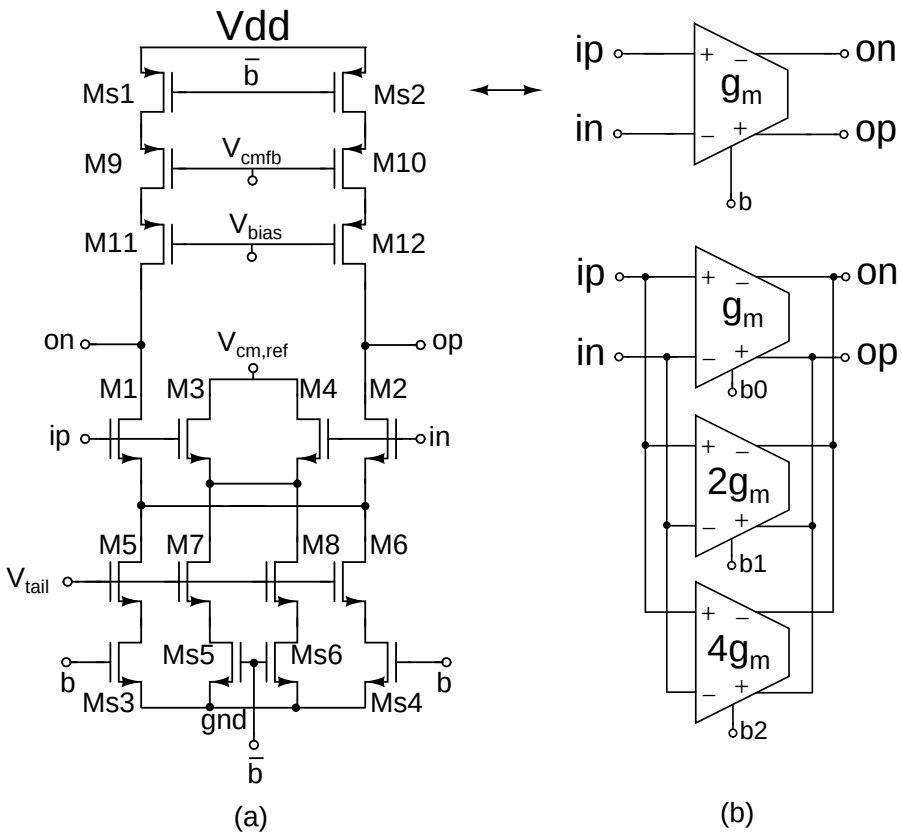


Figure 4.2: Programmable transconductor (a) Unit g_m-cell and (b) Realization of programmable Gm using unit g_m-cells.

4.1.1 A Simple QS Model for the Programmable Transconductor

A simple intrinsic small signal model for the transistors M1 and M2 in Figure 4.2(a), assuming quasi-static operation, is shown in Figure 4.3 (using the results from Tsividis

(1999)). Assuming this model for the transistors, the resulting intrinsic small signal

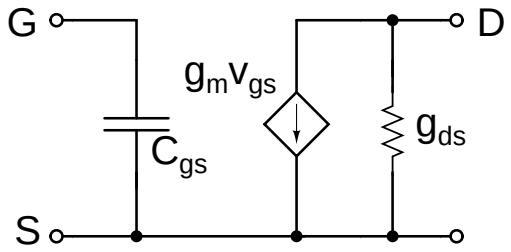


Figure 4.3: A simple quasi-static small signal model of a MOSFET operating in saturation

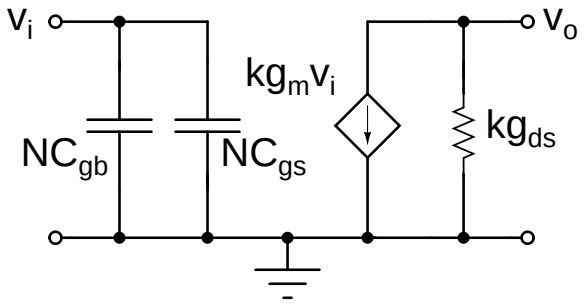


Figure 4.4: A simple quasi-static small signal model of the programmable transconductor of Figure 4.2. N is the number of unit cells per transconductor and k is an integer that sets the filer bandwidth ($1 \leq k \leq N$).

model of the programmable transconductor of Figure 4.2 is shown in Figure 4.4. The word "intrinsic" used here means that only that part of the programmable transconductor that is responsible for transconductor action is considered. N is the number of unit cells per transconductor (N=7 for the transconductor in Figure 4.2). k is an integer that determines the filter bandwidth, settable in the range $1 \leq k \leq N$. g_m, g_{ds}, C_{gs} & C_{gb} have their usual meanings and refer to the quantities for a unit transconductor. The QS model of the programmable transconductor, shown in Figure 4.4 is constant-C scaled since *all* the (trans)conductances scale with the bandwidth setting k, while *all* the capacitances are unaltered. If the simple QS model is valid, a Gm-C filter built using such transconductors will also be constant-C scaled, and if the filter is design centered for one bandwidth setting, the shape of the response is preserved for all bandwidth set-

tings. However, the frequency limit of validity for the simple QS model is found to be proportional to the quantity -

$$\omega_o = \frac{\mu_o(V_{GS} - V_T)}{\alpha L^2} \tag{4.1}$$

A safe limit on the frequency of validity is considered to be $0.1\omega_o$ (Tsividis (1999)). For the transistors used in this work, ω_o turns out to be about 41 Grad/sec ($f_o \approx 6.5$ GHz).

From (4.1), the upper limit on the frequency of validity is proportional to $1/L^2$. Therefore, in principle, it is possible to model the transistor for frequencies above the safe limit by splitting the transistor into several sections (Tsividis (1999), Scholten *et al.* (1999)). The length of each section is chosen such that the QS model is valid for that section. However, care should be taken for the internal sections so that no extrinsic capacitances exists at their terminals and no short-channel effects are introduced. Therefore, when using existing SPICE models, one need to modify these models for fitting them to the transistors of the sections (a tricky proposition). Therefore this method of modeling the transistor for higher frequencies is usually not adopted by circuit designers.

4.1.2 A Complete QS Model for the Programmable Transconductor

A complete QS small signal model for the MOS transistors is given in (Bagheri and Tsividis (1985), Tsividis (1999)). It is a more precise model in the sense that, it has an improved upper limit on frequency of validity of about ω_o/3 (Bagheri and Tsividis (1985)). For a transistor operating in saturation, with source and bulk incrementally grounded, the model reduces to a form shown in Figure 4.5. C_m is the transcapacitance.

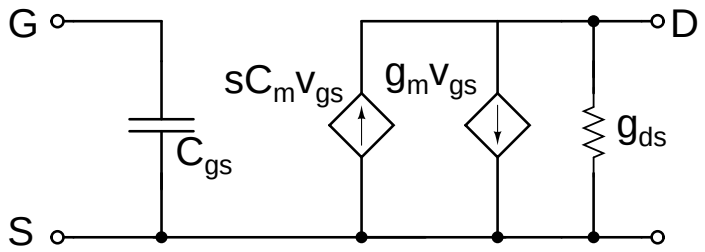


Figure 4.5: Complete QS small signal model of a MOSFET operating in saturation

In saturation region the value of C_m can be shown to be $\frac{4}{15}C'_{ox}WL$ (Tsividis (1999), where C'_{ox} is the gate oxide capacitance per unit area. Note that the transconductance of the complete QS model is $g_m(1 - s\tau_1)$, where $\tau_1 = \frac{C_m}{g_m}$. Considering the complete QS model for the transistors for M1 and M2 of the unit g_m-cell, the intrinsic small signal model of the transconductor can be drawn as in Figure 4.6.

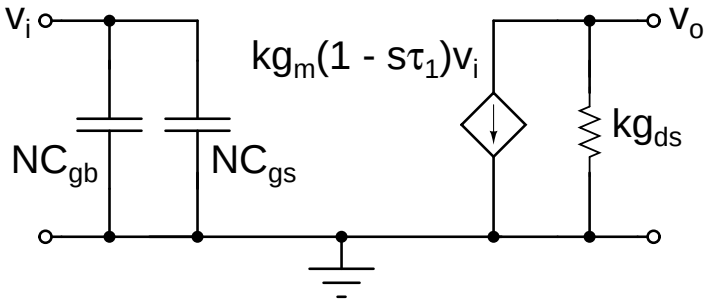


Figure 4.6: Intrinsic small signal model of the programmable transconductor. A complete QS model is assumed for the transistors

The transfer function of a Gm-C filter built using such transconductors, will be a function of $g_m(1 - s\tau_1)$ and the integrating capacitors and can be written as,

$$TF_{qs1}(s) = H\left(\frac{sC}{kg_m(1 - s\tau_1)}\right) \tag{4.2}$$

Comparing (4.2) with transfer function of an ideal filter $TF_i(s) = H\left(\frac{sC}{kg_m}\right)$, it is seen that $TF_{qs1}(s)$ can be obtained by replacing s in $TF_i(s)$ by $\frac{s}{(1-s\tau_1)}$. In other words, the ideal filter transfer function can be transformed to a QS transfer function by using the

transformation

$$\omega \rightarrow \left(\frac{j\omega}{1-j\omega\tau_1}\right) \tag{4.3}$$

$$\rightarrow -\frac{\omega^2\tau_1}{1+(\omega\tau_1)^2} + j\frac{\omega}{1+(\omega\tau_1)^2} \tag{4.4}$$

The frequency response $TF_{qs1}(j\omega)$ of the filter can be thought of as $TF_i(s)$ evaluated along the contour $\left(-\frac{\omega^2\tau_1}{1+(\omega\tau_1)^2} + j\frac{\omega}{1+(\omega\tau_1)^2}\right)$.

We now explain the effect of assuming the complete QS model for the transconductor on the magnitude response of the filter. We take the example of a fifth order filter. For the simplicity of analysis assume $(\omega\tau_1)^2 \ll 1$. The transformation in (4.4) simplifies to $-\omega^2\tau_1 + j\omega$. A graphical intuition is provided in Figure 4.7 (Pavan (2004*b*)). $p1$, $p2$, $p2^*$, $p3$, $p3^*$ are the five poles of the filter. A response along the $j\omega$-axis will give us the magnitude response of the ideal filter, that is $|TF_i(j\omega)|$. By definition, the magnitude response at a point $j\omega_x$ in Figure 4.7(a) can be written as,

$$|TF_i(j\omega_x)| = \frac{1}{a \times b \times c \times d \times e} \tag{4.5}$$

a, b, c, d, e are the lengths of the vectors from the poles $p1$, $p2$, $p2^*$, $p3$, $p3^*$ respectively to ω_x, the point at which the response is evaluated. To evaluate the complete magnitude response, the $|TF_i(j\omega)|$ should be evaluated at all the points on the $j\omega$ axis.

The magnitude response of the filter assuming the QS model ($|TF_{qs1}(j\omega)|$), is evaluated in a similar fashion but along the contour $-\omega^2\tau_1 + j\omega$ as shown in Figure 4.7(b).

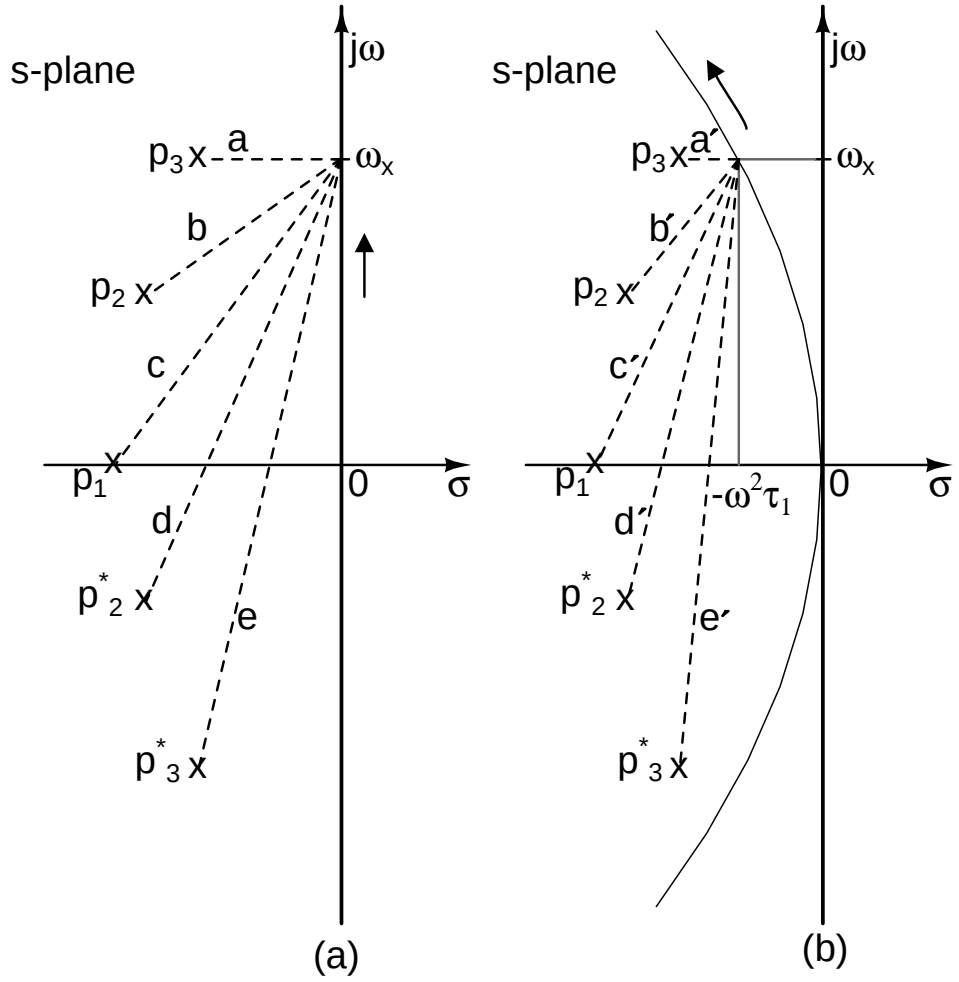


Figure 4.7: Evaluation of (a) $TF_i(j\omega)$ and (b)$TF_{nqs}(j\omega)$ of a fifth order all-pole filter

$|TF_{qs1}(j\omega_x|$ is given as

$$|TF_{qs1}(j\omega_x)| = \frac{1}{a' \times b' \times c' \times d' \times e'} \tag{4.6}$$

It can be noted from (4.5) and (4.6) that $|TF_{qs1}(j\omega_x)| > |TF_i(j\omega_x)|$. Since the transformed contour is always to the left of the $j\omega$-axis, we can generalize the result that $|TF_{qs1}(j\omega)| > |TF_i(j\omega)|$.

In Figure 4.7(b), the poles are closer to the transformed $j\omega$-axis, with the highest pole pair (p_3 and p_3^*) being the closest. This enhances the Q of the poles resulting

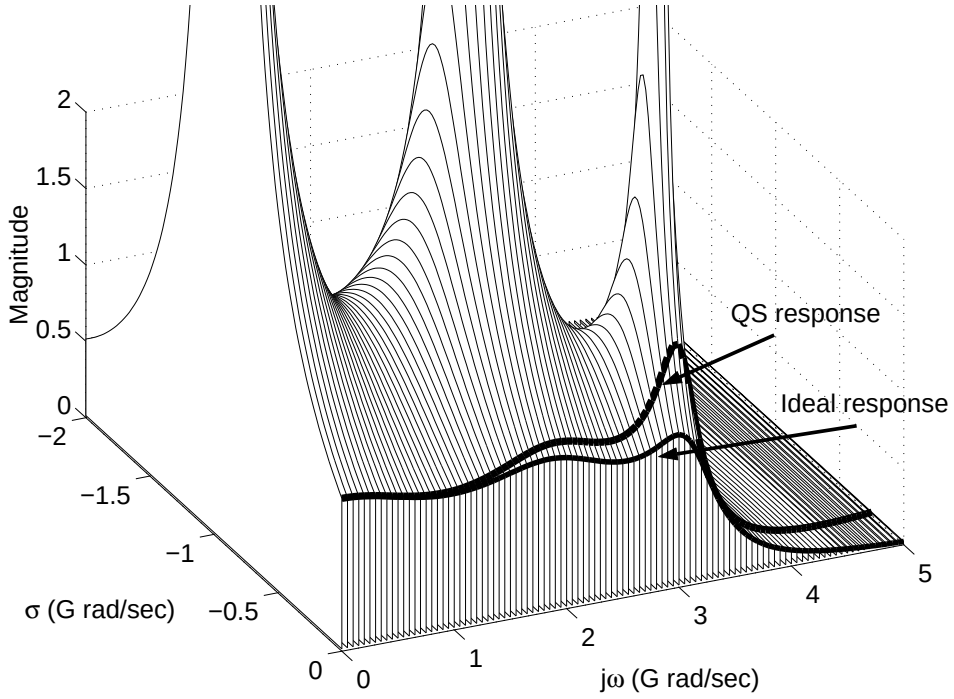


Figure 4.8: A 3-D plot illustrating the Q-enhancement in the filter when the QS model is considered

in peaking of the response. The deviation of $|TF_{qs1}(j\omega)|$ from $|TF_i(j\omega)|$ is maximum near the bandedge of the filter. This is illustrated with a 3-D plot in Figure 4.8. In figure, $|TF_i(s)|$ of a fifth order Chebyshev filter, having a bandwidth of 500 MHz, is plotted. The -ve real part and +ve imaginary part of s are only considered. The ideal response $|TF_i(j\omega)|$ of the filter is the shape obtained when the surface plot of $|TF_i(s)|$ is sliced along the $j\omega$-axis. The QS response ($|TF_{qs}(j\omega)|$) is obtained by slicing $|TF_i(s)|$ along the contour $-\omega^2\tau_1 + j\omega$. The so obtained ideal and QS frequency responses are shown in the figure. In this example τ_1 is assumed to be 10 ps. Clearly we can see the peaking in the magnitude response of the filter when the QS behaviour is considered.

Using the complete QS model for the programmable transconductor one can predict the filter behaviour at higher frequencies. However, some aspects of the filter performance are not satisfying. The complete QS model predicts that as $s \rightarrow \infty$, the transconductance $g_m(1 - s\tau_1) \rightarrow -\infty$ which seems fundamentally incorrect. Another

point is that for $s \rightarrow \infty$, the transformed contour $\left(\frac{j\omega}{1-j\omega\tau_1}\right)$ approaches $-\frac{1}{\tau_1}$ and therefore, $TF_{qs}(j\infty)$ approaches a constant. These seemingly strange results are due to the use of QS models beyond its region of validity (approximately ω_o/3) (Bagheri and Tsividis (1985)). For higher frequencies it is necessary to consider the non-quasi-static operation of the transistors.

4.1.3 Non-quasi-static model for the programmable transconductor

A first-order small-signal model for a four-terminal long channel MOSFET valid upto the frequency of about ω_o is presented in (Bagheri and Tsividis (1985)). For the detailed derivation/discussion of this model the reader is referred to (Tsividis (1999)). For a transistor operating in saturation with source and bulk terminals incrementally grounded, the high frequency model presented in (Bagheri and Tsividis (1985)) simplifies to a form as shown in Figure 4.9.

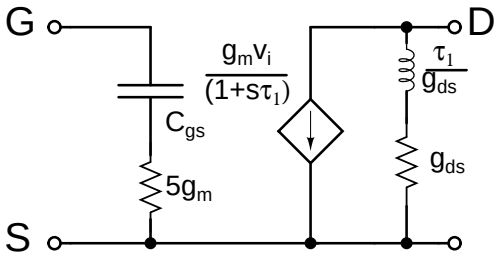


Figure 4.9: An intrinsic small signal model of a MOSFET operating in saturation with bulk and source terminals at the same potential, valid for high frequencies

The finite time lag in the channel charges is modelled by a pole at $1/\tau_1$ and can be shown to be $\frac{15}{4}\frac{g_m}{C_{gs}}$. Note that, τ_1 used here is same as the time constant τ_1 used in the complete static model with the assumption $C_{gs} = \frac{2}{3}C_{ox}$.

When the NQS model is used for the transistors M1 and M2 in Figure 4.2, the small signal model for the programmable transconductor can be drawn as shown in

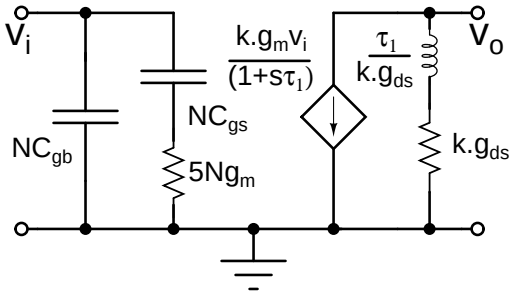


Figure 4.10: The intrinsic model of the programmable transconductor considering NQS effects

Figure 4.10. As k is changed, *all* the conductances *do not* scale with k. Therefore the transconductor is no longer constant-C scaled. Note specifically that the transconductance g_m has a finite bandwidth associated with it. The input capacitance of the transconductor is no longer lossless. The output conductance has an inductor in series with it. However, even when the filter bandwidth is a significant fraction of the f_T of the transistor, it is found from simulations that the deviations in filter response due to the conductance of $5Ng_m$ in series with C_x and the inductor in the drain are insignificant in comparison to the "finite bandwidth" of the transconductance. This makes sense because, at frequencies when the reactance of C_x and reactance of inductor becomes comparable to the resistances $1/5Ng_m$ and $1/g_{ds}$ respectively, the parasitic capacitances existing in parallel to them will have a much lower reactance. Figure 4.11 shows the magnitude response of the filter model designed in chapter 2 with and without the inductor and the gate resistance. It is seen that the effects of the conductance $5Ng_m$ (denoted as resistor R_{gs}) and the inductor $\frac{\tau_1}{k.g_m}$ (denoted as L_{ds}) are negligible.

Considering only the finite bandwidth of the transconductor, the transfer function of the filter can be written as a function of $kg_m/(1+s\tau_1)$ and the integrating capacitors in a form

$$TF_{nqs}(s) = H\left(\frac{sC(1+s\tau_1)}{k.g_m}\right) \tag{4.7}$$

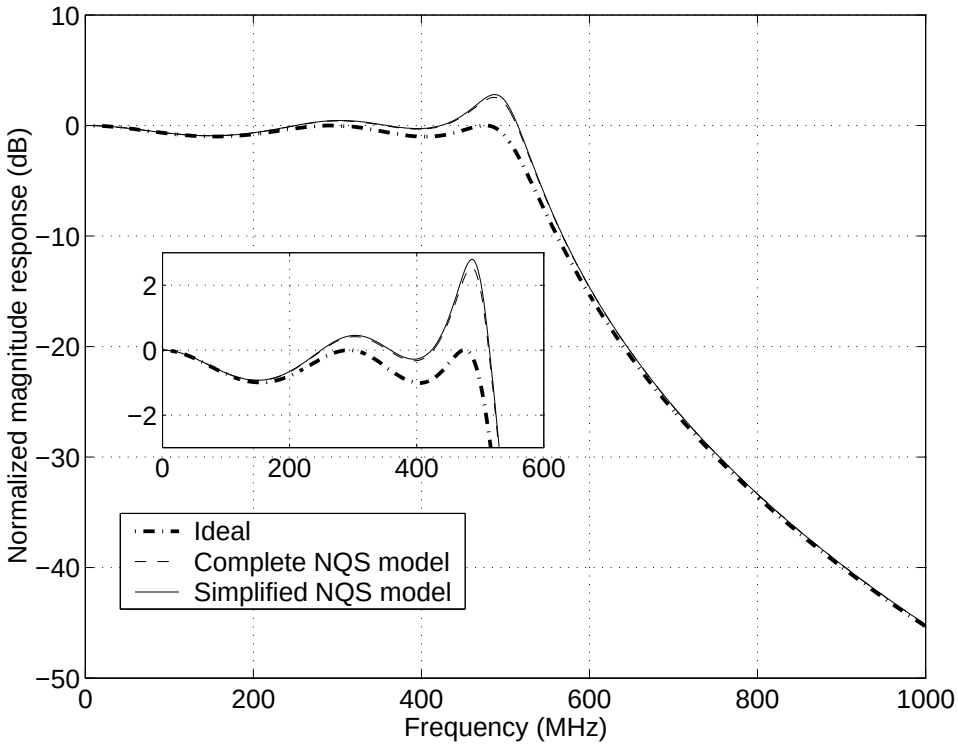


Figure 4.11: Effect of R_{gs} and L_{ds} in the NQS model of the transistor on the magnitude response of the fifth order Chebyshev ladder filter. The complete NQS model includes the effect of R_{gs} and L_{ds} in addition to the pole in transconductance, while in the simplified model R_{gs} and L_{ds} are neglected.

Defining $s_{nqs} = s(1 + s\tau_1)$ we can write,

$$TF_{nqs}(s) = H\left(\frac{s_{nqs}C}{k.g_m}\right) \tag{4.8}$$

Proceeding in a similar fashion as done for the complete QS model, the transfer function $TF_{nqs}(s)$ can be obtained from the ideal transfer function $TF_i(s)$ using the transformation

$$s = s(1 + s\tau_1) \tag{4.9}$$

$$\text{Or} \qquad j\omega_{nqs} = j\omega\left(1 + j\omega\tau_1\right) \tag{4.10}$$

$$= j\omega - \omega^2\tau_1 \tag{4.11}$$

Therefore, the magnitude response $|TF_{nqs}(j\omega)|$ of the filter with NQS effects can be thought of as $TF_i(s)$ evaluated along the contour $j\omega - \omega^2\tau_1$. Recall that when the complete QS model was considered, the transformation simplified to the same form as in (4.11) for $(\omega\tau_1)^2 \ll 1$. This is because, at frequencies much lower than $1/\tau_1$, complete QS model is valid. A plot of the contours of (4.4) for the complete QS model

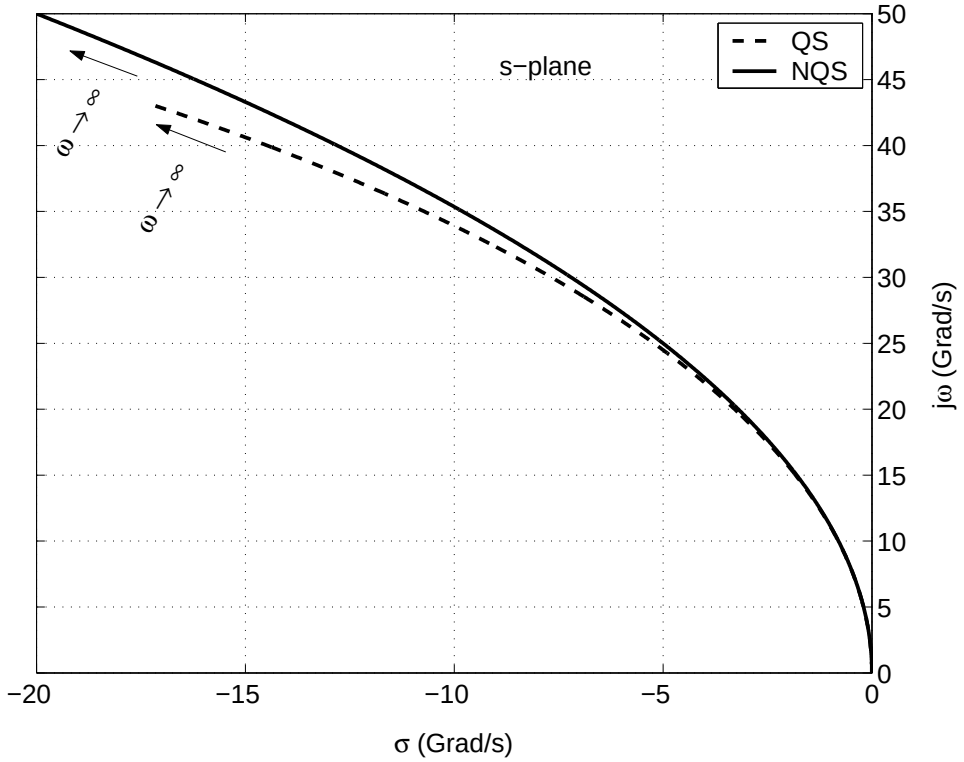


Figure 4.12: Shift in the $j\omega$-axis due to the QS behaviour and the NQS behaviour of transconductors

and (4.11) for the NQS model are shown in Figure 4.12 for ω ranging from zero to 50 Grad/s. It is evident that if the QS model is used, the resulting response will be in error at high frequencies. Observe that the QS contour is always to the left of the NQS contour. This means, for any bandwidth setting, the response of the filter with the QS model will have a higher peaking than for a filter with the NQS model.

Figure 4.13 compares the magnitude responses of a fifth order Chebyshev Gm-C filter model when the complete QS model and NQS model are considered for the pro-

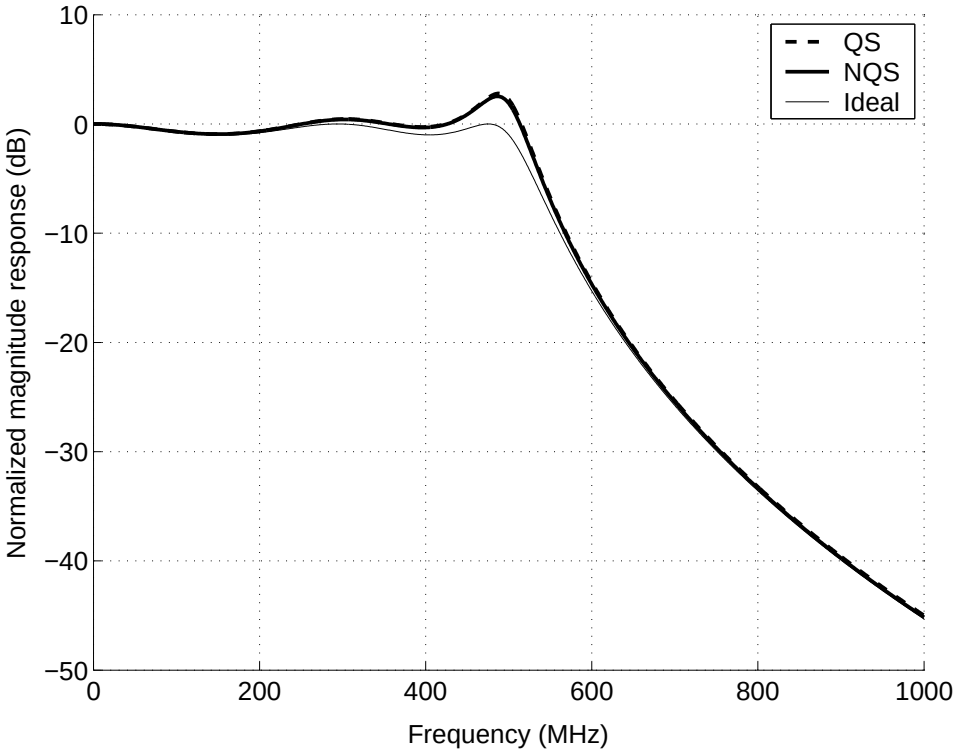


Figure 4.13: Comparison of the magnitude responses of the fifth order Chebyshev ladder filter model considering the complete QS model and NQS model for the programmable transconductor.

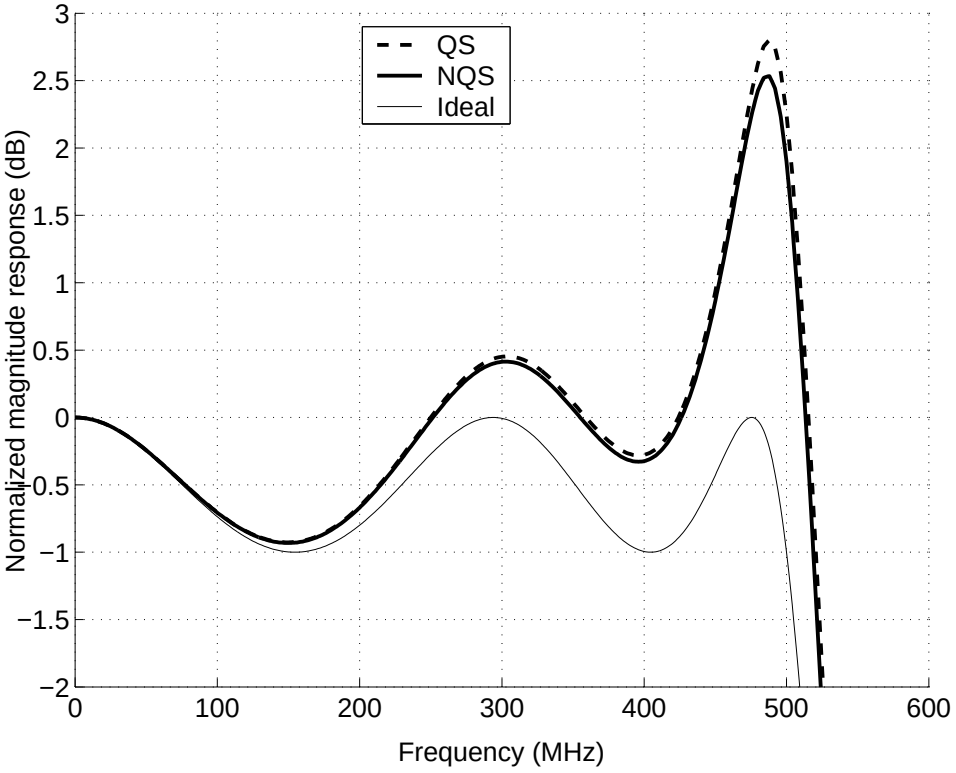


Figure 4.14: Passband detail of Figure 4.13

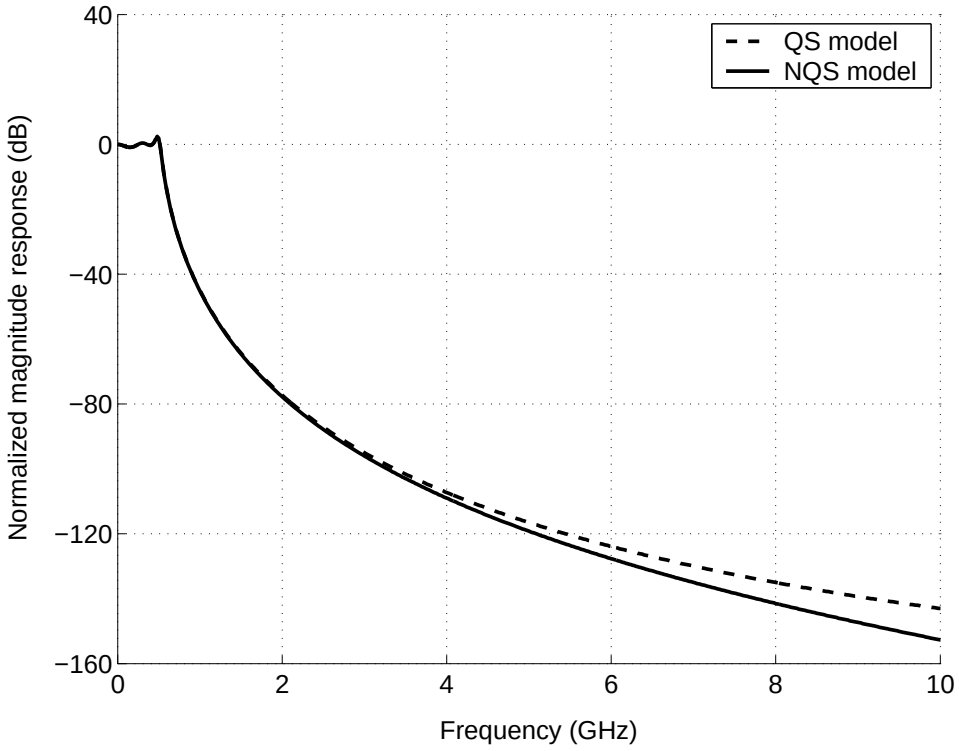


Figure 4.15: Stopband detail of Figure 4.13 plotted up to 10 GHz

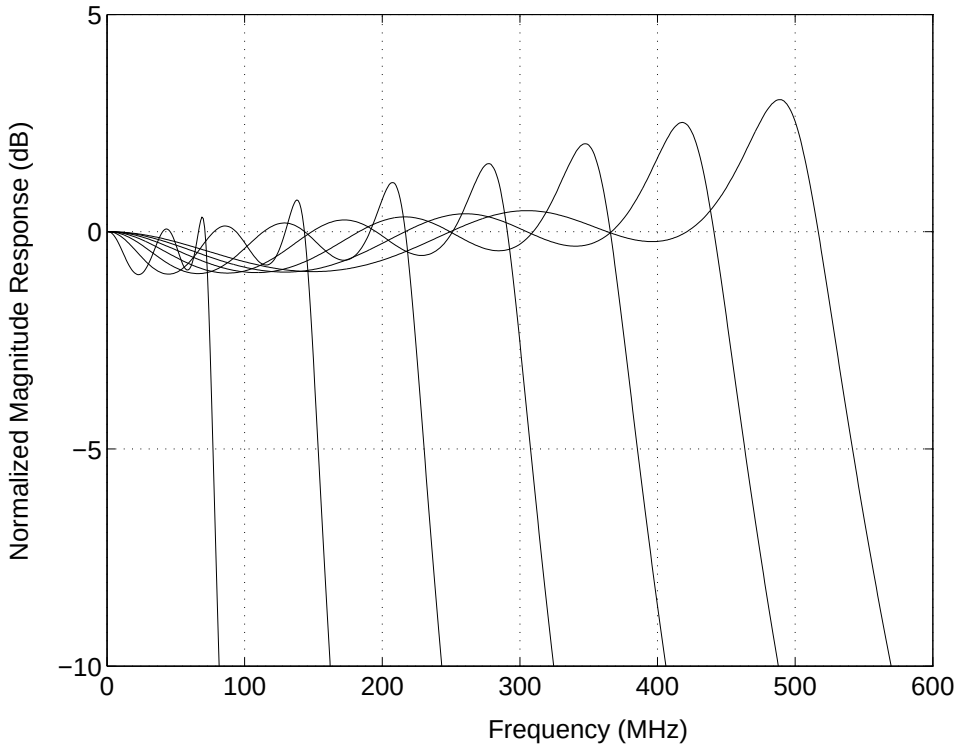


Figure 4.16: Magnitude response of the filter model across the bandwidth settings when NQS effects are considered - Passband details

grammable transconductor. Figure 4.14 shows the passband detail of Figure 4.13. Notice that with the QS model, the response peaks higher than for the NQS model as expected. Figure 4.15 shows the stopband comparison upto 10 GHz. At higher frequencies, the error between the QS model response and the NQS model response increases. The error is about 10 dB at 10 GHz. Though not important it practice, it remains an interesting theoretical point.

Recall that the NQS model (and also the complete QS model) for the programmable transconductor is not constant-C scaled. The result is that the shape of the filter frequency response varies with the bandwidth setting, as shown in Figure 4.16. It is seen that the peaking in the response is bandwidth dependent, which is not desirable. The following section presents a simple compensating strategy.

4.2 COMPENSATING FOR MOS NQS EFFECTS - A BIQUAD EXAMPLE

For simplicity, we explain our technique using a biquad example. The same reasoning can be extended to more complex filter topology like a ladder.

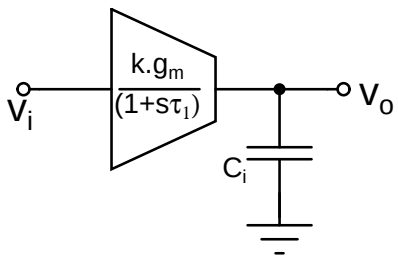


Figure 4.17: Simplified schematic of an integrator incorporating MOS NQS effects.

Consider a Gm-C integrator as shown in Figure 4.17. The NQS effect of the transconductor is modeled with a pole at $1/\tau_1$. For simplicity, it is assumed that g_m/g_{ds} is large, so that the effects of g_{ds} can be neglected to first order. Denoting the total integrating

capacitance (intentional and parasitic) by C_i, the excess phase lag of the integrator at its unity-gain frequency $k\frac{g_m}{C_i}$ is given by

$$\Delta\phi_e = \tan^{-1}\left(\frac{4k}{15}\frac{C_{gs}}{C_i}\right) \tag{4.12}$$

From (4.12), it is clear that the excess phase of the integrator is bandwidth dependent. In a biquad formed using two such integrators, Q enhancement due to the excess phase in the transconductors increases with bandwidth setting. However, it can be seen that for a given bandwidth setting, the excess phase will remain independent of temperature if C_i is of the same kind as C_{gs}. This is easy to achieve if MOS accumulation capacitors are used as the integrating capacitors. This makes MOS accumulation capacitors *the* choice for integrating capacitors in the filter designed in this thesis (in addition to their high density, mentioned in Chapter 2).

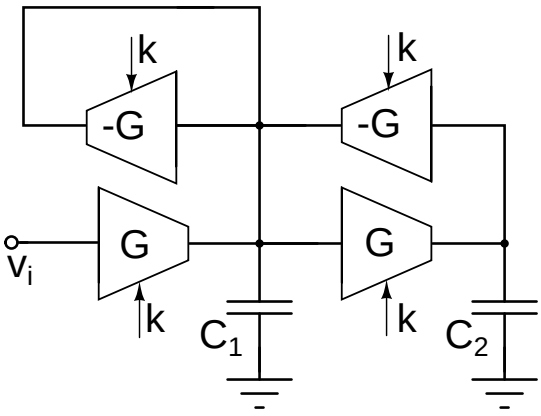


Figure 4.18: Gm-C biquad

Figure 4.18 shows a biquad formed using the integrator shown in Figure 4.17. C_1 and C_2 represent the *total* capacitance at the integrating nodes. If NQS effects were

absent, the center frequency f_o & Q of the biquad would be

$$f_o = \frac{1}{2\pi}\frac{kg_m}{\sqrt{C_1C_2}} \tag{4.13}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \tag{4.14}$$

When NQS effects are considered, f_o & Q are modified from the intended values, in a bandwidth dependent fashion. The modified f_o & Q can be approximated (Appendix A) as the following:

$$f_o' \approx f_o\left(1 - \frac{\pi f_o \tau_1}{Q}\right) \tag{4.15}$$

$$Q' \approx \frac{Q}{1 - 4\pi f_o Q \tau_1} \tag{4.16}$$

The set bandwidth f_o is of the form $2\pi k\frac{g_m}{C_i}$ and τ_1 is of the form $\frac{4}{15}\frac{C_{gs}}{g_m}$. Hence the product $f_o\tau_1$ depends only on ratios of like elements and is stable with temperature. It is thus seen from (4.16) that even though Q is modified from the ideal value depending on the bandwidth setting k, it does not change with temperature. Another key point is that since $f_o\tau_1$ and Q are stable with temperature, f_o' can be stabilized over temperature using a transconductance servo loop.

4.2.1 Biquad - Compensating for NQS effects

Compensating for NQS effects means restoring f_o and Q to their intended values and can be done by appropriately modifying C_1 and C_2. This modification must be a function of the bandwidth setting k. This is accomplished by the digitally programmable capacitor banks $\Delta C_1(k)$ and $\Delta C_2(k)$. These capacitors are implemented

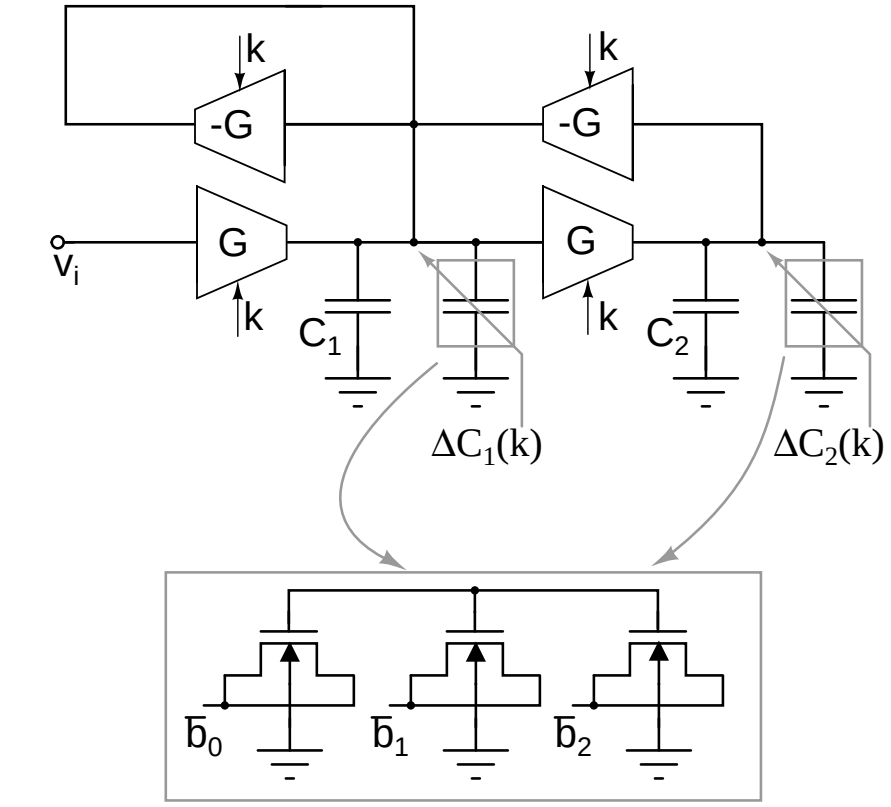


Figure 4.19: Gm-C biquad: compensating strategy

using three terminal NMOS structures with drain and source connected together to the control bit as shown in the inset of Figure 4.19.

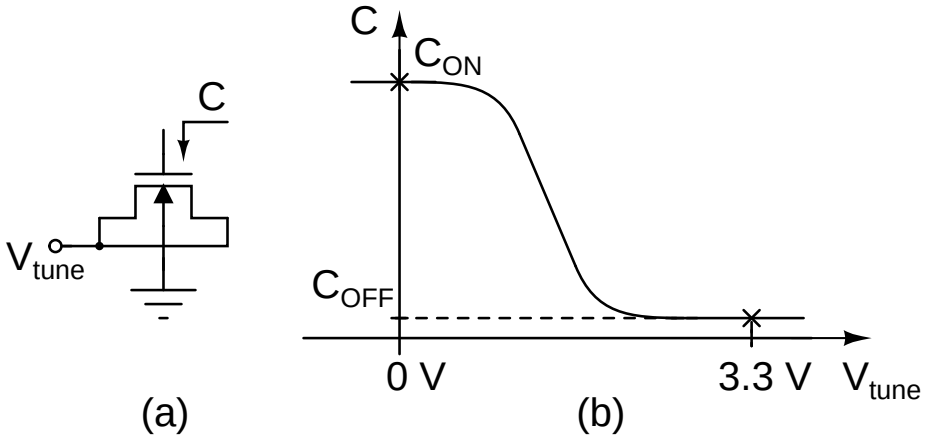


Figure 4.20: (a) Unit NMOS capacitor used for the ΔC (b) C-V curve of the unit NMOS capacitor in (a), showing the operating regions

For a unit MOS structure, when the drain/source terminal is connected to ground, the capacitance is high. Let us denote the resulting capacitance by C_{ON}. When the drain is

connected to Vdd, the capacitance is low since a channel cannot be formed. Denote this capacitance by C_{OFF}. The operating regions are shown in Figure 4.20. If the capacitor bank has M number of NMOS capacitors and if m is the number of capacitors that are ON for a given bandwidth setting k, the effective capacitance offered by the capacitor bank is given by

$$\Delta C(k) = mC_{ON} + (M-m)C_{OFF} \tag{4.17}$$

$$= m(C_{ON} - C_{OFF}) + MC_{OFF} \tag{4.18}$$

From (4.18), the component MC_{OFF} in $\Delta C(k)$ is independent of bandwidth setting k and the component $m(C_{ON} - C_{OFF})$ is dependent on k. For each k, one can determine the required number (m) of NMOS capacitors to be turned ON in ΔC_1 and ΔC_2 that would restore the values of f_o and Q. Note, since ΔC_1 and ΔC_2 are of the same kind as the integrating capacitors, f_o and Q will not vary with temperature.

Table 4.1: Example for the strategy to find ΔC to compensate for the MOS NQS effects.

Bandwidth	δn	δn_1	$m = \frac{\delta n_1 C_{ON}}{C_{ON} - C_{OFF}}$
001	10 $\uparrow$	14	20
010	7 $\uparrow$	11	16
011	5 $\uparrow$	9	13
100	2 $\uparrow$	6	9
101	0	4	6
110	2 $\downarrow$	2	3
111	4 $\downarrow$	0	0

The procedure for finding the ΔC-banks can be explained for the biquad as follows.

1. Compute the frequency response of the layout extracted filter for each bandwidth setting considering NQS effects. The BSIM3v3 model for the transistors provide a parameter *nqsmod* for turning the NQS effects on. Several foundries do not provide this switch in their models, as it is not important for most applications. In that case, the channel charge partition can be modified to use the QS model of

Figure 4.5 instead of the simple model of the Figure 4.3. Though the QS model is not quite accurate at high frequencies, it is sufficiently precise to predict the shape of the filter response, as shown in Figure 4.13.

2. For each bandwidth setting, compute the capacitances to be added/removed in the integrating nodes so as to bring the response back to the desired. One example for finding ΔC (say ΔC_1) is given in Table 4.1. Column-2 shows the number of unit capacitors (denoted as δn) to be added/removed in the integrating node-1. '$\uparrow$' and '$\downarrow$' indicate that the capacitors should be added and removed respectively.

   At a given integrating node, capacitance may need to be added for some bandwidth settings, while it may need to be removed for the remaining bandwidths. However, ΔC banks which are realized using 3-terminal NMOS structures can only add the capacitances.

   This is taken care by adding/removing an appropriate number of unit capacitors in C_1 and C_2, so that the capacitance to be realized using ΔC banks monotonically increase/decrease with the bandwidth setting.

   In the example table, we choose to remove 4 unit capacitors from node-1. The resulting number of unit capacitors to be realized from the ΔC_1 bank is listed in column-3 (δn_1). Observe that δn_1 is monotonically decreasing for this case. Column-3 tells us that, for each bandwidth setting, one need to add capacitance equal to $\delta n_1 \times C_{ON}$ using the ΔC_1 bank (assuming that the unit capacitance of C_1 is equal to C_{ON} of the unit NMOS capacitor).

3. From (4.18), it is known that adding a unit NMOS capacitor to a node increments the capacitance at that node by ($C_{ON} - C_{OFF}$). Therefore, we need to find the number of unit NMOS capacitors (m) required to realize the desired capacitance in ΔC (i.e. $\delta n_1 \times C_{ON}$) for each bandwidth setting. This number can be found using $m = \delta n_1 C_{ON}/(C_{ON} - C_{OFF})$ and approximating the result to the nearest integer. This is shown in column-4 of table where C_{ON} and C_{OFF} are assumed to be 20 fF and 6 fF respectively.

4. Decide upon the suitable strategy to switch-in the desired number of unit NMOS capacitors in ΔC_1 and ΔC_2 (calculated in the previous step), using the programmable structure shown in the inset of Figure 4.19. For the example shown, the best strategy would be to switch 13, 6 and 3 unit NMOS capacitors using the bandwidth setting bits b_2, b_1 and b_0 respectively.

5. If M is the total number of unit NMOS capacitors in ΔC_1 branch, the fixed capacitance MC_{OFF} must be taken into account by subtracting an equal capacitance from C_1. Similar adjustment should be done for the other node also. For the example, the number of unit capacitors to be removed from C_1 can be computed as $(16 + 6 + 3)\mathrm{C_{OFF}}/\mathrm{C_{ON}} = 6$ fingers.

6. Repeat the steps 1 & 2. If the capacitors to be added/removed are more than the unit capacitor, then repeat the steps 3 through 7.

The idea presented for the Gm-C biquad can be extended to more complex architec-

tures like the ladder filter used in this thesis. With the efficient design centering technique (presented in the chapter 3), one can easily compute the values of ΔC required for each bandwidth setting.

Q enhancement is traditionally handled using complex Q-tuning loops (see for example, Stevenson and Sanchez-Sinencio (1998)). These techniques are not only complex and have an area overhead but also suffer from clock feedthrough. The proposed technique accomplishes the same objective, using a DC servo loop (which is needed anyway to stabilize f_o). It is a simple and area efficient technique. This is possible because the integrator high frequency pole (occurring due to NQS effects) tracks the unity gain frequency (thanks to the use of accumulation MOS capacitors as integrating elements).

4.3 SIMULATION RESULTS

The technique presented in the previous section has been used to compensate for MOS NQS effects on the 5^{th} order ladder filter designed in Chapter 2.

The layout extracted filter is simulated by setting the flag *nqsmod=1* in the MOSFET model files. The resulting response is plotted in Figure 4.21 for all bandwidth settings. These responses are used for correcting for the NQS effects.

Figure 4.22 show the response of the filter after correction. Notice that all the peaks in the responses are brought back to 0 dB. The variations in the first minima of pass band is due to the minimum realizable unit capacitor. The proposed theory is borne out by experimental results from the fabricated chips. These measurements are presented in chapter 6.

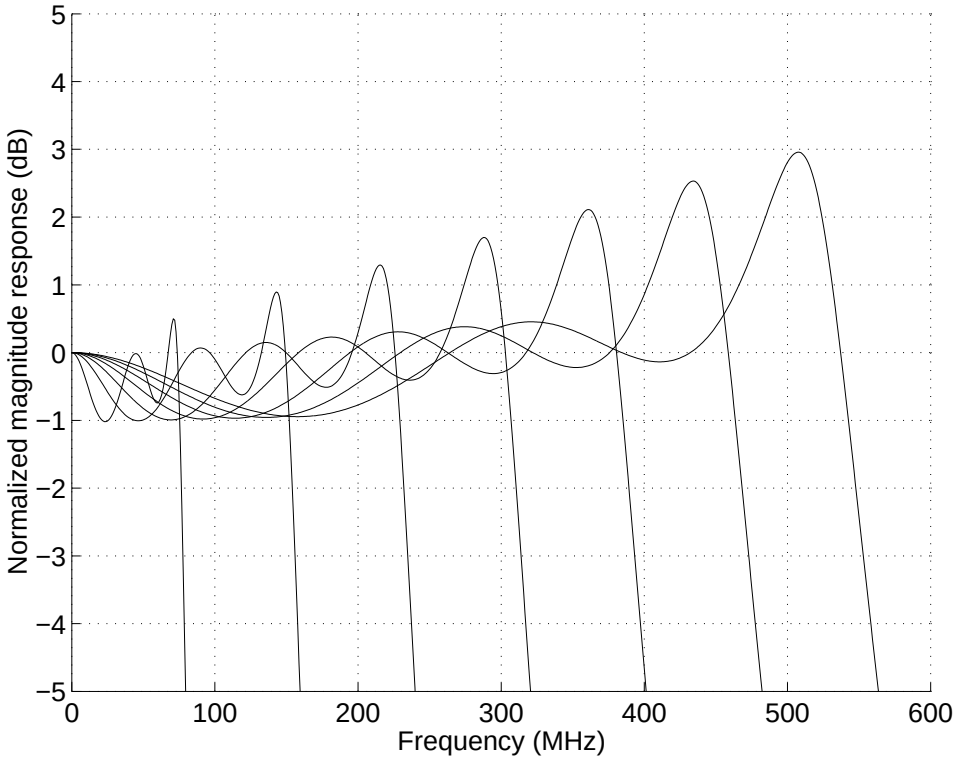


Figure 4.21: Normalized magnitude response of the layout-extracted filter without NQS compensation.

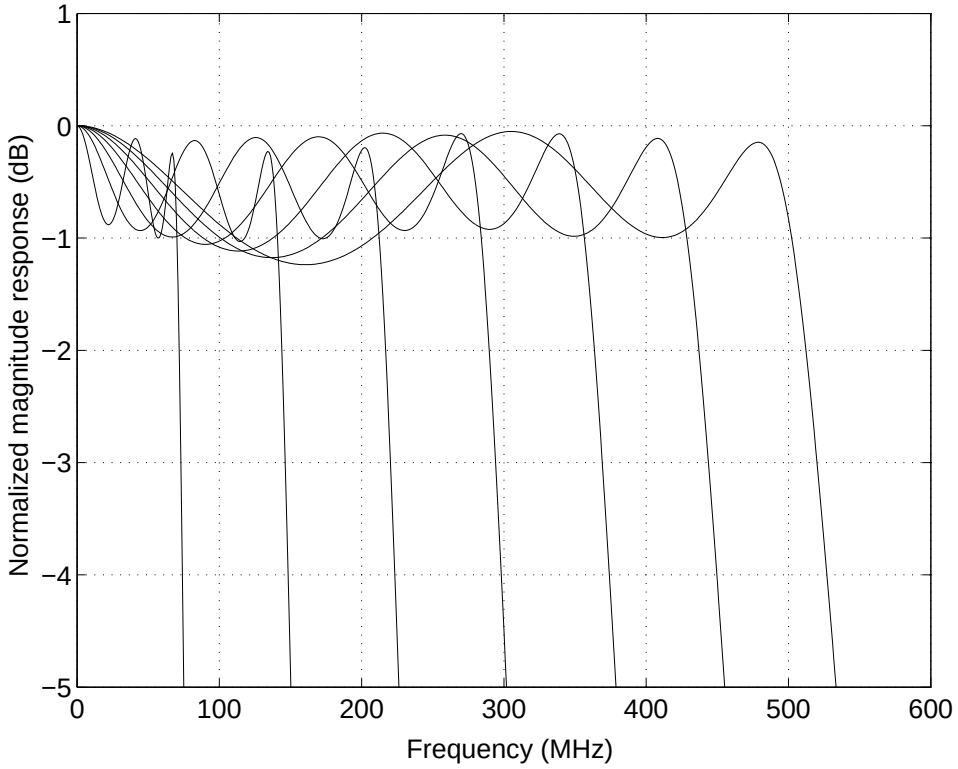


Figure 4.22: Normalized magnitude response of the layout-extracted filter with NQS compensation.

CHAPTER 5

ACCURATE CHARACTERIZATION OF ON-CHIP INTEGRATED FILTERS

Integrated filters are not stand alone devices, but intended to be embedded parts of a complete on-chip analog front end. Hence, they are not designed to drive parasitics due to the package and test board. When characterizing the filter in packaged chips, the effects of the package must be de-embedded from the response of the filter. The characterizing procedures should be able to accurately measure the filter frequency response both in the passband and the stopband.

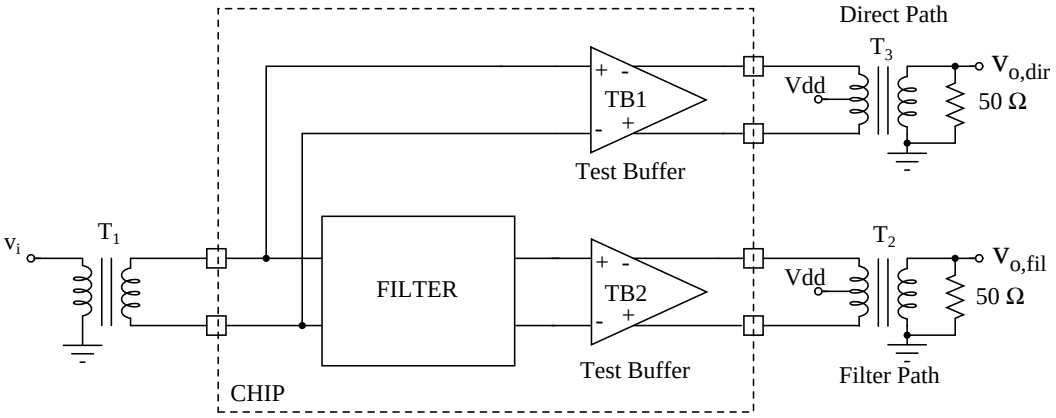


Figure 5.1: Conventional on-chip filter measurement test setup.

A common technique, originally proposed by Nauta (1992), employed for on-chip filter characterization is shown in Figure 5.1. The filter to be tested is assumed to be fully differential. Transformer T1 converts the single-ended stimulus (from the test equipment) into a fully differential signal that excites the filter. Since the filter is not designed to drive external loads, two nominally identical on-chip test buffers TB1 and

TB2 are used. These test-buffers, which are biased with sufficiently large currents so that external loads can be driven, are only activated during characterization. TB1 senses the input of the filter and forms the direct measurement path, while TB2 senses the filter output. T2 and T3 convert the test-buffer outputs into single-ended signals that are measured by the test instruments. The test buffers, IC package and board parasitics have a frequency response that must be de-embedded in order to obtain the true filter response. The following assumptions are made regarding the test-setup.

a. TB1 & TB2 are matched.
b. The measurement paths at the outputs of TB1 & TB2 are identical.
c. The input impedance of TB1 & TB2 is negligible.
d. The reverse transmissions of the filter, TB1 & TB2 are negligible in the frequency range of interest.

Assumption (a) is reasonable. (b) is a bit harder to achieve, since the designer has little control over the package. (c) can be enforced by design, and is necessary anyway as the test-buffers should not load the signal path. As for (d), the usually used active filter and test buffer topologies can easily achieve reverse isolations of 90-100 dB even at high frequencies. The signal flow graph (SFG) of the test setup, used to calculate $H(f)$ is shown in Figure 5.2. H_{in} is the transfer function of the input path, i.e, from v_i to the filter input. H_f is the transfer function of the filter and H_b is the transfer function from the test buffer input to the balun (T2, T3) output.

If the SFG of Figure 5.2 is valid, it is seen that the frequency response of the filter is given by

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} \tag{5.1}$$

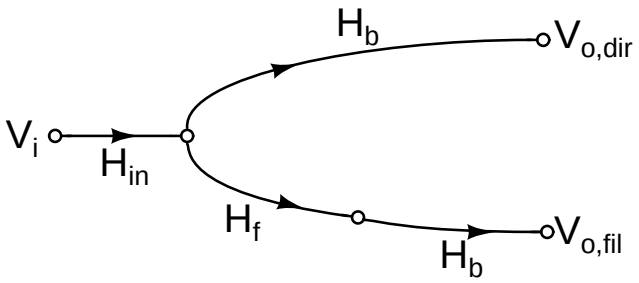


Figure 5.2: Signal flow graph of the conventional test setup.

In practice, since the magnitude response of $H_f(f)$ is of interest, a Spectrum Analyzer (SA) can be used to measure the magnitudes of $V_{o,fil}(f)$ and $V_{o,dir}(f)$. Alternately, a Vector Network Analyzer (VNA) can be used to measure the S-parameters of the filter path and direct path. It can be shown that

$$H_f(f) = \frac{V_{o,fil}(f)}{V_{o,dir}(f)} = \frac{S_{21,fil}(f)}{S_{21,dir}(f)} \tag{5.2}$$

The setup described above has the advantage of simplicity. Apparently, filters with very high bandwidth can be measured even with a very low-cost package, since all package and board parasitics are calibrated out. This technique has been the *de facto* method used to characterize filters by several workers over the years.

From the measured magnitude responses reported by various authors, the conventional test technique enables a very accurate characterization of the passband response (where $H_f(f)$ is large). However, in our experience, as well as experimental results reported in the literature (for example De Veirman and Yamasaki (1992), Pavan *et al.* (2000), Harrison and Weste (2003), Panday *et al.* (2006) Chamla *et al.* (2005)), the accuracy of the measurement in the stop-band of the filter is poor. Typically, the measured $|H_f(f)|$ does not reduce beyond -60 dB even at high frequencies, and is quite sensitive to the package and test board. The equiripple group delay filter of De Veirman

and Yamasaki (1992) has a measured stopband attenuation that does not reduce below -60 dB beyond 40 MHz. Measurements made on the fourth order Butterworth filter reported in Pavan *et al.* (2000) were only accurate for frequencies where the attenuation was less than about 60 dB. The measured stopband attenuation of the fifth order elliptic filter in Harrison and Weste (2003) was -50 dB at 300 MHz but went down to -35 dB at higher frequencies. The authors of Panday *et al.* (2006) report that the response deviates from the ideal at about 300 MHz due to test setup issues. Test setup problems are not restricted to high frequency filters - measurements of the baseband Butterworth filters reported in Chamla *et al.* (2005) show a deviation from the ideal beyond a few megahertz, where the attenuation is greater than 70 dB. Usually, such problems are attributed to the "quality of the test-setup", implicitly *assuming* that the filter itself has no problems. It is therefore seen that there is a need for a characterization technique that is also accurate in the filter stopband, and robust with respect to package properties.

Like the frequency response, the output noise spectral density of the filter is also effected by the package and board parasitics. With the technique of Figure 5.1, the measured noise spectrum will be the combination of the noise due to the filter, test-buffer and any other device (contributing noise) present in the measurement path. In order to obtain the filter noise spectral density, it is necessary to remove the effect of the package and other sources. Rizzoli and Lipparini (1985) and Pucel *et al.* (1992) presented techniques to measure the noise spectral densities of packaged two-ports. However, a multiport package model is assumed to be available (from package measurements or simulations).

In this chapter, we propose techniques for accurate characterization of on-chip ac-

tive filters, without some of the disadvantages associated with prior work as discussed above. The additional complexity introduced in the on-chip test hardware due to our techniques is negligible. Two improved techniques, one using a VNA and another using only a spectrum analyzer are proposed for the accurate frequency response measurement. A technique for the accurate measurement of the noise spectral density of the filter is also proposed.

5.1 LIMITATIONS OF THE CONVENTIONAL MEASUREMENT TECHNIQUE

An implicit assumption made in arriving at (5.1) is that there is no coupling between the three ports of Figure 5.1 (the input, direct path output and the filter path output). While this is accurate at low frequencies, the isolation between the three ports decreases with frequency. This makes sense, since the inductive coupling (through the bond-wires and PCB traces) and capacitive coupling (through the pin-to-pin & PCB inter-trace capacitance) increases with frequency. The measured isolation between the three ports of the test board used in this work to characterize the filter prototype designed in chapter 2, is shown in Figures 5.3, 5.4 and 5.5. In all these figures, the lower curve is the isolation of the board (without the packaged IC), while the upper curve shows the isolation with the IC package, but without the die. From these figures, it is seen that the package is the dominant contributor of port-to-port coupling. Note specifically that the isolation between any of the ports is only about 55 dB at 500 MHz. This means that, with this particular test setup, a filter with a stop-band attenuation better than 55 dB at 500 MHz cannot be measured accurately, since direct feedthrough due to the package dominates the filter path output. It is clear, therefore, that any characterization technique

must account for (or eliminate) spurious coupling through the package.

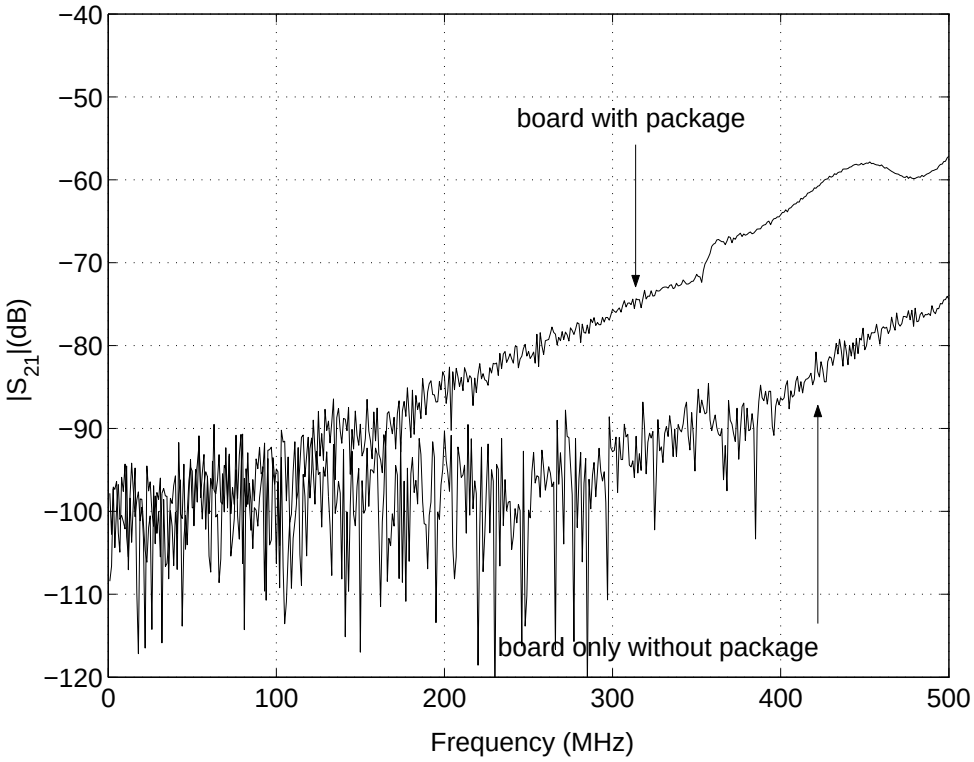


Figure 5.3: Isolation of the filter path with and without the packaged IC.

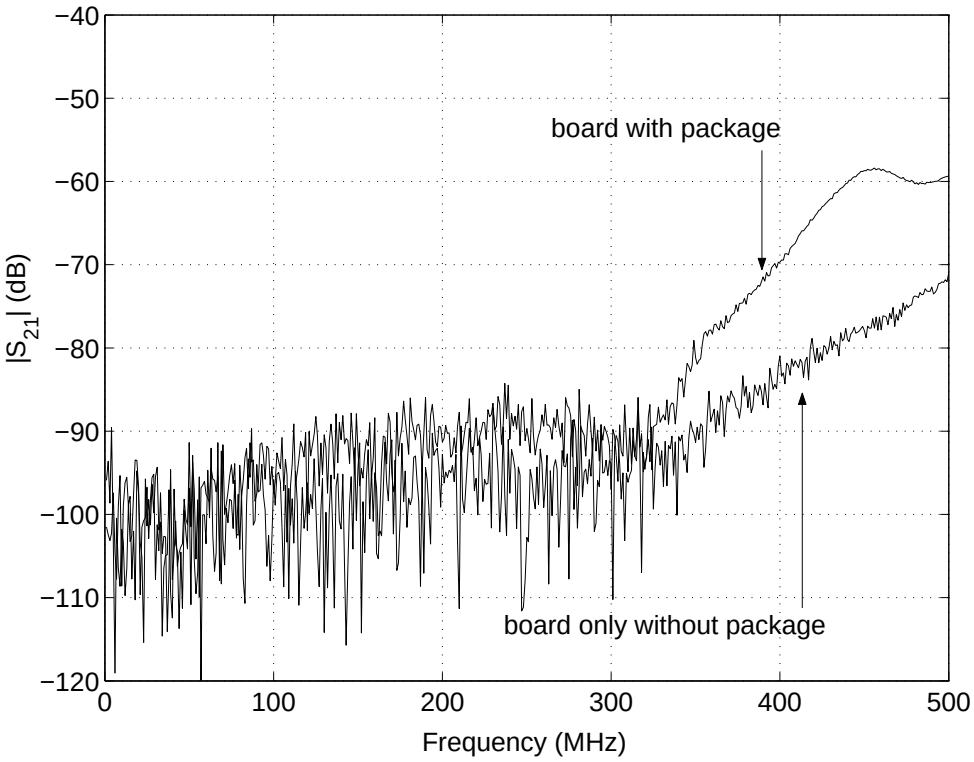


Figure 5.4: Isolation of the direct path with and without the packaged IC.

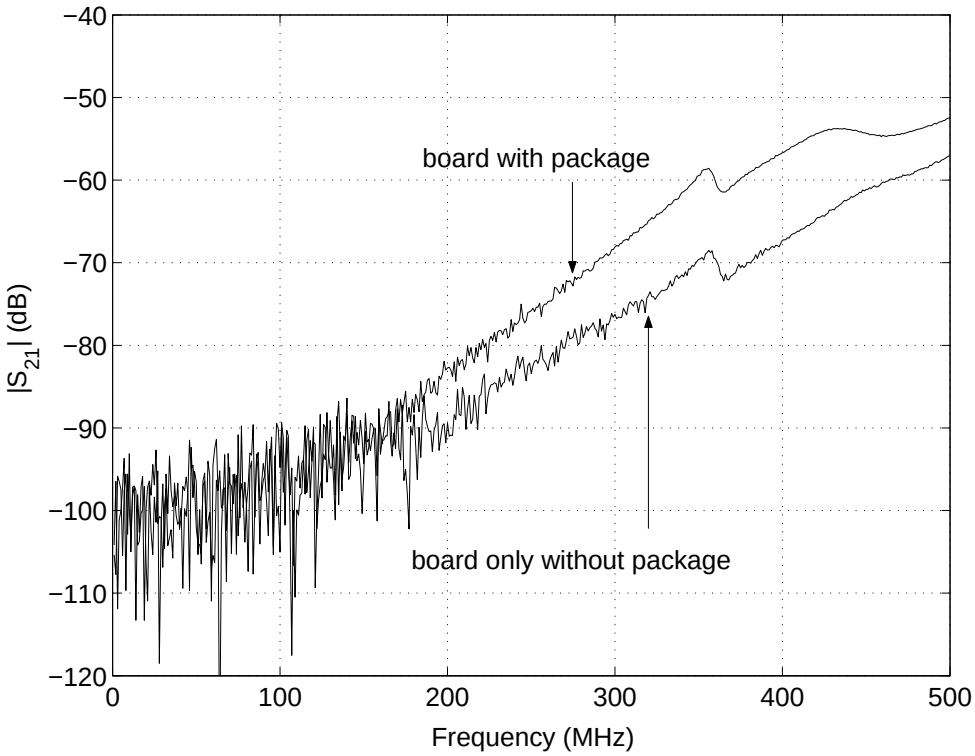


Figure 5.5: Isolation between the output ports with and without the packaged IC.

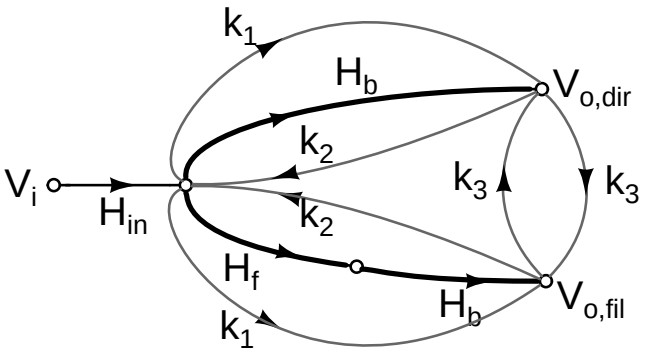


Figure 5.6: Signal flow graph with finite package isolation.

Considering package and board feedthrough, the signal flow graph of Figure 5.2 can be redrawn as in Figure 5.6. k_1, k_2 and k_3 model the package feedthrough terms. Here we assume that the output ports of TB1 and TB2 are symmetric with respect to the input port. This is not necessary (from Figure 5.3 and Figure 5.4), but makes the analysis simple and expressions less tedious. Solving the signal flow graph, and

neglecting higher powers of k_1, k_2 and k_3 (since they are small), we obtain

$$\begin{aligned}
\frac{V_{o,fil}(f)}{V_i(f)} &\approx H_{in}H_fH_b + k_1H_{in} + k_3H_{in}H_b \\
&\quad + k_2(H_{in}H_b^2H_f^2 + H_{in}H_b^2H_f) \qquad (5.3) \\
\frac{V_{o,dir}(f)}{V_i(f)} &\approx H_{in}H_b + k_1H_{in} + k_3H_bH_fH_{in} \\
&\quad + k_2(H_{in}H_b^2 + H_{in}H_b^2H_f) \qquad (5.4)
\end{aligned}$$

Clearly the ratio of (5.3) and (5.4) is no longer H_f. However, in the filter passband, the direct and filter path outputs can be approximated as follows.

$$\begin{aligned}
\frac{V_{o,fil}(f)}{V_i(f)} &\approx H_{in}H_fH_b \text{ (filter path)} \qquad (5.5) \\
\frac{V_{o,dir}(f)}{V_i(f)} &\approx H_{in}H_b \text{ (direct path)} \qquad (5.6)
\end{aligned}$$

The ratio of the outputs of these paths is seen to be H_f, independent of the package. In the filter stopband (when H_f is very small), the filter path output is dominated by direct feedthrough. (5.3) and (5.4) can now be written as

$$\begin{aligned}
\frac{V_{o,fil}(f)}{V_i(f)} &\approx k_1H_{in} + k_3H_{in}H_b \text{ (filter path)} \qquad (5.7) \\
\frac{V_{o,dir}(f)}{V_i(f)} &\approx H_{in}H_b + k_1H_{in} + k_2H_{in}H_b^2 \text{ (direct path)} \qquad (5.8)
\end{aligned}$$

From the above, it is seen that the measured stopband response is independent of H_f! To make matters worse, the k_i's typically increase with frequency, while $|H_f|$ decreases with frequency - hence the conventional technique can lead to gross measurement errors in the filter stopband (this observation can be confirmed by several measured filter responses reported in the literature). Further, since the k_i's depend on packaging details,

the measured stopband response is a function of the package/PCB used to characterize the filter.

5.2 PROPOSED MEASUREMENT TECHNIQUES

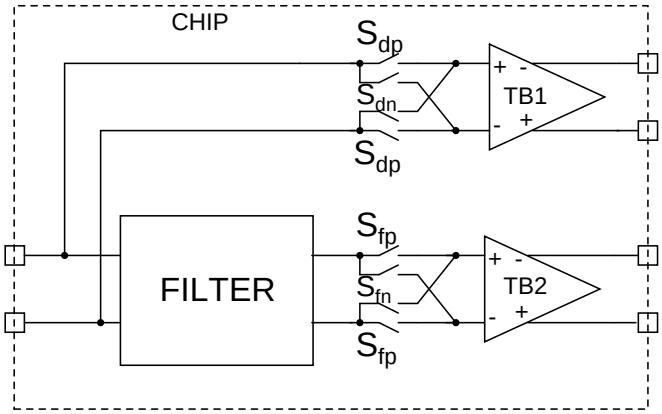


Figure 5.7: On-chip portion of proposed technique.

In this section, we present two improved measurement techniques which account for and eliminate package feedthrough to a large degree. The schemes does not require knowledge of the package details, or measurements of isolation of the package. The additional complexity introduced on-chip is negligible.

5.2.1 Method - 1 : Using a Vector Network Analyzer (VNA)

The basic idea behind this technique is the following - If the filter gain is multiplied by -1, we see from (5.3) that the term due to the filter ($H_{in}H_fH_b$) changes sign, while all the terms due to package feedthrough (except $k_2H_{in}H_b^2H_f$, which can be neglected in the stopband) remain the same. Thus, the difference of the filter path transfer functions measured with the filter as is, and with the filter gain multiplied by -1 is largely free from feedthrough terms. Since the filter and testbuffers are fully differential, mul-

tiplication of the filter gain by -1 is trivial, and is accomplished using a simple cross coupled switch network.

The on-chip portion of the proposed technique is shown in Figure 5.7. The off-chip portion is not shown as it remains identical to that shown in Figure 5.1. Each test-buffer has two pairs of switches at the input. Considering the filter-path, two pairs of switches (labelled S_{fp} and S_{fn}) are added between the filter and TB2. When the switches S_{fp} are turned ON, they enable the direct connection of the filter to TB2. Turning on the two inner switches S_{fn} instead is equivalent to multiplying the gain of the filter by -1. Note that S_{fp} and S_{fn} are not closed simultaneously. A similar arrangement is provided in the direct path (switches S_{dp} and S_{dn}). Each pair of switches is controlled by an external digital signal. It is necessary (and straightforward) to ensure that the input impedance of the test buffers remains the same irrespective of which pair of switches is turned on. The proposed technique calls for 4 measurements - two for the filter-path and two for the direct-path. The filter-path transfer functions measured when S_{fp} and S_{fn} are ON are denoted by $H_{fil,p}$ and $H_{fil,n}$ respectively. $H_{fil,p}$ is approximately given by the right hand side of (5.3). Replacing H_f with $-H_f$ in (5.3) gives $H_{fil,n}$. From this, we see that

$$H_{fil,p} - H_{fil,n} \approx 2H_{in}H_fH_b(1 + k_2H_b) \tag{5.9}$$

The direct feedthrough terms get eliminated as their phase does not change when the filter gain changes sign. A similar set of measurements is made on the direct-path, with S_{dp} and S_{dn} ON and the resulting transfer functions are denoted by $H_{dir,p}$ and $H_{dir,n}$ respectively. Using (5.4), and proceeding in a manner analogous to the derivation of

(5.9), we see that

$$H_{dir,p} - H_{dir,n} \approx 2H_{in}H_b(1 + k_2H_bH_f) \tag{5.10}$$

Using (5.9) and (5.10), the filter response can be obtained as

$$H_f(f) \approx \frac{H_{fil,p} - H_{fil,n}}{H_{dir,p} - H_{dir,n}} \tag{5.11}$$

The approximation above is justified since the feedthrough terms are very small compared to unity.

The procedure discussed above involves measurement of complex frequency responses and the operations are complex. Therefore, the technique requires a VNA to measure the S-parameters of the filter path and direct path, in which case, it can be shown that,

$$H_f(f) \approx \frac{S_{21,filp} - S_{21,filn}}{S_{21,dirp} - S_{21,dirn}} \tag{5.12}$$

Test Buffer Design

Figure 5.8 shows the simplified schematic of the test-buffer and the associated switches S_{fp} and S_{fn}. When the control bit B is high, transistors M_{s2} and M_{s4} are ON, while M_{s1} and M_{s3} are off. The opposite situation occurs when $\overline{B}$ is high. The source follower stage at the input results in a very high input impedance, which is almost fully capacitive. This (small) capacitance can be taken into account during the filter design process. Notice that the input impedance of the test-buffer remains the same regardless of which of switch pairs are ON.

The dimensions of M3 and M4, which form a differential pair, are chosen so that

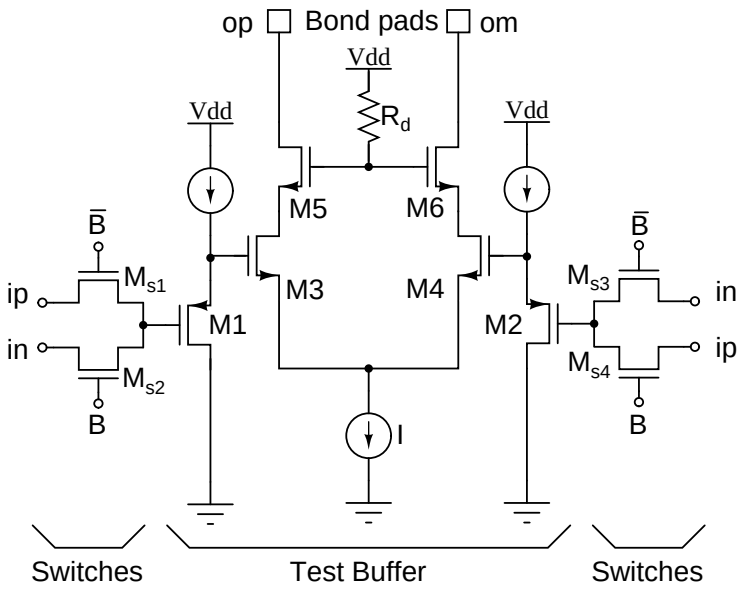


Figure 5.8: Simplified schematic of the test buffer and polarity reversal switches.

they have a large gate overdrive voltage. This is important, since the distortion of the test-buffer should be small when compared to that introduced by the filter. M5 & M6 are cascode devices that increase the isolation of the test-buffer, whose output is a current that is terminated with a resistance on the test-board. R_d is a damping resistor that prevents common-mode oscillation of the cascode with the package inductance.

5.2.2 Method - 2 : Using a Spectrum Analyzer

One advantage of the technique proposed in Nauta (1992) is that it needs only magnitude measurements, which can be made using a spectrum analyzer with a tracking generator (note that the VNA technique described in the previous section needed both magnitude & phase). In this subsection, we propose a technique that attempts to eliminate package feedthrough, but uses only magnitude response measurements. The basic idea behind the technique is as follows. The output of the filter path is the (complex) sum of the signal through the filter and that through the package. If there was no

feedthrough, changing the gain of the filter-path by a factor α would result in the amplitude of the filter-path output changing by α. This will no longer be the case with package feedthrough. Thus, the amount of feedthrough can be estimated (and eliminated) by monitoring the amplitude of the filter-path output when the path gain is changed.

With independent control of the gains of the filter & direct paths, the signal flow graph of Figure 5.6 is modified as Figure 5.9. α_1 & α_2 represent the programmable gains of the filter & direct paths respectively.

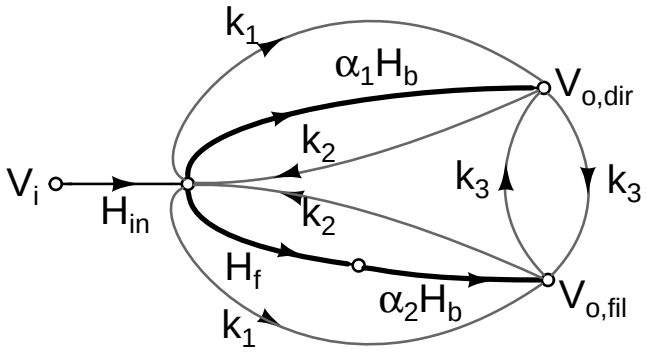


Figure 5.9: Signal flow graph of the setup with gain control.

The equations (5.3) and (5.4) are now modified as

$$\begin{aligned} H_{fil} &\approx \alpha_2 H_{in} H_f H_b [1 + k_2(\alpha_2 H_b H_f + \alpha_1 H_b)] \\ &\quad + k_1 H_{in} + k_3 \alpha_1 H_{in} H_b \end{aligned} \tag{5.13}$$

$$\begin{aligned} H_{dir} &\approx \alpha_1 H_{in} H_b [1 + k_2(\alpha_2 H_b H_f + \alpha_1 H_b)] \\ &\quad + k_1 H_{in} + k_3 \alpha_2 H_b H_f H_{in} \end{aligned} \tag{5.14}$$

In the above equations, we assume that $|k_2(\alpha_2 H_b H_f + \alpha_1 H_b)| \ll 1$, since feedthrough

terms are small compared to unity. (5.13) and (5.14) then simplify to

$$H_{fil} \approx \alpha_2 H_{in} H_f H_b + H_x \tag{5.15}$$

$$H_{dir} \approx \alpha_1 H_{in} H_b + H_y \tag{5.16}$$

where, $H_x = k_1 H_{in} + k_3 \alpha_1 H_{in} H_b$ and $H_y = k_1 H_{in} + k_3 \alpha_2 H_b H_f H_{in}$, represent feedthrough terms. The magnitudes of the filter and direct path transfer functions can be written as

$$\begin{aligned} |H_{fil}|^2 &\approx |\alpha_2 H_{in} H_f H_b|^2 + |H_x|^2 \\ &\quad +2\,|\alpha_2 H_{in} H_f H_b||H_x|\,\cos\theta_1 \end{aligned} \tag{5.17}$$

$$\begin{aligned} |H_{dir}|^2 &\approx |\alpha_1 H_{in} H_b|^2 + |H_y|^2 \\ &\quad +2\,|\alpha_1 H_{in} H_b||H_y|\,\cos\theta_2 \end{aligned} \tag{5.18}$$

θ_1 is the angle between $H_{in} H_f H_b$ and H_x, while θ_2 is the angle between $H_{in} H_b$ and H_y.

In each of the equations (5.17) and (5.18), we have 3 unknowns. The left hand side can be obtained from measurements.This means that three sets of measurements on each path are needed to compute the three unknown variables. Note that our interest is to determine $|H_{in} H_f H_b|$ and $|H_{in} H_b|$, and thereby $|H_f|$. This is done as follows.

a. Three magnitude response measurements are made on the filter path, with different gains : α_2 = 2, -2 and 1, with α_1 set to 1. Solving (5.17) for $|H_{in} H_f H_b|^2$, it can be shown that

$$\begin{aligned} |H_{in} H_f H_b|^2 &\approx |H_{fil}|^2_{\alpha_2=2} + \frac{1}{3}\,|H_{fil}|^2_{\alpha_2=-2} \\ &\quad - \frac{4}{3}\,|H_{fil}|^2_{\alpha_2=1} \end{aligned} \tag{5.19}$$

b. Three magnitude response measurements are made on the direct path, with dif-

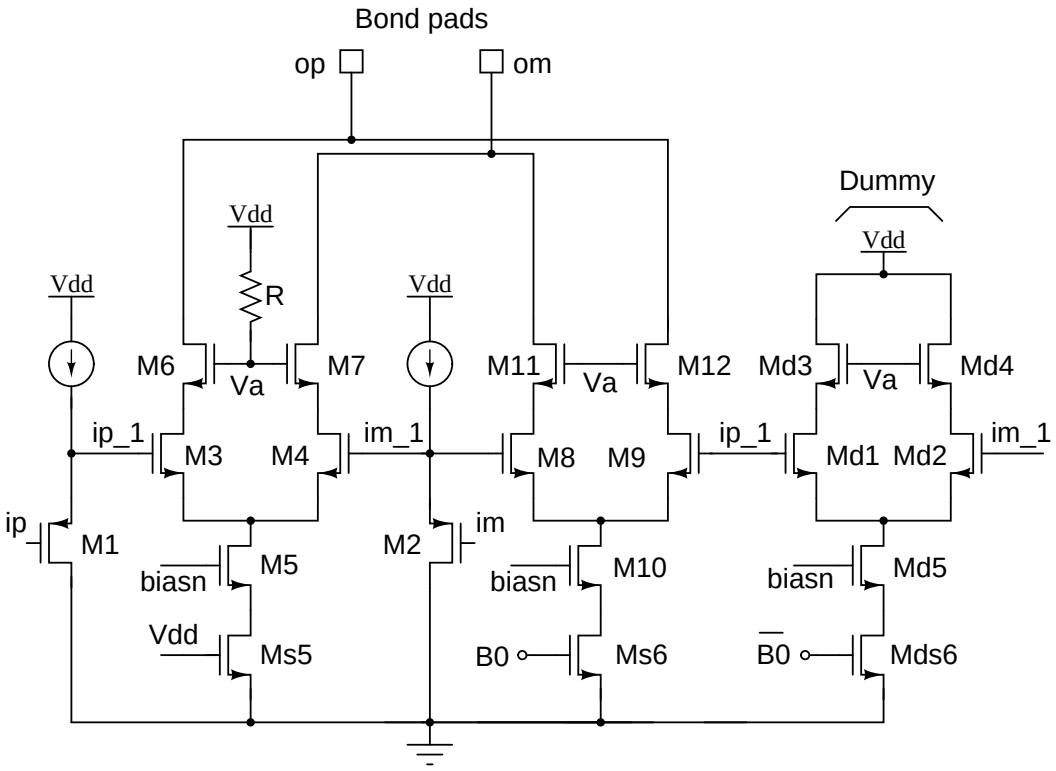


Figure 5.10: Simplified schematic of the test buffer with variable gain and constant bandwidth.

ferent gains : α_1 = 2, -2 and 1, with α_2 set to 1. Solving (5.18) for $|H_{in}H_b|^2$ yields

$$|H_{in}H_b|^2 \approx |H_{dir}|^2_{\alpha_1=2} + \frac{1}{3}|H_{dir}|^2_{\alpha_1=-2} - \frac{4}{3}|H_{dir}|^2_{\alpha_1=1} \quad (5.20)$$

c. The ratio (5.19)/(5.20) yields the squared magnitude response of the filter.

Programmable gain test buffer

Figure 5.10 shows the schematic of the programmable gain test-buffer. The polarity reversal switches at the input are not shown, since the arrangement is similar to that in Figure 5.8. To achieve gain programmability, a differential pair M8-M9, whose tail current can be shut off using a digital control signal B0, is added in parallel with the original pair (M3-M4). When M8-M9 are turned off, a dummy pair Md1-Md2 is turned

on, so that the impedance at nodes ip_1 & im_1 remain the same. It is thus seen that the gain of the test-buffer can be increased by a factor of two, *while maintaining the same normalized frequency response.*

5.3 A MODIFIED TEST-SETUP FOR THE PROPOSED MEASUREMENT TECHNIQUES

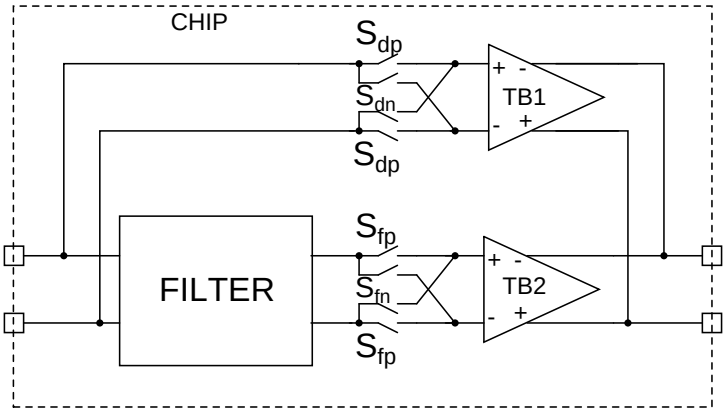


Figure 5.11: On-chip portion of improvement to the proposed technique.

An improvement to the test-setup for the proposed measurement techniques presented in section 5.2 is shown in Figure 5.11. The improvement is on chip where, the outputs of the two test buffers (TB1 and TB2) are tied together and a single output is brought out of the chip. Only one test buffer will be on at any time. Since, at a given time, only one path from the input to the output is active, the effect of package feedthrough will be reduced to a large extent. The SFG of this setup is shown in Figure 5.12(a) & (b) for the cases when TB1 and TB2 are on.

Solving the SFG in Figure 5.12(a)&(b) for the filter path measurement, neglecting higher powers of k_1 and k_2, we get -

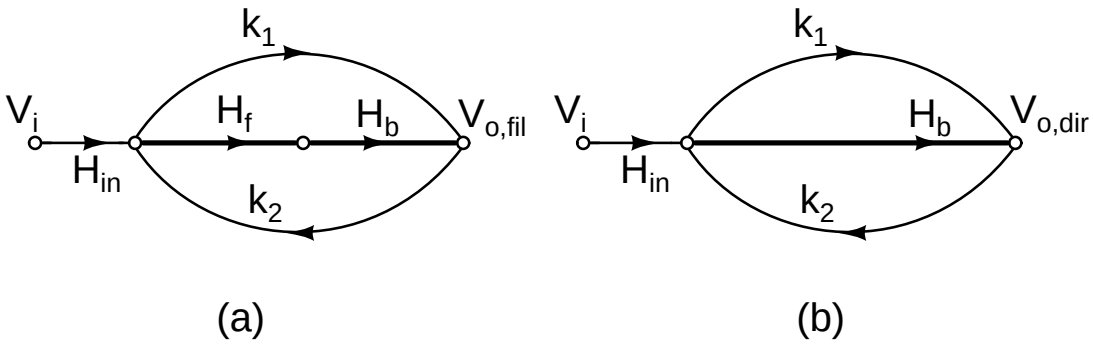


Figure 5.12: Signal flow graph for the improved method when (a) TB2 is on (filter path measurement) and (b) TB1 is on (direct path measurement).

$$\frac{V_{o,fil}(f)}{V_i(f)} \approx H_{in}H_fH_b + k_1H_{in} + k_2H_{in}H_b^2H_f^2 \tag{5.21}$$

$$\frac{V_{o,dir}(f)}{V_i(f)} \approx H_{in}H_b + k_1H_{in} + k_2H_{in}H_b^2 \tag{5.22}$$

Notice that (5.21) and (5.22) are largely free from the feedthrough terms when compared with (5.3) and (5.4). When the proposed VNA method is used for this test-setup, we see that *all* the feedthrough terms are cancelled and no further approximation (like it was made in arriving at (5.11)) is necessary. Therefore the modified on-chip test setup improves the measurement accuracy in the stopband.

5.4 MEASUREMENT OF NOISE SPECTRAL DENSITY

The output noise spectral density of a filter is an other important quantity that needs to be measured. Usually, the spectral density of the noise at the output of the filter path (as shown in Figure 5.1) is measured, from which the mean square noise of the filter is calculated. Since the frequency response of the package and the noise of the test-buffers is not accounted for, this approach can lead to erroneous results. In the

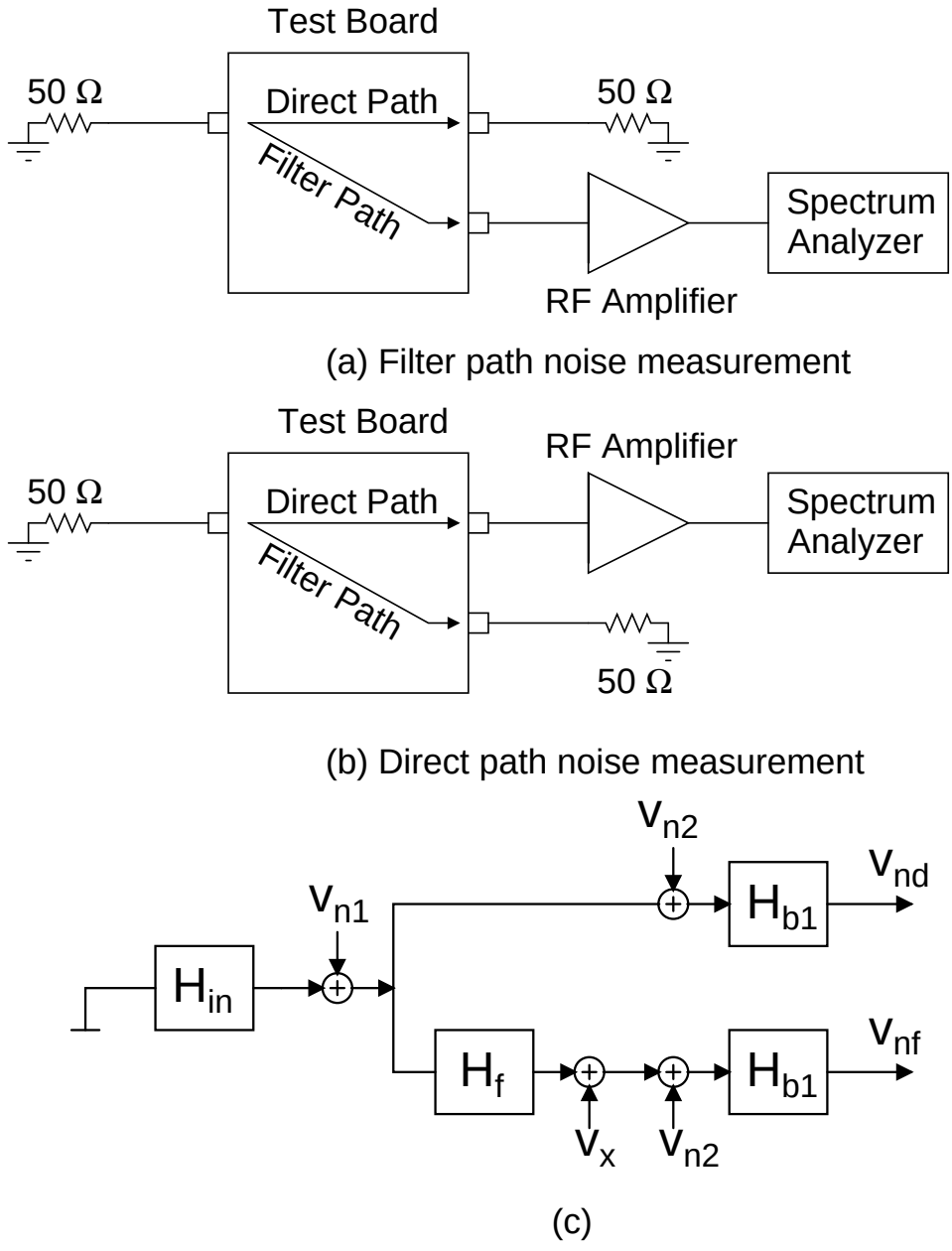


Figure 5.13: (a) & (b) Test setup for the measurement of noise spectral density of the filter. (c) Block diagram of the test setup.

microwave literature, several authors have reported techniques to measure the noise properties of packaged two ports. These techniques are accurate but require knowledge of the package, from measurements or simulation. Here, we present an approximate technique that does not need package information. The test setup used in our work for measuring the filter output noise spectral density is shown in Figure 5.13(a)&(b). It is a two step process, involving the measurement of the filter and direct path noise spectral densities. Since the spectrum analyzer has a poor noise figure, a low noise RF amplifier is used to amplify the noise output of the desired path. Unused ports are terminated in $50\,\Omega$.

The equivalent block diagram of the test setup is shown in Fig 5.13(c). v_{n1} & v_x are the output noise voltages of the input path and the filter respectively. The input path has a transfer function H_{in} and H_{b1} is the transfer function of the path from the filter output to the spectrum analyzer input. v_{n2} is the input referred noise voltage of this path (note that H_{b1} includes the RF amplifier). v_{nf}, v_{nd} are the filter path and direct path noise voltages measured in the spectrum analyzer. From Figure 5.13(c), the spectral densities of the filter & direct output noise are seen to be

$$\begin{aligned} S_{nf}(f) &= S_{vn1}(f)|H_f H_{b1}|^2 + (S_{vx}(f) + S_{vn2}(f))|H_{b1}|^2 \\ S_{nd}(f) &= (S_{vn1}(f) + S_{vn2}(f))|H_{b1}|^2 \end{aligned} \tag{5.23}$$

From the above equations, we see that

$$S_{nf}(f) - S_{nd}(f) = S_{vn1}(f)(|H_f|^2 - 1)|H_{b1}|^2 + S_{vx}(f)|H_{b1}|^2 \tag{5.24}$$

The first term on the right hand side of (5.24) is much smaller than the second term due to the following. Noise contributed by the input path is negligible compared to that (S_{vx}) generated by the filter as input path noise is only due to the input termination resistors (about 25 Ω). Further, in the filter passband (where the noise spectral density is significant), $|H_f|^2 \approx 1$. Thus, $S_{vx}(f)$ can be approximated as

$$S_{vx}(f) = \frac{S_{nf}(f) - S_{nd}(f)}{|H_{b1}|^2} \tag{5.25}$$

The direct measurement of H_{b1} is problematic since H_{in} & H_{b1} are in cascade, as seen from Figure 5.13(c). In the active filter literature, it is common practice to assume the noise at the filter path output is only due to the filter, neglecting the test-buffer noise. When the buffer noise is significant, or when the effects of the package are not accounted for, it becomes difficult to estimate the filter noise spectrum (for example, see the measurements reported in Gopinathan *et al.* (1999)). Another common technique is to assume that $|H_{b1}|$ is the same as the gain of the direct path. In this work, we propose a technique to estimate $|H_{b1}|$, thereby enabling a more accurate measurement of noise due to the filter.

5.4.1 Measurement of $|H_{b1}|$

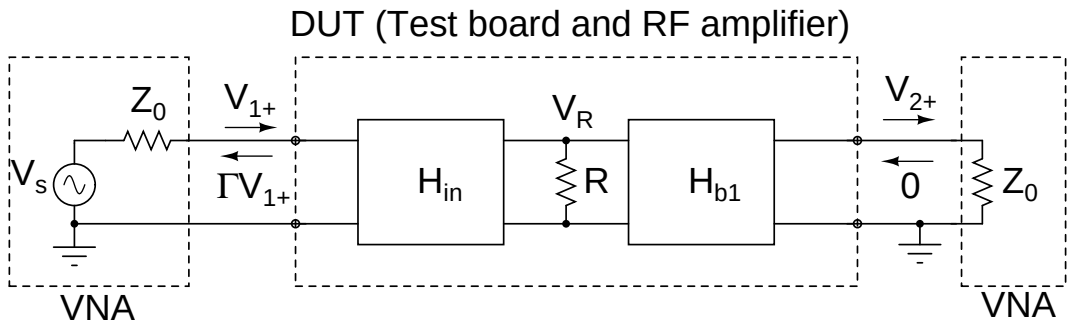


Figure 5.14: Test setup for finding H_{b1}

The basic idea is to observe that $|H_{b1}|$ can be determined if it was somehow possible to infer the magnitude of $|H_{in}|$. From Figure 5.14, it is seen that the input reflection coefficient can be used to determine $|H_{in}|$ as follows. R is a nominally $50\,\Omega$ on-chip termination resistor (in practice, this can be implemented by a transistor, which is only turned on during test time). V_{1+} denotes the voltage wave incident on the input port of the Device Under Test (DUT). Γ is the reflection coefficient. If the transmission from the input port of DUT to the resistor (R) is lossless

$$\frac{V_{1+}^2}{Z_0}\left(1-|\Gamma|^2\right)=\frac{V_R^2}{R} \tag{5.26}$$

Also, $S_{21}=\dfrac{V_{2+}}{V_{1+}}$, $H_{b1}=\dfrac{V_{2+}}{V_R}$ and $\Gamma=S_{11}$. Thus, $|H_{b1}|^2$ is given by

$$|H_{b1}|^2=\frac{|S_{21}|^2}{\frac{R}{Z_0}(1-|S_{11}|^2)} \tag{5.27}$$

In practice, the transformer (used for single-ended to differential conversion) has a loss (1 dB in our case). Denoting the power loss by α, it can be shown that $|H_{b1}|^2$ can be determined by using

$$|H_{b1}|^2=\frac{|S_{21}|^2}{\alpha\frac{R}{Z_0}(1-\frac{|S_{11}|^2}{\alpha^2})} \tag{5.28}$$

S_{21} and S_{11} are be obtained by measuring the scattering parameters of the direct path . R can be easily measured across the input terminals of the chip. (5.25) can be evaluated to obtain the noise spectral density of the filter.

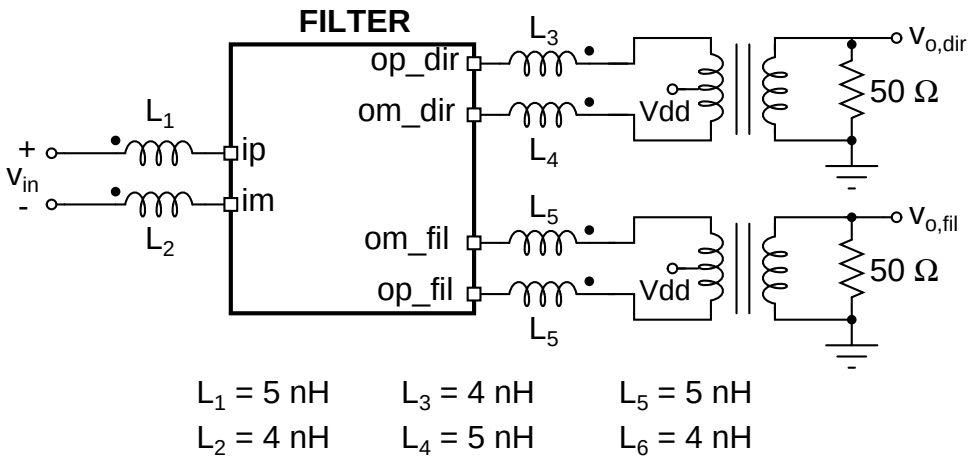


Figure 5.15: Schematic of the test bench used for validating the proposed measurement technique. The mutual inductance used for the test-setup is given in Table 5.1

Table 5.1: Mutual coupling between the bondwire inductances used for the simulation

	L_2	L_3	L_4	L_5	L_6
L_1	0.6	0.3	0.3	0.3	0.6
L_2	–	0.6	0.3	0.3	0.3
L_3	–	–	0.6	0.3	0.3
L_4	–	–	–	0.6	0.3
L_5	–	–	–	–	0.6

5.5 SIMULATION RESULTS

To validate the proposed frequency response measurement techniques, simulations were run on the extracted netlist of the filter designed in chapter 2. The test chip has independent filter path and direct path. Inductive couplings were deliberately introduced between the three ports of the filter chip. Figure 5.15 shows the schematic of the test-bench used for the simulation. $L1 - L6$ represent the bond-wire inductances and are mutually coupled to each other. The coupling that was used between these inductors are shown in Table 5.1.

Figure 5.16 shows the simulation results for the filter set at the lowest bandwidth (71.4 MHz). It can be seen that in presence of coupling, the conventional technique is

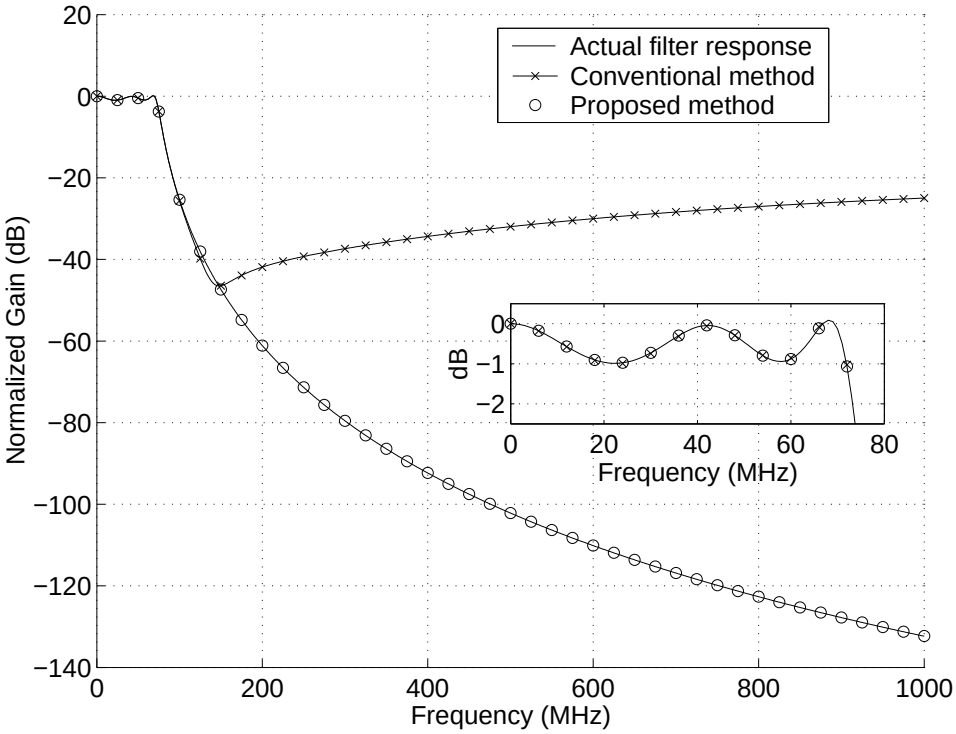


Figure 5.16: Simulation results for the proposed measurement technique using a VNA

accurate only upto an attenuation of about 50 dB at 150 MHz, where as the proposed measurement technique is robust even till 1 GHz. However, in the passband the conventional technique is still accurate, as mentioned earlier in this chapter.

CHAPTER 6

EXPERIMENTAL RESULTS

This chapter presents the experimental results of the fabricated chips along with the details of the test board. Two filter test-chips were fabricated in a 0.35 μm CMOS process from Austria Micro Systems (AMS) through the Europractice program. One chip did not incorporate NQS compensation and was design centered using a simple model for the transconductor, as is the normal practice. Another chip, fabricated on the same run, had incorporated in it our proposed NQS correction scheme. Both the chips were fabricated in a single die of 10 mm^2. Figure 6.1 shows the die photograph of the chip without NQS compensation. Figure 6.2 shows the bonding diagram of the chip. The chips were packaged in a 40-pin DIP. Both the NQS uncompensated and compensated chips are pin compatible. The pin-out of the packaged IC and the functionality of each pin is given in Appendix B.

6.1 DESIGN OF THE TEST BOARD

A two layered printed circuit board (PCB) was used to characterize the filter chips. The dimensions of the PCB are measured $4.7'' \times 3.2''$. A photograph of the populated PCB is shown in Figure 6.3.

The baluns (T1-T3, referring to Figure 5.1 in chapter 5) for the signal conversion from single-ended to differential and vice-versa are wide-band RF transformers ADT1-1WT from Mincircuits. They have a frequency range of 0.4-800 MHz with an insertion

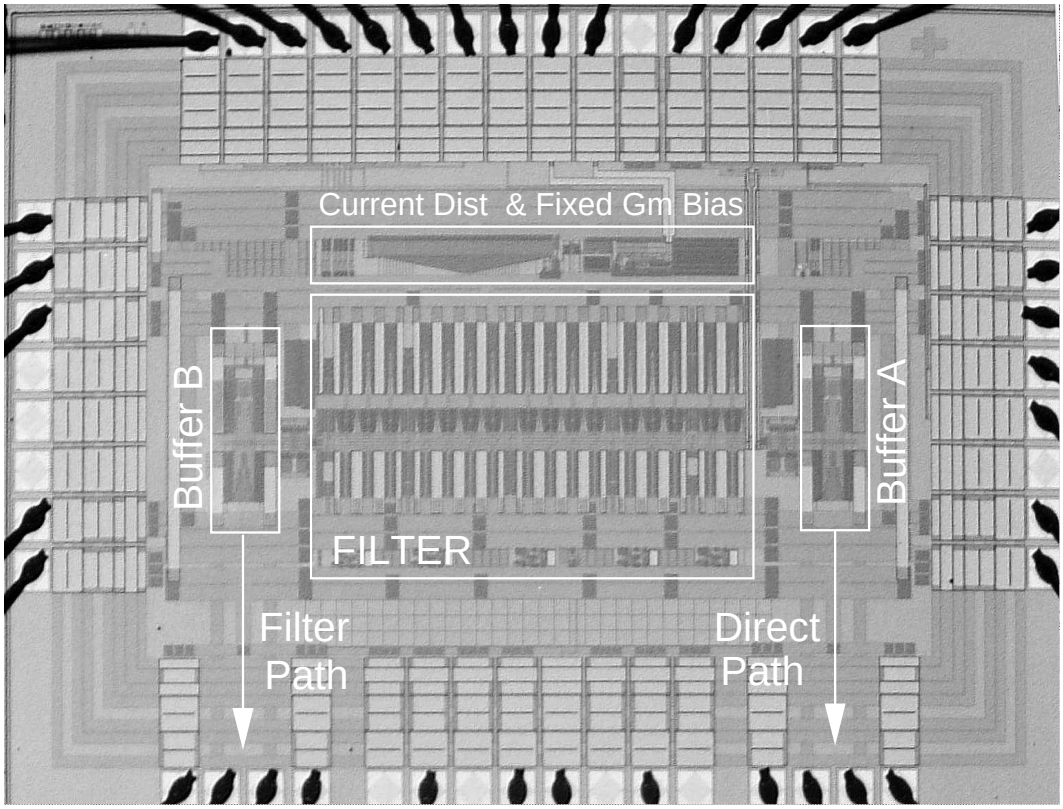


Figure 6.1: Chip die photograph.

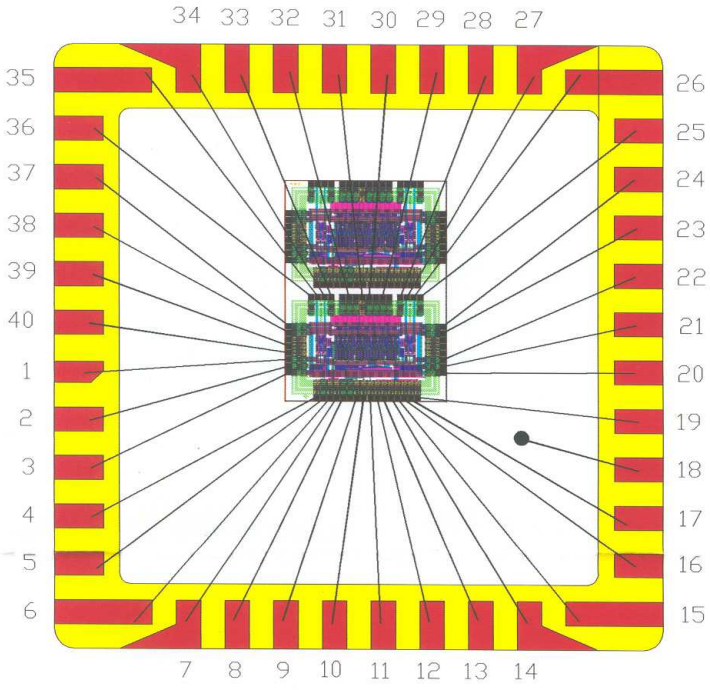


Figure 6.2: Bonding Diagram

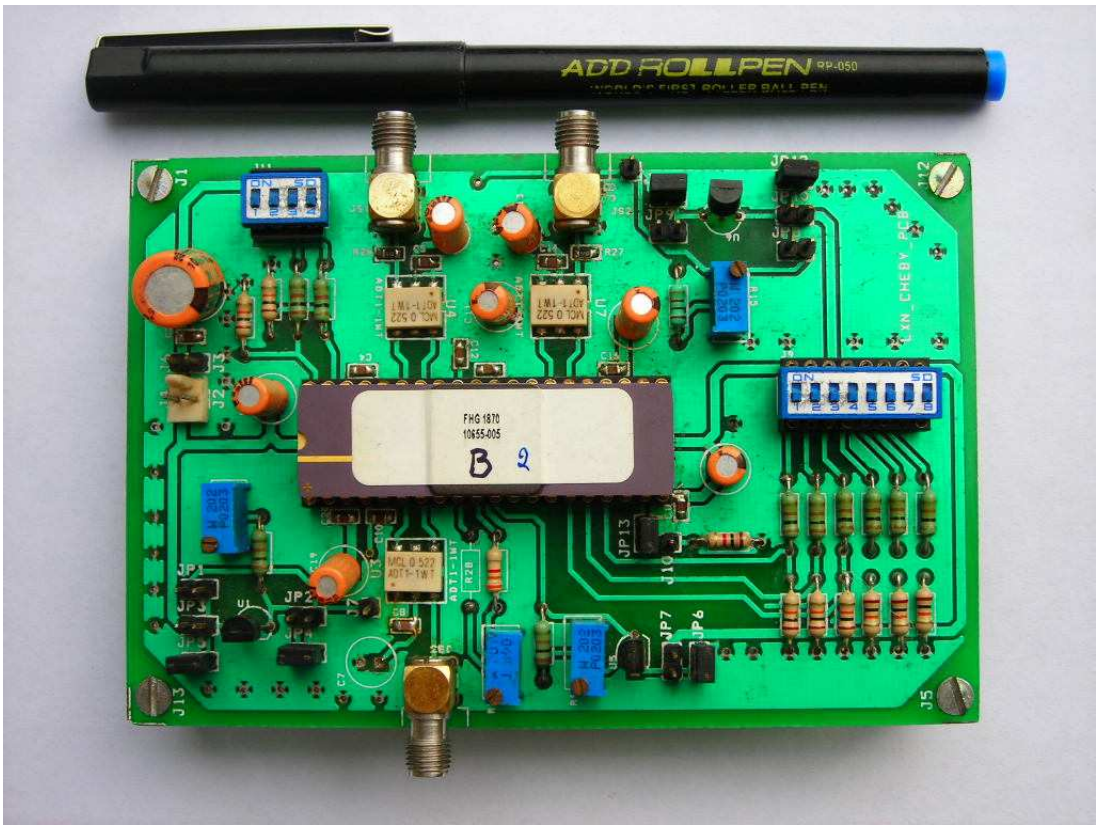


Figure 6.3: Snap-shot of the populated PCB

loss of 3 dB. Every attempt is made to decouple the supply voltage from the possible signal coupling and/or noise by inserting decoupling capacitors close to each supply pin and of the chip. The decoupling at each point is done using a 10 μF electrolytic capacitor (for suppressing low frequency noise) in parallel with a 10 nF surface-mount capacitor (for decoupling high frequency noise). Other DC bias voltages are also decoupled in a similar manner.

The board has two LM334 based current source/sink circuits. These circuits are used as a provision to modify the common-mode reference voltage and the cascode bias voltage (for the transconductors) which are generated on-chip if necessary. The details of these circuits are given in Appendix C. The bandwidth setting control word and the test buffer control bits are set manually using DIP switches.

6.2 RESULTS ON NQS EFFECTS AND ITS COMPENSATION

Figure 6.4 shows the response of the filter without NQS compensation as the bandwidth is programmed. The test-setup has a bandwidth of about 800 MHz due to the baluns used. Hence the magnitude response is shown only up to that frequency. Notice the excellent stop-band response. The stop-band response of the filter with NQS compensation is shown in Figure 6.5.

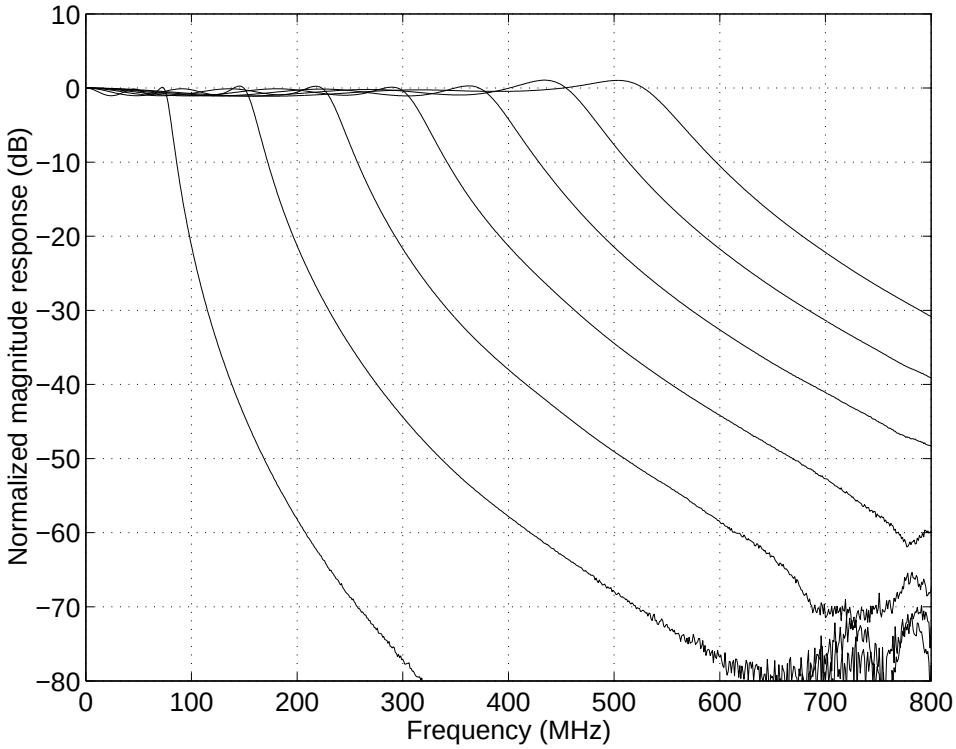


Figure 6.4: Magnitude response of the filter without correcting for NQS effects.

Figure 6.6 shows the frequency response of 20 chips each kind (with and without NQS compensation) plotted on the same plot, for the highest bandwidth setting. Observe the consistently higher peaking and higher cutoff frequency when NQS effects in the transistors are neglected. Due to an error in MOS capacitor modeling, series resistance of the MOS accumulation devices used as integrating capacitors was not taken into account during simulation. This resistance along with the interconnect resistances,

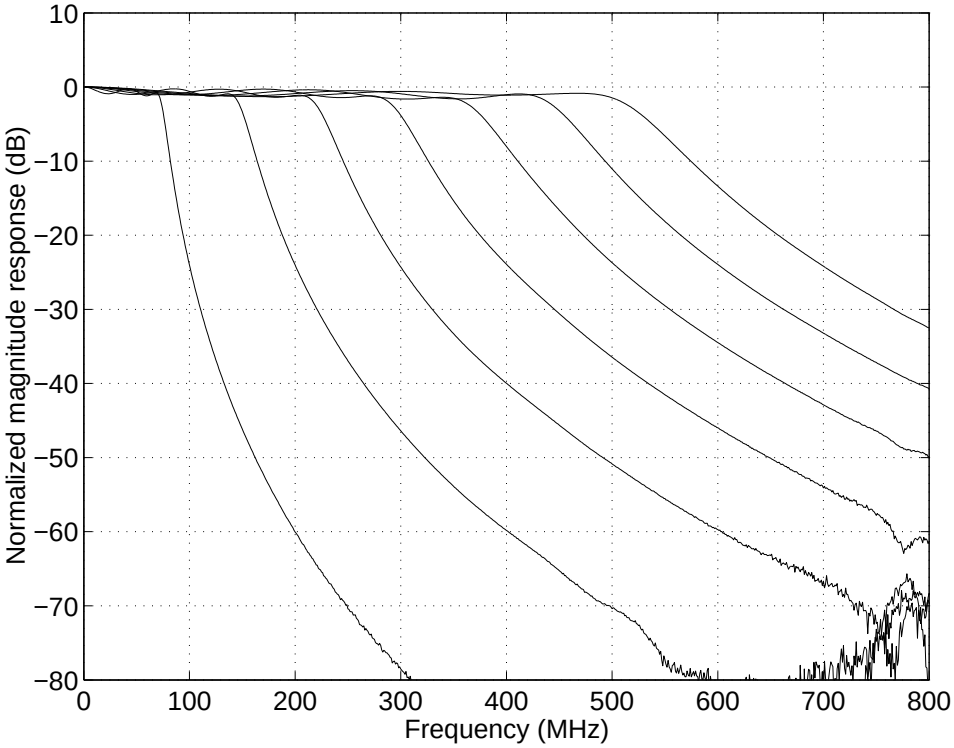


Figure 6.5: Magnitude response of the filter with NQS compensation.

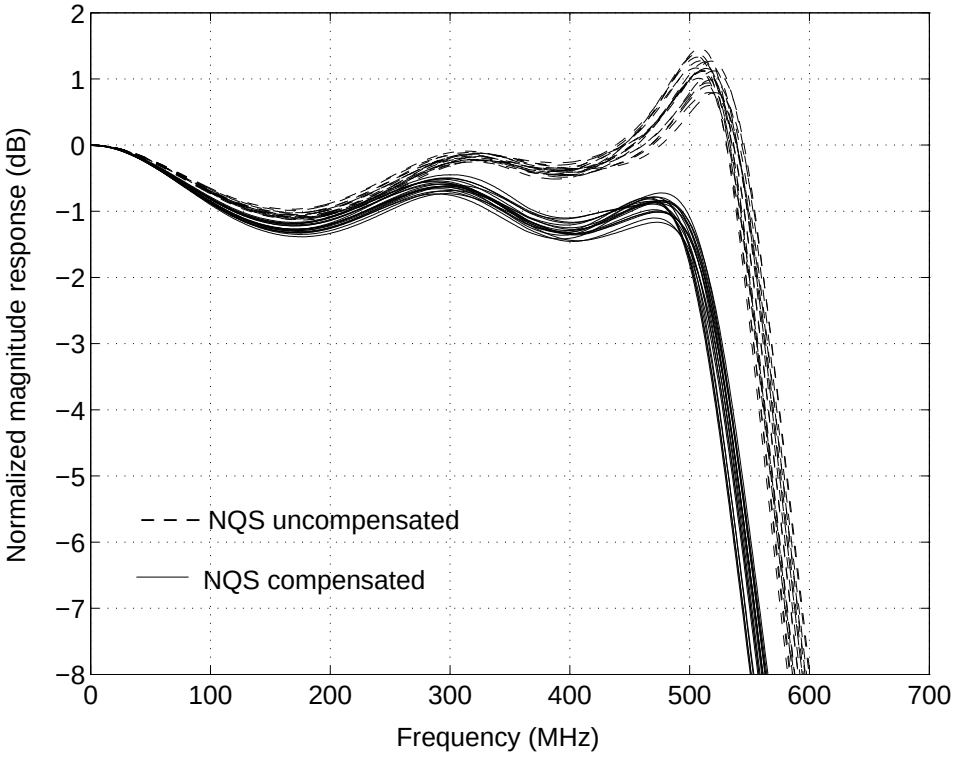


Figure 6.6: Comparison of the frequency response of 20 chips measured under identical conditions, with and without NQS compensation. In both cases, the filter is set to the highest bandwidth.

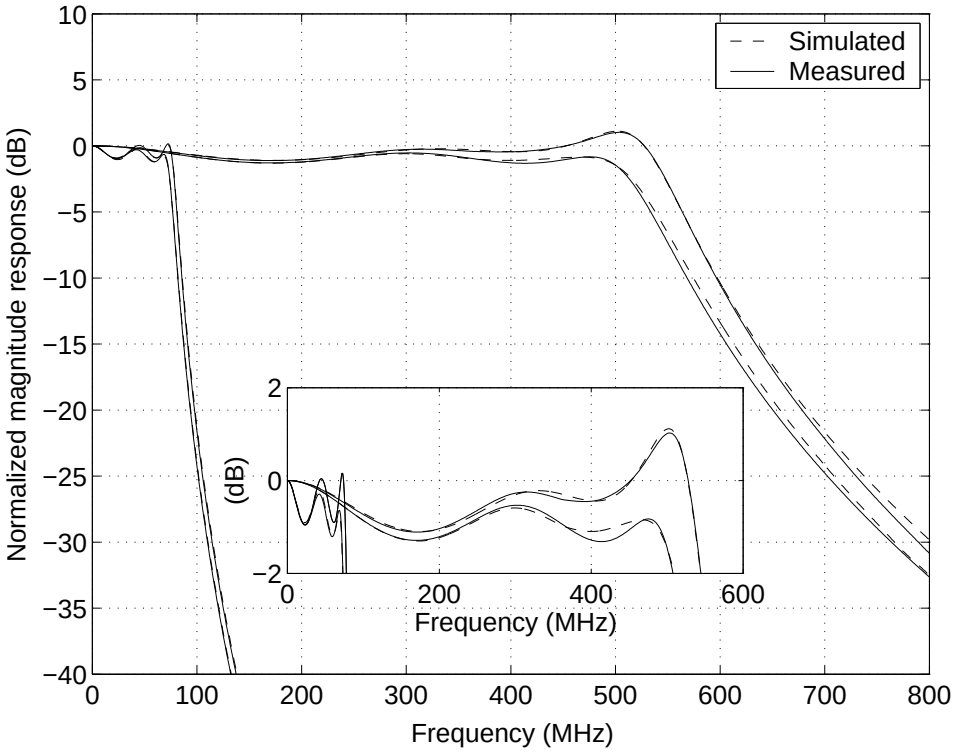


Figure 6.7: Measured filter response is compared with that of the simulated filter considering the channel resistance of MOS capacitors and interconnect resistances, for the NQS uncompensated and the NQS compensated filters. The responses are plotted for both the highest and the lowest bandwidth settings.

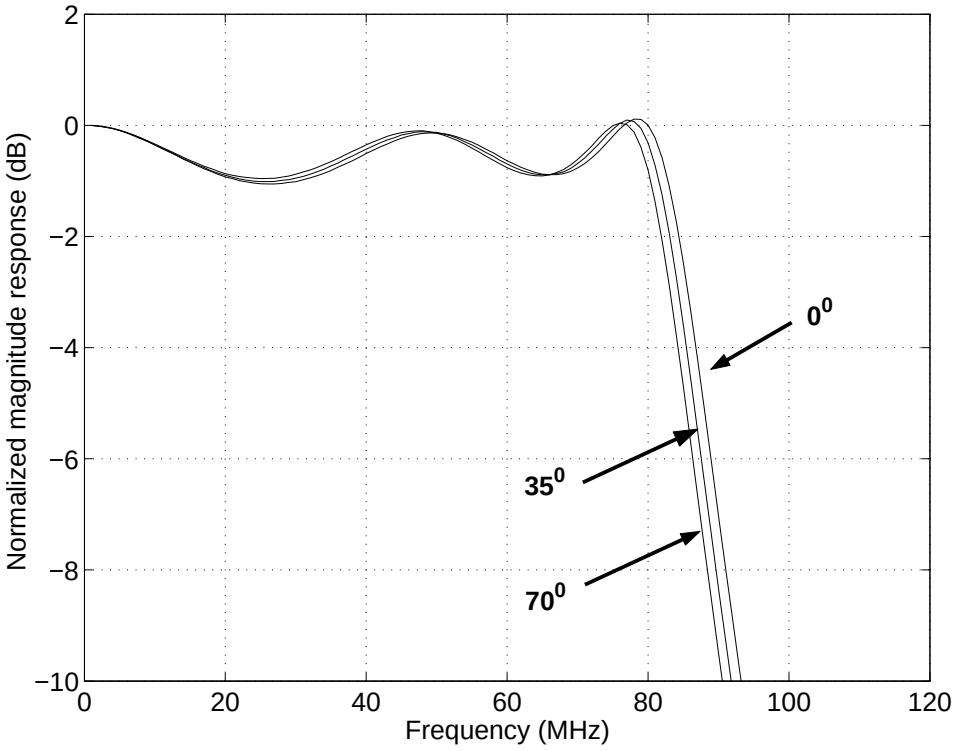


Figure 6.8: Measured frequency response variation with ambient temperature.

leads to additional damping of the filter response. Hence, the peaking in the filter without NQS compensation was smaller than expected. This also explains the droop in the responses with NQS compensation, as the proposed scheme effectively overcompensates for the excess phase of the integrator. The good repeatability of the filter responses indicates that the proposed technique is robust. The cutoff frequency variation among the samples is $\pm 1.4\%$.

To verify the effect of resistance of MOS capacitors, simulations were done on the model of the NQS uncompensated and the NQS compensated filters by including the estimated value of the MOS capacitor resistances along with the interconnect resistances. The distributed effect of these resistances were taken into account (Razavi *et al.* (1994) and Larsson (1997)). The result is shown in Figure 6.7. The simulated response shows that the smaller peaking in the measured response (than expected) is indeed due to the unaccounted MOS resistances and the interconnect resistances.

Figure 6.8 shows the measured frequency response over an ambient temperature range of $0^{o} - 70^{o}\mathrm{C}$. The bandwidth variation with the temperature is found to be ± 1.7 %.

6.3 RESULTS ON PROPOSED CHARACTERIZATION SCHEMES

6.3.1 Frequency Response Measurement Using a VNA

Since the stop-band response is of prime interest here, we present results with the filter bandwidth set to the lowest value (71.4 MHz). A VNA (E5070-B model from Agilent Technologies) was used to measure the S-parameters of the direct and filter

paths. Note that the filter has stopband attenuation of 90 dB at 400 MHz, which is about 30 dB smaller than the isolation of the package !

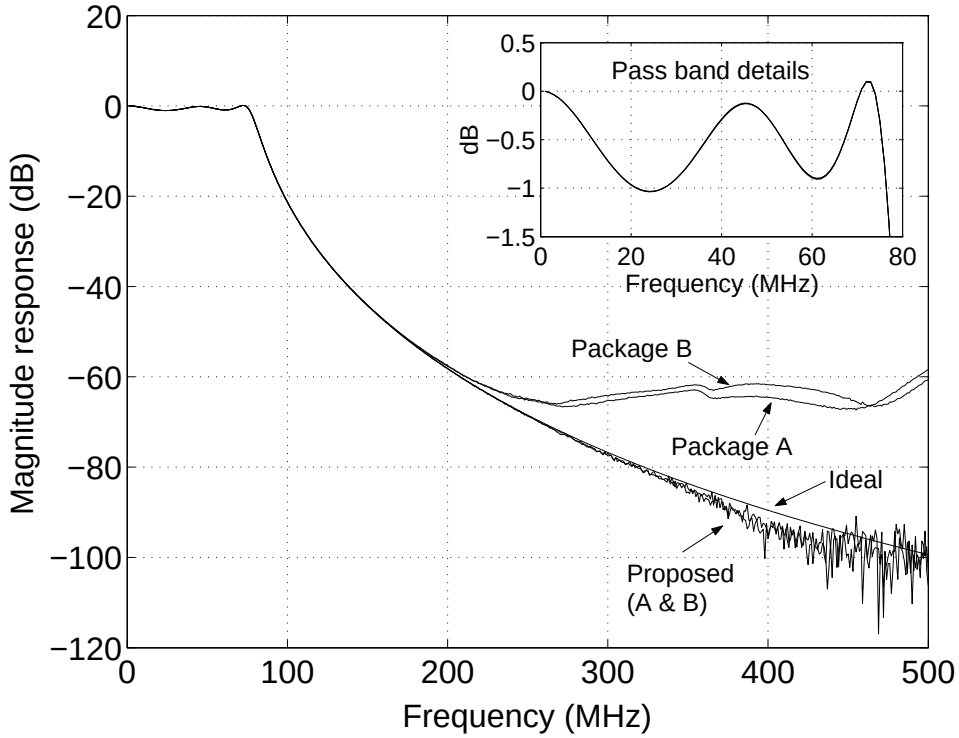


Figure 6.9: Comparison of the responses obtained for the conventional technique and proposed VNA based method. The inset shows the passband detail - the responses measured using the conventional and proposed techniques are virtually identical, since package isolation is high in the filter passband. Notice that the stopband attenuation measured using the proposed technique is less sensitive to package variations.

The measured passband detail is shown in the inset of Figure 6.9, using the conventional and proposed techniques. There are actually two measurements in the inset, but they are virtually indistinguishable. This is to be expected, since package isolation is high at low frequencies (within the filter passband, see Figures 5.3,5.4 & 5.5).

To investigate the sensitivity of the measurements (especially in the filter stop-band) to the package, measurements were made for two “different packages”, named A & B in the discussion to follow. Package A was a 40 pin DIP, while the Package B was the same 40 pin DIP with a copper strip pasted on to the top of the package, thereby mod-

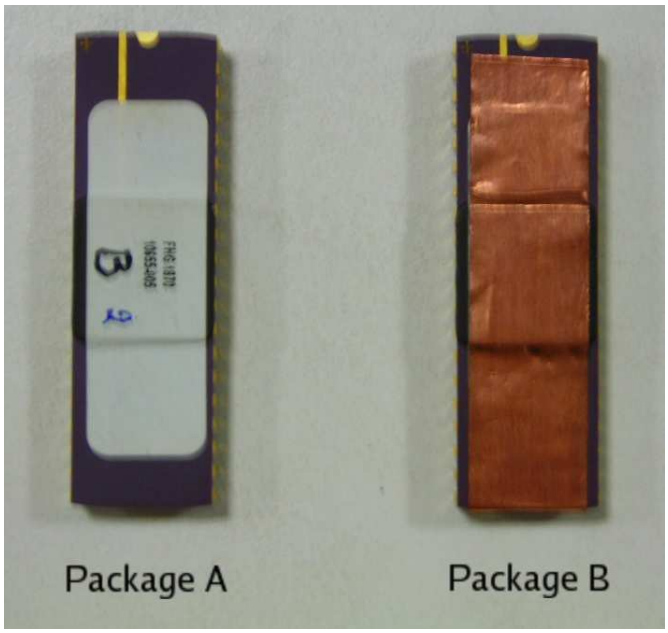


Figure 6.10: Photograph of the package A and B used for investigating the sensitivity of the proposed measurement technique. Package A is a 40 pin DIP and Package B is the same 40 pin DIP but with a copper strip pasted on it.

ifying the high frequency port-to-port isolation. Photograph of the package A and B are shown in Figure 6.10. Figure 6.9 compares the responses obtained through the use of the conventional technique and proposed VNA based technique. It is seen that the conventional measurement is in error beyond about 200 MHz. Moreover, the measured stopband response is sensitive to package characteristics. In contrast, the proposed technique is seen to be almost insensitive to the package, while being accurate to 350 MHz, where the attenuation of the filter is about 90 dB. The deviation from the ideal response beyond this frequency is due to higher order terms neglected in the derivation of the technique, as well as mismatches in the filter and buffer paths. The response is not shown beyond 500 MHz since $H_{fil,p}$ and $H_{fil,n}$ are so small that they are buried in the measurement noise of the VNA.

The 40 pin DIP used to package the filter is unsuitable for high-frequency work such as this. Thanks to the proposed technique, accurate measurements can be made

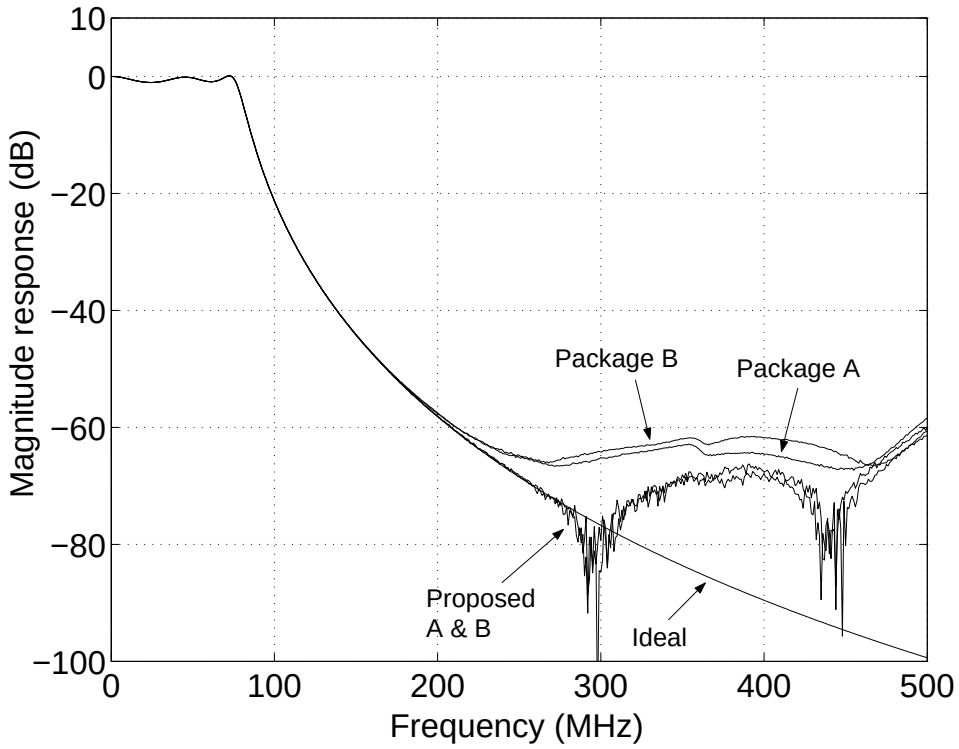


Figure 6.11: Magnitude responses measured using the conventional method and proposed spectral analyzer method.

even in such packages. Note that higher accuracy can be obtained (through our technique) by using a better package, as well as increasing the gains of the test-buffers. Further, the proposed technique can be extended to higher frequency filters, packaged in correspondingly higher performance packages. Examples of such filters include transmission-line based multi-GHz analog adaptive filters for data communication (Sewter and Carusone (2006)).

6.3.2 Frequency Response Measurement Using Spectrum Analyzer Method

Figure 6.11 compares the filter responses obtained using the conventional and proposed spectrum analyzer methods. It is seen that while the proposed spectrum analyzer based technique is an improvement over the conventional method, the performance is not quite as good as the VNA based measurement described in the previous section.

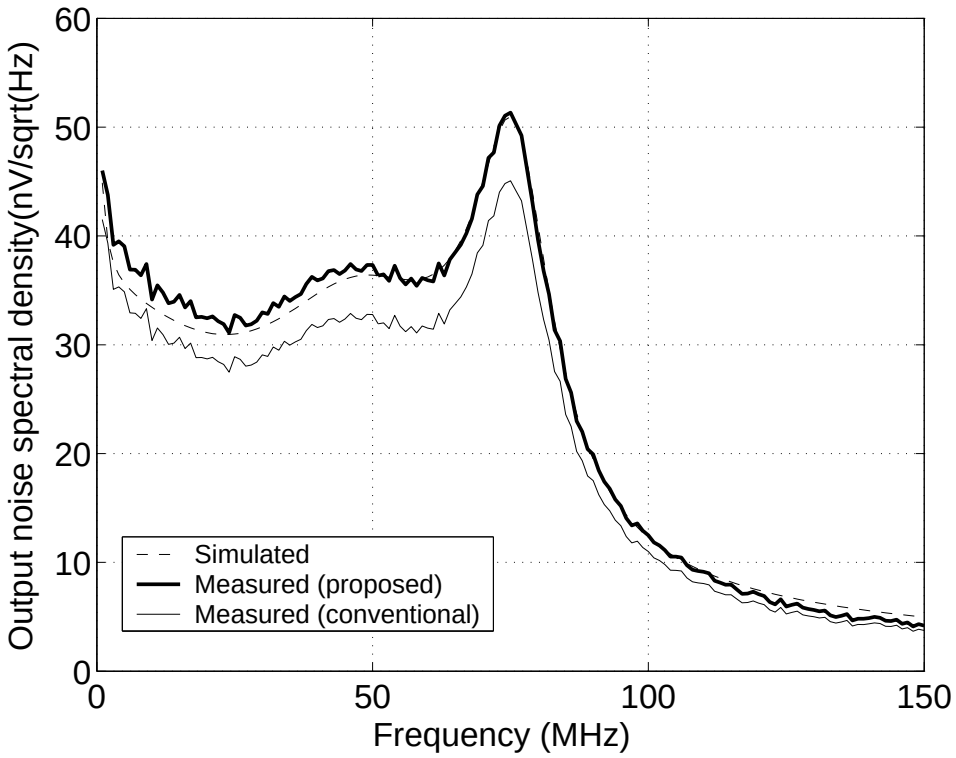


Figure 6.12: Measured and simulated output noise spectral density of the filter for the lowest bandwidth setting.

This makes sense due to the following. In the filter stop-band the magnitude measurements depend on subtraction of two small *squared* numbers, each of which is corrupted by measurement noise (compare this with the VNA method, where squaring is avoided). Further, mismatch in test-buffer gain factors also contribute to error in the measured filter response.

6.3.3 Noise Spectral Density Measurement

During measurements, as mentioned in Chapter 5, two low noise wide-band RF amplifiers (ZKL-2R5 from Minicircuits) were used in cascade to amplify the noise of the filter to levels much higher than the input noise of the spectral analyzer. Figure 6.12 shows the measured output noise spectral density of the filter using the proposed technique. The noise measured using conventional technique is also shown where, $|H_{b1}|$

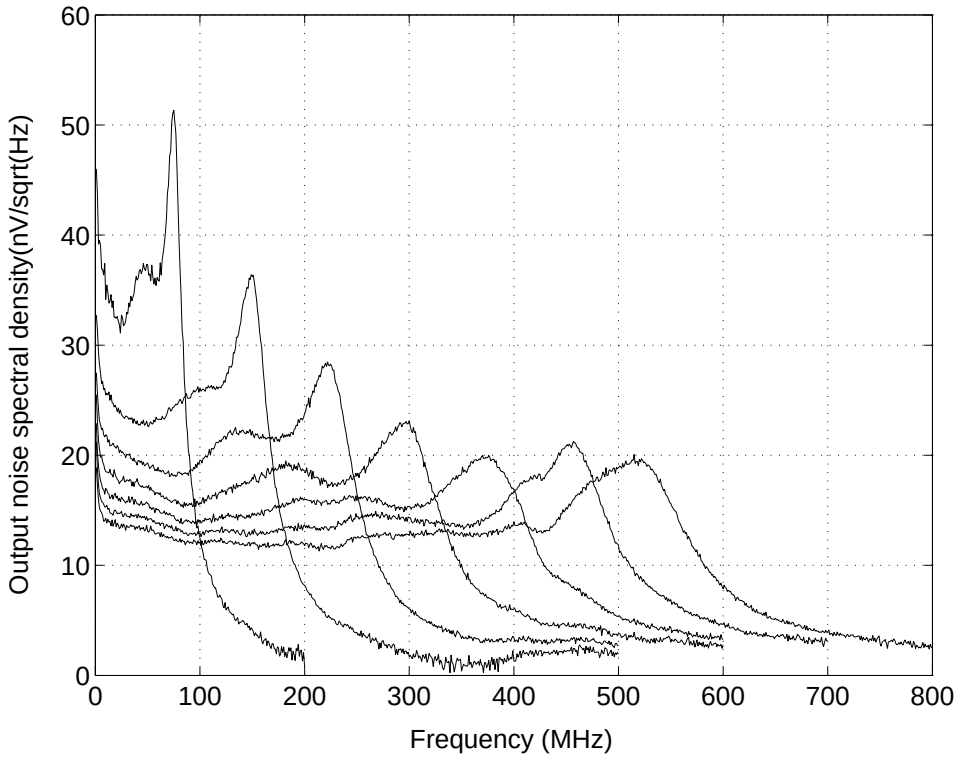


Figure 6.13: Measured output noise spectral density of the filter when the filter bandwidth is tuned over its range.

is (incorrectly) assumed to be the same as the direct path gain. Figure 6.13 shows the output noise of the filter when the bandwidth setting control word is swept from 000 to 111. It is seen that the filter follows the noise properties of constant-C scaled networks as explained by Pavan and Tsividis (2000). The measured integrated output noise of the filter is 356 μV rms, while the simulated noise is 340 μV rms.

6.4 DISTORTION MEASUREMENT

Figure 6.14 shows the third harmonic distortion (HD_3) of the filter as a function of input peak-to-peak differential voltage. The 2^{nd} harmonic is found to be about 20 dB below the third. The filter can handle a signal upto 0.5 V peak-to-peak with total harmonic distortion (THD) $< 1\,\%$. For the measurement, the filter bandwidth is set to the

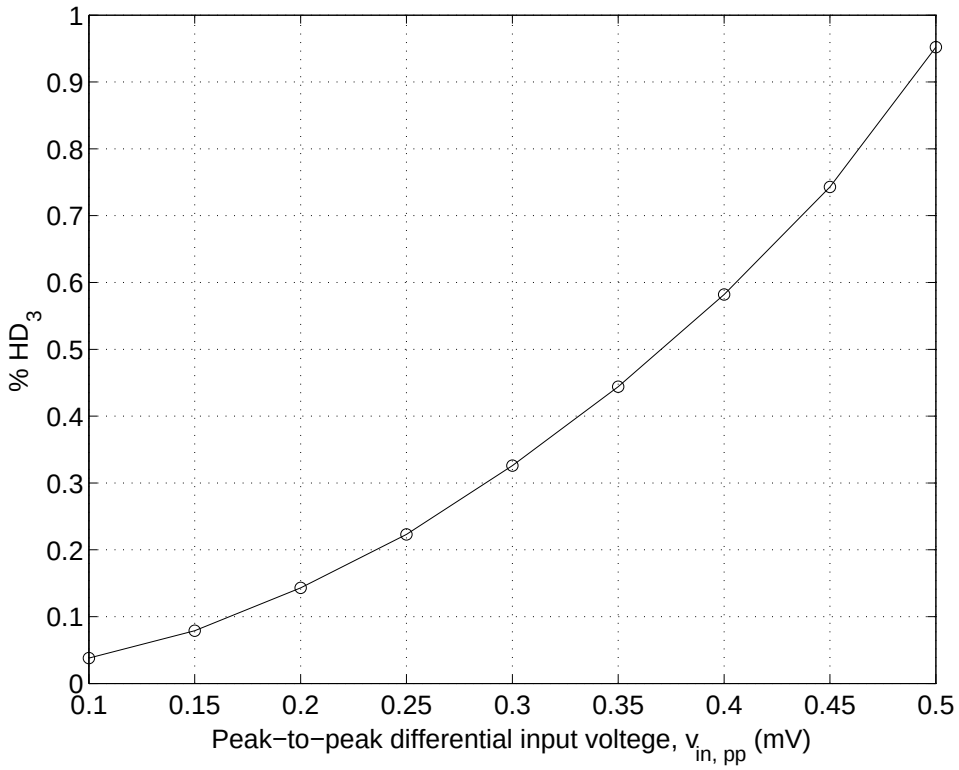


Figure 6.14: Third harmonic distortion of the filter as a function of the input voltage. The filter is set to the lowest bandwidth and the test-tone is given at one-third of the filter band-edge.

minimum (71.4 MHz), as the random mismatches are maximum in this setting. The test tone is set at a frequency such that the third harmonic lies at the band-edge. This is because at very low frequencies no current flows through the integrating capacitors and the non-linearities of transconductors are cancelled by each other (Tsividis and Shi (1985)), while for a test tone at higher frequencies, the third harmonic lies outside the filter pass-band leading to wrong results. To justify this fact, a test is conducted where $\%HD_3$ is measured as a function of frequency for an input signal of 0.5 V peak-to-peak. Figure 6.15 shows the plot of HD_3 as a function of frequency. It can be seen that the distortion is maximum at 21 MHz (about a third of the bandwidth). The filter has a dynamic range of 52 dB for THD$<$1% and consumes a power of 100 mW from a 3.3 V supply. The summary of the measurement results are given in Table 6.1.

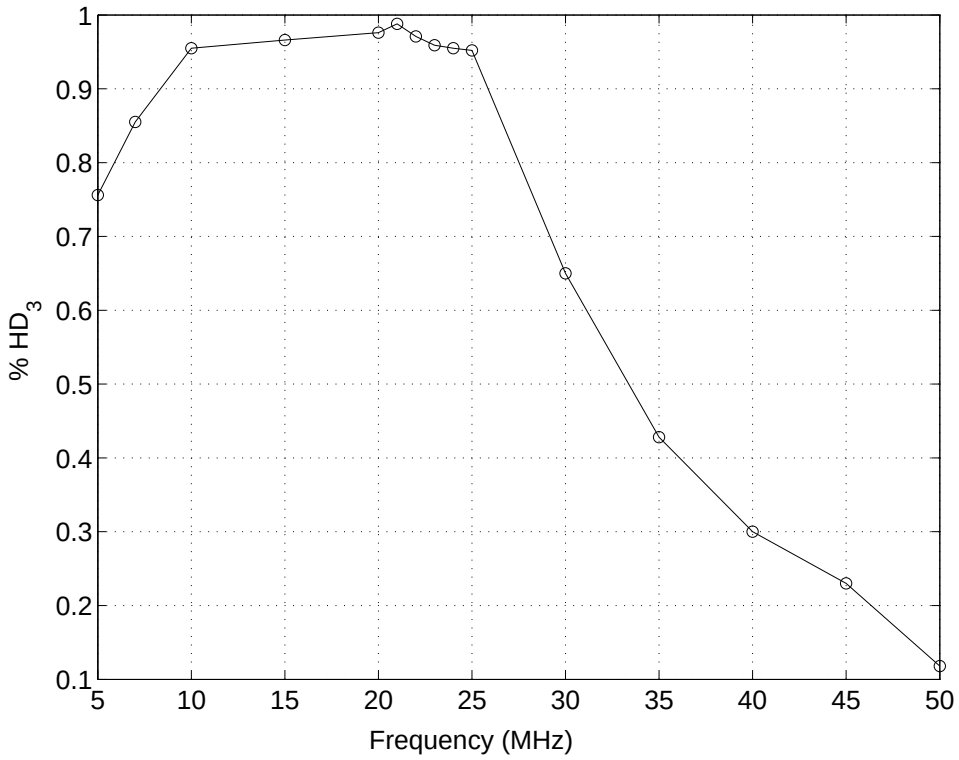


Figure 6.15: Third harmonic distortion of the filter as a function of the input frequency for an input signal of 0.5 V peak-to-peak. The filter is set to the lowest bandwidth.

Thus from the test-chip results presented in this chapter, it is seen that the proposed NQS compensation technique effectively compensates for MOS NQS effects without any power overheads, while the proposed frequency response measurement technique is found to be effective in cancelling the package feedthrough giving an improvement of about two orders of magnitude when compared the conventional method. The proposed method of noise spectral density measurement accurately estimates the noise of the filter de-embedding the noise from other sources in the chip.

Table 6.1: Summary of measurement results

Technology	0.35 μm CMOS
Filter type	5th order Chebyshev
Supply voltage	3.3 V
Bandwidth	71.4-500 MHz
Active chip area	0.65 mm^2
Power	100 mW
Integrated output noise	356 μV rms
Bandwidth variation -	
for V_{dd}= 3.3 V $\pm$10%	$\pm$0.6%
with temperature (0 - 70^{o}C)	$\pm$1.7%
Test tone at $\frac{f_{-1\mathrm{dB}}}{3}$	
$V_{in,pp}$ for THD$\leq$-40 dB	500 mV
Dynamic range for THD=-40 dB	52 dB
Stop-band attenuation measurement at the lowest bandwidth setting	
Package Details	40 pin DIP
Conventional Measurement Technique	Measured response deviated from the ideal response at 200 MHz. Filter attenuation did not reduce below about -65 dB & was sensitive to the package used.
Proposed Technique using a Vector Network Analyzer	Measured response deviated from the ideal response at around 350 MHz. Stopband response was monotonically decreasing to about -100 dB & was insensitive to the package used.
Proposed Technique using Spectrum Analyzer	Measured response deviated from the ideal response at 275 MHz. The measurements were less sensitive to the package when compared to the conventional technique.

CHAPTER 7

CONSTANT-C SCALED ACTIVE-RC FILTERS

The opamp-RC architecture is attractive, since the excellent linearity and low excess noise of active-RC integrators result in filters that dissipate very low power for a given dynamic range. However, designing high frequency opamp-RC filters is problematic since the gain-bandwidth product of the opamps in an active-RC biquad must be much larger than twice the f_oQ product of the highest quality pole pair of the filter transfer function. In practice, the opamp is replaced by an operational transconductance amplifier (OTA) with a sufficiently large transconductance to avoid the swing limitations and power dissipation associated with the design of a low output impedance stage needed in the case of an opamp Tsividis (1994). Even so, the active-RC architecture is (mostly) avoided at high frequencies due to the difficulties associated with the design of OTAs with adequate gain and bandwidth in low voltage CMOS processes.

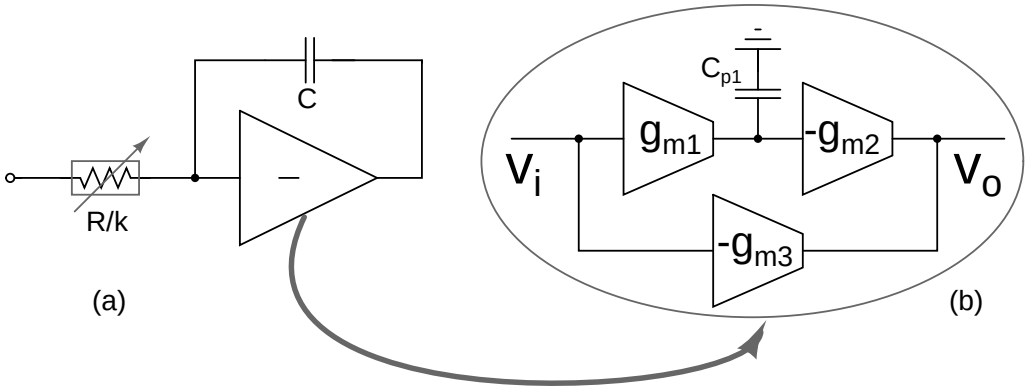


Figure 7.1: (a) The programmable integrator of Harrison and Weste (2003) and (b) single-ended block diagram of the OTA.

OTA finite gain and bandwidth issues are exacerbated when the filter bandwidth has to be programmed over a wide range. To illustrate the problems associated with

programmability, consider the digitally tuned active-RC integrator shown in Figure 7.1. The integrating resistor is tuned by means of a digital code k. The OTA is a feed forward compensated structure, proposed by Harrison and Weste (2003). g_{m1} and g_{m2} are cascaded to achieve high DC gain. g_{m3} is a feed forward transconductor, which introduces a left-half plane zero. When compared to a two stage design, this structure is advantageous due to the following. The Miller capacitor required for compensation in a two stage design needs to be charged and discharged at high frequencies, thereby necessitating significant bias current in the second stage. Since this is avoided in the feed forward compensated structure, it is fundamentally more power efficient.

To program the filter bandwidth, the typical strategy (see for example Harrison and Weste (2003)) is to vary the integrating resistors, while keeping the OTA unchanged. At low filter bandwidth settings, the excess phase of the integrator is small, resulting in a filter response close to the desired response. As the bandwidth setting is increased, integrator excess phase increases, resulting in significant Q enhancement in the filter. One solution to this problem is to design an OTA with so large a bandwidth that the integrator excess phase remains very small for all bandwidth settings. Designing such wideband OTAs would lead to significant power dissipation. It this thus seen if one is interested in minimizing power dissipation in a programmable filter, the usual strategy of tuning only the integrating resistors results in a response whose shape varies with bandwidth setting, as can be seen in several reported works (Harrison and Weste (2003) and Khorramabadi *et al.* (1996)).

In this chapter, we propose an active-RC technique that enables the design of high frequency filters while maintaining frequency response shape and dynamic range when

the bandwidth is programmed over a wide range. The basic idea is the use of the "constant-capacitance scaling" principle, hitherto applied to high speed Gm-C filters), in active-RC networks. An active-RC ladder filter is designed a 0.18 μm CMOS process to validate the proposed technique.

7.1 CONSTANT-C SCALED ACTIVE-RC INTEGRATORS

When an electrical network is constant-C scaled by a factor α, *all* the poles and zeros of that network are scaled by α. Therefore the frequency response of that network also scales by α. In a filter, when all integrators are constant-C scaled by α, the bandwidth of the filter increases by α but the shape of the response remains the same, thereby enabling wide-range programmability while maintaining performance. Figure 7.2(a) shows the

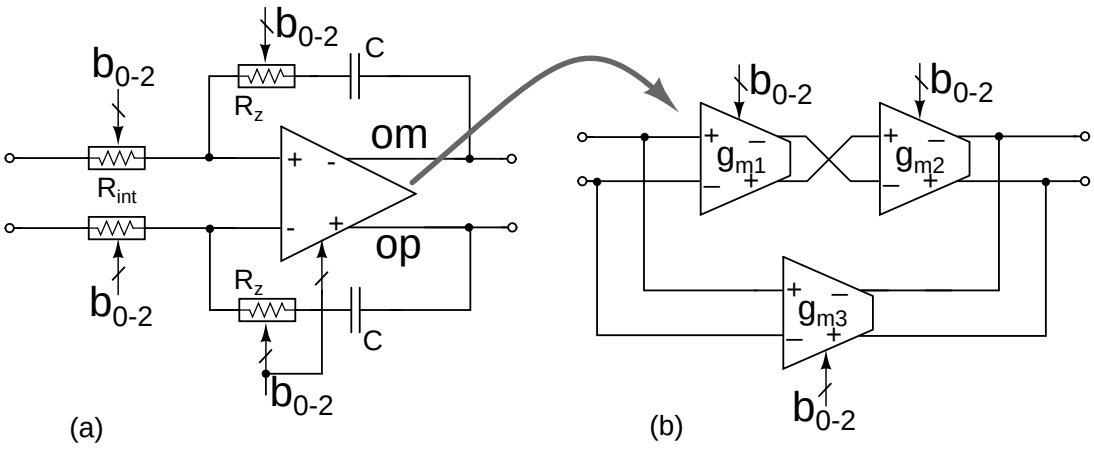


Figure 7.2: Schematic of constant-C scaled (a) active-RC integrator and (b) OTA.

constant-C programmable integrator used in this work. The OTA is a constant-C programmed version of the topology shown in Figure 7.1(b), and R_{int} and R_z are digitally programmable integrating resistors and zero-compensating resistors respectively. The implementation details are described in this section. All circuits are fully differential.

7.1.1 Programmable OTA

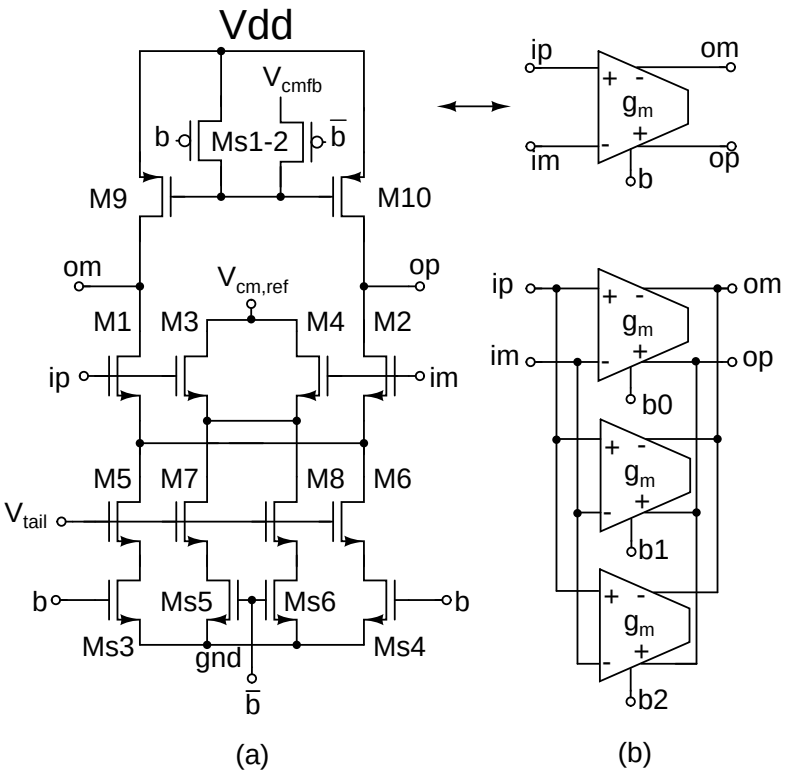
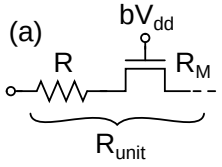
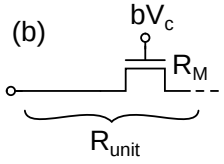
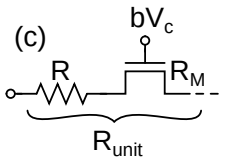


Figure 7.3: (a) Unit constant-C Gm-Cell and (b) Binary weighting of unit cells to realize a 3-bit programmable constant-C transconductor.

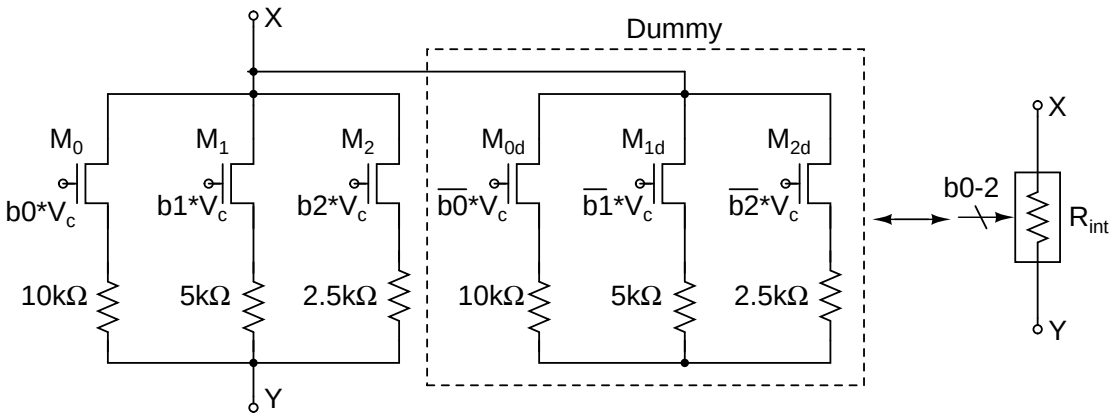
The block diagram of programmable OTA used in this work is shown in Figure 7.2(b). g_{m1} and g_{m2} form the main signal path and g_{m3} forms the feed-forward path. Each transconductor is made 3-bit programmable by connecting binary weighted constant-C unit transconductors in parallel. The schematic of the unit transconductor is shown in Figure 7.3(a) the architecture of which is similar to the unit transconductor shown in Figure 2.10. M1-M2 and M3-M4 form the main and dummy differential pairs respectively. When the main pair is "on", the dummy pair is "off" and viceversa, so as to keep the input capacitance independent of the number of unit transconductors that are "on".

Table 7.1: Choices for implementing the unit resistor

	(a) 	(b) 	(c) 
R_M/R_{unit}	$\ll 1$	1	< 1
Parasitics	Large	Small	Medium
Linearity	High	Medium	High
Control	No	Yes	Yes

7.1.2 Programmable Integrating Resistor (R_{int})

The programmable integrating resistor is realized by connecting binary weighted unit resistances in parallel. The unit resistance used for this purpose can be realized in any one of the ways shown in Table 7.1. We denote the resistance of the FET and the unit resistor by R_M and R_{unit}. Figure (a) in the table shows a switch in series with a fixed resistor (usually polysilicon resistor). The switch is made large, so that $R_M/R_{unit} \ll 1$. Though this strategy has good linearity, the large parasitic capacitances associated with the switch are problematic in high frequency filters. Also, there is no control over the integrating resistor across process and temperature. An alternative approach is to use a MOSFET, operated in triode region (figure (b) of Table 7.1). A tuning loop is used to control the conductance of the MOSFET. The parasitics of MOSFET is not of a problem as a small sized MOSFET is sufficient to realize the desired resistance. However, it suffers from poor linearity, when compared to a polysilicon resistor. Figure (c) in Table 7.1 combines the merits of Figures (a) and (b). Here, the resistance is realized as a series combination of a triode operated MOSFET resistance and a fixed resistor. The resistance of the MOSFET is made a small percentage of the total resistance. This reduces the signal swing across the MOSFET, increasing the linearity. R_{unit} can be kept



M_0, M_{0d} : 0.31/0.18 ;	M_1, M_{1d} : 2(0.31/0.18) ;	M_2, M_{2d} : 4(0.31/0.18)

Figure 7.4: Programmable integrating resistor

constant across process and temperature by tuning the MOSFET resistance.

In the active-RC ladder filter designed in this thesis, the unit resistor of a digitally programmable integrating resistor (R_{int}) is realized as in option (c) of Table 7.1. Figure 7.4 shows the complete 3-bit programmable integrating resistor. The MOS resistor (M_0) in series with a 10 kΩ high resistivity polysilicon resistor forms the LSB. The MOS resistors are controlled using logic signals b0-b2. Nodes X & Y denote the terminals of R_{int}, which are connected to the virtual ground and output nodes of the filter OTAs respectively. Dummy resistors and switches are used in an attempt to keep the capacitance at node X the same, irrespective of the bandwidth setting. M_{d0}, M_{d1} and M_{d2} are the dummies corresponding to M_0, M_1 and M_2 respectively. While similar dummies could be used at node Y, simulations show that maintaining constant-C at node Y is not so critical and hence avoided to reduce the layout complexity.

A tuning loop controls the resistance of the transistor, so that R_{int} is maintained relatively constant over process and temperature. The gate voltage of the MOS resistors is boosted above the supply voltage to reduce the size of MOS resistor (hence the

parasitic capacitances) and to improve the linearity. At the highest bandwidth setting, R_{int} is 1.667 kΩ. The MOSFET resistance is about 15% of R_{int}.

7.1.3 Programmable Zero-Compensating Resistor (R_z)

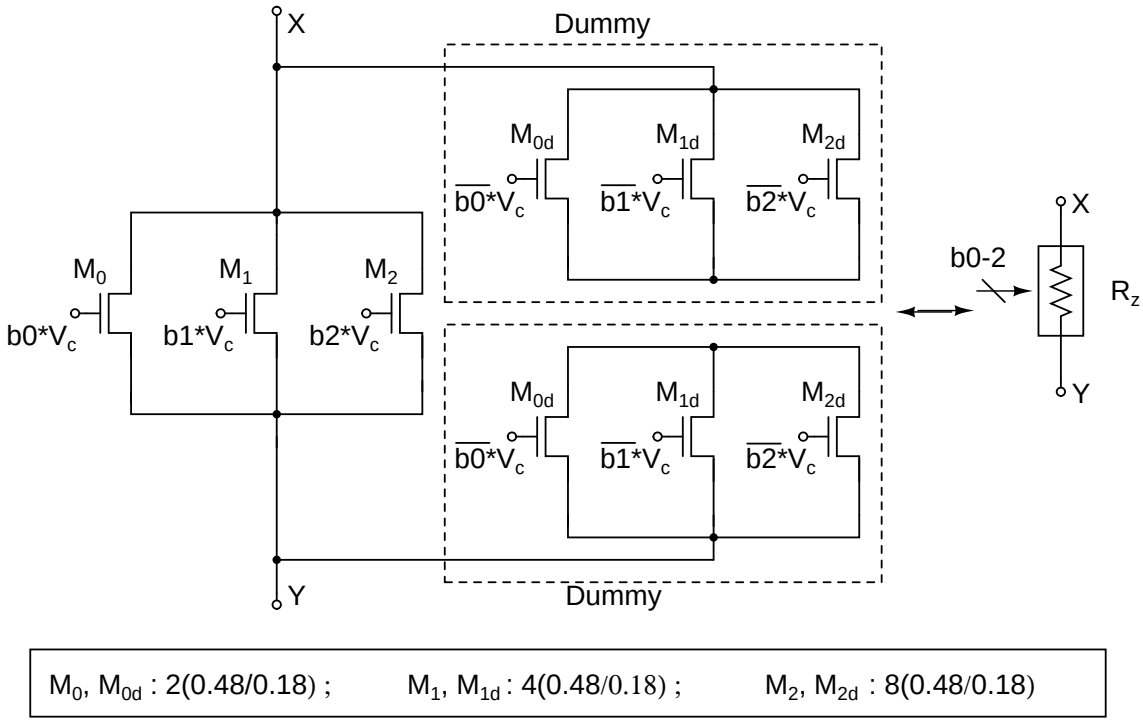


Figure 7.5: Programmable compensating resistor

The programmable resistor R_z compensates for the right half plane zero occurring because of OTA based integrator. It is realized using a bank of three binary weighted MOS transistors operated in triode region, as shown in Figure 7.5. R_z is small when compared to the impedance of the integrating capacitor in the frequency band of interest. Therefore swing across R_z is small and distortion is not an issue. Dummy transistors are used to maintain constant-C scaling. A tuning loop servoes R_z to the same stable off-chip resistor to which R_{int} is servoed.

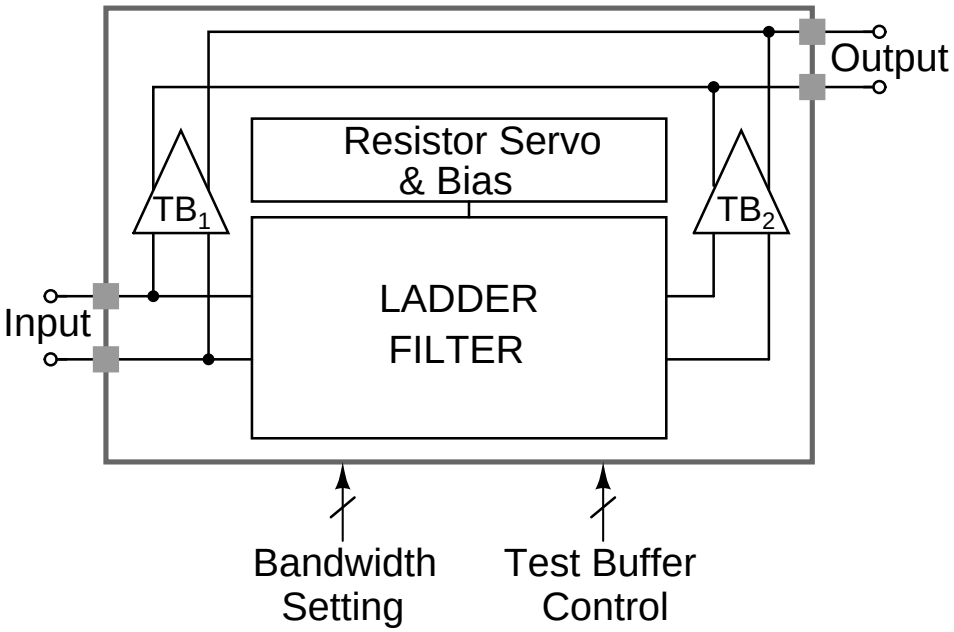


Figure 7.6: Floor-plan of the test chip.

7.2 DESIGN OF A FIFTH ORDER ACTIVE-RC LADDER FILTER

A fifth order Chebyshev active-RC filter with 1 dB pass-band ripple was designed to test the ideas presented in the previous section. The bandwidth is 3-bit digitally programmable over a 7X range from 44 MHz to 300 MHz. The filter is implemented as a singly terminated ladder. Figure 7.6 shows the floor-plan of the test chip. Apart from the filter, the chip consists of resistor-servo and bias distribution circuits. It also has two nominally identical test buffers TB_1 and TB_2 to facilitate accurate characterization of the frequency response.

A single-ended node-scaled version of the filter is shown in Figure 7.7. The element values shown are for the highest bandwidth setting of 300MHz. Metal-Insulator-Metal (MIM) capacitors are used as the integrating elements. The proposed constant-C scaled active-RC integrator, explained in the previous section, forms the building block of the filter. The tail currents of the differential pairs in the OTA are derived from a fixed

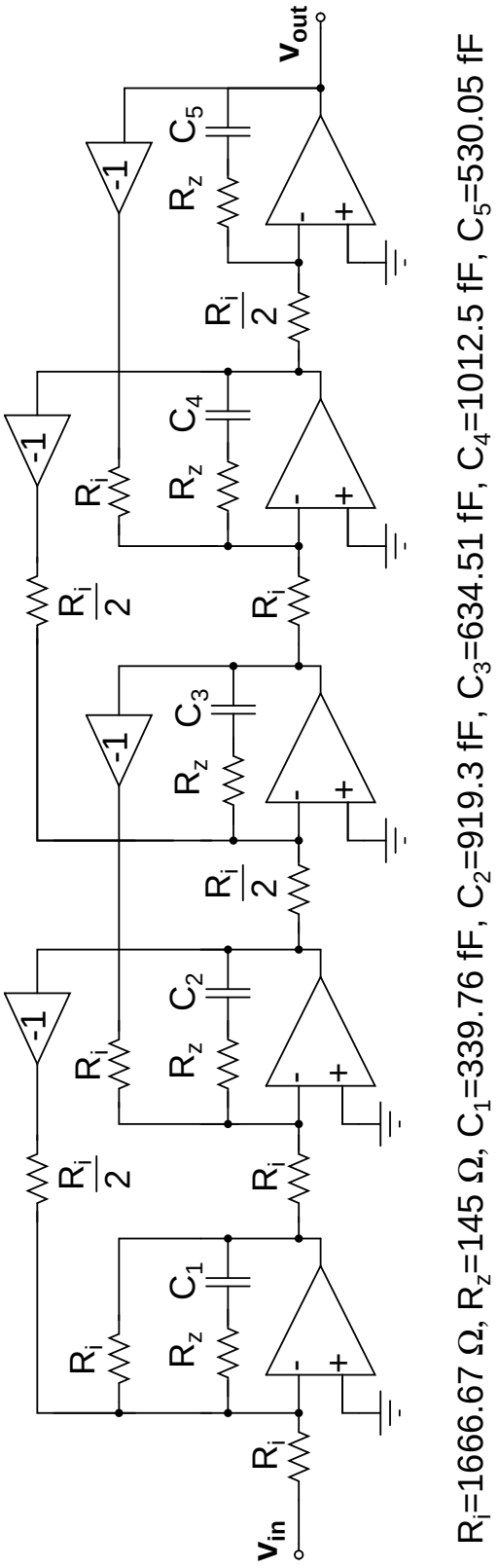


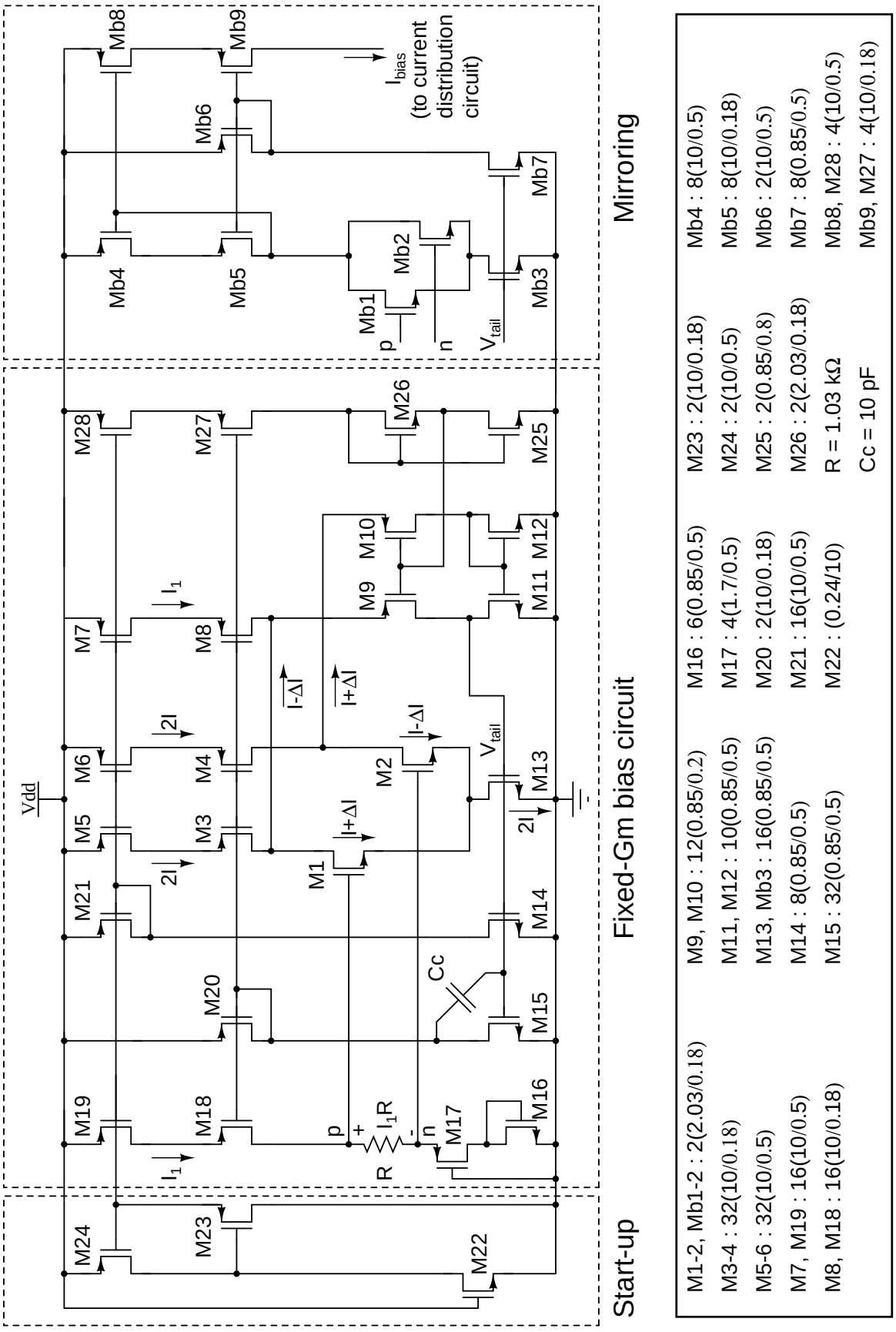
Figure 7.7: Single ended schematic of the filter - component values are for the highest bandwidth setting.

transconductance bias circuit that servoes the transconductance of the OTA to an off-chip stable resistor keeping the transconductance stable across process and temperature variations. The fixed-Gm bias circuit and the bias distribution scheme are similar to those explained in chapter 2. The schematic of fixed-Gm bias and the bias distribution circuit is shown in Figure 7.8 and 7.9 respectively.

7.2.1 Common-Mode Feedback circuit

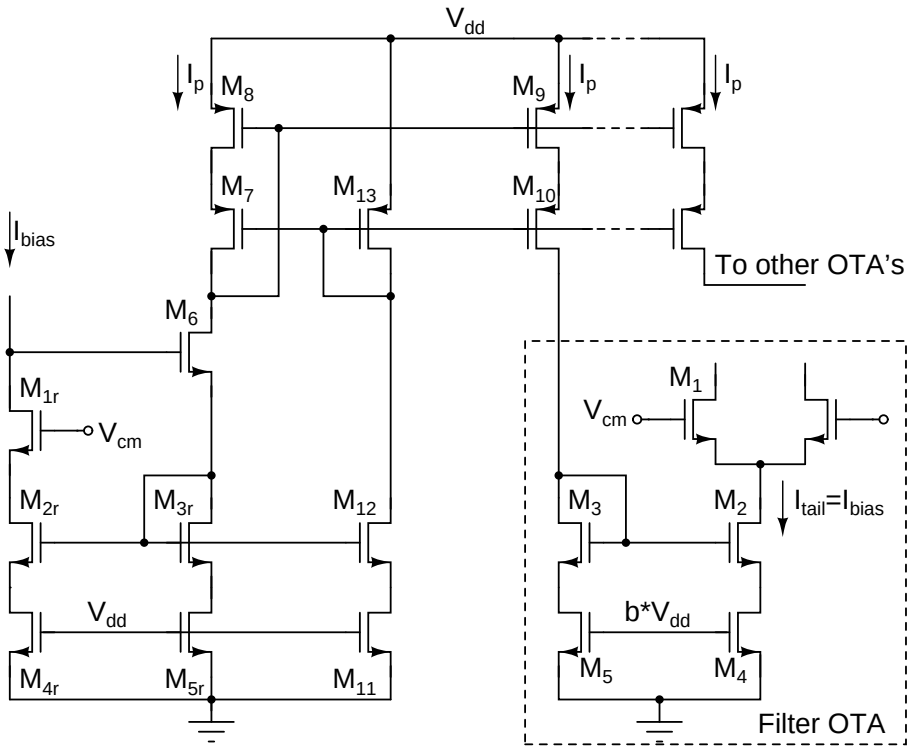
The common-mode output of each stage of the OTA is fixed by a separate common-mode feedback (CMFB) circuit. Figure 7.10 shows the CMFB circuit that fixes the common-mode of the second stage (i.e. output) of OTA. A resistor based common-mode sensing is used. R_{CM} is the common mode sensing resistor. The detected common mode is compared with a common-mode reference voltage (generated on-chip) and the resulting error is amplified using an error amplifier formed by M_1- M_5. C_c is the compensating capacitor (2 pF) for stabilizing the common-mode loop. M_6-M_7 forms a NMOS source follower and drives the large C_c. C_{CM}s are small capacitors (30 fF) used to compensate for the pole formed by R_{CM} and the input capacitance of the error amplifier.

In order to keep the common-mode sensing circuit simple, R_{CM} is kept constant (i.e. R_{CM} do not scale with the bandwidth setting). Since, differentially, R_{CM} is in parallel with the load on OTA, care has been taken in choosing R_{CM} so that its influence is minimum on constant-C scaling. A similar CMFB circuit fixes the common-mode of the first stage output of OTA.



M1-2, Mb1-2 : 2(2.03/0.18)	M9, M10 : 12(0.85/0.2)	M16 : 6(0.85/0.5)	M23 : 2(10/0.18)	Mb4 : 8(10/0.5)
M3-4 : 32(10/0.18)	M11, M12 : 10(0.85/0.5)	M17 : 4(1.7/0.5)	M24 : 2(10/0.5)	Mb5 : 8(10/0.18)
M5-6 : 32(10/0.5)	M13, Mb3 : 16(0.85/0.5)	M20 : 2(10/0.18)	M25 : 2(0.85/0.8)	Mb6 : 2(10/0.5)
M7, M19 : 16(10/0.5)	M14 : 8(0.85/0.5)	M21 : 16(10/0.5)	M26 : 2(2.03/0.18)	Mb7 : 8(0.85/0.5)
M8, M18 : 16(10/0.18)	M15 : 32(0.85/0.5)	M22 : (0.24/10)	R = 1.03 kΩ	Mb8, M28 : 4(10/0.5)
			Cc = 10 pF	Mb9, M27 : 4(10/0.18)

Figure 7.8: Fixed-Gm bias circuit



M_1, M_{1r} : 2(2.03/0.18)	$M_{5,}$ M_{5r} : 8(1.16/0.18)	M_{11}, M_{12} : 6(1.16/0.18)
$M_{2,}$ M_{2r} : 12(1.16/0.18)	M_6 : 16(1.16/0.18)	M_{13} : 2(10/1)
$M_{3,}$ M_{3r} : 8(1.16/0.18)	M_8, M_9 : 8(10/0.5)	
$M_{4,}$ M_{4r} : 12(1.16/0.18)	M_7, M_{10} : 8(10/0.5)	

Figure 7.9: Current distribution circuit

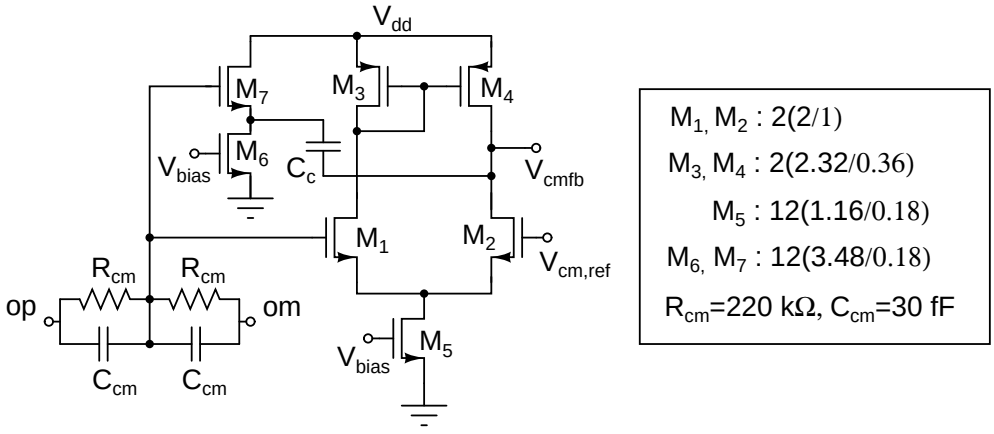


Figure 7.10: Common-mode feedback circuit

7.2.2 Resistor Servo Circuit

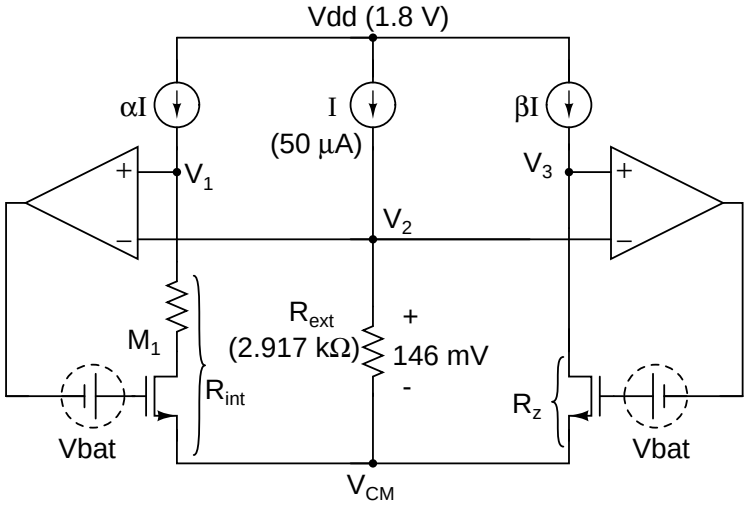


Figure 7.11: Simplified schematic of the resistor servo loops.

As mentioned in the previous section, the MOS resistors used in R_{int} and R_z are servoed to an off-chip stable resistor and their gate voltage is boosted above the supply voltage. It was decided to have a control voltage in the vicinity of 3.3V. Figure 7.11 shows a simplified schematic of the resistor servo loop. R_{ext} is the off-chip resistor to which R_{int} and R_z are servoed. The working of this circuit can be explained as follows. Consider the servo loop containing R_{int}. The Opamp $A1$ forces the voltage V_1 to be equal to V_2 by changing the gate voltage of M_1. When this happens, $I \times R_{ext}$=$\alpha I \times R_{int}$.

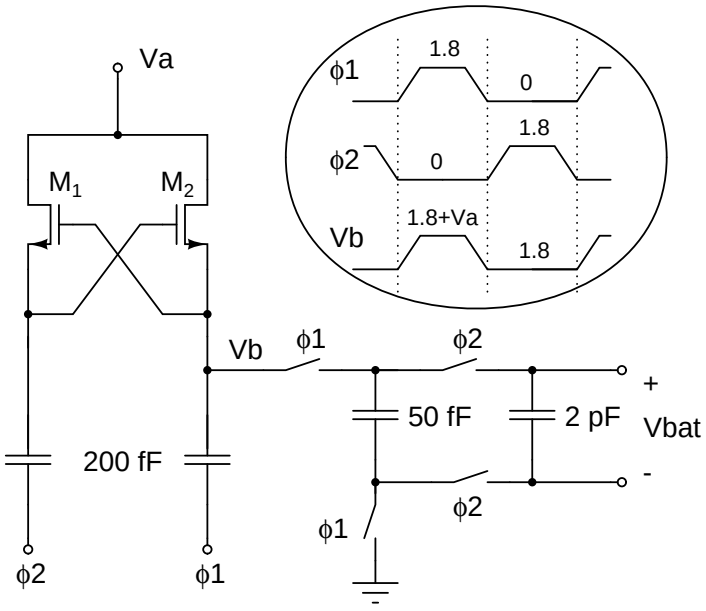


Figure 7.12: Charge pump based battery generator

In other words, R_{int} is adjusted to a value R_{ext}/α. A similar analysis holds for servo loop containing R_z, in which case, R_z=R_{ext}/β.

Since the complete servo circuit works with a 1.8 V supply, the boosting of the gate voltages above the supply voltage is done by connecting a "battery" in series with the opamp output. The battery is realized by a capacitor charged to a DC voltage using a charge-pump based circuit. Figure 7.12 shows the charge-pump based battery generator. The timing diagram is shown in the inset. In the steady state, $Vbat = Vdd + Va = 1.8 + Va$. $Vbat$ is suitably set so as to give a sufficient headroom for the opamps to adjust its output for any variations in the resistance. The charge pump circuit is designed to operate at 1MHz.

7.2.3 Test Buffers

Two nominally identical test buffers (TB_1 and TB_2) are used to drive the external loads (the measuring instrument), since the filter is not designed to drive these large

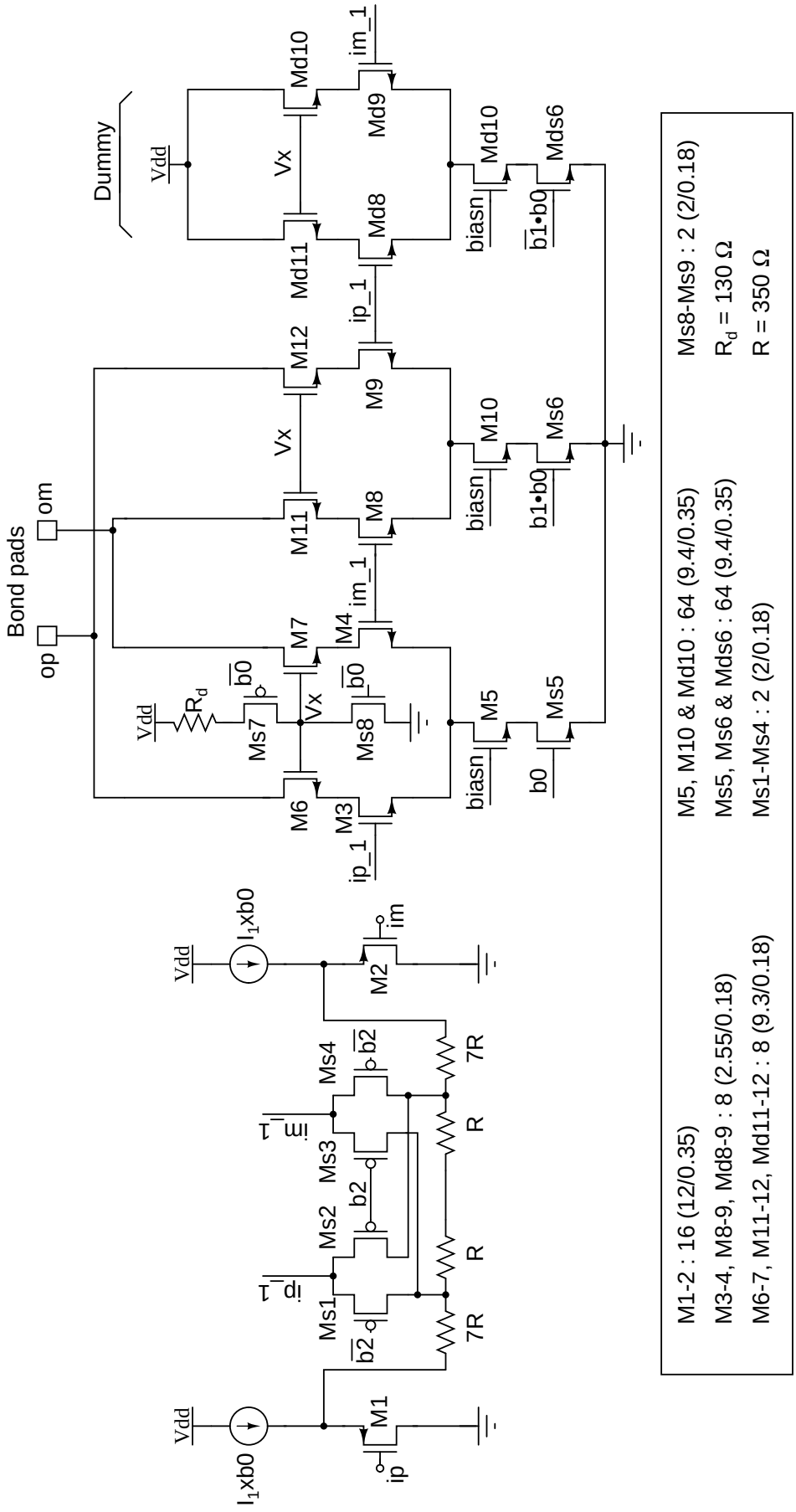


Figure 7.13: Schematic of the test buffer

loads. The outputs of these test buffers are tied on-chip and a single differential output is brought out of the chip. Only one test buffer will be on at a given time. The scheme used for the filter characterization is same as that discussed in chapter 5. Baluns are used at the input and output of the chip for the single ended to differential conversion of the signal and vice-versa.

Figure 7.13 shows the simplified schematic of the test buffer used in the filter chip. The architecture is similar to the test buffer designed for the Gm-C filter in chapter 5, except that in the test buffer used here, the output of the first stage (the source follower) is attenuated by a factor of 8 before feeding it to the next stage (the differential pair) using a resistive potential divider. This is done to avoid the linearity issues related to the second stage as the filter is designed to work at a differential swing of 2 V peak-to-peak. The test buffer is operated at 3.3 V supply to minimize the distortion introduced by it. Each test-buffer takes a total current of 21 mA from the supply.

The test buffer has three control bits $b0$, $b1$ and $b2$. Bit $b0$ turns on/off the test buffer. When $b0$ is low, all the current sources are switched OFF, turning off the buffer completely. Bit $b0$ also controls the switches Ms4-Ms5, turning the bias for the cascode transistors of the differential pair on/off, which ensures virtually that no signal leaks to the output from the input when the test buffer is turned off. A high on $b0$ turns the test buffer ON. The the test buffer has the gain programmability. The control bit $b1$ sets the gain. A high on $b1$ adds the differential pair M7-M8 in parallel with the differential pair M3-M4, doubling the gain. When M8-M9 are turned off, a dummy differential pair Md8-Md9 is turned on so as to ensure that the capacitance at the nodes ip_1 and ip_2 remain unaltered. Control bit $b2$ enables to multiply the test buffer gain by ± 1, which

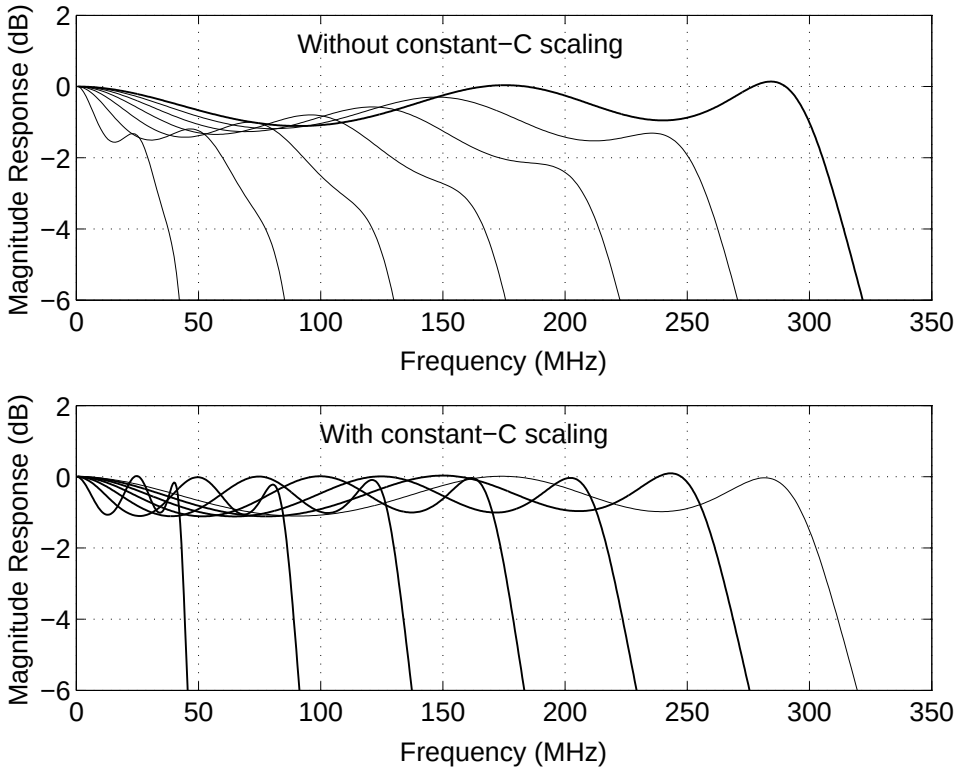


Figure 7.14: Simulated filter response (a) without constant-C scaling, only R_{int} is varied to change bandwidth and (b) with constant-C scaled OTA, R_{int} and R_z.

is necessary for the accurate measurement of the filter frequency response. Ms1-Ms4 are the cross-coupled switches used for this purpose.

7.3 SIMULATION RESULTS

To illustrate the benefits of constant-C scaling in active-RC filters, the following two simulations were run on the layout extracted netlist of the filter designed in the previous section.

1. Without constant-C scaling: Only the integrating resistors R_{int} are programmed to vary the bandwidth and the OTA and R_z are fixed to the highest bandwidth.
2. With constant-C scaling: Constant-C scaled OTA, R_{int} and R_z are used.

Figure 7.14 shows the simulated passband responses of the filter for the above cases.

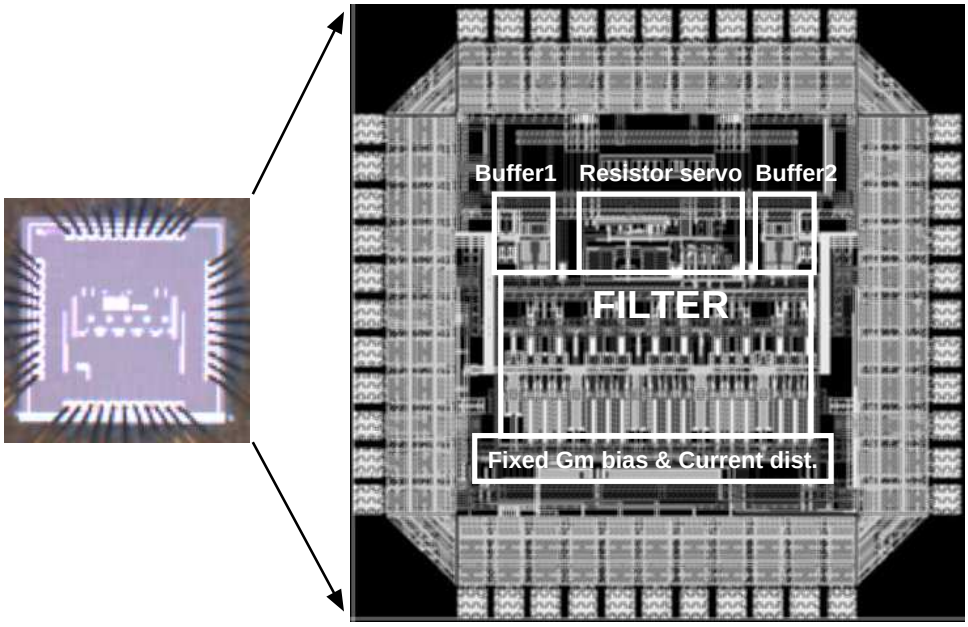


Figure 7.15: Die photograph and top-level layout.

Part (a) shows the simulated responses without constant-C scaling. Notice that while the response at the highest bandwidth setting is as desired, it progressively droops at the band-edge as the set bandwidth is reduced. At the lowest bandwidth setting, the third maximum characteristic of the Chebyshev response has drooped by more than 6 dB. Figure 7.14(b) shows the simulated passband responses when a constant-C scaled OTA, R_{int} and R_z are used. The dramatic improvement in performance is apparent. It can be noticed that the shape of the response is preserved when the filter bandwidth is varied across its tuning range.

7.4 EXPERIMENTAL RESULTS

The filter test-chip was fabricated in a UMC 0.18 μm CMOS process through Europractice. The die photograph and the top level layout of the chip are shown in Figure 7.15. The active area of the filter is 0.63 mm^2. The chip was packaged in a 44-pin J-leaded chip carrier (JLCC) package. The pinout of the packaged chip and the func-

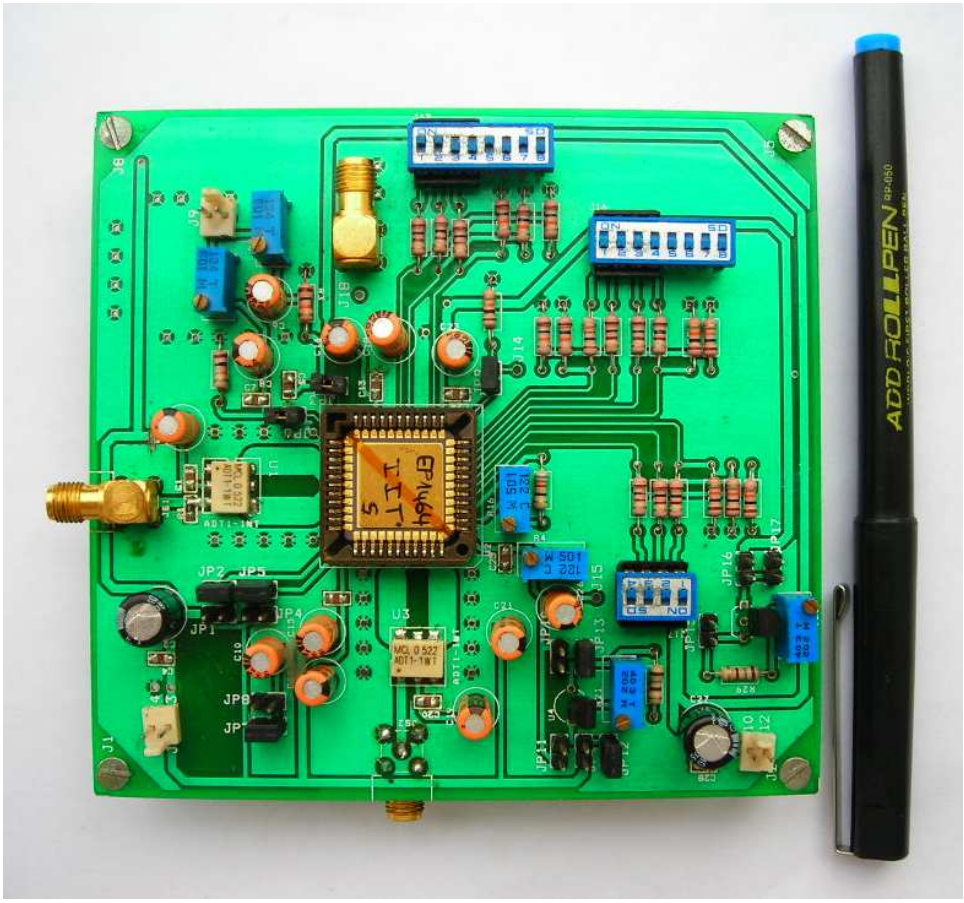


Figure 7.16: Photograph of the test board.

tionality of the pins are given in appendix D. A two-layered PCB was designed for testing the fabricated chip. Figure 7.16 shows a photograph of the PCB.

Figure 7.17 shows the measured frequency response of the filter for all bandwidth settings and the passband details are shown in the inset. Note that the shape of the response remains virtually unaltered in spite of being programmed over a 7X range. Thanks to constant-C scaling. Figure 7.18 shows the normalized response of 15 chips on the same plot, at the highest and lowest (in the inset) bandwidth settings. All the chips were measured under identical test conditions. Good repeatability is seen.

Figure 7.19 shows the measured IIP3 of the filter as a function of frequency with the filter set at lowest bandwidth (44 MHz). The lowest IIP3 is 2.5 V rms and occurs

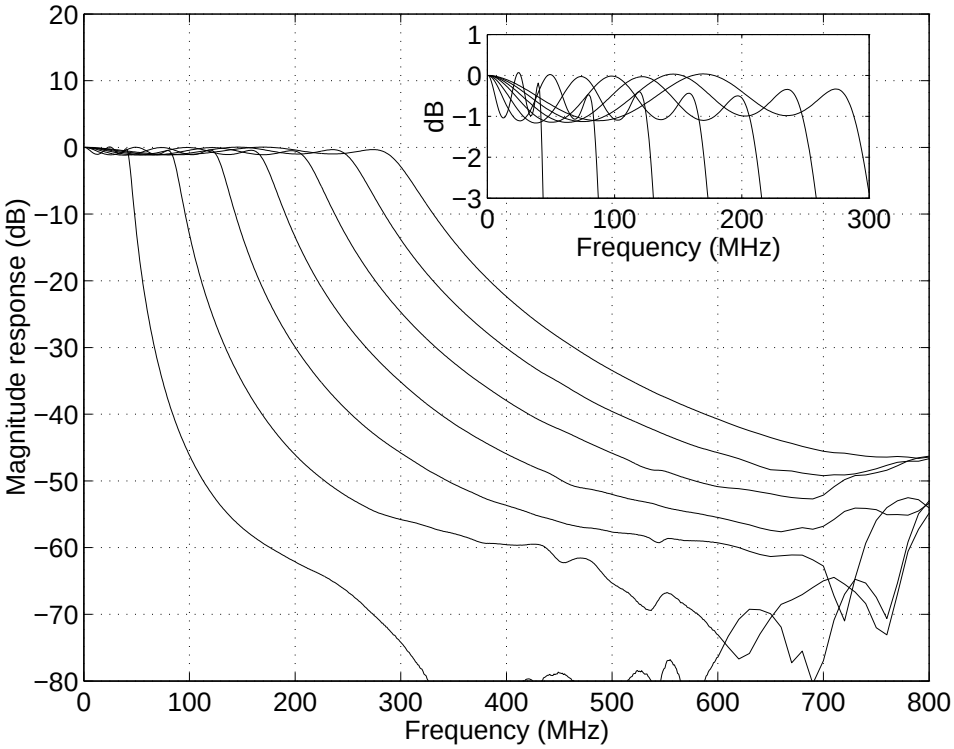


Figure 7.17: Measured frequency response across all bandwidth settings.

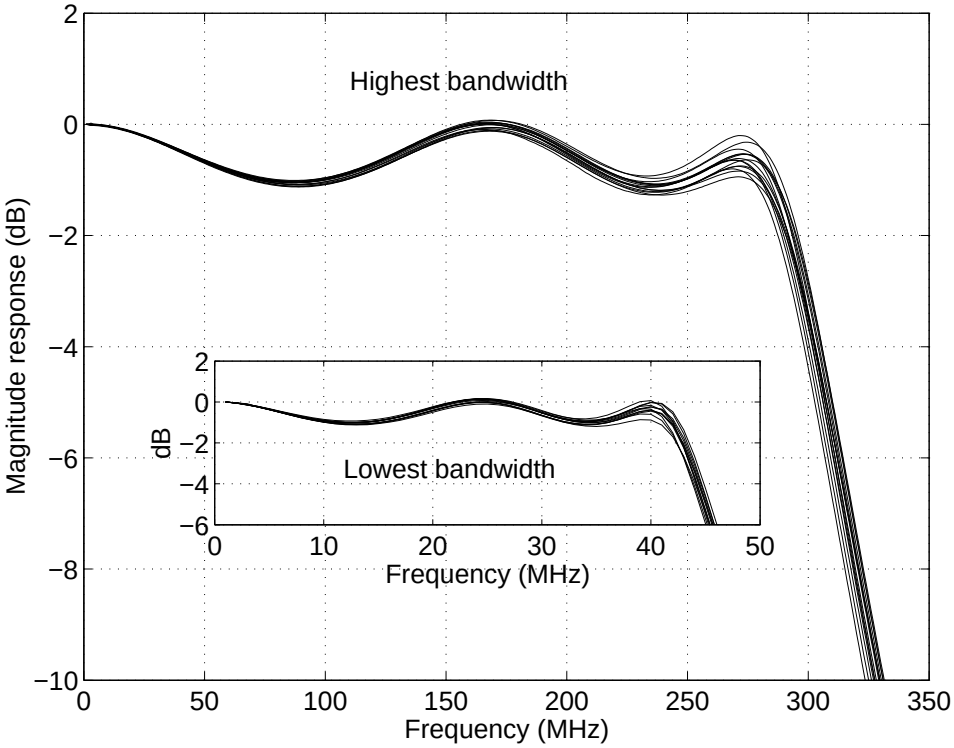


Figure 7.18: Passband detail for 15 chips at the highest and lowest bandwidth setting.

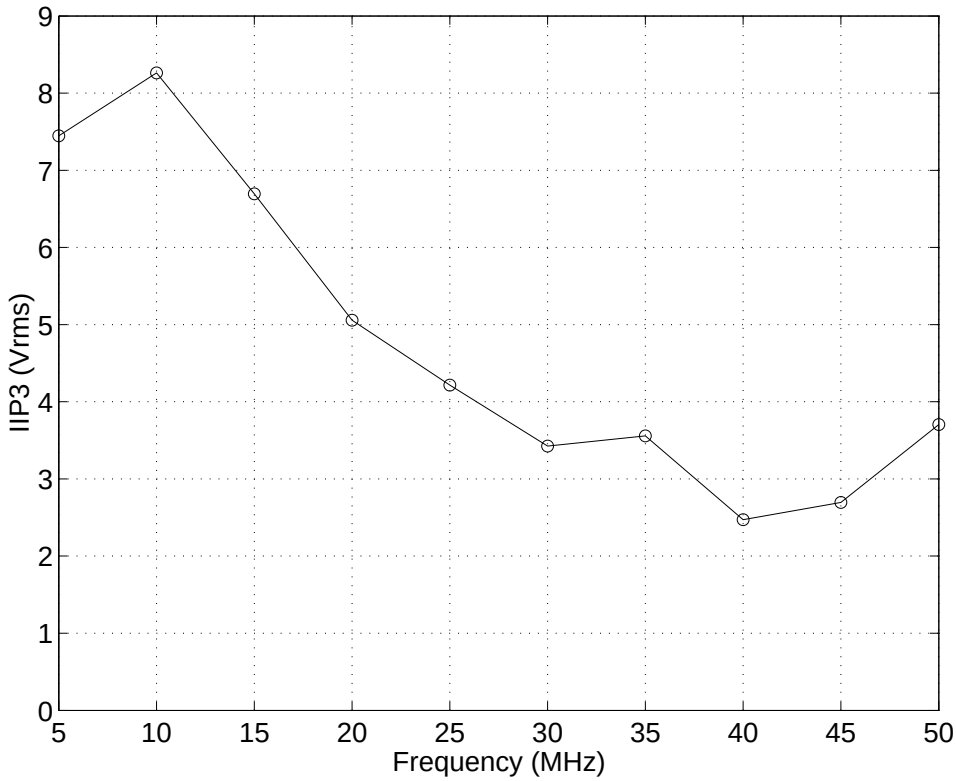


Figure 7.19: Measured IIP3 of the filter as a function of frequency for the lowest bandwidth setting

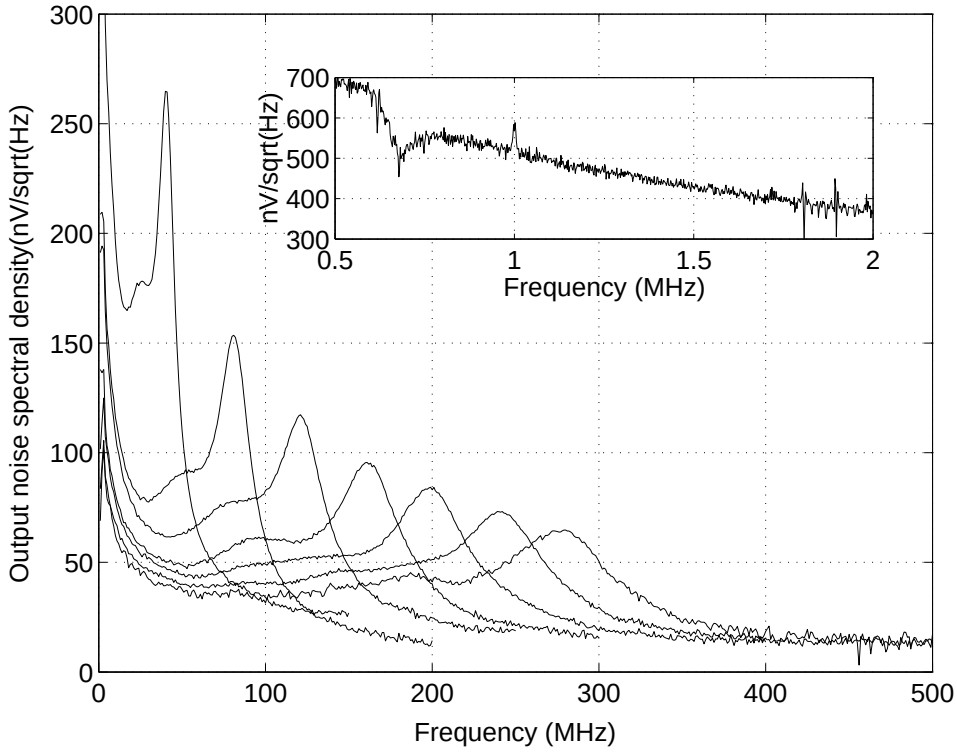


Figure 7.20: Measured noise spectral density of the filter

at the band-edge since all the integrating nodes swing almost equally at the band-edge. The use of poly-resistor based active-RC integrators results in excellent filter linearity - when a 2.2 V (peak-to-peak differential) input tone at one third of the band-edge frequency is applied to the filter, the third harmonic distortion was 1%. The measured output noise spectral density of the filter across the bandwith settings is shown in Figure 7.20. In the inset, plotted the noise spectral density around 1 MHz for the lowest bandwidth. The small tone seen at 1 MHz is due to the clock feedthrough. The RMS output noise of the filter was measured to be 860 μV, without considering the clock feedthrough, resulting in a dynamic range of 56.6 dB for 1% THD. The filter consumes 54 mW at 1.8 V supply. Table 7.2 summarizes the measured results.

Table 7.2: Summary of measurement results of active-RC filter chip

Technology	0.18 μm CMOS
Filter type	5th order Chebyshev, Opamp-RC
Supply voltage	1.8 V
Bandwidth	40-300 MHz
Active chip area	0.63 mm^2
Power	
OTAs + CMFB circuits	54 mW
Fixed-Gm bias circuit	3 mW
Current distribution circuit	5.9 mW
Resistor servo circuit	2.7 mW
Integrated output noise	860 μV rms
IIP3 @ band-edge (when set to lowest bandwidth)	2.5 V rms
Test tone at $\frac{f_{-1\mathrm{dB}}}{3}$ for the lowest bandwidth	
$V_{in,pp}$ differential for THD$\leq$-40 dB	2.2 V
Dynamic range for THD=-40 dB	56.6 dB

Table 7.3 compares the present work with some of the published filters. A figure of merit (FOM) is used for the comparison and is given in (7.1).

$$FOM = \frac{P_{diss}}{p \times f_o \times Q_{max} \times DR^2} \tag{7.1}$$

where, P_{diss} is the power dissipated (Watts), p is the number of filter poles, f_o is the filter cut-off frequency (Hertz), Q_{max} is the maxmimum Q of the filter and DR is the dynamic range of the filter. The unit of FOM is Joules (J). From the Table 7.3 the Gm-C filters have poor FOM compared to their counterparts. This is expected as Gm-C filters are power hungry for a given dynamic range. Comparing our active-RC filter with the filter presented by Harrison and Weste (2002), both the filters have the same OTA architectures and the OTAs consume same power (4 mA at 1.8 V) but the former has the better FOM with the merit of preserving the frequency response shape over the tuning range. The active-RC filter presented in (Harrison and Weste (2003)), uses power optimized OTAs with two feedforward loops. Thus has a better FOM, but with a short-fall that the shape of the frequency response is bandwidth dependent.

Thus it is shown that constant-C scaling applied to active-RC integrators allows the realization of widely programmable active-RC filters while preserving the shape of the frequency response intact when the bandwidth is programmed over the tuning range.

Table 7.3: Comparison with some of the published filters

Reference	Bandwidth (MHz)	Order	Supply voltage (V)	Power (mW)	Q_{max}	Dynamic range (dB) (for THD $\approx$ -40 dB unless specified)	Topology	Technology	FOM (aJ)	Comments
Harrison and Weste (2002)	350	5	1.8	25.2	3.1	52	Active-RC	0.18 μm CMOS	29.3	–
Harrison and Weste (2003)	500	5	1.8	90	3.1	64	Active-RC	0.18 μm CMOS	4.6	–
Panday *et al.* (2006)	550	4	$\pm$1.65	140	1.065	40	Gm-C	0.35 μm CMOS	5781	–
Chen *et al.* (2003)	200	4	2.3	72	1.065	52	Gm-C	0.35 μm CMOS	651.6	THD=44 dB
Bollati *et al.* (2001)	120	8	2.5	120	1.5	45	Gm-C	0.25 μm CMOS	2633	–
This thesis	500	5	3.3	100	5.55	52	Gm-C	0.35 μm CMOS	45.4	–
This thesis	300	5	1.8	54	5.55	56.6	Active-RC	0.18 μm CMOS	14.1	–

CHAPTER 8

CONCLUSIONS AND FUTURE DIRECTIONS

In this thesis, we addressed the issues of accurate design and characterization of high frequency continuous-time filters. An efficient design centering technique was proposed for ensuring the filter response is indeed the desired one, even in the presence of layout parasitics. The proposed design centering technique drastically reduces the design time.

The influence of non-quasi-static effects of the MOS transistors on the high frequency continuous-time filters was analyzed. A simple technique to compensate for these non-quasi-static effects is presented. The technique requires less hardware and is free from the problem of clock feedthough unlike conventional Q-tuning techniques.

Two novel techniques that enable accurate measurement of the frequency response of on-chip high frequency filters in the face of package feedthrough were presented. The first technique, using a VNA, results in a dramatic increase in the precision and frequency range over which accurate measurements become possible. A second technique, which uses only magnitude measurements, is an improvement over the conventional technique but not quite as effective as the VNA based technique. A technique to accurately measure the noise spectral density of on-chip filters, accounting for the frequency response of the package and test-setup, as well as the noise of the test buffers was presented.

A widely programmable fifth order lowpass Chebyshev Gm-C ladder filter was designed in a 0.35 μm CMOS process to validate the proposed ideas. The filter bandwidth

is digitally programmable with 3-bits from 71.4–500 MHz and has a passband ripple of 1 dB. Measurements from fabricated chips confirm our theory. The filter achieved a dynamic range of 52 dB consuming a power of 100 mW from a 3.3 V supply.

We proposed a constant-C scaled active-RC integrator that enables the realization of widely programmable high frequency active-RC filters whose frequency response shape and dynamic range are maintained over the entire tuning range. A fifth order active-RC ladder filter was deigned in a 0.18 μm CMOS process. The bandwidth is digitally programmable from 44–300 MHz. The efficacy of the proposed technique was proved by the test-chip results. The filter has a dynamic range of 56.6 dB and consumes 54ṁW of power from a 1.8 V supply.

8.1 FUTURE DIRECTIONS

A simplified space-mapping was sufficient for design centering the filter designed in this work due to fact that the coarse model of the filter was simply a translated version of the actual filter. For complicated filters like higher order active-RC filters, it may not be possible to arrive at a coarse model which is just a translated version of the actual filter. Investigations on applying advanced space mapping techniques to such filters are required.

Constant-C scaling in high frequency active-RC filters is limited by the integrating resistor, for the architecture used in this thesis. At higher frequencies, the presence of parasitic capacitances make the integrating resistor to violate constant-C scaling principle, since the unit resistor which is turned off, is not isolated completely from the circuit. Work towrads achieving a true constant-C scaled integrating resistor is necessary.

APPENDIX A

EFFECT OF THE PARASITIC POLE OF A TRANSCONDUCTOR ON ω_o AND Q OF A Gm-C BIQUAD

The transfer function of a biquadratic lowpass filter is given as

$$H(s) = \frac{1}{\left(\frac{s}{\omega_o}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_o}\right) + 1} \tag{A.1}$$

Given a biquadratic lowpass filter, to find ω_o one finds the frequency at which the phase of the filter transfer function $H(j\omega)$ reaches $-\pi/2$. Q is the gain of the filter at ω_o.

When the integrators of the biquad have parasistic pole at $1/\tau_1$, the modified transfer function of the filter can be obtained by replacing s in (A.1) by $s(1+s\tau_1)$ as given below

$$H'(s) = \frac{1}{\frac{s^2(1+s\tau_1)^2}{\omega_o^2} + \frac{1}{Q}\frac{s(1+s\tau_1)}{\omega_o} + 1} \tag{A.2}$$

Expanding and rearranging the terms,

$$H'(s) = \frac{1}{\frac{s^2}{\omega_o^2}(1 + s^2\tau_1^2 + 2s\tau_1) + \frac{1}{Q}\frac{s}{\omega_o}(1 + s\tau_1) + 1} \tag{A.3}$$

$$H'(j\omega) = \frac{1}{1 - \frac{\omega^2}{\omega_o^2}\left(1 - \omega^2\tau_1^2 + \frac{\tau_1}{Q\omega_o}\right) + j\frac{1}{Q}\frac{\omega}{\omega_o}\left(1 - \frac{2\omega^2\tau_1 Q}{\omega_o}\right)} \tag{A.4}$$

To find the modified value of ω_o (denoted as ω_o'), we find the frequency at which

$\angle H'(j\omega) = \pi/2$, as per the definition given earlier in this appendix. In other words, ω'_o is the frequency at which the real part of denominator in $H'(j\omega)$ becomes zero. i.e. at ω'_o,

$$1 - \frac{(\omega'_o)^2}{\omega_o^2}\left(1 - (\omega'_o)^2\tau_1^2 + \frac{\tau_1}{Q\omega_o}\right) = 0 \tag{A.5}$$

Assuming $(\omega'_o)^2\tau_1^2 \ll 1$,

$$\omega'_o \approx \frac{\omega_o}{\sqrt{1 + \frac{\omega_o\tau_1}{Q}}} \tag{A.6}$$

$$\approx \omega_o\left(1 - \frac{\omega_o\tau_1}{2Q}\right) \tag{A.7}$$

$$\Rightarrow \quad f'_o \approx f_o\left(1 - \frac{\pi f_o\tau_1}{Q}\right) \tag{A.8}$$

Denote Q' as the modified Q of the filter. By definition of Q, $Q' = |H'(j\omega)|_{\omega=\omega'_o}$. Therefore we can write,

$$\frac{1}{Q'} = \frac{1}{Q}\frac{\omega'_o}{\omega_o}\left(\frac{2\omega'^2_o\tau_1 Q}{\omega_o}\right) \tag{A.9}$$

Substituting (A.8) in (A.9) for ω'_o, for a biquad with large Q>1, Q' can be approximated as

$$Q' = \frac{Q}{1 - 4\pi f_o Q\tau_1} \tag{A.10}$$

APPENDIX B

PIN DETAILS OF THE Gm-C FILTER CHIP

Figure B.1 shows the pinout of the packaged chip. The functional details of the pins are given in Table B.1.

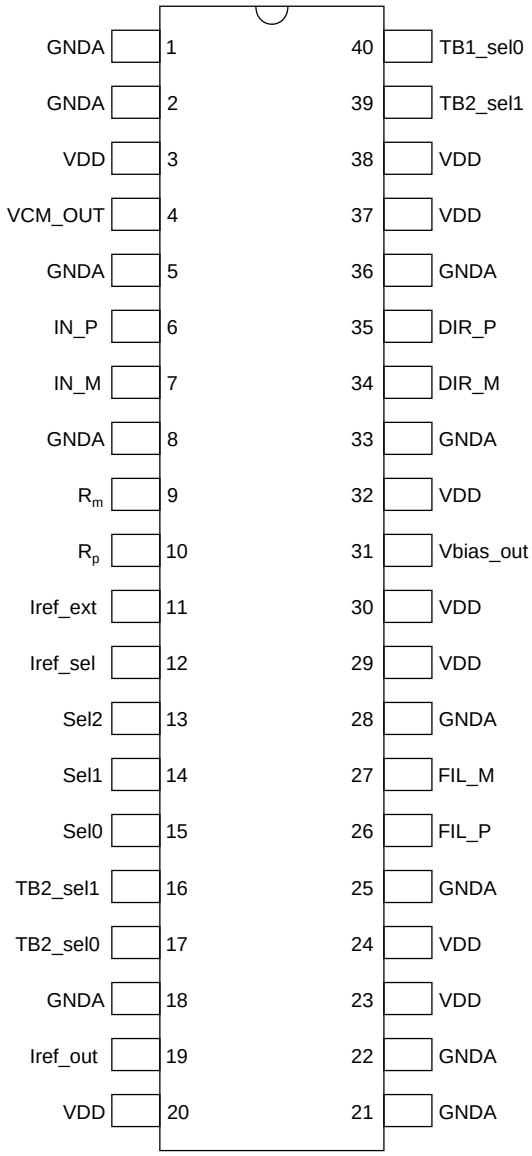


Figure B.1: Pinout of the packaged chip

Table B.1: Functionality of pins of Gm-C filter chip

Pin number	**Pin Name**	**Functionality**
1, 2, 5, 8, 18, 21, 22, 25, 28, 33 & 36	$GNDA$	Ground
3, 20, 23, 24, 29, 30, 32, 37 & 38	VDD	Supply voltage (3.3 V nominal)
4	VCM_OUT	Common-mode reference output. Used to test/tap the common-mode reference voltage generated on-chip.
6 7	IN_P IN_M	Differential analog input.
9 10	R_m R_p	Stable resistance for the fixed-Gm bias circuit is connected between these two pins.
11 12	$Iref\_ext$ $Iref\_sel$	$Iref\_sel$ is the control to select between an internal fixed-Gm bias circuit or an external current $Iref\_ext$.
13–15	$Sel2$, $Sel1$ and $Sel0$	3-bit select lines setting the bandwidth of the filter. $Sel0$ is the LSB.
16 17	$TB2\_sel1$ $TB2\_sel0$	Control bits for test buffer TB2.
19	$Iref\_out$	A test pin, where the transconductor bias current is brought out.
26 27	FIL_P FIL_M	Filter path differential output.
31	$Vbias\_out$	Bias voltage for the cascoded transistors of Gm-cell.
34 35	DIR_M DIR_P	Direct path differential output.
39 40	$TB2\_sel1$ $TB2\_sel0$	Control bits for test buffer TB1.

APPENDIX C

LM334 BASED CURRENT SOURCE/SINK

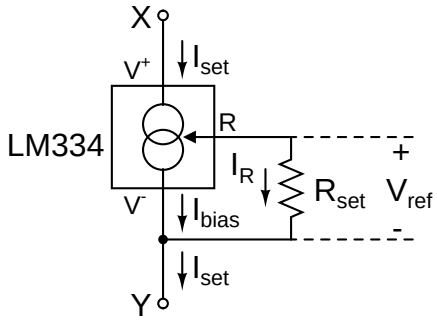


Figure C.1: Basic current source using LM334

LM334 is a three terminal adjustable current source (from National Semiconductor). A basic current source circuit using LM334 is shown in Figure C.1. The current source is built between the node-X and node-Y where X is at higher potential than Y. The three terminals of LM334 are named V^+, R and V^-. LM334 generates a constant voltage V_{ref} between R and V^- for a given temperature, which is approximately given by 214 μV/^{o}K. An external resistance R_{set} sets the current I_R between terminals R and V^-. I_{bias} is the current consumed in LM334 for producing I_R. Therefore the current set I_{set} by the current source is given as -

$$I_{set} = \frac{V_R}{R} + I_{bias} \tag{C.1}$$

The bias current I_{bias} depends on I_R. A typical ratio $\frac{I_{set}}{I_{bias}}$ is about 18 for 2 μA $<$ I_{set} $<$ 1 mA. Using this value, in (C.1), the resistance R_{set} required to generate a given

Table C.1: Jumper settings

Jumper setting	**Operation**
$J1$, $J5$	Current sink
$J2$, $J4$	Current source
$J3$, $J5$	Turned OFF

I_{set} at room temperature (300 ^{o}K) can be simplified to -

$$R_{set} = \frac{68\,\mathrm{mV}}{I_{set}} \tag{C.2}$$

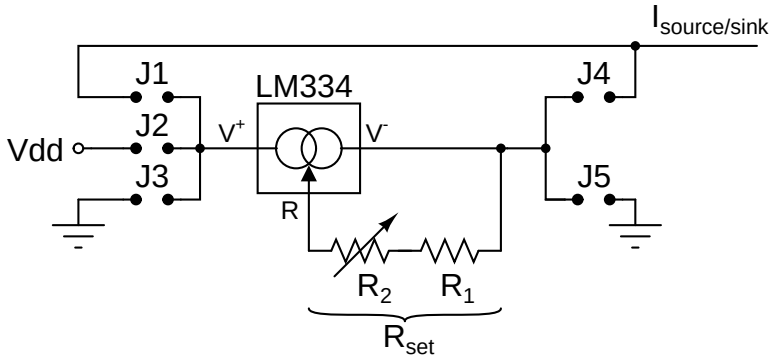


Figure C.2: Schematic of the current source/sink circuit

An adjustable current source/sink is built using the basic current source circuit (Figure C.1) and is shown in Figure C.2. Resistor R_1 decides the maximum current the circuit can source/sink, while $R_1 + R_{2,max}$ decide the minimum source/sink current. The jumper settings shown in Table C decide the source/sink operation of the circuit.

APPENDIX D

PIN DETAILS OF THE ACTIVE-RC FILTER CHIP

Pinout of the packaged active-RC filter chip is shown in Figure D.1. The functionality of each pin is given in Table D.1

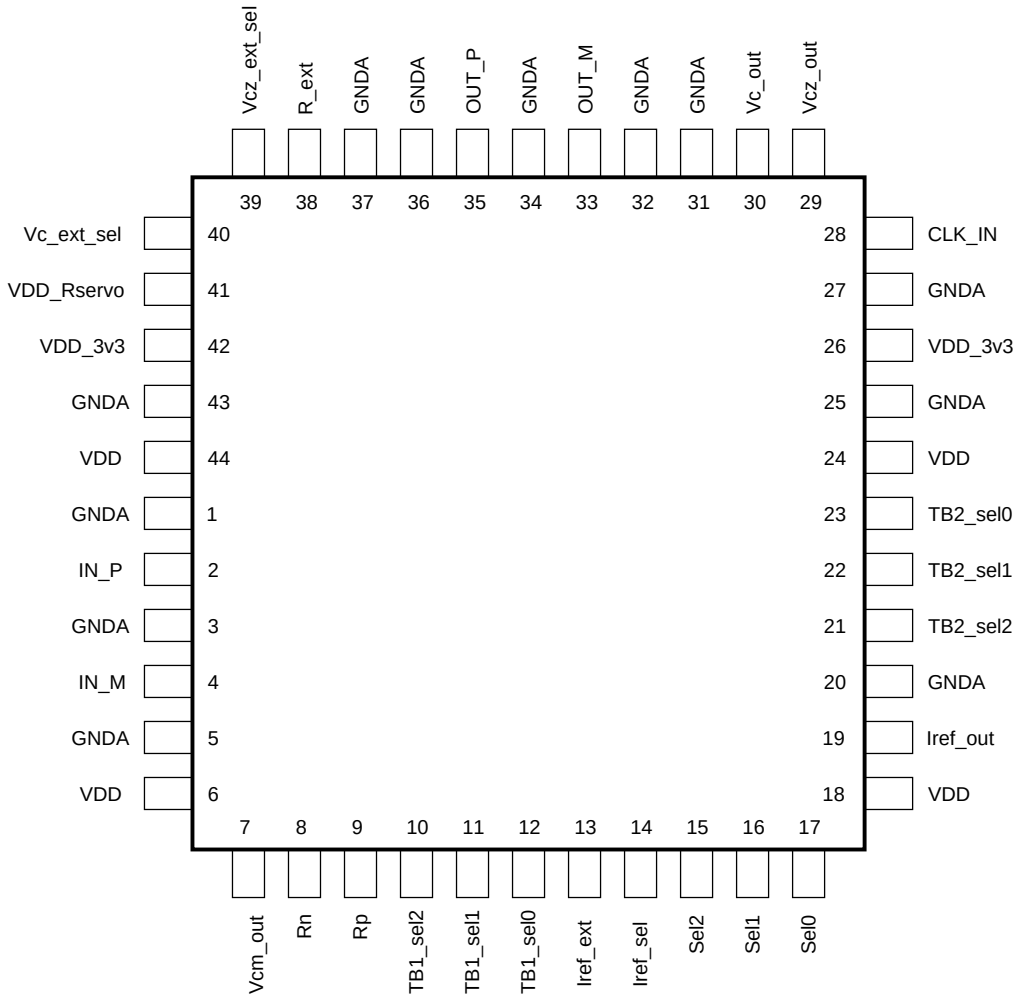


Figure D.1: Pinout of the packaged active-RC chip

Table D.1: Functionality of pins of the active-RC filter chip

Pin number	**Pin Name**	**Functionality**
1, 3, 5, 20, 25, 27, 31, 32, 34, 36, 37 & 43	$GNDA$	Ground
6, 18, 24 & 44	VDD	Supply voltage (3.3 V nominal)
2 4	IN_P IN_M	Differential analog input.
7	VCM_OUT	Common-mode reference output. Used to test/tap the common-mode reference voltage generated on-chip.
8 9	R_n R_p	Stable resistance for the fixed-Gm bias circuit is connected between these two pins.
10 11 12	$TB1\_sel2$ $TB1\_sel1$ $TB1\_sel0$	Control bits for test buffer TB1.
13 14	$Iref\_ext$ $Iref\_sel$	$Iref\_sel$ is the control to select between an internal fixed-Gm bias circuit or an external current $Iref\_ext$.
15–17	$Sel2$, $Sel1$ and $Sel0$	3-bit select lines setting the bandwidth of the filter. $Sel0$ is the LSB.
19	$Iref\_out$	A test pin, where the transconductor bias current is brought out.
21 22 23	$TB2\_sel2$ $TB2\_sel1$ $TB2\_sel0$	Control bits for test buffer TB2.
26 & 42	VDD_3v3	3.3 V supply for the test-buffers.
28	CLK_IN	1 MHz Clock for the resistor servo circuit.
29	Vcz_out	Control voltage of the zero-compensating resistor R_z is tapped out.
30	Vcz_out	Control voltage of the integrating resistor R_i is tapped out.
33 34	OUT_M OUT_P	Differential analog output.
38	R_ext	Offchip resistor (1 kΩ) of the Resistor servo circuit. The other end of the resistor is connected to pin 7.
39	Vcz_ext_sel	Control to select the internal resitor servo circuit or an external voltage at Vcz_out.
40	Vc_ext_sel	Control to select the internal resitor servo circuit or an external voltage at Vc_out.
41	VDD_Rservo	Supply for the Resistor servo loop.

REFERENCES

1. **Alini, R.**, **A. Baschirotto**, and **R. Castello** (1992). Tunable BiCMOS continuous-time filter for high-frequency applications. *IEEE Journal of Solid-State Circuits*, **27**(12), 1905–1915.

2. **Bagheri, M.** and **Y. Tsividis** (1985). A small signal dc-to-high-frequency nonquasistatic model for the four-terminal MOSFET valid in all regions of operation. *IEEE Transactions on Electron Devices*, **32**(11), 2383–2391.

3. **Bakr, M. H.** (2000). *Advances in space mapping optimization of microwave circuits*. Ph.D. thesis, McMaster University.

4. **Bandler, J.**, **R. Biernacki**, **S. H. Chen**, **P. Grobelny**, and **R. Hemmers** (1994). Space mapping technique for electromagnetic optimization. *IEEE Transactions on Microwave Theory and Techniques*, **42**(12), 2536–2544.

5. **Bandler, J.**, **Q. Cheng**, **S. Dakroury**, **A. Mohamed**, **M. Bakr**, **K. Madsen**, and **J. Sondergaard** (2004). Space mapping: the state of the art. *IEEE Transactions on Microwave Theory and Techniques*, **52**(1), 337–361.

6. **Behr, A.**, **M. Schneider**, **S. Filho**, and **C. Montoro** (1992). Harmonic distortion caused by capacitors implemented with MOSFET gates. *IEEE Journal of Solid-State Circuits*, **27**(10).

7. **Bollati, G.**, **S. Marchese**, **M. Demicheli**, and **R. Castello** (2001). An eighth-order CMOS low-pass filter with 30-120 MHz tuning range and programmable boost. *IEEE Journal of Solid-State Circuits*, **36**(7), 1056–1066.

8. **Chamla, D.**, **A. Kaiser**, **A. Cathelin**, and **D. Belot** (2005). A Gm-C low-pass filter for zero-IF mobile applications with a very wide tuning range. *IEEE Journal of Solid-State Circuits*, **40**(7), 1443–1450.

9. **Chen, M.**, **J. Silva-Martinez**, **S. Rokhsaz**, and **M. Robinson** (2003). A 2-V_{pp}, 80–200MHz fourth–order continuous–time linear phase filter with automatic frequency tuning. *IEEE Journal of Solid-State Circuits*, **38**(10), 1745–1749.

10. **De Veirman, G.** and **R. Yamasaki** (1992). Design of a bipolar 10-MHz programmable continuous-time 0.05^o equiripple linear phase filter. *IEEE Journal of Solid-State Circuits*, **27**(3), 324–331.

11. **Gopinathan, V.**, **M. Tarsia**, and **D. Choi** (1999). Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in submicrometer CMOS. *IEEE Journal of Solid-State Circuits*, **34**(12), 1698–1707.

12. **Harrison, J.** and **N. Weste** (2002). 350 MHz opamp-RC filter in 0.18 μm CMOS. *Electronics Letters*, **38**(6), 259–260.

13. **Harrison, J.** and **N. Weste** (2003). A 500 MHz CMOS anti-alias filter using feed-forward op-amps with local common-mode feedback. *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, **1**, 132–483.

14. **Khorramabadi, H.**, **M. Tarsia**, and **N. Woo** (1996). Baseband filters for IS-95 CDMA receiver applications featuring digital automatic frequency tuning. *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, 172–173.

15. **Khoury, J.** (1991). Design of a 15-MHz CMOS continuous-time filter with on-chip tuning. *IEEE Journal of Solid-State Circuits*, **26**(12), 1988–1997.

16. **Khoury, J.** and **Y. Tsividis** (1987). Analysis and compensation of high-frequency effects in integrated MOSFET-C continuous-time filters. *IEEE Transactions on Circuits and Systems*, **34**(8), 862–875.

17. **Larsson, P.** (1997). Parasitic resistance in an MOS transistor used as on-chip decoupling capacitance. *IEEE Journal of Solid-State Circuits*, **32**(4), 574–576.

18. **Moulding, K.** and **G. Wilson** (1978). A fully integrated five-gyrator filter at video frequencies. *IEEE Journal of Solid-State Circuits*, **13**(3), 303–307.

19. **National Semiconductor**, *LM334 datasheet*. URL `http://www.national.com/mpf/LM/LM334.html`.

20. **Nauta, B.** (1992). A CMOS transconductance-C filter technique for very high frequencies. *IEEE Journal of Solid-State Circuits*, **27**(2), 142–153.

21. **Panday, P.**, **J. Silva-Martinez**, and **X. Liu** (2006). A CMOS 140-mW fourth-order continuous-time low-pass filter stabilized with a class AB common-mode feedback operating at 550 MHz. *IEEE Transactions on Circuits and Systems*, **53**(4), 811–820.

22. **Pavan, S.** (1999). *High frequency continuous time filters in digital CMOS process*. Ph.D. thesis, Columbia University.

23. **Pavan, S.** (2004*a*). A fixed-transconductance bias technique for CMOS analog circuits. *Proc. IEEE International Symposium on Circuits and Systems, Vancouver*, 661–664.

24. **Pavan, S.**, *Lecture notes on active filter design – EE534*. Indian Institute of Technology Madras, 2004*b*.

25. **Pavan, S.**, **M. Tarsia**, **S. Kudszus**, and **D. Pritzkau** (2005). Design considerations for integrated modulator drivers in silicon germanium technology. *International Journal of High Speed Electronics and Systems*, **15**(3), 477–495.

26. **Pavan, S.** and **Y. Tsividis** (2000). Time-scaled electrical networks - Properties and applications in the design of programmable analog filters. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **47**(2), 161–165.

27. **Pavan, S.**, **Y. Tsividis**, and **K. Nagaraj** (2000). Widely programmable high-frequency continuous-time filters in digital CMOS technology. *IEEE Journal of Solid-State Circuits*, **35**(4), 503–511.

28. **Pu, L.-J.** and **Y. Tsividis** (1990). Transistor-only frequency-selective circuits. *IEEE Journal of Solid-State Circuits*, **25**(3), 821–832.

29. **Pucel, R. A.**, **W. Struble**, **R. Hallgren**, and **U. L. Rohde** (1992). A general noise de-embedding procedure for packaged two-port linear active devices. *IEEE Transactions on Microwave Theory and Techniques*, **40**(11), 2013–2024.

30. **Razavi, B.**, **R. Yan**, and **K. Lee** (1994). Impact of distributed gate resistance on the performance of MOS devices. *IEEE Transactions on circuits and Systems - I, Fundamental Theory and Applications*, **41**(11), 750–754.

31. **Rizzoli, V.** and **A. Lipparini** (1985). Computer-aided noise analysis of linear multiport networks of arbitrary topology. *IEEE Transactions on Microwave Theory and Techniques*, **33**(12), 1507–1512.

32. **Schaumann, R.** and **M. Tan** (1989). The problem of on-chip automatic tuning in continuous-time integrated filters. *Proc. IEEE International Symposium on Circuits and Systems*, 106–109.

33. **Scholten, A.**, **L. Tiemeijer**, **P. De Vreede**, and **D. Klaassen** (1999). A large signal non-quasi-static MOS model for RF circuit simulation. *International Electron Devices Meeting: Technical Digest.*, 163–166.

34. **Sewter, J.** and **A. Carusone** (2006). A CMOS finite impulse response filter with a crossover traveling wave topology for equalization up to 30Gb/s. *IEEE Journal of Solid-State Circuits*, **41**(4), 909–917.

35. **Shi, B.**, **J. Khoury**, and **Y. Tsividis** (1986). High frequency effects in MOSFET-C Tow-Thomas biquads. *IEEE Transactions on Circuits and Systems*, **33**(6), 648–651.

36. **Steininger, J.** (1990). Understanding wide-band MOS transistors. *IEEE Circuits and Devices Magazine*, **6**(3), 21–26.

37. **Stevenson, J.-M.** and **E. Sanchez-Sinencio** (1998). An accurate quality factor tuning scheme for IF and high-Q continuous-time filters. *IEEE Journal of Solid-State Circuits*, **33**(12), 1970–1978.

38. **Tsividis, Y.** (1994). Integrated continuous-time filter design - an overview. *IEEE Journal of Solid-State Circuits*, **29**(3), 166–176.

39. **Tsividis, Y.**, *Operation and modeling of the MOS transistor*. McGraw Hill, 1999.

40. **Tsividis, Y.** and **B. Shi** (1985). Cancellation of distortion of any order in integrated active RC filters. *Electronics Letters*, **21**, 132.

41. **Voorman, J.**, **W. Bruls**, and **P. Barth** (1982). Integration of analog filters in a bipolar process. *IEEE Journal of Solid-State Circuits*, **17**(4), 713–722.

42. **Zele, R.** and **D. Allstot** (1996). Low power CMOS continuous time filters. *IEEE Journal of Solid-State Circuits*, **31**(2), 157–168.

LIST OF PAPERS BASED ON THESIS

INTERNATIONAL JOURNALS

1. **T. Laxminidhi and S. Pavan**. Efficient design centering of high-frequency integrated continuous-time filters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(7), July 2007, 1481–1488.

2. **S. Pavan and T. Laxminidhi**. Accurate characterization of integrated continuous-time filters. *IEEE Journal of Solid-State Circuits*, 42(8), August 2007, 1758–1766.

INTERNATIONAL CONFERENCES

1. **S. Pavan and T. Laxminidhi**. A technique for accurate frequency response measurement of integrated continuous-time filters. *Proceedings of the IEEE Custom Integrated Circuits Conference 2006*, September 2006, 77–80.

2. **S. Pavan and T. Laxminidhi**. A 70-500 MHz programmable CMOS filter compensated for MOS nonquasistatic effects. *Proceedings of the 32nd European Solid-State Circuits Conference 2006*, September 2006, 328–331.

3. **T. Laxminidhi and S. Pavan**. Design centering high frequency integrated continuous-time filters. *Proceedings of the IEEE International Symposium on Circuits and Systems 2007*, May 2006, 1939–1942.

4. **T. Laxminidhi, V. Prasadu and S. Pavan**. A low power 44-300 MHz programmable active-RC filter in 0.18 μm CMOS. *Proceedings of the IEEE Custom Integrated Circuits Conference 2007*, September 2007, 683–686.

CURRICULUM VITAE

1. **NAME** : Laxminidhi T.

2. **DATE OF BIRTH** : 3^{rd} May 1975.

3. **EDUCATIONAL QUALIFICATIONS**

1996 Bachelor of Engineering (B.E.)

Institution	:	Nitte Mahalinga Adyanthaya Memorial Institute of Technology, Nitte.
University	:	Mangalore University.
Specialization	:	Electrical and Electronics Engineering.

1998 Master of Technology (M.Tech.)

Institution	:	National Institute of Technology Karnataka, Surathkal (Formerly – Karnataka Regional Engineering College).
University	:	Mangalore University.
Specialization	:	Industrial Electronics.

Doctor of Philosophy (Ph.D.)

Institution	:	Indian Institute of Technology, Madras.
Registration date	:	03-08-2004.

DOCTORAL COMMITTEE

CHAIRPERSON:	Head of the Department, Department of Electrical Engineering.
GUIDE:	Dr. Y. Shanthi Pavan, Asst. Professor, Department of Electrical Engineering.
MEMBERS:	Dr. Vinita Vasudevan, Professor, Department of Electrical Engineering.
	Dr. Anil Prabhakar Asst. Professor, Department of Electrical Engineering.
	Dr. T. S. Natarajan, Professor, Department of Physics.
	Dr. Manu Santhanam, Asst. Professor, Department of Civil Engineering.