Design of a 15 MHz Bandwidth Single Bit Continuous Time $\Delta\Sigma$ Modulator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a 15 MHz Single Bit Continuous Time $\Delta\Sigma$ Modulator** , submitted by **Muthusubramanian.N.V**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally, I would like to dedicate this thesis to my parents who have been a true moral support all through my student life.

Abbreviations

DSM	$\Delta\Sigma$ Modulator
CTDSM	Continuous Time $\Delta\Sigma$ Modulator
OBG	Out of Band Gain
OSR	Over-Sampling Ratio
SNR	Signal to Noise Ratio
MSA	Maximum Stable Amplitude
DT	Discrete Time
CT	Continuous Time
SQNR	Signal to Quantisation Noise Ratio
FFT	Fast Fourier Transform
DAC	Digital to Analog Converter
STF	Signal Transfer Function
NTF	Noise Transfer Function
NRZ	Non-Return to Zero
FS	Full-Scale
V_{ppd}	Volts, Peak to Peak Differential
ADC	Analog to Digital Converter
PSD	Power Spectral Density

ABSTRACT

This project involves the design of a single-bit continuous time $\Delta\Sigma$ modulator to achieve a resolution of 11 bits for a 15 MHz input bandwidth. The modulator has been designed in 130 nm UMC CMOS technology with a supply voltage of 1.2 V. It is operated at a sampling frequency of 960 MHz. The modulator consumes a total power of 2.2mW, and occupies an active area of 850 μm X 450 μm. The output driver consists of a deserializer which outputs data at half the clock rate.

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CHAPTER 1

Introduction to $\Delta\Sigma$ Modulation

This chapter provides a brief overview of the concepts involved in $\Delta\Sigma$ modulators. We also discuss the choice of architecture for the building blocks of the modulator design presented in this thesis.

$\Delta\Sigma$ modulators are a class of oversampled data converters which employ the technique of feedback to achieve high resolution [1]. The basic architecture of a $\Delta\Sigma$ Modulator is shown in Fig 1.1.

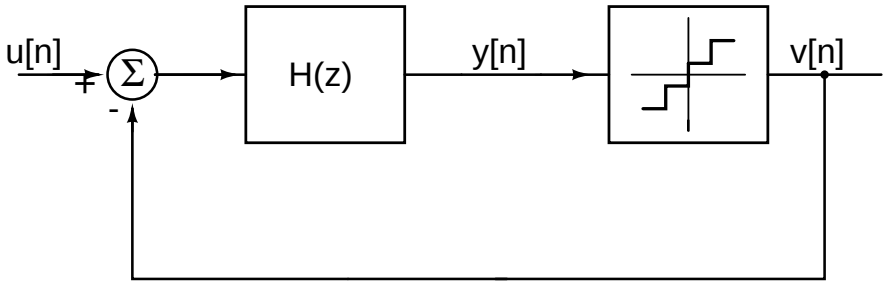


Figure 1.1: Block diagram of a $\Delta\Sigma$ Modulator

The modulator consists of the loop-filter $H(z)$ which is designed to have a very high gain at low frequencies and a low gain at high frequencies. Hence, at the input of the loop-filter, the signal consists mainly of high frequency components. Thus, if the input $u[n]$ is restricted to a low frequency, the output $v[n]$ will be a faithful reproduction of the input signal $u[n]$ alongwith quantization noise at higher frequencies. In other words, we can say that the quantization noise has been shaped outside the input frequency band. At the output of the modulator, a decimator should be used to remove the high frequency quantization noise.

$\Delta\Sigma$ modulators are inherently non-linear due to the quantizer block. A linear approximation of the modulator enables us to analyse the modulator. Fig 1.2 shows a linearized model of a $\Delta\Sigma$ modulator.

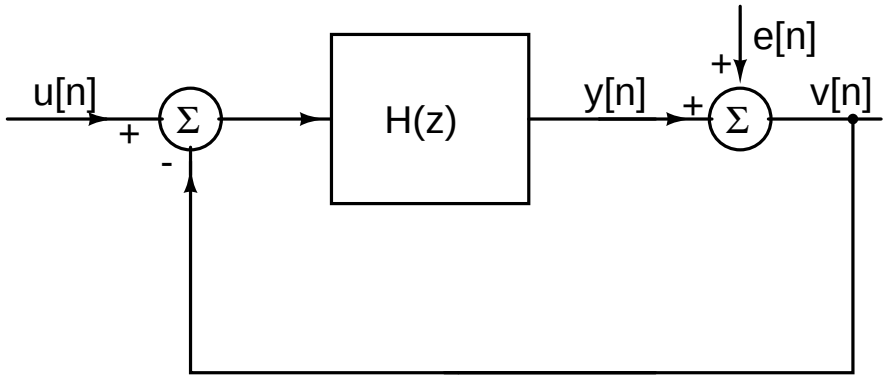


Figure 1.2: Linear model of a $\Delta\Sigma$ Modulator

In the linear model, the quantizer is replaced by an adder consisting of 2 **independent** inputs, $e[n]$ which represents the quantization noise and $y[n]$.

From the linear model, we can see that the output $V[z]$ as:

$$V(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{1.1}$$

$$= STF(z)U(z) + NTF(z)E(z) \tag{1.2}$$

Here, STF(z) and NTF(z) represent the Signal Transfer function and the Noise Transfer Function. If H(z) has a large magnitude in the frequency band of interest, STF(z) will be almost unity, while NTF(z) will be very small. Thus, the quantization noise can be reduced in the band of interest.

As an example, if $H(z) = 1/(z-1)$, then from (1.1), we get

$$STF(z) = z^{-1} \tag{1.3}$$

$$NTF(z) = 1 - z^{-1} \tag{1.4}$$

From (1.3) we see that STF(z) is just a delay while NTF(z) has a high pass response. If we want to achieve a very high in-band *Signal to quantization Noise*

Ratio (SQNR), we must choose a sampling rate f_s much higher than the Nyquist rate so that the total quantization noise within the frequency of band is reduced. Hence, $\Delta\Sigma$ Modulators are a class of oversampled data converters. If f_b is the input frequency bandwidth, then the *Oversampling Ratio*(OSR) is defined as

$$OSR = \frac{f_s}{2f_b} \tag{1.5}$$

1.1 Architectural Details

1.1.1 Continuous-Time vs Discrete-Time

Switched-capacitor (SC) circuits form the building blocks of Discrete-time (DT) $\Delta\Sigma$ Modulators. SC filters used to be the choice of design for $\Delta\Sigma$ Modulators as they provide high accuracy and linearity. SC filters are unattractive for use in very high speed designs as the settling time and power requirements of opamps used in SC filters pose a serious limitation. Moreover, the need for an anti-aliasing filter before converting the continuous-time input to a discrete-time input has led to an increase in the usage of Continuous-time(CT) modulators.

The block diagram of a Continous-time $\Delta\Sigma$ Modulator (CTDSM) is shown in Fig 1.3.

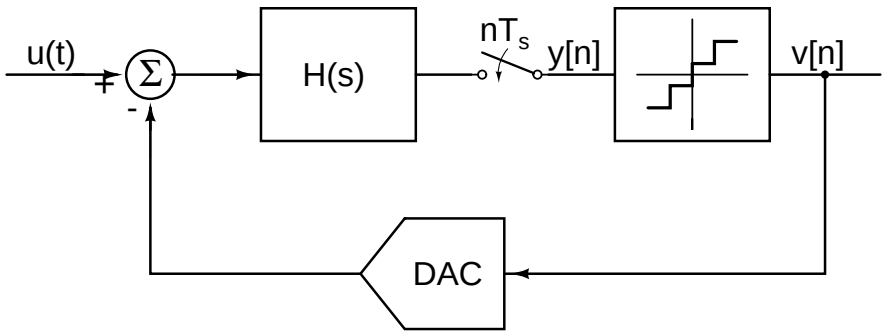


Figure 1.3: Block diagram of a Continuous-Time $\Delta\Sigma$ Modulator

A CT modulator is derived from its DT counterpart by pushing the sampler

from outside the loop to within the loop. A DAC is used in the feedback path to convert the digital output $v[n]$ to an analog signal, which feeds to the input of the loop-filter . CT modulators obviate the need for anti-aliasing filters because the loop-filter does inherent anti-aliasing [1]. The maximum frequency of operation in CT modulators are limited by the delay in the quantizers and the feedback DAC while DT modulators are limited by the settling time of the opamps. In general, CT modulators can be operated at a higher frequency than a DT modulator in a given technology [1].

1.1.2 Quantizer Resolution: Single-Bit vs Multi-Bit

Today, in most applications, multi-bit quantizers are the choice of design due to the following de-merits of single-bit modulators.

1. Single-bit modulators with *Out of Band Gain* (OBG) greater than 1.5 can cause instability [1]. Hence, only a moderate NTF can be chosen which results in a low SNR.

2. Since the input of the loop-filter experiences a large change from sample to sample in a single-bit modulator, opamp slew poses a big challenge. It results in an increase in in-band noise floor. Hence, a very large power needs to be dissipated in the opamp to overcome the problem of slewing. This problem makes a multi-bit modulator more attractive as it results in lesser power consumption.

3. Since the quantization noise is very high in a single-bit modulator, the *Maximum stable amplitude* (MSA) of a single-bit modulator is smaller than that of a corresponding multi-bit modulator for a fixed full-scale and the same NTF.

4. Multi-bit modulators provide lower jitter sensitivity because the Least Significant Bit (LSB) size is lower.

However, single-bit quantizers have the advantage that they have very low complexity because the latch and the feedback DAC have only one bit. Hence, the issue of matching in the comparators of the latch and the feedback DAC do not arise. Nonidealities, such as *Integral Non-Linearity* (INL) and *Differential Non-linearity* (DNL) in the feedback DAC are directly referred at the input and this degrades the performance of Multi-bit modulators significantly. To overcome the problem of non-idealities, typically methods such as *Dynamic Element Matching* (DEM) [2] are used. But these techniques further increase the power requirements of the modulator. These problems of multi-bit make single-bit modulators an attractive choice in certain applications.

1.1.3 Order of Loop-filter and Oversampling Ratio

The order of the loop-filter is the highest power of z in the NTF. The simplest m^{th} order loop-filter is a cascade of m integrators. The noise-transfer function of the m-th order modulator is:

$$NTF(z) = (1 - z^{-1})^m \tag{1.6}$$

For an m^{th} order modulator with an oversampling ratio of OSR, Δ as the Least Significant Bit (LSB) of the quantizer, it can be shown that the in-band quantization noise power is [2]:

$$P_e = \frac{\Delta^2}{12} \frac{\pi^{2m}}{2m+1} \left(\frac{1}{OSR} \right)^{2m+1} \tag{1.7}$$

From Equation 1.7, we see that increasing both the order of the modulator and the OSR decreases the quantization noise power. The maximum OSR that one chooses is limited by the technology. Increasing the order of the modulator results in the reduction of the MSA. Hence, to achieve a desired SNR, we need to tradeoff the order of the modulator with the OSR. Zeros of the NTF can be

optimised to achieve a better SNR for a given order of the modulator as per the method mentioned in [1].

1.2 Design Specifications

The aim of this project is to design a $\Delta\Sigma$ Modulator having 11 bit resolution (SNR - 66 dB) in a 15 MHz bandwidth . A single-bit quantizer is chosen for simplicity of design. The problem of opamp slewing is overcome by a method called the *Assisted Opamp Technique* as described in Chapter 2 [3]. A fourth order modulator with optimization of zeros is chosen and the OSR used is 32. This means that the sampling rate is 960 MHz. The feedback DAC is chosen to be a current-steering DAC because of the high sampling rate. The pulse shape of the DAC is chosen to be *Non-Return to Zero* (NRZ). The modulator is designed in UMC 130 nm technology with a 1.2 V supply. The full scale (FS) of the quantizer is assumed to be $2.4\,V_{pp,d}$.

Table 1.1 summarises the specifications of the design of the modulator.

Table 1.1: Design Specifications

Input Bandwidth	15 MHz
Resolution	11
SNR	66 dB
Sampling Rate	960 MHz
Supply Voltage	1.2 V
FS of quantizer	$2.4\,V_{pp,d}$
Technology	130 nm CMOS

CHAPTER 2

Loop Filter Design

In the previous chapter, we have seen that a fourth order modulator with optimized zeros and an OSR of 32 is used for the current design. Thus, the NTF that is to be realized is derived from the $\Delta\Sigma$ *Toolbox* in MATLAB and is given by

$$NTF(z) = \frac{(z^2 - 1.999z + 1)(z^2 - 1.993z + 1)}{(z^2 - 1.49z + 0.563)(z^2 - 1.7z + 0.7861)} \tag{2.1}$$

From the NTF, the loop filter response H(z) can be determined by

$$H(z) = \frac{1 - NTF(z)}{NTF(z)} \tag{2.2}$$

$$= \frac{0.8013(z - 0.8325)(z^2 - 1.789z + 0.8355)}{(z^2 - 1.999z + 1)(z^2 - 1.993z + 1)} \tag{2.3}$$

The modulator with the NTF given in (2.10) was simulated in MATLAB. The Power Spectral Density (PSD) of the output is shown in Fig. 2.1. The peak SNR obtained is 77 dB. To determine the Maximum Stable Amplitude (MSA) a slow ramp was given at the input and the power at the output of the loop filter (or the input of the quantizer) was measured. Fig. 2.2 shows the plot of quantizer input versus input amplitude. From Fig. 2.2 , we see that the MSA is 0.66 FS or 1.6 $V_{pp,d}$.

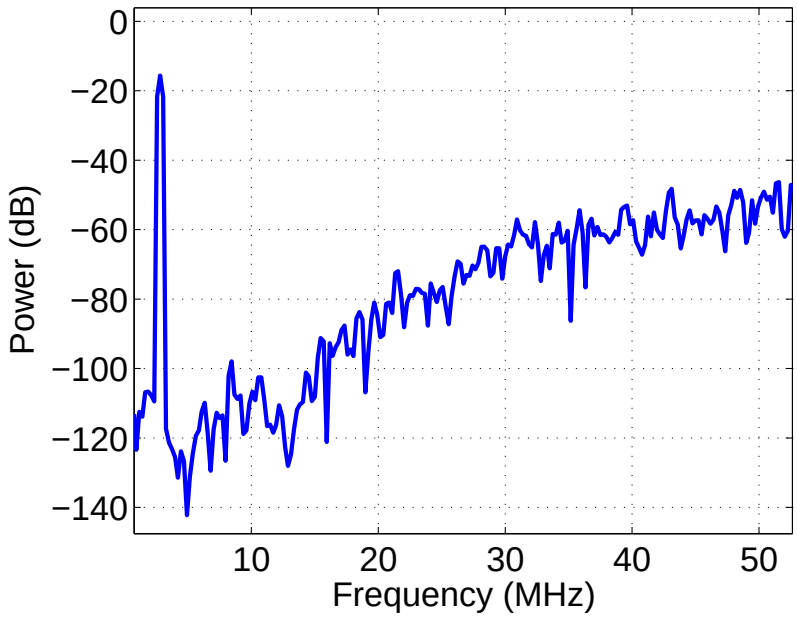


Figure 2.1: PSD of ideal modulator

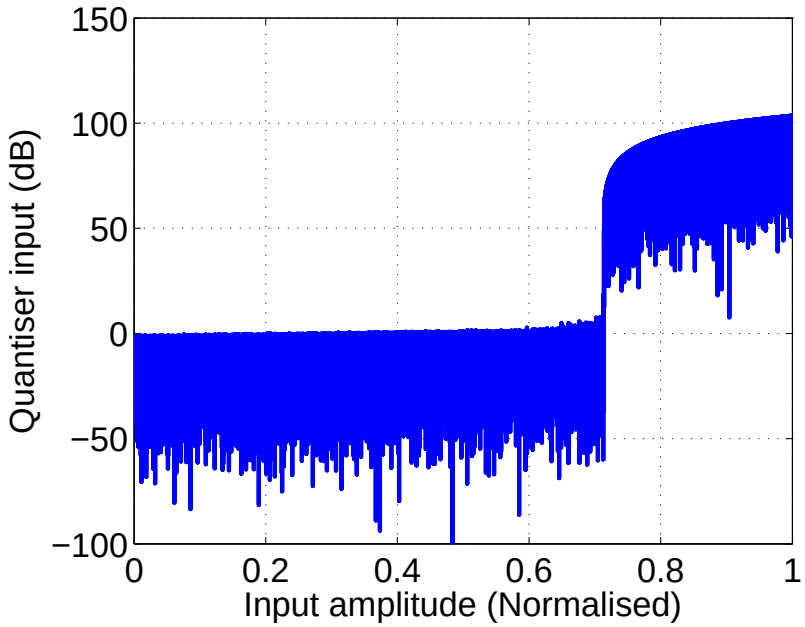


Figure 2.2: MSA estimation

2.1 Continuous-Time Loopfilter realization

If we want to realize the above discrete-time loop filter response in a CT modulator with an NRZ DAC, the sampled value of the pulse response of the CT loop filter should be the same as the impulse response of the DT loop filter. Fig. 2.3 shows the DT and the CT implementations of the loop filter.

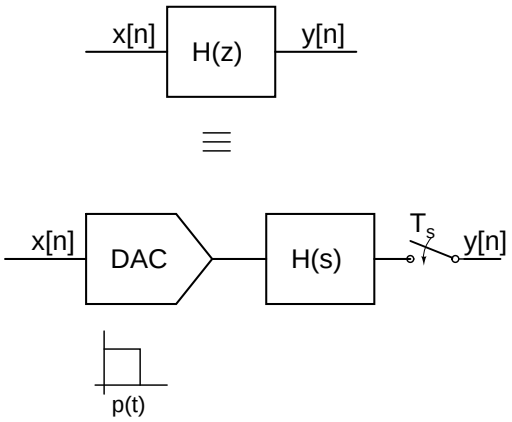


Figure 2.3: Equivalence of CT and DT loop-filters

The two systems shown in Fig. 2.3 are identical if

$$Z^{-1}\{H(z)\} = L^{-1}\{P(s)H(s)\}|_{t=nT_s} \tag{2.4}$$

where P(s) represents the pulse response of the DAC. This transformation of the DT response to the CT response is called as the impulse invariance transform [4]. Thus, for a CT modulator with NRZ DAC, one can write the CT loop filter response from MATLAB as

$$H(s) = \frac{0.6709(s + 0.1829)(s^2 + 0.1802s + 0.05095)}{(s^2 + 0.001114)(s^2 + 0.007147)} \tag{2.5}$$

This forms the prototype CT loopfilter for our design. A fourth order CT loop-filter in CIFF architecture can be realized using a cascade of four integrators. The optimisation zeros of the NTF are realized using the feedback factors β_1 and β_2. Fig. 2.4 shows the block diagram implementation of the prototype filter.

The integrators in the above loop-filter are realized using opamp-RC structures. From the prototype filter, the actual implementation of the loop-filter is realized after frequency scaling, node scaling and excess loop delay compenstaion.

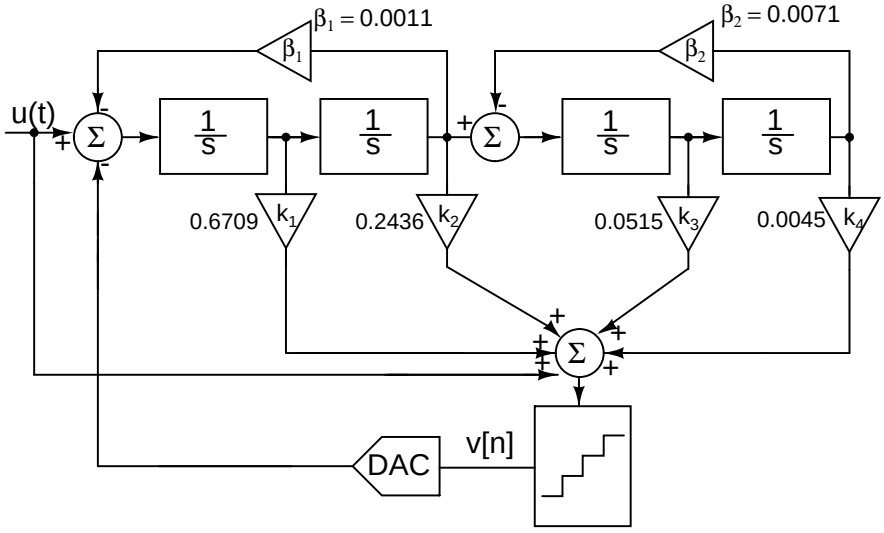


Figure 2.4: Prototype Loop Filter

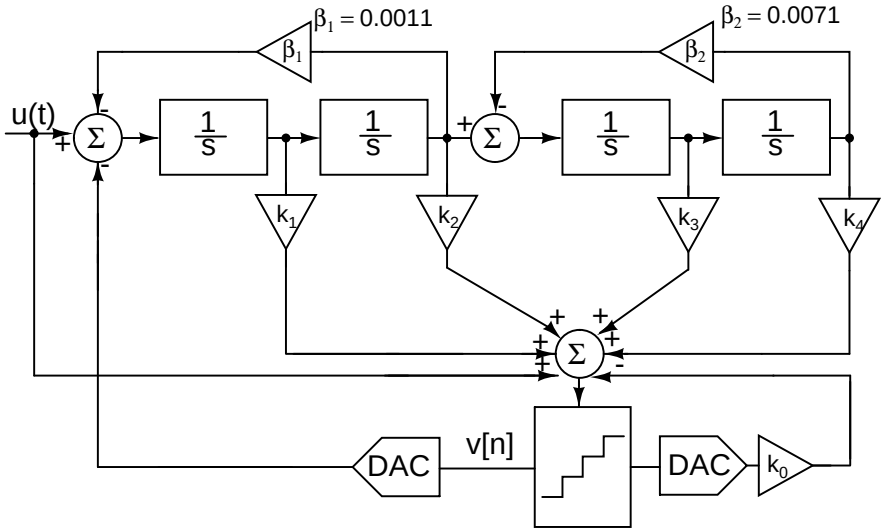


Figure 2.5: Loop Filter with Excess Loop delay compensation

The prototype loop filter response in (2.5) corresponds to the DT response of (2.2) if the sampling rate is assumed to be 1 Hz. In our design, we use a sampling frequency f_s of 960 MHz. So, we have to frequency scale our prototype loopfilter such that the impulse invariance transformation is valid at the sampling frequency

f_s. This can be done by replacing s by s/f_s in (2.5). In other words, $H(s/f_s)$ gives the loop filter response to be operated at a sampling rate of f_s

Nodes are scaled such that that all nodes have a peak-to-peak differential swing approximately $800\,\mathrm{mV_{pp,d}}$. Node scaling ensures that the output of the opamps do not saturate due to high swing.

Excess loop delay is an important problem in CT $\Delta\Sigma$ Modulators. The excess loop delay arises because of the non-idealities in the integrators and the summer used in the loop filter, delay in the regeneration time of the quantizer and the delay in the feedback DAC. This is particularly problematic in the case of high-speed circuits. If the excess loop delay is not compensated for, the modulator may become unstable. Typically, excess loop delay is compensated by adding an additional direct path from the output of the quantizer to the summer as shown in Fig. 2.5.

2.2 Circuit implementation of Loop-filter

Fig. 2.6 shows the single ended circuit diagram of the loop filter used in the current design. In the differential implementation, the gain stage of -1 can be eliminated by swapping the wires. The values of the resistors and capacitors shown in the circuit correspond to the one used in the final design after frequency scaling, node scaling and excess loop delay compensation.

2.2.1 Choice of Resistors and Capacitors

The most critical resistor in terms of the design of the loop filter is the first integrating resistor R_1. The thermal noise contributed by R_1 is directly referred to the input and should be chosen carefully. Since, we are targeting an SNR of 66 dB, we choose R_1 such that the total input referred thermal noise is 70 dB below the signal level or $178\,\mu\mathrm{V_{rms}}$ for an input signal at MSA. The main contributors

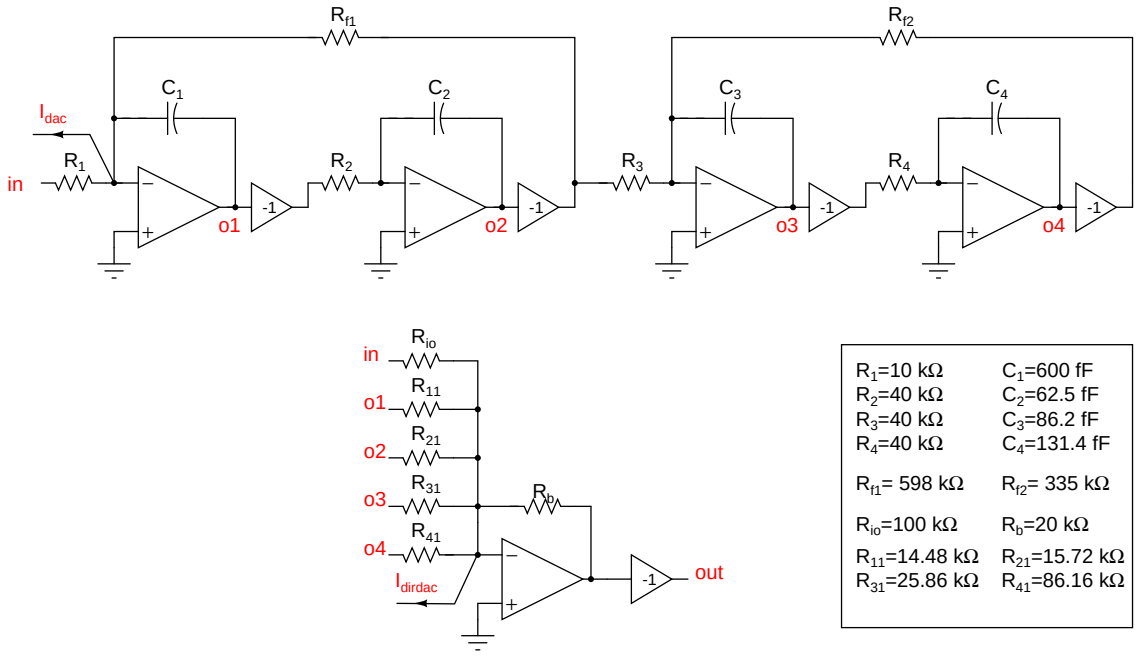


Figure 2.6: Circuit Diagram of Loop Filter

to the input referred noise are the resistor R_1, the feedback DAC and the first integrating opamp. With these factors in mind, R_1 is chosen to be 10 kΩ. The noise contributed by the input resistors alone thus will be $8kTRf_b = 70.4\mu V_{rms}$. The noise due to the other integrating resistors and the feedback resistors are scaled down by the gain of the first integrator and hence, do not contribute to the input referred noise significantly. Hence, R_2, R_3, R_4 are chosen to be 40 kΩ. Further increasing the value of the resistors decrease the integrating capacitors to very small values and would be difficult to realize accurately.

Ideally, one would choose capacitors such that

$$\frac{1}{R_1C_1} = \frac{1}{R_2C_2} = \frac{1}{R_3C_3} = \frac{1}{R_4C_4} = f_s \tag{2.6}$$

which will result only in frequency scaling. To ensure node scaling, the capacitors are scaled down or up so that the swing is maintained approximately at $800\,mV_{pp,d}$. After node scaling, the values of the capacitors chosen are

$$C_1 = 600\,\text{fF} \quad C_2 = 62.5\,\text{fF} \quad C_3 = 86.2\,\text{fF} \quad C_4 = 131.4\,\text{fF}$$

Having chosen the integrating capacitors, the notch resistors are chosen such that

$$\frac{1}{R_{f1}C_1R_2C_2} = \beta_1 f_s^2 \tag{2.7}$$

$$\frac{1}{R_{f2}C_3R_4C_4} = \beta_2 f_s^2 \tag{2.8}$$

This gives $R_{f1} = 598\,\text{k}\Omega$ and $R_{f2} = 335\,\text{k}\Omega$.

Realizing Coefficients

The coefficients are realized by adding the outputs of the integrators using a summer opamp. Ideally, the absolute values of the feedback resistor R_f and the coefficient realising resistors R_{11}, R_{21}, R_{31}, R_{41} used in the summer opamp are not of significance but the resistors should be chosen such the ratios should realize the appropriate coefficients. But, in reality, the input parasitics of the summer opamp introduces an additional pole at the input which deteriorates the phase margin of the opamp. The larger the R_f used, the lower the pole and lower the phase margin. If the phase margin is very low, it will result in a lot of ringing in the pulse response of the opamp.

The full scale of the modulator is $2.4\,\text{V}_{\text{pp,d}}$. This means that the summer opamp must support the entire supply range, which is difficult to implement in practice. Since the quantizer is single-bit, only the sign of the output of the opamp is relevant but not its magnitude subject to the constraint that the quantizer doesn't become metastable. So, we can reduce the feedback resistor by a factor of 4 to ensure that the total output swing of the opamp is within $600\,\text{mV}_{\text{pp,d}}$. Thus, in practice, we will be implementing all coefficients scaled down by a factor of 4. If we scale the

output down by a larger value, the swing at the output of the summer will be so low that it can lead to metastability of the quantizer. With these in mind, the feedback resistor R_f is chosen to be $20\,\mathrm{k}\Omega$.

To compensate for excess loop delay, we have an additional current steering DAC which implements the coefficient k_0. The total excess loop delay after implementation of the quantizers and the DAC turns out to be 550ps. The determination of the coefficients of the loop filter is done by the method of *NTF Fitting* which is discussed in the following section. Using this method, the realized resistor values are

$$R_{11} = 14.48\,\mathrm{k}\Omega, R_{21} = 15.72\,\mathrm{k}\Omega, R_{31} = 25.86\,\mathrm{k}\Omega, R_{41} = 86.16\,\mathrm{k}\Omega$$

A direct path resistor R_{io} is also added to the summer from the input. The resistance R_{io} is chosen such that the output of the fourth integrator consists of only quantization noise while all the input component is supplied through the resistor R_{io}. This also ensures that the 4th integrating capacitor doesn't assume a very large value because a very small coefficient is implemented at its output. Thus, R_{io} is chosen to be $100\,\mathrm{k}\Omega$.

2.3 NTF Fitting

The coefficients of the loopfilter implemented using real opamps deviate significantly from the coefficients for an ideal loop filter. These coefficients vary because of excess loop delay, non-idealities in the integrators realized using opamps and the delay in the summer opamp. The non-idealities in the integrators arise due to finite DC gain of the opamp and high-frequency poles which introduce additional delays in the loop filter. Hence, we need to re-determine the coefficients of the loop filter such that the NTF remains the same as what we desire to implement.

In [5], the real opamps are modeled using a state-space representation. Us-

ing the state space description of the opamps, the loop-filter transfer function is determined. Then, a *fminsearch* function in MATLAB is used to determine the coefficients. This method, though reliable, is time consuming and cumbersome. The following section discusses a couple of alternative methods used to fit the NTF.

2.3.1 Open-loop fitting

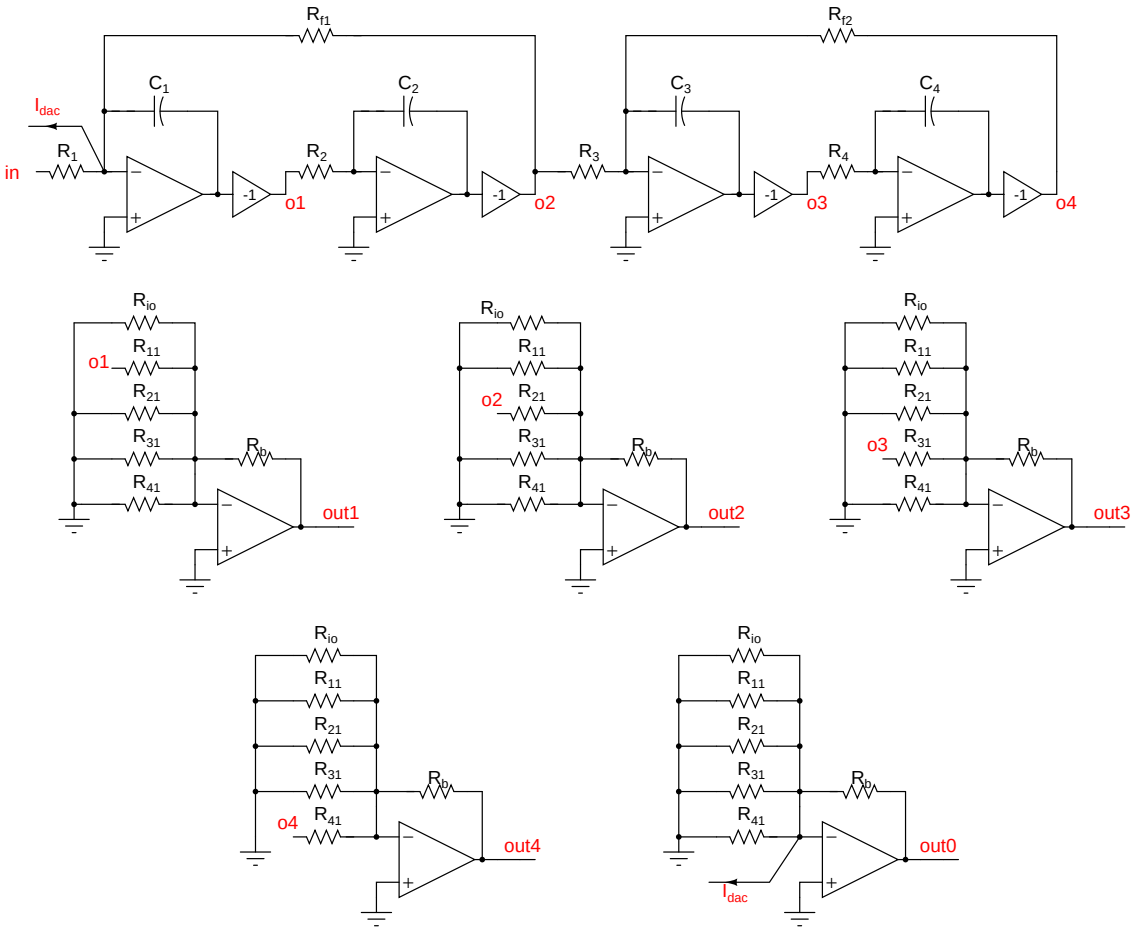
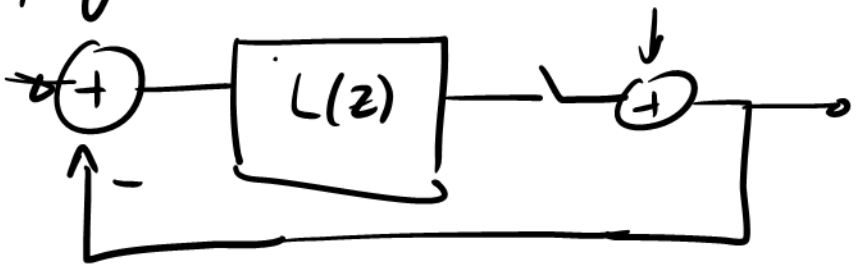


Figure 2.7: Test Bench for Coefficient Determination

We know that the output of the loopfilter is a linear combination of the integrator outputs $o1, o2, o3, o4$ as shown in Fig. 2.6. We also know the ideal loopfilter response h_{loop} that we want to implement. Fig. 2.7 shows the test bench used for determining the coefficients of the loop filter. Each output of the integrator is

In keeping with standard convention,



$$NTF(z) = \frac{1}{1 + L(z)}$$

Denote $\mathcal{Z}^{-1}[NTF(z)] = h[n]$

$(h[0] = 1)$

$$NTF(z) \cdot (1 + L(z)) = 1$$

Let the sampled output pulse responses be denoted as $l_0[n], l_1[n], \cdots, l_4[n]$

Then $L(z) = k_0 L_0(z) + \cdots + k_4 L_4(z)$

$$\Rightarrow \quad h[n] + \sum_i k_i \{ l_i[n] * h[n] \} = \delta[n]$$

$$\Rightarrow \quad \sum_i k_i \underbrace{\{ l_i[n] * h[n] \}}_{\text{Denote as } x_i[n]} = \delta[n] - h[n]$$

$$\Rightarrow \quad \begin{bmatrix} x_0 & x_1 & x_2 & x_3 & x_4 \end{bmatrix} \begin{bmatrix} k_1 \\ k_2 \\ \vdots \\ k_4 \end{bmatrix} = \begin{bmatrix} 0 \\ h_1 \\ h_2 \\ \vdots \\ h_{N-1} \end{bmatrix}$$

In the above equation

x_0 x_1 ... etc. have been truncated beyond (N-1) samples.

Now, use least squares to determine

$$\begin{bmatrix} k_0 \\ \vdots \\ k_q \end{bmatrix}$$

Questions :-

1) Since your equations are all wrong, how do you get the right coefficients?

2) The first columns of Tab. 2.1 & 2.2 seem pretty much the same, so you should get the same NTF by both methods. So the sentence I have underlined in the next page is not correct?

Can you please comment on the questions above.

passed through the summer opamp to account for the delay in the summer opamp as well. Hence, we can write

$$\begin{bmatrix} \mathbf{out0} & \mathbf{out1} & \mathbf{out2} & \mathbf{out3} & \mathbf{out4} \end{bmatrix} \begin{bmatrix} k_0 \\ k_1 \\ k_2 \\ k_3 \\ k_4 \end{bmatrix} = \mathbf{h_{loop}} \tag{2.9}$$

where $out0, out1, out2, out3, out4$ are the integrator outputs passed through the summer opamp as shown in Fig. 2.7. Thus, by taking sufficient set of samples of the integrator outputs, we can determine the coefficient by a least square fit. Initially, the values of $R_{11}, R_{21}, R_{31}, R_{41}$ can be randomly chosen. After one iteration of finding the coefficients, the resistors are appropriately changed and the procedure is continued until the coefficients obtained do not change anymore.

The drawback in this approach is that the coefficients determined vary significantly with the number of points chosen to fit the coefficients. Table. 2.1 shows the coefficients determined for different number of samples used. We see that the coefficients k_0, k_1 and k_2, which affect the out-of-band performance vary significantly with the number of samples used for fitting. Hence, it is difficult to determine the exact value of the coefficients to be used. For any set of coefficients used, we see a significant peaking of 8 dB in the NTF frequency response as shown in Fig. 2.8. Peaking in the NTF response results in more sensitivity to the values of the components and can tend to instability of the modulator. Hence, we use the method of closed-loop fitting to overcome the problem of peaking.

See my question (2) in the previous page.

2.3.2 Closed-loop fitting

In this method, instead of trying to fit the integrator outputs to the open loop transfer function, we try to fit it to the closed-loop NTF response. We know that,

Table 2.1: Coefficients for different number of samples using closed-loop fitting

Coefficients	Number of samples						
	20	30	40	50	60	70	80
k_0	0.7411	0.7400	0.7412	0.7504	0.7759	0.8169	0.8533
k_1	1.1644	1.1702	1.1642	1.1154	0.9837	0.7748	0.5916
k_2	0.4429	0.4385	0.4412	0.4584	0.4939	0.5371	0.5662
k_3	0.0854	0.0865	0.0861	0.0838	0.0806	0.0779	0.0768
k_4	0.0038	0.0037	0.0037	0.0037	0.0037	0.0035	0.0034

$$H(z) = \frac{1}{1 + NTF(z)}$$
$$\Rightarrow H(z)(1 + NTF(z)) = 1 \tag{2.10}$$

Although NTF(z) is an IIR response, one can truncate it because it dies down after a certain number of samples. Suppose we truncate the NTF response to N samples, we can write

$$NTF(z) = \sum_{i=0}^{N-1} b_i z^{-i} \tag{2.11}$$

where b_i are the samples of the NTF. And, we can write H(z) in terms of the integrator responses as

$$H(z) = \sum_{i=0}^{N} h_{loop} z^{-i} \tag{2.12}$$

where h_{loop} is got from (2.9). Hence, from (2.10),(2.11) and (2.12), we can write

$$\begin{bmatrix} b_0 & 0 & \dots & \dots & \dots & 0 \\ b_1 & b_0 & 0 & \dots & \dots & 0 \\ b_2 & b_1 & b_0 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ b_{N-1} & b_{N-2} & \dots & \dots & \dots & b_0 \end{bmatrix} \begin{bmatrix} \mathbf{out0} \\ \mathbf{out1} \\ \mathbf{out2} \\ \mathbf{out3} \\ \mathbf{out4} \end{bmatrix}^T \begin{bmatrix} k_0 \\ k_1 \\ k_2 \\ k_3 \\ k_4 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{2.13}$$

Thus, by doing a least square fit on (2.13), we can determine the coefficients. Here, N is the number of samples chosen for NTF fitting. Table. 2.2 shows the coefficients determined for different number of samples chosen for fitting. We see that the variation in the coefficients determined thus is less sensitive to the number of samples chosen for fitting. Further, this method gives a better estimate of the coefficients as we see that the peaking in the NTF response is much lower than in the open-loop fit case. The peaking in the NTF frequency response reduces to within 1.5 dB. Fig. 2.8 gives a comparison of the NTF responses of the two cases.

Table 2.2: Coefficients for different number of samples using Closed-loop fitting

Coefficients	Number of samples						
	20	30	40	50	60	70	80
k_0	0.7404	0.7398	0.7390	0.7377	0.7372	0.7366	0.7340
k_1	1.1631	1.1647	1.1637	1.1608	1.1599	1.1586	1.1534
k_2	0.4427	0.4406	0.4395	0.4381	0.4372	0.4366	0.4337
k_3	0.0849	0.0853	0.0852	0.0846	0.0845	0.0843	0.0834
k_4	0.0039	0.0038	0.0038	0.0037	0.0036	0.0036	0.0035

2.4 RC Tuning

The capacitors and resistors used in the design of the loop-filter vary across process-corners. In 130 nm technology, resistors vary by ±22% and capacitors vary by ±15%. Thus, the RC time constant of the integrators can vary between −33% and +40%. If the RC time constant becomes too low, the OBG increases

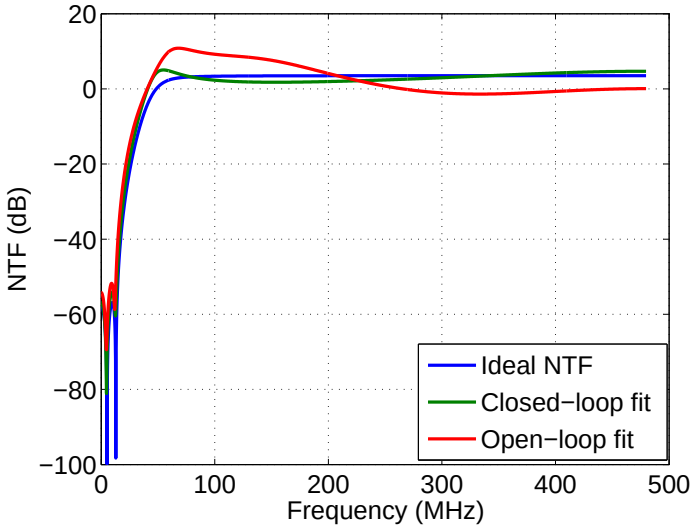


Figure 2.8: NTF Fitting

and can push the modulator towards instability. On the other hand, if the RC time constant increases, the in-band noise floor goes high and results in a deterioration of SNR. Hence, a course tuning of the resistors and capacitors is required to ensure that the modulator doesn't go into instability or result in a deterioration of SNR.

In this design, we employ tuning in both capacitors and resistors. 2 bit tuning in resistors and 3 level tuning in capacitors in employed. This ensures that the RC time constant is within 10% of the nominal value. Fig. 2.9 and Fig. 2.10 shows the capacitive and resistive banks respectively.

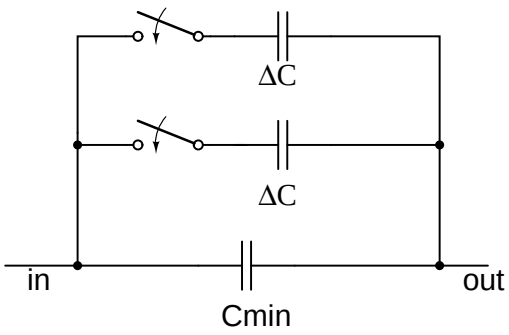


Figure 2.9: Capacitor Bank

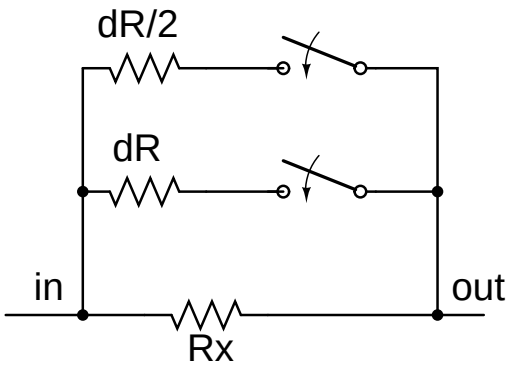


Figure 2.10: Resistor Bank

2.5 Opamp Design

In this section, we shall discuss the design of the opamps used in the loop filter. Also will be discussed the method of *Opamp Assistance*, which helps in reducing the distortion introduced by the first opamp.

2.5.1 First Integrating Opamp

The first integrating opamp is the most critical opamp in the design of the loopfilter. The noise of the first opamp reflects directly at the input and the first opamp is also the main contributor for distortion.

To choose the architecture of the opamp to be used, we need to arrive at the specifications required for the design. Firstly, the opamp has to have a large enough DC gain such that it doesn't degrade the SNR significantly. It can be shown that the DC gain A > OSR [6] if the SNR is not to degrade significantly. The output and the input common mode levels should be identical and the noise of the opamp should be such that SNR at the input is at least 70 dB. With these specifications, we can conclude that single stage opamps cannot be used, because their DC gains are very low. If we try improving the DC gain by using a telescopic cascode , it would be very difficult to maintain the input and the output common mode levels identical by maintaining all the transistors in saturation. A folded cascode can eliminate the problem of common mode levels but at the cost of

additional noise. These drawbacks force us to choose two stage architectures.

Two stage Miller compensated architectures provide high DC gain, high output swings and lower noise. But the drawback is that they require a large amount of power and area for getting a particular bandwidth. Instead, one can use feed-forward compensated architectures which give the same bandwidth at much lower power and area but at the cost of output swing. But since we can scale down the output swings such that the opamp does not saturate without affecting the performance of the modulator, feed-forward architecture was the choice of this design.

Feed-forward Compensated architecture

Fig. 2.11 shows the block diagram of a feedforward compensated opamp. We can write the transfer function of the opamp as

$$H(s) = \frac{Gm_1Gm_2 + Gm_3G_{01} + sC_1Gm_3}{(sC_1 + G_{01})(sC_2 + G_{02})} \tag{2.14}$$

The transfer function has two poles at G_{01}/C_1 and G_{02}/C_2 and a zero at Gm_1Gm_2/sC_1Gm_3. The DC gain is

$$\frac{Gm_1Gm_2 + Gm_3G_{01}}{G_{01}G_{02}}$$

If the zero is much lower than the Unity Gain Frequency (UGF) of the opamp, then we get a first order (20 dB/dec) roll off at the UGF and at the same time, we get the DC gain of a Two stage opamp.

Technique of Opamp Assistance

Fig. 2.12 shows the circuit diagram of an Active RC integrator. The opamp is assumed to behave like a transconductor g_m. The nonlinearity in the opamp arises due to the nonlinear dependence of the output current to the input voltage

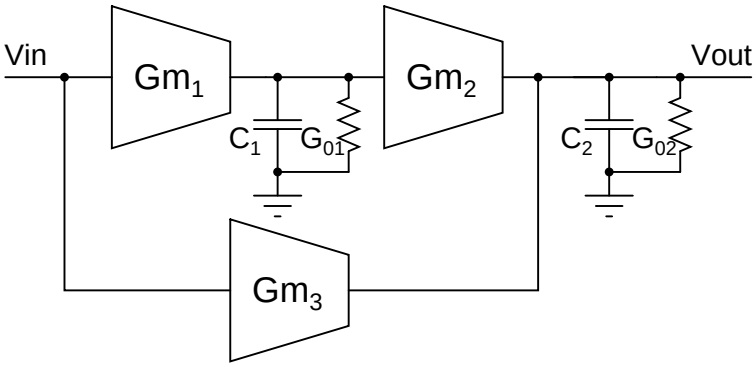


Figure 2.11: Feed Forward Architecture

of the opamp. We can write the non-linear output current as

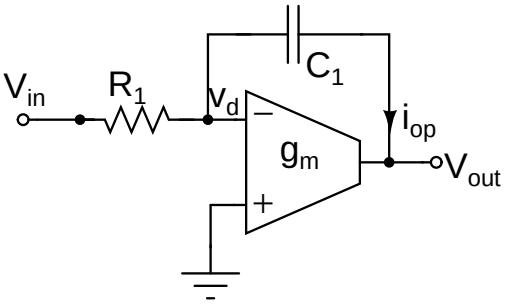


Figure 2.12: Active RC Integrator

$$i_{op} = g_m v_d - g_3 v_d^3 \tag{2.15}$$

Thus, we see that the non-linearity increases as v_d increases and vice-versa. We can roughly write v_d as

$$v_d = \frac{V_{in}}{1 + g_m R_1} \tag{2.16}$$

Thus, by increasing the loop gain $g_m R_1$, we can reduce v_d and thus, reduce non-linearity. But, we cannot increase R_1 because it will increase the input referred thermal noise. Increasing g_m means that it would require more power consumption in the opamp.

The primary function of the g_m cell is to maintain the virtual ground for C_1 such that integration happens. In the process, it supplies all the current through

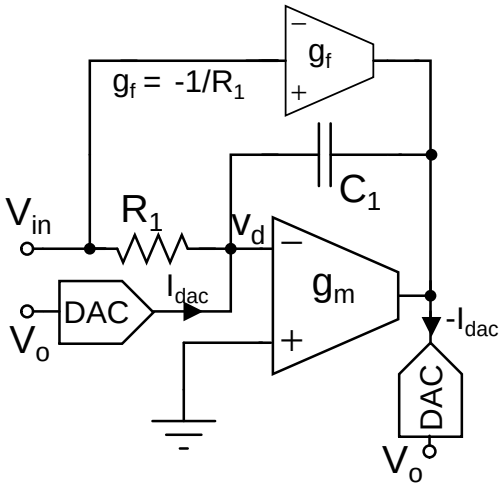
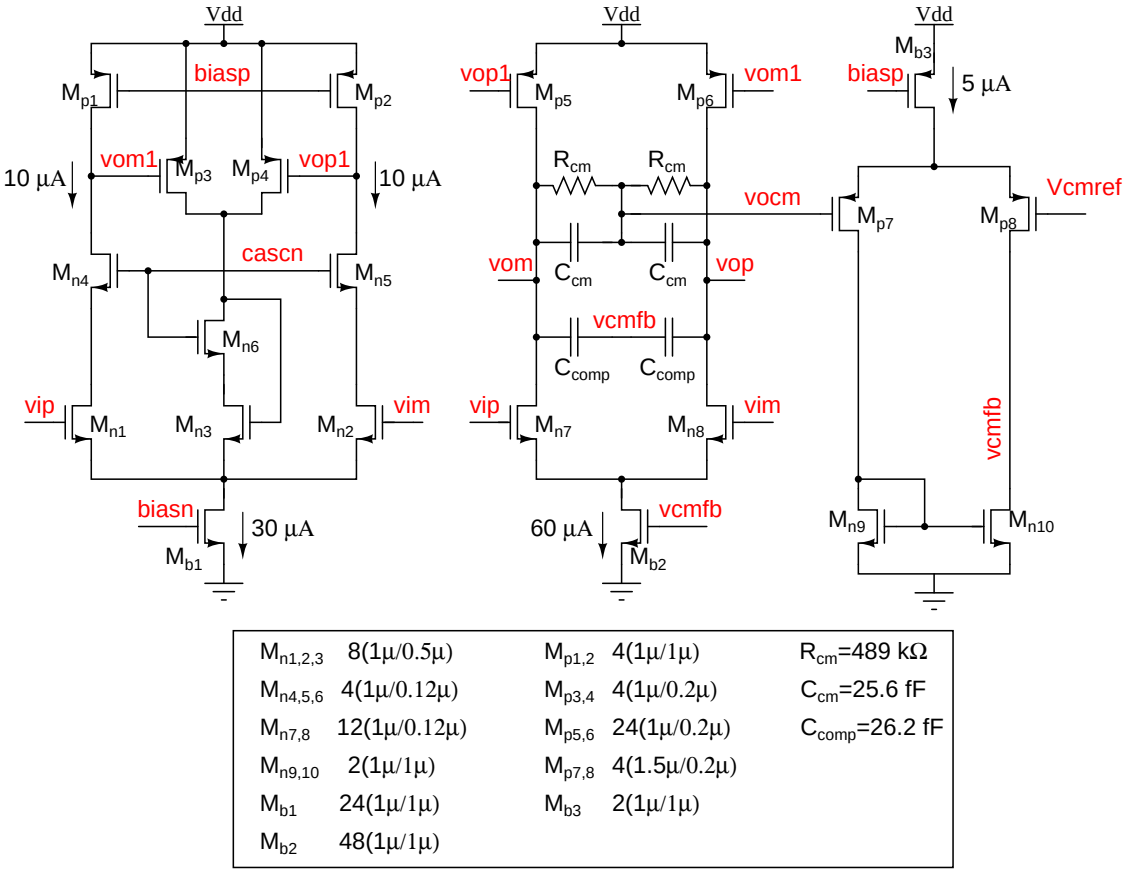


Figure 2.13: Technique of Current Injection

C_1 and hence, causes non-linearity. Hence, if there is an external element which supplies the current through C_1, the current supplied by the opamp will reduce and also the non-linearity. Fig. 2.13 shows the technique of *Opamp Assitance*, wherein, an additional DAC and a transconductor block G_f supply the DAC current and the input current respectively at the output of the opamp. This ensures that the opamp supplies only the error current between the input and the output currents thereby reducing the non-linearity. Also, the power and the slew rate requirements of the opamp are significantly reduced.

Design of First Integrating Opamp

Fig. 2.14 shows the circuit diagram of the first integrating opamp. The main contributor to the total noise is the first stage of the opamp because it passes through a high gain. Flicker noise is not a serious issue in this design because the bandwidth of interest is assumed to be 500 kHz to 15 MHz. Yet, to reduce the flicker noise, the input transistors are chosen to have a length of 500 nm. The total input referred thermal noise voltage spectral density of the opamp can be



$M_{n1,2,3}$	8(1µ/0.5µ)	$M_{p1,2}$	4(1µ/1µ)	R_{cm}	=489 kΩ
$M_{n4,5,6}$	4(1µ/0.12µ)	$M_{p3,4}$	4(1µ/0.2µ)	C_{cm}	=25.6 fF
$M_{n7,8}$	12(1µ/0.12µ)	$M_{p5,6}$	24(1µ/0.2µ)	C_{comp}	=26.2 fF
$M_{n9,10}$	2(1µ/1µ)	$M_{p7,8}$	4(1.5µ/0.2µ)		
M_{b1}	24(1µ/1µ)	M_{b3}	2(1µ/1µ)		
M_{b2}	48(1µ/1µ)				

Figure 2.14: First Integrating Opamp

roughly written as

$$S_n(f) = \frac{16kT}{3g_{mn}}(1 + \frac{g_{mp}}{g_{mn}}) \tag{2.17}$$

where g_{mn} and g_{mp} are the transconductances of the transistors $M_{n1,2}$ and $M_{p1,2}$ respectively. Thus, to reduce the input referred noise, we need to have a large g_{mn} and a small g_{mp}. In the current design, the total input referred noise due to the opamp alone is $57.9\mu V_{\text{rms}}$. The cascode device is eliminated on the PMOS side of the first stage by having a long channel transistor for $M_{p1,2}$ which ensures that the output impedance of the PMOS and the NMOS legs are comparable.

The second stage is designed such that it carries enough current to supply the second integrating resistor, the resistor which realizes the coefficient k_1 and also the common mode sensing circuit. The current to be supplied to the integrating

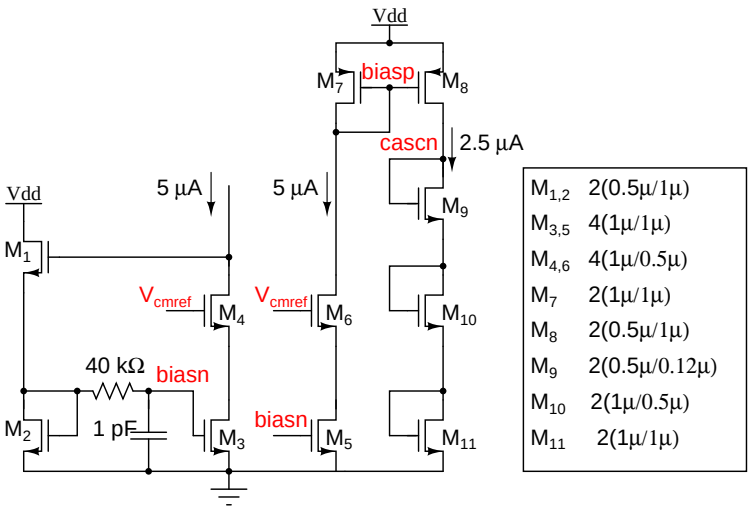


Figure 2.15: First Integrating Opamp bias circuit

capacitor is supplied by the feedforward DAC and the G_m block. Transistors $M_{p5,6}$ are a scaled version of $M_{p3,4}$ and this determines the second stage current.

CMFB circuitry

The feedforward opamp has two stages of common-mode feedback. The first-stage CMFB loop consists of the transistors, $M_{n3}, M_{n6}, M_{p3,4}$, $M_{n1,2}$ and $M_{n4,5}$. If the common-mode level of v_{om1} and v_{op1} increases, the currents in $M_{p3,4}$ will decrease which in turn will decrease the current in M_{n3}. Since the total tail current is constant, this will result in an increase in current in $M_{n1,2}$ thus helping in bringing down the common mode output level of the first stage.

The second-stage CMFB loop has the common-mode sensing resistors R_{cm} and the feedback loop ensures that the common-mode level is fixed to V_{cmref}. We add additional capacitors C_{cm} signals in parallel to R_{cm} which help in sensing high frequency common mode jumps. Since the CMFB loop is a two stage, we need to compensate it by adding a miller capacitance C_{comp} to stabilize the loop.

Fig. 2.16 shows the magnitude and phase responses of the first integrating opamp. Table 2.3 summarizes the opamp characteristics. Fig. 2.17 shows the common-mode step response of the first opamp.

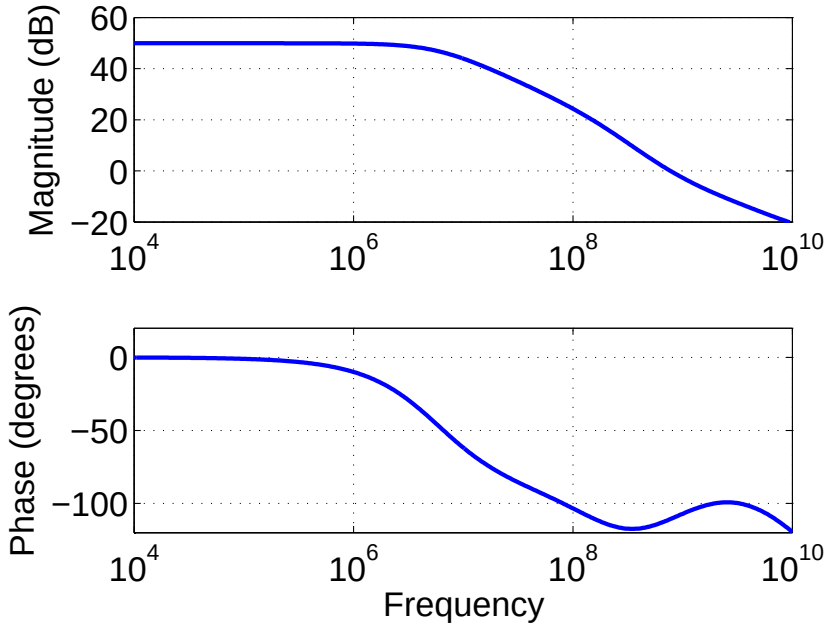


Figure 2.16: First Integrating Opamp AC Response

Table 2.3: First Opamp Characteristics

DC Gain	49.5 dB
UGF	773 MHz
Phase Margin	69.5°
Input Referred Noise	57.9 μV_{rms}
Power consumption	12,μW

2.5.2 Other Integrating Opamps

The other integrating opamps have relaxed constraints on the specifications on DC gain, unity gain frequency and slew rate. Hence, we use a scaled version of the first opamp for the other integrators. The only limitation is that it has to supply enough current for its loads. Hence, we choose an output stage tail current of 30 μA. Fig. 2.18 shows the circuit diagram of the other integrating opamps and Fig. 2.19 shows the corresponding bias circuitry.

Fig. 2.20 shows the magnitude and phase responses of the second integrating opamp. Tab. 2.4 summarizes the opamp characteristics. Fig. 2.21 shows the

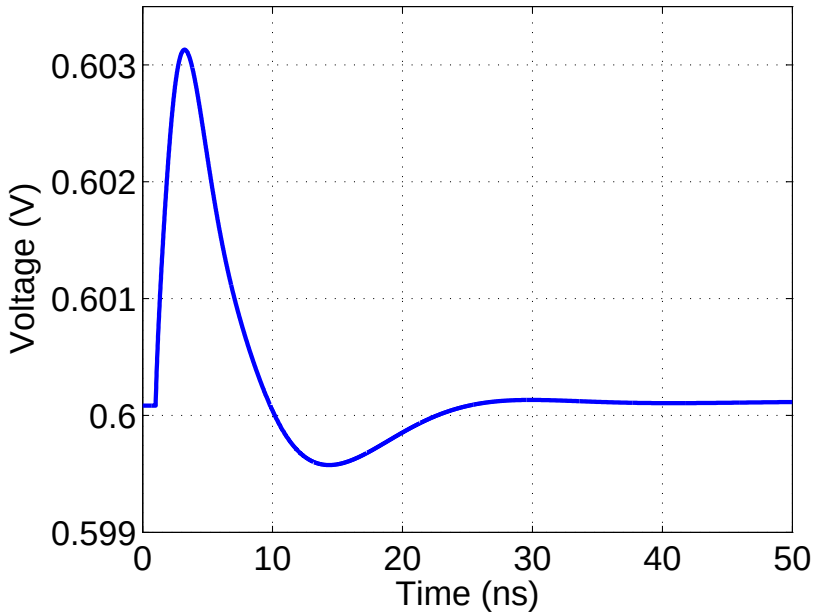


Figure 2.17: First Integrating Opamp Common Mode Step Response

common-mode step response of the second opamp.

Table 2.4: Second Opamp Characteristics

DC Gain	51 dB
UGF	438 MHz
Phase Margin	81°
Power consumption	57 μW

2.5.3 Summer Opamp

The summer opamp design has tight specifications on the UGF and the phase margin. The bandwidth of the summer block has to be greater than the f_s to ensure that the pulse response of the summer block settles within one clock period. The swing at the output of the opamp is limited to 600mV$_{\text{pp,d}}$ by scaling down the feedback resistance by a factor of 4. This enables us to use feed-forward architecture for the summer opamp as well. The summer opamp is also a scaled version of the first integrating opamp. Fig. 2.22 shows the circuit diagram of

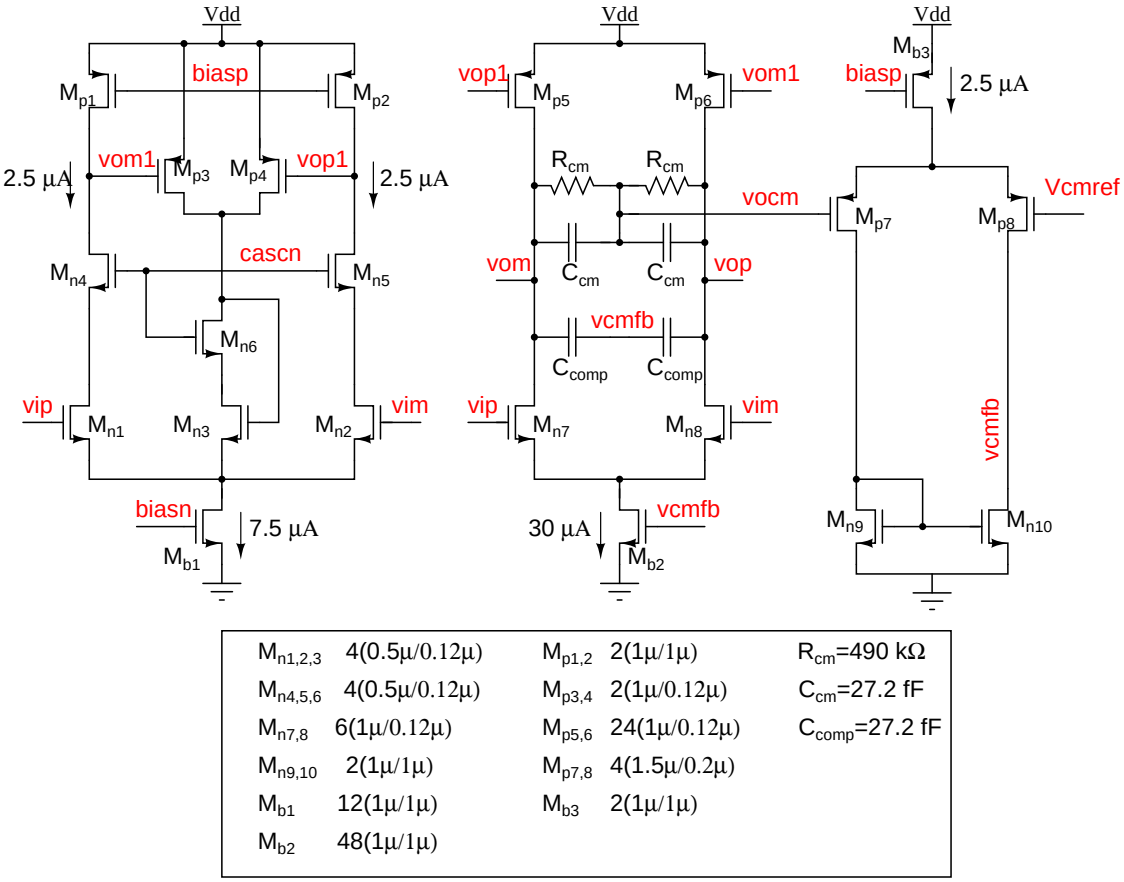


Figure 2.18: Second Integrating Opamp

the summer opamp and Fig. 2.23 shows its bias circuit. The sizes of the input transistors are chosen such that their input capacitances are as small as possible so that they do not result in a deterioration of the phase margin.

Fig. 2.24 shows the magnitude and phase responses of the summer opamp. Tab. 2.5 summarizes the Opamp characteristics. Fig. 2.25 shows the common-mode step response of the summer opamp. Fig. 2.26 shows the response to a pulse of the summer opamp.

Table 2.5: Summer Opamp Characteristics

DC Gain	50 dB
UGF	2.468 GHz
Phase Margin	89°
Power consumption	276 μW

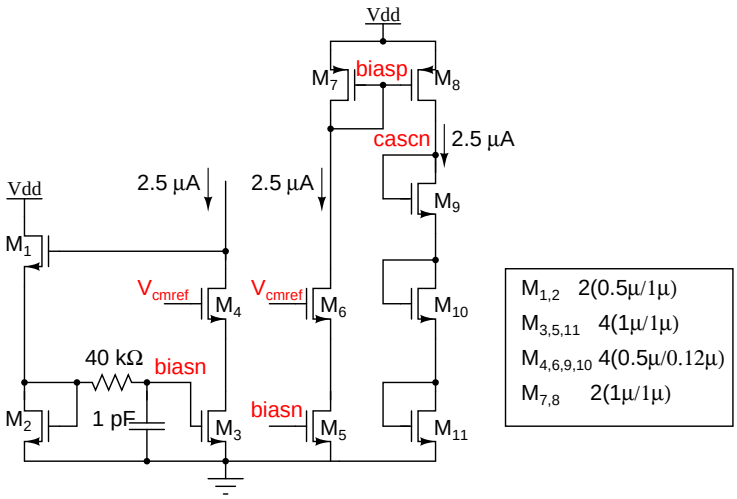


Figure 2.19: Second Integrating Opamp bias circuit

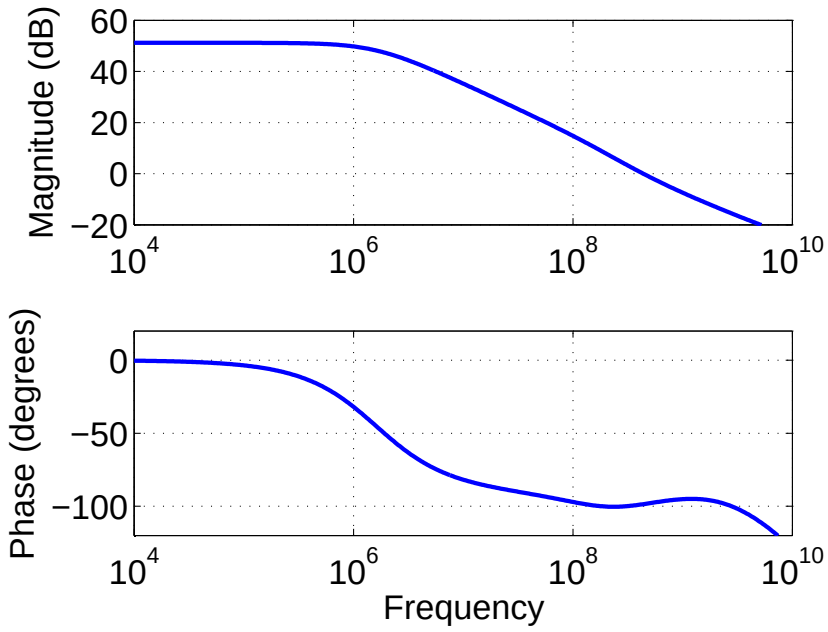


Figure 2.20: Second Integrating Opamp AC Response

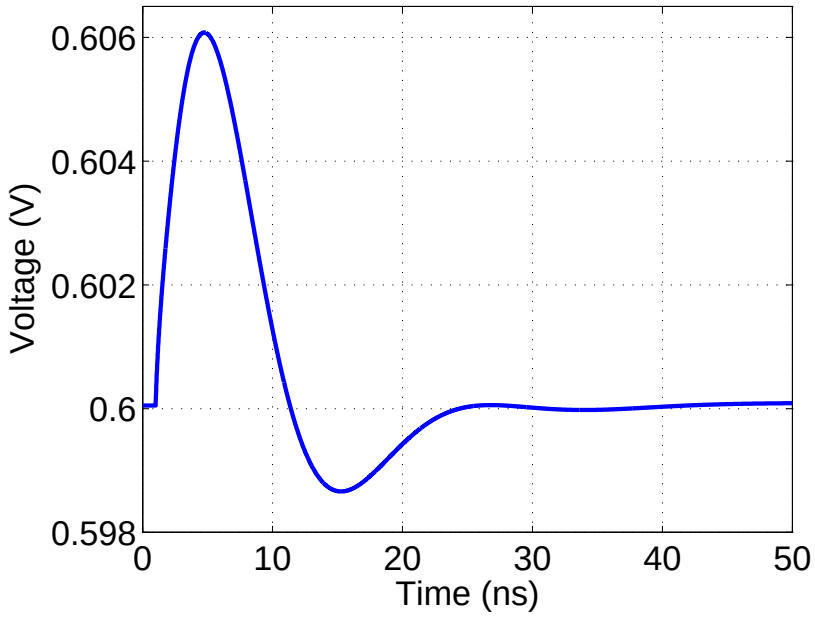
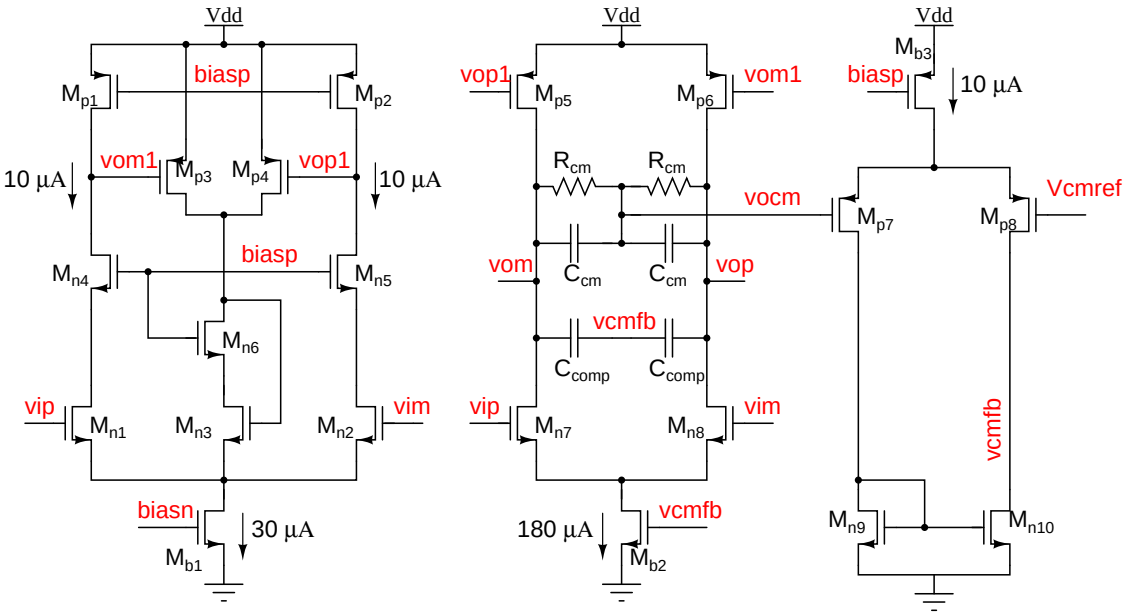


Figure 2.21: Second Integrating Opamp CMFB Response



$M_{n1,2,3}$	4(0.5µ/0.2µ)	$M_{p1,2}$	4(2µ/1µ)	R_{cm}	=490 kΩ
$M_{n4,5,6}$	4(0.5µ/0.12µ)	$M_{p3,4}$	2(0.3µ/0.12µ)	C_{cm}	=17.8 fF
$M_{n7,8}$	6(1.5µ/0.12µ)	$M_{p5,6}$	36(0.3µ/0.12µ)	C_{comp}	=17.8 fF
$M_{n9,10}$	2(1µ/0.5µ)	$M_{p7,8}$	4(1.5µ/0.2µ)		
M_{b1}	12(1µ/0.5µ)	M_{b3}	4(2µ/1µ)		
M_{b2}	72(1µ/0.5µ)				

Figure 2.22: Summer Opamp

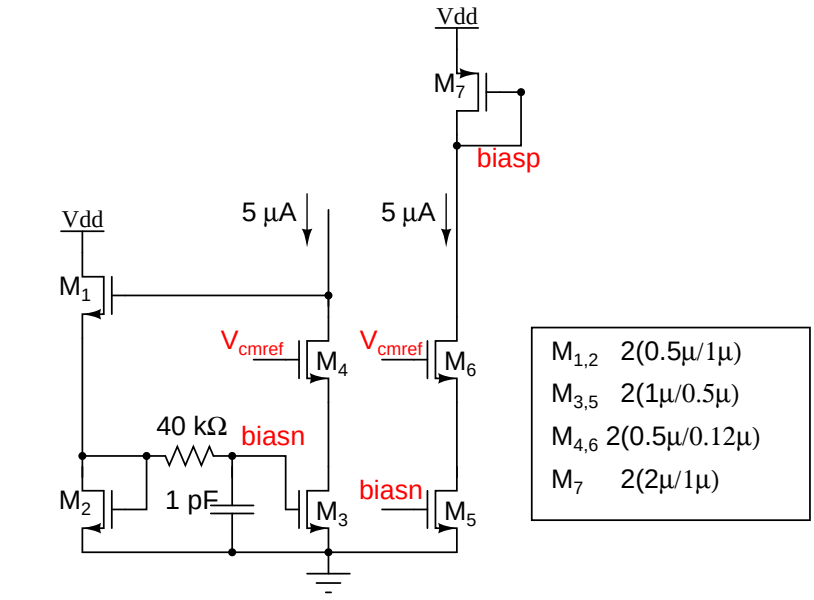


Figure 2.23: Summer Opamp bias circuit

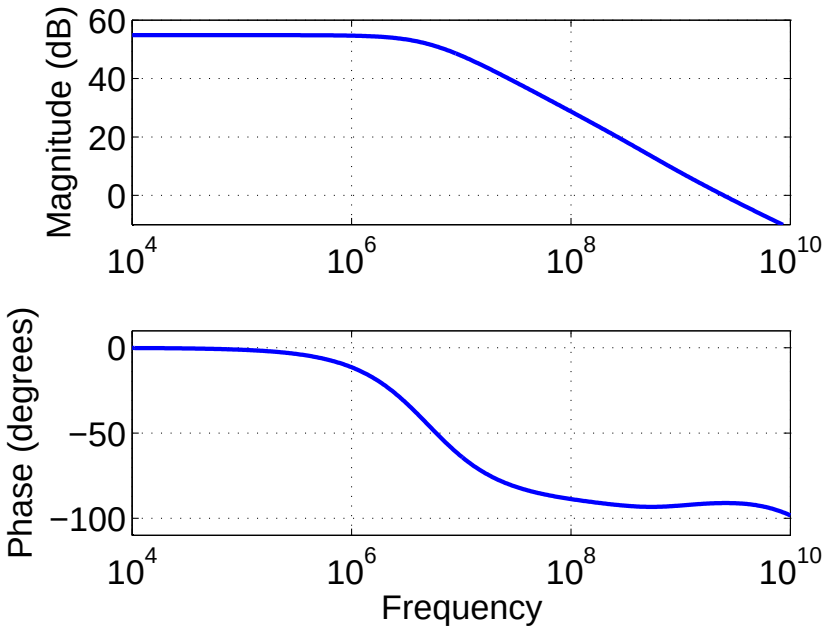


Figure 2.24: Summer Opamp AC Response

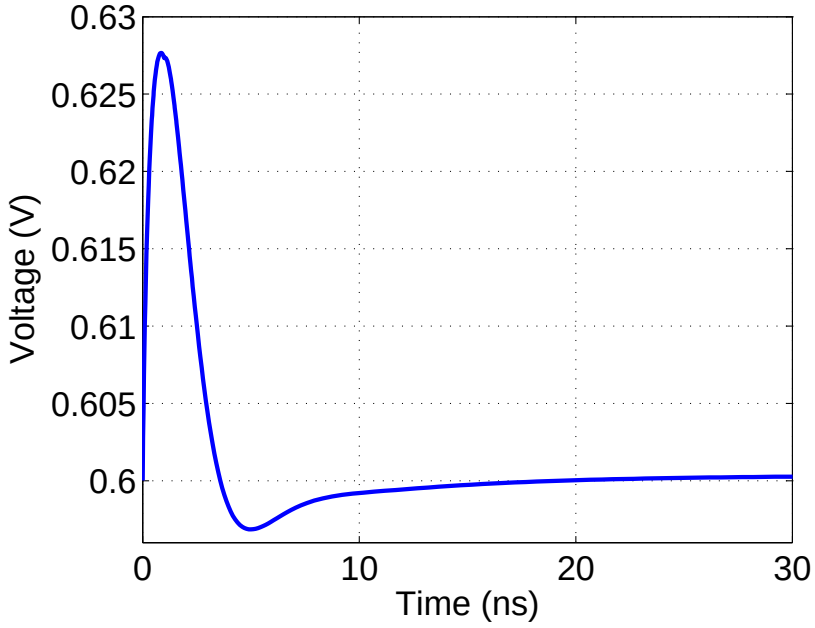


Figure 2.25: Summer CMFB Response

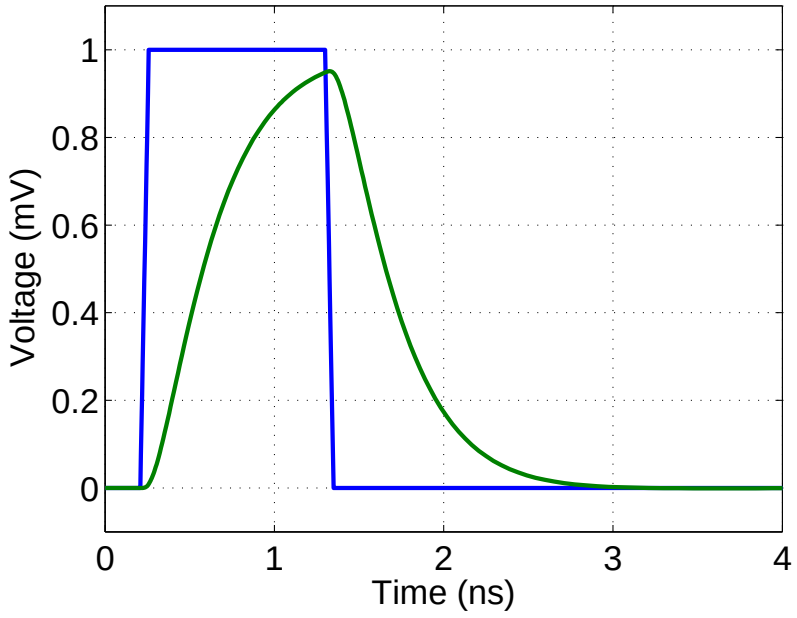


Figure 2.26: Summer Pulse Response

CHAPTER 3

Quantizer and DAC Design

The quantizer block converts the analog continuous-time signal from the output of the loop-filter into a discrete-time digital signal. Typically, in high-speed designs, *Current Mode Logic* (CML) is used to implement latches, buffers or inverters because they tend to consume lesser power and can have lower delays. However, here we choose to use CMOS logic due to the following. Firstly, CMOS logic is easier to implement and provides cleaner waveforms. Further, the quantizer has only one bit, and so the power consumption is comparable to CML. Finally, one needs to use level shifters in CML at the output of the loop filter and before the input of the DAC. These introduce additional delay, and hence, the total delay in either CMOS or CML logic can be comparable.

Fig. 3.1 shows the block diagram of the quantizer followed by the DAC which feeds the analog signal back into the loopfilter. The quantizer consists of a latch and the C^2MOS buffer. The DAC control buffer is used to give a jitter-free digital signal to the input of the feedback DAC. The direct-path DAC is used to compensate for excess loop-delay and the feedforward DAC is used to supply the current to the output of the first opamp to avoid slewing of the opamp.

3.1 Latch Design

Fig. 3.3 shows the circuit diagram of the latch used in the design. It has two back to back connected inverters in positive feedback which help in regeneration of the sampled signal. Fig. 3.2 shows the timing diagram of the clocks used in the latch.

During phase ϕ_1, clock LC is high and LE is low. In this phase, the latch is in tracking mode, where the outputs of the latch track the input. In phase ϕ_2,

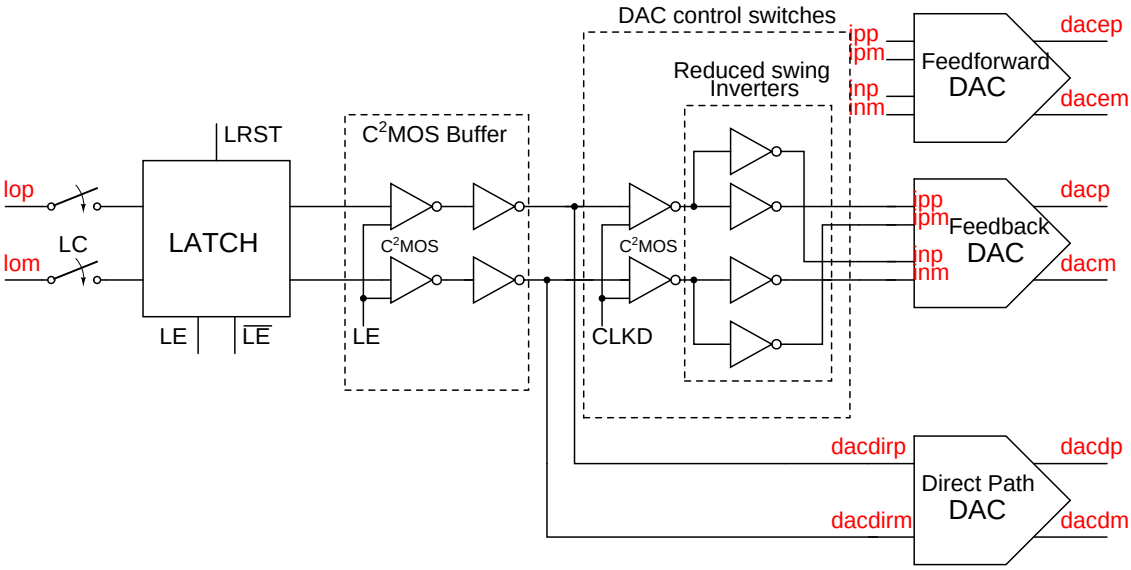


Figure 3.1: Block Diagram of Quantizer

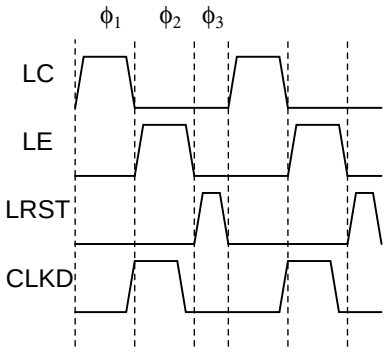


Figure 3.2: Timing Diagram of Clocks

LE goes high and LC goes low. The outputs are disconnected from the input and the latch enters regenerate mode, i.e. in positive feedback. Depending on the sign of the input at the time of sampling (rising edge of LE), the two outputs get regenerated to V_{dd} and gnd respectively.

In phase ϕ_3, the latch enters Reset mode, where the two outputs are shorted together. The Reset phase has two purposes. Suppose there were no reset phase, after the regeneration phase ϕ_2, the outputs are at V_{dd} and gnd. This is kind of memory and the latch has a tendency to retain its previous values. This is called as *hysteresis*. This results in distortion at the output. Also, when the latch enters ϕ_1, the input is close to V_{cm} and hence, large differential spike currents flow

through the switches A,B which has to be supplied by the summer opamp of the loop filter. Large spike currents can result in changes in the output voltage of the loop-filter and hence, a wrong value will be sampled if the opamp is not quick enough to restore the correct value of the output. Also, the initial part of phase ϕ_1 is wasted in bringing the outputs close to V_{cm} after which the latch starts tracking the input. These problems are solved by using a reset phase which prepares the latch for the next tracking phase ϕ_1.

The sizes of the transistors used in the latch are critical to the proper functionality of the latch. The capacitance at the output node of the latch has to be as small as possible to ensure that the tracking and regeneration are fast. Hence, we ensure that all transistors have minimum lengths. The time constant of regeneration is proportional to g_m/C_L where g_m is the transconductance of the inverter close to V_{cm} and C_L is the total capacitance at the output node, which includes the intrinsic capacitance of the latch and the external capacitance of the load the latch drives. A very large inverter will increase the g_m at the cost of increased capacitance. A very small inverter will not have a sufficient g_m to drive the load. Thus, it is imporant to vary the sizes to see where the latch has the least regeneration time. A good starting point is to choose the sizes such that the total intrinsic capacitance is equal to the total external capacitance. The sizes of the PMOS and the NMOS transistors in the inverter are chosen such that the V_{magic} voltage is close to V_{cm}. If the $V_{magic} \neq V_{cm}$, then at the start of phase ϕ_2, if the inputs are very close to each other, both the outputs tend to go towards V_{cm}, and then start regenerating. This increases the regeneration time and also can result in wrong decisions. All the adjustments of the sizes of transistors are done in *ss* corner at 70° C because this is the corner which has the least g_m and hence, the largest regeneration time.

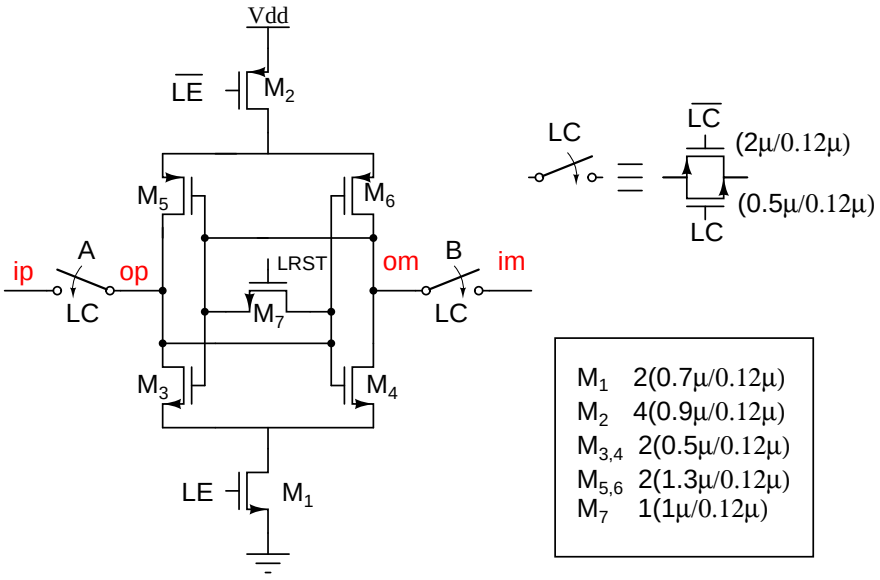


Figure 3.3: Circuit Diagram of Latch

3.2 C^{2}MOS Buffer

Fig. 3.4 shows the circuit diagram of the C^{2}MOS buffer. The C^{2}MOS Buffer is used to hold the output of the latch stable for the entire duration of a clock period. We see that the output of the latch is tracking the input during ϕ_1 and regenerating during ϕ_2. The C^{2}MOS Buffer is active during ϕ_2 when it buffers the regenerated output of the latch. During ϕ_1 the buffer is disconnected from the latch.

3.3 DAC Control Buffer

After the output of the loopfilter has been sampled and quantised, the signal has to be fed back through a DAC to close the loop. The output of the C^{2}MOS Buffer is the output of the quantizer. However, the waveform is highly jittery due to the varying regeneration times of the latch and if fed back, causes a significant rise in the in-band noise floor of the modulator. Hence, we use the DAC control buffer which are controlled by the clock CLKD which ensure a jitter-free DAC current waveform.

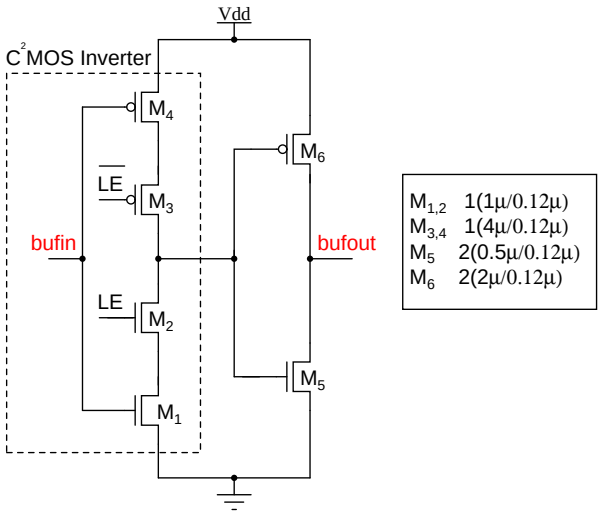


Figure 3.4: C^2MOS Buffer

Fig. 3.5 shows the circuit diagram for the DAC control buffer. The DAC control buffer controls the switches of the feedback and the feedforward current steering DACs. The circuit is a clocked inverter followed by an inverter whose output swing is reduced. The clocked inverter ensures that the output changes only when the clock turns high. The reduced swing inverters drive the feedback and the feedforward DACs.

The reduced swing inverters drive the switches M_{3-6}, M_{13-16} of the current steering DAC shown in Fig. 3.6. The signals which control the switches of the DAC should have a swing such that the current is steered in one direction or the other. On the other hand, if the switches in the DAC are driven by signals which run rail-to-rail, which are much larger than the required swing to steer the current in one branch, the swings at the tail nodes of the current sources of the DAC increase, resulting in distortion. Hence, we reduce the swing of the inverters to 600 mV. The feedback loop in Fig. 3.5 ensures that the swing at the output of the inverters are between 900 mV and 300 mV.

There are two separate inverters which control the NMOS and the PMOS switches. This is to ensure that both the switches do not go off at the same time when the control swings change sign. Ideally, we would like the signals to cross each other at V_{cm} but across corners, this crossover levels would vary which can

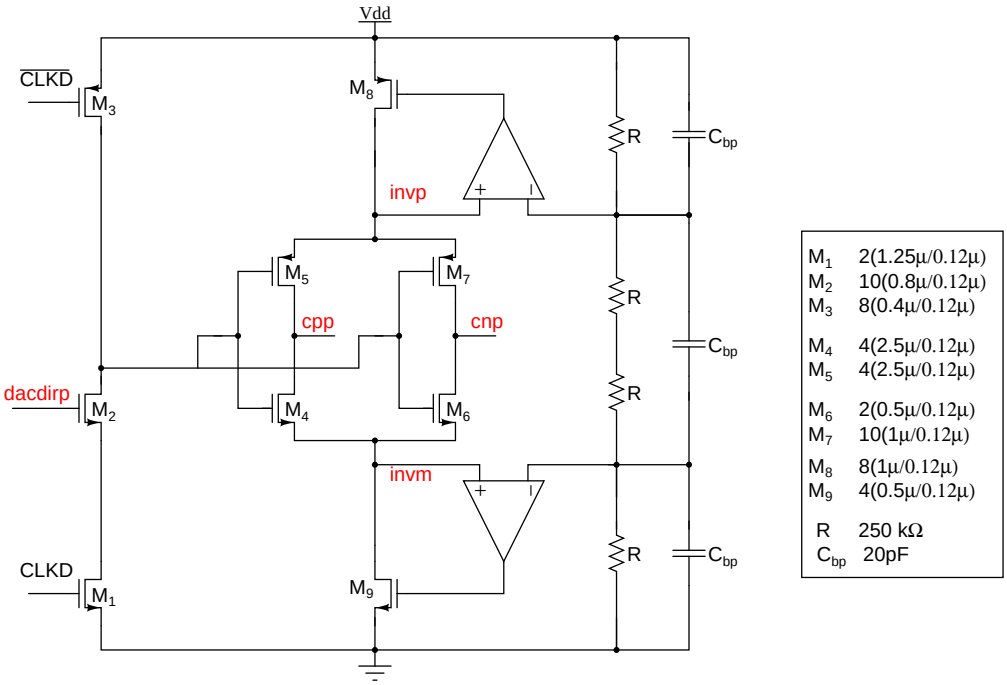


Figure 3.5: DAC Control Buffer

either crush the NMOS or the PMOS current sources. This would result in a dip in the tail node and hence, cause distortion. Hence, for PMOS switches, the control signals cross over at the lowest level while for NMOS switches cross over at the higest level as shown in Fig. 3.7. This ensures that none of the switches are off at the same time. The inverters controlling the PMOS switches have a strong NMOS which ensure that the fall time is much smaller than the rise time and ensure that the crossover is close to the lower level. Similar, the inverters controlling the NMOS switches have a strong PMOS which ensure that the rise time is much smaller then the fall time and the crossover is closer to the higher level. Fig. 3.8 and 3.9 show the signals that control the PMOS and the NMOS switches of the DAC respectively.

3.4 Feedback and Feedforward DAC

Fig. 3.6 shows the circuit diagram of the DAC. Both the feedback and the feed-forward DACs are current-steering DACs. The current in the feedback DAC is

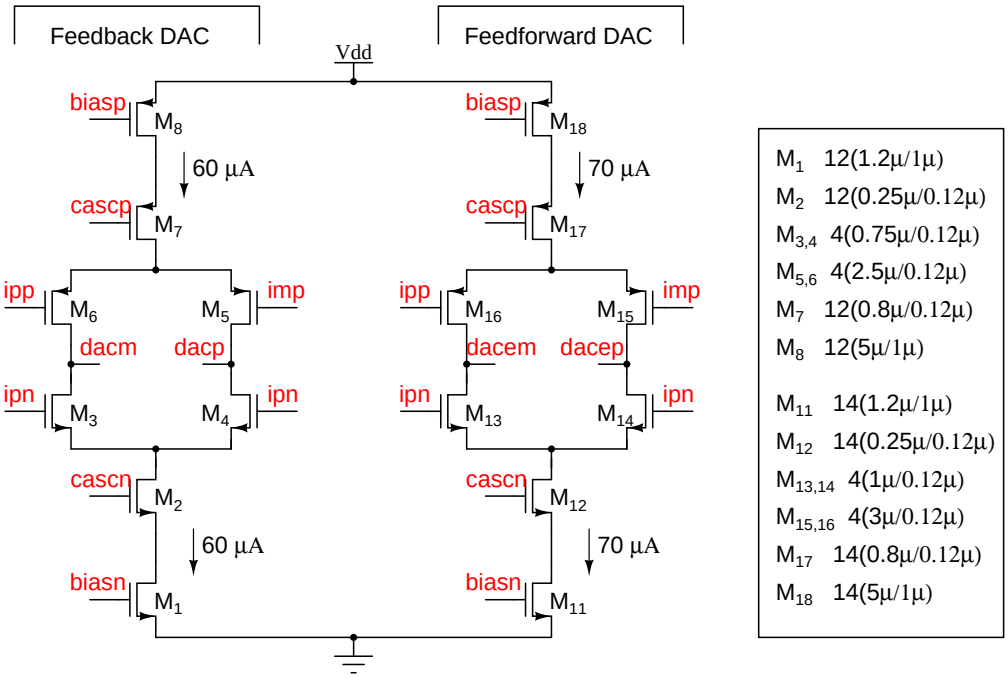


Figure 3.6: Current Steering DAC

designed to carry $60\,\mu$A of current. The FS of the design is $2.4\,\mathrm{V_{pp,d}}$ or $600\,\mathrm{mV}$ amplitude single-ended. Thus, if the input resistance is $10\,\mathrm{k\Omega}$, the current should be

$$I_{DAC} = \frac{600\,\mathrm{mV}}{10\,\mathrm{k\Omega}} = 60\,\mu\mathrm{A} \tag{3.1}$$

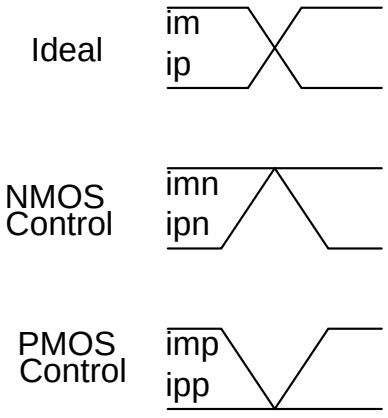


Figure 3.7: DAC control signals

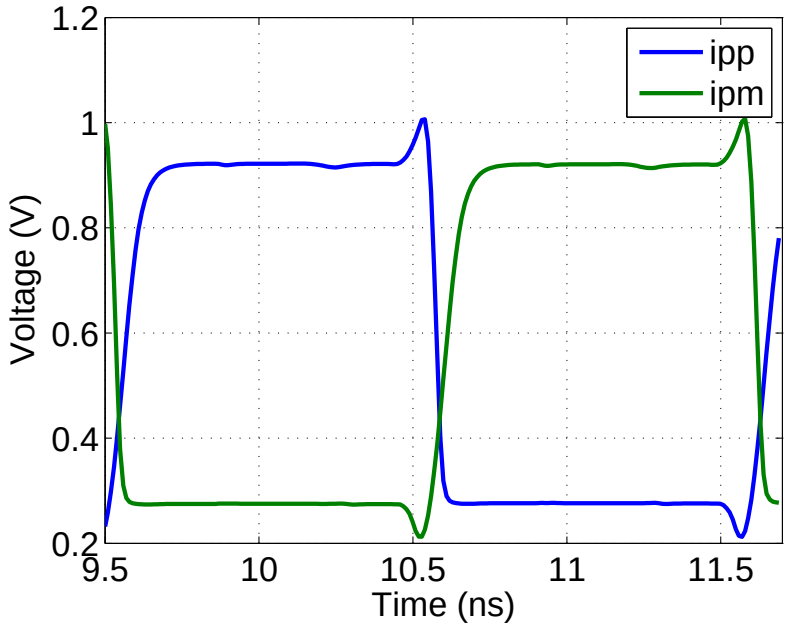


Figure 3.8: PMOS switch control signals

The noise contributed by the DAC is referred directly to the input and is critical to the design of the modulator. If the noise from bias circuit of the DAC is filtered off using a low-pass filter such that it doesn't contribute significant noise, then the input referred voltage noise spectral density contributed by the DAC will be

$$S_n(f) = \frac{8kT(g_{mn} + g_{mp})R^2}{3} \tag{3.2}$$

where g_{mn} and g_{mp} are the transconductances of the current sources M_1 and M_8. Thus, it is important to bias the current sources such that they have a low g_m or have a large overdrive. A very large overdrive will tend to reduce the headroom for the cascode device, which in turn, will lead to increase in the size of the cascode device and the associated capacitance at the tail node which can increase distortion. Thus, there is a trade-off between the overdrive and the tail node capacitance.

The total input referred noise contributed by the DAC is $157\,\mu\mathrm{V_{rms}}$ which

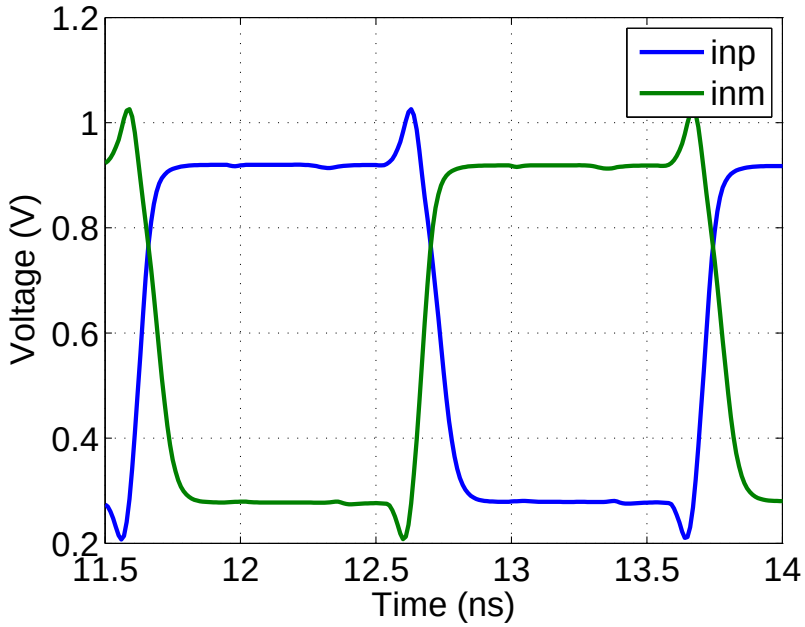


Figure 3.9: NMOS switch control signals

includes the noise from the bias circuit as well. The bias circuit contributes 20% of the total DAC noise. Table 3.1 summarizes the contribution to the total noise from different sources. The input referred thermal noise is such that it is 69.8 dB below the signal level at MSA.

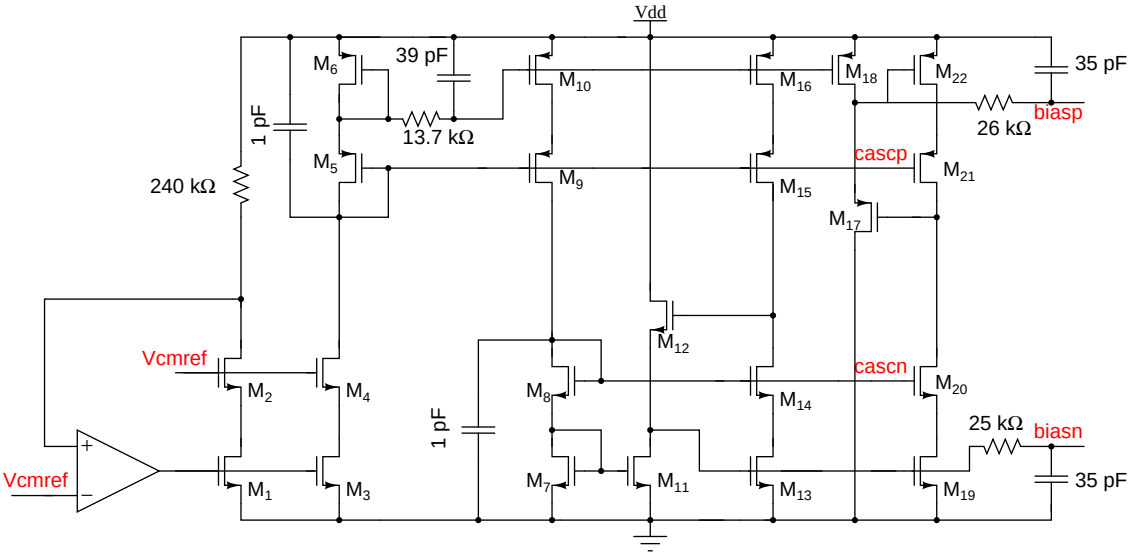
Table 3.1: Noise Contributors

Input Resistors	$70\,\mu V_{rms}$
First Opamp	$57.9\,\mu V_{rms}$
Feedback DAC	$157\,\mu V_{rms}$
Total Input Referred Noise	$182.2\,\mu V_{rms}$

The feedforward DAC is also a current-steering DAC but carries a higher current of $70\,\mu$A. The feedforward DAC feeds current at the output of the first opamp. The additional current helps in providing current to the capacitance in the common mode sensing circuit and the Miller compensating capacitance of the common-mode feedback loop of the first opamp. Thus, the opamp needn't supply the current for the above two capacitances which is taken care of by the

feed-forward DAC.

Fig. 3.10 shows the biasing circuit for the DAC. It uses a resistor servo loop to bias the current sources to a current of V_{ref}/R. The bias voltages generated are then filtered off using a low pass filter to ensure that the bias circuit doesn't contribute to noise significantly. We use MOS capacitors to realize capacitances of about 35 pF. The resistances are realized using MOSFETs operating in the triode region.



$M_{1,3}$	2(1.2µ/1µ)	$M_{7,8}$	2(0.5µ/1µ)	M_{14}	2(0.25µ/0.12µ)	M_{19}	2(1.2µ/1µ)
$M_{2,4}$	2(1.2µ/0.12µ)	M_{11}	2(0.25µ/1µ)	$M_{15,16}$	16(2.5µ/1µ)	M_{20}	2(0.25µ/0.12µ)
$M_{5,6}$	4(2.5µ/1µ)	M_{12}	2(0.25µ/0.12µ)	M_{17}	2(0.5µ/0.12µ)	M_{21}	2(0.8µ/0.12µ)
$M_{9,10}$	4(2.5µ/1µ)	M_{13}	2(1.2µ/1µ)	M_{18}	2(2.5µ/1µ)	M_{22}	2(5µ/1µ)

Figure 3.10: Bias Circuit for DAC

3.5 Direct Path DAC

Fig. 3.11 shows the circuit diagram for the Direct Path DAC. The Direct Path DAC is used to compensate for the excess loop delay in the system. It feeds current into the summer opamp. A resistor servo loop fixes the bias current in the DAC. As shown in Fig. 3.1, the input to the direct path DAC is taken from the output of the C^2MOS buffer and not after the DAC control buffers, i.e. the delay

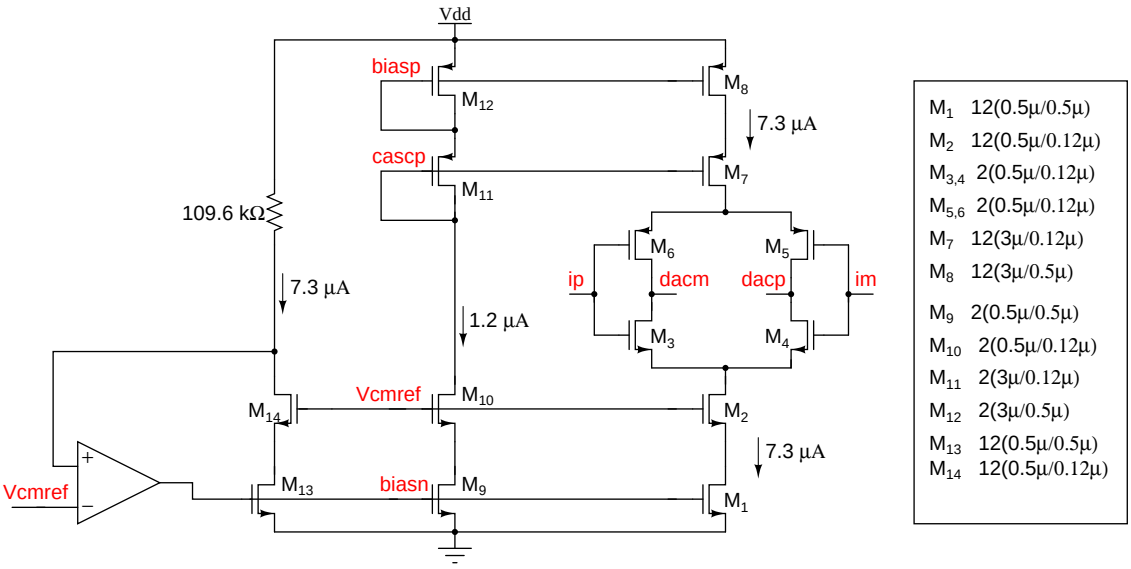


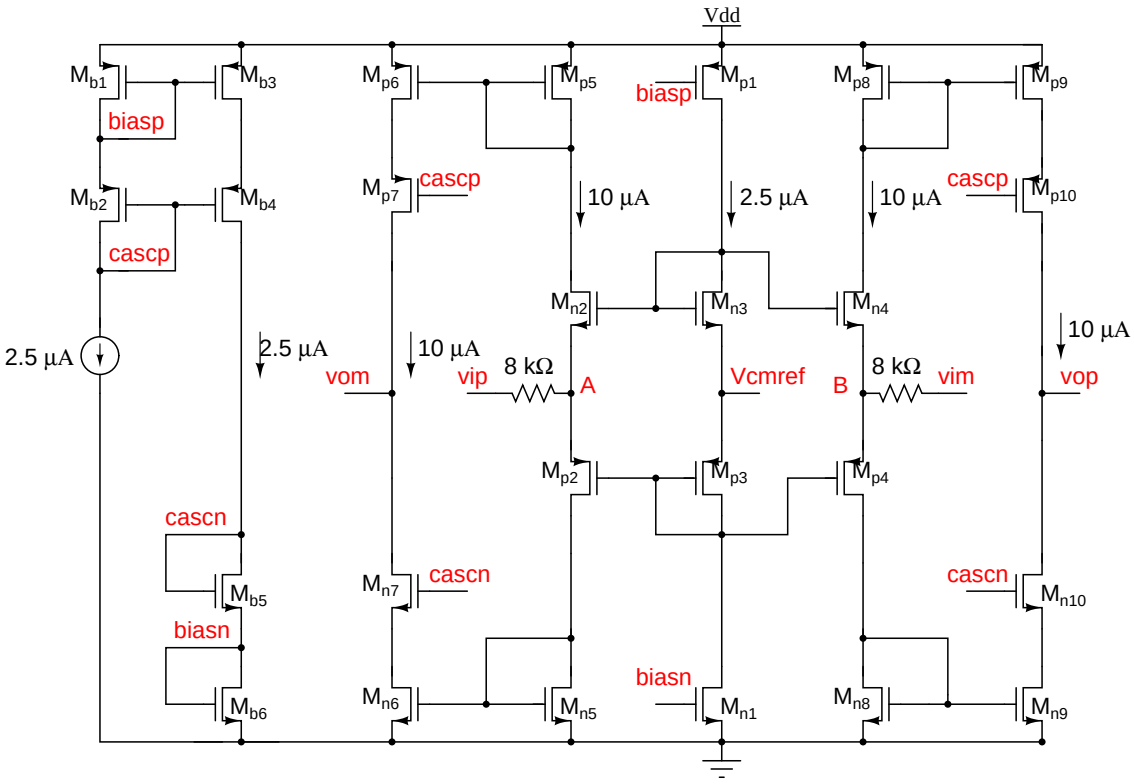
Figure 3.11: Direct Path DAC

for the direct path DAC is lower than that for the main feedback DAC. This is done for two reasons. Firstly, the signal provided by the direct path DAC need not be jitter free because jitter in the direct path DAC doesn't degrade the SNR. Hence, the jittery output of the C^2MOS buffer can be used to control the DAC. Secondly, by feeding the C^2MOS buffer output to the DAC, the summer opamp gets more time to respond to the pulse, such that it gives a settled output at the time of sampling. On the other hand, if the DAC pulse were to come at the input of the summer opamp at the same time as the feedback DAC pulse, the summer opamp should have been much faster so that the pulse response settles before the sampling instant.

CHAPTER 4

Miscellaneous Circuits

4.1 Feedforward G_m circuit



$M_{b1,3}$	2(1µ/0.5µ)	M_{n1}	2(0.5µ/0.5µ)	M_{p1}	2(1µ/0.5µ)
$M_{b2,4}$	2(1µ/0.12µ)	$M_{n5,6,7}$	8(0.5µ/0.5µ)	$M_{n5,6,8,9}$	8(1µ/0.5µ)
$M_{b5,6}$	2(0.5µ/0.5µ)	$M_{n8,9,10}$	8(0.5µ/0.5µ)	$M_{p7,10}$	8(1µ/0.12µ)
		M_{n2}	2(1µ/0.5µ)	M_{p2}	2(4µ/0.5µ)
		$M_{n3,4}$	8(1µ/0.5µ)	$M_{p3,4}$	8(4µ/0.5µ)

Figure 4.1: Feedforward G_m circuit

Fig. 4.1 shows the circuit diagram used for the feedforward G_m block. The feedforward G_m is used to supply the magnitude of the input current at the output

of the first integrating opamp so that the opamp doesn't need to provide the input current.

The feedforward G_m is a Class-AB type amplifier where the peak current supplied is much higher than the quiescent current. Nodes A and B in the circuit are low impedance nodes and are roughly maintained around V_{cmref}. Hence, if v_{ip} goes high, a current of $(v_{ip} - V_{cmref})/R$ flows into A through M_{n5}, M_{p2} and gets mirrored through $M_{n6,7}$ to the output. During this cycle, the transistors M_{n2} and M_{p5} get cut-off. Similarly, when v_{ip} goes low, the transistors M_{n2} and M_{p5} carry all the current while M_{n5}, M_{p2} get cut-off. The cascode devices $M_{n7,10}$ and $M_{p7,10}$ provide high impedance at the output nodes such that the output current doesn't depend on the swing at the output nodes. The G_m block, though is not very linear, does not contribute significantly to distortion because it supplies current at the output of the first opamp and the error current between the input and the G_m current is fed by the opamp. Due to the non-linear nature of the G_m block, the resistance is chosen to be $8\,\mathrm{k}\Omega$ which ensures that the error between the input current and the G_m current is minimum.

4.2 Clock Generator Circuit

Fig. 4.2 shows the clock generating circuit. The clock generating circuit takes in a differential sine wave clock from outside the chip and feeds it to the input of a CML buffer (a differential pair). Fig. 4.3 shows the circuit diagram of the CML buffer. The purpose of taking a differential clock from outside is to ensure that any coupling on to the clock signal is a common mode signal. The differential pair gets rid of the common mode coupling and passes a jitter free signal at the output of the buffer. The inverters following the differential pair convert the sine wave signal to a square wave because of their high gain. Non-overlapping clocks are generated using two back-to-back connected NAND gates.

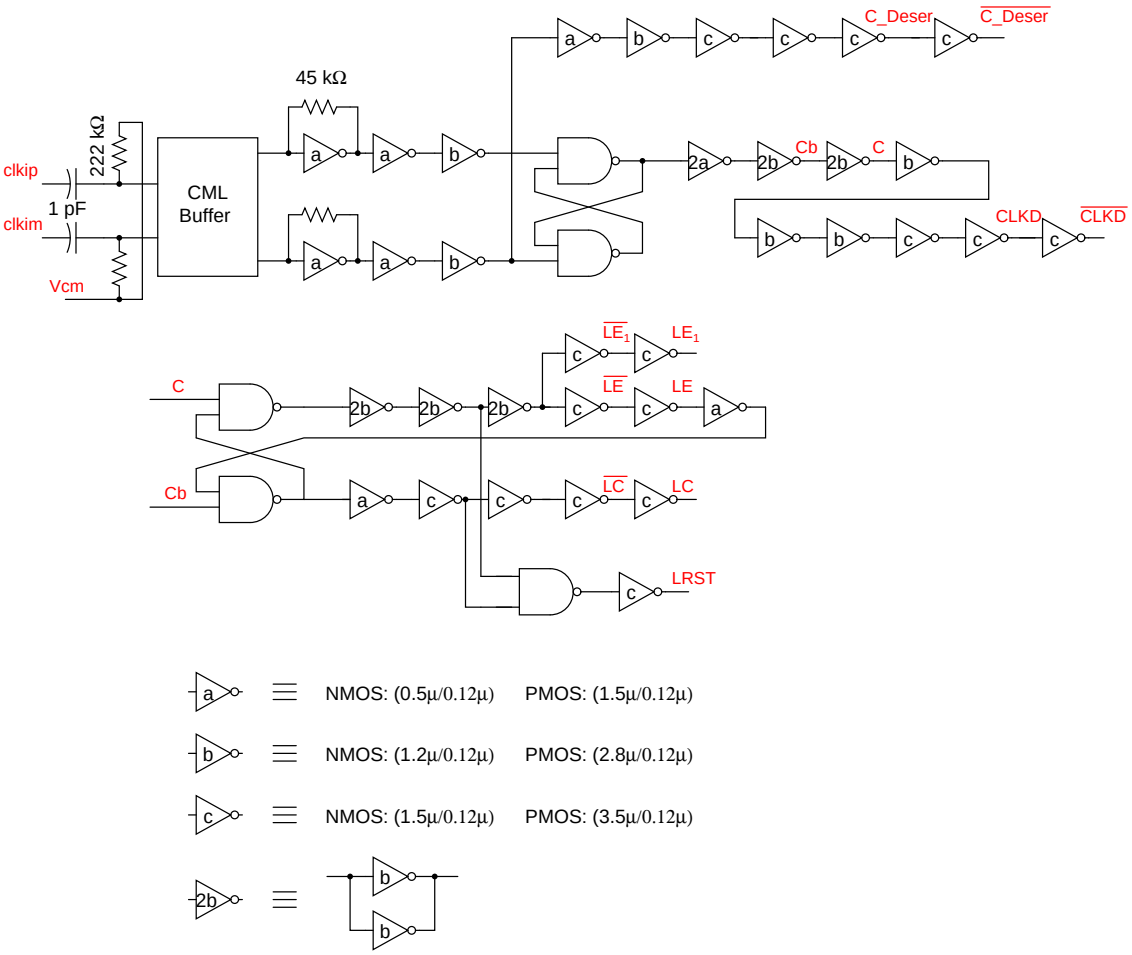


Figure 4.2: Clock Generator Circuit

4.3 Output Driver

The output data rate is at the sampling frequency, $f_s = 960\,\text{MHz}$. The logic analyzer used to measure the output spectrum has a limited bandwidth of about 200 Msps. Hence, it is necessary to deserialize the output to within the bandwidth of the logic analyser. There are not many deserializer chips which take in data at 960 MHz and deserialize it by a factor of 8. Hence, we deserialize the data by a factor of two on chip and further deserialize it on board to be fed into the logic analyzer. The deserializer on chip gives Low Voltage Differential Signal (LVDS) outputs at half the clock rate at 480 Msps.

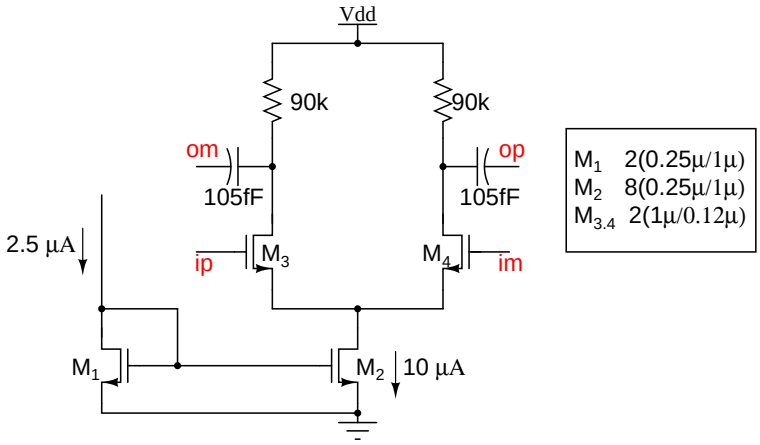


Figure 4.3: CML Buffer

CHAPTER 5

Layout, Simulation Results and Conclusion

5.1 Layout

The designed $\Delta\Sigma$ modulator was laid out using CADENCE Virtuoso Tool. Fig. 5.1 shows the layout of the design. The chip is packaged using a 24 pin QFN package. The modulator occupies an active area of about 850 μm X 450 μm. The deserializer occupies an area of 200 μm X 70 μm.

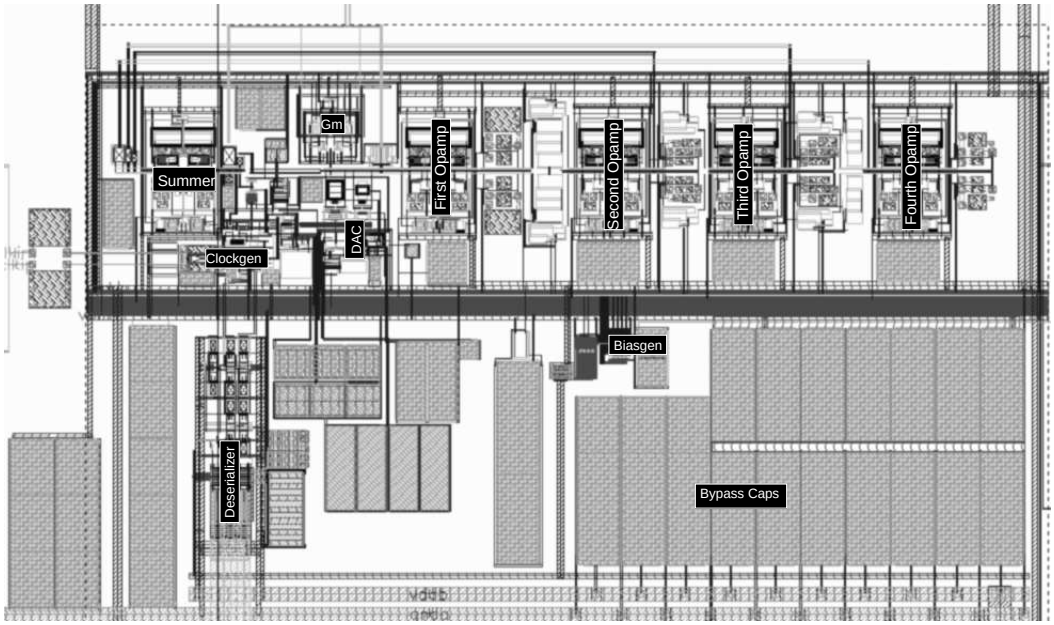


Figure 5.1: Layout of Modulator

5.2 Simulation Results

Simulations of the entire modulator were carried out with the extracted view after layout. An input sine wave of 1.3 $V_{pp,d}$ at a frequency of 2.8125 MHz was used

for the simulations. Table. 5.1 tabulates the SNDR and SFDR obtained across different corners. Fig. 5.2 shows the corresponding Power Spectral Densities.

Table 5.1: Simulation Results

Corners			SNDR	SFDR
MOS	Resistor	Capacitor		
ss	typ	typ	69.9 dB	76.7 dB
tt	typ	typ	67.2 dB	76.8 dB
ff	typ	typ	66.8 dB	72.2 dB
ss	max	max	68.9 dB	80.8 dB
ff	min	min	66.2 dB	76.4 dB

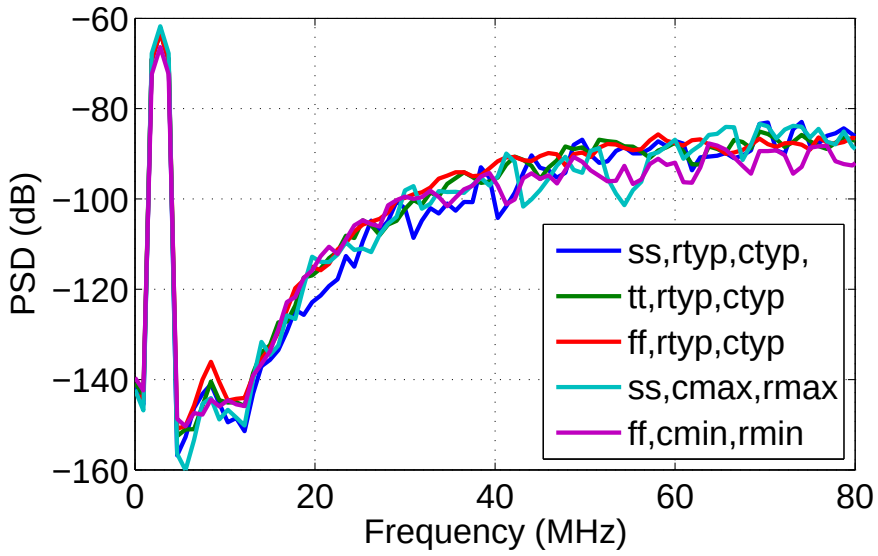


Figure 5.2: PSD of modulator

5.3 Conclusion

A fourth order single-bit continuous time $\Delta\Sigma$ modulator has been designed for 15 MHz bandwidth in 130 nm UMC CMOS technology. The technique of Opamp assitance has been used to reduce the distortion and the power consumption in the modulator. The total power consumption in the modulator is 2.23 mW, of which 850 μW is static power consumption in the loop filter, the DACs and the feed-

forward G_m blocks, 450 μW average power dissipated in the latch, C^{2}MOS buffer and the DAC control buffer and the remaining 936 μW in the clock generator.

5.4 Future Work

The maximum power dissipation in the modulator is in the clock generator circuitry because of the various clock phases required. Improvements in the latch design to eliminate the need for various clocks and redesigning of the clock generator circuit efficiently can reduce the power consumption by a significant factor.

APPENDIX A

Pin Details of the $\Delta\Sigma$ Modulator Chip

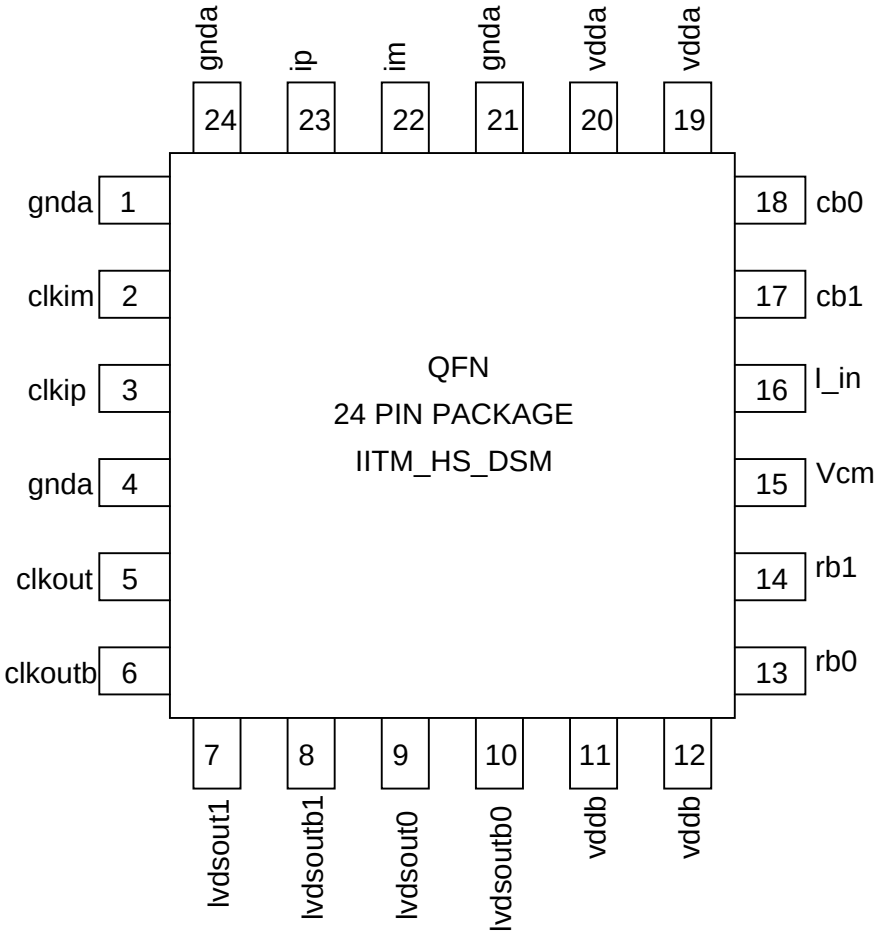


Figure A.1: Pin diagram of the $\Delta\Sigma$ modulator chip

Table A.1: Functionality of each pin

Pin	**Name**	**Functionality**
1,4,21,24	gnda	Ground
2,3	clkim, clkip	Differential input clocks
5,6	clkout, clkoutb	Differential output LVDS clocks
7,8,9,10	lvdsout1, lvdsoutb1, lvdsout0, lvdsoutb0	Deserialized differential output LVDS data stream
11,12	vddb	1.2 V supply voltage for the Deserializer
13,14	rb0, rb1	Resistor tuning bits
15	Vcm	Common mode reference voltage of 0.6 V
16	I_in	Reference Current source
17,18	cb1, cb0	Capacitor tuning bits
19,20	vdda	1.2 V supply voltage for the Modulator
22,23	im, ip	Differential input signals

REFERENCES

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley and Sons Inc, 2004.

[2] P. Ramalingam, "Design of a 16-bit continuous time delta-sigma modulator for digital audio," Master's thesis, IIT Madras, 2006.

[3] S. Pavan and P. Sankar, "A 110 μW single-bit audio continuous-time $\Delta\Sigma$ modulator with 92.5 dB dynamic range," in *Proceedings of the European Solid State Circuits Conference*, 2009.

[4] F. M. Gardner, "A transformation for digital simulation of analog filters," in *IEEE Trans. on Communications*, pp. 676–680, July 1986.

[5] R. Karthikeyan, "Analysis of clock jitter in delta-sigma modulators," Master's thesis, IIT Madras, 2007.

[6] M. W. Hauser and R. W. Brodersen, "Circuit and technology considerations for mos delta-sigma A/D converters," in *In Proc. Int. Symp. Circuits and Systems*, pp. 1310–1315, 1986.