DESIGN AND MODELING OF HIGH SPEED CURRENT STEERING DIGITAL-TO-ANALOG CONVERTERS

A THESIS

submitted by

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for the award of the degree

of

MASTER OF SCIENCE

(by Research)

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

JULY 2007

THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN AND MODELING OF HIGH SPEED CURRENT STEERING DIGITAL-TO-ANALOG CONVERTERS**, submitted by **Murali.S.S**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Science**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 6th September 2007

ACKNOWLEDGEMENTS

At the outset I am very grateful to my adviser Dr.Y.Shanthi Pavan for giving me an opportunity to work in the field of analog circuit design. I am also thankful to him for his excellent guidance and continuous motivation through out my project work. I am also thankful to Texas Instruments India Pvt Ltd for supporting my project work. My stay at IIT, Madras was made more than memorable by some great lab mates like Reddy Karthikeyan, I.Rajesh, Laxminidhi, Srini, Nanda Govinda and T.J. A special thanks to I.Rajesh who patiently put up with all my silly computing queries and was responsible for the seamless computing facilities in the lab. A special thanks to Laxminidhi for his great soldering finesse. I also thank Ms.Chella for helping me in populating the test board. And I dedicate this thesis work to my parents who were the greatest source of support and motivation during these three years.

ABSTRACT

A 10-bit current steering DAC has been designed, layed out and fabricated in 0.35 μm CMOS digital process. The DAC has been segmented in a manner to optimize area. To achieve an accuracy of 10 bits, special schemes have been employed in the layout of the thermometer section. The static and dynamic performances of the DAC have been characterized. The INL is less than 0.5 LSB and it exhibits a SFDR of around 52dB at Nyquist frequencies for a sampling frequency of 280MHz. Apart from this we have proposed a technique to model the thermometer section so as to reduce the simulation time.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Evolving technological fields such as video signal processing, digital signal synthesis and wireless communications demand high-speed and high accuracy digital-to-analog converters(DAC's).For such high linearity and high speed applications current steering DAC's have become the mainstay because of their inherent advantages over resistor string DAC's. This is because - 1) they can be designed in a standard CMOS digital process, thereby cutting down cost and power consumption as they can be easily integrated with digital circuits, and 2) they are intrinsically faster and more linear than other architectures and 3) they can drive an output resistive load directly without requiring the use of an extra buffer.

The DAC that we have designed is a 10-bit segmented current steering DAC. The segmentation is done in a manner to optimize the area (Lin and Bult (1998)). To achieve an accuracy of 10-bit, apart from careful design a lot of attention should be given to the layout. This is because linear and quadrant gradients in the surface of the die will give rise to systematic errors. These errors will contribute to the output non-linearity. Hence to reduce these errors we adopt certain switching and arrangement techniques in the layout. Apart from the systematic errors, random errors too lead to non-linearity. The current sources should be sized appropriately depending on the INL specification that we want to meet.

Current steering DAC's, especially thermometer coded DACs consume a lot of simulation time. Though many techniques to model the DAC so as to reduce the simulation time have been proposed, they suffer from many pitfalls. In this thesis we have proposed a modeling technique which apart from reducing the simulation time drastically overcomes the pitfalls of the previous techniques.

1.2 ORGANIZATION OF THE THESIS

The thesis is organized as follows. In chapter 2, the various architectures available in current steering DACs are discussed. Also the static non-linearity in each of these architectures is dealt with. Chapter 3 deals with the design of the various sub-blocks in detail. In Chapter 4, the modeling technique that we have proposed is discussed. Chapter 5 talks about the layout of the design. The simulation results are given in Chapter 6. The static and dynamic testing of the DAC is discussed in Chapter 7. Conclusions are given in Chapter 8.

CHAPTER 2

GENERAL INTRODUCTION TO CURRENT STEERING DACs

Current steering DACs are based on an array of matched current sources which are switched to the output depending on the input digital code. They are implemented using three architectures namely - Binary weighed, Thermometer coded and Segmented.

2.1 BINARY-WEIGHED ARCHITECTURE

In the binary-weighed architecture, every bit controls a current source twice as large as the next least significant bit. So in an N-bit binary-weighed DAC, there will be N binary weighed current sources carrying 1LSB to 2^{N-1} LSB current. The current sources corresponding to the bits which are '1' in the input are switched to the output. A macro-model depicting the binary-weighed DAC is shown in Figure 2.1. The advantage of this

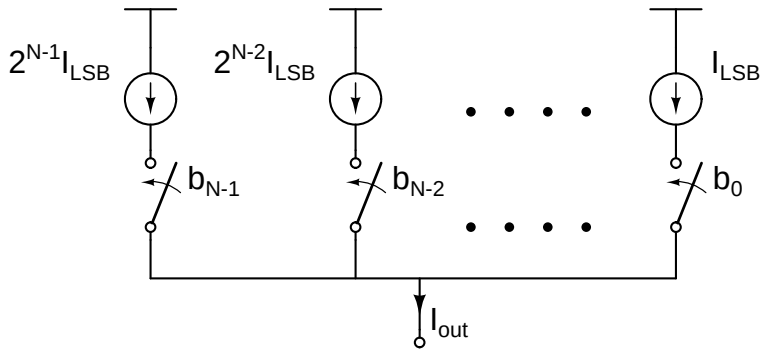

Figure 2.1: Binary-weighed architecture

architecture is the simplicity and reduced area of the digital circuitry, as no decoding

logic is needed. But it suffers from a large differential nonlinearity (DNL) error and an increased dynamic error. At the mid code transition all the current sources are being switched. This results in a large differential nonlinearity error. On the other hand timing mismatches results in a large glitch which greatly affects the dynamic performance.

2.2 THERMOMETER CODED ARCHITECTURE

In the thermometer coded architecture, the binary input is decoded to thermometer code. Each bit in the thermometer code controls a LSB current source. So in a N-bit thermometer-coded DAC, there will be 2^{N-1} current sources each carrying 1LSB current. A macromodel illustrating the thermometer-coded DAC is shown in Figure 2.2. The advantages of this architecture is its better DNL performance and reduced dynamic

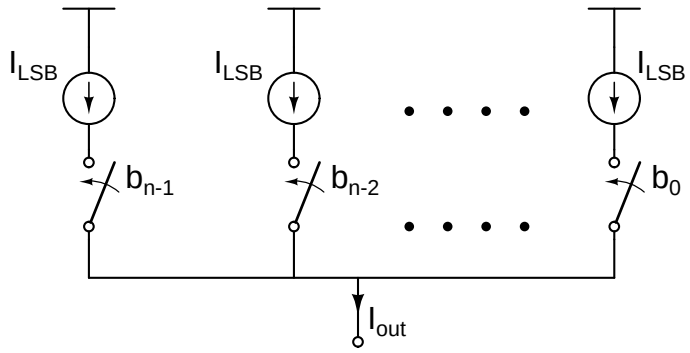

Figure 2.2: Thermometer-coded architecture

errors. Also this architecture guarantees monotonicity. But the problem is the complexity, area and power-consumption of the thermometer decoder.

2.3 SEGMENTED ARCHITECTURE

To leverage the advantages of the above architectures, current steering DACs are implemented using the segmented architecture. In this architecture, certain number of LSBs are binary-weighed and the remaining bits are thermometer coded. The segmentation is done so as to optimize the area for the given static linearity specifications.

2.4 STATIC NON-LINEARITY

There are two types of static non-linearity associated with DACs namely - Integral nonlinearity (INL) and Differential non-linearity (DNL).

2.4.1 Integral Nonlinearity (INL)

INL of a DAC is the deviation of the actual transfer function from a straight line. The straight line is constructed from the actual response using end-point or straight line fit method. This is done to nullify the gain and offset errors. The maximum INL error of a N-bit thermometer-coded architecture occurs at the final code and is given by the cumulative error of all 2^{N-1} current sources:

$$INL_{max} = \frac{1}{2} \times \sqrt{2^N - 1} \times \sigma_I \tag{2.1}$$

where $\sigma_\mathbf{I}$ is the standard deviation of the current variation in the current cell. The factor half is due to the end-point analysis. Even for a binary weighed DAC the maximum INL will be the same because it only depends on the total current source area.

This suggest that irrespective of the segmentation the maximum INL error is the same and it depends only on the resolution of the DAC.

2.4.2 Differential Nonlinearity (DNL)

DNL error of a DAC is the difference between the measured and ideal output response for successive DAC codes. As in the case of INL, the ideal response is obtained from the measured response using end-point method. The maximum DNL error of a N-bit thermometer-coded DAC is given by,

$$DNL_{max} = \sigma_I \tag{2.2}$$

This is because for every code only one additional current source is switched on. The maximum DNL error of a N-bit binary weighed DAC is given by,

$$DNL_{max} = \sqrt{2^N - 1} \times \sigma_I \tag{2.3}$$

This maximum error occurs at the mid-code transition when the current source controlled by the MSB is switching ON and all the others are switching OFF. Since all the current sources are switching, the DNL error is the cumulative error of all the current sources.

From the above discussion we can conclude that the maximum DNL error is depen-

dent on the segmentation and is given by,

$$DNL_{max} = \sqrt{2^{N_{bin}+1} - 1} \times \sigma_I \tag{2.4}$$

where N_{bin} is the number of bits in the binary section. Also the maximum error occurs at that code where all the current sources in the binary section are switched off and a current source in the thermometer section is switched on.

CHAPTER 3

DESIGN OF THE DAC

The architecture of the segmented DAC that we have designed is shown in Figure 3.1.

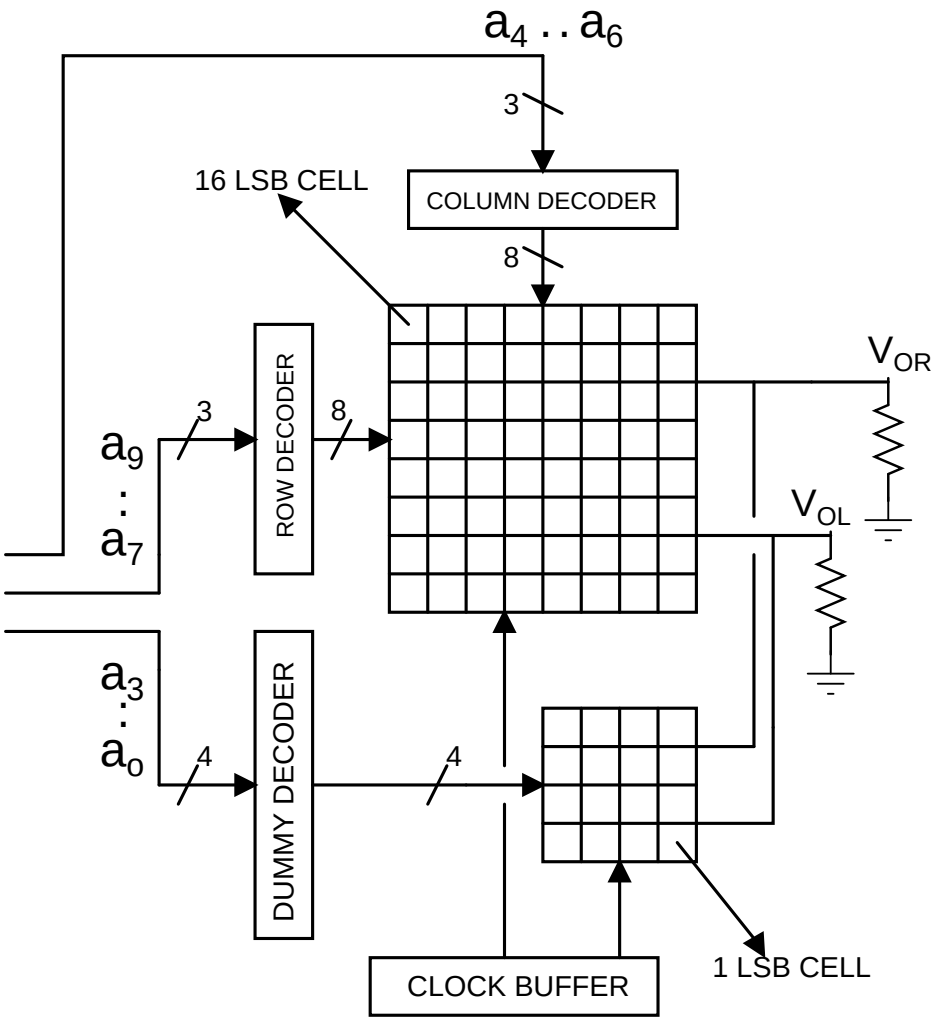

Figure 3.1: Block diagram of the segmented DAC

The segmentation of the DAC that we have designed is (6+4). The reason for this chose of segmentation will be discussed in Section 3.4. The cells in the thermometer section are layed out in a two dimensional manner and decoding of the 6 bits in the

thermometer section is done in two stages. The dummy buffers in the binary section are to compensate for the delay in the thermometer section due to the row and column decoders. The current cells in the binary section are binary weighed from 1 LSB to 8 LSB and that in the thermometer section are 16 LSB each. The various building blocks of the DAC are discussed below.

3.1 CURRENT CELL

The core block of a current steering DAC is the current cell. A typical current cell is illustrated in Figure 3.2.

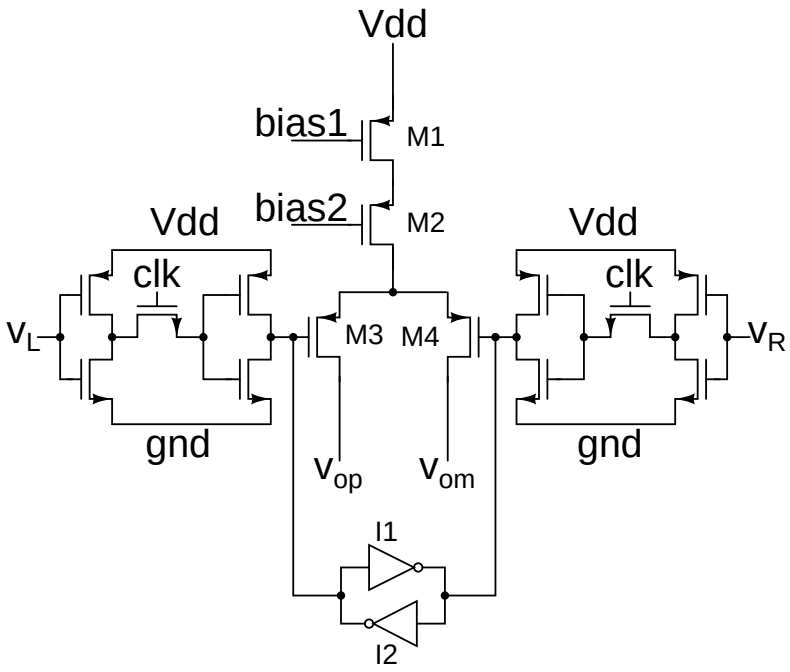

Figure 3.2: Illustration of current cell

The current cell can be split into an analog section and digital section. First let us discuss about the analog section. The analog section consists of -

- The current source

- The switches
- Bias circuit

3.1.1 The Current Source

The current source (M1 & M2) used in the current cell is a cascoded one. M1 is the transistor that determines the current and M2 is the cascode transistor which increases the output impedance of the current source. Since M1 determines the current in a current cell, they must be sized appropriately to reduce static linearity errors due to mismatch.

As already discussed the INL error in a N-bit DAC due to random variation in the currents is,

$$INL_{max} = \frac{1}{2} \times C \times \sqrt{2^N - 1} \times \sigma_I \tag{3.1}$$

where 'C' is the inverse cumulative normal distribution of (0.5+$\frac{inl_yield}{2}$).

For a 10-bit DAC,

$$INL_{max} \quad = \quad \frac{1023}{2} \times C \times \sigma_I \quad \simeq \quad 16 \times C \times \sigma_I \tag{3.2}$$

The INL depends only on the resolution of the DAC and is independent of the segmentation. So we can use this expression to determine the dimensions of transistor M3, even though we don't have knowledge of the percentage of segmentation at the beginning of the design phase.

Since we want to keep the INL error within 0.5 LSB,

$$0.5I = 16 \times C \times \sigma_I \tag{3.3}$$

For the targeted INL yield of 99.7% the value of C is 3.2. So rearranging the

above equation we get an expression for the relative standard deviation of the current as,

$$\frac{\sigma_I}{I} = \frac{0.5}{16 \times C} = \frac{0.5}{51.2} \tag{3.4}$$

The relative standard deviation of the current is a function of the standard deviation of the threshold voltage (σ_{VT}) and the standard deviation of the β (σ_β) of the transistor.

$$\frac{\sigma_{\mathbf{I}}^2}{I^2} = \frac{4\sigma_{VT}^2}{V_{OD}^2} + \frac{\sigma_\beta^2}{\beta^2} = \frac{4A_{VT}^2}{V_{OD}^2(W \times L)} + \frac{A_\beta^2}{(W \times L)} \tag{3.5}$$

Here 'A_{VT}' and 'A_β' are process parameters, 'V_{OD}' is the overdrive and (W $\times$ L) is the area of M1. From the square law equation for current in a MOSFET, we can get a expression for the aspect ratio ($\frac{W}{L}$) of M1. So solving these two equations we can get the dimensions of transistor M1.

The cascode transistor (M2) is sized such that its overdrive voltage is sufficiently enough to keep it in saturation with the available headroom between the supply and the source voltage at the switches. The length of M2 is made minimum and the width is determined from the current it needs to carry and its overdrive voltage.

3.1.2 The Switches

The switches (M3 & M4) must be made as small as possible to

- Minimize the parasitic capacitance which deteriorates the dynamic behavior.
- Minimize the loading on the synchronized driver.

3.1.3 Effect Of Finite Output Impedance

The DC output impedance of the current cell must be made as large as possible so that its influence on the INL of the DAC is negligible. In our case we must ensure that the INL contribution due to finite output impedance is much less than 0.5 LSB. The relationship between the output impedance and the INL of the DAC is given by (B.Razavi (1995)),

$$INL = \frac{I_{unit} R_L^2 N^2}{4 R_{imp}} \tag{3.6}$$

In our case the DC output impedance of the LSB current cell is given by $g_{msw} r_{Osw} g_{mcas} r_{Ocas} r_{Ocs}$. On substituting the corresponding values we get R_{imp} to be 1.5GΩ. The INL contribution due to such a high R_{imp} is much less than 0.5 LSB.

3.1.4 Biasing Circuit

The biasing setup is shown in Figure 3.3.

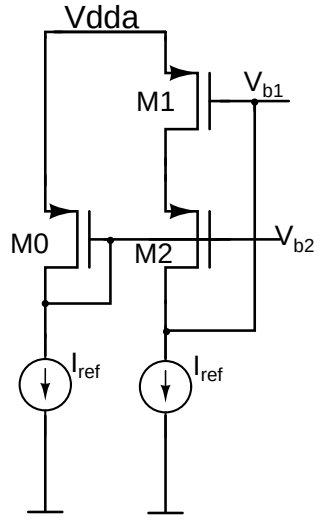

Figure 3.3: The bias circuit

The bias current (I_{ref}) is 80μA, which is eight times the LSB current. Hence M1 and M2 are sized eight times that of the current source transistors. Since I_{ref} is

fixed and the dimension of M1 is known, V_{b1} can be calculated. The bias voltage V_{b2} depends on the dimension of M0, and is constrained by the need to keep M3 and M4 in saturation. For M3 to be in saturation,

$$V_{b2} \quad \leq \quad V_{b1} + V_{t(M3)} - V_{GS(M4)} \tag{3.7}$$

For M4 to be in saturation,

$$V_{b2} \quad \geq \quad V_{GS(M5,M6)} - V_{t(M4)} \tag{3.8}$$

So V_{b2} must be chosen so as to satisfy the above two equations. Once V_{b2} is determined the dimension of M0 can be calculated.

3.2 SYNCHRONIZED DRIVER

The synchronized driver forms the digital section of a current cell. It helps in the synchronization of the control signals to the switches. Apart from synchronizing the control signals, it adjusts the rise and fall times of the control signals so that neither of the switches are switched off at the same time.

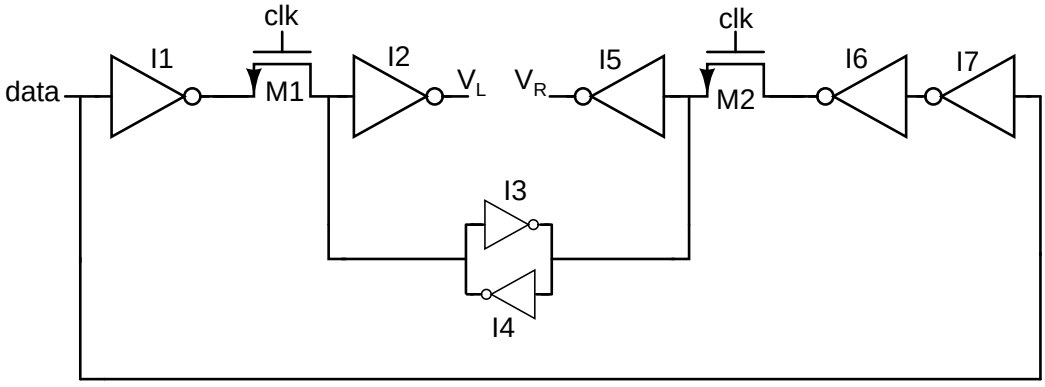

Figure 3.4: Schematic of synchronized driver

The schematic of the synchronized driver that we have used is shown in Figure 3.4.

3.2.1 I1/I6/I7

Inverters I1, I6 and I7 are used as buffers. The extra inverter in the right branch is to generate the complementary signal. There are no special constraints in designing these inverters except that they must similarly sized.

3.2.2 M1/M2

M1 and M2 are NMOS transistors which serve as switches to synchronize the complementary signals. The gate of the transistors are connected to the global clock signal. They must have the same sizes to maintain the symmetry. Their lengths must be kept minimal to decrease the ON resistance of the switches. Increasing the width decreases the resistance but loads the clock buffers which drive the switches. So we must settle with some sort of optimal width.

3.2.3 I3/I4

The cross-coupled inverters I3 and I4 serve two purposes -

- To synchronize the complementary signals.
- To pull the HIGH output of the switches to V_{dd}.
- To reduce clock feed-through due to 'clk'.

When the switches have to pass a logic '1' signal, the output settles at (V_{dd} - V_t). The cross-coupled inverters help in pulling the output voltage from (V_{dd} - V_t) to V_{dd}. Also whenever the clock goes low, the output voltage shifts down depending on the ratio of the C_{gd} of the switch to the output capacitance.

3.2.4 I2/I5

The cross-point of the control signals at the output of inverters I2 and I5 affects the dynamic performance of the current cell. This is because, when the cross-point is high both the differential switches are switched off simultaneously and

vice-versa. When both switches are switched off, the drain node of the cascode transistor rises and thereby pushing it into linear region. This deteriorates the dynamic performance of the cell. This effect is illustrated by simulation in Figure 3.5. The switching takes place at 82 ns. Since both switches are switched off, the drain node rises initially and finally settles to the quiescent voltage.

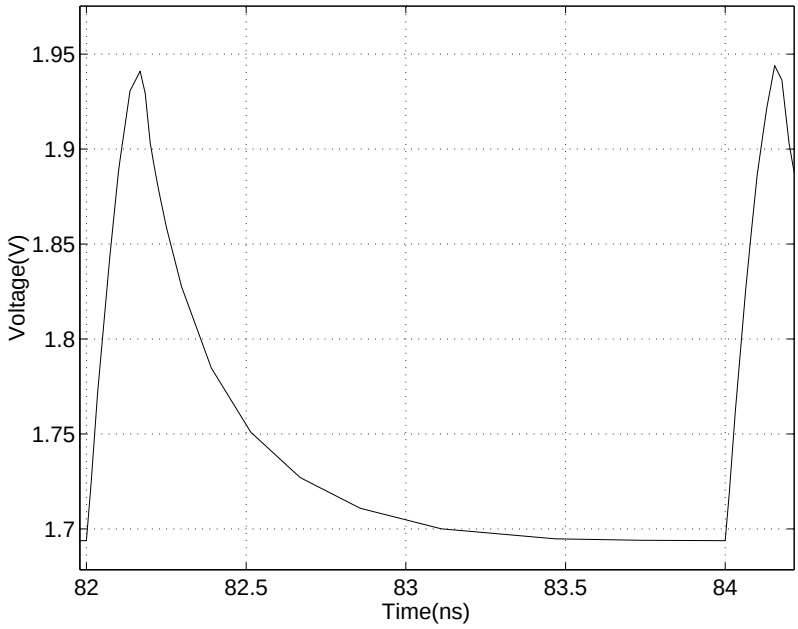

Figure 3.5: Voltage variation at drain of cascode when cross-point is high

To mitigate this, we ensure that either of the switches are always turned on. This is possible by lowering the cross-point of the control signals since the differential switches are PMOS based. In other words the rise time must be large when compared with the fall time. This is done by sizing the inverters I2 and I5 appropriately. The effect of lowering the cross-point is shown in Figure 3.6. The voltage variation is around 60mV in this case, whereas in the previous case it is around 250mV.

So in the above two sections we have discussed about the important points to be kept in mind while designing the current cell. Once we have designed the current cell for LSB current, we just have to scale the sizes appropriately depending on the current calibration of the cell.

3.3 ROW-COLUMN DECODING

In a segmented DAC, the current cells in the thermometer section will be layed out in 2-D arrangement, the reasons for which will be explained later. Now the decoding will be done in two stages -

- In the first stage, two thermometer decoders - called the row decoder and column decoder - decode the binary input.
- In the second stage, the output of the thermometer decoders are decoded by row-column decoding circuits to generate the digital input to the synchronized drivers. These row-column decoding circuits are presently locally within every current cell.

3.3.1 Thermometer Decoder

The thermometer decoder takes a n-bit binary input and gives (2^n-1)-bit output. The input-output relationship for a 3-bit thermometer decoder is shown below.

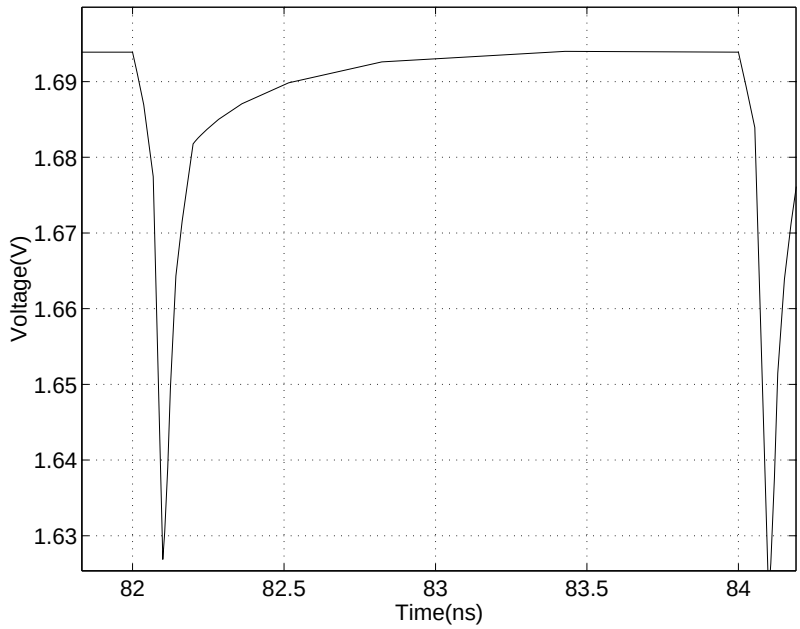

Figure 3.6: Voltage variation at drain of cascode when cross-point is low

Table 3.1: 3-bit thermometer decoder output

I2	I1	I0	Output
0	0	0	0000000
0	0	1	0000001
0	1	0	0000011
0	1	1	0000111
1	0	0	0001111
1	0	1	0011111
1	1	0	0111111
1	1	1	1111111

From the table we can understand that the thermometer code for a binary input contains as many 1's, as the decimal equivalent of the input, starting from the LSB. Also the successive thermometer codes differ only by one bit. This is what gives rise to monotonicity in a thermometer-coded DAC.

3.3.2 Row-Column Decoding Circuit

The row-column decoding circuit is a combinational circuit which decodes the output of the two thermometer decoders to control the current cell.

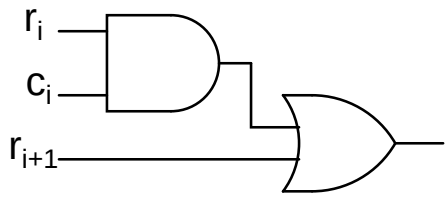

Figure 3.7: Row-column decoding circuit

3.4 OPTIMAL SEGMENTATION

Segmentation is dividing the DAC into two sub-DACs one for MSB's and one for LSB's. The sub-dac containing the MSB's is thermometer coded and the LSB DAC is binary weighed. The steps involved in optimal segmentation are

– Based on the DNL performance alone, the minimum analog area for 100% segmentation is A_{unit} and that for 0% segmentation is $1024 \times A_{unit}$.

– The INL performance is independent of the segmentation.

– If A_{decode} is the required area for the digital decoding logic per current source, then $2^M * A_{decode}$ is the decoding area required if 'M' bits are in the MSB section.

- In our case $A_{unit} = 9.155\mu^2$ and $A_{decode} = 5\mu^2$.

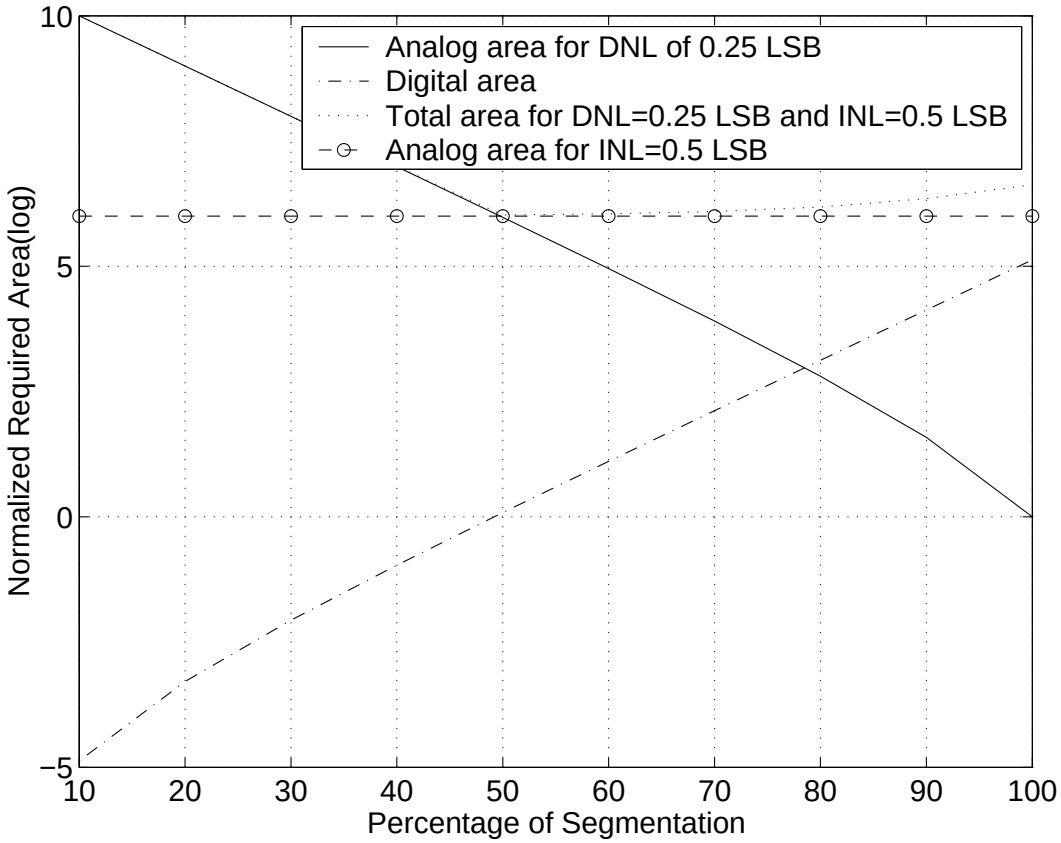

Figure 3.8: Plot of normalized required area versus percentage of segmentation

In the plot shown in Figure 3.8, the variation of analog, digital and total area of the DAC are plotted against the percentage of segmentation.

As the percentage of segmentation increases, the required total area is first dom-

inated by DNL performance, then by INL performance and lastly by decoding area. From the plot we can see that the minimum area is around 50% to 60% segmentation. We go for 60% segmentation because we will be getting a better DNL performance. Therefore the 6 MSB's are thermometer coded and the 4 LSB's are binary weighed.Since more accuracy is required in the MSB's, they are thermometer coded as this will reduce the glitches in MSB transitions.

3.5 LVDS RECEIVER

LVDS stands for Low Voltage Differential Signaling. This is an IEEE standard used for transmission and reception of high frequency signals. Since the digital input to our DAC keeps switching at very high frequencies, we use on-chip LVDS receivers. These LVDS receivers will receive data in the LVDS format and convert them to CMOS levels. We have a LVDS receiver for each bit and the input to each LVDS receiver is differential.

The block diagram of LVDS transceiver is shown in Figure 3.9. The output of a LVDS transmitter is differential current. So we have a termination resistor at the input of the receiver to convert the current to voltage.

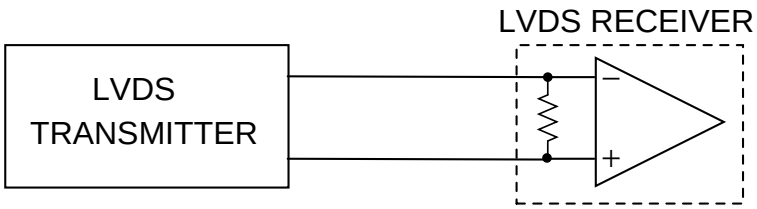

Figure 3.9: Block diagram of LVDS system

The schematic of the LVDS receiver that we have used on our chip is shown in Fig-

ure 3.10.

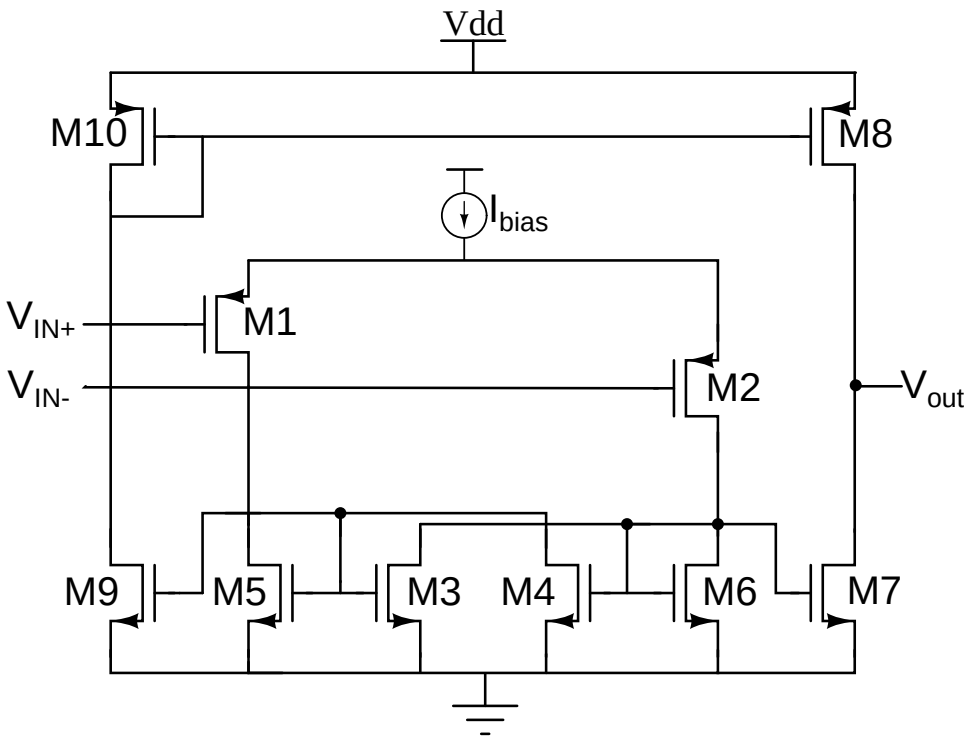

Figure 3.10: Schematic of LVDS receiver

- The transistors M1 to M6 function as Schmitt trigger.
- The transistors M5 and M6 are just to provide hysteresis. So their sizes must be small when compared with M3 and M4.
- Full swing CMOS levels are obtained at the output of the inverters M7 and M8.

CHAPTER 4

MODELING OF SEGMENTED CURRENT STEERING DAC'S

In the previous section we had discussed how to segment the DAC so as to optimize the core area. In our case, it turns out that there are 6 bits in the thermometer section and 4 bits in the binary section. Once we have decided the percentage of segmentation, the design of the DAC core is almost over except for the clock buffers and other auxiliary circuits. So the DAC is now ready to be simulated for studying its spurious performance. To be able to do this, we need to simulate the DAC for hundreds of clock cycles. Also these simulations must be run repeatedly to get an insight of the effects of various non-linearities on the spurious performance.

4.1 WHY NEW MODELING TECHNIQUE ?

The current cell has around 25 transistors. So the thermometer section which has 63 cells will contain about 1600 transistors. The simulation time of a schematic increases exponentially with the number of transistors in it. Typically it takes around 400 minutes to simulate the DAC for the minimum time required to get its SFDR performance. Hence running such time consuming simulations iteratively will be a big strain on the design phase.

In order to mitigate this, several macromodeling strategies have been proposed. In

(Andersson and Wikner (2000)) & (Chen and Gielen (2004)), the authors approximately model the behavior of a current switch using linear elements and switches. The DAC, comprising many such elements, is implemented in MATLAB. They apply this technique to investigate the effect of current source output impedance on the SFDR of the DAC. Others use similar techniques to investigate asymmetrical switching errors (Clara *et al.* (2004)) and rise/fall time waveform asymmetry (Andersson and Vesterbacka (2005)). While these macromodeling techniques reduce simulation time, they have several problems listed below.

- Nonlinearity of output impedance and parasitic capacitance cannot be accounted for in simulation, since the switch is modeled using linear elements.
- Effects of switch gate drive are not considered. It is well known that improper design of the switch waveforms can impact DAC performance Mercer (2004).
- The model for the current switch has parameters that must be extracted from a SPICE simulation of the unit current cell. While this is alright during the final analysis of the DAC, it is not useful during design, where several iterations of the drive circuitry might be necessary to optimize power and performance.

From the above considerations, it is seen that there is a need for a DAC macromodel that takes into account switch drive waveforms and nonlinear nature of device parasitics, while requiring a small simulation time. It is also preferable that the designer should not have to go back-and-forth between multiple tools. In this paper, we present a technique that maintains the accuracy of the full transistor level DAC, while drastically reducing simulation time. This is achieved using time varying current-controlled current sources (easily implemented in Verilog-A) to reduce device count in the thermometer portion of the DAC.

4.2 DERIVING A MACROMODEL USING STATE SPACE

A timing diagram of the signals in a current cell is shown in Fig. 4.1. The clock signal, which synchronizes the drives of all the current switches is shown towards the right of the figure. The cell selection logic outputs v_L and v_R are available before clk goes high. v_R is the complement of v_L.

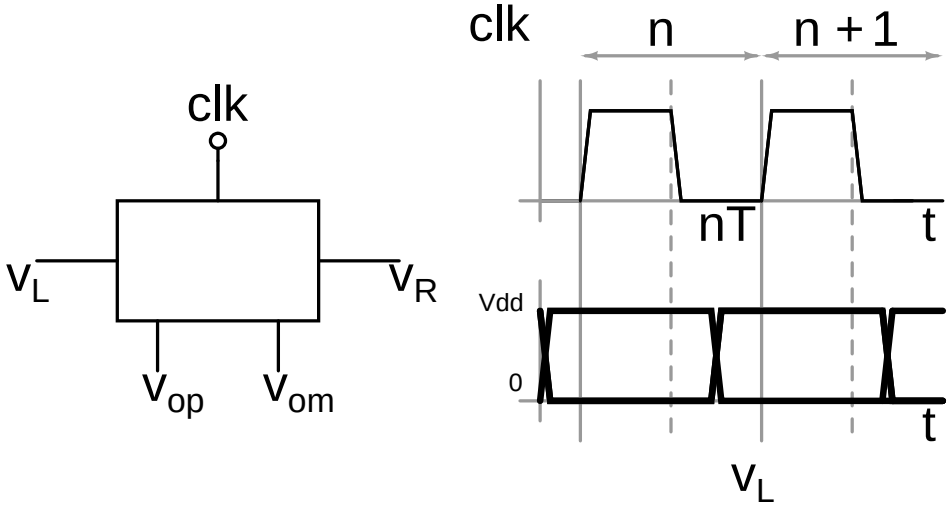

Figure 4.1: Timing of drive waveforms in a current cell. v_R is the complement of v_L.

Within a cycle of clk, any current cell is in one of two states - its tail current is being steered into node v_{om}, which we refer to as the "0" state, or into node v_{op}, which we refer to as the "1" state. The key point to note is that in the k^{th} clk cycle, each of the $2^M - 1$ current cells belongs to one of the following categories:

a. The current cell is in state '0' in clock cycle k, and was in state '0' in clock cycle $k-1$ (Category 00).

b. The current cell is in state '1' in clock cycle k, but was in state '0' in clock cycle $k-1$ (Category 01).

c. The current cell is in state '0' in clock cycle k, but was in state '1' in clock cycle $k-1$ (Category 10).

d. The current cell is in state '1' in clock cycle k, and was in state '1' in clock cycle $k-1$ (Category 11).

Table 4.1: Number if current cells in each category in the $(n+1)^{th}$ clock cycle. The decimal equivalent of the DAC input code in the n^{th} clock cycle is $C(n)$.

Clock cycle	$n+1$
Input Code	$C(n+1)$
Cat. 00	$(2^M-1)-max\{C(n),C(n+1)\}$
Cat. 01	$0,\ if\ C(n+1)<C(n)$ $C(n+1)-C(n)\ otherwise$
Cat. 10	$0,\ if\ C(n+1)>C(n)$ $C(n)-C(n+1)\ otherwise$
Cat. 11	$min\{C(n),C(n+1)\}$

In the discussion to follow, we denote the decimal equivalent of the thermometer DAC input code in the n^{th} clock cycle is denoted as $C(n)$. Table 4.1 shows the number of current sources in each category in the $(n+1)^{th}$ clock cycle.

To derive a simplified macromodel for a thermometer DAC, we first write the differential equations governing the the outputs of the DAC. Let $\mathbf{x}$ denote the vector of all MOSFET terminal voltages in a current cell, except v_{op} and v_{om}. Further, let $\mathbf{v}$ be $[v_{op}\ v_{om}]^T$. Note that $\mathbf{x}$ includes the drive waveforms v_L & v_R, clk and bias/supply voltages. Since transistor currents can be expressed in terms of terminal voltages and their derivatives, the output currents in each of the legs of the current cell can be written in the following form :

$$i_L(t) = f_L(\mathbf{x}, \dot{\mathbf{x}}, \mathbf{v}, \dot{\mathbf{v}}) \tag{4.1}$$

$$i_R(t) = f_R(\mathbf{x}, \dot{\mathbf{x}}, \mathbf{v}, \dot{\mathbf{v}}) \tag{4.2}$$

There are fundamentally four different types of current cells (00, 01, 10 & 11). We use use $\mathbf{x_{kl}}$ to denote the column vector of terminal voltages in the current cell of type "kl". $\mathbf{v}$ is common to all the cells. To determine $v_{op}(t)$, we proceed as follows. Without

loss of generality, we consider the case $C(n+1) > C(n)$. Further, let $C(n) = C(n-1)$. This means that in the n^{th} clock cycle, every current cell belongs to the "00" or "11" categories. Referring to the timing diagram of Fig. 4.1, the internal voltages in all cells of the same type are identical at $t = nT$. For every cell, v_L and v_R settle before the rising edge of clk - hence all current switches in cells of the same type will have the same waveforms. Thus, the differential equation for $v_{op}(t)$ in the $(n+1)^{th}$ clock cycle (the time interval $nT \leq t < (n+1)T$) can be written as

$$\begin{aligned}(1/R)v_{op}(t) &= \{2^M - 1 - C(n+1)\}f_L(\mathbf{x}_{00}, \dot{\mathbf{x}}_{00}, \mathbf{v}, \dot{\mathbf{v}}) \\ &+ \{C(n+1) - C(n)\}f_L(\mathbf{x}_{01}, \dot{\mathbf{x}}_{01}, \mathbf{v}, \dot{\mathbf{v}}) \\ &+ \{0\}f_L(\mathbf{x}_{10}, \dot{\mathbf{x}}_{10}, \mathbf{v}, \dot{\mathbf{v}}) \\ &+ \{C(n)\}f_L(\mathbf{x}_{11}, \dot{\mathbf{x}}_{11}, \mathbf{v}, \dot{\mathbf{v}}) \qquad (4.3)\end{aligned}$$

A similar equation can we written for $v_{om}(t)$. The key observation is that since all current cells of the same type behave in an identical manner, the RHS has only four terms. If v_{op}, v_{om} and $\mathbf{x}$ completely settle at $t = (n+1)T$, an equation similar to (4.3) can be written for the next clock cycle (the time interval $(n+1)T \leq t < (n+2)T$), with the coefficients modified according to $C(n+2)$ and $C(n+1)$. From the RHS of (4.3), we see that the complete thermometer DAC can be implemented by using only 4 basic current cells and time varying current controlled current sources (CCCS).

The four basic current cells (Fig. 4.2) denoted by A, B, C and D operate in the following manner. A is a cell which always remains in the '0' state. This can be implemented by setting $v_R = 0$. Note that v_L is driven by a signal that is the complement of v_R. Similarly, D is a cell which always remains in the '1' state. This can be im-

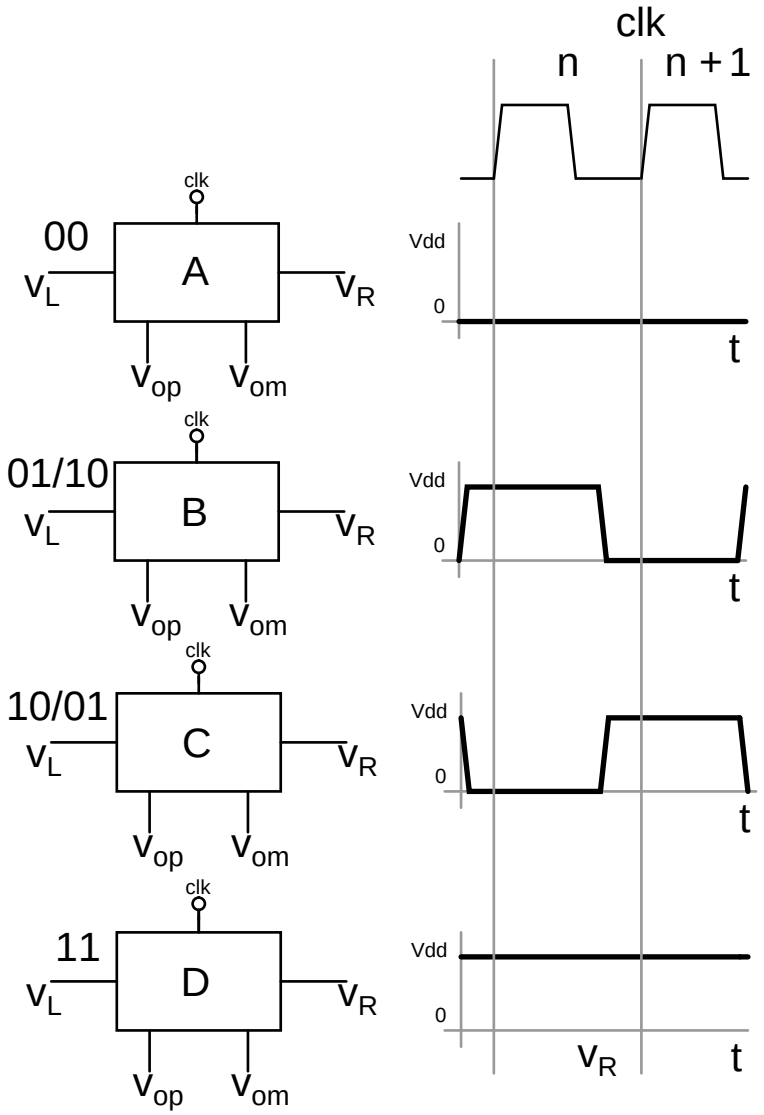

Figure 4.2: The four basic current sources and their drive waveforms.

plemented by setting $v_R = Vdd$. A and D implement the "00" and "11" current cells respectively. B is driven by making v_R a square wave with a frequency $f_s/2$. C is also driven a v_R with frequency $f_s/2$, but offset in time by one clock cycle with respect to v_R of source B, as shown in Fig. 4.2. Further, we observe that B implements a "01" cell in the n^{th} clock cycle and a "10" cell in the $(n+1)^{th}$ cycle, while C implements a "10" cell in the n^{th} clock cycle and a "01" cell in the $(n+1)^{th}$ cycle.

Fig. 4.3 shows a macromodel for the complete thermometer portion of the DAC. It has only 4 current cells (though only two cells are shown to avoid clutter in the

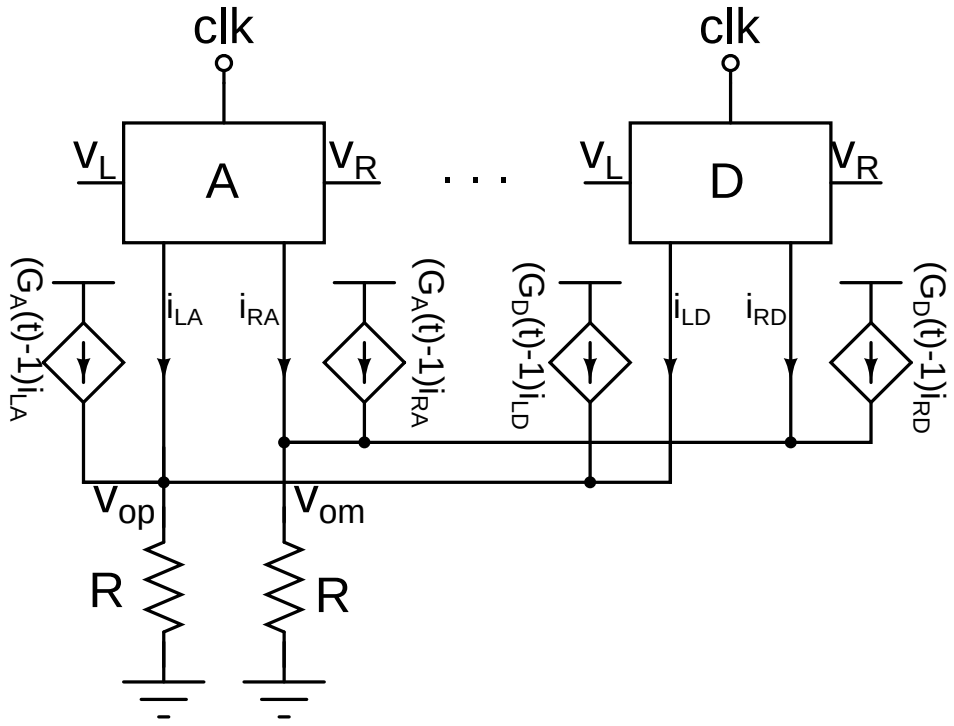

Figure 4.3: Implementation of the thermometer DAC using only four current cells and time-varying CCCS.

diagram), and 8 current controlled current sources, whose gain changes just before the beginning of a clock cycle. These controlled sources are implemented in Verilog-A. For $C(n+1) > C(n)$, the differential equation describing v_{op} in Fig. 4.3 is identical to (4.3) if the CCCS gains are chosen according to the following for $nT \leq t < (n+1)T$:

$$\begin{aligned} G_A &= 2^M - 1 - C(n+1) \\ G_B &= 0 \\ G_C &= C(n+1) - C(n) \\ G_D &= C(n) \end{aligned} \tag{4.4}$$

At the beginning of every clock cycle, the CCCS gains are computed from the DAC input code in the previous and present cycle. An example of the gains as a function of

clock cycle when $C(n+2) > C(n+1) > C(n)$ is given in Tab. 4.2.

Table 4.2: CCCS Gains as a function of clock cycle : $C(n+2) > C(n+1) > C(n)$

Clock cycle	n	n+1	n+2
Code	C(n)	C(n+1)	C(n+2)
G_A	2^M -1 - C(n)	2^M-1 - C(n+1)	2^M -1 - C(n+2)
G_B	0	0	C(n+2) - C(n+1)
G_C	0	C(n+1) - C(n)	0
G_D	C(n)	C(n)	C(n+1)

Since the proposed "macromodel" implements the same differential equations as the complete DAC, second order effects like drive waveforms, nonlinear conductances and capacitances are fully accounted for. It is thus seen that a drastic reduction in simulation time is possible since the number of transistors is reduced by a large factor. Further, no back-and-forthing between multiple tools is necessary.

4.2.1 Glitch Free Switching

One concern with our proposed technique is the likelihood of glitches occurring in the output waveforms whenever the CCCS gains change. In this subsection, we show that glitches can be avoided if timing of the CCCS gains is chosen in the manner shown in Fig. 4.4. As seen earlier, the drive waveform v_L arrives before clk goes high. CCCS gains are updated after v_L has settled, but before clk goes high. To see how this avoids glitches, consider the case where $C(n+1)$ is greater than $C(n)$. Just before the gains change, v_{op} is given by $C(n)RI_{cell}$. Immediately after the gains change, but before clk goes high, the current cells B & C still have the drives corresponding to the n^{th} clock cycle ($i_{LC} = 0$ & $i_{LB} = I_{cell}$). Thus $v_{op} = C(n)RI_{cell}$ until clk rises and glitches are avoided.

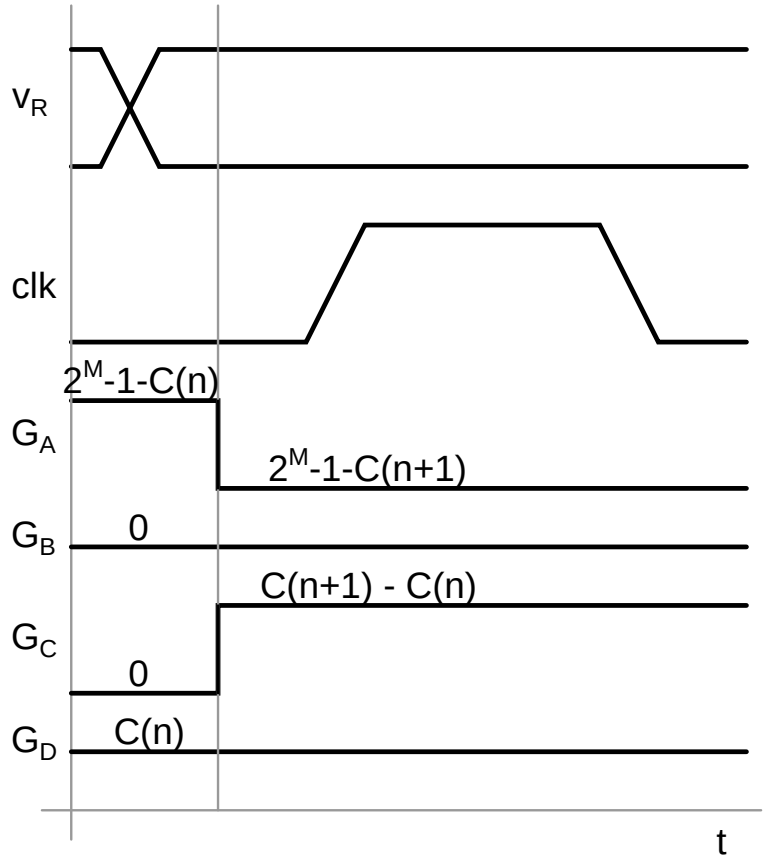

Figure 4.4: Timing of the gain switching CCCS to avoid glitches in the DAC outputs.

4.3 COMPARISON BETWEEN COMPLETE AND MODELED DAC

To compare the complete DAC and the macromodel, both these DAC's were simulated at a sampling frequency of 500 MHz and different input frequencies. In our macromodel, the thermometer DAC was simplified, while the binary DAC was simulated as is. Fig. 4.5 compares a full transistor level simulation at Nyquist frequency, with the macromodelling technique proposed in this work, where the differential output of the DAC is shown. The two outputs are virtually indistinguishable. A closer look (inset) shows the accuracy of our technique - it is seen that nuances of the waveform in the complete schematic are captured. Tab. 4.3 compares the SFDR obtained on the single-ended and differential outputs of the DAC for macromodel and full transistor

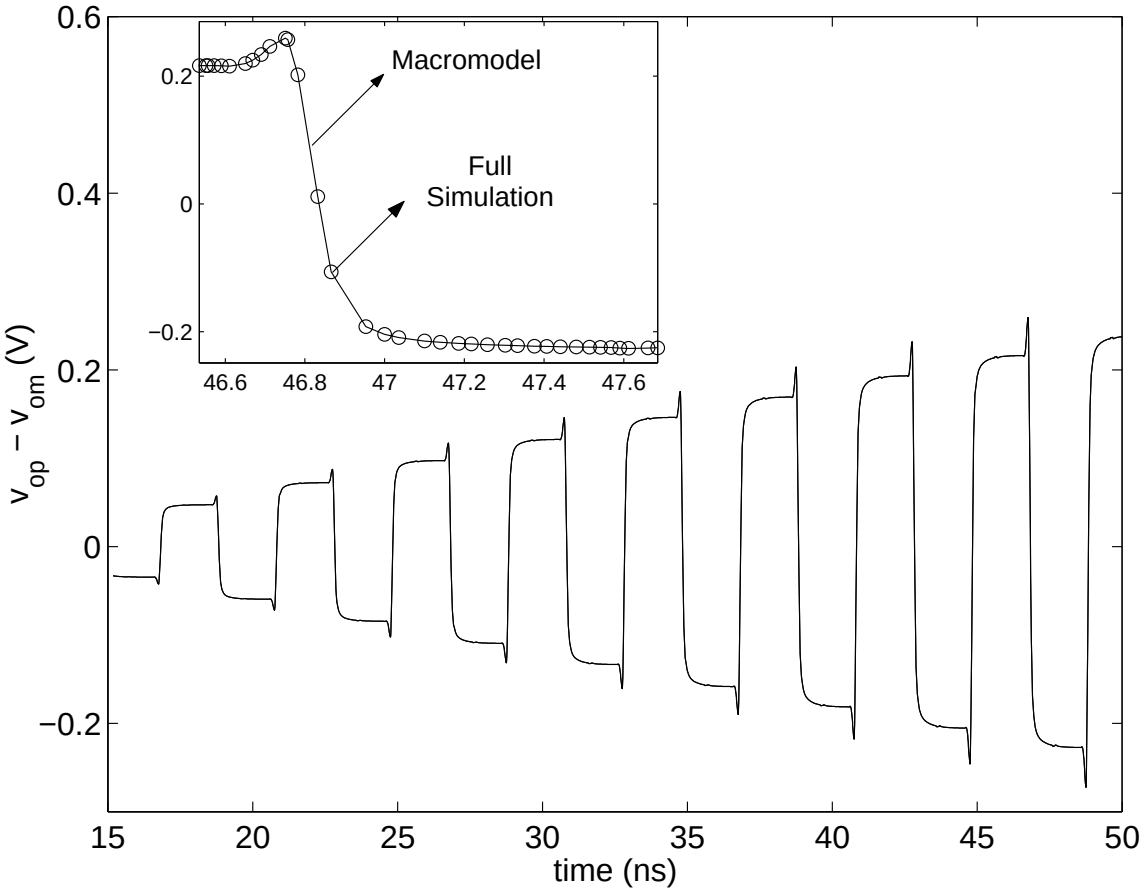

Figure 4.5: Comparison of the differential DAC output for the macromodel & full transistor level schematic : the outputs are indistinguishable. The inset shows the time axis zoomed around 47 ns - (o)-full simulation, (-) macromodel.

level simulation. Excellent agreement is seen.

So we have come up with a new technique to model segmented current steering DAC's, wherein the binary section is retained as it is but the thermometer section is replaced by the proposed macromodel. This model reduces the simulation time by a huge factor and at the same time captures all non-linearities. In the case of our DAC, the simulation time for the complete schematic was 400 minutes for each input frequency. With our technique, simulation time was reduced to 10 minutes. During our entire design phase at schematic level, we used the macromodel to study the spurious performance of the complete DAC.

Table 4.3: SFDR of the waveforms at v_{op} & $(v_{op} - v_{om})$

f_{in}(MHz)	SFDR(dB) Complete DAC v_{op}/v_{op}-v_{om}	SFDR (dB) Macromodel v_{op}/v_{op}-v_{om}
44.921	54.400/68.124	54.401/68.127
80.078	50.253/63.827	50.251/63.820
126.953	48.225/59.568	48.229/59.570
189.453	50.159/57.232	50.165/57.243
248.046	53.190/57.288	53.191/57.295

CHAPTER 5

LAYOUT OF THE DAC

5.1 SYSTEMATIC ERRORS

After the design has been finalized at the schematic level, we move to the layout phase of the DAC. To ensure that the DAC has an accuracy of 10 bits, the current sources must have an error of less than 0.5 LSB. There are two types of errors that can arise in current sources. One is the random errors, which we have already dealt with by suitably sizing the current sources to ensure that INL does not exceed 0.5 LSB. The other source of error is systematic errors which arise due to the linear and quadratic gradients in the chip. The linear gradient arises due to the radial pattern of the oxide thickness, which gives rise to a linear shift in the values of the current sources. On the other hand, quadratic gradients arise due to temperature and stress gradients. So to mitigate these systematic errors, we need to prudently lay out the current cells.

These systematic error sources are 2-D in nature. In the binary weighed section these errors can be easily compensated by selecting the unit current sources associated with each bit in an uniform pattern all over the current source array.

5.2 SYMMETRICAL HIERARCHICAL SWITCHING

In case of the thermometer section, the 6-bit DAC is divided into 4 sub DAC's and these four DAC's are mirrored with respect to the horizontal and vertical axis. Then by

implementing symmetrical switching scheme in both dimensions of each DAC, the linear errors are compensated in each DAC, and because of the spatial symmetry they are completely canceled out in the overall arrangement. Also the switching sequence combined with the 2-D mirroring of the DAC's implements in the overall arrangement a hierarchical symmetrical switching sequence that compensates and averages the quadratic errors. This scheme is illustrated in figure 5.1.

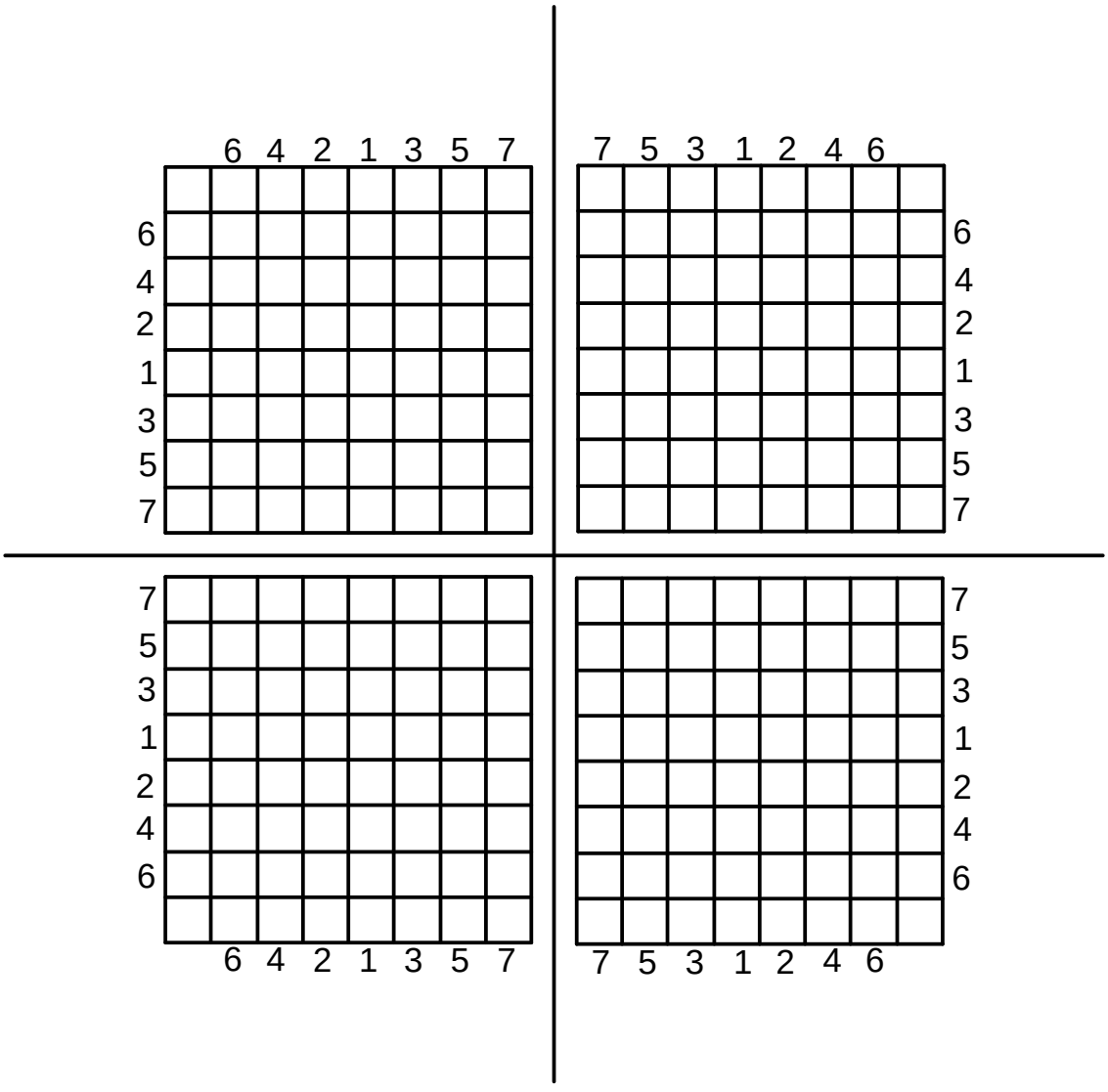

Figure 5.1: 2-D mirrored arrangement and hierarchical symmetrical switching in the 6-bit thermometer section

This scheme however is not enough to compensate systematic errors due to voltage

drop across the ground lines. To compensate this, we need to make the ground lines sufficiently wide so that the resistance of the line is reduced. The layout of the complete DAC is shown in Figure 5.2.

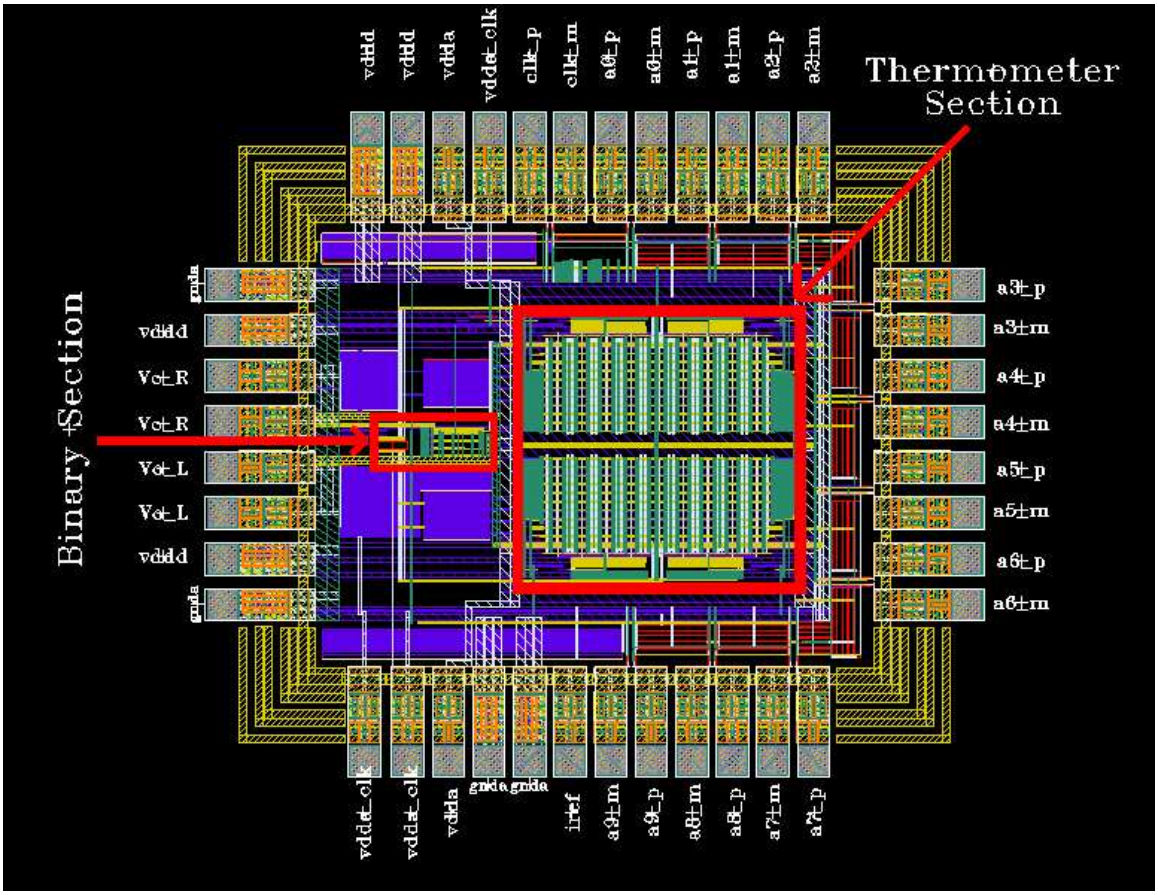

Figure 5.2: Snapshot of the complete layout of the DAC

CHAPTER 6

SIMULATION RESULTS

The simulated time domain output of the full extracted version of the DAC is shown in Figure 6.1. The input frequency is 248.04 MHz and sampling frequency is 500 MHz. The simulation was run in typical corner and at a temperature of 70^{o}C.

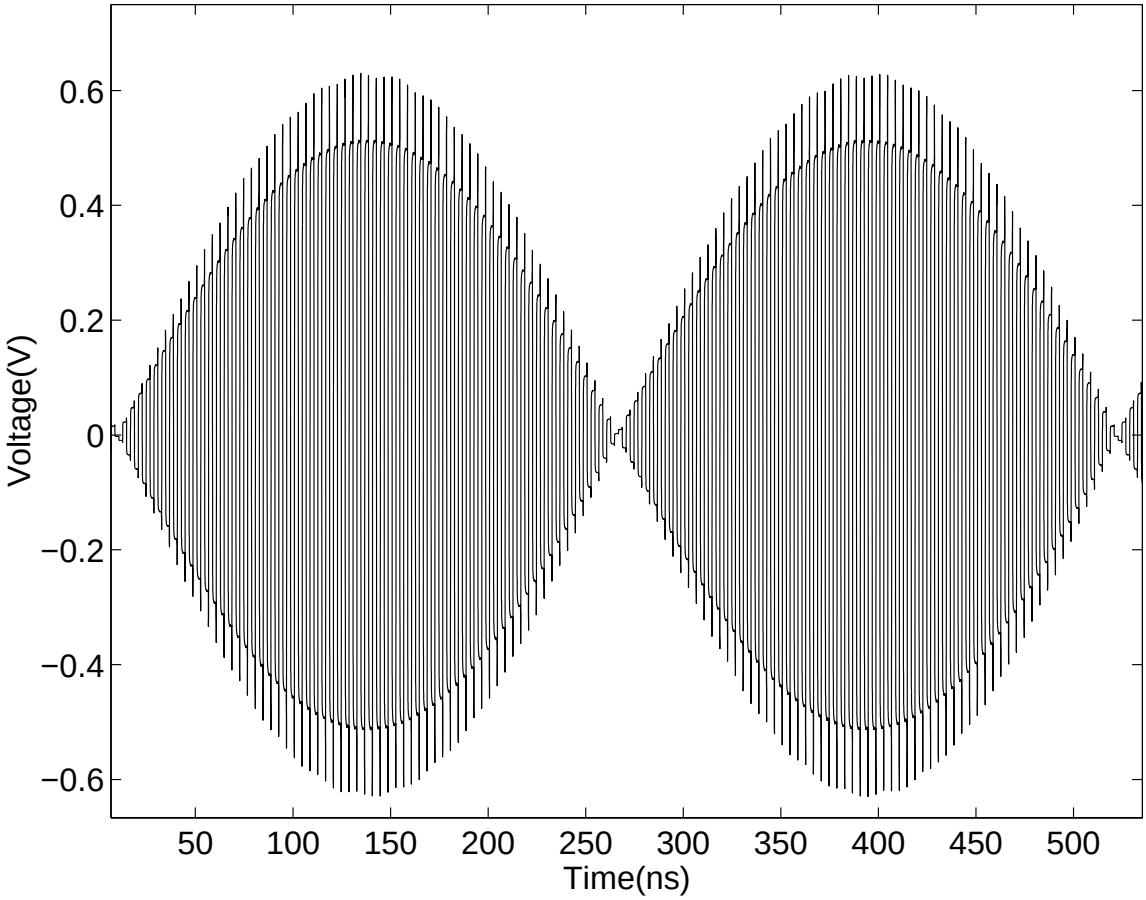

Figure 6.1: Differential output of the DAC

The spectral performance of the DAC for the same test conditions is depicted in Figure 6.2. The SFDR performance is 55.23 dB.

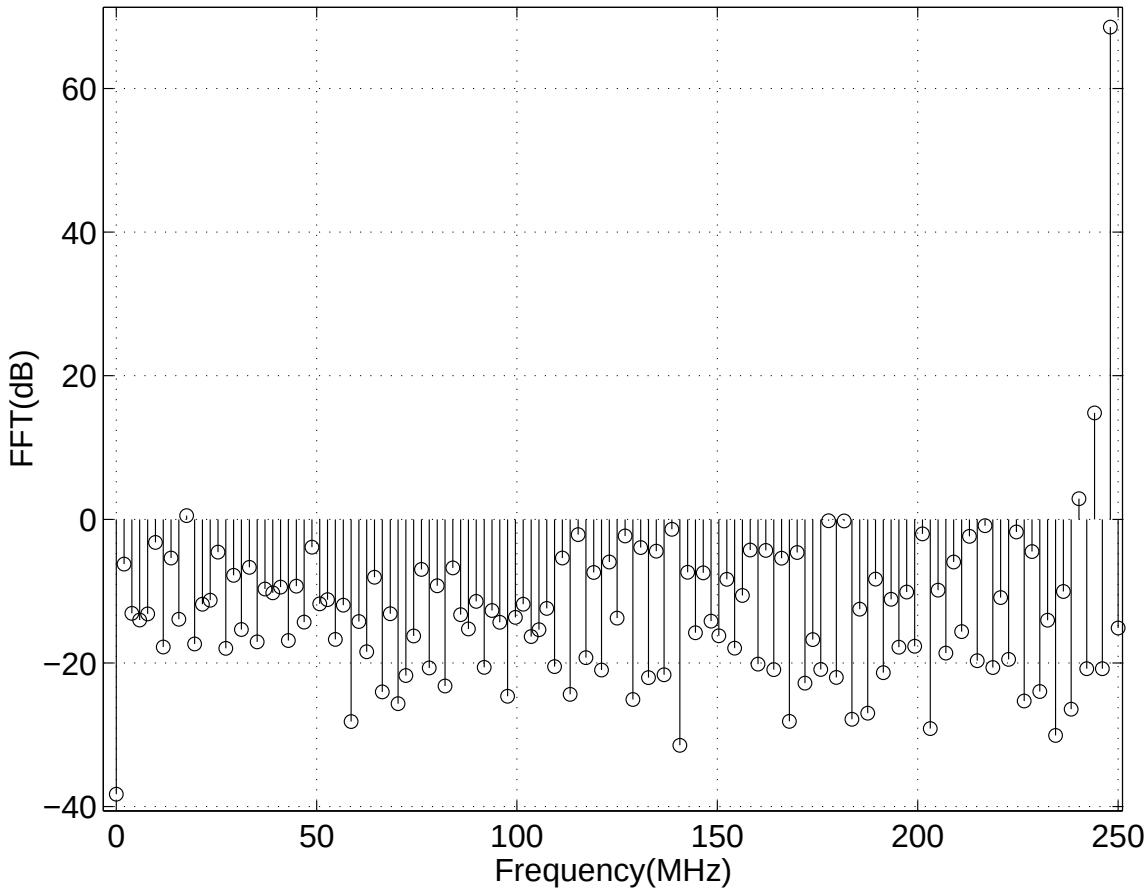

Figure 6.2: FFT of the differential output

The SFDR of the DAC for different corners at a temperature of 70^{o}C and supply of 3.3 V is tabulated in Table 6.1.

Table 6.1: Simulated SFDR of the differential ouptut across corners

Corner	SFDR(dB)
cmostm	55.23
cmosws	52.2
cmoswp	54.81
cmoswo	55.67
cmoswz	52.1

The pin diagram of the chip is shown in Figure 6.3. Pins 1-20 are for the LVDS inputs. Pins 21 and 22 are the LVDS clock input. Pins 29,30,31 and 32 are the differential outputs. The bias current is injected through Pin 40. The remaining pins are supply and ground pins.

The die photograph of the taped out chip is shown in Figure 6.4.

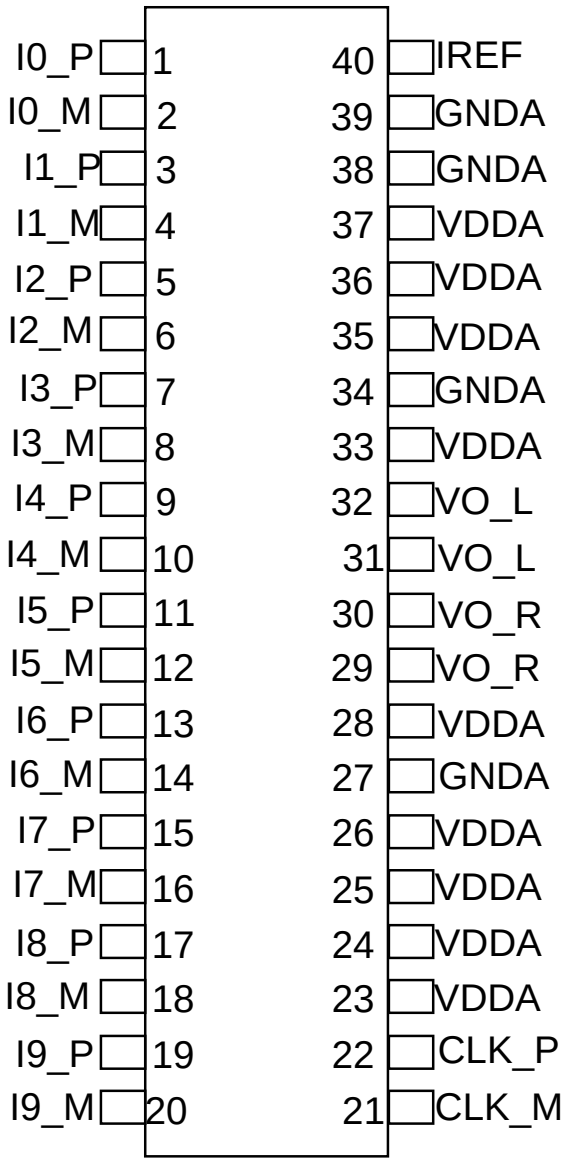

Figure 6.3: Pin diagram of the chip

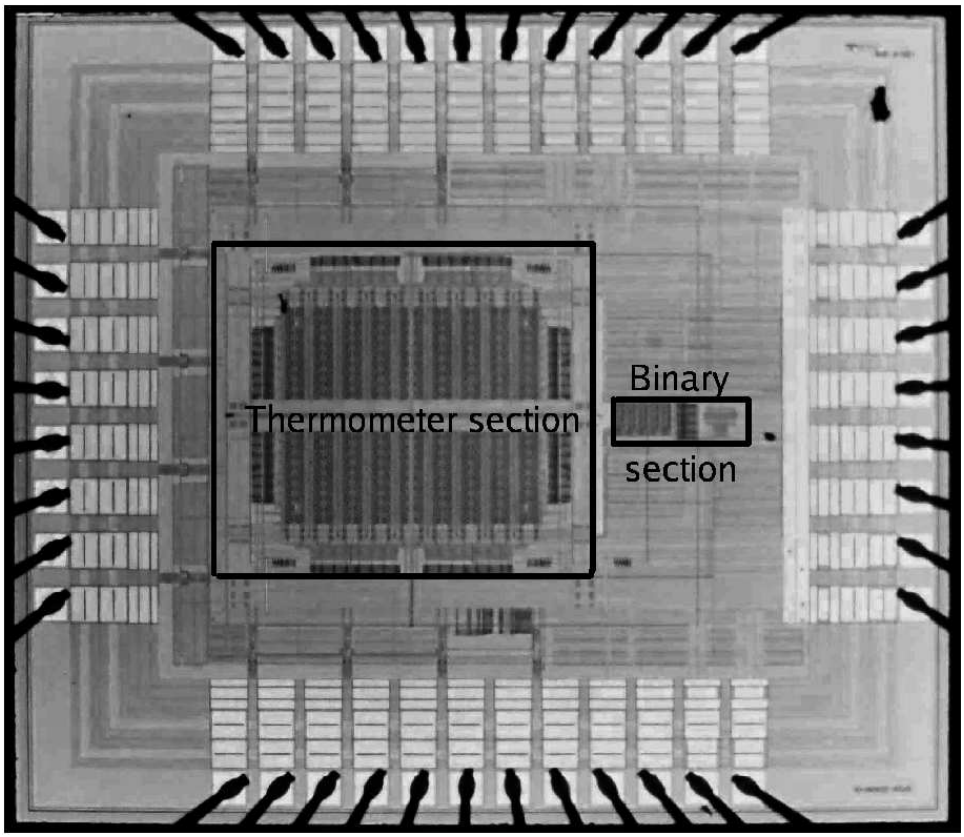

Figure 6.4: Die photograph of the chip

CHAPTER 7

TESTING AND CHARACTERIZATION

7.1 PRINTED CIRCUIT BOARD

To characterize the DAC designed, we need to design a PCB(Printed Circuit Board). This PCB was designed with the help of OrCAD layout software. This was a two layered board and was fabricated through Zeta electronics, Chennai. The dimensions of the board are 4"$\times$5" and the material is FR4 glass epoxy. The thickness of the board is 1.6 mm. A snapshot of the board with all the components populated on it is as shown in Figure 7.1. The thickness of the tracks carrying the digital input and the analog output is made 60 mils so that the characteristic impedance of the track is 50 Ω. This is done to ensure that there is no reflection.

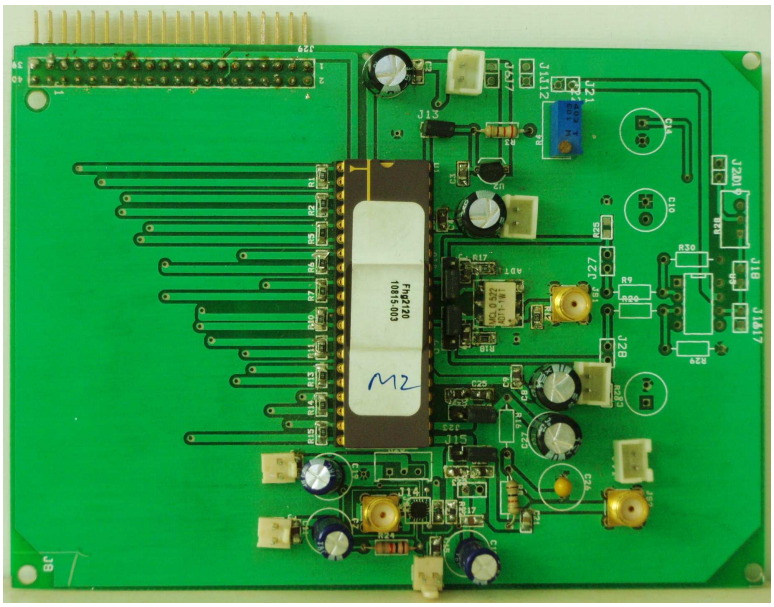

Figure 7.1: Snapshot of the test board

The schematic of the board is shown in Figure 7.2.

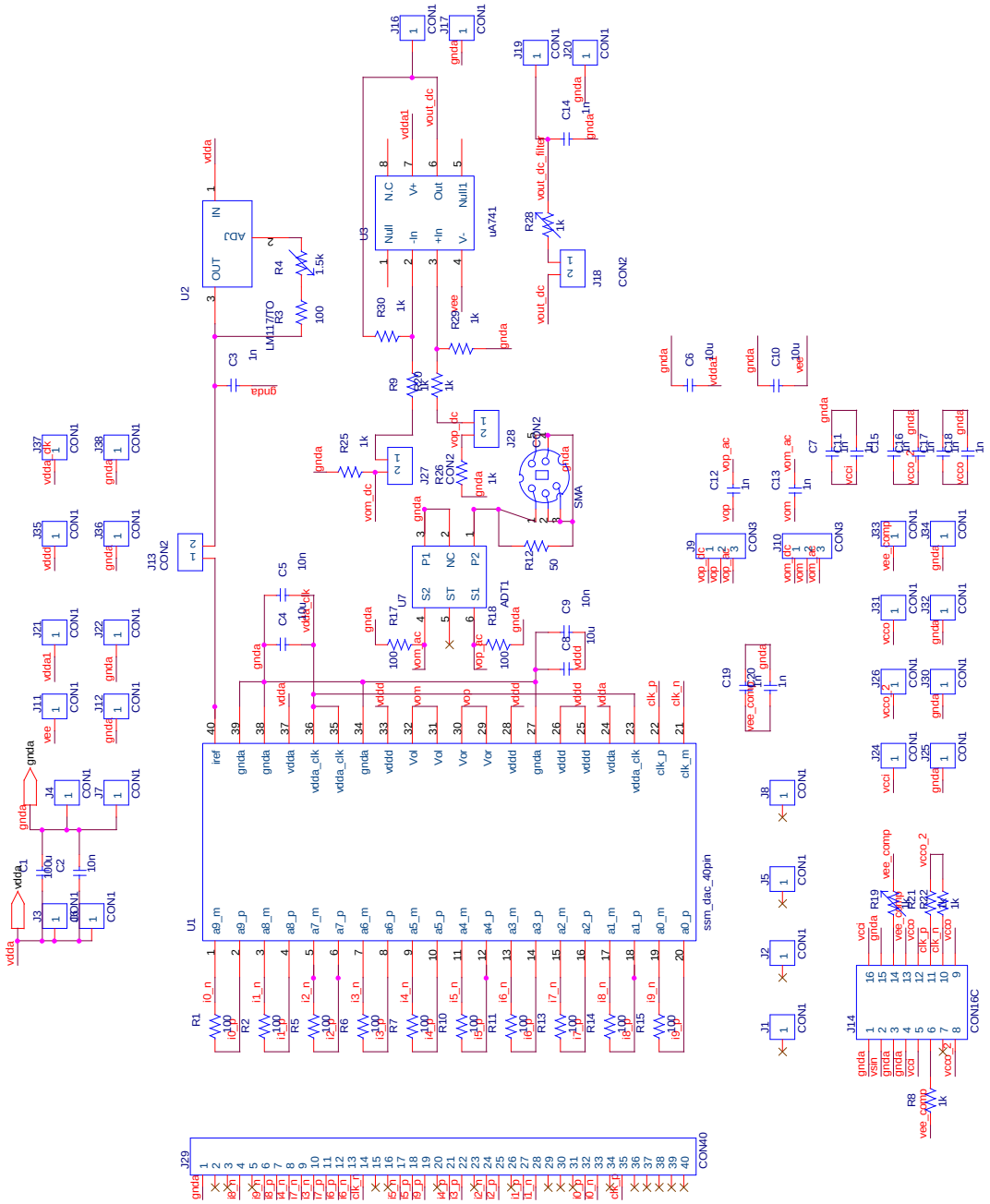

Figure 7.2: Schematic of the PCB

7.2 Quantities generated on the board

The quantities generated on the board are -

- Reference current
- High frequency clock
- Differential to single-ended conversion of DAC output

7.2.1 Reference Current

The bias current needed to generate the bias voltages for the current cell inside the chip has to be feed through pin 40 (seen in Figure 6.3). This constant current is generated on the test board using the chip LM334. Figure 7.3 shows the configuration of the chip so that it can source current.

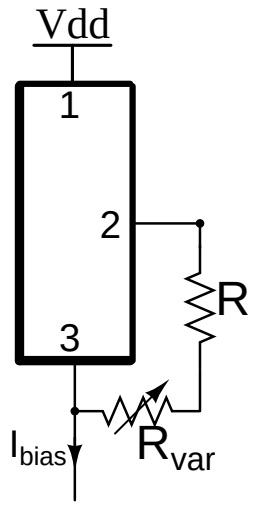

Figure 7.3: LM334 as current source

It is a 3-pin IC. Pin 1 is connected to supply. A fixed resistor and variable resistor are connected in series between Pin 2 and 3. The current I_{bias} sourced by the chip is given by,

$$I_{bias} = \frac{0.68}{R + R_{var}} \tag{7.1}$$

In our case I_{bias} is 80μA, so the total resistance is 8.5 kΩ. The variable resistor is used so that we can change the bias current.

7.2.2 Differential To Single-ended Conversion Of DAC Output

The differential output of the DAC is converted to a single-ended signal using the center tapped transformer ADT1-1WT from minicircuits as shown in Figure 7.4. The differential signals are connected to the secondary of the transformer. The center tapped node and one of the primary terminals is grounded. The output is available at the other primary terminal.

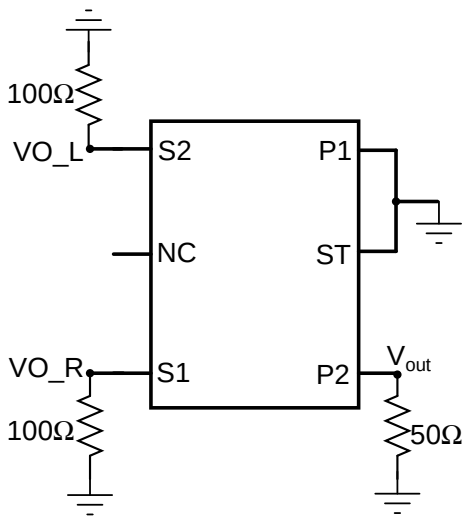

Figure 7.4: ADT1-1WT transformer

7.2.3 High Frequency Clock Generation

To generate the high frequency clock on the board, we convert a sine wave into two complementary clocks using the high speed comparator ADCMP566 from Analog Devices.

7.3 DC CHARACTERIZATION

Now let us move on to the DC performance characterization of the DAC. This involves both INL and DNl performances of the DAC. The test setup for characterizing the DC performance is shown in Figure 7.5. The LVDS inputs to the DAC are generated

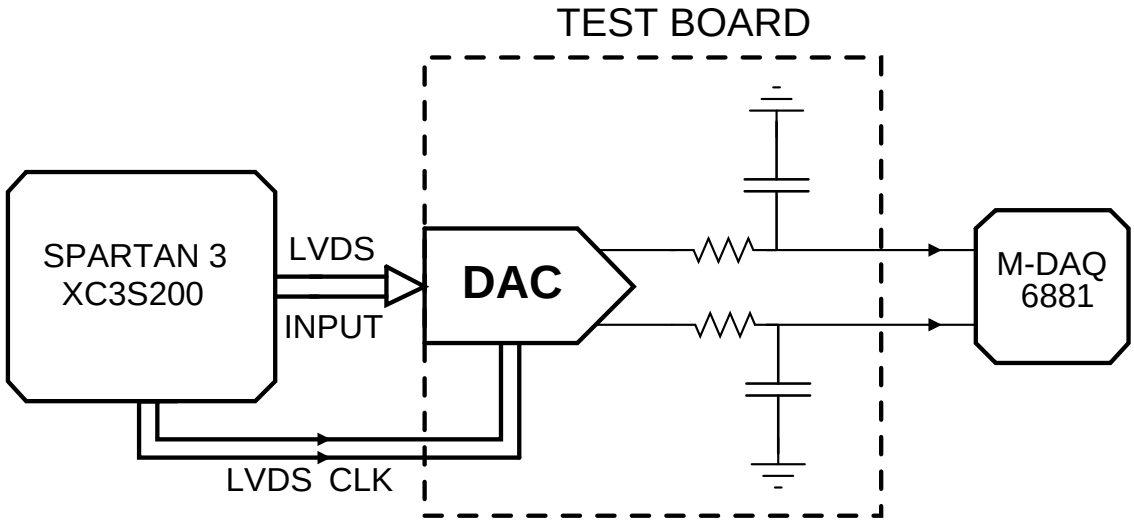

Figure 7.5: Test setup for DC characterization

using the SPARTAN-3 (XC3S200) FPGA from Xilinx. The LVDS clocks for the DAC are also derived from the FPGA. Since we need to find the INL and DNL performance of the DAC, a very low frequency (100 Hz) digital ramp is generated and the DAC is clocked at a much higher frequency of 250 MHz. The output of the DAC is filtered using a simple RC low-pass filter and then sensed by the Data Acquisition card. The

data from the card is taken to MATLAB where we manipulate the data to get the INL and DNL plot.

The INL and DNL characteristics of the tested chip are shown in Figure 7.6 and Figure 7.7 respectively.

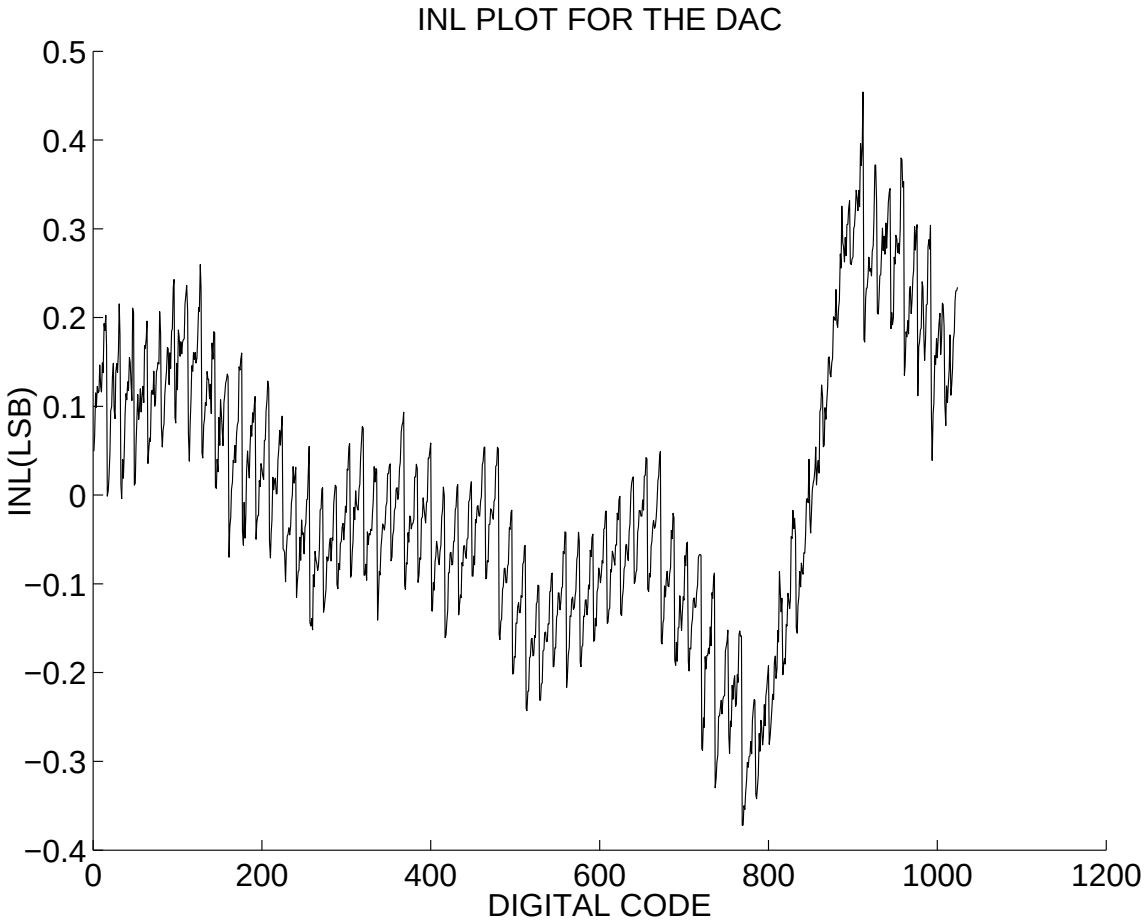

Figure 7.6: INL curve of the DAC

From the plots we can see that the non-linearity is less than 0.5 LSB. So the DAC has a linearity of 10 bits. The spatial distribution of the current in the thermometer section is shown in Figure 7.8

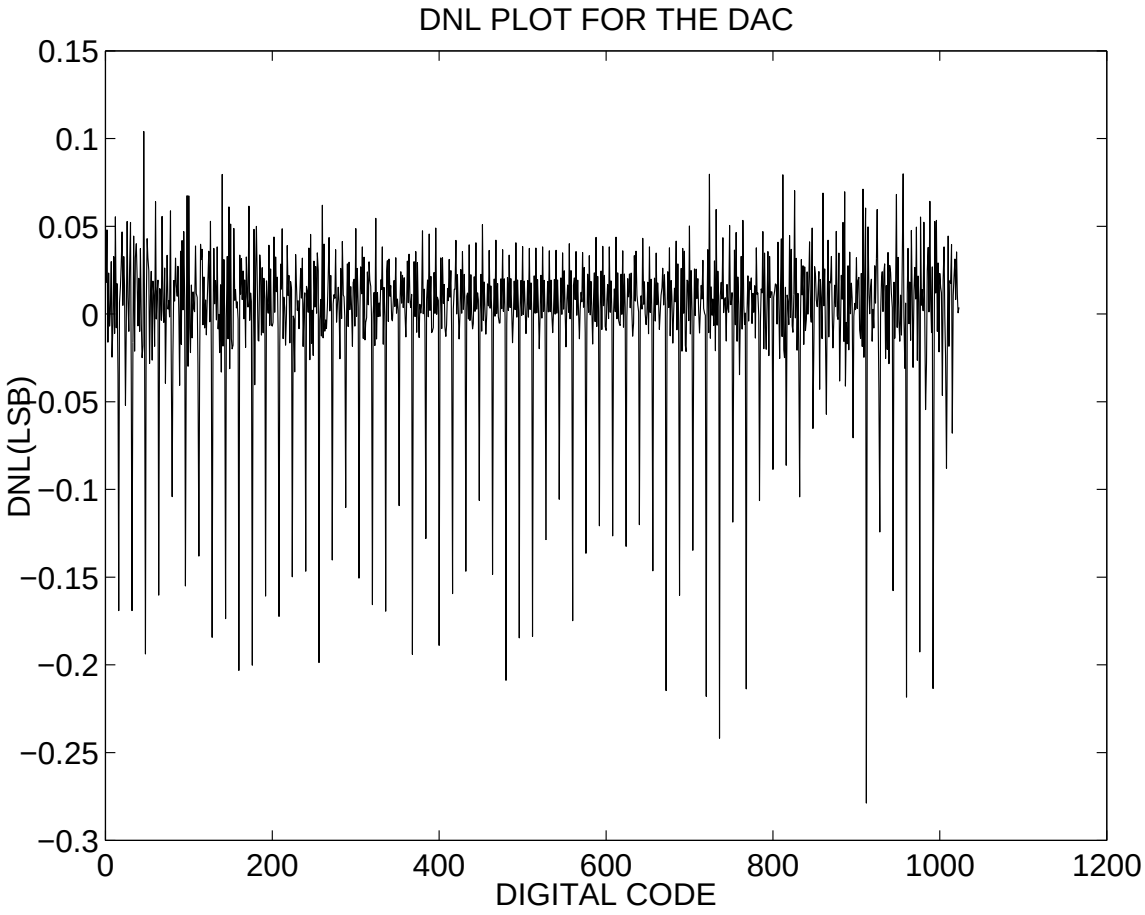

Figure 7.7: DNL curve of the DAC

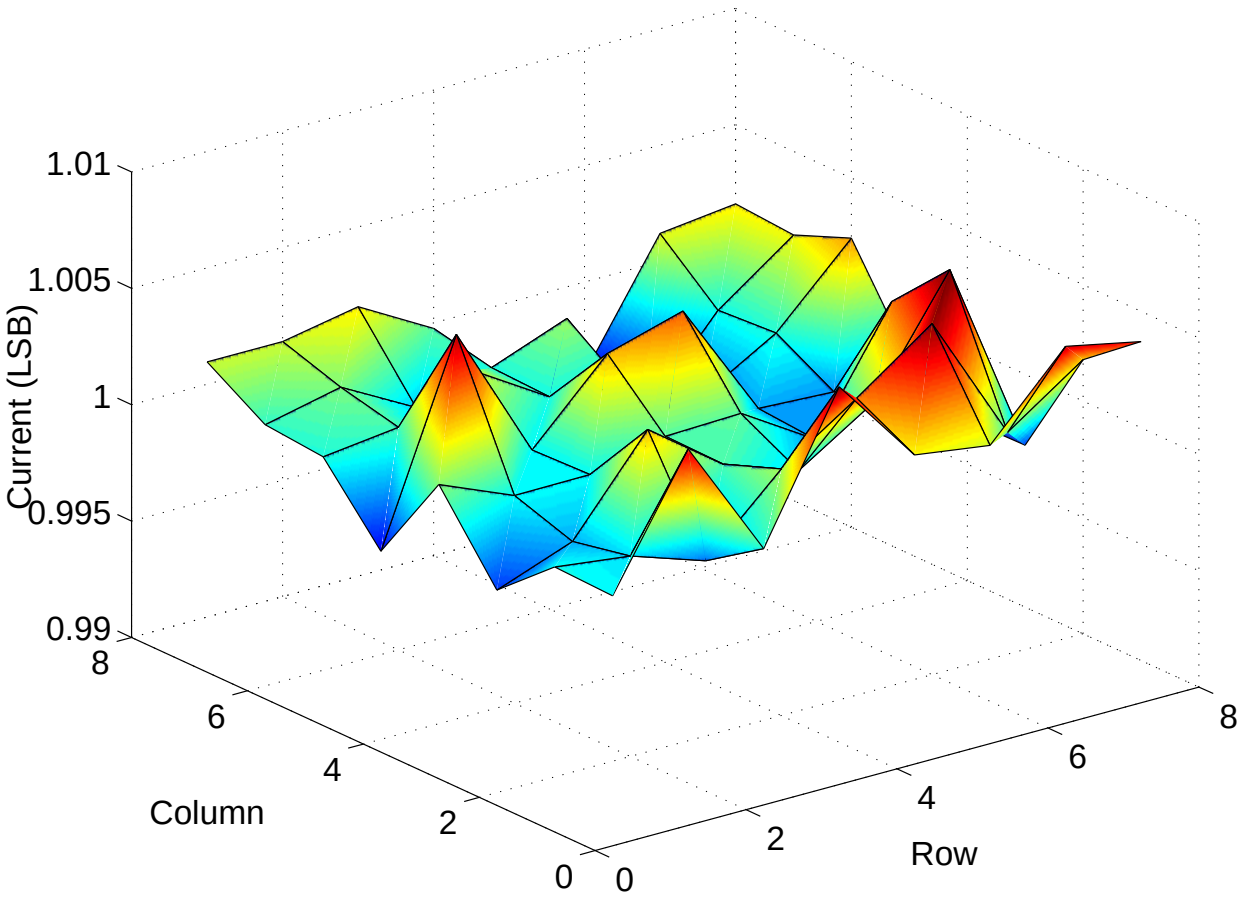

Figure 7.8: Spatial distribution of the currents in the thermometer section

7.4 AC CHARACTERIZATION

The test setup for characterizing the spurious performance of the DAC is shown in Figure 7.9.

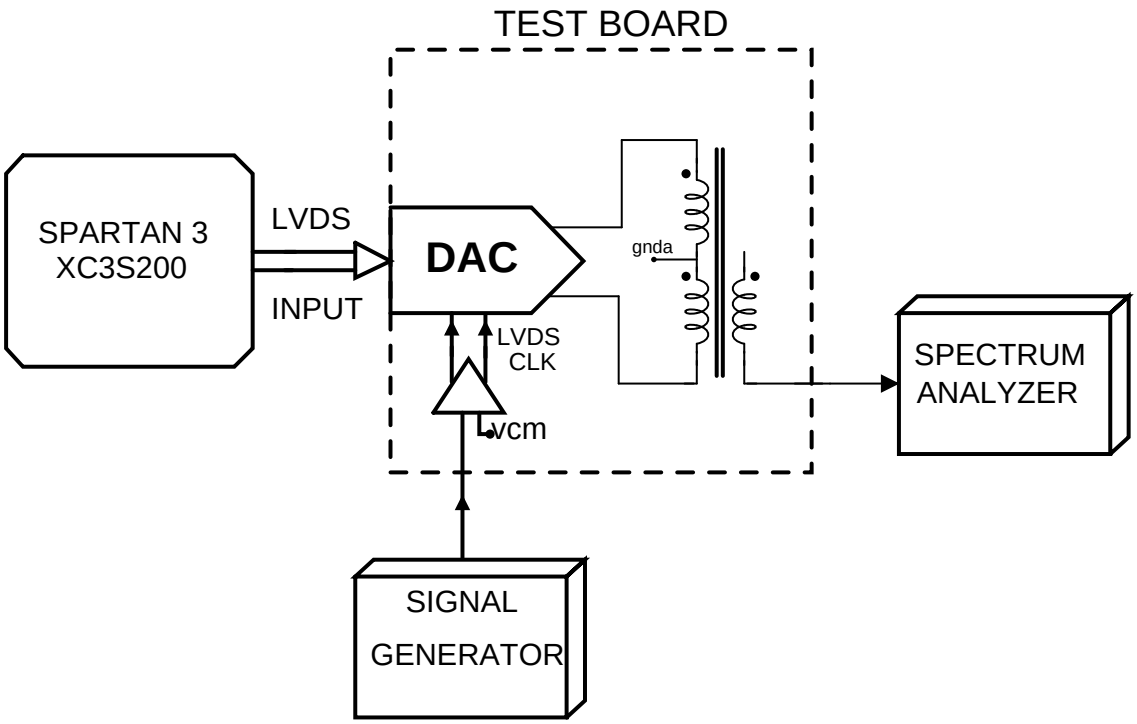

Figure 7.9: Test setup for AC characterization

In this setup, the LVDS clocks for the DAC are generated using a sine wave generator rather than from the FPGA. This is because the quality of the clocks from the FPGA is very poor at high frequencies. The inputs are generated from the FPGA. As discussed already the differential output of the DAC is converted into a single ended-output using a center-tapped transformer with turns ratio of 1:1. The output is then analyzed using a spectrum analyzer to obtain the power spectral density of the output.

First the DAC was tested for sampling frequencies less than 100 MHz. The harmonic distortion for various input frequencies is plotted in Figure 7.10 and Figure 7.11.

From the plots we can see that the HD2 is lesser than HD3. But this is a contradiction because the DAC is a differential system and hence the HD2 must be much less than HD3.

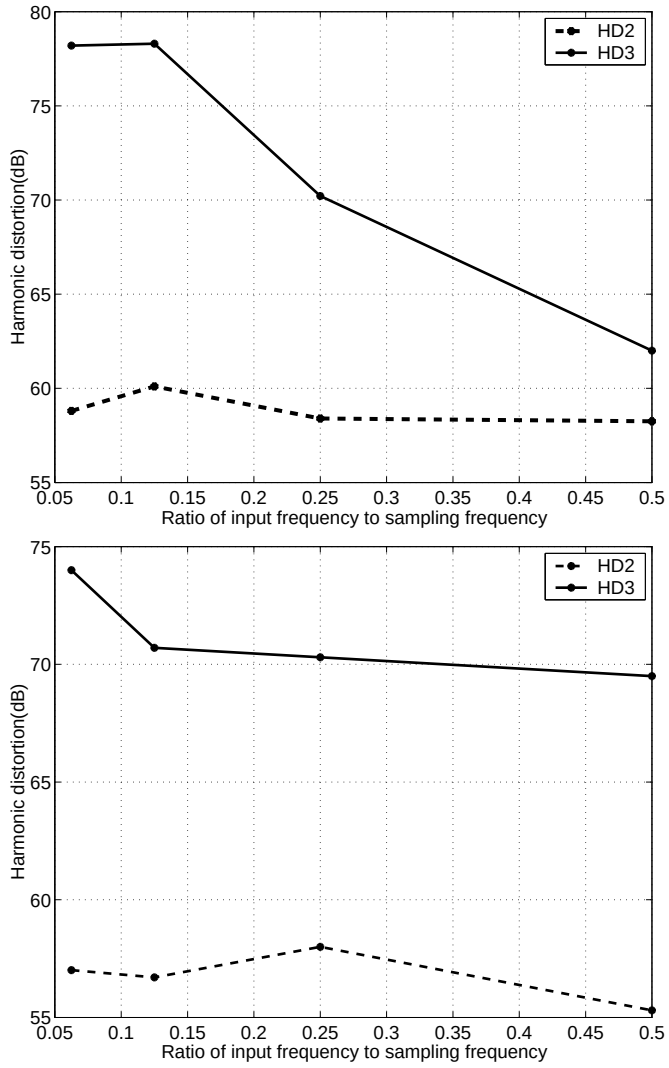

Figure 7.10: Harmonic distortion variation with input frequencies @ sampling frequencies of 32 MHz and 50 MHz

To debug the problem, the macromodel with the current cells extracted was simulated at these sampling frequencies. The SFDR was around 75 dB and HD2 was higher than HD3. But once the VCVS that were used at the bias nodes of the current cell were replaced by capacitances equal to that in the complete layout, there was a degradation in SFDR. Also the HD2 dropped below the HD3, and these values were comparable to that

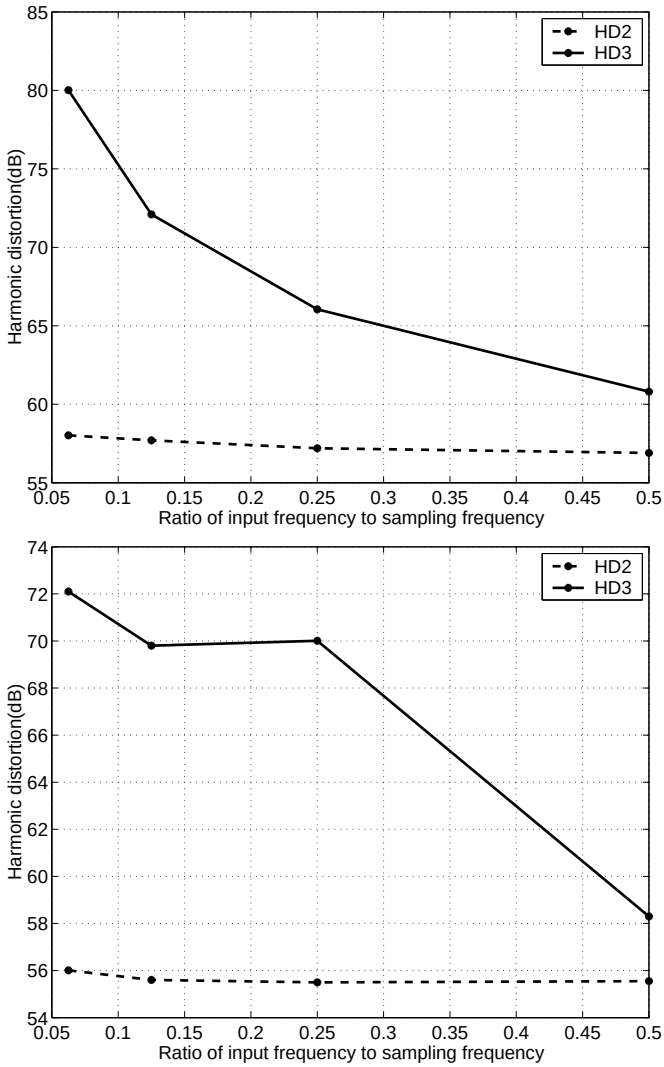

Figure 7.11: Harmonic distortion variation with input frequencies @ sampling frequencies of 80 MHz and 100 MHz

obtained in the chip testing. After many iterative simulations the problem was traced down to the interconnect capacitance formed between the bias node and the output of the 63 row-column decoding circuits.

The macromodel depicting this problem is shown in Figure 7.12. Since the output of the row-column decoding circuits is thermometer decoded, the number of 1's at its output is equal to the decimal equivalent of the input (x[n]). Now an expression for the voltage variation at the bias node can be obtained using charge conservation principle.

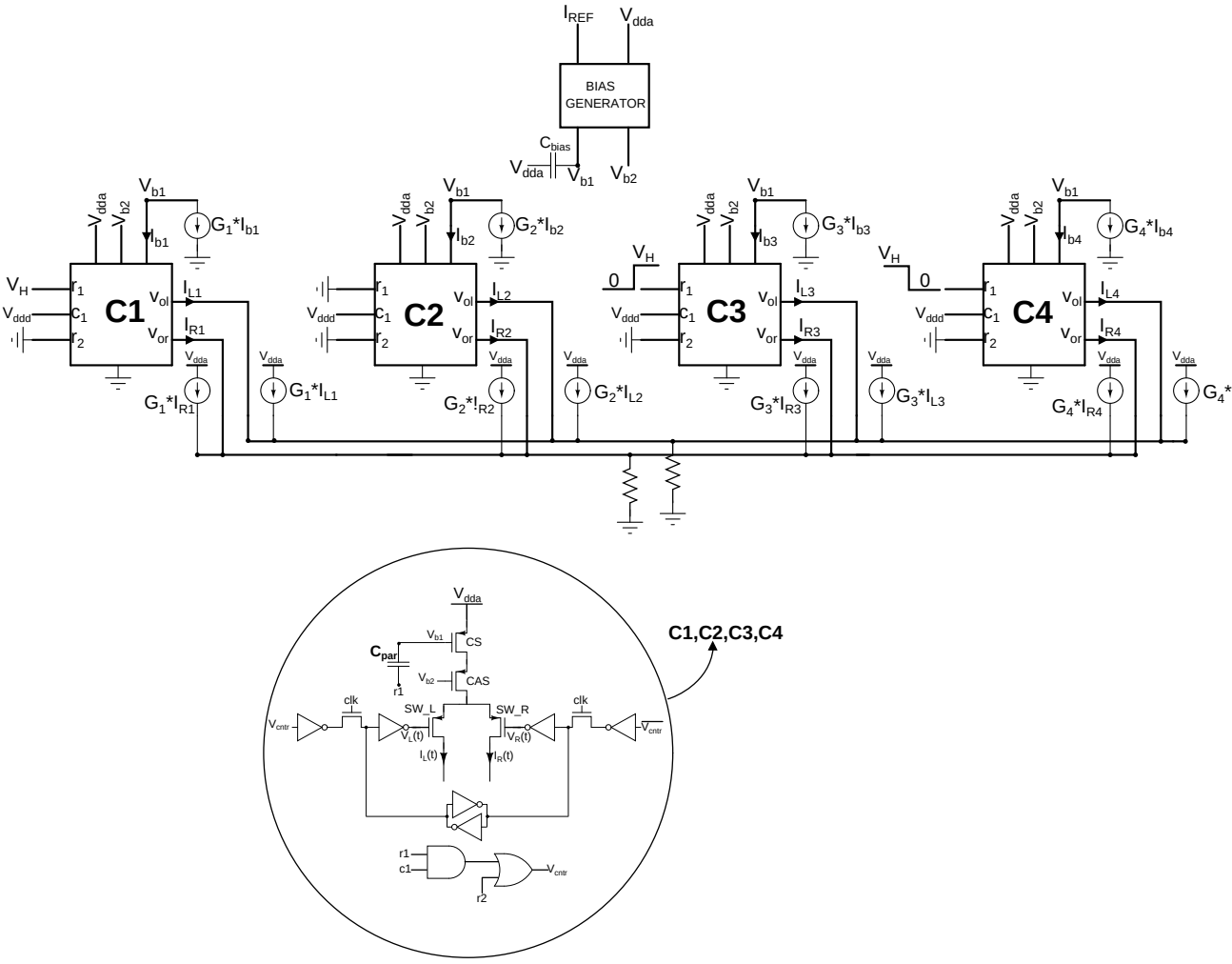

Figure 7.12: Macromodel depicting the bias problem

$$V_b[n] \quad = \quad V_b[0] - \frac{V_H C}{C_{bias}} x[n] \tag{7.2}$$

Here V_b[n] is the bias voltage at the 'n' the clock cycle, V_b[0] is the bias voltage initially, V_H is the voltage level corresponding to logic HIGH at the decoders output, 'C' is the interconnect capacitance and 'C_{bias}' is the capacitance layed out on the chip between the bias node and supply. From the above expression we can see that the bias node variation reflects the DAC output. To understand how this bias variation manifests itself as 2^{nd} harmonic at the DAC output, we will neglect all higher order odd harmonics except the first harmonic. Then,

$$V_O[n] \quad \simeq \quad a_1 x[n] R \tag{7.3}$$

Here a_1 is I_{bias} when there is no bias node variation. But when the node is varying,

$$a_1 \quad = \quad I_{bias} + g_m(V_b[n] - V_b[0]) \quad = \quad I_{bias} - \frac{g_m V_H C}{C_{bias}} x[n] \tag{7.4}$$

where 'g_m' is the transconductance of the current source transistor. So the DAC output can be written as,

$$V_O[n] \quad = \quad \Big(I_{bias} - \frac{g_m V_H C}{C_{bias}} x[n]\Big) x[n] R \quad = \quad I_{bias} x[n] - \frac{g_m V_H C}{C_{bias}} x[n]^2 \tag{7.5}$$

From the above equation we see that the bias variations reflect the output giving

rise to 2^{nd} harmonic even when the DAC is completely symmetric. The validity of the above expression was confirmed with further simulations. First the digital supply line (V_{DD}) which is numerically equal to V_H was varied. As the 2^{nd} harmonic is directly proportional to V_H, any dB change in V_{DD} should cause the same dB change in the 2^{nd} harmonic. In Figure 7.13 we have compared the calculated and observed HD2 variations with digital supply voltage. The observed results were obtained from the chip. We can see that the observed and calculated values are very closely matched. Hence the reason for the poor HD2 performance has been reasoned out.

The plot shown in Figure 7.14 compares the SFDR for various input frequencies at different sampling frequencies. The chip has been tested only to a maximum sampling frequency of 280 MHz because of limitation on the maximum rate at which the FPGA can clock out data.

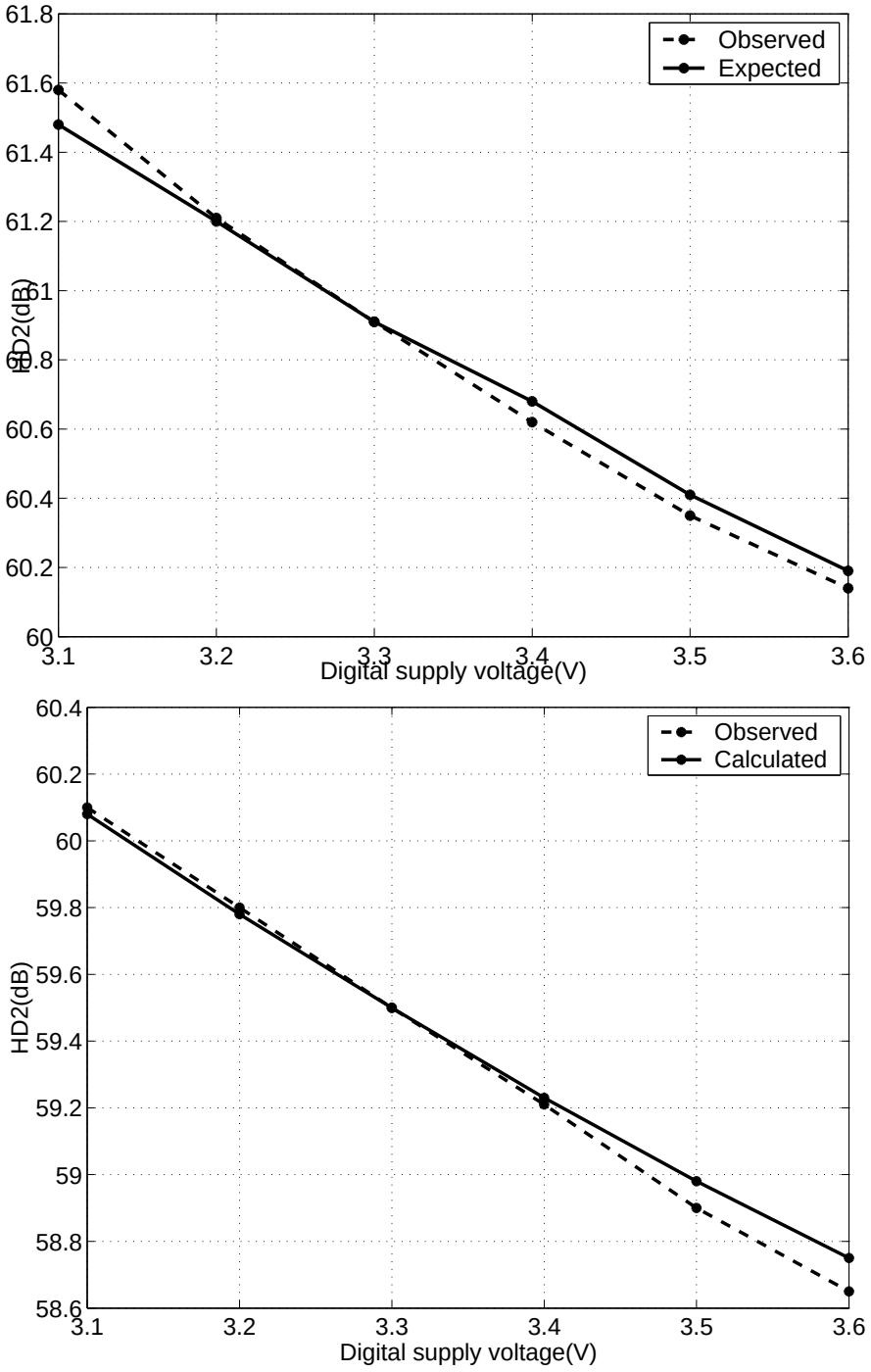

Figure 7.13: HD2 variation with digital supply voltage

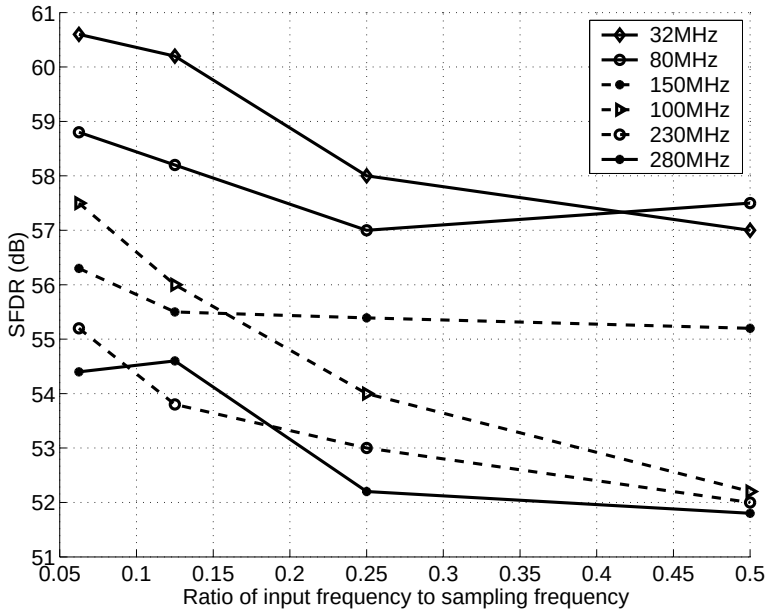

Figure 7.14: SFDR comparison for various sampling frequencies

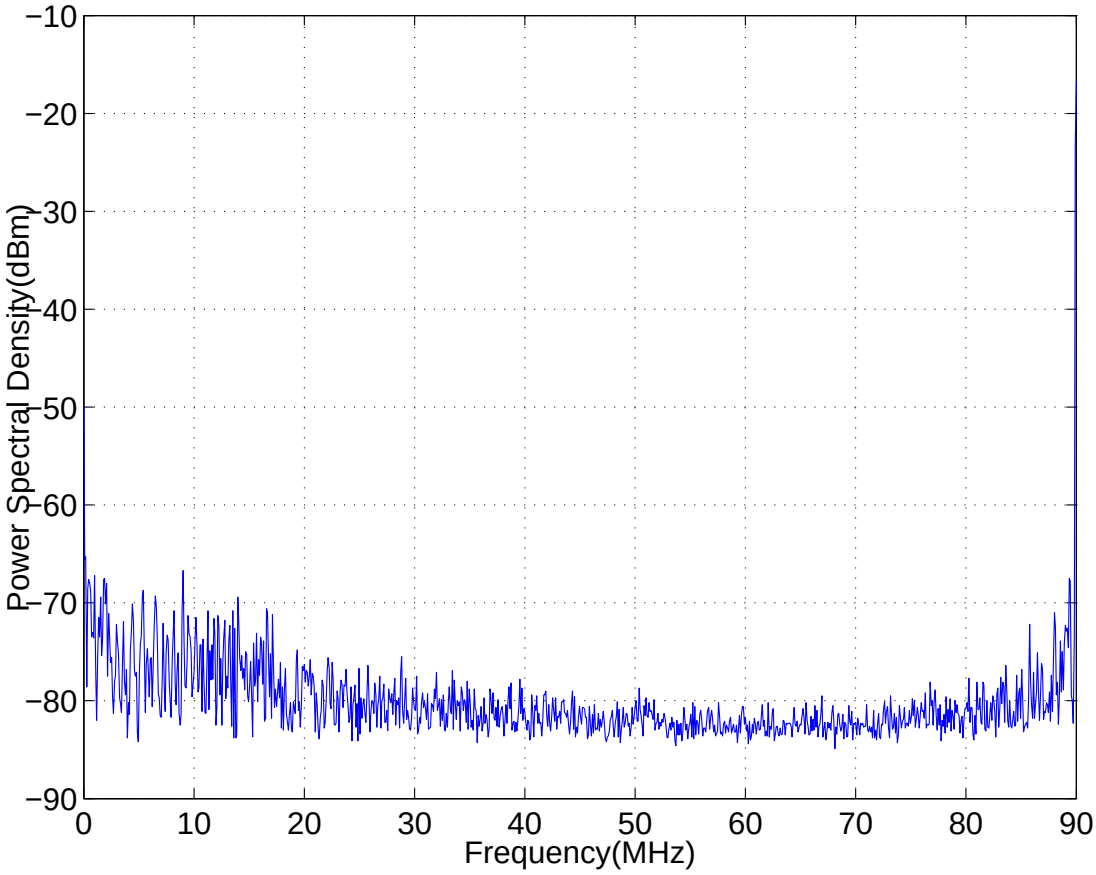

Figure 7.15: Sampling frequency of 180MHz and f_{in} =90 MHz

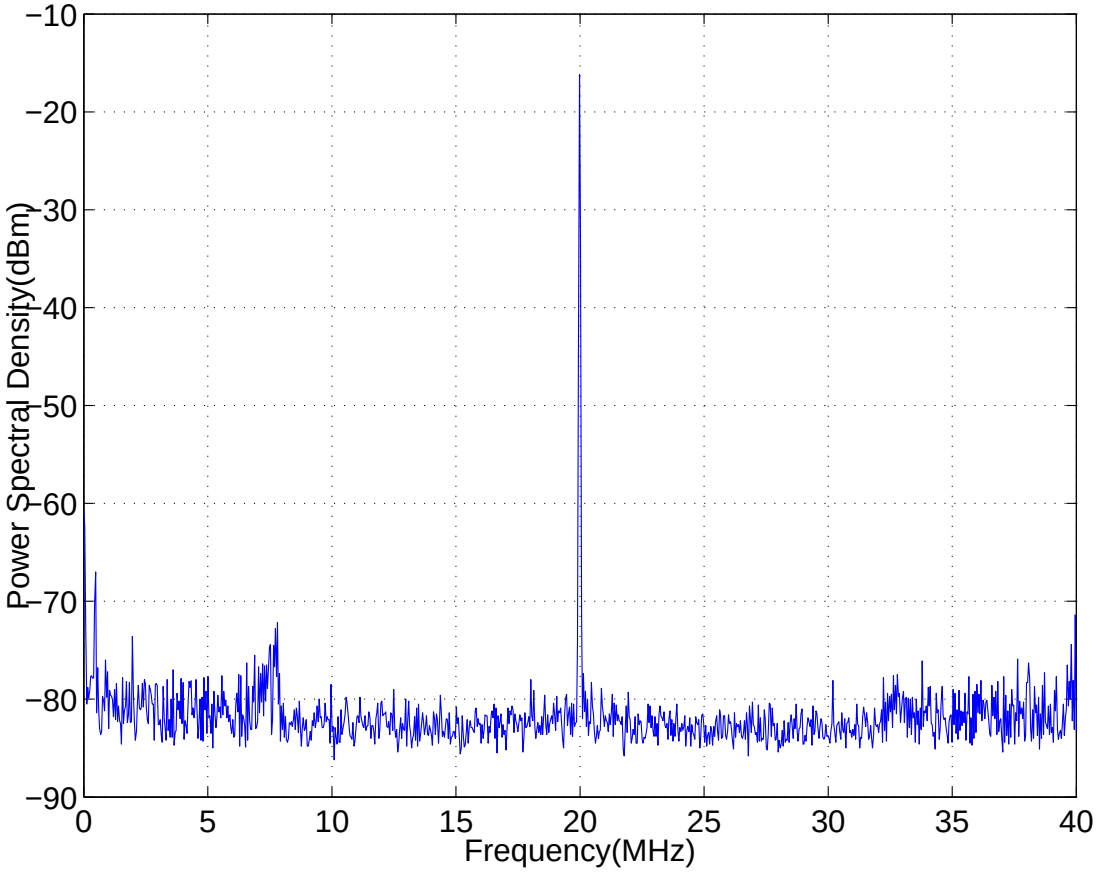

Figure 7.16: Sampling frequency of 80MHz and f_{in} =20 MHz

CHAPTER 8

CONCLUSIONS

A 10-bit current steering DAC which can operate till 500 MHz was designed and layed out in 0.35μm CMOS process. It is a (6+4) segmented DAC and the segmentation was done in a manner to optimize area. To achieve an accuracy of 10 bits, utmost care was taken in laying out the thermometer section. The INL of the chip is less than 0.5 LSB and the DNL is around 0.25 LSB. The dynamic performance of the DAC was characterized till 280 MHz where it exhibited a spurious performance of 52 dB at Nyquist frequency. We have also proposed a new technique to model the thermometer section which very accurately models all the non-linearities in the complete DAC. The simulation time had improved by a factor of 40.

REFERENCES

1. **Andersson, K.** and **M. Vesterbacka** (2005). Modeling of glitches due to rise/fall asymmetry in current-steering digital-to-analog converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **52**(11), 2265–2275.

2. **Andersson, K.** and **J. Wikner**, Characterization of a CMOS current-steering DAC using state-space models. *In Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems*, volume 2. 2000.

3. **B.Razavi**, *Principles of Data Conversion System Design*. IEEE Press, New Jersey, 1995.

4. **Chen, T.** and **G. Gielen**, Modelling of the impact of the current source output impedance on the SFDR of current-steering CMOS D/A converters. *In Proc. IEEE Int. Sym. Circuits and Systems*, volume 1. 2004.

5. **Clara, M.**, **A. Wiesbauer**, and **W. Klatzer**, Nonlinear distortion in current-steering D/A-converters due to asymmetrical switching errors. *In Proceedings of the International Symposium on Circuits and Systems*, volume 1. 2004.

6. **Lin, C.** and **K. Bult**, A 10-b, 500-Msps CMOS DAC in 0.6mm^2. *In Proc. IEEE Custom Integrated Circuits Conference*. 1998.

7. **Mercer, D.**, A study of error sources in current steering digital-to-analog converters. *In Proc. IEEE Custom Integrated Circuits Conference*. 2004.

LIST OF PAPERS BASED ON THESIS

1. S. Murali and S. Pavan. "Rapid Simulation of Current Steering DACs using Verilog-A," *IEEE Custom Integrated Circuits Conference, CICC* 2006, San Jose, September 2006