Design of High Performance Blocks for a Hearing Aid and a Headphone Driver

A THESIS

submitted by

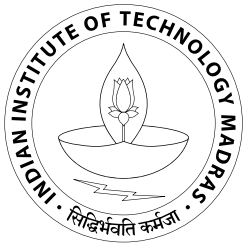
KUNAL KARANJKAR

for the award of the degree

of

MASTER OF SCIENCE

(by Research)



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CERTIFICATE

This is to certify that the thesis titled **Design of High Performance Blocks for a Hearing Aid and a Headphone Driver**, submitted by **Kunal Karanjkar**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Science**, is a bonafide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

The present work focusses on the design of high performance blocks for the frontend of a hearing aid and a headphone driver. The frontend blocks for the hearing aid are targeted for a low power consumption, a low input referred noise of $2\,\mu V_{rms}$, and a high dynamic range of 108 dB. The headphone driver is targeted for a low distortion of -90 dB, and a high output swing of 1.6 V peak while driving 16 Ω load. The frontend blocks include, the programmable gain amplifier (PGA), decimation filter, low dropout regulator (LDO), and ring oscillator.

The PGA is used to amplify the input signal to a sufficiently large output signal recognized by the ΔΣ analog-to-digital converter (ADC). The gain range is from -1 dB to 40 dB with a resolution of 0.5 dB. Its input referred noise is $2\,\mu V_{rms}$ with a total harmonic distortion (THD) of -80 dB in a bandwidth of 100 Hz - 10 kHz. To achieve this low input noise at a low power consumption, a pMOS + nMOS transistor differential input pair is used in the PGA.

The decimation filter removes the shaped quantization noise at the output of the ΔΣ ADC. It reduces the sampling rate of the input signal from 2.56 MHz to 40 kHz. To achieve low power, different techniques like multistage decimation, pipelining and retiming of registers, canonical signed digits (CSD) encoding for the filter coefficients, polyphase structure, and optimal register width are used in the decimation filter.

An LDO provides a supply regulated low noise voltage for the ring oscillator and the microphone. The LDO driving the ring oscillator is a complete on-chip LDO, whereas the LDO driving the microphone is stabilized by an off-chip capacitor. The ring oscillator provides the clock to the ΔΣ ADC, the decimation filter, and the backend blocks. Since the ΔΣ ADC is a single bit with a feedback digital-to-

analog converter (DAC) pulse of non-return-to-zero (NRZ), it is very sensitive to clock jitter. The oscillator's period jitter is required to be 30 ps or less in a 391 ns period.

Miscellaneous blocks for the hearing aid such as an automatic gain control (AGC) and a power-on reset (POR) are also discussed. The frontend blocks consume 144 μW of power in the 130 nm CMOS process.

The headphone driver utilizes a simple ac coupling to achieve class-AB operation in the audio bandwidth of 20 Hz - 24 kHz. It is highly linear with a THD $<$ -90 dB for a 1.6 V_p output signal while driving a 16 Ω load. The driver is driven from a dual supply of 1.8 V and -1.8 V to avoid a large dc blocking capacitor. Furthermore, the dual supply driver can support higher output voltage swing compared to the single supply driver, thus delivering higher output power. The -1.8 V is derived from the 1.8 V using a negative voltage converter. The negative voltage converter operates at a clock frequency of 200 kHz resulting in a negative voltage conversion efficiency of 96 %. The driver consumes a quiescent power of 1 mW from the 1.8 V supply and delivers a maximum power of 80 mW to the load. The headphone driver is designed in the 180 nm CMOS process.

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ABBREVIATIONS

PGA	Programmable Gain Amplifier
AGC	Automatic Gain Control
ADC	Analog to Digital Converter
LDO	Low Dropout Regulator
POR	Power On Reset
CMFB	Common Mode Feedback
DAC	Digital to Analog Converter
CTDSM	Continuous Time Delta Sigma Modulator
DSP	Digital Signal Processor
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
CIC	Cascaded Integrator Comb
CTS	Clock Tree Synthesis
MSA	Maximum Stable Amplitude
NRZ	Non Return-to Zero
OSR	Oversampling Ratio
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion and Noise

CHAPTER 1

Introduction

Hearing impairment in humans affects the ability to understand speech, and to localize the surrounding sound sources. Hearing aids are used to improve a person's hearing ability. All the hearing aids, whether analog or digital, are designed to increase the strength of the sound reaching the ear-drum so that the hearing impaired person can understand speech better.

1.1 Analog hearing aids

Analog hearing aids have a microphone that picks up the sound and converts it into an electrical signal. The signal is then amplified by the transistors and fed to the ear phone speaker on the hearing aid which is next to the ear-drum so that the listener can hear the sound. Most of the analog hearing aids compress the sound using an AGC. This amplifies the low sounds until they are loud enough to be heard, and gives less amplification to the loud sounds, thus protecting against uncomfortably loud sounds. Analog hearing aids are cheaper than the digital ones. However, one of the major drawback of the analog hearing aid is, it amplifies the signal and the noise equally, without suppressing the noise. An analog hearing aid block diagram is shown in Fig. 1.1.

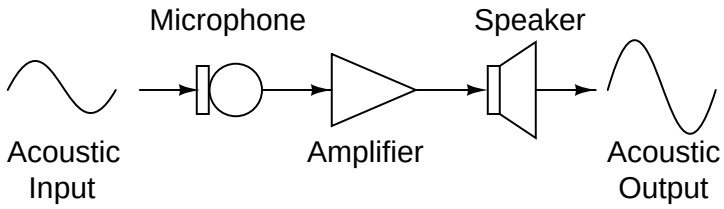


Figure 1.1: Analog hearing aid block diagram.

1.2 Digital hearing aids

Digital hearing aids are similar to the analog hearing aids except that they convert the amplified analog signal to digital, process it digitally, and convert the digital signal back to analog. The digitized signal is processed by a digital signal processor (DSP). Some of the important DSP functions are[1]:

- Increasing or decreasing levels of sounds in different frequency ranges
- Reducing background noise by certain noise reduction algorithms
- Varying the gain of the programmable gain amplifier
- Providing directional sound focus

A digital hearing aid block diagram is shown in Fig. 1.2.

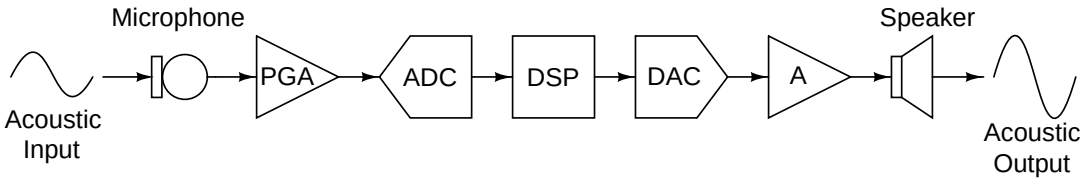


Figure 1.2: Digital hearing aid block diagram.

The major power is consumed by the DSP[1]. For more advanced DSP requirements in the future, the DSP power levels can go further up. So, the power consumed by other blocks has to be reduced. The frontend is composed of the blocks coming before the DSP, and the backend is composed of the blocks following the DSP. The backend can consume a significant amount of power. By adopting a class-D driver stage, the backend power can be brought down to less than 10 % of the total power[2]. The frontend consumes minimum amount of power in the complete chain. The ADC is a $\Delta\Sigma$ modulator based ADC which enables low power design. The PGA should provide variable gain at low power. The power thus saved can be allocated to the DSP for its advanced functions. In this work, the design of the frontend blocks for the digital hearing aid are discussed.

The frontend includes the PGA and the ADC. Since, the ADC used is a $\Delta\Sigma$ modulator based ADC, it is required to be followed by the decimation filter to remove

the shaped quantization noise. The clock for the ADC and the decimation filter is provided by the ring oscillator. Since the ring oscillator frequency is dependent on its supply voltage, the supply voltage should be very stable and having low noise. This supply voltage is obtained from an LDO. One additional LDO is used to provide the supply voltage for the microphone. The complete frontend chain is shown in Fig. 1.3.

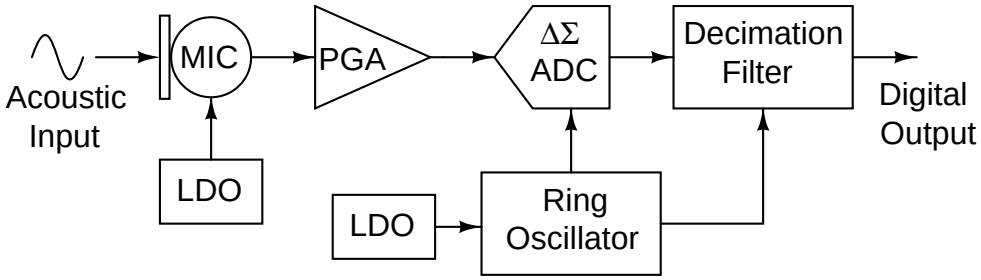


Figure 1.3: Front end block diagram.

1.3 Headphone driver

Due to rapid growth in the manufacture of consumer electronic goods like cell phones, the demand for high efficiency headphone drivers has also increased. Battery life is an important aspect of a portable audio device. This demands for maximum efficiency of the driver. The class-D amplifiers are more efficient than class-AB amplifiers. But owing to electromagnetic interference (EMI) issues with the class-D amplifier, class-AB amplifiers are preferred for headphone applications[3]. Headphone speakers have a typical resistance of $16\,\Omega$. If the dc bias at the output of the driver is not removed, a large dc current flows through the headphones, which wastes power, clips the output signal, and potentially damages the headphones. In order to remove this dc bias, a large capacitor ($> 500\,\mu$F) is required. Such a large capacitor consumes a large area, and thereby it is not suitable for portable audio applications. During start-up or shutdown, this capacitor has to be charged or discharged which causes an audible pop.

If the output bias is kept at $0\,$V, the dc blocking capacitor is not required. This

eliminates the disadvantages associated with it. To achieve the 0 V output bias, the driver should be supplied from a dual supply of 1.8 V and -1.8 V. In addition, the dual supply driver can support higher output voltage swing compared to the single supply driver, thus delivering higher output power. The negative supply voltage is generated using a charge pump based negative voltage converter.

1.4 Organization of the thesis

The first part of the thesis is about the design of the frontend blocks for the hearing aid. The second part deals with the design of the 16 Ω headphone driver. The thesis is organized as follows:

Chapters 2-6 form the first part of the thesis which discuss the frontend blocks for the hearing aid.

Chapter 2 discusses the design of the PGA.

Chapter 3 discusses the design of the decimation filter.

Chapter 4 discusses the design of the ring oscillator.

Chapter 5 discusses the design of the LDO for the ring oscillator and the microphone.

Chapter 6 discusses the measured results from the hearing aid chip.

Chapters 7 & 8 form the second part of the thesis which discuss the headphone driver.

Chapter 7 discusses the design of the headphone driver used to drive the 16 Ω load.

Chapter 8 discusses the design of the negative voltage converter for the headphone driver.

CHAPTER 2

Programmable Gain Amplifier

2.1 Introduction

The PGA is used to amplify the output of the microphone to a sufficiently large value, avoiding overloading of the $\Delta\Sigma$ ADC. The PGA amplifies an input signal in a particular range to an output signal of a fixed amplitude. This output signal amplitude is the maximum stable amplitude (MSA) of the $\Delta\Sigma$ ADC. Thus for the particular input signal range, the ADC operates at its peak SNR. This increases the dynamic range of the frontend. In our case, the input signal range is from $4\,\mathrm{mV_p}$ to $450\,\mathrm{mV_p}$, for which the PGA gain varies from 40 dB to -1 dB, giving a constant output amplitude of $400\,\mathrm{mV_p}$. For an input amplitude less than $4\,\mathrm{mV_p}$ and greater than $450\,\mathrm{mV_p}$, the transfer characteristic is linear with a constant gain of 40 dB and -1 dB, respectively. Fig.2.1 shows the transfer characteristics of the PGA. Table.2.1 shows the design specifications of the PGA.

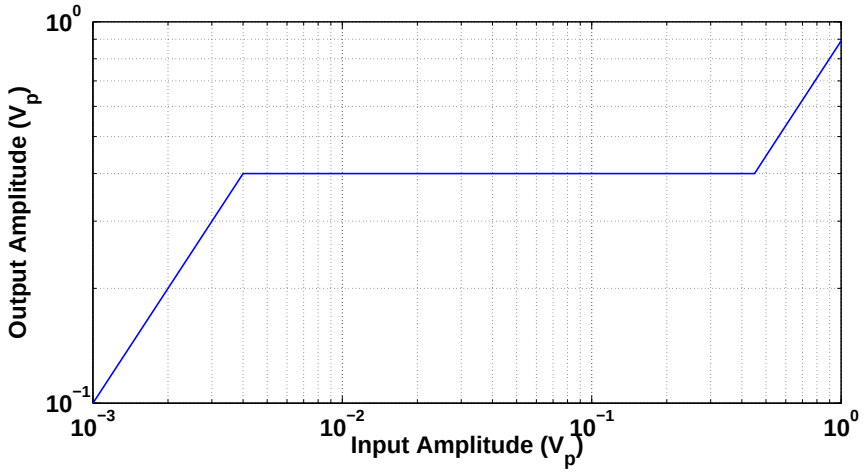


Figure 2.1: PGA transfer characteristics.

Table 2.1: Design specifications.

Input referred noise	$2.4\,\mu V_{rms}$
Bandwidth	100 Hz - 10 kHz
THD	-80 dB
Gain range	-1 dB - 40 dB
Gain step	0.5 dB
Process	130 nm CMOS

2.2 PGA design

The microphone output is single-ended, while the ADC input is differential. The input impedance of the ADC is $R_L = 120\,k\Omega$. The PGA must convert the single-ended input to a differential output. The differential feedback PGA architecture is shown in Fig. 2.2. The PGA outputs are

$$V_{op} = \frac{R_2}{2R_1}V_i, V_{om} = -\frac{R_2}{2R_1}V_i \tag{2.1}$$

$$A = \frac{V_{op} - V_{om}}{V_i} = \frac{R_2}{R_1} \tag{2.2}$$

The voltage at both the input terminals of the op-amp is equal due to negative feedback, and is

$$V_x = \frac{R_2}{2(R_1 + R_2)}V_i \tag{2.3}$$

Thus from (2.3), there is a considerable fraction of the input signal appearing at the input terminals of the op-amp, which can degrade the THD.

The single ended feedback PGA architecture for the same gain is shown in Fig. 2.3. We get the same output voltages as given by (2.1), (2.2). But there is no signal component at both the input terminals of the op-amp due to negative feedback. Thus, the single ended feedback PGA is more linear than the differential feedback PGA. In addition, the number of resistors required in the single ended feedback PGA are less. Thus, noise contribution from the resistors is avoided. But noise contribution from the transistors in the output stage common mode feedback (CMFB) circuit comes directly at the single ended feedback PGA outputs.

However, this noise is more than the reduced noise contribution from the resistors, thereby increasing the total noise. In the case of differential feedback PGA, noise from the output stage CMFB circuit will be cancelled by virtue of differential feedback. Thus, the differential feedback PGA achieves a lower noise than the single ended feedback PGA. The required THD of -80 dB can be achieved in the differential feedback PGA by a suitable op-amp architecture as explained below. So, the differential feedback PGA architecture is used.

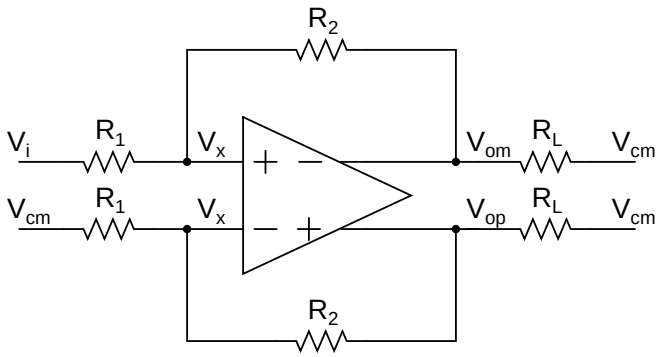


Figure 2.2: Differential feedback PGA architecture.

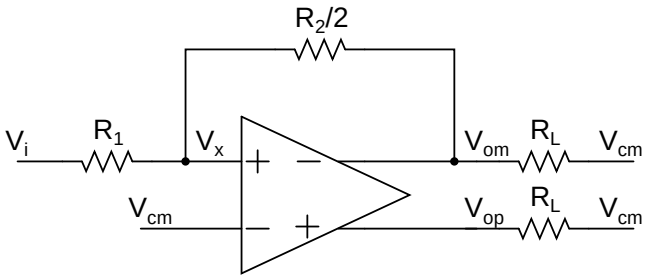


Figure 2.3: Single ended feedback PGA architecture.

2.2.1 Op-amp architecture

Distortion reduces with increasing the loop gain. For a PGA gain of 40 dB, the loop gain around the op-amp becomes minimum, which increases the distortion. So, a high dc gain of 100 dB is obtained using a three stage op-amp. The input referred voltage noise spectral density of the op-amp with the pMOS input pair

and an nMOS load is

$$S_{n1}(f) = \frac{16kT}{3g_{mp}}\left(1 + \frac{g_{mn}}{g_{mp}}\right) + \frac{1}{C_{ox}f}\left(\frac{K_p}{W_pL_p} + \frac{K_n}{W_nL_n}.\frac{g_{mn}^2}{g_{mp}^2}\right) \tag{2.4}$$

where g_{mp}, g_{mn} are the transconductances; W_p, W_n are the widths; and L_p, L_n are the lengths of the pMOS and the nMOS, respectively. The pMOS input pair is contributing transconductance, while the nMOS load is contributing only noise. To reduce the input referred noise, a large input transconductance is required. This could be obtained by increasing the current through the input pMOS transistor. But since the need is to design low power PGA, this option is ruled out. Instead, it is decided to give input to both the pMOS and nMOS differential pair. The input transconductance becomes $g_{mp} + g_{mn}$. The input referred voltage noise spectral density of the op-amp with both the pMOS and nMOS input pair is

$$S_{n2}(f) = \frac{16kT}{3(g_{mp} + g_{mn})} + \frac{1}{C_{ox}f}\left(\frac{K_p}{W_pL_p} \cdot \frac{g_{mp}^2}{(g_{mp} + g_{mn})^2} + \frac{K_n}{W_nL_n} \cdot \frac{g_{mn}^2}{(g_{mp} + g_{mn})^2}\right) \tag{2.5}$$

Comparing (2.4) and (2.5), results in $S_{n1}(f) > S_{n2}(f)$. Thus, a lower input referred noise can be achieved without increasing the power.

The minimum value of resistor R_1 is decided based on the loading of the microphone. In our case, the minimum impedance the microphone can drive is $17\,\mathrm{k\Omega}$. The input impedance of the PGA is

$$Z_{in} = \frac{2R_1(R_1 + R_2)}{2R_1 + R_2} = \frac{2R_1(1 + A)}{2 + A} \tag{2.6}$$

The minimum input impedance, $Z_{in,min} = 20\,\mathrm{k\Omega}$ is used. So, for a gain of $40\,\mathrm{dB}$, using (2.6) results in $R_1 = 10\,\mathrm{k\Omega}$, $R_2 = 1\,\mathrm{M\Omega}$. The input referred integrated noise voltage of the PGA is

$$V_{n,in}^2 = \left(8kTR_1 + 8kTR_2\left(\frac{R_1}{R_2}\right)^2 + S_{n,opa}\left(1 + \frac{R_1}{R_2}\right)^2\right) \cdot BW \tag{2.7}$$

For $V_{n,in} = 2\,\mu\mathrm{V_{rms}}$ we get $V_{n,opa} = 1\,\mu\mathrm{V_{rms}}$.

Fig. 2.4 shows the circuit diagram of the op-amp while Fig.2.5 shows its CMFB

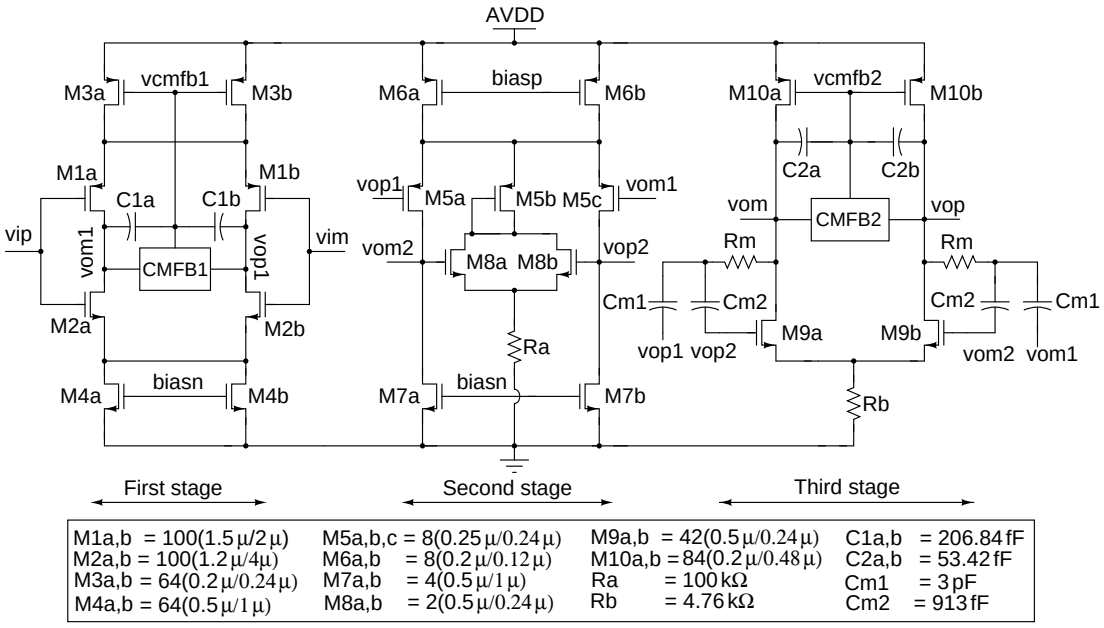


Figure 2.4: Circuit diagram of the op-amp.

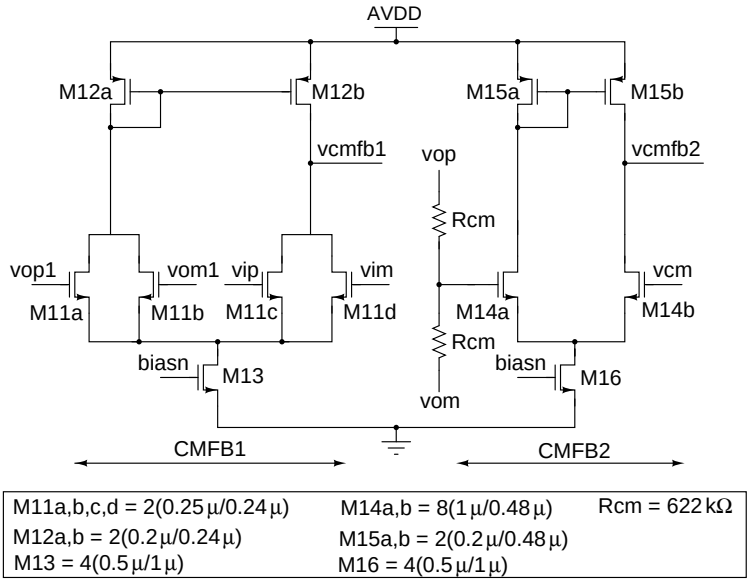


Figure 2.5: CMFB circuit of the op-amp.

circuit diagram. The transistors M1a-M1b and M2a-M2b form the input pMOS pair and the nMOS pair, respectively. Their widths and lengths are kept large to reduce flicker noise. The bias voltages biasn and biasp are derived from a current mirror based biasing circuit. The first stage CMFB circuit in Fig. 2.5 ensures that

its output has the same common mode as the input. Miller capacitors C1a and C1b are used to compensate this CMFB loop. The current in each of the input pairs is $4\,\mu$A to get an input referred noise of $1\,\mu\mathrm{V_{rms}}$.

Transistors M5-M8 form the second stage. Transistors M5b and M8a-M8b form the CMFB circuit for this stage. If the common mode voltage at the nodes vop2 and vom2 decreases, it will decrease the current in M8a-M8b, and hence decreases the current in M5b. This increases the current through M5a-M5c as the total current through M6a-M6b is constant, eventually increasing the common mode voltage at the nodes vop2 and vom2. The drain voltage of M7 is decided by the gate voltages of M8a,b. At ff MOS corner, where the threshold voltage (V_T) decreases, the V_{GS} of M8a,b will reduce causing an increase in the g_{ds} of M7a,b, thus degrading the second stage gain. So, a resistance of $100\,\mathrm{k}\Omega$ is kept in series with the source of M8a,b. This resistance carries a voltage drop of 50 mV to provide sufficient V_{DS} for M7a,b.

Since the input and the output common mode voltages are same, the swing at the op-amp output will be limited by the threshold voltage (V_T) of M9a,b. Apart from providing gain, the second stage also shifts the common mode input of the second stage to a value lower than the third stage output common mode. This is to ensure a signal swing of $200\,\mathrm{mV_p}$ peak over the common mode at the output of the third stage keeping M9a, M9b always in the saturation region. Transistors M14-M16, and the resistor Rcm form the CMFB for the third stage. This CMFB ensures that the output common mode voltage is at vcm. Since it is a two stage CMFB, it is compensated by adding Miller capacitors C2a and C2b. Nested Miller compensation[4] employing capacitors Cm1, Cm2 and a zero-cancelling resistor Rm is used for stabilizing the op-amp. The current in the third stage is fixed to $5.25\,\mu$A to get a phase margin of 69^0 for a PGA gain of 0 dB.

Table 2.2 shows the op-amp characteristics. Fig. 2.6, and Fig. 2.7 shows the magnitude and the phase response of the loop gain for a PGA gain of 0 dB, respectively. Fig. 2.8 and Fig. 2.9 shows the common mode feedback loop magnitude and phase

response, respectively. Fig. 2.10 shows the common mode step response of the op-amp for a PGA gain of 40 dB and a step of 1 mV_p at the PGA's input node V_i.

Table 2.2: Op-amp characteristics.

Input referred noise	1 μV_{rms}
DC loop gain	96 dB
Unity loop gain frequency	5.5 MHz
Phase margin	69^0
Power consumption	25 μW

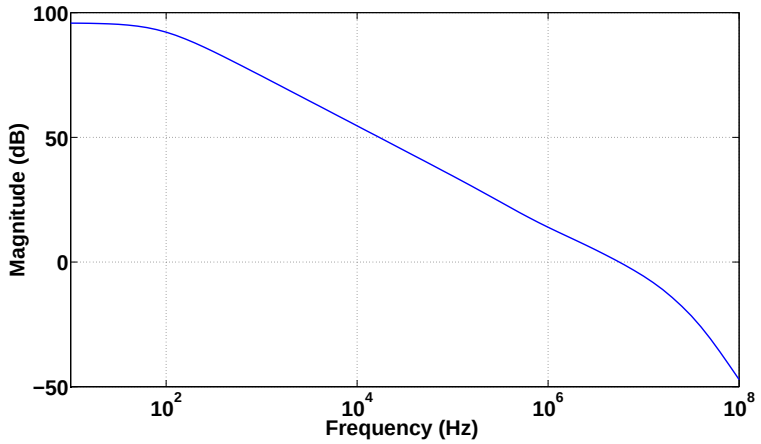


Figure 2.6: Magnitude response of the loop gain.

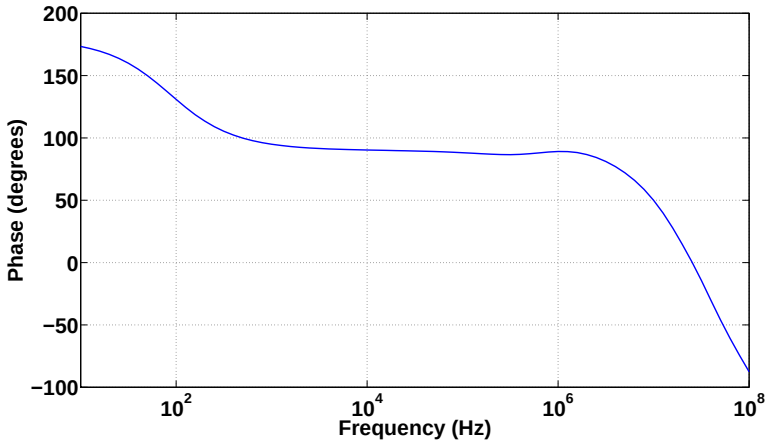


Figure 2.7: Phase response of the loop gain.

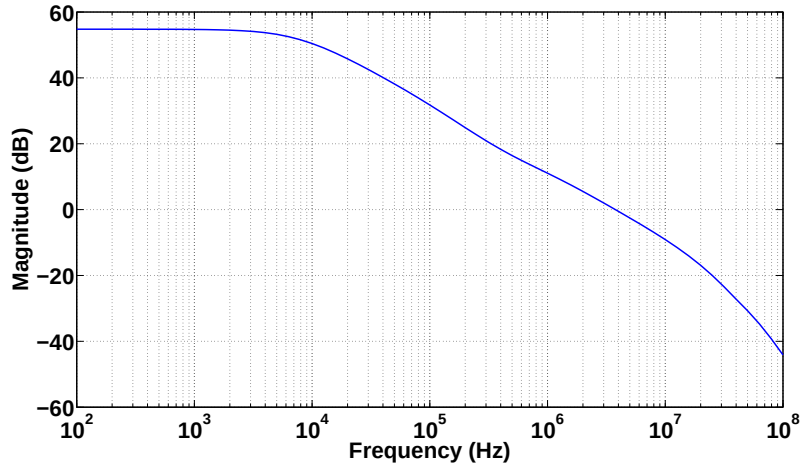


Figure 2.8: Magnitude response of the CMFB loop gain.

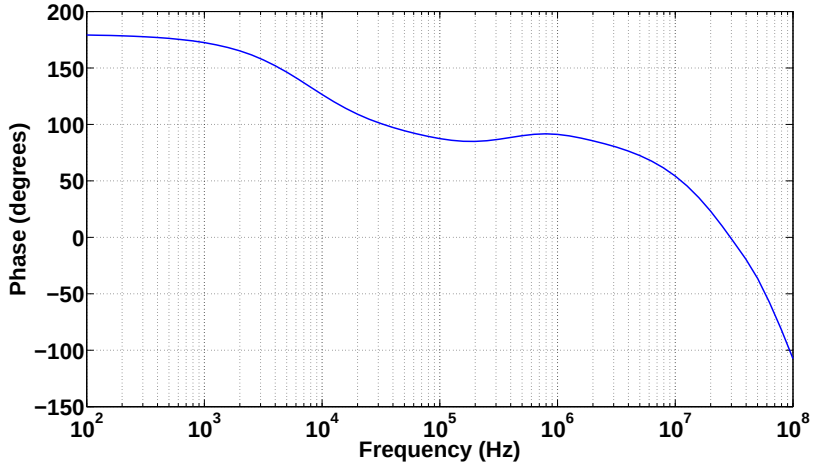


Figure 2.9: Phase response of the CMFB loop gain.

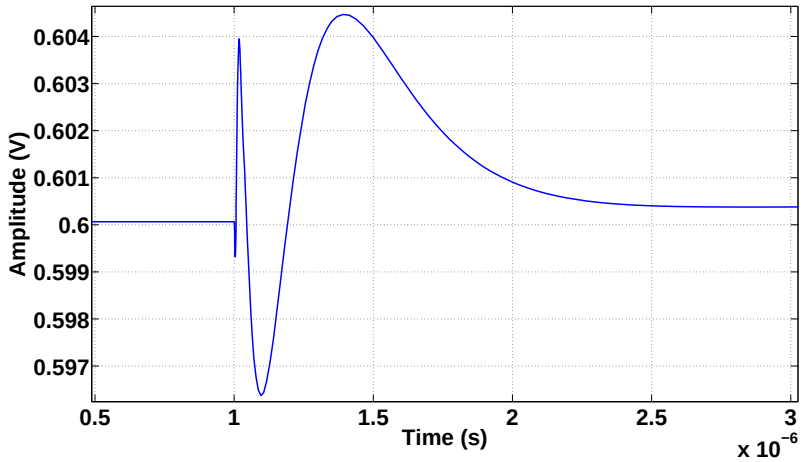


Figure 2.10: Common mode step response of the op-amp.

2.2.2 Programming linear-in-dB gain steps

The PGA gain varies from -1 dB to 40 dB in steps of 0.5 dB. For this linear-in-dB gain step, changing the input or the feedback resistor exponentially results in non-uniform resistor values. We want to obtain linear-in-dB gain steps with linear changes in the resistor values. Consider a gain decrement of 0.5 dB from an initial gain G_0 to a gain G.

$$G_0 = \frac{R_{20}}{R_{10}}, G = \frac{R_2}{R_1} \tag{2.8}$$

$$\frac{G}{G_0} = 10^{\frac{-0.5}{20}} = e^{\frac{-ln(10)}{40}}$$

$$e^x = \frac{e^{x/2}}{e^{-x/2}} = \frac{1+x/2}{1-x/2}$$

Using the above approximation for a small x, we get

$$\frac{R_2}{R_1} = \frac{R_{20}\left(1 - \frac{\ln(10)}{80}\right)}{R_{10}\left(1 + \frac{\ln(10)}{80}\right)} \tag{2.9}$$

The error in the gain step should be < 0.1 dB. For this, a particular value of R_{10} and R_{20} is used and the R_1, R_2 values are changed as given by (2.9) for 0.5 dB gain decrement. The R_{10} and R_{20} values are shown in Table 2.3.

For the maximum gain of 40 dB, $R_{10} = 10\,\text{k}\Omega$ and $R_{20} = 1\,\text{M}\Omega$. Then after every 4 dB decrement in the gain, R_{20} is kept as 1 MΩ till a gain of 12.5 dB is reached and R_{10} is increased to get the required gain. We have chosen to increase R_{10} instead of decreasing R_{20} to reduce power dissipation. After a further 4 dB decrement in the gain, R_{10} is kept as 158.5 kΩ, while R_{20} is decreased to get the required gain. This ensures that the input noise for the minimum gain does not degrade the signal to noise ratio (SNR) of the frontend.

Fig. 2.11 shows the input resistor (R_1) bank. Terminal T1 is connected to the input source and T2 is connected to the input terminal of the op-amp. The resistor bank is divided in seven branches. Each branch has eight resistors giving a

Table 2.3: R_{10}, R_{20} for different gains.

$\boldsymbol{R_{10}}$ **(kΩ)**	$\boldsymbol{R_{20}}$ **(kΩ)**	**Gain interval (dB)**
10	1000	40 - 36.5
15.85	1000	36 - 32.5
25.12	1000	32 - 28.5
39.81	1000	28 - 24.5
63.1	1000	24 - 20.5
100	1000	20 - 16.5
158.5	1000	16 - 12.5
158.5	631	12 - 8.5
158.5	398	8 - 4.5
158.5	251.2	4 - 0.5
158.5	158.5	0 - -1

minimum gain step of 0.5 dB. All switches are implemented using nMOS transistors. The first resistor in each branch corresponds to R_{10}, followed by seven equal resistors. The first branch is programmed for a gain range of 40 dB to 36.5 dB, the second branch is programmed for a gain range of 36 dB to 32.5 dB, the third branch is programmed for a gain range of 32 dB to 28.5 dB, the fourth branch is programmed for a gain range of 28 dB to 24.5 dB, the fifth branch is programmed for a gain range of 24 dB to 20.5 dB, the sixth branch is programmed for a gain range of 20 dB to 16.5 dB, and the seventh branch is programmed for a gain range of 16 dB to 12.5 dB. For further lower gains, the input resistor is set to one of the resistors in the seventh branch.

A similar resistor bank, as shown in Fig. 2.12, which has five branches, is used for the feedback resistor. Terminal T1 is connected to the op-amp output and T2 is connected to the input terminal of the op-amp. The fifth branch is programmed for a gain range of 40 dB to 36.5 dB. This branch is repeatedly used for lower 4 dB gain intervals till a gain of 12.5 dB is reached. The fourth branch is programmed for a gain range of 12 dB to 8.5 dB, the third branch is programmed for a gain range of 8 dB to 4.5 dB, the second branch is programmed for a gain range of 4 dB to 0.5 dB, and the first branch is programmed for a gain range of 0 dB to -1 dB.

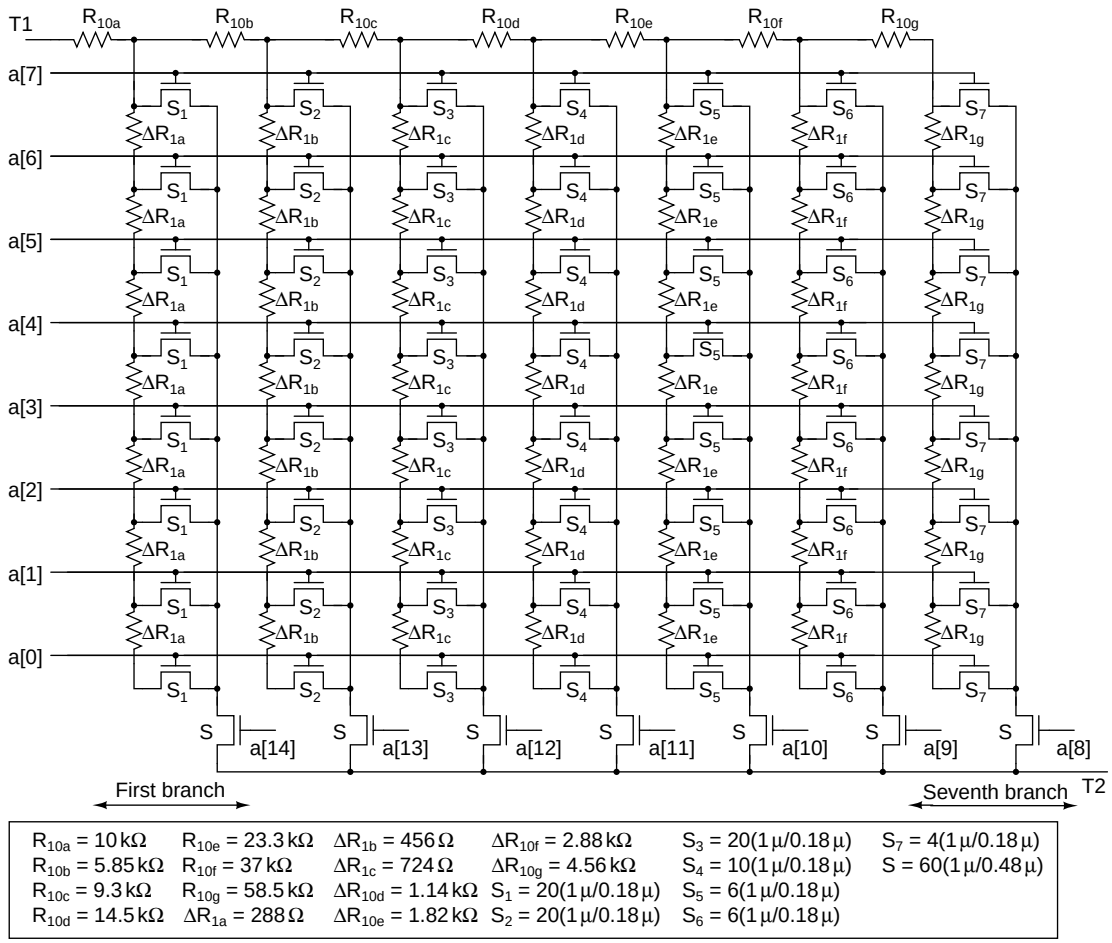


Figure 2.11: Input resistor bank in the PGA.

2.2.3 Switches in the resistor banks

For any gain setting, one of the branches is selected using the switch connected at that branch end, and then using another switch in that branch, the required resistor is selected. The control signals a[14:8] are used to select a particular branch in the input resistor bank, while the control signals a[12:8] are used to select a particular branch in the feedback resistor bank. The control signals a[7:0] are used to select a particular input and feedback resistor among each of the selected branches. This kind of switching considerably reduces the number of control signals required. The control signals a[19:0] are generated either by an internal AGC loop or by an external DSP. The switches in each branch are implemented using low V_T nMOS transistors to get a very small ON resistance compared to the smallest resistor in that branch. But this reduces the OFF resistance of the switches.

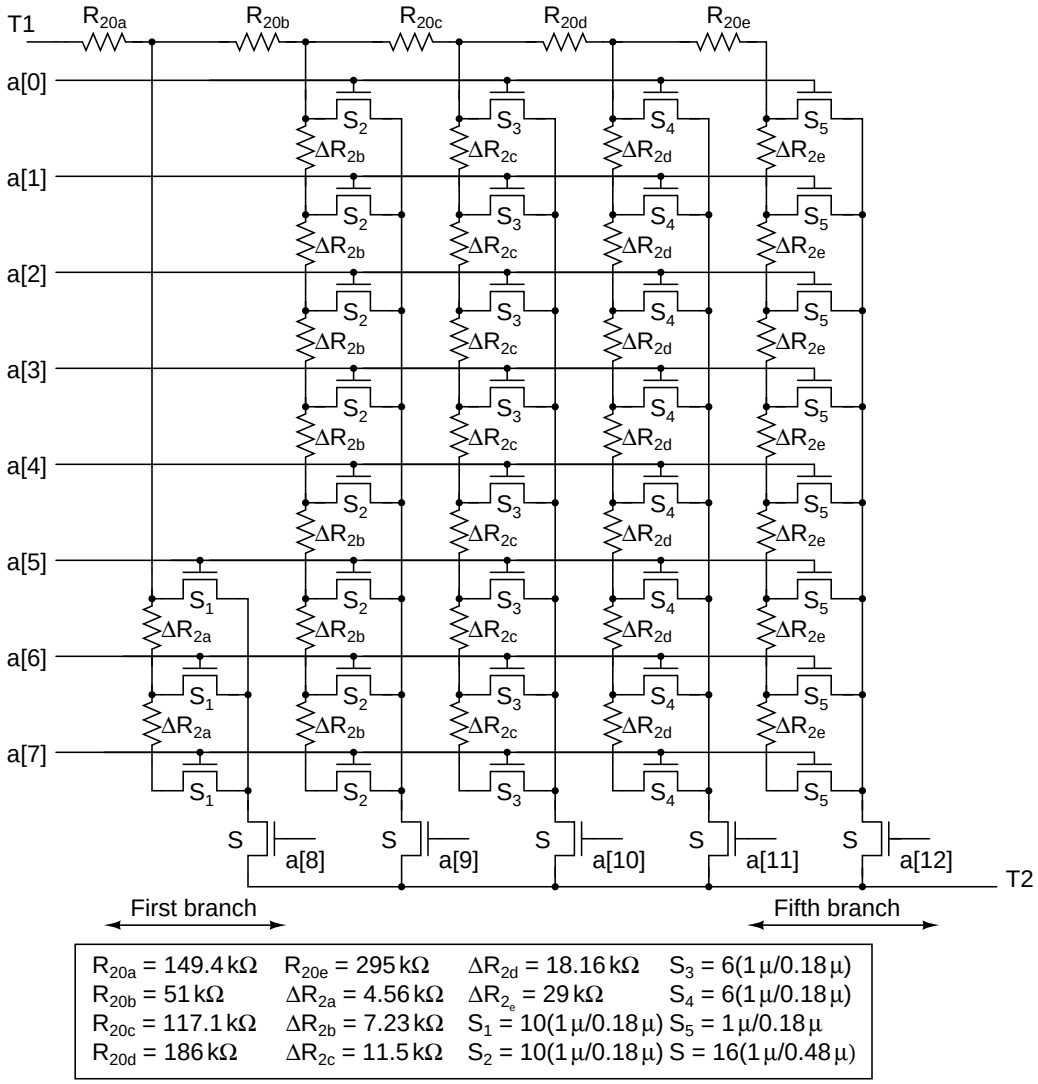


Figure 2.12: Feedback resistor bank in the PGA.

One regular nMOS transistor switch S is connected at the end of each branch in both the resistor banks. It is sized to have very high OFF resistance. The ON resistance of this switch is smaller than the smallest resistor in the branch. The reason for using two switches in series with the resistor is to reduce the effect of non-linearity introduced by the OFF switches. As the input signal is single-ended, the input terminal of the op-amp sees a voltage swing of V_x given by (2.3). So if we use only one switch in series with the resistor, drain to source voltage of all the OFF switches will be

$$V_{DS} = V_i \frac{2R_1 + R_2}{2(R_1 + R_2)} \tag{2.10}$$

Due to this large V_{DS}, considerable non-linear transient current is injected at the input terminal of the op-amp which degrades the distortion performance of the PGA. To reduce this distortion, the V_{DS} of all the OFF switches should be reduced by isolating their source terminals from the input terminal of the op-amp. Using one extra switch for each branch, the V_{DS} of all the other branch switches is reduced to 0 V. Thus the effect of the non-linear current due to the OFF switches is reduced, and the distortion is minimized.

2.3 Monotonicity in the PGA gain

Monotonicity in the PGA gain needs to be ensured. At every 4 dB gain interval starting from 0 dB, for a 0.5 dB gain increment, both R_1, R_2 are increased till a 16 dB gain is reached. And at every 4 dB gain interval starting from 16 dB, for a 0.5 dB gain increment, both R_1, R_2 are decreased till a 40 dB gain is reached. The detailed resistor values are tabulated in the appendix A. In the above cases, the gain should increase and not decrease due to random mismatch in the resistors. We calculate the standard deviation of the ratio of the two gains G_1 and G_2 where, $G_2 = G_1 + 0.5$ dB, at every 4 dB gain interval. The nominal values of G_1 and G_2 are related as $G_{20} = G_{10} + 0.45$ dB. The minimum value of (G_2/G_1) is

$$\left(\frac{G_2}{G_1}\right)_{min} = \frac{G_{20}}{G_{10}}\left(1 - 3\sigma\left(\frac{G_2}{G_1}\right)\right) \tag{2.11}$$

To ensure monotonicity in the gain, $(G_2/G_1)_{min} > 0$ dB.

Consider the gain increment from 36 dB to 36.5 dB, for which both R_1, R_2 are decreased. Fig. 2.13 shows the single ended circuit giving the details of the switching for this gain increment. We have denoted the resistors with reference to Fig. 2.11 and Fig. 2.12 as: $\mathrm{R_{2b}} = \mathrm{R_{20a}} + \mathrm{R_{20b}} + \mathrm{R_{20c}} + \mathrm{R_{20d}} + \mathrm{R_{20e}}$, $\mathrm{R_{1a}} = \mathrm{R_{10a}}$,

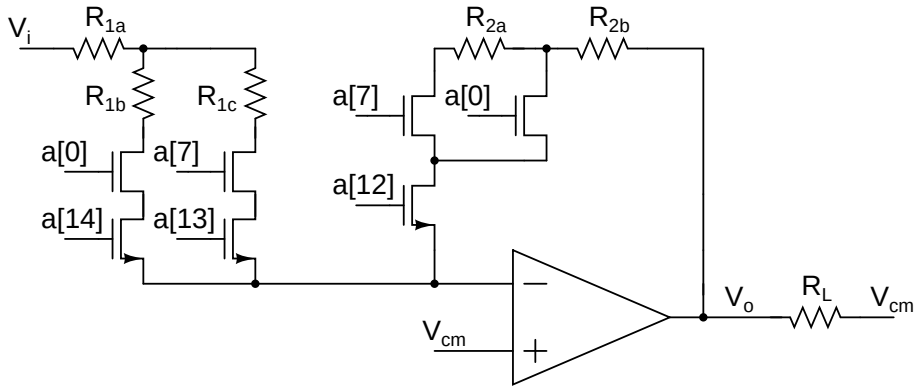


Figure 2.13: PGA gain switching from 36 dB - 36.5 dB.

$R_{1b} = 7\Delta R_{1a}$, $R_{2a} = 7\Delta R_{2e}$, $R_{1c} = R_{10b}$

$$G_{20} = \frac{R_{2b}}{R_{1a} + R_{1b}}, G_{10} = \frac{R_{2a} + R_{2b}}{R_{1a} + R_{1c}} \tag{2.12}$$

Considering resistor variations due to random mismatch, G_2 and G_1 are

$$G_2 = \frac{R_{2b} + \delta R_{2b}}{R_{1a} + R_{1b} + \delta R_{1a} + \delta R_{1b}}, G_1 = \frac{R_{2a} + R_{2b} + \delta R_{2a} + \delta R_{2b}}{R_{1a} + R_{1c} + \delta R_{1a} + \delta R_{1c}} \tag{2.13}$$

where R_{2a}, R_{2b}, R_{1a}, R_{1b}, and R_{1c} are the nominal values and δR_{2a}, δR_{2b}, δR_{1a}, δR_{1b}, δR_{1c} are the respective resistor variations due to random mismatch. Substituting G_1 and G_2 in (G_2/G_1) and simplifying we get

$$\frac{G_2}{G_1} = A_1 A_2 \tag{2.14}$$

$$A_1 = \frac{R_{2b}}{R_{2a} + R_{2b}} \left(1 + \frac{R_{2a}}{R_{2a} + R_{2b}} \left(\frac{\delta R_{2b}}{R_{2b}} - \frac{\delta R_{2a}}{R_{2a}}\right)\right) \tag{2.15}$$

$$\begin{aligned} A_2 \;=\; & \frac{R_{1a} + R_{1c}}{R_{1a} + R_{1b}} \left(1 + \frac{R_{1a}(R_{1b} - R_{1c})}{(R_{1a} + R_{1b})(R_{1a} + R_{1c})} \left(\frac{\delta R_{1a}}{R_{1a}}\right)\right) \\ & + \frac{R_{1c}}{R_{1a} + R_{1b}} \left(\frac{\delta R_{1c}}{R_{1c}}\right) - \frac{R_{1b}(R_{1a} + R_{1c})}{(R_{1a} + R_{1b})^2} \left(\frac{\delta R_{1b}}{R_{1b}}\right) \end{aligned} \tag{2.16}$$

$$\sigma^2\left(\frac{G_2}{G_1}\right) = A\left(\sigma^2\left(\frac{\delta R_{2b}}{R_{2b}}\right)+\sigma^2\left(\frac{\delta R_{2a}}{R_{2a}}\right)\right)+B\sigma^2\left(\frac{\delta R_{1a}}{R_{1a}}\right)+C\sigma^2\left(\frac{\delta R_{1c}}{R_{1c}}\right) +D\sigma^2\left(\frac{\delta R_{1b}}{R_{1b}}\right) \tag{2.17}$$

$$\begin{aligned} A &= \frac{R_{2a}^2R_{2b}^2(R_{1a}+R_{1c})^2}{(R_{2a}+R_{2b})^4(R_{1a}+R_{1b})^2} \\ B &= \frac{R_{1a}^2(R_{1b}-R_{1c})^2R_{2b}^2}{(R_{1a}+R_{1b})^4(R_{2a}+R_{2b})^2} \\ C &= \frac{R_{1c}^2R_{2b}^2}{(R_{1a}+R_{1b})^2(R_{2a}+R_{2b})^2} \\ D &= \frac{R_{1b}^2R_{2b}^2(R_{1a}+R_{1c})^2}{(R_{1a}+R_{1b})^4(R_{2a}+R_{2b})^2} \end{aligned} \tag{2.18}$$

Substituting the resistors and their variance values, $(G_2/G_1)_{min} = 0.21\,dB$. Similarly, for 0.5 dB increment in the gain at every 4 dB gain interval we ensure, $(G_2/G_1)_{min} > 0\,dB$. Within a 4 dB gain interval, R_2 is decreased and R_1 is increased as given by (2.9) for 0.5 dB gain decrement. This will definitely decrease the gain and hence maintain monotonicity within the 4 dB gain interval.

2.4 Complete PGA architecture

The hearing aid requirement is to accept two different inputs, one from the microphone, and other from the telecoil. One way is to put a multiplexer before the PGA to select one of the two inputs. Since an analog multiplexer is implemented using switches, the V_{GS} of the switches will be equal to the input signal swing. This modulates the ON resistance of the switch increasing the distortion. In order to avoid this, the switches are inserted near the input terminal of the op-amp as shown in Fig. 2.14. Since the input terminal of the op-amp sees a voltage swing given by 2.3, the V_{GS} of the switches will be reduced decreasing the distortion.
An additional input resistor bank (R_1) is used. Using the switches S_1 and S_2 at

the vip input terminal of the op-amp, the user can switch between the two inputs. At a time, only one of the inputs will be amplified by the PGA. To maintain the differential nature of the circuit, switches S_3, S_4 and S_7 are used at the vim input terminal of the op-amp. The complementary control signals a, ā for the switches can be generated by the DSP. Additional switches S_5, S_6 are used to reduce the V_{DS} of the switches S_1, S_2, respectively when they are OFF. This is to avoid degrading the distortion performance of the PGA when both the microphone and telecoil inputs are active.

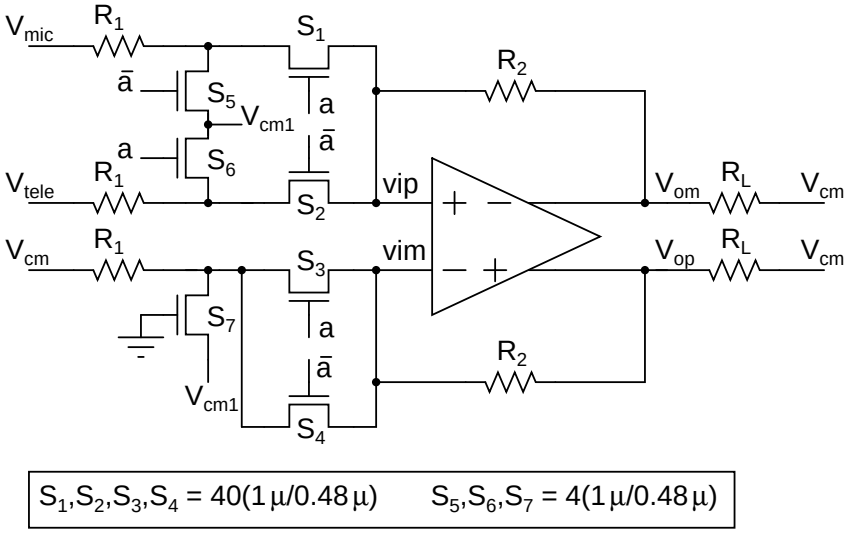


Figure 2.14: Complete PGA architecture.

2.5 Simulation results

The PGA is simulated for measuring its distortion and noise performance in the 10 kHz bandwidth for various gain settings. The input is given to the V_{mic} node, while the V_{tele} node is at V_{cm}. Table 2.4 shows the simulated results. Fig. 2.15 shows the power spectral density (PSD) of the PGA output for the gain of -1 dB for an input amplitude of 450 $\mathrm{mV_p}$ and a frequency of 1.25 kHz.

Table 2.4: THD and input noise in 10 kHz bandwidth.

Input amplitude (mV_p)	**Gain (dB)**	**THD (dB)**	**Input referred noise (μV_{rms})**
4	40	-82.3	2.1
7.11	35	-82	2.56
12.65	30	-82.2	3.24
22.5	25	-81	4.2
40	20	-83.1	6.1
71.1	15	-83.8	8.13
126.5	10	-78.2	8.8
225	5	-79.5	10
450	-1	-84	11

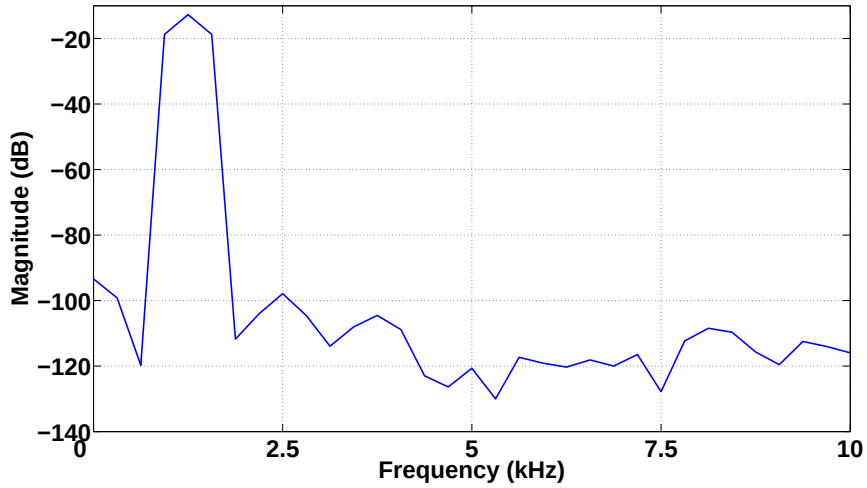


Figure 2.15: PSD of the PGA output for 450 mV_p input.

2.6 Automatic Gain Control

An AGC loop is used to provide coarse gain control in the PGA. The AGC is used to prevent a steady state input up to the defined PGA limit from being clipped[5]. If the input level is higher than the defined PGA upper limit of 450 mV_p, the AGC will set the PGA gain to -1 dB. If the input level is smaller than the defined PGA lower limit of 4 mV_p, the AGC will set the PGA gain to 40 dB. For input levels between the lower and the upper PGA limit, the AGC will set the PGA gain to give an output voltage between 283 $mV_{p,d}$ and 400 $mV_{p,d}$.

The AGC comprises of a peak detector which senses the peak output voltage of the PGA. This peak voltage is then compared with the two references, 800 mV

and 741 mV, using an op-amp based comparator. The output of the comparators control a seven bit up-down counter, which counts up if the input level is higher than 800 mV, and counts down if the input level is lower than 741 mV. The counter is disabled when the input is between 800 mV and 741 mV. Initially the AGC is reset and the gain is set to 0 dB. As the counter counts up, the PGA gain decreases by 0.5 dB on every count, and as the counter counts down, the PGA gain increases by 0.5 dB on every count. This continues till the PGA output settles between 283 $mV_{p,d}$ and 400 $mV_{p,d}$. Fig. 2.16 shows the block diagram of the AGC loop. The counter operates at a clock frequency of 160 kHz.

The peak detector circuit is shown in Fig. 2.17. The diode will pass only the

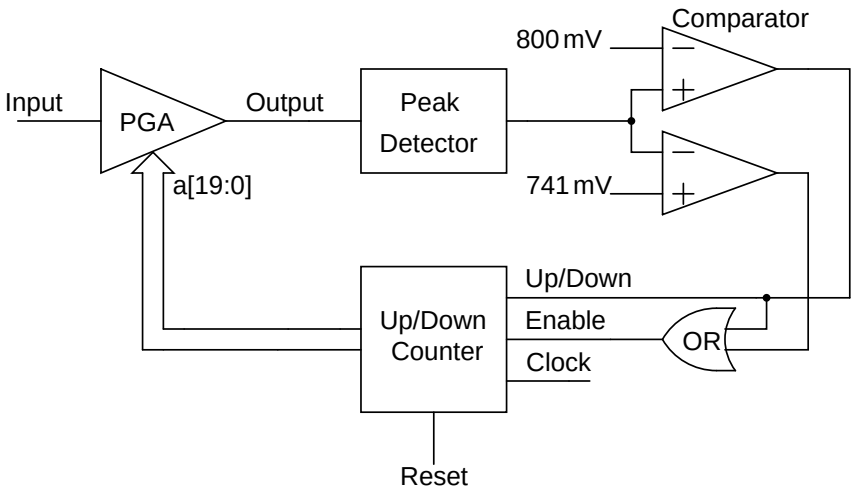


Figure 2.16: AGC block diagram.

positive input cycle to the output and the capacitor will get charged to the peak input voltage. The transistor M0 acts as a switch controlled by the clock. The clock frequency is 78 Hz, so that the circuit can detect the lowest frequency signal of 100 Hz. When the switch is OFF, the input peak is detected and the AGC loop changes the PGA gain accordingly. When the switch is ON, the capacitor voltage is held at V_{cm}, and the counter retains its previous count. The schematic of the comparator is shown in Fig. 2.18.

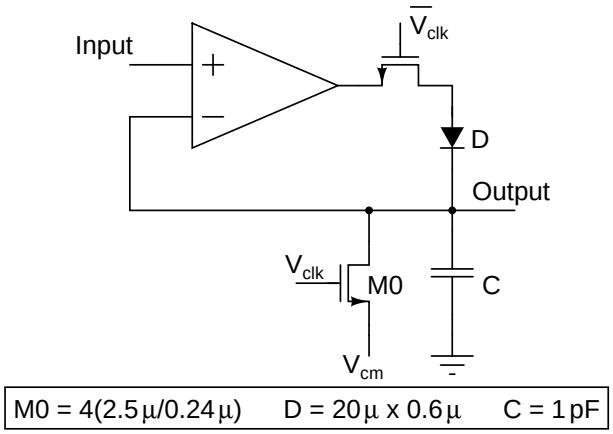


Figure 2.17: Peak detector circuit diagram.

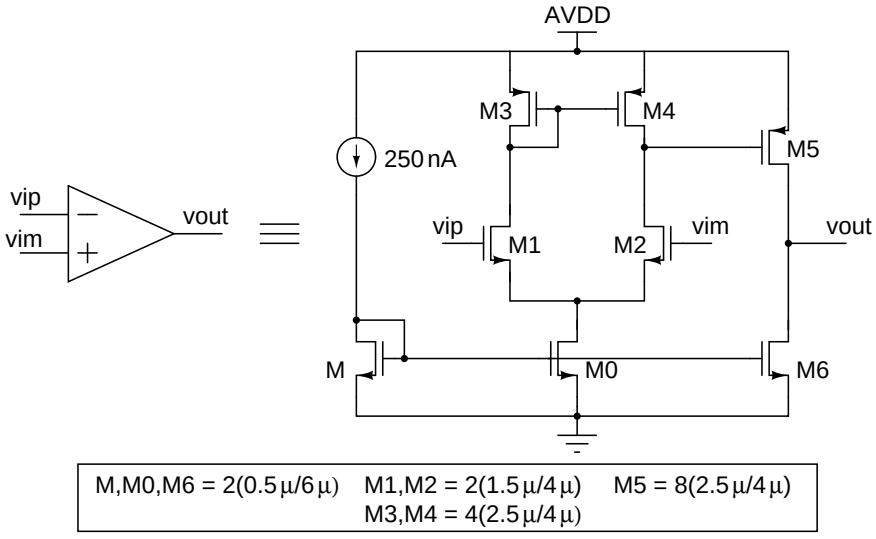


Figure 2.18: Comparator schematic.

Three different input amplitudes of 1 mV_p, 100 mV_p, and 500 mV_p and a frequency of 1 kHz are given as inputs to the PGA and the gain set by the AGC is calculated. The single ended PGA output voltages are shown in Fig. 2.19. The output settles to the expected final value after initial transients. Table 2.5 shows the calculated gain.

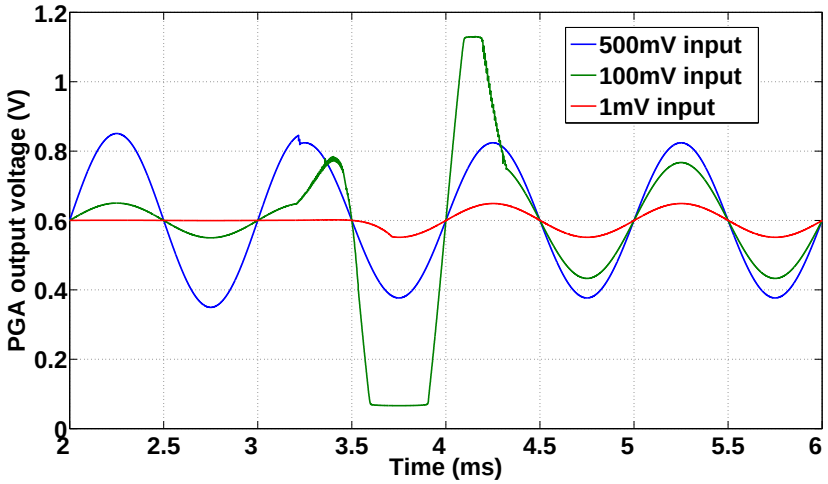


Figure 2.19: Single ended PGA outputs using AGC.

Table 2.5: Simulation results using AGC.

Input amplitude (mV_p)	**Output amplitude ($mV_{p,d}$)**	**Gain (dB)**
1	98	39.8
100	334	10.5
500	448	-0.95

CHAPTER 3

Decimation Filter

3.1 Introduction

The PGA output is converted into digital data by the $\Delta\Sigma$ ADC. The $\Delta\Sigma$ ADC provides a high dynamic range which is an essential requirement of an audio system. The output of the $\Delta\Sigma$ ADC is input plus shaped quantization noise. Decimation filter removes the shaped quantization noise to get a high dynamic range. Before decimation, the signal is digitally lowpass filtered to prevent aliasing of the quantization noise. The block diagram of a decimator for the $\Delta\Sigma$ ADC is shown in Fig. 3.1. Table 3.1 shows the design specifications of the decimation filter.

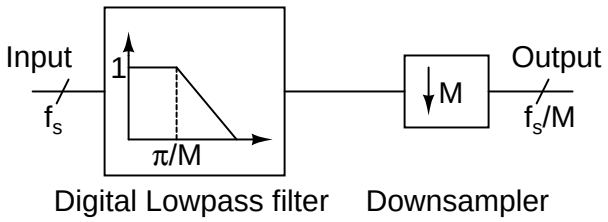


Figure 3.1: Decimation filter block diagram.

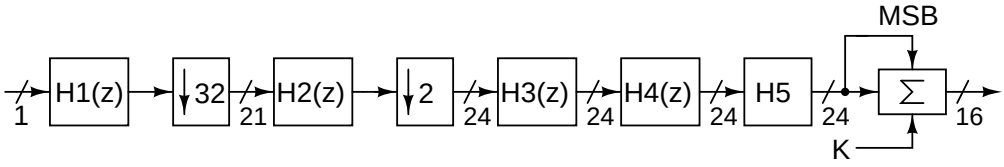
Table 3.1: Design specifications.

Sampling Rate	2.56 MHz
Input bits	1
Downsampling factor	64
Output rate	40 kHz
Output bits	16
Process/Supply voltage	130 nm CMOS/1.2 V

3.2 Multistage decimation

The digital lowpass filter required for decimation should have a narrow transition band. If this filter is realized in a single stage, followed by downsampling, the order of the filter required will be very high (>1000)[6]. A high order filter operating at a high sampling rate consumes a very high power. When a signal of bandwidth f_b is downsampled from a sampling rate of f_s to f_s/M, the aliasing region is from $kf_s/M - f_b$ to $kf_s/M + f_b$, where k is an integer. Downsampling in multiple stages, with appropriate decimation factor at each stage ensuring that aliasing noise in that particular stage is negligible, provides efficient decimation. This is called multistage decimation[6]. Fig. 3.2 shows the architecture of the decimation filter.

The overall downsampling factor of sixty-four is realized in two stages as thirty-two, and two. The first stage filter is a cascade of four SINC filters before downsampling by thirty-two. It operates at f_s. A SINC filter can be implemented using only adders (without multipliers) and helps in reducing the power. The remaining downsampling by two is done after lowpass filtering by a halfband filter. The FIR lowpass filter is used to remove the noise in the frequency band of 10 kHz to 20 kHz. The IIR highpass filter is used to remove the dc offset. The scaling block restores the signal to the full scale of the $\Delta\Sigma$ ADC. Each block implementation is described in the following sections of this chapter.



H1(z) - SINC4 filter H2(z) - Halfband filter H5 - Scaling Block
H3(z) - FIR lowpass filter H4(z) - IIR highpass filter

Figure 3.2: Decimation filter architecture.

3.3 Decimation filter architecture

3.3.1 SINC4 filter

These filters do lowpass filtering by taking average of N samples. The transfer function of the SINC4 filter is

$$H1(z) = \left[1 + z^{-1} + z^{-2} + z^{-3} + ... + z^{-31}\right]^4 = \left[\frac{1 - z^{-32}}{1 - z^{-1}}\right]^4 \tag{3.1}$$

SINC filters have zeros at kf_s/N where k = 1,2,...N-1, and N is the number of samples taken for averaging. The noise in the bands which alias when downsampled by N are heavily attenuated because of these zeros. Here N=32. The signal is downsampled from 2.56 MHz to 80 kHz. A third order $\Delta\Sigma$ ADC shapes the quantization noise at its output as f^3. In order to provide sufficient attenuation of the shaped quantization noise, we use a cascade of 4 SINC filters, which has a $1/f^4$ roll-off[7].

The denominator of $H1(z)$ in (3.1) is implemented as cascade of accumulators. The numerator is implemented as cascade of differentiators with the downsampling and the delay element exchanged. This structure is called the Hogenauer structure or Cascaded Integrator Comb (CIC) structure[8]. Fig. 3.3 shows this structure. The accumulators are retimed by shifting the delay element from the feedback path to the forward path[9]. Hence the glitches in combinational adders in one accumulator are prevented from propagating to the next accumulator, thereby reducing unwanted switching power[10]. The pipelining register at the output of the fourth accumulator prevents the data at f_s propagating through the differentiators. This structure helps in reducing the power because the differentiators operate at a relatively lower frequency of 80 kHz than the accumulators (2.56 MHz). Fig. 3.4 shows the implementation of the SINC4 filter.

The accumulator adds the previous state value with its current input and can result in an overflow.The width of all the registers in the SINC4 filter is chosen

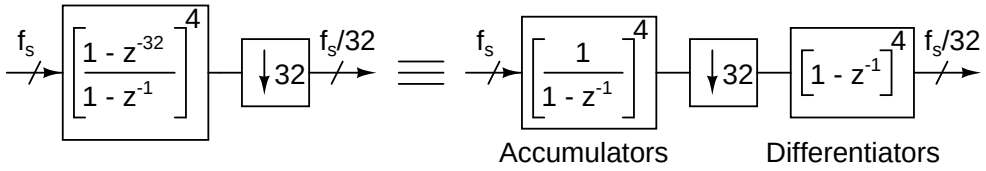


Figure 3.3: Hogenauer structure.

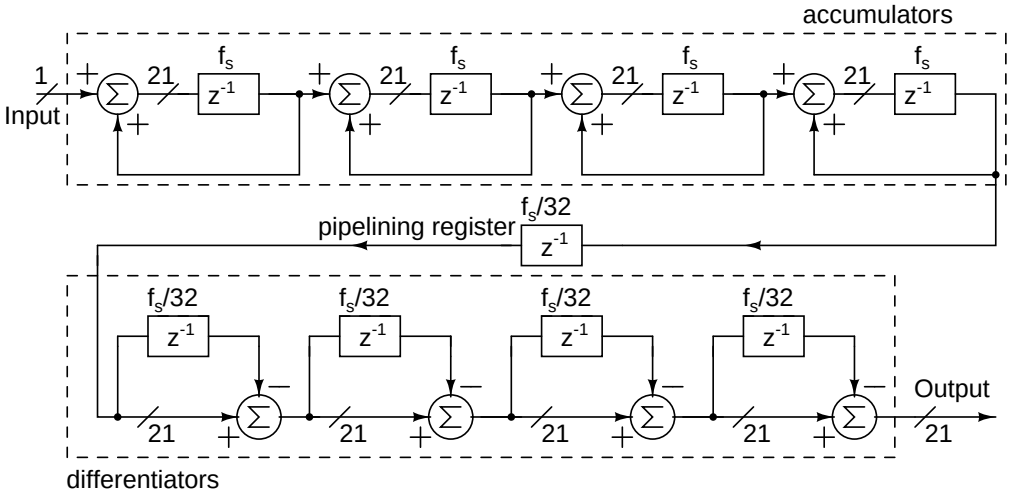


Figure 3.4: SINC4 filter implementation.

according to[8] as $B_{in} + k \log_2 N = 21$, where, B_{in} = input data bit width = 1, k = No. of SINC filters in cascade = 4, N = No. of averaging samples = 32.

The $\Delta\Sigma$ ADC output swings on either side of its dc value, i.e., 1 and -1. But its output is coded in one bit binary as 0 and 1. Thus there is a dc offset of 0.5. The value to be subtracted from the output of the SINC filter = 0.5 * dc gain of SINC4 =0.5 * 32^4. This subtraction is done within the SINC4 filter itself. Thus after the subtraction, the output of the SINC4 filter should be interpreted with two's complement arithmetic. The magnitude response of the SINC4 filter is shown in Fig. 3.5.

3.3.2 Halfband filter

Halfband filters are a class of equiripple FIR filters with order N=4P+2, where P=1,2,3..[10]. Alternate coefficients are zero except the middle one. This reduces the number of multiplications required. The middle coefficient is 0.5. Halfband filters have their -6 dB frequency at $f_s/4$ where f_s is the sampling rate of the

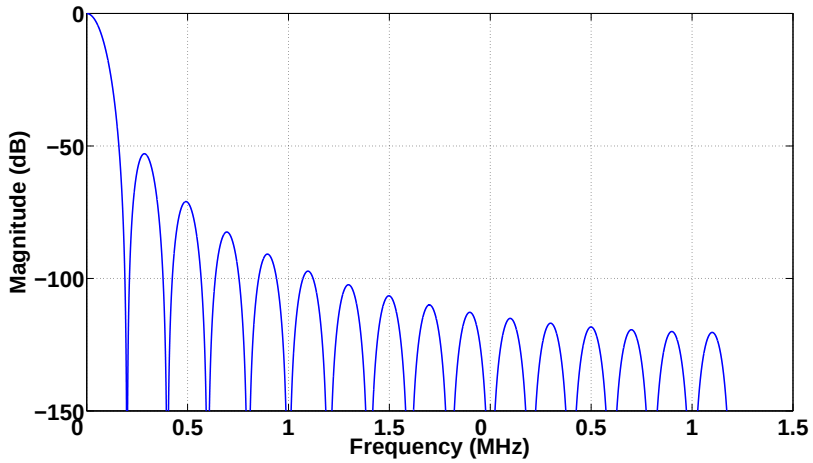


Figure 3.5: SINC4 filter magnitude response.

filter. Hence the maximum downsampling factor that is allowed after filtering is two[10]. The input of the halfband filter comes from the SINC4 filter at 80 kHz. The output of the halfband filter is at 40 kHz. The noise that aliases to the in-band when downsampled by a factor of two lies in the band 30 kHz to 40 kHz. The passband edge is kept at 20 kHz.

The coefficients should be encoded in a particular format to minimize the power dissipation. Encoding a binary number in signed digit representation such that it contains the least number of non-zero bits is called canonic signed digit (CSD) [11]. CSD implementation minimizes the number of multiplications and hence the power dissipation. For example $7 = 2^3$ - 2^0 instead of $2^2 + 2^1 + 2^0$. Fig. 3.6 shows the magnitude response of the filter. A tenth order filter is chosen so that it sufficiently attenuates the aliasing noise. The stopband attenuation is around 60 dB.

Halfband filter is implemented as a polyphase structure. The data stream is split into two phases. The filter transfer function is also split into two parts and each transfer function operates on each phase of the signal. Outputs from these phases are added to get the filtered and downsampled signal. Each phase operates at a reduced rate thus reducing the effective sampling rate of the filter. This reduces the power consumption. $H2(z)$ is the filter transfer function and the downsampling

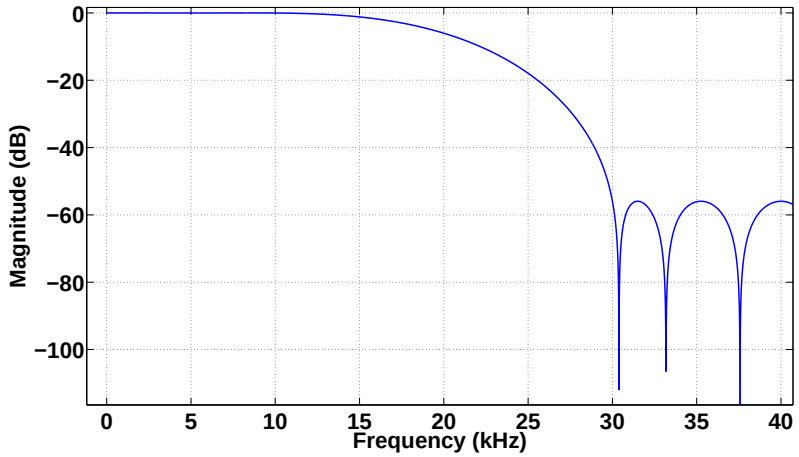


Figure 3.6: Halfband filter magnitude response.

factor is two. $H2(z)$ is represented as

$$H2(z) = \sum_{i=0}^{10} a_i z^{-i} \tag{3.2}$$

This transfer function is split into two phases as given by

$$\begin{aligned} H2(z) &= a_0 + a_2 z^{-2} + a_4 z^{-4} + a_6 z^{-6} + a_8 z^{-8} + a_{10} z^{-10} + \\ &\quad z^{-1}(a_1 + a_3 z^{-2} + a_5 z^{-4} + a_7 z^{-6} + a_9 z^{-8}) \\ &= H_e(z) + z^{-1} H_o(z) \end{aligned}$$

The original transfer function $H2(z)$ is split into even $H_e(z)$ phase and odd phase $H_o(z)$. The polyphase structure used in the halfband filter is shown in Fig. 3.7. The downsampling and filtering are interchanged. So the transfer function $H_e(z)$ becomes $H_e(z^{1/2})$ and $H_o(z)$ becomes $H_o(z^{1/2})$.

$$\begin{aligned} H_e(z^{1/2}) &= a_0 + a_2 z^{-1} + a_4 z^{-2} + a_6 z^{-3} + a_8 z^{-4} + a_{10} z^{-5} \\ &= a_0(1 + z^{-5}) + a_2 z^{-1}(1 + z^{-3}) + a_4 z^{-2}(1 + z^{-1}) \\ H_o(z^{1/2}) &= (a_1 + a_3 z^{-1} + a_5 z^{-2} + a_7 z^{-3} + a_9 z^{-4}) = a_5 z^{-2} \end{aligned}$$

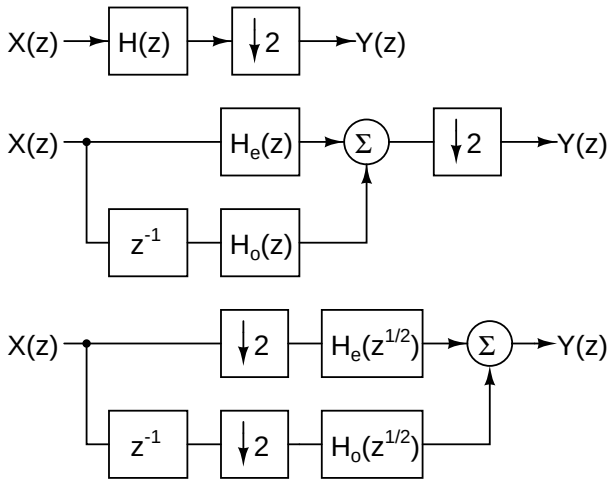


Figure 3.7: Polyphase structure in the halfband filter.

where, $a_0 = a_{10}, a_2 = a_8, a_4 = a_6$, $a_1 = a_3 = a_7 = a_9 = 0$, and $a_5 = 0.5$. Implementation of the filter and its internal state representation is shown in Fig. 3.8 and Fig. 3.9 respectively.

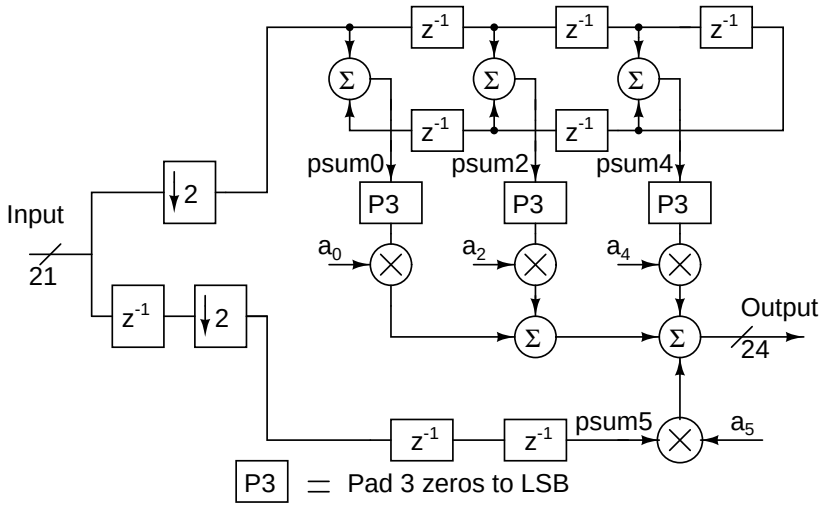


Figure 3.8: Polyphase implementation of the halfband filter.

The P3 block pads three least significant bit (LSB) zeros to the data to increase the dynamic range to 24 bits. The output of the filter is a weighted addition of the internal states psum0, psum2, psum4, and psum5. The tap weights are less than unity, and are expanded in the powers of 2^{-1} in the CSD format. A 2^{-m} in the tap weight corresponds to right shifting the signal by dropping its m LSB. Hence a tap weight multiplication is obtained by adding and subtracting the right shifted signals. This multiplication is further nested based on Horner's rule[12].

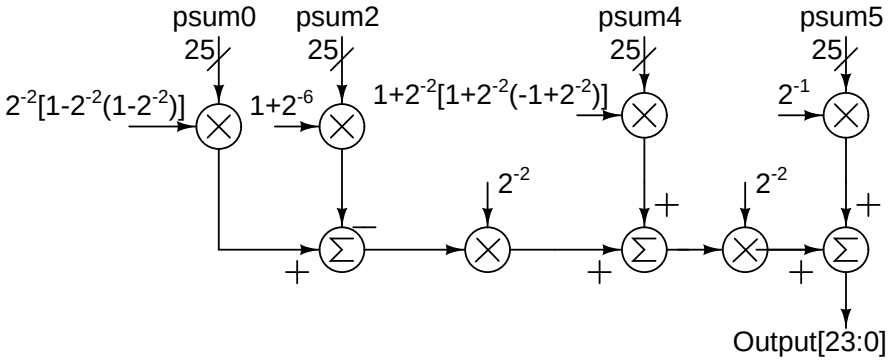


Figure 3.9: Internal state representation of the halfband filter.

This reduces the effective right shift operation and hence the effect of truncation noise[10]. For e.g. $2^{-2} - 2^{-4} + 2^{-6} = 2^{-2}[1 - 2^{-2}(1 - 2^{-2})]]$.

The digital signal should have adequate dynamic range to suppress the quantization noise[10]. The dynamic range of the filtered signal is proportional to the number of bits used in filtering. Every bit gives 6 dB more dynamic range. It is found that a 48 dB attenuation of aliasing noise (with respect to the in-band noise floor) is sufficient to preserve the in-band SNR[10]. So, the internal states of the filter are represented with eight extra bits than the signal in-band resolution of 16 bits. The number of bits used for the register width are 24.

3.3.3 FIR lowpass filter

Lowpass filtering is done with 10 kHz bandwidth. But since the output rate is 40 kHz, downsampling is not done to the Nyquist rate of 20 kHz. To get a 60 dB stopband attenuation, a thirty-sixth order FIR filter with the passband edge at 11.4 kHz is used. These specifications are chosen for the droop of the overall filter at 10 kHz to be 1.2 dB, and noise in 10 kHz to 20 kHz is sufficiently low to preserve the in-band SNR. The coefficients are encoded in the CSD format as done for the halfband filter coefficients. The coefficients are symmetric about the middle coefficient. Fig. 3.10 shows the Direct-Form-I implementation of the FIR filter. Fig. 3.11 shows the magnitude response of the FIR filter.

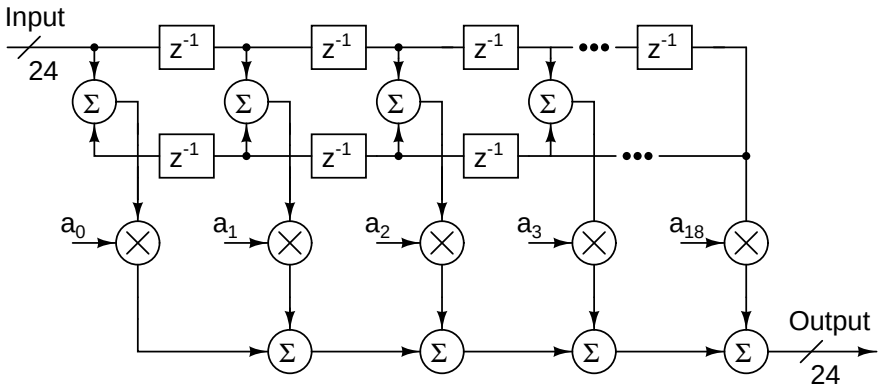


Figure 3.10: FIR filter implementation.

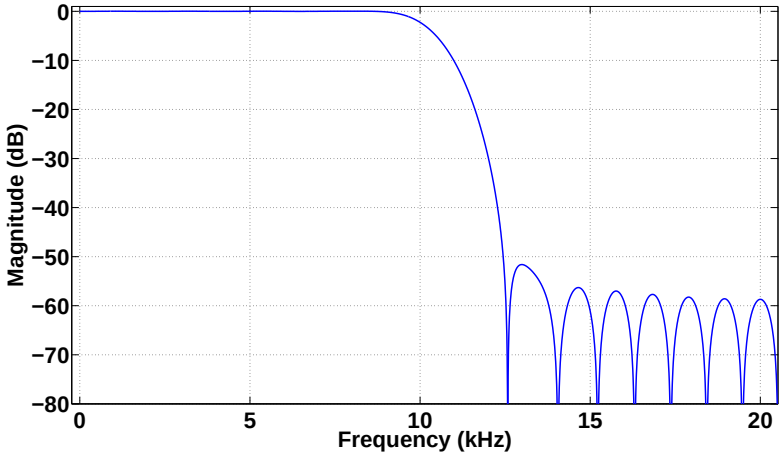


Figure 3.11: FIR filter magnitude response.

3.3.4 IIR highpass filter

In order to remove the dc offset introduced by the frontend, a first order Butterworth highpass filter is used. It has programmable cut-off frequencies of 50 Hz and 100 Hz. There is also a mode in which the highpass filter is disabled. The default mode is 50 Hz cut-off frequency. The cut-off frequency is decided by the two bits of a digital input signal ctrl[1:0] (generated by DSP) as shown in the Table 3.2. The transfer function of the first order Butterworth IIR highpass filter with 50 Hz

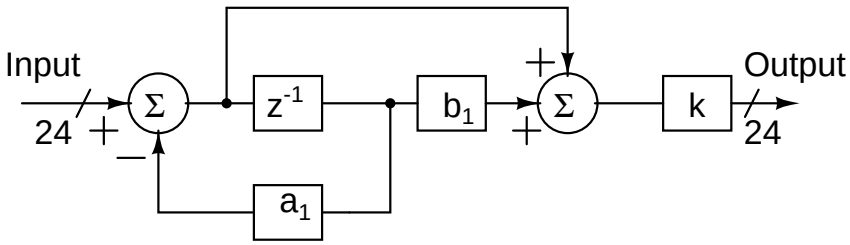
Table 3.2: Programming cut-off frequencies of IIR filter.

ctrl[1]	ctrl[0]	Cut-off frequency
0	0	50 Hz
0	1	bypass mode
1	0	100 Hz
1	1	50 Hz

cut-off frequency is

$$H4(z) = \frac{0.9961(1 - z^{-1})}{1 - 0.9922z^{-1}} \tag{3.3}$$

Fig. 3.12 and Fig. 3.13 shows the Direct-Form-I implementation and the magnitude respose of the IIR filter with 50 Hz cut-off frequency, respectively.



b_1=-1, a_1=-0.9922,
k=0.9961

Figure 3.12: IIR filter block diagram.

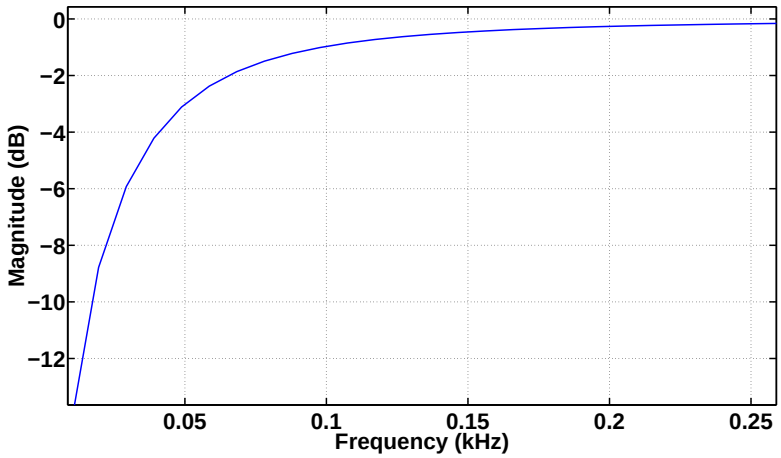


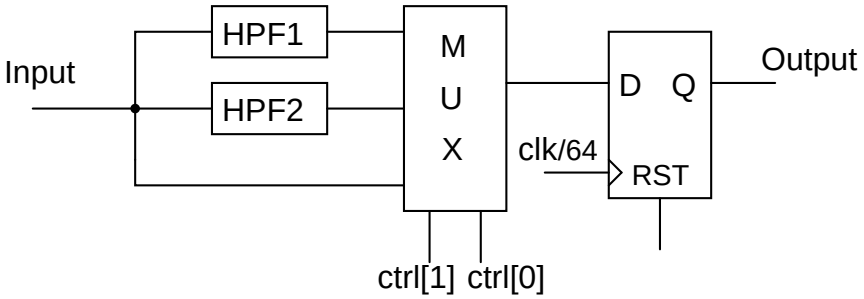
Figure 3.13: IIR filter magnitude response with 50 Hz cut-off.

The transfer function of the first order Butterworth IIR highpass filter with the cut-off frequency of 100 Hz is

$$H4(z) = \frac{0.9922(1 - z^{-1})}{1 - 0.9844z^{-1}} \tag{3.4}$$

It is implemented in a similar way as shown in Fig. 3.12. Fig. 3.14 shows how the different modes are implemented in the highpass filter. Two control signals

ctrl[1:0] select one of the three inputs of the multiplexer (MUX) to be its output, thus giving different highpass cut-off frequencies.



HPF1 - Highpass filter with 50 Hz cut-off frequency
HPF2 - Highpass filter with 100 Hz cut-off frequency

Figure 3.14: Implementation of the modes in the highpass filter.

3.3.5 Scaling block

The input signal to the $\Delta\Sigma$ ADC is not at full-scale of the quantizer because of the maximum stable amplitude (MSA). For the $\Delta\Sigma$ ADC used, the MSA is 70 %. The signal should be restored to its full swing after filtering the high frequency noise to get the peak SNR at the decimator output. Ideally, the required scaling number here is 1/0.35. But some margin should be kept to avoid overflow. The margin is determined by trial and error by giving a tone at various frequencies and ensuring that there is no overflow in the complete filter structure. When the swings are maximized, the round-off noise decreases. The scaling number is chosen to be

$$\frac{1}{0.36} = 3 + 2^{-2}\{-1 + 2^{-3}[1 + 2^{-3}\{-1 + 2^{-3}(1 - 2^{-3})\}]\} \tag{3.5}$$

3.3.6 Truncation block

The required signal resolution is 16 bits. Hence there is a need to truncate the 24 bit scaled output signal to 16 bits. Conventional truncation of the binary signals involves discarding some of its LSB. This, when applied to two's complement numbers, produces an asymmetry between the positive and the negative truncated

numbers[13]. Truncation of the positive two's complement numbers produces numbers which tend towards zero whereas truncation of the negative two's complement numbers produces numbers which tend towards more negative numbers. This introduces an undesirable dc component in the truncated signal.

The truncation block adds the 24 bit two's complement signal, its MSB and an integer K, where $K = 2^{N-1} - 1$, N = Number of LSB to be dropped[13]. The sum is truncated by dropping 8 LSB to produce a symmetrically rounded 16 bit output signal. For example, we want to truncate two numbers M and $-M$, represented by P bits in two's complement, to Q bits by dropping its $P - Q$ LSB. This will produce $\left\lfloor \frac{M}{2^{P-Q}} \right\rfloor = A$ and $\left\lfloor \frac{-M}{2^{P-Q}} \right\rfloor = -A - 1$, respectively. Instead, if we add the individual numbers, with their respective MSB and an integer $K = 2^{P-Q-1} - 1$, we get $\left\lfloor \frac{M+0+2^{P-Q-1}-1}{2^{P-Q}} \right\rfloor = A$ and $\left\lfloor \frac{-M+1+2^{P-Q-1}-1}{2^{P-Q}} \right\rfloor = -A$, respectively.

3.4 Simulation results

The combined frequency response of the decimation filter is shown in Fig. 3.15. The spectrum at the output of the filter for a tone at 4.6875 kHz is shown in Fig.

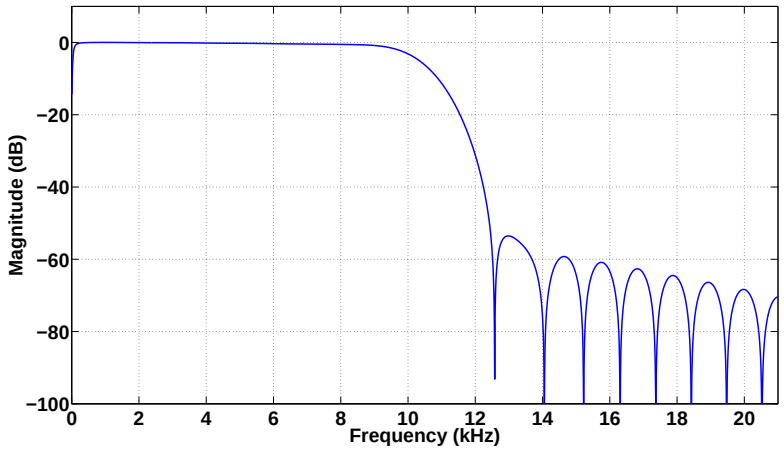


Figure 3.15: Complete Decimation filter magnitude response.

3.16. Tones at various frequencies are given as input to the filter and the output SNR and the swings are tabulated in Table 3.3. The power consumed by the

decimation filter is 6 μW.

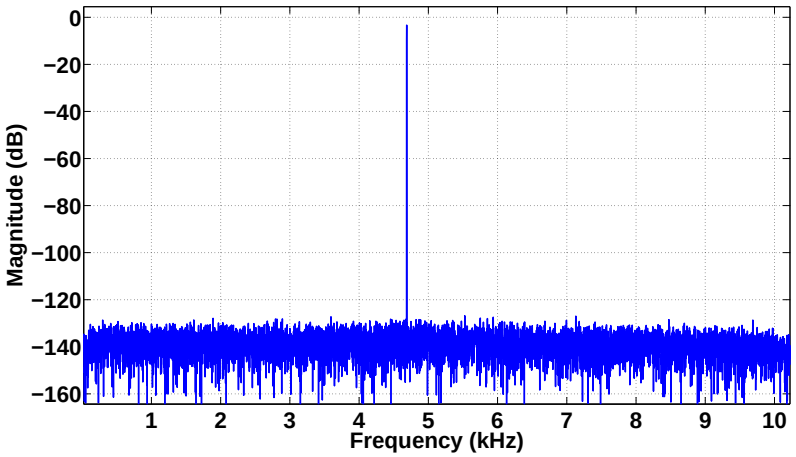


Figure 3.16: Decimation filter output spectrum.

Table 3.3: Simulation results of the decimation filter.

Input tone (kHz)	**Output SNR (dB)**	**Output Swing (V_p)**
0.234	94.1	0.9961
0.703	94.45	0.9906
1.172	94.32	0.9961
1.641	94.5	0.9945
3.203	95.2	0.9957
4.6875	96	0.9957
6.172	95.5	0.9967
7.578	95	0.9965
8.828	94.66	0.9956

3.5 Design flow

The complete decimation filter design is done using automated CAD tools. The hardware circuit implementation of the filter is done in 130 nm CMOS technology with low-leakage (LL) Faraday-Library cells. Table 3.4 shows the various tools used in designing the decimator. Using MATLAB, the filter order and coefficients are modelled. The decimation filter function is coded in verilog with the required bit precision as mentioned in the earlier part. The verilog code is converted to gate-level netlist using Design Compiler. This is known as synthesis. All the

Table 3.4: CAD tools for the decimator design.

Tools	**Purpose**
MATLAB	Filter design
Modelsim	Simulation
Design Compiler	Synthesis
SoC Encounter	Place and Route

design constraints such as the load capacitance, area, frequency of operation and delay are given during this synthesis. After this, place and route is done for[10]

- Placing the standard cells according to the floor plan
- Clock Tree Synthesis (CTS)
- Routing the design to meet the timing requirements

It is ensured that there are no timing violations after place and route. With the annotation of interconnect delays, simulation is done to verify SNR performance.

CHAPTER 4

Ring Oscillator

4.1 Introduction

The minimum number of inverters required in a ring oscillator is three. A three stage ring oscillator is shown in Fig. 4.1. The waveform at the output of each inverter is also shown in the same figure. It is assumed that all the inverters have equal rise and fall times = t_d. The time period of oscillation is $6t_d$, and the frequency is $1/(6t_d)$. This ring oscillator's frequency varies significantly with

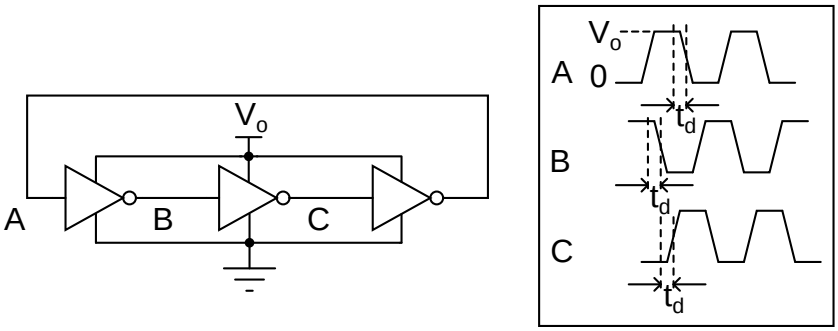


Figure 4.1: Three stage ring oscillator.

process, voltage and temperature variations. So, a current-starved inverter based ring oscillator is utilized, in which the frequency of oscillation can be controlled by the current I_o. The architecture is shown in Fig. 4.2. It utilizes current sources at the top and the bottom to improve PSRR. The time period of the first-half cycle is $2t_f + t_r$, while that of the second-half cycle is $2t_r + t_f$, where t_r, t_f are the inverter's rise and fall time, respectively. Thus, the total time period is $3(t_r + t_f)$ giving an oscillation frequency of

$$f = \frac{1}{3(t_r + t_f)} \tag{4.1}$$

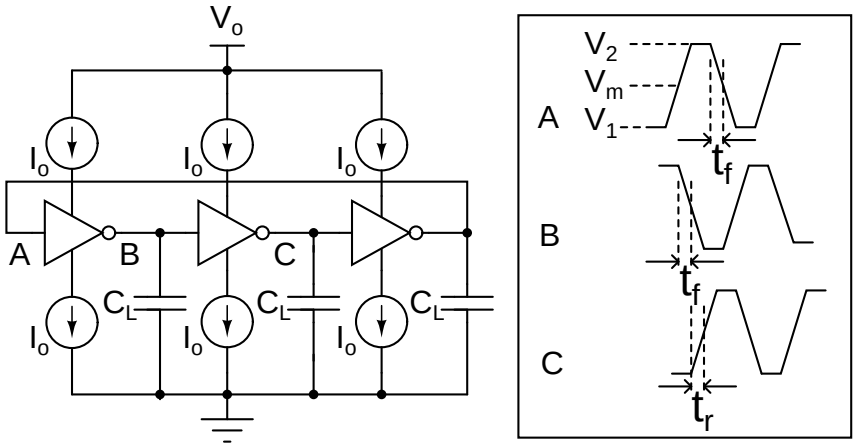


Figure 4.2: Ring oscillator architecture.

The inverter's rise and fall times are decided by the charging and discharging time of the capacitor C_L at each of the nodes A, B, and C. Consider the first rising edge at node A and the corresponding falling edge at node B. In this phase, C_L is getting discharged from the voltage V_2 to the trip voltage V_m through a constant current source I_o in time t_f. The current through C_L is

$$I_o = C_L \frac{dV}{dt} = C_L \frac{\Delta V}{\Delta t} = C_L \frac{V_2 - V_m}{t_f} \tag{4.2}$$

$$t_f = \frac{C_L(V_2 - V_m)}{I_o} \tag{4.3}$$

During the charging phase of the capacitor C_L, the current through C_L is

$$I_o = C_L \frac{dV}{dt} = C_L \frac{\Delta V}{\Delta t} = C_L \frac{V_m - V_1}{t_r} \tag{4.4}$$

$$t_r = \frac{C_L(V_m - V_1)}{I_o} \tag{4.5}$$

Substituting the rise and fall time delays from (4.3) and (4.5) in (4.1), we get

$$f = \frac{I_o}{3C_L(V_2 - V_1)} \tag{4.6}$$

4.2 Current-starved ring oscillator

A three stage ring oscillator based on a current-starved inverter topology is designed to provide an internal clock for the ADC and the DAC. It is shown in Fig. 4.3. The voltage V_o is obtained from the LDO which will be described in the next

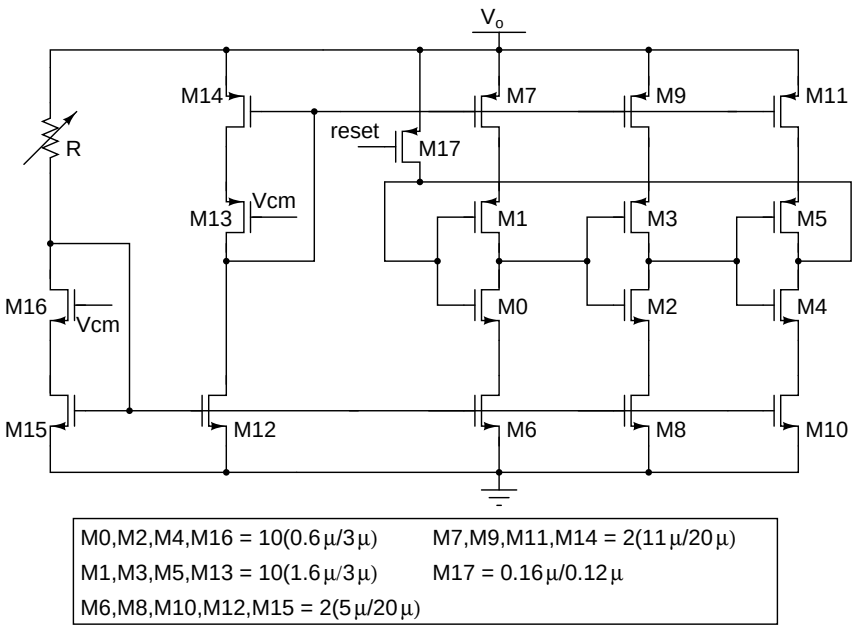


Figure 4.3: Current-starved ring oscillator schematic.

chapter. Transistors M0-M1, M2-M3, M4-M5 form the three inverters. These inverters are biased by the current sources M6-M11. Transistors M12-M16 form the biasing circuitry to provide the current I_o for each inverter stage. The inverters are sized so that the device parasitic capacitor itself acts as the load capacitor C_L. To reduce thermal and flicker noise of the current sources, their lengths are kept very large ($20\,\mu$m). M17 is used to provide start-up for the oscillator. The reset is obtained from a power-on reset (POR) block as explained in the next section. The frequency of oscillation is set to 20.48 MHz. The frequency varies from -16 % to 16 % with process and temperature variation (0^0 C $-$ 70^0 C). In order to keep the frequency constant, the current I_o needs to be tuned. This is done by varying the resistor R. From simulations across process and temperature, it is found that seven different values of R are required to reduce the frequency variation from -6 % to 6 %. The resistor values for different process corners are shown in Table 4.1. A

3-to-7 decoder is used to select one of the seven resistors. The resistor bank is shown in Fig. 4.4. A pMOS transistor M acting as a switch is kept in series with

Table 4.1: Resistor tuning in the ring oscillator.

Transistor corner	**Resistor corner**	**R** (kΩ)	**Frequency (MHz)**
TT	Rtyp	61.74	20.5
FF	Rtyp	64.3	20.54
TT	Rmin	76.3	20.47
FF	Rmin	78	20.5
TT	Rmax	51.3	20.56
FF	Rmax	54.8	20.52
SS	Rmax, Rmin, Rtyp	0.3	20

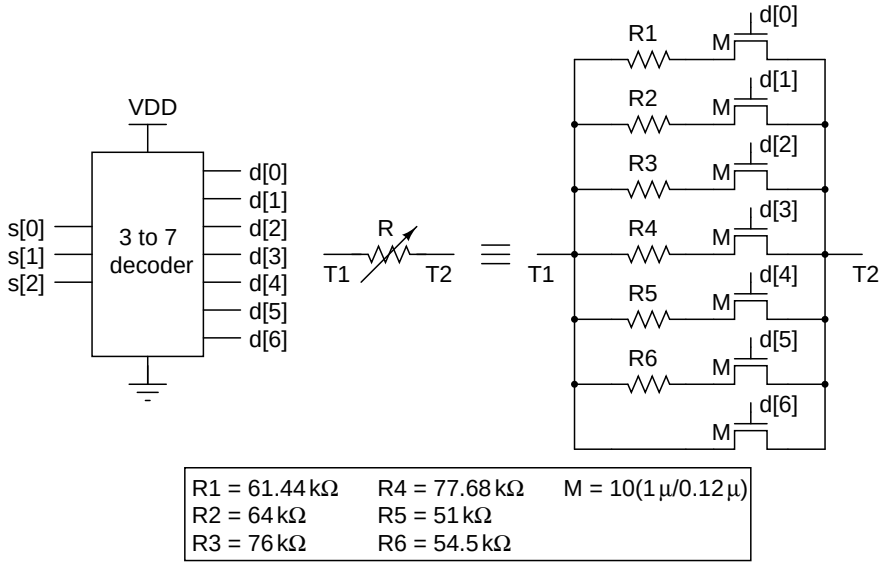


Figure 4.4: Resistor tuning in the oscillator.

each resistor. Monte Carlo analysis is done to see the effect of process variation and mismatch in the transistors on the oscillator frequency. Fig. 4.5 shows the histogram of the frequency for 100 runs. The 20.48 MHz clock is required for the digital backend. It is divided by eight to get a 2.56 MHz clock which is given to the $\Delta\Sigma$ ADC. Fig. 4.6 shows the circuit diagram of the frequency divider block made using D-flip flops. Table 4.2 shows the characteristics of the clock. Fig. 4.7 shows the phase noise contribution of the oscillator. Since the $\Delta\Sigma$ ADC is a single bit with the feedback DAC pulse of non-return-to zero (NRZ), it is very sensitive to clock jitter. The effect of oscillator's clock jitter on the $\Delta\Sigma$ ADC is analyzed in the next section.

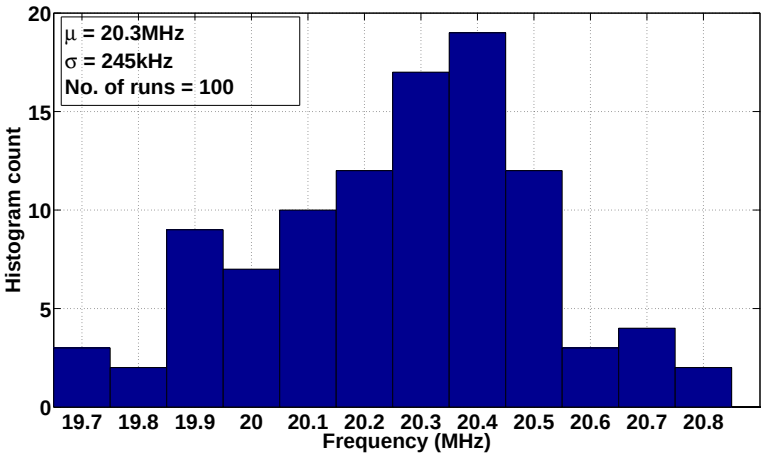


Figure 4.5: Histogram of frequency.

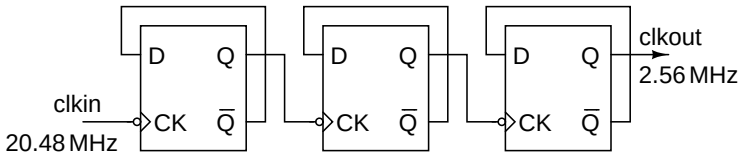


Figure 4.6: Clock divider.

Table 4.2: Clock characteristics.

Frequency	2.56 MHz
Phase noise at 1 MHz	-134 dBc/Hz
Period jitter	30 ps
Power	55 μW

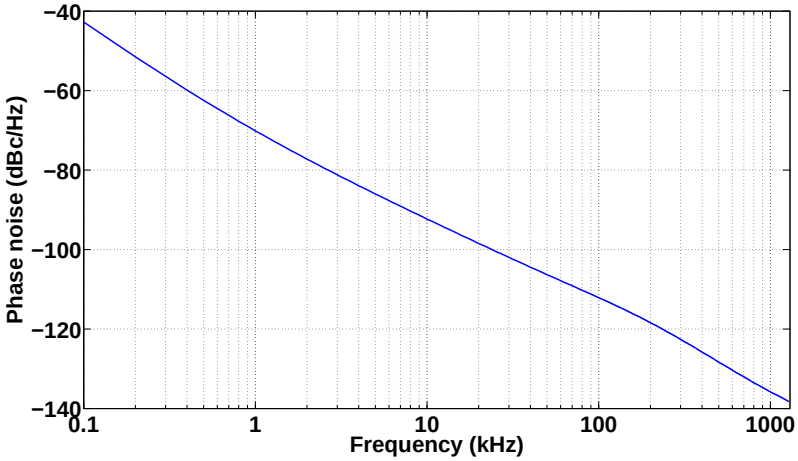


Figure 4.7: Phase noise spectral density($S_{\Delta t/T}(f)$) of the oscillator.

4.2.1 Clock jitter

The effect of the clock jitter in a $\Delta\Sigma$ ADC or a continuous time delta sigma modulator (CTDSM) is analyzed in this section. The block diagram of the CTDSM clocked by a jittery clock is shown in Fig. 4.8. The error due to the variation of the sampling instant of the ADC (e[n]) is noise shaped due to the high loop gain[15]. So, it does not contribute to the in-band noise floor. The error due to the variation of the width of the feedback DAC pulse ($e_1(t)$) is not noise shaped by the loop and adds directly at the input of the CTDSM[15]. This contributes to the in-band noise floor and can degrade the performance of the CTDSM.

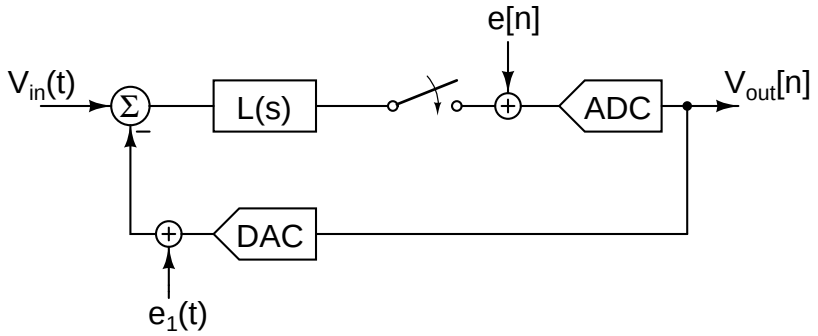


Figure 4.8: Clock jitter in the CTDSM.

For a feedback DAC pulse of NRZ, the error sequence $e_j[n]$ due to the clock jitter is [15]

$$e_j[n] = (y[n] - y[n-1])\frac{\Delta t[n]}{T} \tag{4.7}$$

where $y[n]$ is the n^{th} output sample of the CTDSM, T is the sampling period, and $\Delta t[n]$ is the clocking uncertainty of the n^{th} edge of the DAC pulse. $\Delta t[n]$ is not an independent identically distributed random variable. Its spectral density $S_{\Delta t/T}(f)$ is the phase noise spectral density of the current-starved ring oscillator. The spectral density of $y[n] - y[n-1]$ is $S_{dy}(f)$. The spectral density of $e_j[n]$ is

$$S_{ej}(f) = S_{dy}(f) * S_{\Delta t/T}(f) \tag{4.8}$$

where the convolution operation used here is circular in nature. Fig. 4.9 shows the plot of all the spectral densities. The in-band is from f_s to $f_s + f_s/(2 * OSR)$, where OSR is the oversampling ratio of the CTDSM. The in-band spectral density is shown zoomed-in in the same figure. The variance of $e_j[n]$ gives the total jitter noise power. The in-band noise power is calculated as

$$\sigma_{ej}{}^2 = \int_{f_s}^{f_s + \frac{f_s}{2*OSR}} S_{ej}(f)df \tag{4.9}$$

The jitter noise power $= 3.24 \times 10^{-10}\,\mathrm{V}^2$. So, for an input signal at the MSA of $0.7\,\mathrm{V_p}$, the signal to jitter noise ratio (SJNR) is 89 dB. whereas, for the ADC, SNDR = 87 dB[16]. Thus the oscillator is used in open loop itself instead of putting it in a PLL which would have further reduced the jitter.

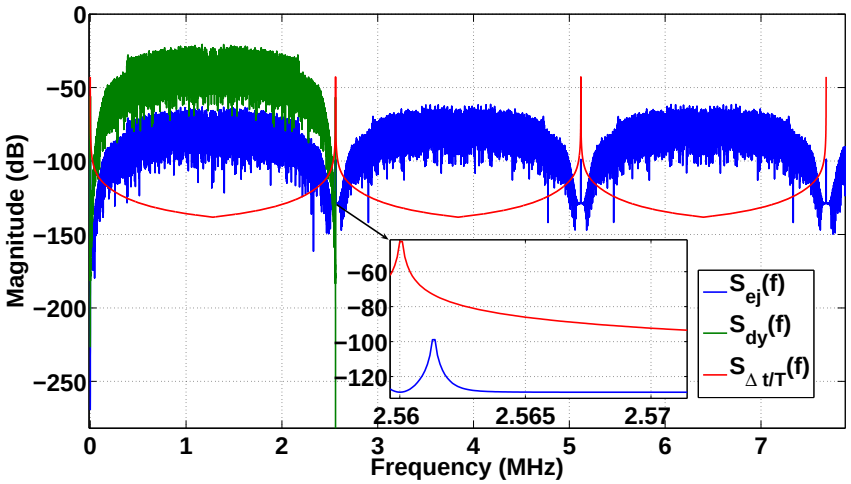


Figure 4.9: Spectral densities.

4.3 Power-On Reset

Power-on reset (POR) is used to provide an active-low reset signal to the hearing aid upon power-up. The supply voltage AVDD does not settle immediately after powering up. A typical time of 100 ms is assumed till the AVDD becomes stable after the switch bounce has settled. During this period, all the digital blocks

should be in reset mode. The POR block is shown in Fig. 4.10. The bandgap

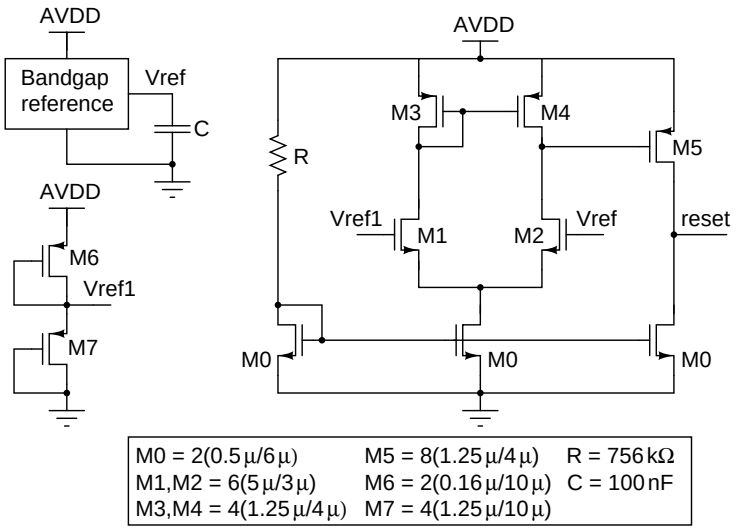


Figure 4.10: POR schematic.

output voltage is available on chip, and hence can be bypassed by a capacitor of high value to get a time constant of the order of 10 ms. Thus when the AVDD is ramping to 1.2 V, the bandgap output Vref will ramp to 0.6 V. The voltage Vref is compared to the potential divider output Vref1 = 0.4 V. Till the voltage Vref is less than Vref1, the POR will provide the active-low reset. When the voltage Vref becomes greater than Vref1, the reset is deactivated. If the voltage AVDD drops to 0 V, the reset voltage tracks the voltage AVDD thus asserting reset. Fig. 4.11 shows the simulated output at the various nodes of the POR block when the supply voltage AVDD is rising from 0 V to 1.2 V in 80 ms and falling again to 0 V in 80 ms.

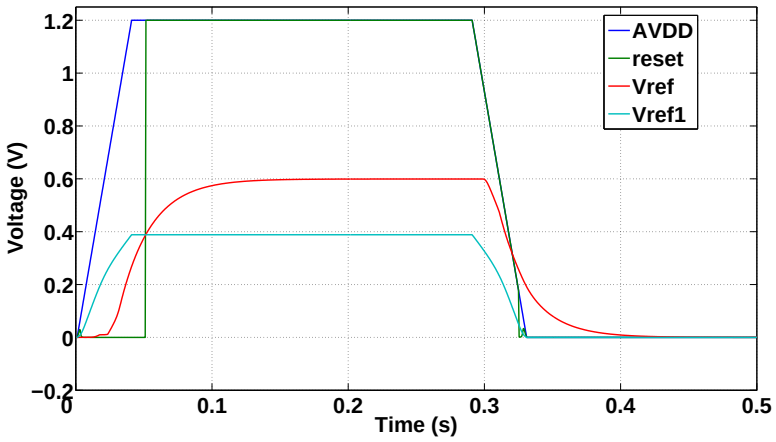


Figure 4.11: POR output.

CHAPTER 5

Low Dropout Regulator

5.1 Introduction

The ring oscillator is used to give a constant frequency clock to the ADC. With the supply voltage variations, the oscillation frequency also changes which is undesirable. Therefore there is a need to keep the supply voltage of the ring oscillator constant. An LDO is used to provide a regulated supply voltage which can be used to drive the ring oscillator. Following are the constraints that need to be met in the design:-

- Output impedance should be low
- The efficiency $\left(\frac{V_{out} \cdot I_L}{AVDD \cdot I_{sup}}\right)$ should be high
- Power supply rejection ratio (PSRR) should be high

The first condition can be met by using a negative feedback loop with a very high loop gain over as wide a bandwidth as possible. To meet the second condition, $I_{sup} - I_L$ should be minimized. This makes it difficult to realize a very high loop gain. The dropout voltage is the V_{DS} of the pass transistor, which should be very low to maximize the efficiency.

Fig. 5.1 shows the schematic of a basic LDO. It is a two stage op-amp used in negative feedback in the non-inverting amplifier configuration. A constant input voltage V_{in} is obtained from a bandgap reference circuit[2]. The output voltage is

$$V_{out} = V_{in}\left(1 + \frac{R_2}{R_1}\right) \tag{5.1}$$

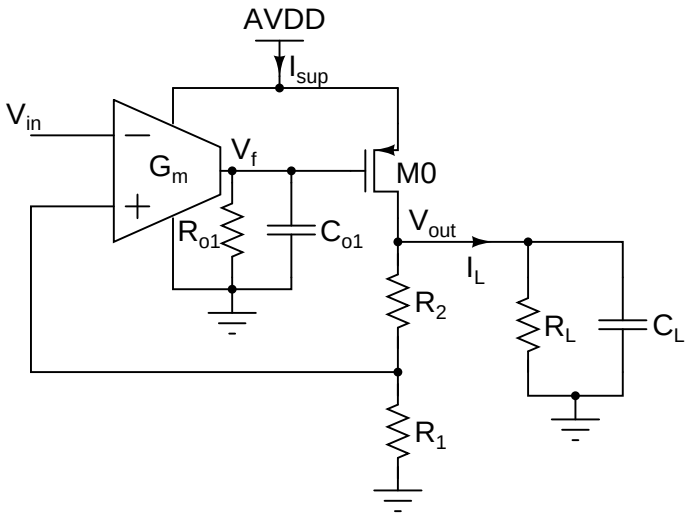


Figure 5.1: Basic LDO schematic.

It is a two stage op-amp in feedback and the loop needs to be compensated. G_{mp} is the transconductance of M0. R_{o1} and C_{o1} are the output resistance and the parasitic capacitance of the transconductance G_m. The loop gain is obtained by breaking the feedback loop at the output of the transconductance G_m, and applying a test voltage V_t at the gate of the transistor M0. The loop gain is

$$\frac{V_f}{V_t} = -\left(\frac{G_m G_{mp} R_1 R_L}{R_L + R_1 + R_2 + sC_L R_L(R_1 + R_2)}\right)\left(\frac{R_{o1}}{1 + sC_{o1}R_{o1}}\right) \tag{5.2}$$

The poles of (5.2) are

$$p_1 = -\frac{1}{(R_L||(R_1 + R_2))C_L}, p_2 = -\frac{1}{R_{o1}C_{o1}} \tag{5.3}$$

For compensating the loop, the poles p_1 and p_2 should be well separated. A high value of the capacitor C_L is used to make the pole p_1 as the dominant pole. This is called dominant pole compensation. The value of the capacitor C_L required for a phase margin $> 60^0$ is too high to be realized on a chip. Another method to separate the poles is using a capacitor C_c across the gate and drain of the transistor M0. This is popularly known as Miller compensation. At high frequencies, the parasitic capacitor C_{gs} of M0 couples the supply voltage to the output node V_{out} through C_c. This degrades the high frequency PSRR of the LDO, increasing the

oscillator's supply noise and hence the clock jitter. Therefore, Miller compensation is not used in this case.

5.2 Compensating the LDO

There is no provision of a separate pin for the supply voltage of the oscillator to compensate it using a large off-chip capacitor. So, the dominant pole compensation technique cannot be used. Instead, we compensate the loop gain by adding zeros in the transfer function by using the architecture as shown in Fig. 5.2[14]. The transistor level LDO schematic is used as shown in Fig. 5.3. The ring oscillator load is indicated by the resistor R_L. G_{mp} is the transconductance of M5. The

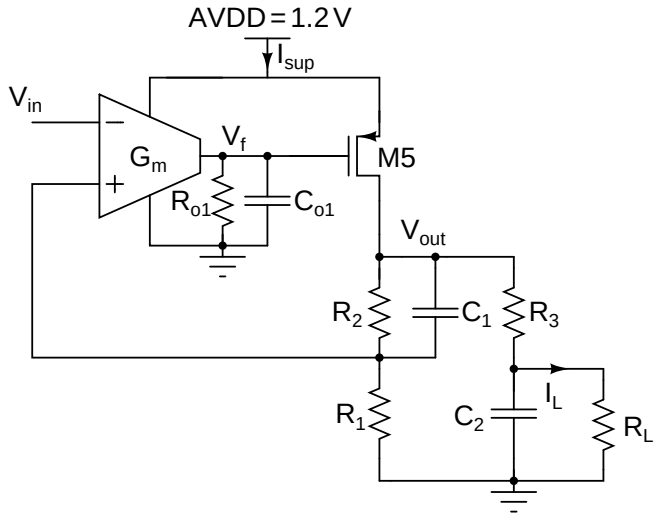


Figure 5.2: LDO architecture.

loop gain is

$$\frac{V_f}{V_t} = -\left(\frac{G_m G_{mp} R_1 (1 + sC_1R_2)(R_3 + R_L + sC_2R_3R_L)}{as^2 + bs + c}\right)\left(\frac{R_{o1}}{1 + sC_{o1}R_{o1}}\right) \quad (5.4)$$

where, $a = (R_1 + R_3)R_2R_LC_1C_2$, $b = (C_1R_2(R_1 + R_L) + C_2R_L(R_1 + R_2))$, and $c = R_1 + R_2 + R_L$

From the resistor and the capacitor values used, $R_1 \gg R_3$, $R_L \gg R_3$, $C_2 \gg C_1$.

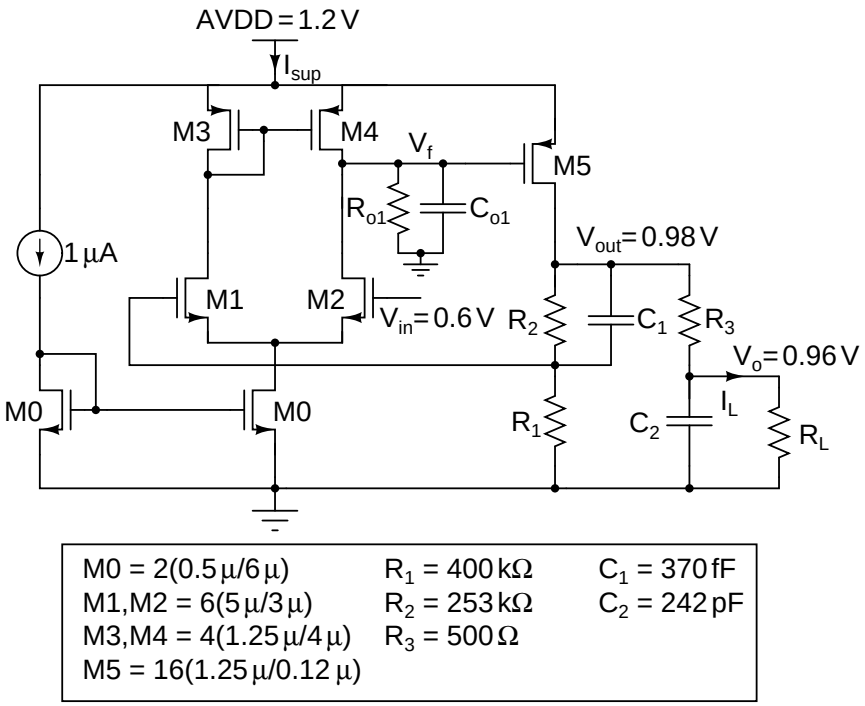


Figure 5.3: LDO schematic.

Using this to simplify (5.4), we get

$$\frac{V_f}{V_t} = -\left(\frac{G_m G_{mp} R_1 (1 + sC_1R_2)(R_L + sC_2R_3R_L)}{s^2R_1R_2R_LC_1C_2 + sC_2R_L(R_1 + R_2) + R_1 + R_2 + R_L}\right)\left(\frac{R_{o1}}{1 + sC_{o1}R_{o1}}\right) \tag{5.5}$$

The zeros and approximate poles of (5.5) are

$$z_1 = -\frac{1}{R_3C_2}, z_2 = -\frac{1}{R_2C_1} \tag{5.6}$$

$$p_1 = -\frac{1}{C_1(R_1 \parallel R_2)}, p_2 = -\frac{1}{C_2(R_L||(R_1 + R_2))}, p_3 = -\frac{1}{R_{o1}C_{o1}} \tag{5.7}$$

The values of R_3, C_1, and C_2 are chosen to get a phase margin of nearly 64^0. The capacitor C_2 is implemented using nMOS capacitors.

5.2.1 Simulation results

Fig. 5.4 shows the PSRR at the nodes V_o and V_{out}. The PSRR at V_o is 24 dB higher than that at V_{out} at the ring oscillator frequency of 20.48 MHz.

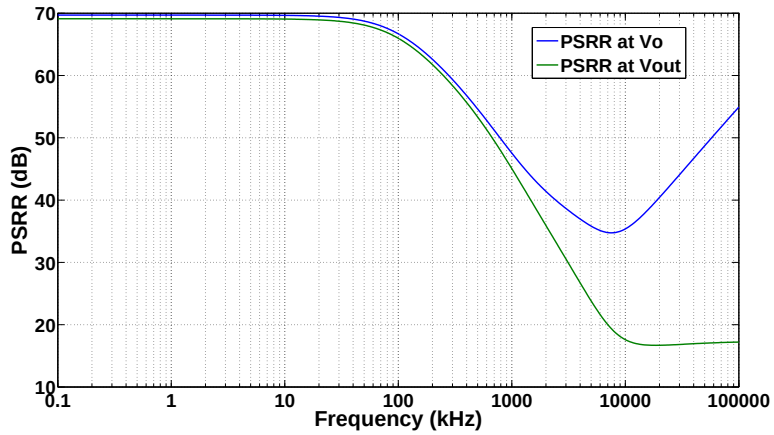


Figure 5.4: LDO PSRR.

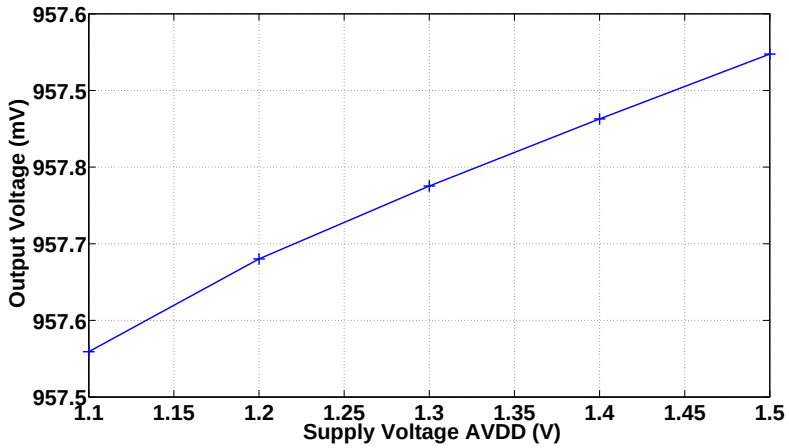


Figure 5.5: LDO output voltage variation.

To see the effect of the supply voltage on the LDO output, the supply voltage is varied from 1.1 V to 1.5 V. The output voltage is shown in Fig. 5.5. The output voltage varies by 0.2 mV. Fig. 5.6 shows the output voltage V_o due to the current step. The LDO is stable for a large current step of 40 μA.

The dropout voltage is 220 mV, and the saturation voltage of the transistor M0 is 90 mV. $V_o = 0.96$ V, $I_L = 41.2\,\mu$A, $AVDD = 1.2$ V, $I_{sup} = 44.7\,\mu$A resulting in an efficiency of 74 %.

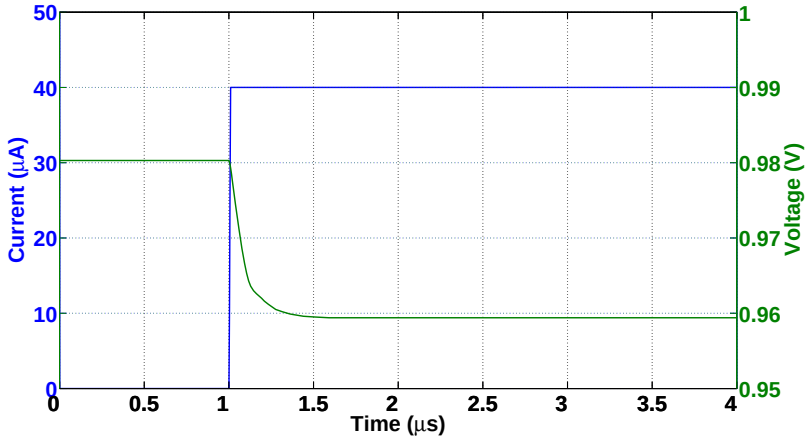


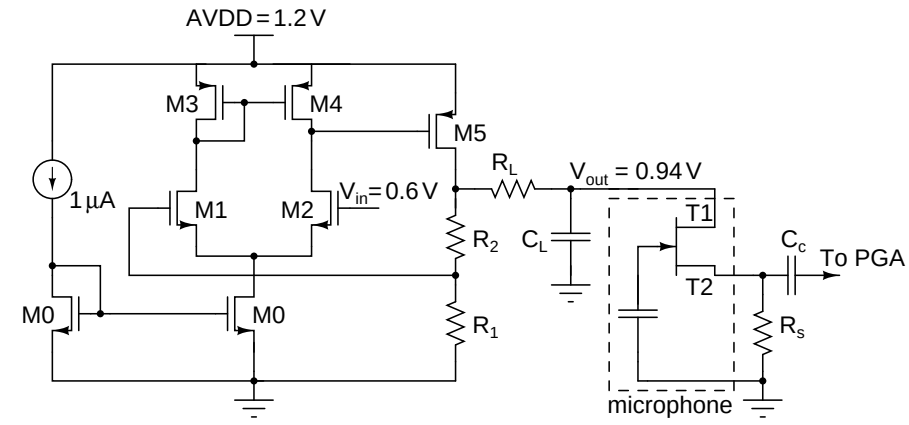
Figure 5.6: LDO current step response.

5.3 LDO for the microphone

The microphone used in the hearing aid is a common drain amplifier as shown in Fig. 5.7. Resistor R_s is used to bias the amplifier. The microphone output signal is taken from the terminal T2 through an ac coupling capacitor. The terminal T1 is connected to the terminal V_{out}. V_{out} should be independent of the supply voltage and hence is derived from the LDO. There is a provision of separate pins for the terminals T1 and T2. The dominant pole compensation technique has been used to compensate the LDO. It employs a large off-chip capacitor $C_L = 100\,\text{nF}$ at the LDO output. This value is chosen to get a phase margin of nearly 90^0. The LDO should be able to supply a continuous current of 20μA and an output voltage of $0.94\,\text{V}$ to the microphone. The PSRR targeted is greater than $55\,\text{dB}$.

5.3.1 Simulation results

The resistor $R_L = 51.6\,\Omega$ is used to improve the high frequency PSRR of the LDO. Fig. 5.8 shows the PSRR of the LDO. Fig. 5.9 shows the output voltage variation of the LDO with the supply voltage varying from $1.1\,\text{V}$ to $1.5\,\text{V}$. Fig. 5.10 shows the output voltage V_{out} due to the current step. The LDO is stable for a large current step of $20\,\mu$A.



M0 = 2(0.5 µ/6 µ)	M3,M4 = 4(1 µ/4 µ)	R_1 = 400 kΩ	R_L = 51.6 Ω	C_L = 0.1 µF
M1,M2 = 6(5 µ/3 µ)	M5 = 6(1 µ/0.12 µ)	R_2 = 226.9 kΩ	R_s = 29.1 kΩ	C_c = 1 µF

Figure 5.7: LDO schematic.

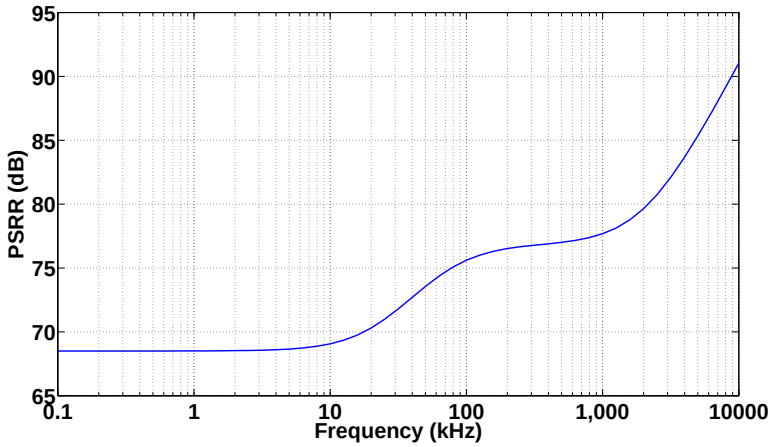


Figure 5.8: LDO PSRR.

5.4 Power contribution of the frontend

Table 5.1 shows the simulated power contribution of all the frontend blocks from a 1.2 V supply.

5.5 Layout of the hearing aid chip

The frontend and backend blocks are integrated and the complete layout is shown in Fig. 5.11. The layout of the ADC and the backend blocks layout is done by other designers[2] [16]. The chip occupies an active area of 2.3 mm x 985 μm.

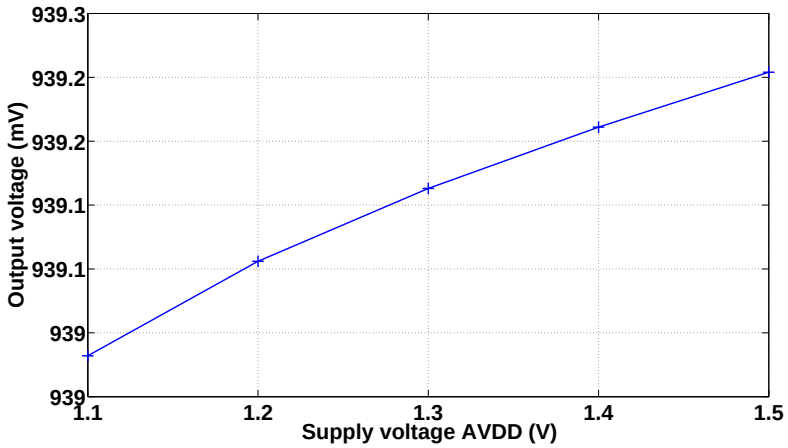


Figure 5.9: LDO output voltage variation.

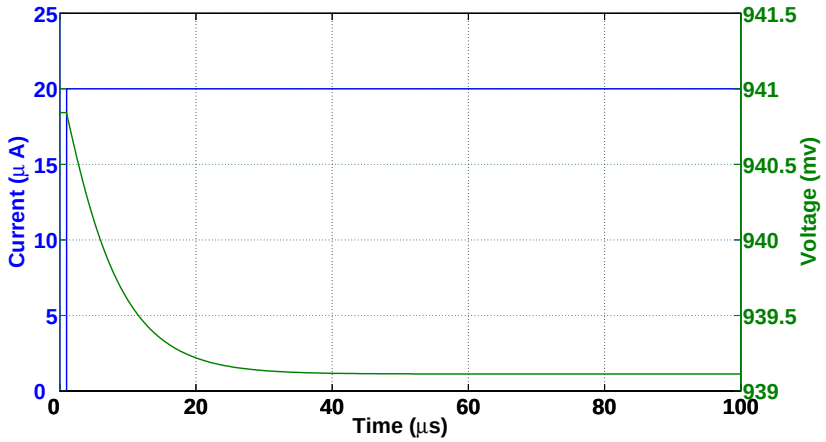


Figure 5.10: LDO current step response.

Table 5.1: Power contribution.

Block	**Power contribution (μW)**	**Percentage power (%)**
PGA	25	17.5
AGC	7	4.8
ADC [16]	36	25
Decimation filter	6	4.2
LDO for the oscillator	3.5	2.4
LDO for the microphone	3.5	2.4
Ring oscillator	55	38.2
POR	3	2
Buffers	5	3.5
Total	144	100

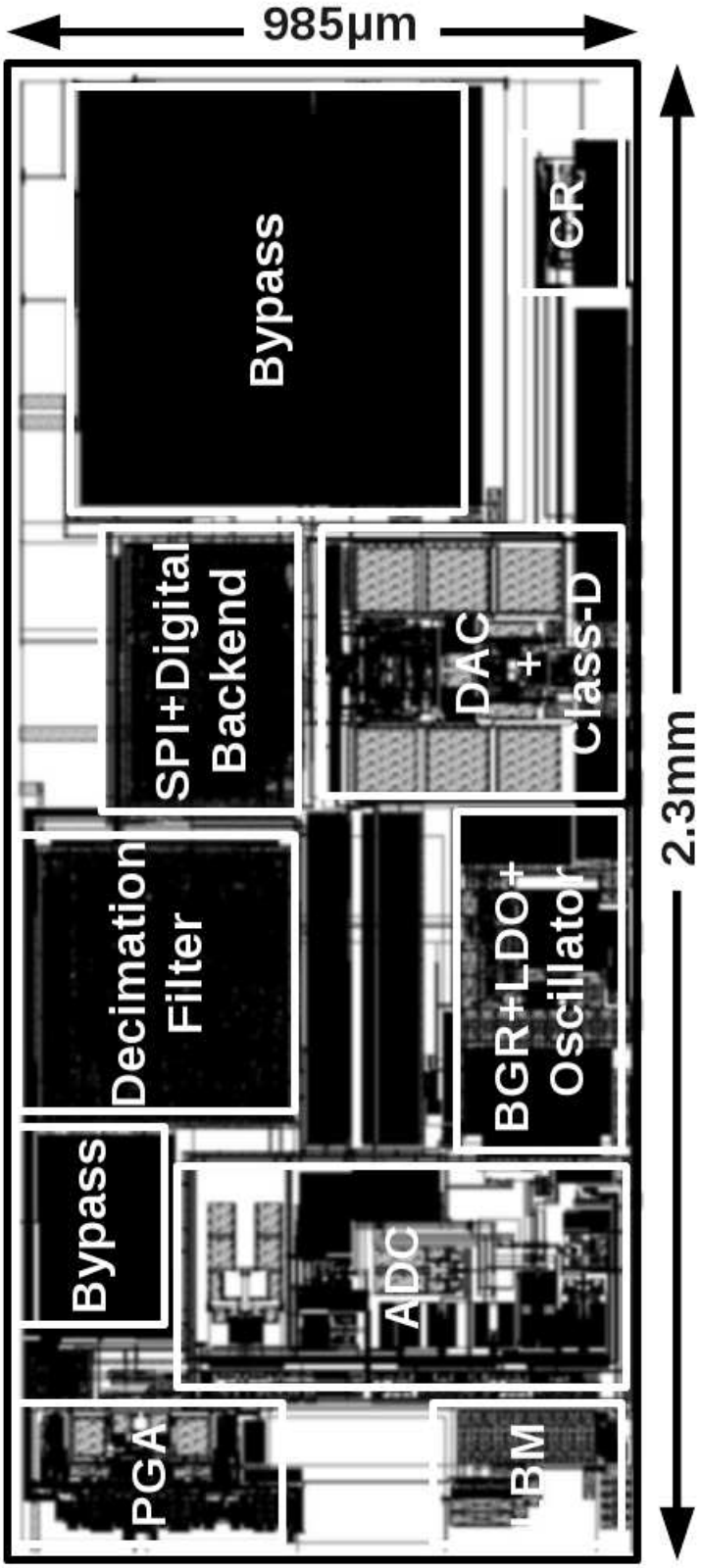


Figure 5.11: Complete hearing aid analog frontend layout.

CHAPTER 6

Measured Results from the Hearing Aid Chip

6.1 Measurement setup

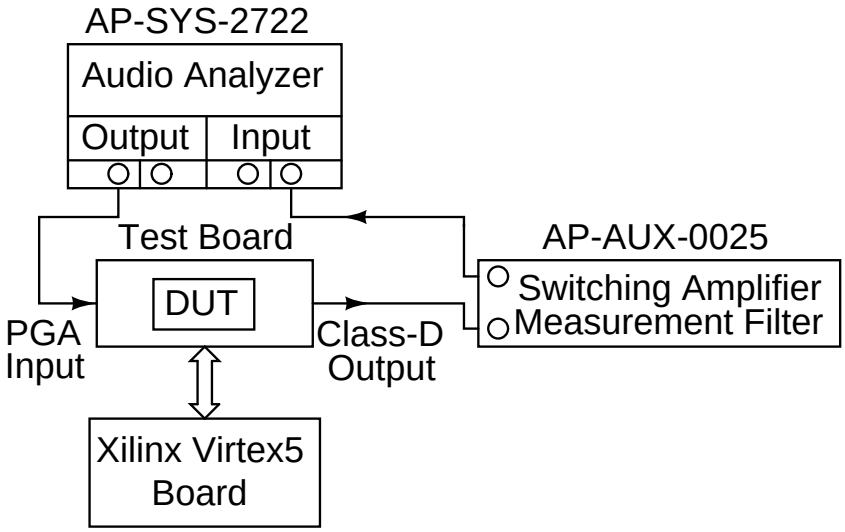


Figure 6.1: Measurement setup.

Fig. 6.1 shows the measurement setup used to test the hearing aid chip. The Audio Precision AP-SYS-2722 audio analyzer is used to give an analog input signal to the PGA. For digital serial interface with the chip, Xilinx Virtex5 FPGA board is used. The class-D amplifier output is filtered using Audio Precision AP-AUX-0025 switching amplifier measurement filter. The filtered output is analyzed using audio analyzer for measuring the performance of the frontend. The test board (four layer PCB) is shown in Fig. 6.2. The hearing aid chip (device under test;DUT) is programmed such that the decimator output is connected to the backend (DAC + class-D).

Instead of the decimator digital output, the class-D analog output is used to analyze the frontend performance. This method is adopted because in the spectrum of the decimator output, the input frequency bin is varied by the jittery sampling

clock. If this digital output is converted to analog using the DAC clocked by the same jittery clock, the spreading of the input frequency bin in the DAC output spectrum is avoided as shown in the following section. The class-D output will be the measure of the frontend performance, since the backend noise floor and distortion is lower than that of the frontend.

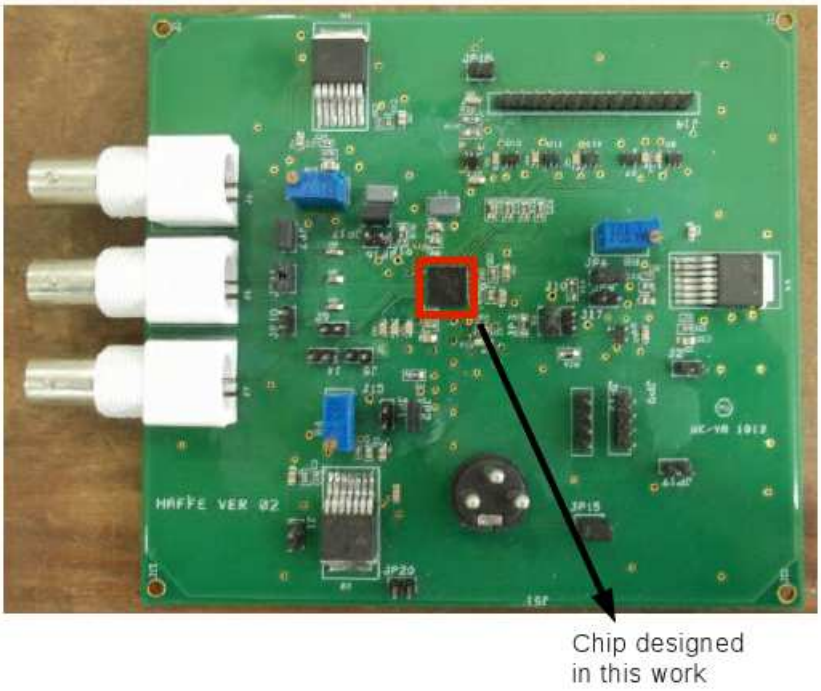


Figure 6.2: Test board.

6.2 Measurement results

6.2.1 Idle channel performance

The input terminals of the PGA are ac coupled to ground. The oscillator frequency is tuned to 18.2 MHz. The supply voltage is 1.2 V. The output noise in the bandwidth of 100 Hz - 9 kHz is measured from the PSD of the filtered class-D output. The input referred noise is calculated by dividing the output noise by the total gain (PGA gain x ADC gain (2.1) x decimator gain (1.4)). Table 6.1 shows the input referred noise for the different PGA gains.

Table 6.1: Input referred idle channel noise.

PGA Gain (dB)	Input referred noise (μV_{rms})
40	1.74
35	2.2
30	2.8
25	3.6
20	5.52
15	8
10	11
5	17
0	28
-1	30.7

6.2.2 Performance with the signal

Single ended inputs of amplitudes 3 mV_p, 30 mV_p, 300 mV_p and 1.1 kHz frequency are given as inputs to the PGA. PGA is programmed for three different gains: 40 dB, 20 dB, and -1 dB. As previously mentioned, the decimator output has the spreading of the input frequency bin as shown in Fig. 6.3. The decimator output is fed to the backend and the in-band spectra of the class-D output are shown in Fig. 6.4. Thus, the spreading of the input frequency bin is avoided. So, the backend output is used for measuring the frontend performance. Table 6.2 shows the measured SNDR/SNR/THD in the 9 kHz bandwidth for the three inputs.

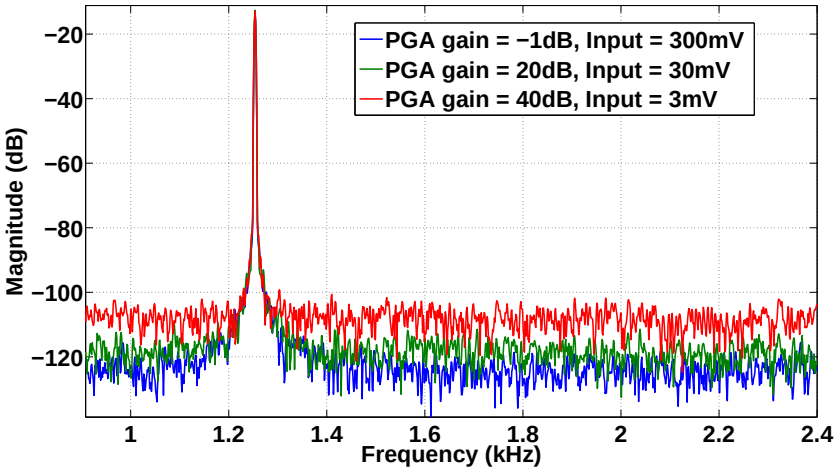


Figure 6.3: PSD of the decimator output.

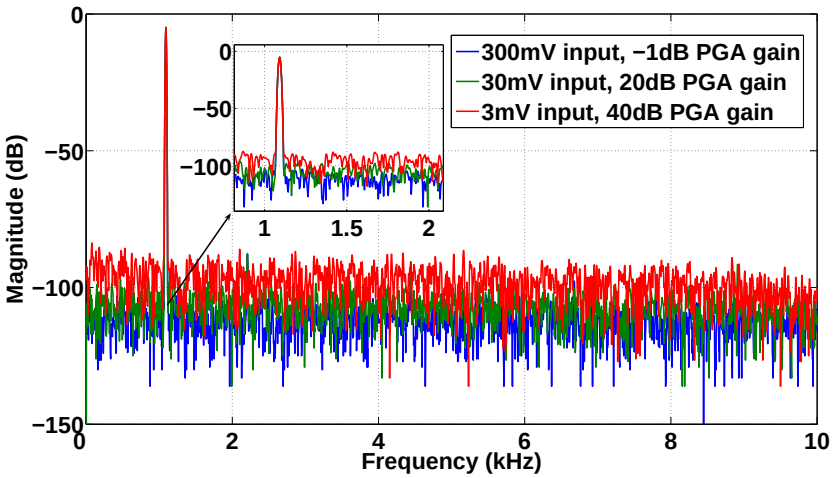


Figure 6.4: PSD of the class-D output.

Table 6.2: Performance for different input amplitudes.

Input amplitude (mV_p)	PGA gain (dB)	SNDR (dB)	SNR (dB)	THD (dB)
3	40	61.1	61.3	-74.2
30	20	71	72	-78
300	-1	76	78	-80

6.2.3 Dynamic range measurement

Single ended inputs of different amplitudes and a frequency of 1.1 kHz are given to the PGA. Fig. 6.5 shows the SNDR and SNR versus input amplitude (dBFS). The dynamic range measured including PGA gain variation is 106 dB. Fig. 6.6 shows the measured THD.

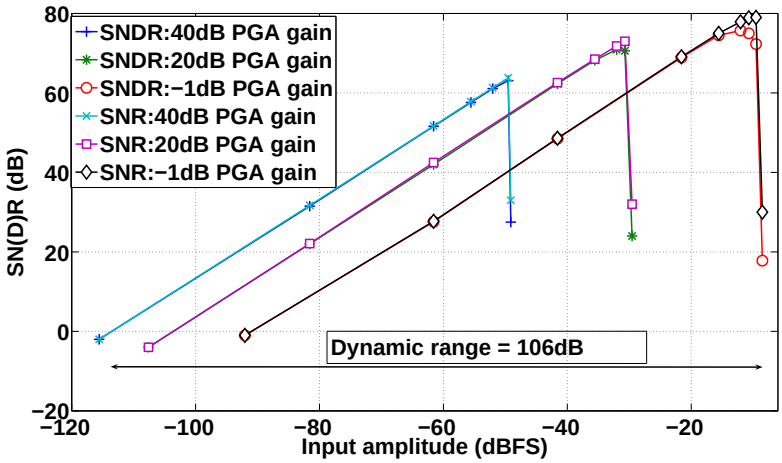


Figure 6.5: Dynamic range plot.

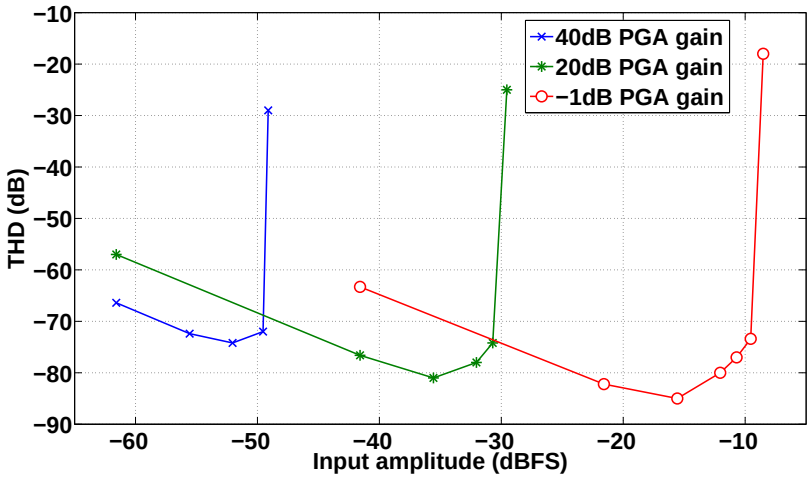


Figure 6.6: THD plot.

6.2.4 Monotonicity in the PGA gain

PGA gain is increased from -1 dB to 40 dB in steps of 0.5 dB. Input signal amplitude is 4 mV_p at a frequency of 1.1 kHz. Fig. 6.7 shows that the output amplitude increases monotonically with the PGA gain. Fig. 6.8 shows the gain step achieved versus the set PGA gain. The simulated gain step variation is 0.45 dB to 0.52 dB, while the measured steps are between 0.3 dB and 0.6 dB.

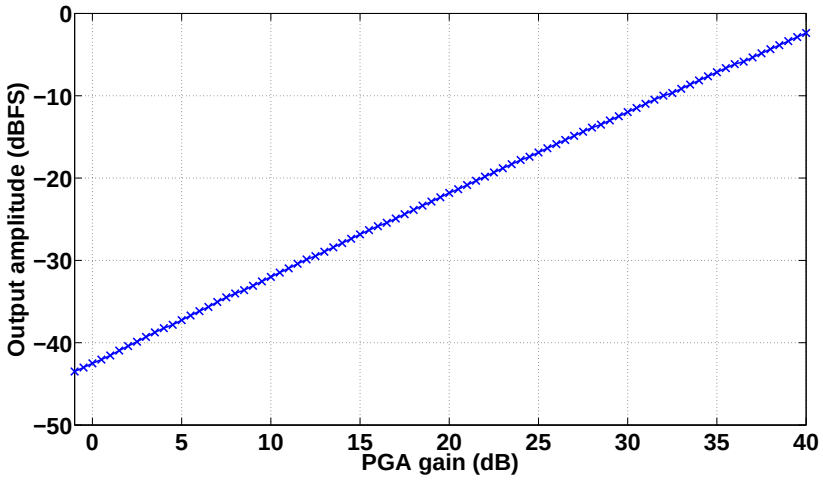


Figure 6.7: Monotonicity in the PGA gain.

Table 6.3 shows the summary of the measured performance.

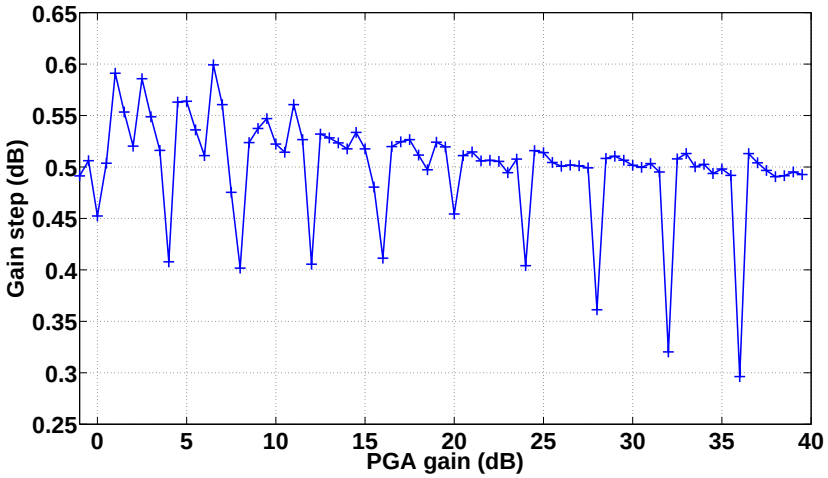


Figure 6.8: PGA gain step.

Table 6.3: Performance summary.

Parameter	**Value**
Process	130 nm CMOS
Supply voltage	1.2 V
Input noise	1.74 μV_{rms}
Frontend power	144 μW
THD	-80 dB
SNR	79 dB
Bandwidth	100 Hz - 9 kHz
Active area	2.3 mm^2
Dynamic range	106 dB

6.3 Comparison with prior work

Table 6.4: Comparison with prior work.

Parameter	**This work**	**[19]**	**[20]**	**[5]**
Process	130 nm	180 nm	1.2 μm	0.6 μm
Supply voltage (V)	1.2	0.9	1	1.1
Input noise (μV_{rms})	1.74	4.2	6	2.8
Power (μW)	384	107	200	297
THD (%)	0.01	-	0.1	0.02
SNR (dB)	79	81	70	-

CHAPTER 7

16 Ω headphone driver for 20 Hz - 24 kHz audio

7.1 Introduction

Table 7.1: Driver specifications.

Load	16 Ω ‖ 100 pF
Maximum output power	80 mW
Bandwidth	20 Hz - 24 kHz
THD + N	< -90 dB
Input noise	5 μV_{rms}
Quiescent power	1 mW
Supply voltage	1.8 V
Technology	180 nm CMOS

Table 7.1 shows the driver specifications. The headphone driver is used to drive the load of 16 Ω. The motivation is to drive the load by consuming minimum quiescent power possible. A class-A amplifier requires the output bias current to be equal to the maximum load current (100 mA in this case). This degrades the efficiency of the power amplifier. In a class-B amplifier, the output bias current is zero. Although its efficiency is high compared to the class-A amplifier, it gives significant distortion. In a class-AB amplifier, a minimum output bias current is maintained to improve the distortion. Therefore, the class-AB amplifier is used in this work to minimize the power dissipation for a given distortion.

7.2 Dual supply driver

Powering the op-amp from 1.8 V and 0 V requires the output common mode to be 0.9 V. The load requires a high quiescent current of 0.9 V/16 Ω = 56.25 mA. To avoid this large dc current, a very large capacitor in series with the load is

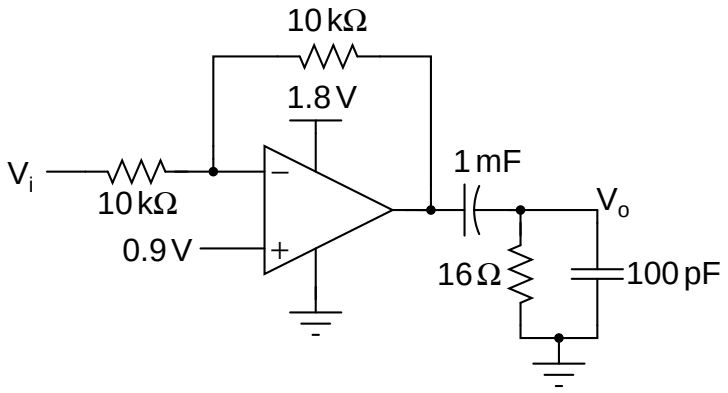


Figure 7.1: Single supply driver.

required as shown in Fig. 7.1. The value of this capacitor should be $> 500\,\mu$F for the highpass cut-off to be $< 20\,$Hz. As already mentioned in the introduction, such a large capacitor consumes a large area, and is not suitable for portable audio applications. During start-up or shutdown, this capacitor has to be charged or discharged which causes an audible pop.

If the output bias is kept at 0 V, the dc blocking capacitor is not required, thus eliminating the disadvantages associated with it. To achieve this, the amplifier is driven by a dual supply of 1.8 V and -1.8 V. The schematic is shown in Fig. 7.2. It is an op-amp used in an inverting unity gain configuration. A negative voltage converter is used to provide the negative supply for the op-amp.

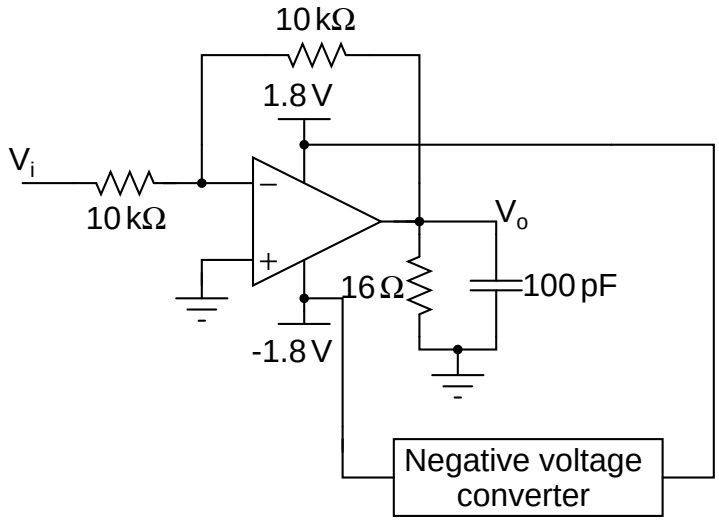


Figure 7.2: Dual supply driver.

7.3 Op-amp design

7.3.1 Op-amp macromodel

A three stage op-amp with a very high dc gain is required for driving the 16Ω load. To compensate the op-amp, a combination of feedforward and Miller compensation is used. Fig. 7.3 shows the macromodel of the op-amp.

The transfer function is

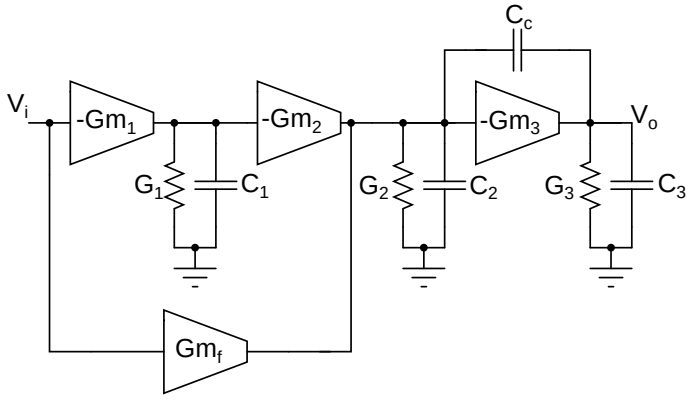


Figure 7.3: Op-amp macromodel.

$$\frac{V_o}{V_i} = \frac{(Gm_1Gm_2 + Gm_fG_1 + sC_1Gm_f)(sC_c - Gm_3)}{(G_1 + sC_1)((G_2 + sC_2 + sC_c)(G_3 + sC_3 + sC_c) - sC_c(sC_c - Gm_3))} \quad (7.1)$$

The approximate values of the poles are

$$p_1 = \frac{-G_2G_3}{G_2(C_3 + C_c) + G_3(C_2 + C_c) + Gm_3C_c} \quad (7.2)$$

$$p_2 = \frac{-(G_2(C_3 + C_c) + G_3(C_2 + C_c) + Gm_3C_c)}{C_2C_3 + C_c(C_2 + C_3)} \quad (7.3)$$

$$p_3 = \frac{-G_1}{C_1} \quad (7.4)$$

Zeros of the transfer function are

$$z_1 = \frac{Gm_3}{C_c}, z_2 = \frac{-(Gm_1Gm_2 + Gm_fG_1)}{Gm_fC_1} \quad (7.5)$$

For sufficient phase margin, the zero (z_2) introduced by the feedforward path should be much less than the unity gain frequency of the first two stages standalone.

$$|z_2| \ll \sqrt{\frac{Gm_1 Gm_2}{C_1 C_2}} \tag{7.6}$$

7.3.2 Op-amp implementation

As mentioned earlier, the output common mode is at 0 V. This makes the input common mode of the op-amp also 0 V. So a pMOS transistor input stage is used. Also to have a lower flicker noise, a pMOS input stage is preferable. To get a very high dc gain, we use a folded cascode structure. Fig.7.4 shows the first stage op-amp schematic along with the bias section.

Transistors M1-M12 form the folded cascode first stage of the op-amp. Transistors

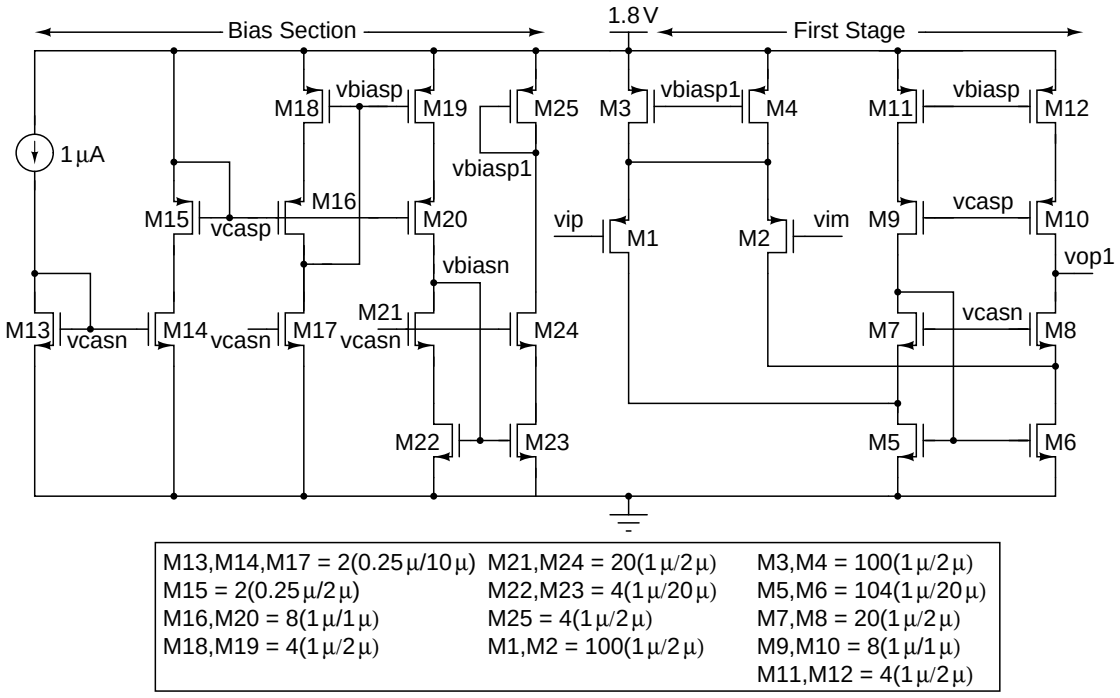
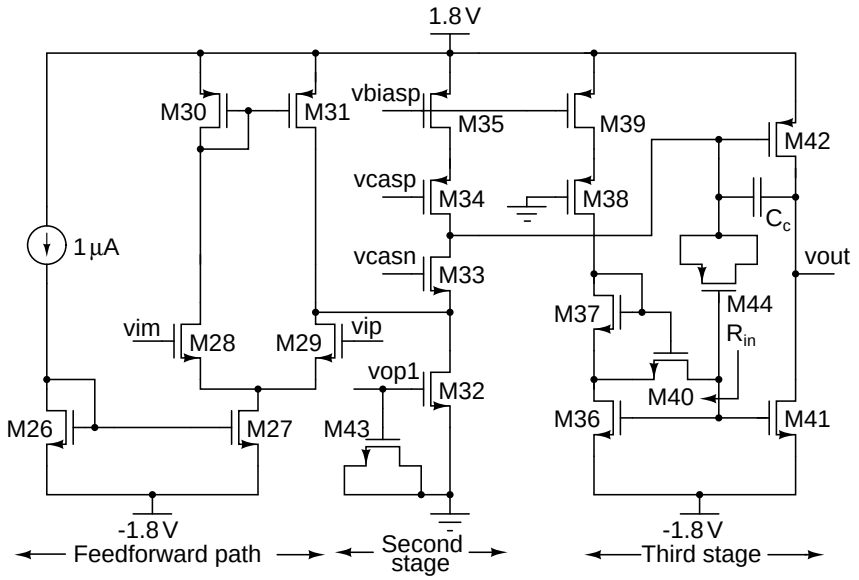


Figure 7.4: First stage op-amp schematic.

M5 and M6 have large lengths to minimize their flicker noise. The current in each input transistor is 25 μA to meet the noise specification. The dc gain of the first stage is 82 dB. Thus most of the dc gain is obtained from the first stage itself. The first stage is operated from 1.8 V and 0 V to save power.

Fig.7.5 shows the circuit diagram of the second and the third stage of the op-



M26 = 2(0.5 µ/2 µ)	M32 = 20(1 µ/20 µ)	M36 = 2(26.67 µ/0.34 µ)	M41 = 150(26.67 µ/0.34 µ)
M27 = 140(0.5 µ/2 µ)	M33 = 100(1 µ/2 µ)	M37 = 100(1 µ/0.34 µ)	M42 = 400(30 µ/0.34 µ)
M28,M29 = 200(2 µ/2 µ)	M34 = 40(1 µ/1 µ)	M38 = 8(1 µ/0.18 µ)	M44 = 5(72 µ/25 µ)
M30,M31 = 2(1.75 µ/2 µ)	M35 = 20(1 µ/2 µ)	M39 = 4(1 µ/2 µ)	C_c = 5 pF
	M43 = 60(10 µ/2 µ)	M40 = 2(0.24 µ/20 µ)	

Figure 7.5: Second and third stage op-amp schematic.

amp. The second stage (M32-M35) is a common source stage with a cascode for the input and the bias transistor. It gives a gain of 40 dB. Transistor M43 is used as a MOS capacitor of value 10 pF. This capacitance is C_1 in the op-amp's macromodel shown in Fig. 7.3. So using a high value for C_1, the zero z_2 is moved to lower frequencies giving higher phase margin without increasing the feedforward transconductance Gm_f[17]. Transistors M27-M31 form the feedforward stage. An nMOS differential pair is used to provide a feedforward path (with higher Gm_f) from the input of the first stage to the second stage output. Its output is not connected directly to the second stage output to avoid loading. In addition, the feedforward op-amp is operated from the positive and the negative supply, as the input common mode is at 0 V.

The third stage (M41-M42) forms the class-AB driving stage. To have an output common mode of 0 V, it is operated from the dual supply. Signal from the second stage output is directly fed to the pMOS (M42) input, and is ac coupled to the nMOS (M41) input. Transistor M44 acts as a coupling capacitor (C_{co}) of value

50 pF. The parasitic gate capacitor of M41 is C_{gg}=5 pF. The looking in impedance R_{in} as shown in Fig. 7.6 is given by

$$R_{in} = \frac{g_{ds36}}{g_{ds40} \cdot g_{m36}}, f = \frac{1}{2\pi R_{in}(C_{co} + C_{gg})} \tag{7.7}$$

where, g_{ds36} and g_{ds40} are the output conductance of M36 and M40, respectively, g_{m36} is the transconductance of M36, and f is the ac coupling cut-off frequency (87 Hz). The bias current for the output class-AB stage is fixed to 176 μA by a simple current mirroring from M36. For the positive-half input cycle, M41 drives the load, while for the negative-half input cycle, M42 drives the load, ensuring class-AB operation.

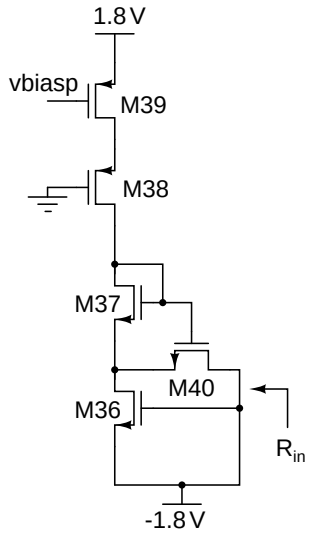


Figure 7.6: Resistance R_{in} in the ac coupling network.

7.4 Simulation results

The driver is simulated with the ideal dual supply of 1.8 V and -1.8 V. Fig. 7.7 and Fig. 7.8 shows the magnitude and the phase response of the loop gain, respectively. Table 7.2 shows the op-amp characteristics. The loop stability is tested by applying a step input of 10 mV with 0.1 ns rise time to the inverting unity gain op-amp. The output is shown in Fig. 7.9. An input signal of 1.6 V_p amplitude and 1.25 kHz

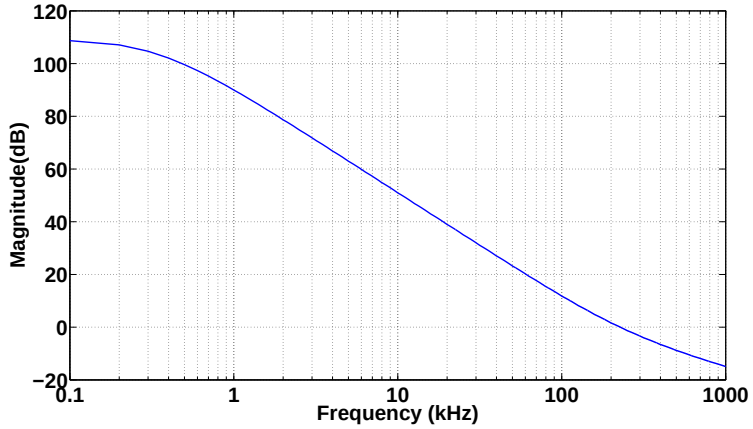


Figure 7.7: Magnitude response of the loop gain.

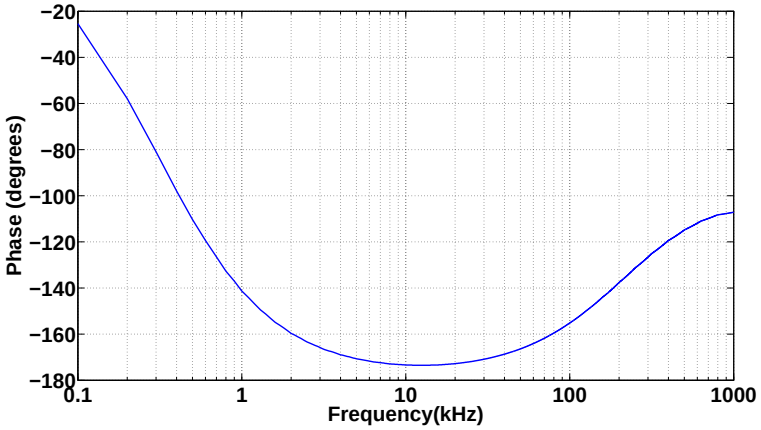


Figure 7.8: Phase response of the loop gain.

frequency is applied to the driver. The voltage waveforms at the gates and the drains of the transistors M41 and M42 are shown in Fig. 7.10. The voltage swing at the gate of M42 is $0.73\,\mathrm{V_{pp}}$, and at the gate of M41 is $0.56\,\mathrm{V_{pp}}$. This small attenuation is due to the capacitive divider (C_{gs44} and C_{gs41}). Fig. 7.11 shows the spectrum of the output voltage. The SNDR/SNR/THD are calculated in the bandwidth of 24 kHz.

Table 7.2: Op-amp characteristics.

DC loop gain	108 dB
Unity loop gain frequency	226 kHz
Phase margin	46^0
Input referred noise	$2\,\mu\mathrm{V_{rms}}$
Quiescent power	1 mW

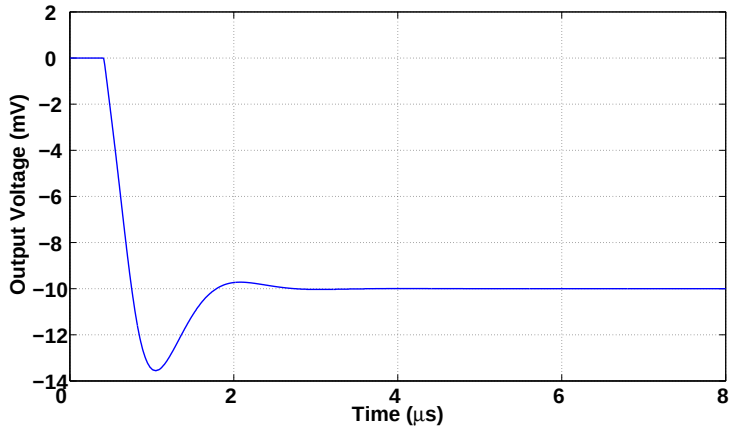


Figure 7.9: Step response.

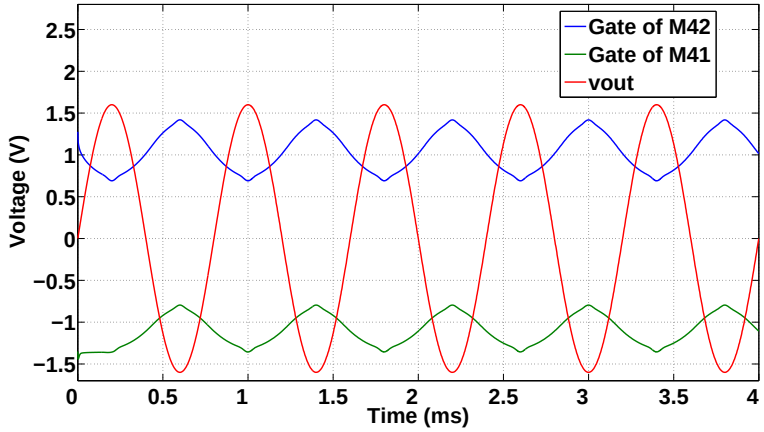


Figure 7.10: Voltage waveforms.

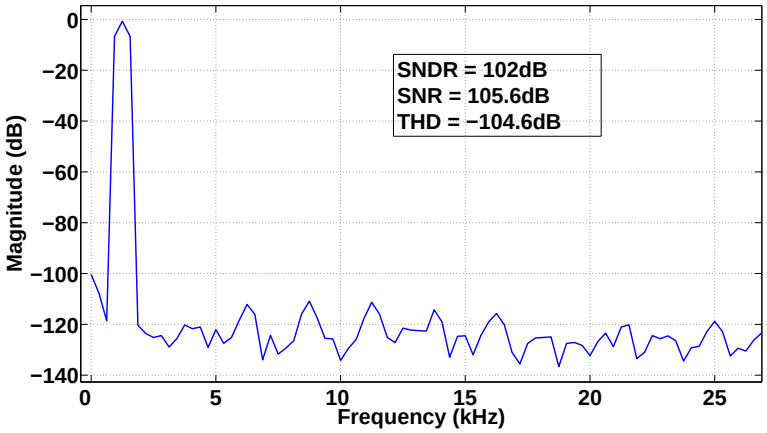


Figure 7.11: Output voltage spectrum.

CHAPTER 8

Negative Voltage Converter

8.1 Architecture

A simple architecture based on a charge pump is used for the negative voltage converter[18]. Fig. 8.1 shows the circuit for the negative voltage converter. Here, all the transistors (M1-M4) are used as switches. During the first half-cycle, the capacitor C1 is charged to 1.8 V through the switches M3 and M4. During the second half-cycle, capacitor C1 transfers the charge through the switches M1 and M2 to the capacitor C2, thus inverting the input voltage. The switching frequency and the ripple specification at the output decides the capacitor value. During the time when the capacitor C1 is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which causes a ripple in the output voltage.

The relation between the operating frequency, output voltage ripple and the value

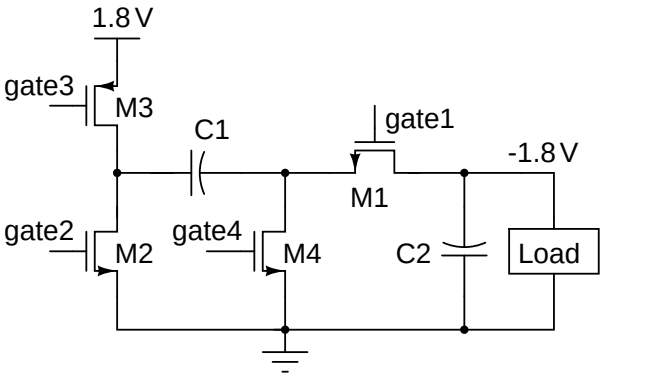


Figure 8.1: Negative voltage converter schematic.

of the capacitor C2 is given below. Let ΔV be the output voltage ripple and f

be the frequency of operation. When C1 is connected between 1.8 V and 0 V, the output capacitor C2 supplies the load current. Thus

$$C2 \cdot \Delta V = I_L \cdot T_{off}, T_{off} = \frac{1}{2f} \tag{8.1}$$

A ripple of 12 mV is tolerable for a THD < -90 dB. For a 16 Ω load, the peak load current is $I_L = 1.6/16 = 100$ mA. For f = 200 kHz, and $\Delta V = 12$ mV, we get C2 = 20 μF. To achieve a maximum efficiency of operation, the impedances of C1 and C2 at the switching frequency f should be very small compared to the load impedance. So an equally high value for C1 is used as is used for C2. The design of this negative voltage converter mainly consists of two parts[18]: switch sizing and switch control signal generation.

8.2 Design

8.2.1 Switch sizing

The sizes of the four switches are shown in Fig. 8.1. The ON resistance (R) of the switches should be very small to satisfy $RC < T_{off}$. The gate-source voltage of the transistors control their ON resistances. Higher the V_{GS}, lower the ON resistance. So to turn on the pMOS transistor M3, we pull down the gate voltage to -1.8 V, thus giving a $V_{GS} = 3.6$ V. Similarly, for the transistor M1, we get $V_{GS} =$ 3.6 V. So without actually boosting the voltage, a $V_{GS} = 3.6$ V is obtained for the transistors M1 and M3. For turning ON the transistor M4, we cannot boost the gate voltage to 3.6 V, as the swing at the gate will become 5.4 V, since its turn-off requires a gate voltage of -1.8 V, violating the reliability of the device. For the gate of the transistor M2, the width is increased to twice the width of M1 (instead of boosting the gate to 3.6 V) to get the same ON resistance as that of M1. The swings at the gates of all transistors are from -1.8 V to 1.8 V.

8.2.2 Switch control signal generation

During one phase the switches M3 and M4 are turned on, and the switches M1 and M2 are turned off. The capacitor C1 is charged to 1.8 V. In the next phase of the clock, the switches M1 and M2 are turned on and the switches M3 and M4 are turned off. To avoid any short circuit current during the transition, the switches must be operated in a particular sequence. While turning off M1 and M2 and turning on M3 and M4 the following order is followed[18]: turn off M1 → turn off M2 → turn on M4 → turn on M3. While turning on M1 and M2 and turning off M3 and M4, the following order is followed: turn off M3 → turn off M4 → turn on M2 → turn on M1.

The external reference clock signal varies from 0 V to 1.8 V. The lower clock voltage level should be shifted from 0 V to -1.8 V for turning off M1, M4. Thus, a level shifter is used to change the clock signal swing from 1.8 V_{pp} to 3.6 V_{pp}. Before

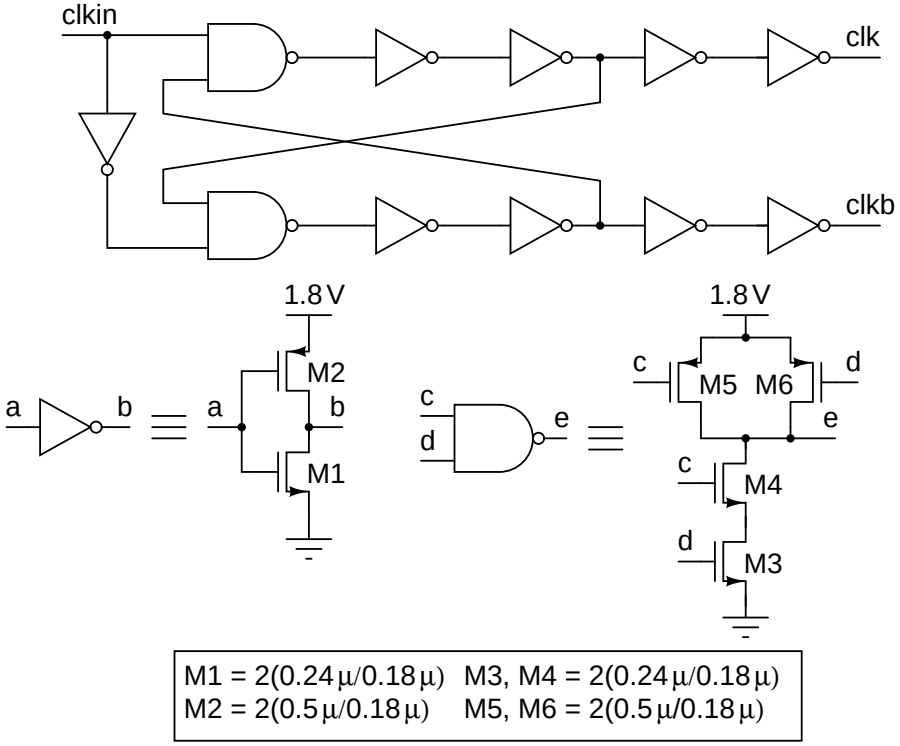


Figure 8.2: Non-overlapping clock generator.

connecting to the level shifter the clock signal passes through a non-overlap generator shown in Fig. 8.2 for generating complementary non-overlapping low signals

required for the level shifter. This eliminates the possibility of short circuit current in the level shifter. The non-overlap generator is supplied from 1.8 V and 0 V. The level shifter is shown in Fig. 8.3[18]. The output of the level shifter swings from

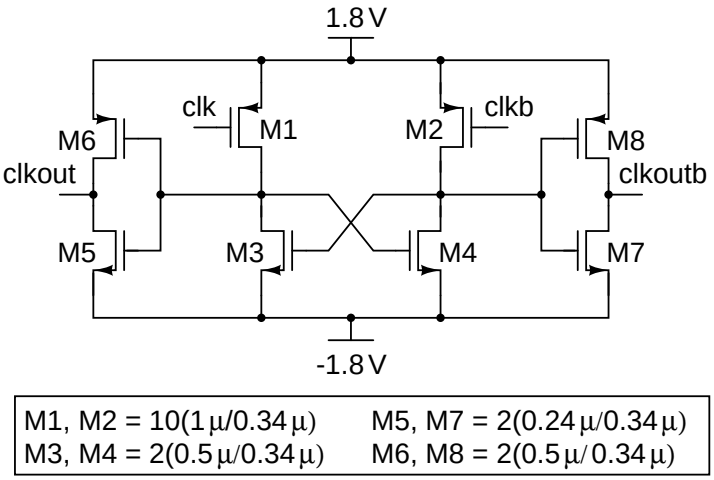


Figure 8.3: Level shifter.

-1.8 V to 1.8 V.

To turn on or turn off the switches M1-M4 in the above mentioned sequence, we need to generate the delayed control signals. The output of the level shifter is passed through a chain of inverters shown in Fig. 8.4, to get different delayed clocks[18]. These delayed clocks from appropriate nodes are OR-ed together to

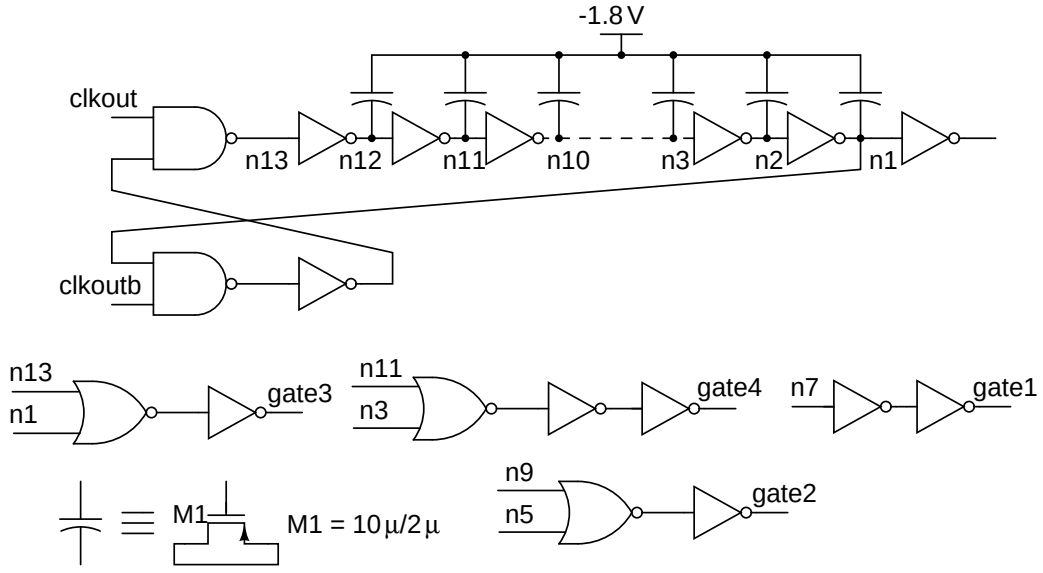
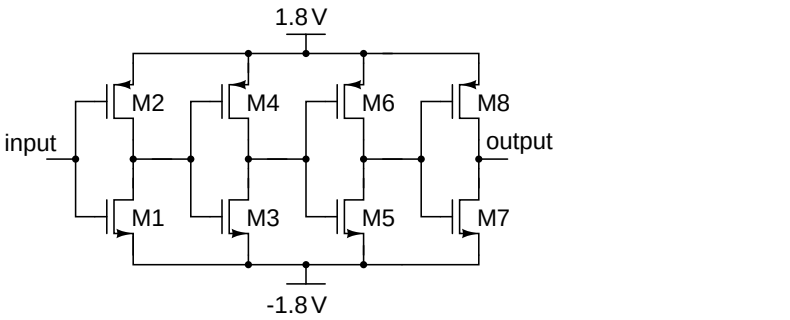


Figure 8.4: Clock delay generator.

get gate2, gate3 and gate4 signals with the required delays. The gate1 signal is di-

rectly obtained from the middle of the chain. The pMOS capacitors are included in the chain to increase the delay in the chain without further increase in the number of inverters. The total transition duration for the four gate signals is 5 ns. The charge pump is operated at 200 kHz. The transition time is only 0.2 % of the steady on or off duration. This circuit is operated from 1.8 V and -1.8 V.

The gate control signals generated from the delay chain are fed to the respective gates through a buffer chain for each gate control signal. The buffer chain is shown in Fig. 8.5. The buffered outputs when C1 gets disconnected from 1.8 V and connects between the output and 0 V are shown in Fig. 8.6. The outputs of the buffer chain when C1 gets disconnected from the output and connects between 1.8 V and 0 V are shown in Fig. 8.7.



M1 = 2(0.5 µ/0.34 µ)	M3 = 4(2.5 µ/0.34 µ)	M5 = 8(12.5 µ/0.34 µ)	M7 = 100(10 µ/0.34 µ)
M2 = 2(2 µ/0.34 µ)	M4 = 10(4 µ/0.34 µ)	M6 = 20(20 µ/0.34 µ)	M8 = 110(36.36 µ/0.34 µ)

Figure 8.5: Clock buffer.

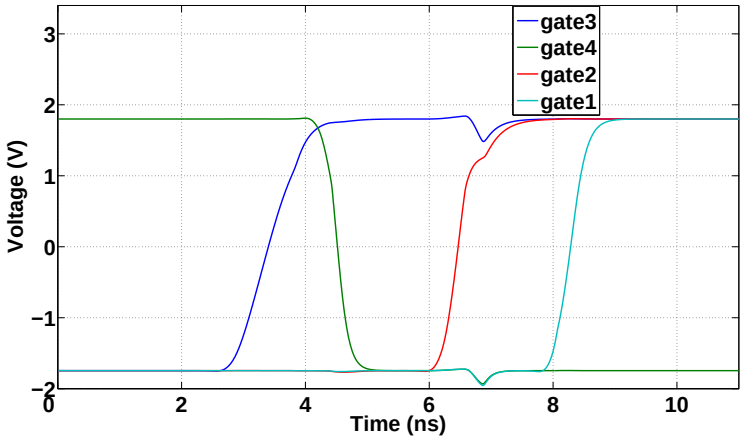


Figure 8.6: Buffer stage outputs during one transition.

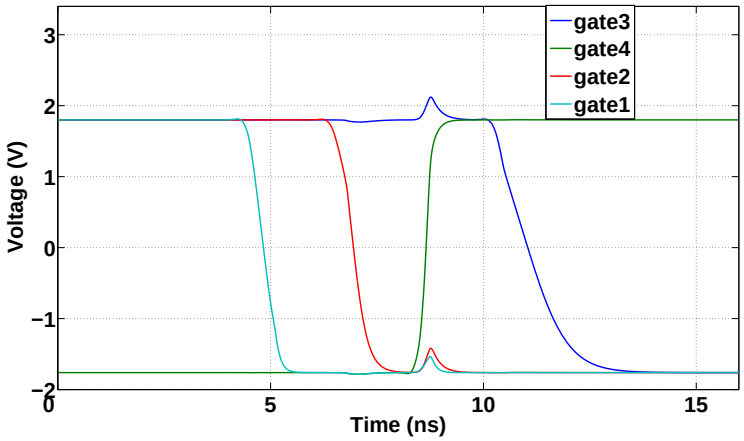


Figure 8.7: Buffer stage outputs during another transition.

8.3 Performance analysis

Efficiency $\left(\dfrac{\text{Power delivered to the load}}{\text{Power drawn from the supply}}\right)$ of the converter is analyzed by varying the frequency. The values of the capacitors C1 and C2 are scaled appropriately to get the same output voltage ripple of 12 mV for each frequency. It is observed that the efficiency decreases with increasing frequency as shown in Fig. 8.8. This is because switching power increases with frequency. Lower switching frequency ensures high efficiency but with the trade-off of using a large capacitor. A switching frequency of 200 kHz is used which results in a negative voltage conversion efficiency of 96 % and requires two capacitors of 20 μF each.

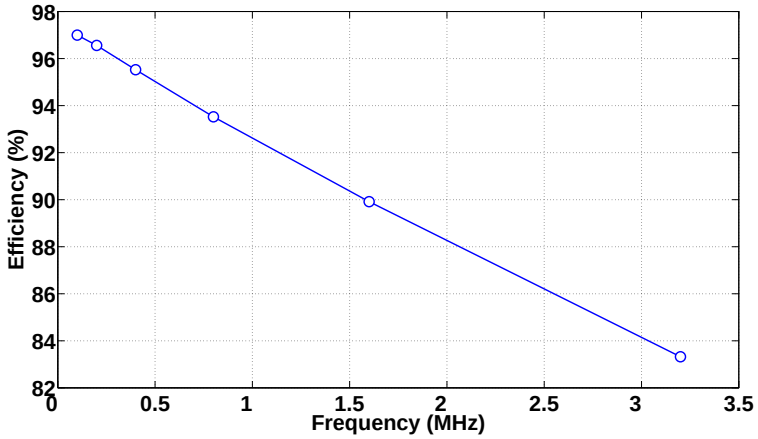


Figure 8.8: Converter efficiency for varying frequency.

8.4 Simulation results

The output voltage of the driver and the negative voltage converter for a 1.6 V_p, 1.25 kHz input is shown in Fig. 8.9. The ripple in the negative voltage is around 12 mV. The driver is simulated with the bond wires of the QFN48 package for slow

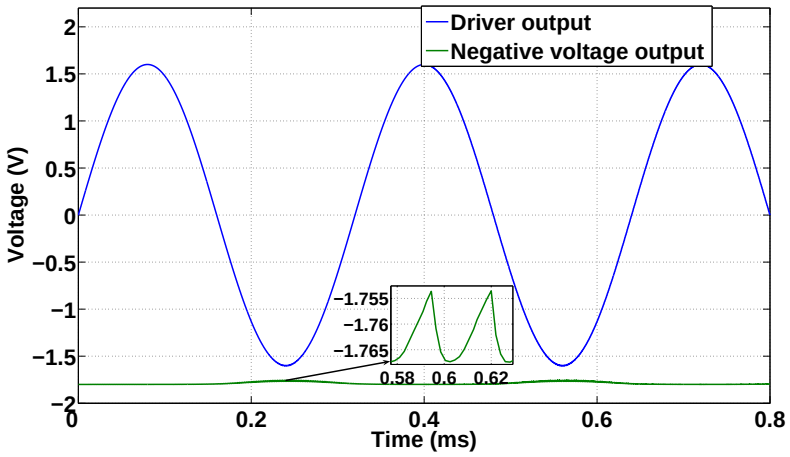


Figure 8.9: Voltage waveforms for 1.6 V_p input.

nMOS and pMOS corner, minimum resistor and capacitor corner at 70^0 C. The $\text{THD} + \text{N}\left(\sqrt{\frac{\text{Harmonic power} + \text{Noise power}}{\text{Signal power}}}\right)$ for an input amplitude varying from 0.1 V_p to 1.6 V_p is plotted in Fig. 8.10. The driver has an efficiency of 63 % for an output power of 80 mW as shown in Fig. 8.10.

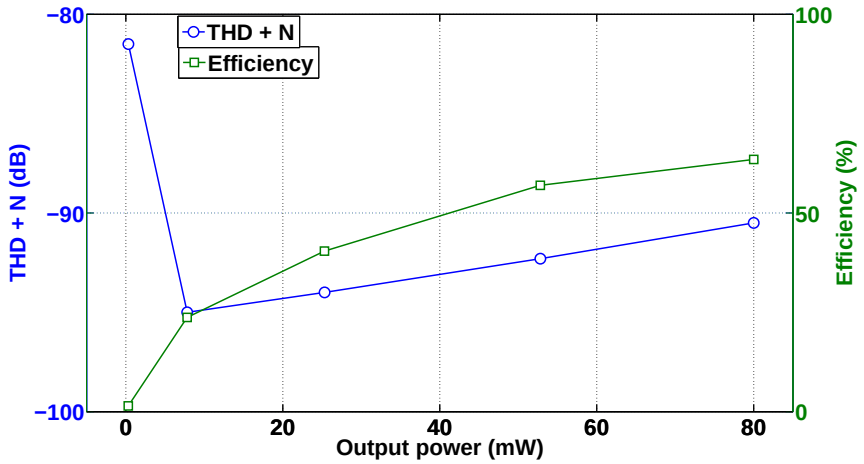


Figure 8.10: THD+N and efficiency of the driver.

8.5 Layout of the headphone driver chip

The headphone driver is integrated with the negative voltage converter and the combined layout is shown in Fig. 8.11. The total area is 1 mm x 1 mm.

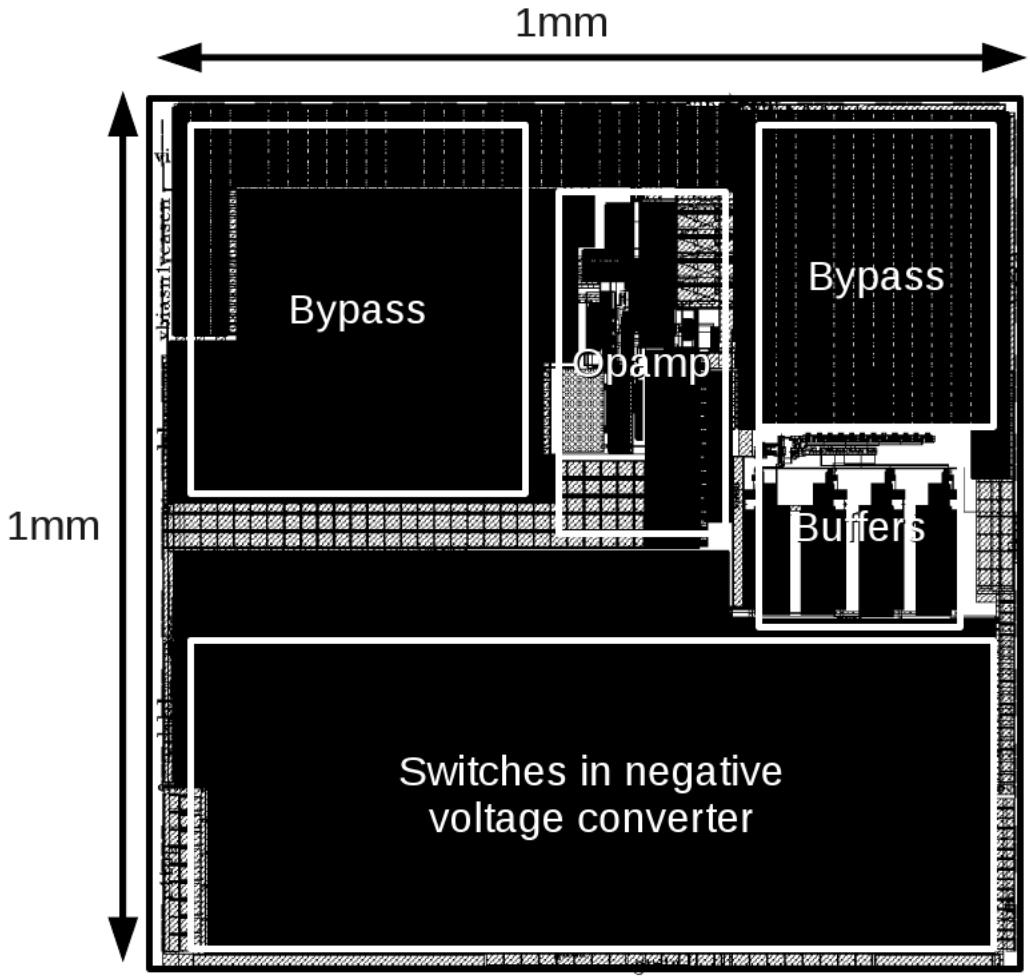


Figure 8.11: Layout of the driver.

CHAPTER 9

Measured Results from the Headphone Driver Chip

9.1 Measurement setup

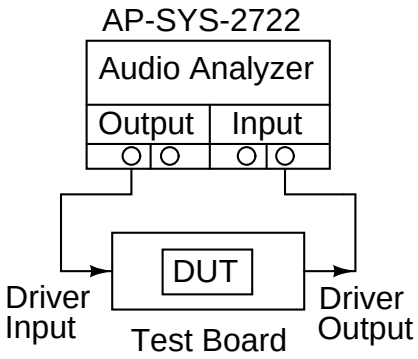


Figure 9.1: Measurement setup.

Fig. 9.1 shows the measurement setup used to test the headphone driver chip. The Audio Precision AP-SYS-2722 audio analyzer is used to give an analog input signal to the driver as well as analyze the driver output signal. The driver performance is measured using external negative supply and with the negative voltage converter.

9.2 Measurement results

9.2.1 With external negative supply

Idle channel noise is measured by grounding the driver input. The idle channel noise is $8\,\mu V_{rms}$. Single ended inputs of different amplitudes and a frequency of 1.25 kHz are given to the driver. Fig. 9.2 shows the THD + N and SNR versus output power.

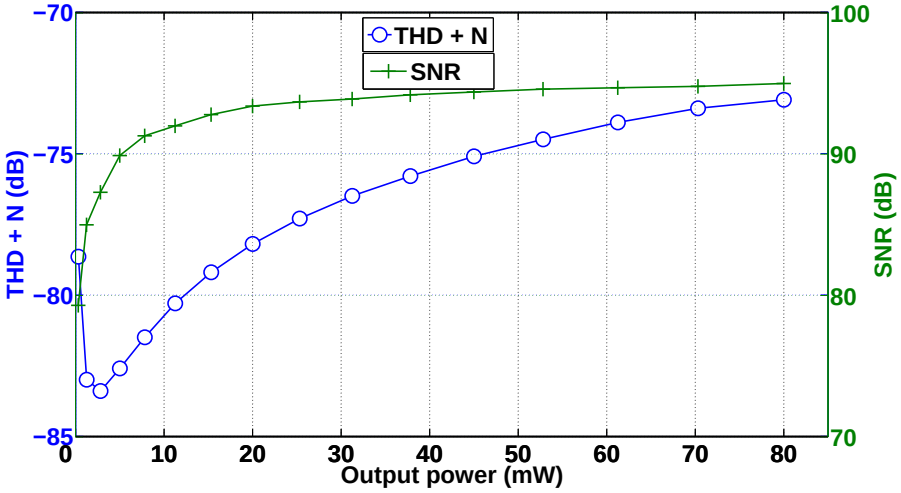


Figure 9.2: THD + N and SNR of the driver.

9.2.2 With negative voltage converter

The switching frequency of the negative voltage converter is 50 kHz. This particular frequency was chosen to optimze the trade-off between the ripple in the negative supply voltage and the loop gain. Idle channel noise is measured by grounding the driver input. The idle channel noise is 10.8 μV_{rms}. Single ended inputs of different amplitudes and a frequency of 1.25 kHz are given to the driver. Fig. 9.3 shows the THD + N and SNR versus output power.

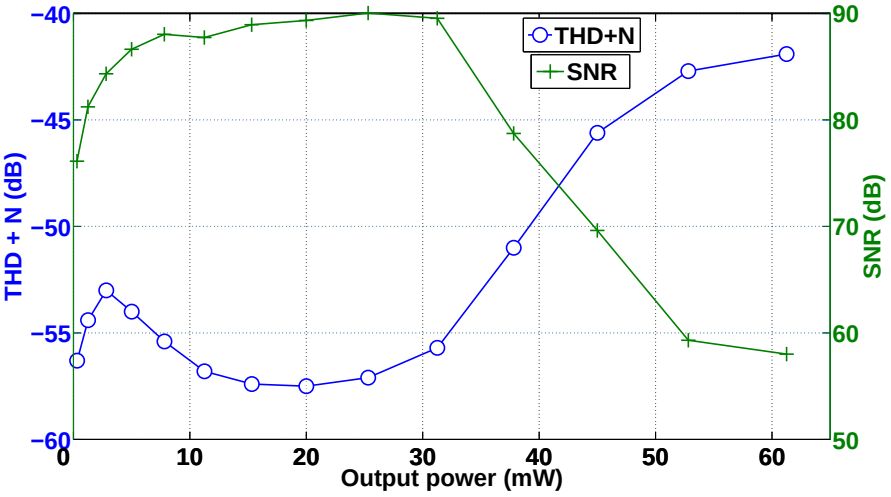


Figure 9.3: THD + N and SNR of the driver.

CHAPTER 10

Conclusions

This thesis deals with the design of high performance frontend blocks for the hearing aid and the 16 Ω headphone driver.

In the first part of the thesis, design of high performance frontend blocks for the hearing aid is described. The measured dynamic range is 106 dB, in a bandwidth of 100 Hz - 9 kHz. A pMOS + nMOS differential input pair enabled low noise, low power PGA design. Linear-in-dB gain steps in the PGA are achieved by linear changes in the resistor values. Techniques like multistage decimation, pipelining and retiming of registers, CSD encoding for the filter coefficients, polyphase structure, and optimal register width are used to reduce the power dissipation in the decimation filter. All the frontend blocks are successfully implemented in a 130 nm CMOS process.

In the second part of the thesis, the design of the high performance headphone driver is described. The driver utilizes a dual supply powered class-AB amplifier to drive the load of 16 Ω. Class-AB operation is achieved by ac coupling of the signal and a simple current mirror based biasing, in a bandwidth of 20 Hz - 24 kHz. The driver achieved a THD $<$ -90 dB for a 1.6 V_p output signal. The driver consumes a quiescent power of 1 mW from a supply of 1.8 V and delivers a maximum power of 80 mW to the load.

APPENDIX A

Resistor values for all the gains in the PGA

Table A.1: Resitor values used in the PGA.

Gain(dB)	R_1**(kΩ)**	R_2**(kΩ)**
-1	167.61	149.37
-0.5	163.05	153.93
0	158.49	158.49
0.5	190.42	200.59
1	185.86	207.82
1.5	181.3	215.05
2	176.74	222.28
2.5	172.17	229.51
3	167.61	236.74
3.5	163.05	244
4	158.49	251.2
4.5	190.42	317.81
5	185.86	329.27
5.5	181.3	340.72
6	176.74	352.18
6.5	172.17	363.63
7	167.61	375.1
7.5	163.05	386.54
8	158.49	398
8.5	190.42	503.87
9	185.86	522
9.5	181.3	540.19
10	176.74	558.35
10.5	172.17	576.52
11	167.61	594.68
11.5	163.05	612.84
12	158.49	631

Gain(dB)	R_1**(kΩ)**	R_2**(kΩ)**
12.5	190.42	798.52
13	185.86	827.31
13.5	181.3	856.09
14	176.74	884.87
14.5	172.17	913.65
15	167.61	942.44
15.5	163.05	971.22
16	158.49	1000
16.5	120.15	798.52
17	117.27	827.31
17.5	114.39	856.09
18	111.51	884.87
18.5	108.63	913.65
19	105.76	942.44
19.5	102.88	971.22
20	100	1000
20.5	75.81	798.52
21	74	827.31
21.5	72.18	856.09
22	70.36	884.87
22.5	68.54	913.65
23	66.73	942.44
23.5	64.91	971.22
24	63.1	1000

Table A.2: Resitor values used in the PGA.

Gain(dB)	$\boldsymbol{R_1}$**(kΩ)**	$\boldsymbol{R_2}$**(kΩ)**
24.5	47.83	798.52
25	46.69	827.31
25.5	45.54	856.09
26	44.39	884.87
26.5	43.25	913.65
27	42.1	942.44
27.5	40.96	971.22
28	39.81	1000
28.5	30.18	798.52
29	29.46	827.31
29.5	28.73	856.09
30	28	884.87
30.5	27.29	913.65
31	26.56	942.44
31.5	25.84	971.22
32	25.12	1000
32.5	19.04	798.52
33	18.59	827.31
33.5	18.13	856.09
34	17.67	884.87
34.5	17.22	913.65
35	16.76	942.44
35.5	16.31	971.22
36	15.85	1000
36.5	12	798.52
37	11.73	827.31
37.5	11.44	856.1
38	11.15	884.87
38.5	10.86	913.65
39	10.58	942.44
39.5	10.29	971.22
40	10	1000

APPENDIX B

Filter coefficients in the decimator

Table B.1: Coefficients of the halfband filter.

Tap weight	Value	CSD
a0, a10	0.0131	$2^{-6} - 2^{-8} + 2^{-10}$
a2, a8	-0.0639	$-2^{-4} - 2^{-10}$
a4, a6	0.3016	$2^{-2} + 2^{-4} - 2^{-6} + 2^{-8}$
a5	0.5	2^{-1}
a1, a3, a7, a9	0	

Table B.2: Coefficients of the FIR lowpass filter.

Tap weight	Value	CSD
a0, a36	0.001	$2^{-10} + 2^{-15}$
a1, a35	-0.0013	$-2^{-9} + 2^{-11} + 2^{-13}$
a2, a34	-0.0008	$-2^{-10} + 2^{-12} - 2^{-15}$
a3, a33	0.003	$2^{-8} - 2^{-10} + 2^{-15}$
a4, a32	-0.0003	-2^{-12}
a5, a31	-0.0057	$-2^{-7} + 2^{-9} + 2^{-13}$
a6, a30	0.004	$2^{-8} + 2^{-15}$
a7, a29	0.0083	$2^{-7} + 2^{-11}$
a8, a28	-0.0118	$-2^{-6} + 2^{-8} - 2^{-13}$
a9, a27	-0.0076	$-2^{-7} + 2^{-12}$
a10, a26	0.0242	$2^{-5} - 2^{-7} + 2^{-10} - 2^{-12} + 2^{-15}$
a11, a25	-0.001	-2^{-10}
a12, a24	-0.0396	$-2^{-5} - 2^{-7} - 2^{-11}$
a13, a23	0.0241	$2^{-5} - 2^{-7} + 2^{-10} - 2^{-12} - 2^{-15}$
a14, a22	0.0547	$2^{-4} - 2^{-7}$
a15, a21	-0.0786	$-2^{-4} - 2^{-6} - 2^{-11} - 2^{-15}$
a16, a20	-0.0659	$-2^{-4} - 2^{-8} + 2^{-11} + 2^{-14}$
a17, a19	0.3084	$2^{-2} + 2^{-4} - 2^{-8} - 2^{-12} + 2^{-15}$
a18	0.5698	$2^{-1} + 2^{-4} + 2^{-7} - 2^{-11}$

Table B.3: IIR highpass: 50 Hz.

Tap weight	Value	CSD
a1	-0.9922	$-2^{0} + 2^{-7}$
k	0.9961	$2^{0} - 2^{-8}$

Table B.4: IIR highpass: 100 Hz.

Tap weight	Value	CSD
a1	-0.9844	$-2^{0} + 2^{-6}$
k	0.9922	$2^{0} - 2^{-7}$

APPENDIX C

Pin details of the hearing aid chip

Fig. C.1 shows the pin details of the hearing aid chip. Table C.1 shows the functionality of each pin.

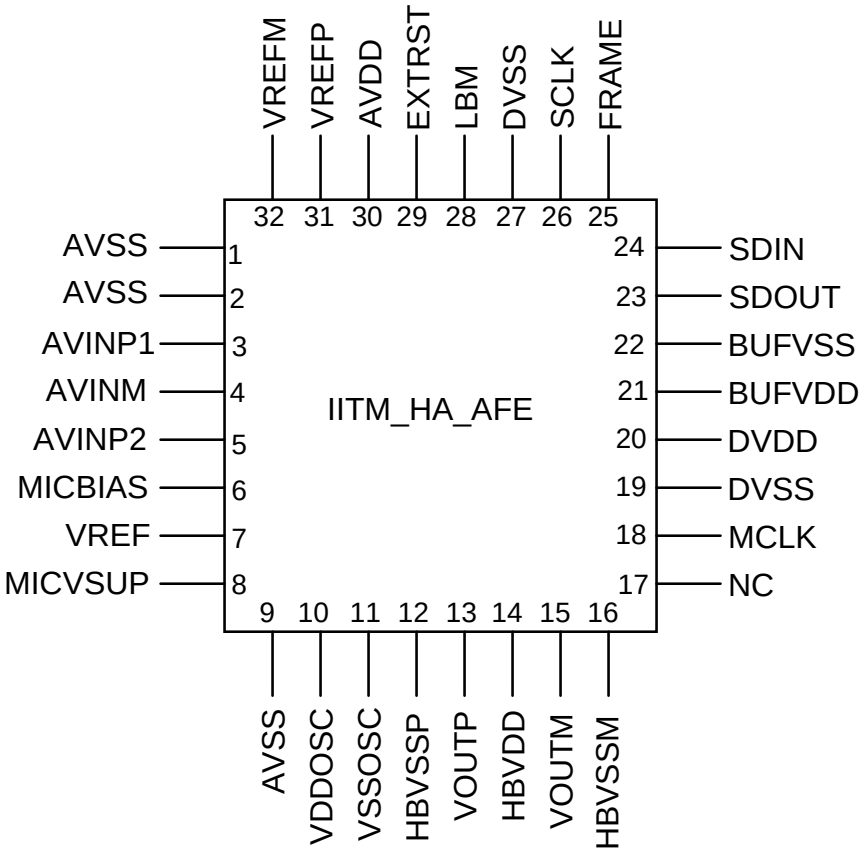


Figure C.1: Hearing aid chip pinout.

Table C.1: Pin details of the hearing aid chip.

Pin No.	**Pin name**	**Pin description**
1, 2, 9	AVSS	Common ground pin
3	AVINP1	Telecoil non-inverting input to the PGA
4	AVINM	Inverting input to the PGA
5	AVINP2	Microphone non-inverting input to the PGA
6	MICBIAS	Source of microphone source follower preamp
7	VREF	Bandgap reference output voltage
8	MICVSUP	Supply voltage for the microphone
10	VDDOSC	Supply voltage for the LDO driving the oscillator
11	VSSOSC	Ground for the ring oscillator
12	HBVSSP	Ground for non-inverting H-bridge amplifier
13	VOUTP	Non-inverting H-bridge output voltage
14	HBVDD	Supply voltage for H-bridge amplifier
15	VOUTM	Inverting H-bridge output voltage
16	HBVSSM	Ground for inverting H-bridge amplifier
17	NC	Not connected
18	MCLK	5 MHz output clock for DSP/μC
19, 27	DVSS	Common ground pin
20	DVDD	Supply voltage for digital circuits
21	BUFVDD	Supply voltage for digital IO buffers
22	BUFVSS	Ground for digital IO buffers
23	SDOUT	Serial data output for digital interface
24	SDIN	Serial data input for digital interface
25	FRAME	Frame signal for digital interface
26	SCLK	Serial shift clock for digital interface
28	LBM	Low battery monitor output
29	EXTRST	External reset
30	AVDD	Supply voltage for analog circuits
31	VREFP	Positive reference voltage for ADC and DAC
32	VREFM	Negative reference voltage for ADC and DAC

APPENDIX D

Pin details of the headphone driver chip

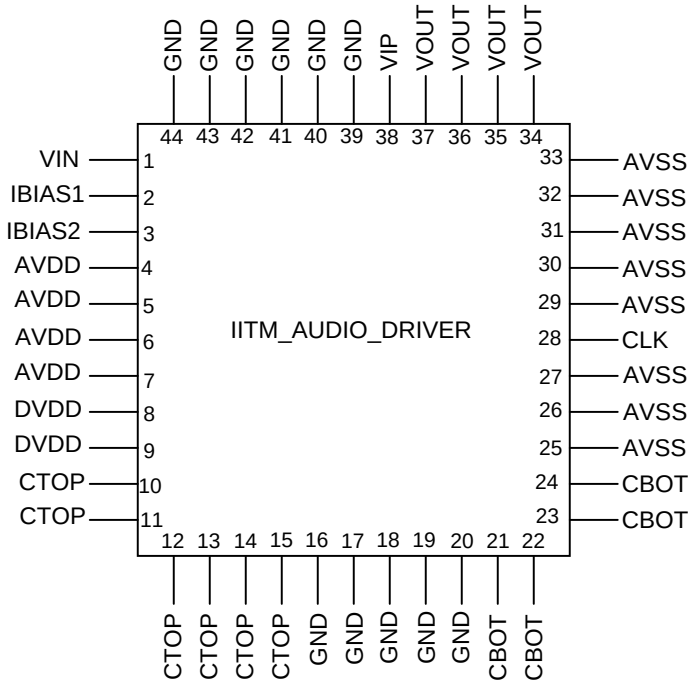


Figure D.1: Headphone driver chip pinout.

Table D.1: Pin details of the headphone driver chip.

Pin No.	**Pin name**	**Pin description**
1	VIN	Input of the driver
2	IBIAS1	Bias current for the first stage($1\,\mu$A)
3	IBIAS2	Bias current for the third stage($1\,\mu$A)
4, 5, 6, 7	AVDD	Positive supply voltage for the driver
8, 9	DVDD	Supply voltage for negative voltage converter
10-15	CTOP	Top pin for external capacitor C1
16-20, 39-44	GND	Common ground pin
21-24	CBOT	Bottom pin for external capacitor C1
25-27, 29-33	AVSS	Negative supply voltage for the driver
28	CLK	Clock input for the negative voltage converter
34-37	VOUT	Output voltage of the driver
38	VIP	Non-inverting input terminal of the driver

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