Design of a 10 KHz Bandwidth Single Bit Continuous Time $\Delta\Sigma$ Modulator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a 10 KHz Single Bit Continuous Time $\Delta\Sigma$ Modulator**, submitted by **Sandeep Jhanwar**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: May 6, 2010

गुरू गोाविन्द दोउॅ खड़े , काके लागूं पांय ।

बलिहारी गुरू आपने , गोाविन्द दियो बताय ।।

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Abbreviations

DSM	$\Delta\Sigma$ Modulator
DT	Discrete Time
CT	Continuous Time
CTDSM	Continuous Time $\Delta\Sigma$ Modulator
DTDSM	Discrete Time $\Delta\Sigma$ Modulator
OBG	Out of Band Gain
OSR	Over-Sampling Ratio
MSA	Maximum Stable Amplitude
STF	Signal Transfer Function
NTF	Noise Transfer Function
SNR	Signal to Noise Ratio
SNDR	Signal to Noise & Distortion Ratio
SQNR	Signal to Quantization Noise Ratio
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
CIFF	Cascade of Integrators with Distributed Feedforward
CIFB	Cascade of Integrators with Distributed Feedback
CMFB	Common Mode Feedback
NRZ	Non-Return to Zero
FS	Full-Scale
$V_{pp,d}$	Volts, Peak to Peak Differential
V_{pp}	Volts, Peak to Peak
FFT	Fast Fourier Transform
PSD	Power Spectral Density

ABSTRACT

First part of this thesis involves designing a $\Delta\Sigma$ modulator for the audio applications. The proposed modulator is operated at 2.56 MHz frequency. It is a single bit modulator having signal bandwidth of 10 KHz. A SNDR of 87 dB is desired at the output of modulator. This modulator is implemented using two architecture CIFF and CIFB. Both the architecture consumes about 36 μW of dynamic power. The design was implemented in UMC 130 nm technology. Area of the each modulator is .7 mm X .4 mm.

In Latter part, the design of PGA (Programmable Gain Amplifier) is also proposed, which is to be used in the front path of a $\Delta\Sigma$ modulator. It is desired to have 90 dB THD in 10 KHz signal bandwidth. PGA consumes about 60 μW of dynamic power.

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CHAPTER 1

Introduction to $\Delta\Sigma$ Modulation

This chapter provides a brief overview of the concepts involved in $\Delta\Sigma$ modulators. We also discuss the choice of architecture for the building blocks of the modulator design presented in this thesis.

$\Delta\Sigma$ modulators are a class of oversampled data converters which employ the technique of feedback to achieve high resolution [1]. The basic architecture of a $\Delta\Sigma$ Modulator is shown in Fig. 1.1.

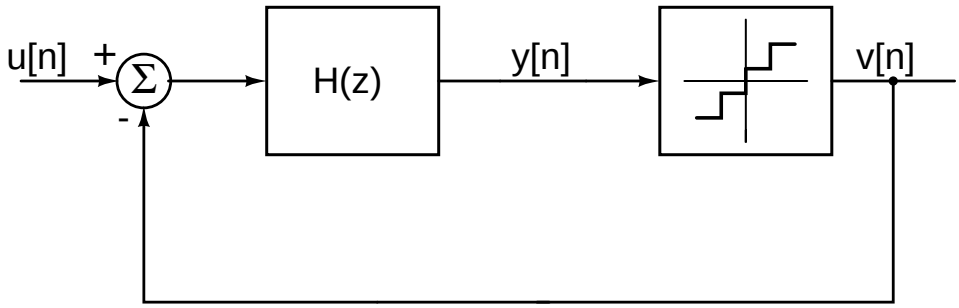


Figure 1.1: Block diagram of a $\Delta\Sigma$ Modulator

The building blocks of a $\Delta\Sigma$ modulator are loop-filter $H(z)$ and a quantizer. The basic idea of $\Delta\Sigma$ modulation is to convert an analog input signal into a digital bit-stream, whose spectrum at low frequency is same as the analog input along with the high frequency quantization noise. Therefore, loop-filter $H(z)$ is low pass in nature. It is designed to have a very high gain in the band of interest. Thus, if the input $u[n]$ is band limited, the output $v[n]$ will be a faithful reproduction of the input signal $u[n]$ along with quantization noise at higher frequencies. In other words, we can say that the quantization noise has been "shaped" away from the input frequency band. At the output of the modulator, a decimator is used to filter out the high frequency quantization noise.

Quantizer is the only non-linear block in $\Delta\Sigma$ modulator. To understand intuitively, how noise "shaping" happens, we can use a linear approximation. Fig. 1.2 shows

a linearized model of a $\Delta\Sigma$ modulator.

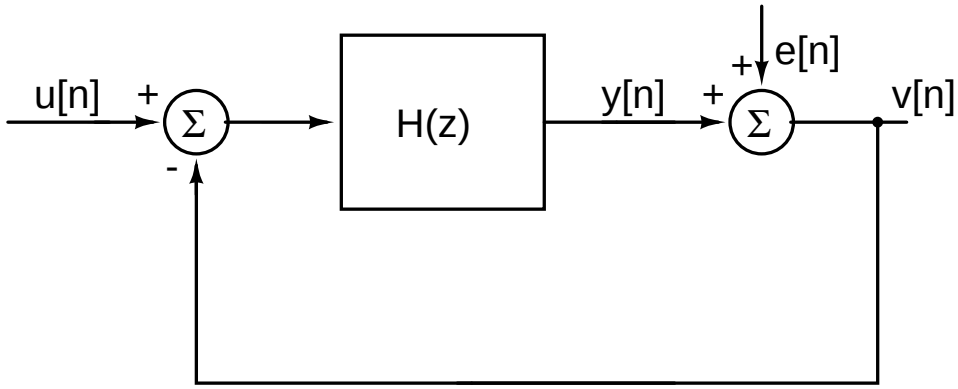


Figure 1.2: Linear model of a $\Delta\Sigma$ Modulator

In the linear model, the quantizer is replaced by an adder, which adds quantization noise $e[n]$ to the loop-filter output. Assumption here is that the quantization noise $e[n]$ is independent of the input signal $u[n]$.

From the linear model, we can write the output $V[z]$ in terms of two independent input $u[n]$ and $e[n]$ as:

$$V(z) = \frac{H(z)}{1+H(z)}\,U(z) \;+\; \frac{1}{1+H(z)}\,E(z) \tag{1.1}$$

$$= STF(z)\,U(z) \;+\; NTF(z)\,E(z) \tag{1.2}$$

Here, $STF(z)$ and $NTF(z)$ represent the Signal Transfer Function and the Noise Transfer Function. If $H(z)$ has a large magnitude in the frequency band of interest, $STF(z)$ will be almost unity, while $NTF(z)$ will be very small. Thus, the quantization noise can be reduced in the band of interest.

As an example, for a first order system $H(z) = 1/(z-1)$, then from Equation 1.1, we get

$$STF(z) \;=\; z^{-1} \tag{1.3}$$

$$NTF(z) \;=\; 1 - z^{-1} \tag{1.4}$$

From Equation (1.3 and 1.4) we see that $STF(z)$ is just a delay while $NTF(z)$ has a high pass response. In fact, $|STF(z)| = 1$ for all the frequencies. And $|NTF(z)| \to 0$ at low frequencies and it increases as we move to higher frequencies, which means that quantization noise is "shaped away" from dc. Therefore, If we want to achieve a very high in-band *Signal to Quantization Noise Ratio* (SQNR), we must choose a sampling rate f_s much higher than the Nyquist rate f_N so that the total quantization noise within the frequency of band of interest is reduced. Hence, $\Delta\Sigma$ Modulators are a class of oversampling data converters. If f_b is the input frequency bandwidth, then the *Oversampling Ratio*(OSR) is defined as

$$OSR = \frac{f_s}{2f_b} = \frac{f_s}{f_N} \tag{1.5}$$

1.1 Choice of Architecture

There are wide range of design choices for the $\Delta\Sigma$ modulators. Major ones are discussed here briefly.

1.1.1 Continuous-Time vs Discrete-Time

Switched-capacitor (SC) circuits form the building blocks of Discrete-time (DT) $\Delta\Sigma$ modulators whereas active-RC integrators forms the building block of Continuous-time (CT) $\Delta\Sigma$ modulators. The key differences in both type of modulators are enlisted here:

- DT modulators are attractive for their high accuracy and linearity.
- DT modulators have better jitter immunity compared to their continuous time counter part. CT modulators have fundamental limitation due to clock jitter[2].
- Since the current waveform in SC filters are impulsive in nature, they are unattractive for use in very high speed designs. The settling time and power

requirements of opamps used in SC filters pose a serious limitation.

- CT loop-filters provide an inherent anti-aliasing. Therefore, it relaxes the design specs of anti-alias filter needed before the modulator. This anti-aliasing property has led to an increase in the usage of CT modulators.

Scope of this thesis is to design a low power $\Delta\Sigma$ modulator for audio applications. A Continuous-time (CT) modulator is the best choice of architecture for an audio system.

The block diagram of a CT $\Delta\Sigma$ Modulator (CTDSM) is shown in Fig. 1.3.

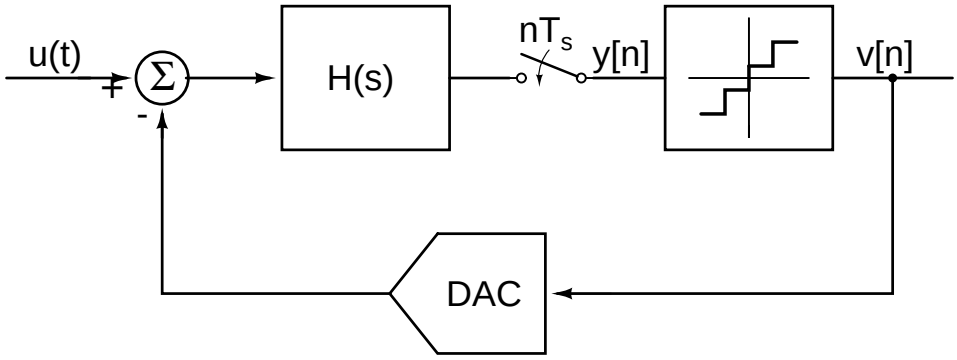


Figure 1.3: Block diagram of a Continuous-Time $\Delta\Sigma$ Modulator

A CT modulator is derived from its DT counterpart by pushing the sampler from outside the loop to within the loop. A feedback DAC is used to convert the digital output $v[n]$ to an analog signal and feed it back to the input of loop-filter. Thus, at the input of the loop-filter signal content is mostly high frequency quantization noise. The maximum frequency of operation in CT modulators are limited by the delay in the quantizers and the feedback DAC while DT modulators are limited by the settling time of the opamps. In general, CT modulators can be operated at a higher frequency than a DT modulator in a given technology [1].

1.1.2 Quantizer Resolution: Single-Bit vs Multi-Bit

Today, in most applications, multi-bit quantizers are the choice of design due to the following de-merits of single-bit modulators.

- Single-bit modulators with *Out of Band Gain* (OBG) greater than 1.5 can cause instability [1]. Hence, only a moderate NTF can be chosen which results in a moderate SQNR.
- Since the input of the loop-filter experiences a large change from sample to sample in a single-bit modulator, opamp slew poses a big challenge. It results in an increase in in-band noise floor. Hence, a very large power needs to be dissipated in the opamp to overcome the problem of slewing. This problem makes a multi-bit modulator more attractive as it results in lesser power consumption. There is a technique of assistant opamp reported in [3] to overcome the slew rate of opamp.
- Since the quantization noise is very high in a single-bit modulator, the *Maximum Stable Amplitude* (MSA) of a single-bit modulator is smaller than that of a corresponding multi-bit modulator for a fixed full-scale and the same NTF.
- Multi-bit modulators provide lower jitter sensitivity because the Least Significant Bit (LSB) size is lower.

However, single-bit quantizers have the advantage that they have very low complexity because the regenerative latch and the feedback DAC have only one bit. Hence, the issue of matching in the comparators of the latch and the feedback DAC do not arise in single-bit modulators. Whereas multi-bit feedback DAC is non-linear because of element mismatch. Non-idealities, such as *Integral Non-Linearity* (INL) and *Differential Non-linearity* (DNL) in the feedback DAC are directly referred at the input and this degrades the performance of Multi-bit modulators

significantly. To overcome the problem of non-idealities, typically methods such as *Dynamic Element Matching* (DEM) [4] are used. But these techniques further increase the power requirements and complexity of the modulator. These problems of multi-bit make single-bit modulators an attractive choice in certain applications.

1.1.3 Order of Loop-filter and Oversampling Ratio

The order of the loop-filter is the maximum power of z in the NTF denominator. The simplest m^{th} order loop-filter is a cascade of m integrators. The noise-transfer function of the m^{th} order modulator is:

$$NTF(z) = (1 - z^{-1})^m \tag{1.6}$$

For an m^{th} order modulator with an oversampling ratio of OSR, Δ as the Least Significant Bit (LSB) of the quantizer, it can be shown that the in-band quantization noise power is [4]:

$$N_q = \frac{\Delta^2}{12} \cdot \frac{\pi^{2m}}{2m+1} \left(\frac{1}{OSR} \right)^{2m+1} \tag{1.7}$$

From Equation 1.7, we see that increasing both the order of the modulator and the OSR decreases the quantization noise power. Choosing a higher OSR is always beneficial, but the given technology puts a upper limit on it. Increasing the order of the modulator results in the reduction of the MSA. Hence, to achieve a desired SNR, we need to trade off the order of the modulator with the OSR. Zeros of the NTF can be optimized to achieve a better SNR for a given order of the modulator as per the method mentioned in [1].

1.2 Design Specifications

The aim of this project is to design a CTDSM having 14 bit resolution (SNR - 87 dB) in a 10 KHz bandwidth. A single-bit quantizer is chosen for simplicity of design. The problem of opamp slewing is overcome by the method of *Assisted Opamp Technique*. It is fully explained in Chapter 2 [3]. A third order modulator with optimization of zeros is chosen and the OSR used is 128. This means that the sampling rate is 2.56 MHz. A resistive feedback DAC is chosen for simplicity. The pulse shape of the DAC is chosen to be *Non-Return to Zero* (NRZ). The modulator is designed in UMC 130 nm technology with a 1.2 V supply. The full scale (FS) of the quantizer is assumed to be 2.4 $V_{pp,d}$.

Table 1.1 summarizes the specifications of the design of the modulator.

Table 1.1: Design Specifications

Input Bandwidth	10 KHz
Resolution	14 bits
SNDR	87 dB
Sampling Rate	2.56 MHz
Supply Voltage	1.2 V
FS of quantizer	2.4 $V_{pp,d}$
Technology	130 nm CMOS

CHAPTER 2

Loop-Filter Design

As stated earlier, a third order modulator with optimized zeros and an OSR of 128 is used for the current design. Thus, the NTF that is to be realized is derived from the *Schreier* Toolbox in MATLAB and is given by:

$$NTF(z) = \frac{(z-1)(z^2 - 1.9996z + 1)}{(z - 0.6693)(z^2 - 1.531z + 0.6638)} \tag{2.1}$$

From the NTF, the loop-filter response $H(z)$ can be determined by

$$H(z) = \frac{1}{NTF(z)} - 1 \tag{2.2}$$

$$= \frac{0.7995(z^2 - 1.64z + 0.695)}{(z-1)(z^2 - 1.9996z + 1)} \tag{2.3}$$

The modulator with the NTF given in Equation 2.1 was simulated in MATLAB. To determine the Maximum Stable Amplitude (MSA) a slow ramp was given at the input and the loop-filter output (or the quantizer input) was measured. Fig. 2.2 shows the plot of quantizer input versus input amplitude. MSA is maximum amplitude at which the modulator is stable. From Fig. 2.2, we see that the modulator is stable up to 0.78 FS or 1.872 $V_{pp,d}$. For safety margins we will take MSA as 90% of this value. So, the MSA is 0.7 FS or 1.68 $V_{pp,d}$. The Power Spectral Density (PSD) of the output at MSA is shown in Fig. 2.1. The peak SNR obtained is 110 dB.

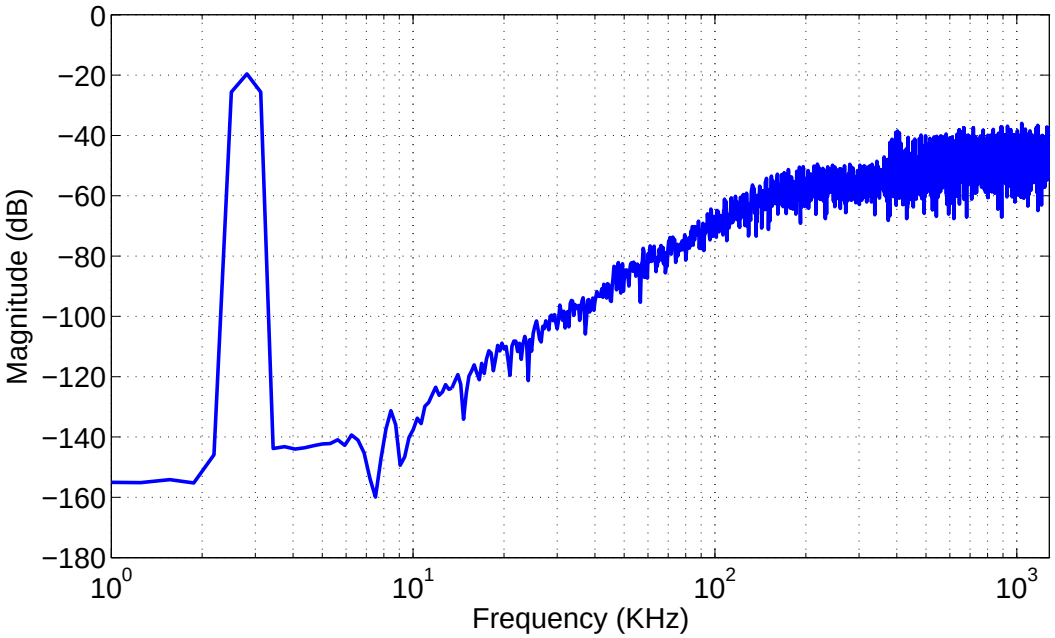


Figure 2.1: PSD of a ideal modulator

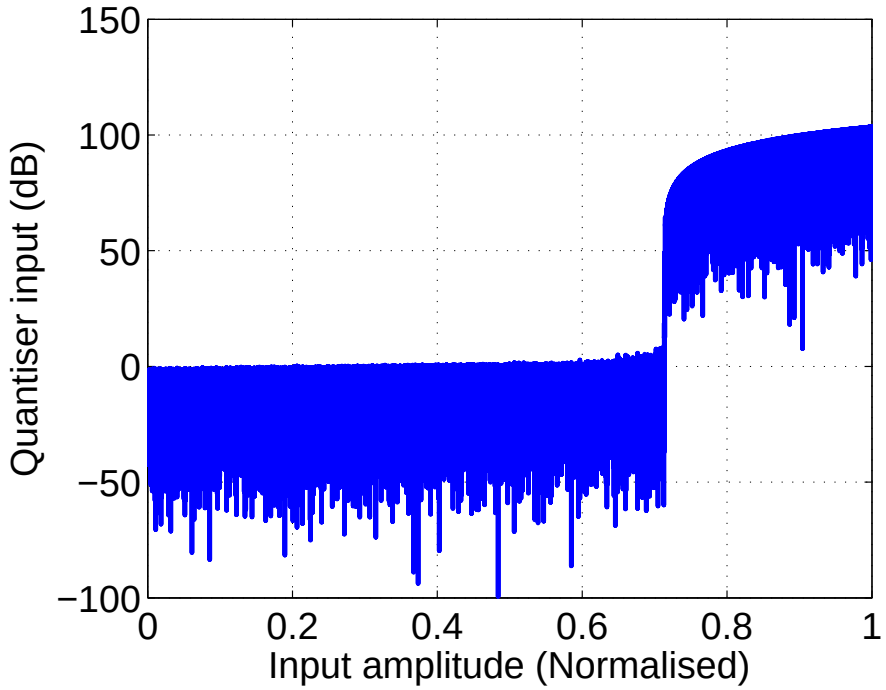


Figure 2.2: MSA estimation

2.1 CT/DT Equivalence

If we want to realize the above discrete-time loop-filter response in a CT modulator with an NRZ DAC, the sampled value of the DAC pulse response of the CT loop-filter should be same as the impulse response of the DT loop-filter. Fig. 2.3 shows the DT and the CT implementations of the loop-filter.

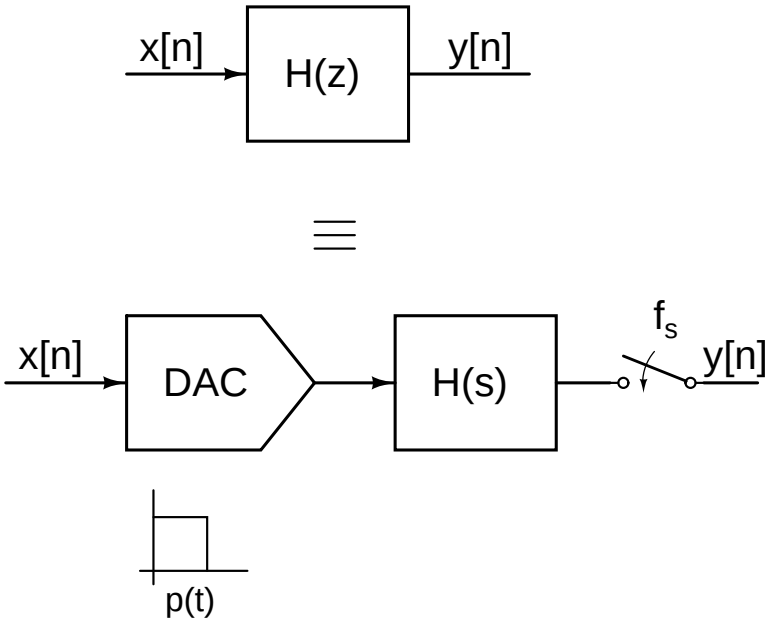


Figure 2.3: Equivalence of CT and DT loop-filters

The two systems shown in Fig. 2.3 are identical if [5]

$$Z^{-1}\{H(z)\} = L^{-1}\{P(s)H(s)\}|_{t=nT_s} \tag{2.4}$$

where P(s) represents the pulse response of the DAC. This transformation of the DT response to the CT response is called as the impulse invariance transform [6]. Thus, for a CT modulator with NRZ DAC, one can write the CT loop-filter response from MATLAB as

$$H(s) = \frac{0.6703}{s} + \frac{0.2439}{s^2} + \frac{0.0437}{s^3} \tag{2.5}$$

This is the transfer function for prototype CT loop-filter for our design. This CT

loop-filter can be implemented either using CIFF architecture or CIFB architecture. We would require a cascade of three integrators in both the cases. The optimization zeros of the NTF are realized using the feedback factor β. Fig. 2.4 shows the block diagram implementation of the prototype CT loop-filter using CIFF architecture. This section deals with the implementation of CIFF loop-filter. We will discuss CIFB implementation in the next section.

The integrators in the above loop-filter are realized using opamp-RC structures. From the prototype filter, the actual implementation of the loop-filter is realized after frequency and node scaling.

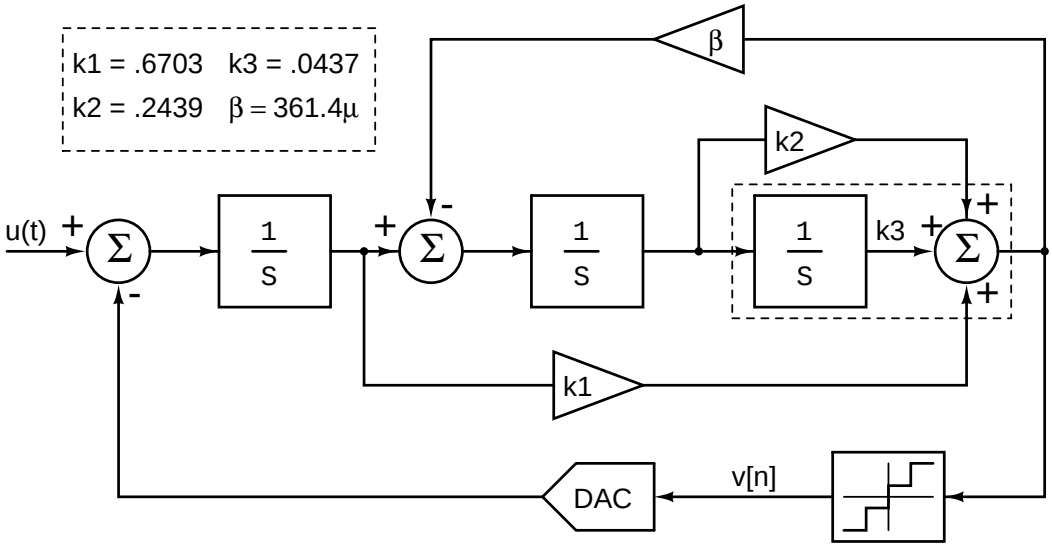


Figure 2.4: Prototype of the CIFF Loop-Filter

CT loop-filter response in Equation 2.5 is equivalent to the DT loop-filter response in Equation 2.2 if the sampling frequency is 1 Hz. Since our sampling frequency is f_s we need to scale the $H(s)$ accordingly. Therefore, scaling of $H(s)$ is done by changing s to s/f_s in Equation 2.5. So, the new loop-filter response is $H(s/f_s)$.

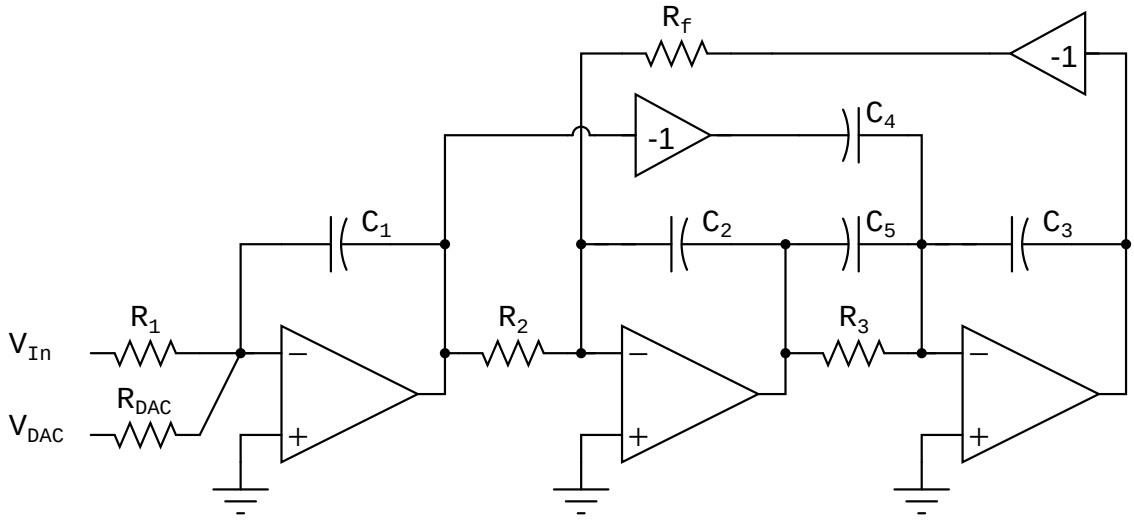
Opamp output nodes are scaled such that that they have peak-to-peak differential swings of 600 $\mathrm{mV_{pp,d}}$ approximately. Node scaling ensures that the output of the opamps do not saturate due to high swing and performance of the modulator does not deteriorate.

Excess loop delay is an important problem in CTDSM. The excess loop delay arises because of the non-idealities in the integrators and the summer used in the loop-

filter, delay in the regeneration time of the quantizer and the delay in the feedback DAC. This is particularly problematic in the case of high-speed circuits. If the excess loop delay is not compensated for, the modulator may become unstable. Since our band of interest is low frequencies, excess loop delay is not an issue in this design.

2.2 Circuit Implementation of CIFF Loop-Filter

Fig. 2.5 shows the circuit diagram of the CIFF loop-filter used in the modulator design. A new architecture is proposed for summing the loop-filter coefficients as oppose to conventional CIFF architecture, which does not require additional summing opamp.



R_1 = 240 kΩ	R_f = 145.3 MΩ	C_3 = 129.85 fF
R_2 = 1.2 MΩ	C_1 = 9.76 pF	C_4 = 087.04 fF
R_3 = 15 MΩ	C_2 = 1.49 pF	C_5 = 145.12 fF
R_{DAC} = 240 kΩ		

Figure 2.5: Circuit Diagram of CIFF Loop-Filter

2.2.1 Choice of Components

The most critical resistor in terms of the design of the loop-filter is the first integrating resistor R_1 and feedback DAC resistor R_{DAC}. The thermal noise contributed by these resistors is directly referred to the input and should be chosen carefully. Since we are targeting the SNDR of 87 dB, and SQNR of a ideal loop-filter is 110 dB, we can safely assume that SNDR is going to be dominate by the input referred thermal noise. First integrating opamp in loop-filter also is a main contributors to the input referred noise. Noise split between loop-filter & input and feedback resistors is roughly 50% each. A margin of 3 dB is kept in the design. So, we choose input and feedback resistors such that the total input referred thermal SNR is 90 dB for an input signal at MSA.

With these factors in mind, R_1 and R_{DAC} is chosen to be 240 kΩ. The noise due to the other integrating resistors and the feedback resistors are scaled down by the gain of the first integrator and hence, do not contribute to the input referred noise significantly. Hence, R_2 is chosen to be 1.2 MΩ.

Since we are using the third opamp as summing amplifier as well, we want the capacitor loading of this opamp to be minimum. Therefore, to have the same UGF of the third integrator, third integrating resistor has to increase. We have chosen R_3 as 15 MΩ. Since this is a very large value of the resistor, a **t-network** scheme shown in Fig. 2.6 is chosen for implementation of third integrating resistor to save the layout area. Thus, summing capacitors $C_3,\ C_4,\ C_5$ can be kept at minimum. Further increasing the value of the resistor, decreases the integrating capacitors to very small values and it would be difficult to realize them accurately.

For a t-network shown in Fig. 2.6 node "x" is connected to second integrator's output and "y" is connected to third integrator's virtual ground node. Impedance looking in from "x" is still $R_{t1} + R'_{t1}||R_{t2}$ ($\approx R_{t1}$ if $R_{t2} \ll R'_{t1},\ R_{t1}$), but current gain $\frac{I_y}{I_x}$ has reduced by a factor of $(R_{t2} + R'_{t1})/R_{t2}$). Therefore, next integrating stage sees it as a huge resistor of value R given in Equation 2.6

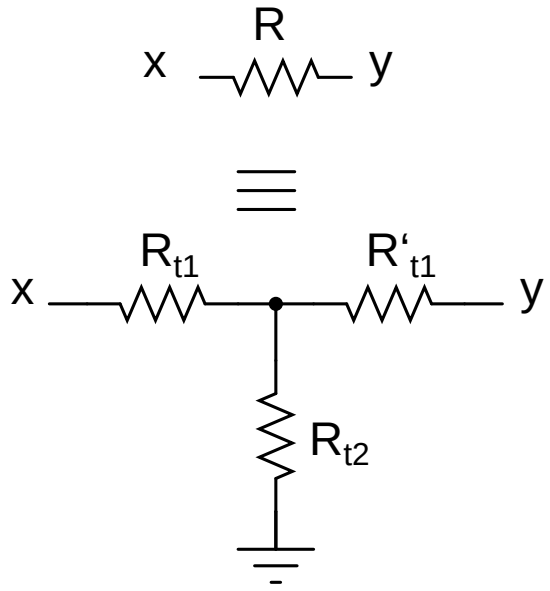


Figure 2.6: T-network implementation of third integrating resistor

$$R = R_{t1}\left(\frac{R'_{t1}}{R_{t2}} + 1 + \frac{R'_{t1}}{R_{t1}}\right) \tag{2.6}$$

$$R \approx \frac{R_{t1}R'_{t1}}{R_{t2}} \tag{2.7}$$

Generally R_{t1} and R'_{t1} are chosen much larger than R_{t2}. Therefore, Equation 2.7 holds true in our case. We have chosen $R_{t1} = R'_{t1}$ for simplicity. For a 15 MΩ of R_3 we have R_{t1} as 1.25 MΩ and R_{t2} 125 kΩ.

We see that t-network implementation of R_3 has reduced the sizes of resistors used. It has to be noted that having a t-network does not give any advantages in the input referred noise. The input referred noise at "x" will increase due to this t-network scheme. Noise of resistor R'_{t1} when input referred to "x" will get multiplied by current gain $\frac{I_x}{I_y}$. So, this gives the input referred noise approximately equal to a resistor of the value $\frac{R_{t1}R'_{t1}}{R_{t2}}$.

The full scale of the modulator is 2.4 $V_{pp,d}$. This means that the summing opamp must support the entire supply range, which is difficult to implement in practice. Since the quantizer is single-bit, only the sign of the output of the loop-filter is relevant but not its magnitude subject to the constraint that the quantizer

does not become metastable. So, we can scale the capacitors and resistor which ensures that the total output swings of the all the opamps are within $600\,\mathrm{mV_{pp,d}}$. Therefore, we are implementing loop-filter coefficients as $k_i/6$ instead of k_i. The capacitors values for the new coefficients are

$$C_1 = 9.765\,\mathrm{pF} \tag{2.8}$$

$$C_2 = 1.492\,\mathrm{pF} \tag{2.9}$$

$$C_3 = 129.85\,\mathrm{fF} \tag{2.10}$$

$$C_4 = 87.04\,\mathrm{fF} \tag{2.11}$$

$$C_5 = 145.12\,\mathrm{fF} \tag{2.12}$$

Having chosen the integrating capacitors, the notch resistor is chosen such that

$$\frac{1}{R_f\,C_2\,R_3\,C_3} = \beta f_s^2 \tag{2.13}$$

This gives $R_f = 145.3\,\mathrm{M\Omega}$. Since this is again a huge value of the resistor. This is also implemented using the t-network scheme with R_{t1} as $1.13\,\mathrm{M\Omega}$ and R_{t2} as $8.93\,\mathrm{k\Omega}$, so that area is minimized.

2.3 Capacitive Summing

Third integrating capacitor C_3 act as a summing capacitor also. The coefficients are realized by connecting the outputs of first two integrators, to the input of last integrator via capacitors C_4 and C_5 respectively. This scheme obviates the use of a separate summing amplifier. Since we are saving the power required in the summing opamp, this capacitive summing scheme, makes the design low power. The sizes of these capacitors are kept at minimum so that the phase margin and bandwidth of the summing opamp do not suffer much. In other words, we should

not burn extra power in the integrators to compensate for the capacitive loading. The loop-filter coefficients implemented are

$$k1 = \frac{1}{R_1 C_1} \cdot \frac{C_3}{C_4} = \frac{0.6703}{6} \tag{2.14}$$

$$k2 = \frac{1}{R_1\, C_1\, R_2\, C_2} \cdot \frac{C_3}{C_5} = \frac{0.2439}{6} \tag{2.15}$$

$$k3 = \frac{1}{R_1\, C_1\, R_2\, C_2\, R_3\, C_3} = \frac{0.0437}{6} \tag{2.16}$$

2.4 RC Tuning

The capacitors and resistors used in the design of the loop-filter vary across process-corners. In 130 nm technology, resistors vary by ±23% and capacitors vary by ±15%. Therefore, the RC time constant of the integrators can roughly vary by ±40%. If the RC time constant becomes too low, the OBG increases and can push the modulator towards instability. On the other hand, if the RC time constant increases, the in-band noise floor goes high and results in a deterioration of SQNR. Hence, a course tuning of the resistors and capacitors is required to ensure that the modulator doesn't go into instability or result in a deterioration of SNR.

In this design, we employ tuning in both capacitors and resistors. A *two* bit tuning in both resistors and capacitors is employed, which means that we have 16 levels for tuning. This ensures that the RC time constant is within 5% of the nominal value. Fig. 2.9 and Fig. 2.10 shows the capacitive and resistive banks respectively.

Tuning bits for capacitors are $cb1$ & $cb0$, and for resistors are $rb1$ & $rb0$. Signals a_{1-3} and b_{2-4} are the outputs of decoders as shown in Fig. 2.7 and Fig. 2.8.

For tuning in notch resistor R_f only R_{t1} is tuned using bits a_{1-3}, while R_{t2} is kept constant.

The capacitors C_3, C_4, C_5 are very small in their size. To realize the loop-filter coefficients only the ratio of these capacitors matters, so, we are not tuning these

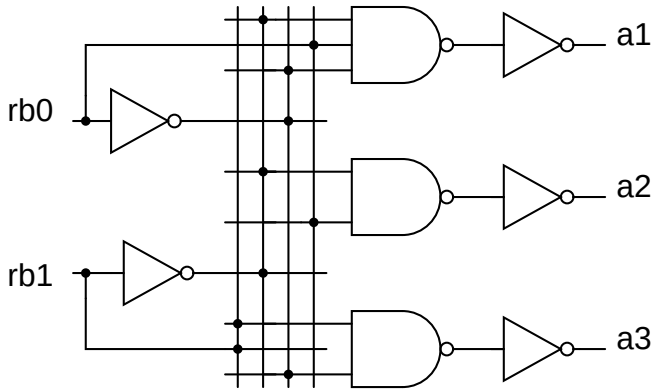


Figure 2.7: Circuitry for First Decoder

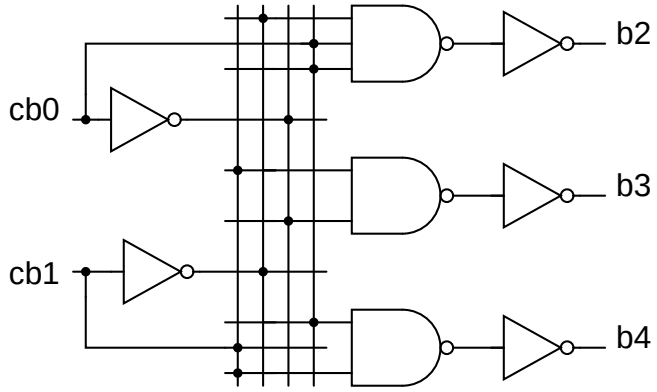


Figure 2.8: Circuitry for Second Decoder

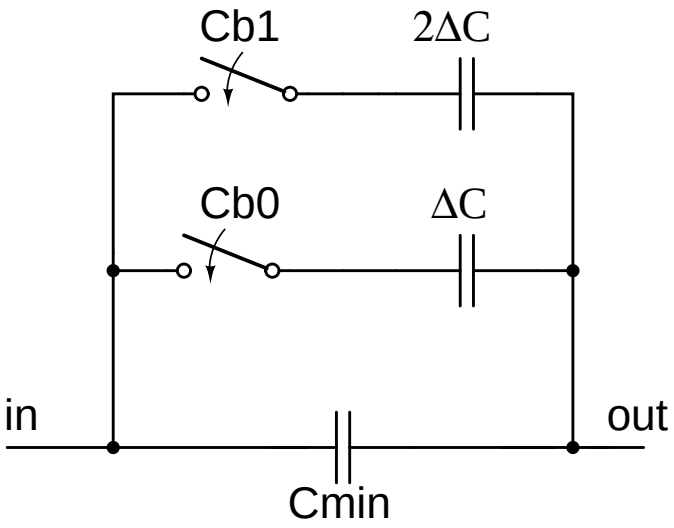


Figure 2.9: Capacitor Bank

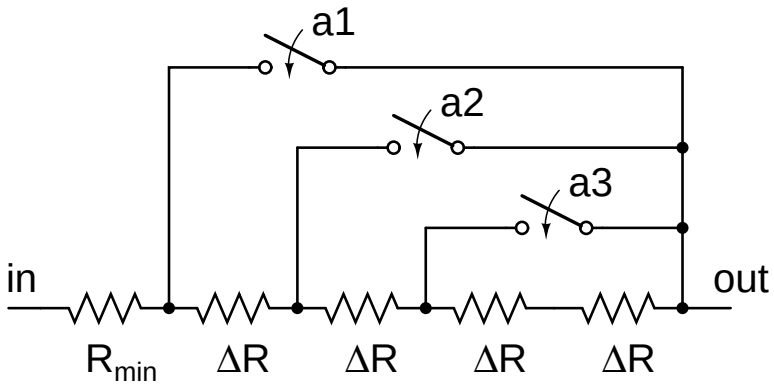


Figure 2.10: Resistor Bank

capacitors. Therefore, to track the RC time constant of the final integrator, tuning for variation in both resistor and capacitor is done in the t-network itself as shown in Fig. 2.11. R_{t1} is tuned to track the resistor process corners and R_{t2} is tuned to track capacitor process corners. When it is *cap-max* corner R_{t2} is increased, which results in decrease in R_3 according to the Equation 2.6. And Similarly at the *cap-min* corner R_{t2} is decreased, which results in an increase in R_3. Since the variation in C_3 is $\pm 15\%$, R_{t2} also is design to have the same variation roughly.

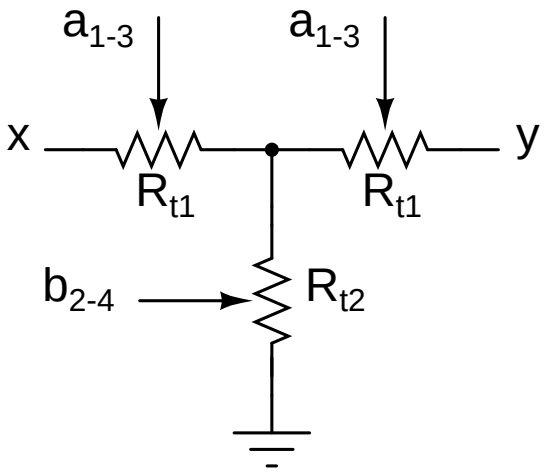


Figure 2.11: T-network tuning for both Resistor & Capacitor Variation

2.5 Opamp Design

In this section, we will discuss the design of the opamps used in the loop-filter. We will also discuss the method of *Opamp Assistance*, which helps in reducing the distortion introduced by the first opamp.

2.5.1 First Integrating Opamp

The first integrating opamp is the most critical opamp in the design of the loop-filter. The noise of the first opamp reflects directly at the input and the it is also the main contributor for distortion.

To choose the architecture of the opamp to be used, we need to arrive at the specifications required for the design. Firstly, the opamp has to have a large enough DC gain such that it does not degrade the SNR significantly. It can be shown that if the DC gain A > OSR [7] then SNR does not to degrade significantly. The output and the input common mode levels of opamp should be identical and the noise of the opamp should be such that input referred thermal SNR is 90 dB at MSA. Output of the opamp should have the swing of $600\,\mathrm{mV_{pp,d}}$. With these specifications, we can conclude that it has to be a two stage opamp.

Feed-forward Compensated architecture

Feed-forward compensated opamps are used for the loop-filter design. Fig. 2.12 shows the block diagram of a feed-forward compensated opamp. We can write the transfer function of such an opamp as

$$H(s) = \frac{Gm_1Gm_2 + Gm_3G_{01} + sC_1Gm_3}{(sC_1 + G_{01})(sC_2 + G_{02})} \tag{2.17}$$

The transfer function has two poles at G_{01}/C_1 and G_{02}/C_2 and one zero at $(Gm_1Gm_2 + Gm_3G_{01})/C_1Gm_3$. A Miller opamp uses the dominant pole compensation. Whereas in a feed-forward opamp poles remains where they were, instead a zero is introduced using the feed-forward path Gm_3. This results in

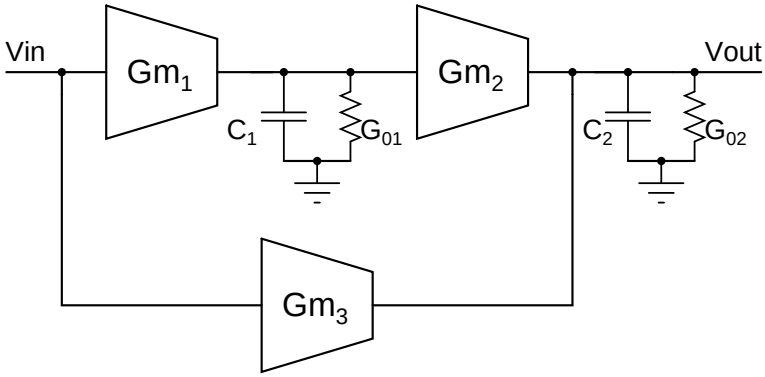


Figure 2.12: Feed Forward Architecture

better bandwidth compared to the Miller architecture consuming same amount of power. Of course, this comes at an expense of output swings. Since opamp output nodes are scaled and swings requirement is only $600\,\mathrm{mV_{pp,d}}$, we can use this architecture. The DC gain is

$$\frac{Gm_1Gm_2 + Gm_3G_{01}}{G_{01}G_{02}} \tag{2.18}$$

Gm_1 is decided by the first stage noise and Gm_2 is chosen according to the UGF requirement. Gm_3 introduces the zero for frequency compensation of the opamp. This zero needs to be much lower than the Unity Gain Frequency (UGF) of the opamp, then we will get a first order (20 dB/decade) roll off at the UGF for opamp stability.

Technique of Opamp Assistance

Fig. 2.13 shows the circuit diagram of an active-RC integrator. We can model the opamp as a transconductor block g_m. The nonlinearity in the opamp arises due to the fluctuations in the virtual ground node, and the nonlinear dependence of the output current to the input voltage of the opamp.

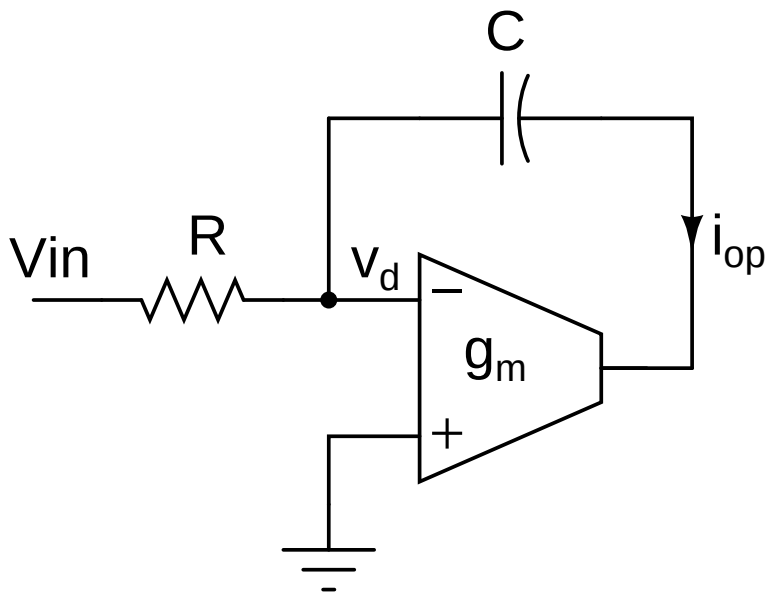


Figure 2.13: Active RC Integrator

We can write the non-linear output current as

$$i_{op} = g_m v_d - g_3 v_d^3 \tag{2.19}$$

Thus, we see that the non-linearity increases as v_d increases. We can roughly write v_d as

$$v_d = \frac{V_{in}}{1 + g_m R} \tag{2.20}$$

Therefore, by increasing the loop gain $g_m R$, we can reduce v_d and thus, reduce non-linearity. But, R is fixed because of design constraints and increasing g_m would result in more power consumption in the opamp.

The main function of the opamp is to maintain the virtual ground at input node, such that integration happens without any errors. But in this process, it has to supply all the current through capacitor C and hence, arises the non-linearity. Since the feedback DAC current has NRZ pulse shape, opamp needs to have high slew rate. Hence, if there is an external element which supplies the current through capacitor C, the current supplied by the opamp will reduce and so as the

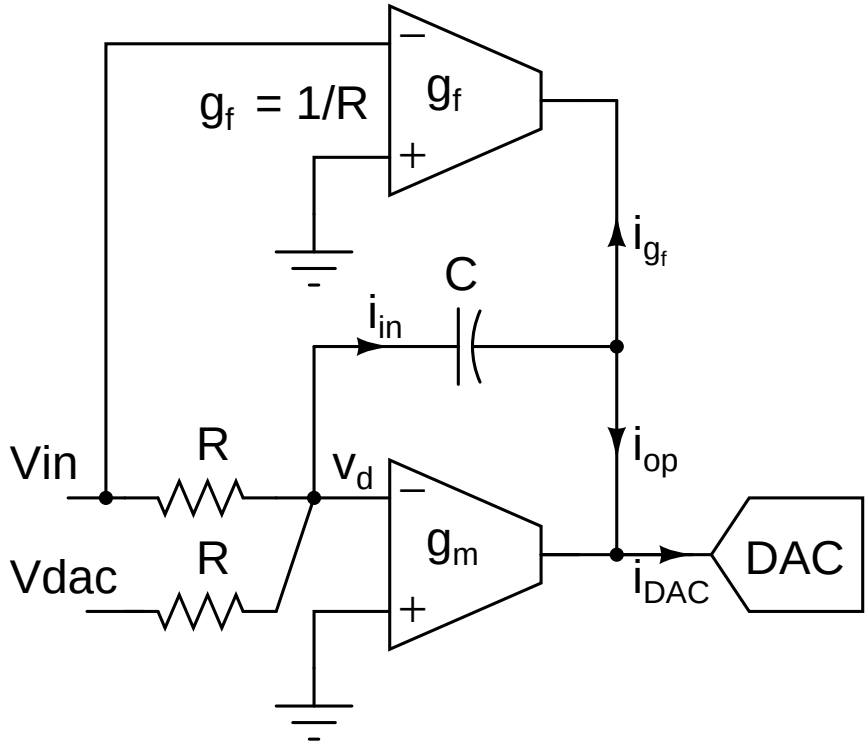


Figure 2.14: Technique of Opamp Assistance

non-linearity.

Fig. 2.14 shows the technique of *Opamp Assitance*, wherein, an additional DAC and a transconductor block G_f supply the DAC current and the input current respectively at the output of the opamp. This ensures that the opamp supplies only the "error current" between the input and the output currents, thereby reducing the non-linearity. Also, the power and the slew rate requirements of the opamp are significantly reduced.

Design of First Integrating Opamp

Fig. 2.15 shows the circuit diagram of the input stage of first integrating opamp. The main contributor to the total noise is this stage. Flicker noise is of a main concern for us, because the bandwidth of interest is 100 Hz to 10 KHz. Therefore, to reduce the flicker noise, PMOS input stage is chosen. Furthermore, the input transistors M4a,b are chosen to have a length of 2 um and tail NMOS transistors M9a,b have the length of 10 um. Since tail NMOS transistors have large lengths,

they provide high enough output impedance, comparable to PMOS side and hence, NMOS cascode is not needed. The total input referred thermal noise voltage spectral density of the opamp can be roughly written as

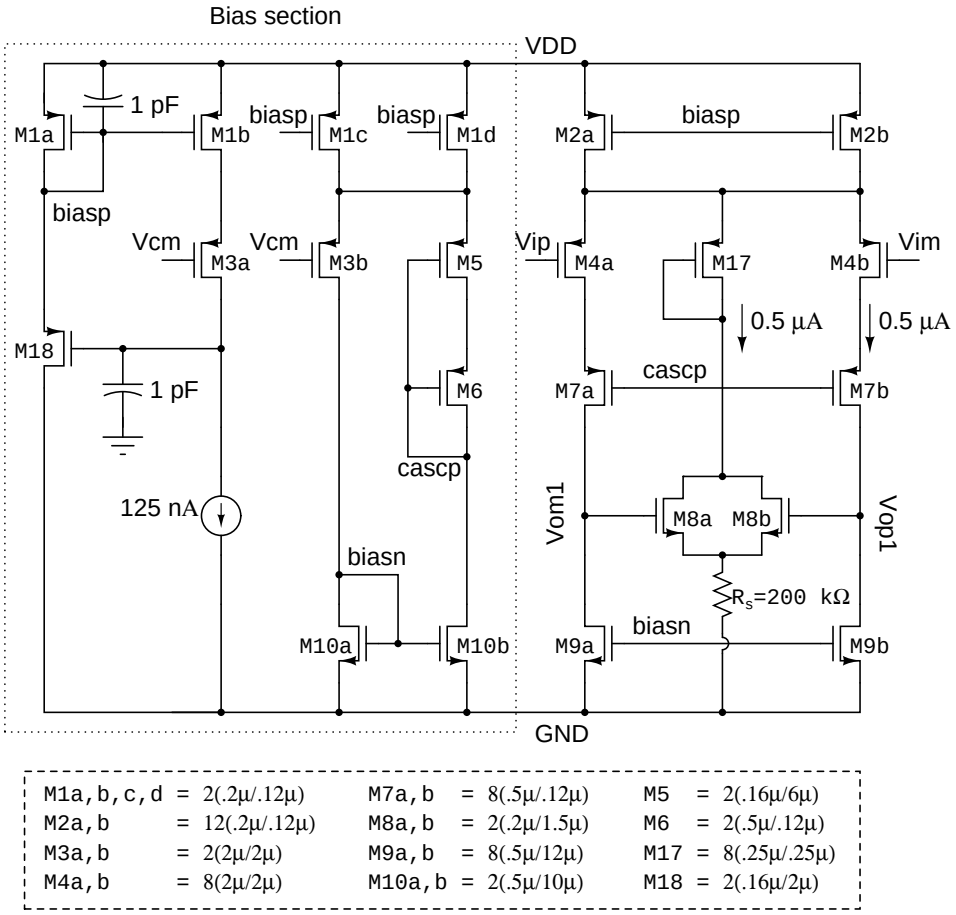


Figure 2.15: First Stage of First Integrating Opamp

$$S_n(f) = \frac{16kT}{3g_{mp}}\left(1 + \frac{g_{mn}}{g_{mp}}\right) + \frac{1}{C_{ox}f}\left(\frac{K_p}{W_pL_p} + \frac{K_n}{W_nL_n}\cdot\frac{g_{mn}^2}{g_{mp}^2}\right) \tag{2.21}$$

where g_{mp} and g_{mn} are the transconductances of the transistors M4a,b and M9a,b respectively. Thus, to reduce the input referred noise, we have chosen a large g_{mp} and a small g_{mn} accordingly. Input referred noise of the opamp, stand alone, is $6.4\,\mu\mathrm{V_{rms}}$. Since the loop gain around the loop-filter is (R_{DAC}/R_1) 1, input referred noise voltage of the opamp will get doubled *i.e.* $12.8\mu\mathrm{V_{rms}}$ when put in loop-filter.

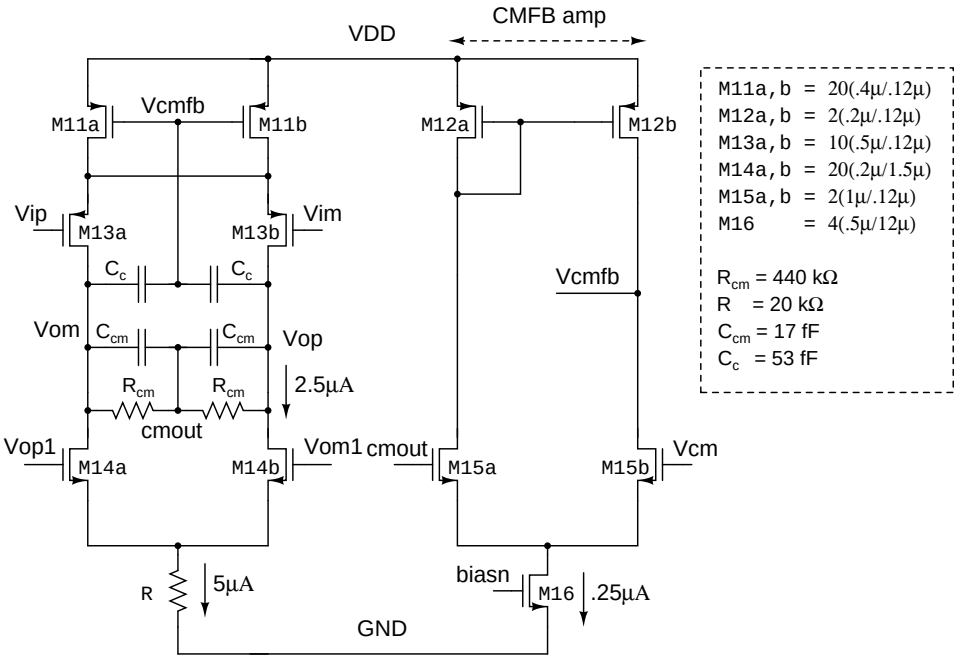


Figure 2.16: Second Stage of First Integrating Opamp

The drain voltages of transistors M9a,b are decided by the transistors M8a,b and at *"ff"* process corner (low V_T corner) not enough V_{GS} of M8a,b can cause significant increase in G_{ds} of M9a,b. This will reduce the first stage DC gain and thus deteriorate the overall performance of the loop-filter. Therefore, A resistance R_s of 200 kΩ is put up at the source of M8a,b. This resistance carries a voltage drop of 100 mV to provide sufficient headroom to M9a,b at all process corners. We have ensured that at *"ss"* process corner PMOS cascodes are not going in triode region.

Fig. 2.16 shows the schematic for the second stage. The second stage is designed such that it carries enough load current to supply the second stage integrating resistors R_2, the summing capacitor C_4 which realizes the coefficient k_1 and also the common mode sensing circuit. The current to be supplied to the integrating capacitor C_1 is taken care by the replica block consisting of feed-forward DAC and the G_m block. A margin should be kept in second stage current to provide the error current between replica block and the input current. Transistors M14a,b are scaled version of M8a,b and this determines the second stage current. Scaled version R of R_s is also copied in the output stage.

CMFB Circuitry

The feed-forward opamp has two stages of common-mode feedback. The first-stage CMFB loop consists of the transistors, M4a,b, M7a,b, M8a,b, M17 and R_s. If the common-mode level of V_{om1} and V_{op1} decreases, the currents in M8a,b will decrease, which in turn will decrease the current in M17. Since the total tail current is constant, this will result in an increase in current in M4a,b, thus helping in bringing up the common mode output level of the first stage.

The second-stage CMFB loop has the common-mode sensing resistors R_{cm} and the feedback loop ensures that the common-mode level is fixed to V_{cm}. We add additional capacitors C_{cm} in parallel to R_{cm} which helps in sensing high frequency common mode jumps. Since the CMFB loop is a two stage, we need to compensate it by adding a miller capacitance C_c to stabilize the loop.

Fig. 2.17 shows the magnitude and phase responses of the first integrating opamp. Table 2.1 summarizes the opamp characteristics. Fig. 2.18 shows the common-mode step response of the first opamp.

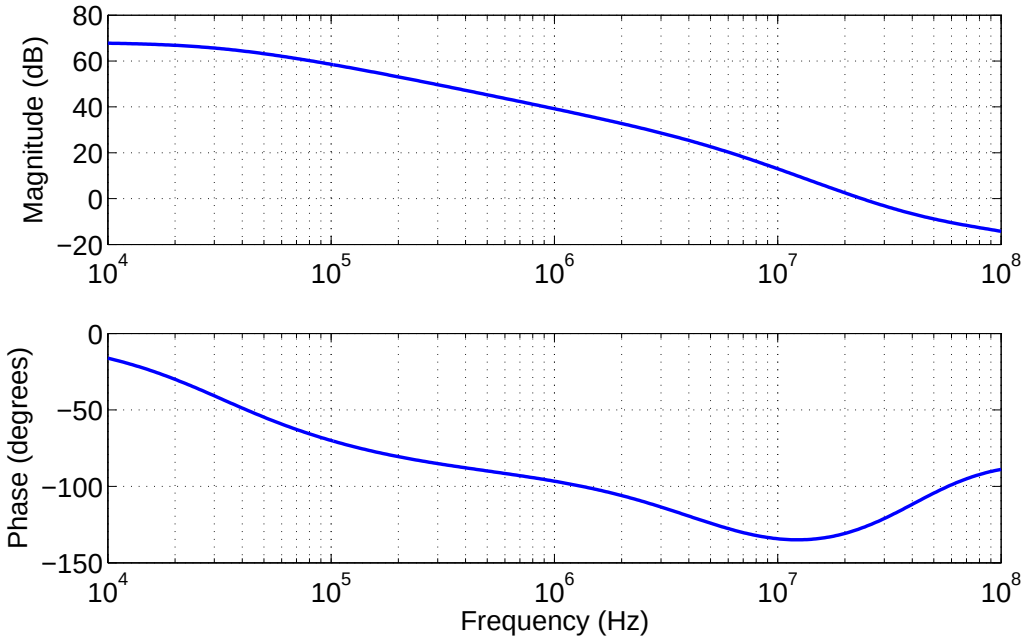


Figure 2.17: First Integrating Opamp's AC Response

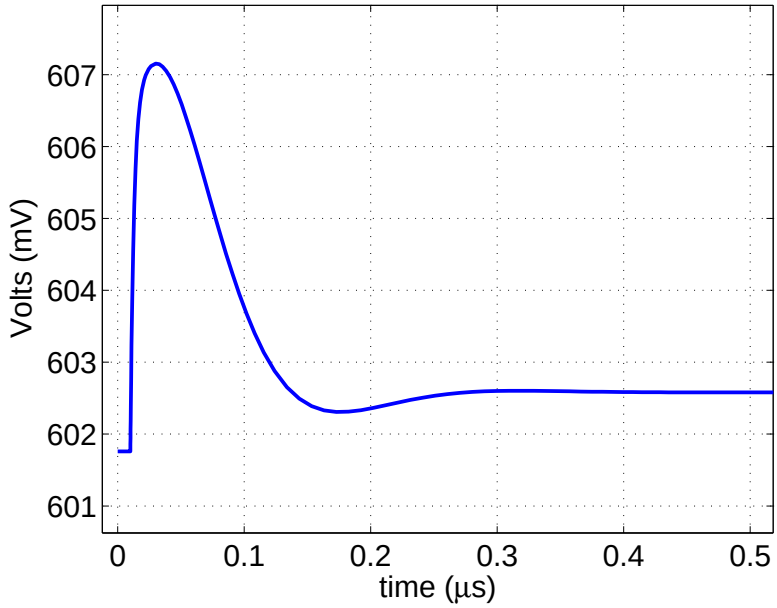


Figure 2.18: First Integrating Opamp's Common Mode Step Response

Table 2.1: First Opamp Characteristics

DC Gain	67 dB
UGF	23.77 MHz
Phase Margin	52.75°
Input Referred Noise	12.8 μV_{rms}
Power consumption	8.75 μW

2.5.2 Second Integrating Opamp

The second integrating opamp has relaxed constraints on DC gain and input referred noise. Hence, a NMOS input stage is chosen to have a relatively higher bandwidth for the same current. And output stage current is kept such that it can supply enough load current. Hence, we choose an output stage tail current of $2\,\mu$A. Fig. 2.19 shows the circuit diagram of the first stage and Fig. 2.20 shows the corresponding second stage.

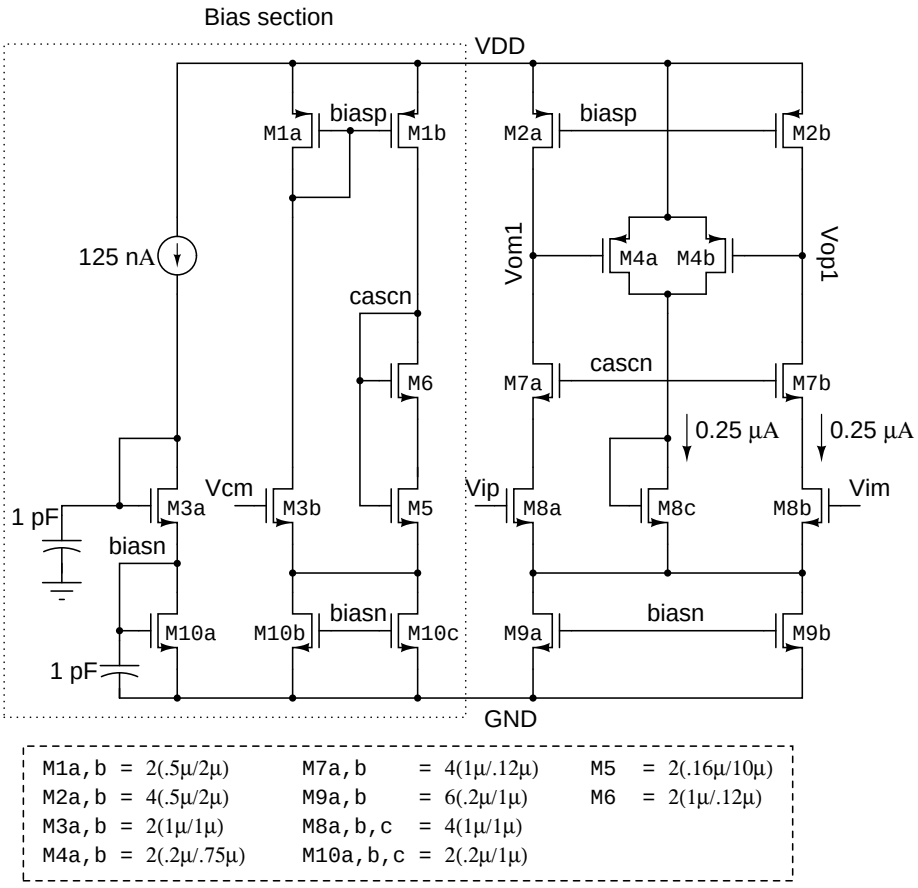


Figure 2.19: First Stage of Second Integrating Opamp

Fig. 2.21 shows the magnitude and phase responses of the second integrating opamp. Table 2.2 summarizes the opamp characteristics. Fig. 2.22 shows the common-mode step response of the second opamp.

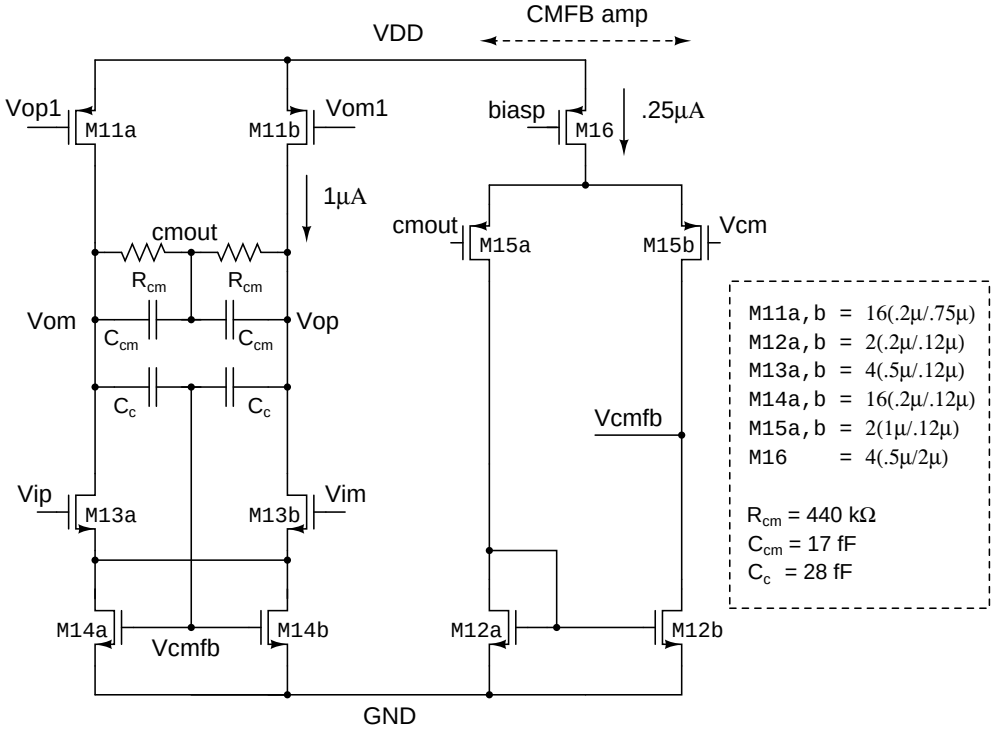


Figure 2.20: Second Stage of Second Integrating Opamp

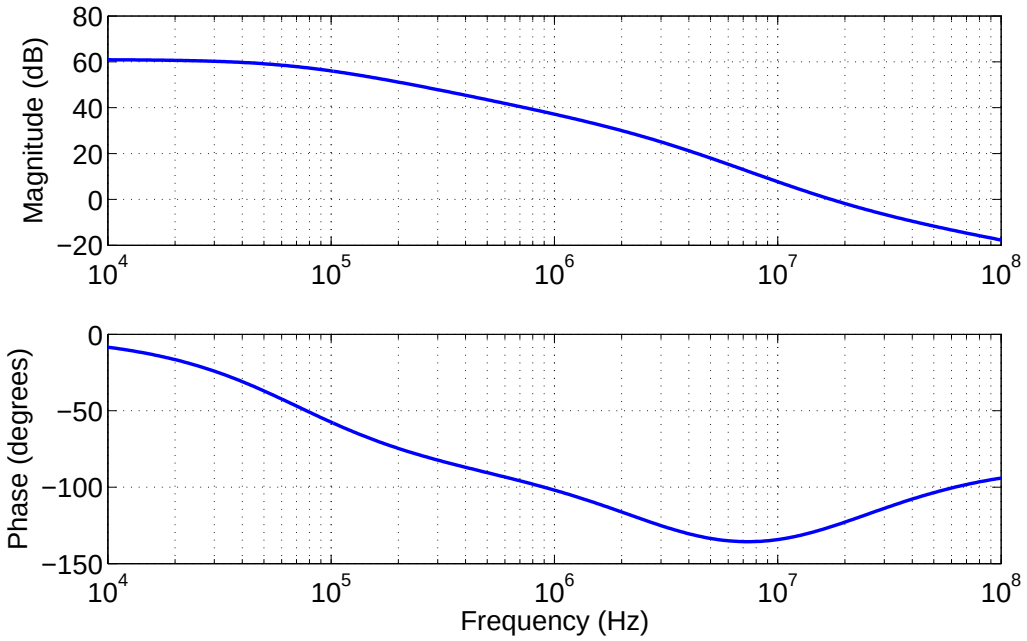


Figure 2.21: Second Integrating Opamp's AC Response

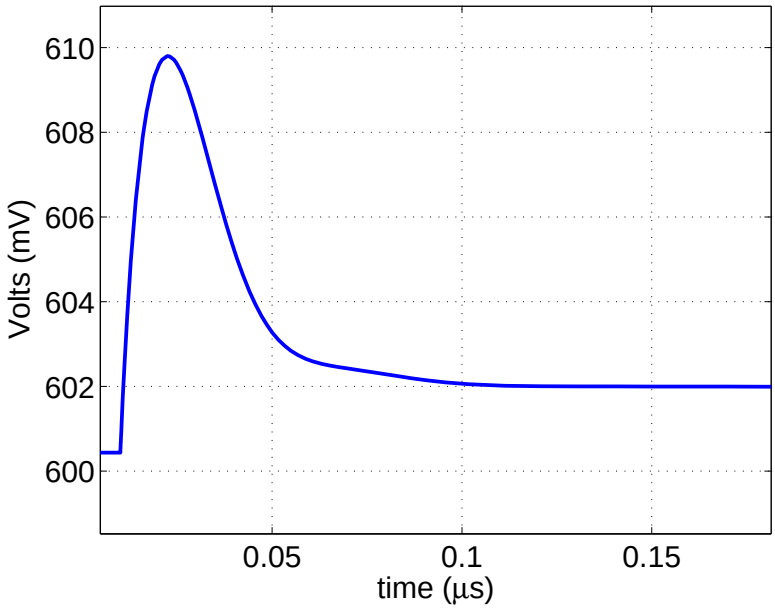


Figure 2.22: Second Integrating Opamp's Common Mode Step Response

Table 2.2: Second Opamp Characteristics

DC Gain	62.2 dB
UGF	17.36 MHz
Phase Margin	54.17°
Power consumption	4.2 μW

2.5.3 Summing Opamp

Since summing opamp is loaded by capacitors at its input, it has to burn more power to get the required UGF. To reduce the power, we made sure that sizes of capacitors are kept minimum by doing node scaling. Summing opamp is a scaled version of the second opamp. First stage is chosen same as second opamp. A tail current of 3μA is desired in the second stage. Fig. 2.23 shows the circuit diagram of the first stage and Fig. 2.24 shows the corresponding second stage.

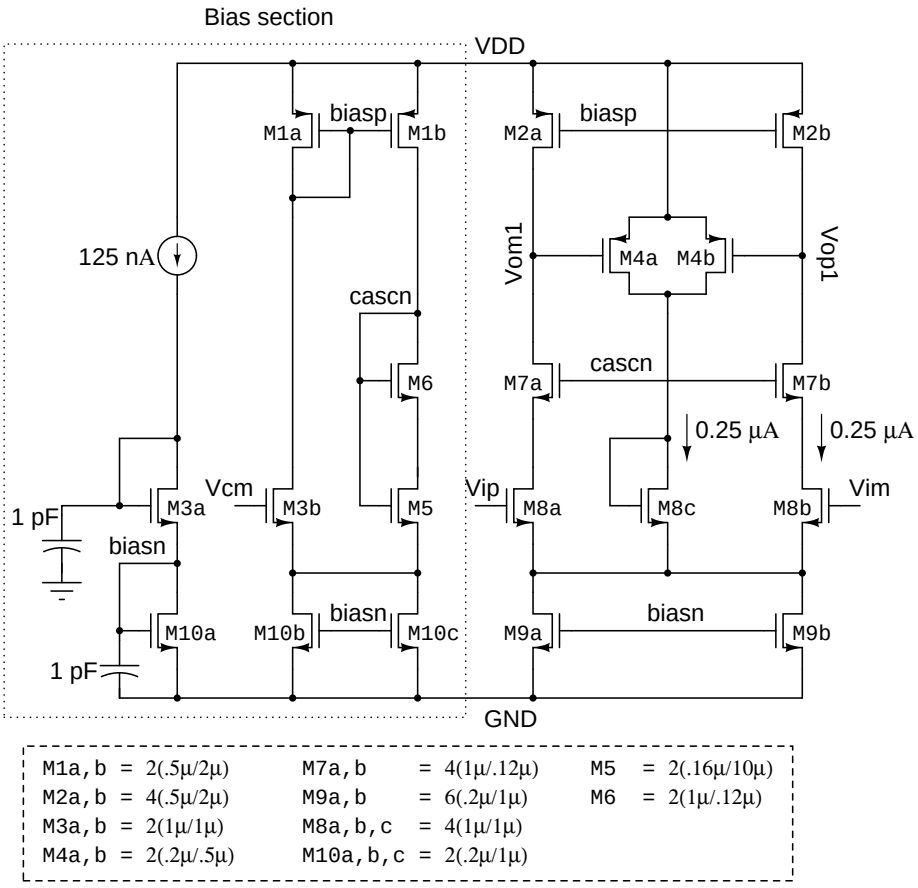


Figure 2.23: First Stage of Summing Opamp

Fig. 2.25 shows the magnitude and phase responses of the summing opamp. Table 2.3 summarizes the Opamp characteristics. Fig. 2.26 shows the common-mode step response of the summing opamp.

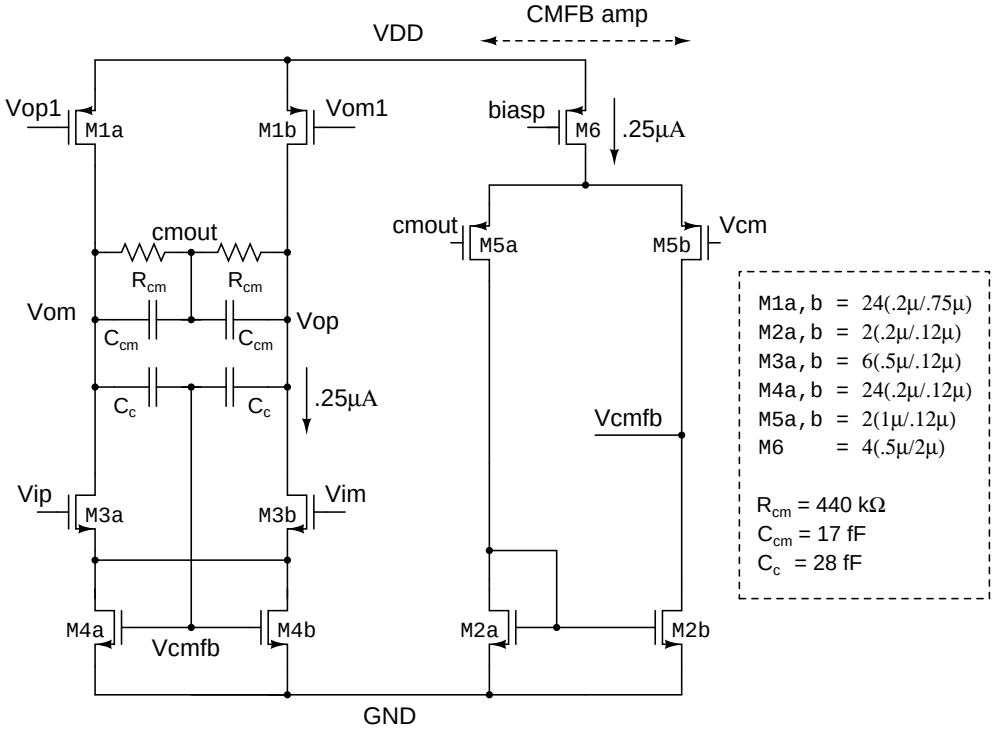


Figure 2.24: Second Stage of Summing Opamp

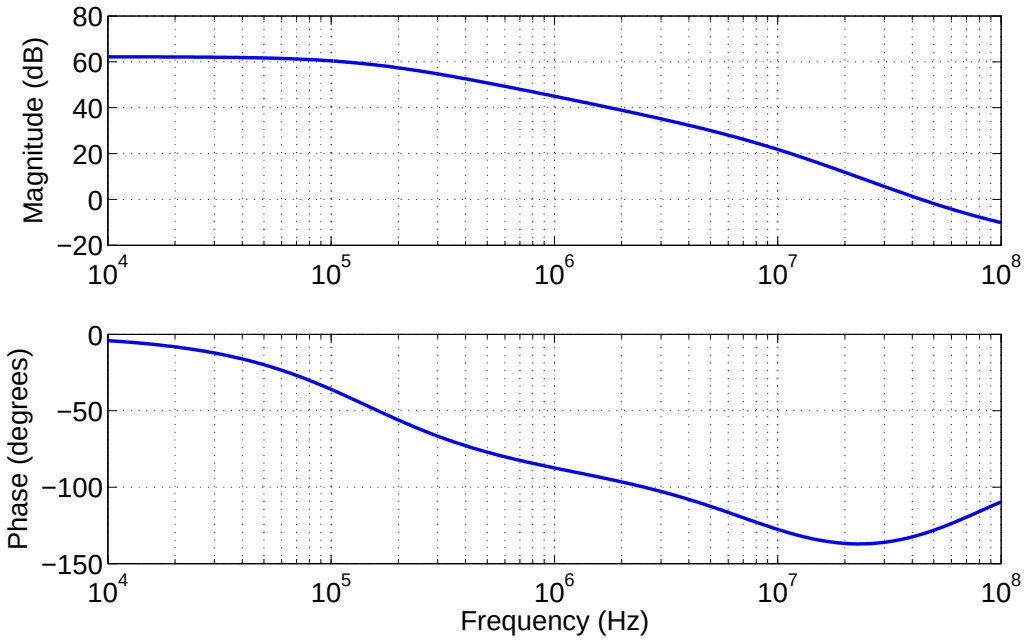


Figure 2.25: Summing Opamp's AC Response

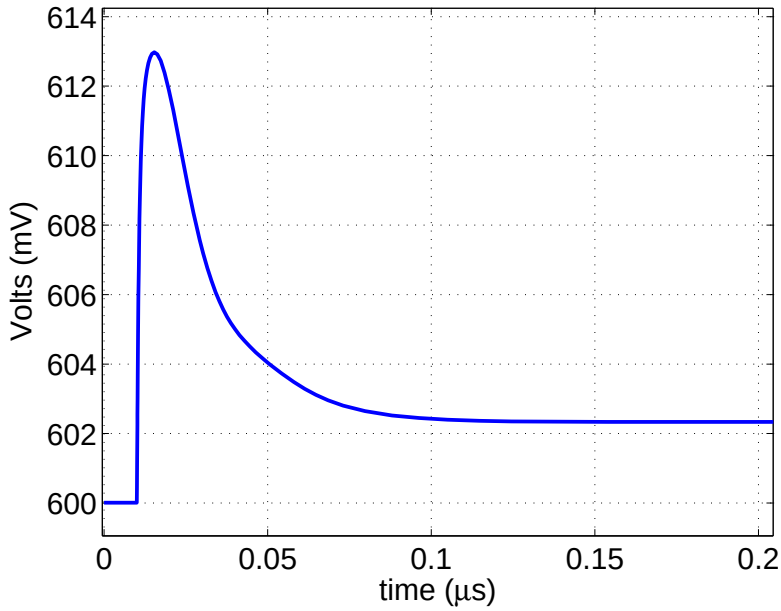


Figure 2.26: Summing Opamp's Common Mode Step Response

Table 2.3: Summing Opamp Characteristics

DC Gain	62 dB
UGF	43.3 MHz
Phase Margin	49.3°
Power consumption	5.4 μW

2.6 Circuit Implementation of CIFB Loop-Filter

Fig. 2.27 shows the prototype loop-filter for CIFB implementation. A CIFB architecture does not require a separate summing amplifier. Summing of coefficients happens in third integrator itself.

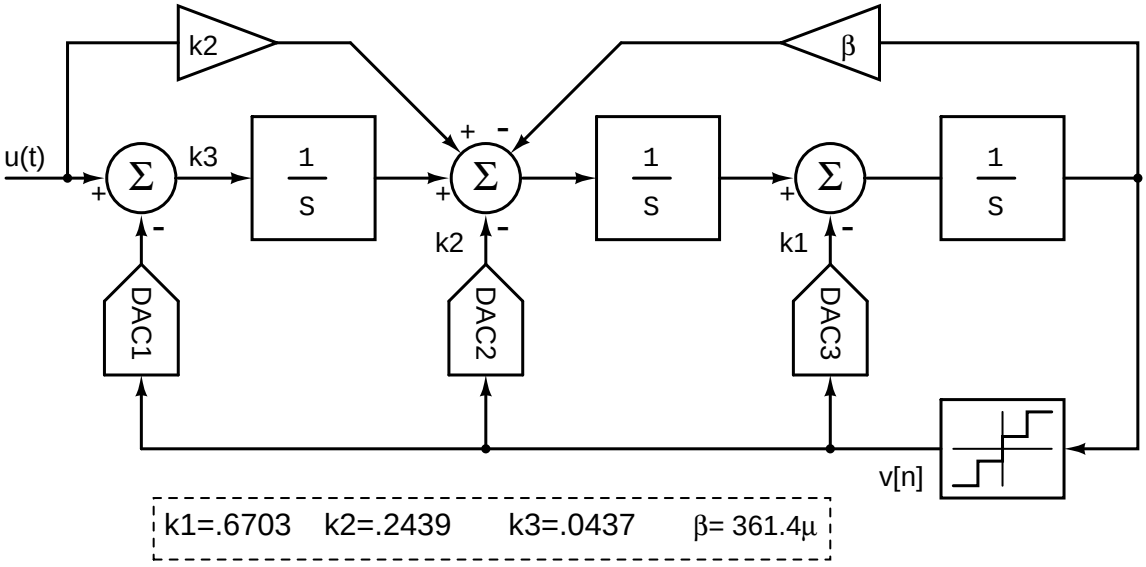


Figure 2.27: Prototype of CIFB Loop-Filter

Choice of Components

In a CIFB loop-filter, coefficients are realized by distributive feedback. Hence, at the output nodes of integrators there will be a signal component along with the high frequency quantization noise. This can lead to a tremendous increase in the integrating capacitors value because we have to do node scaling to ensure limited output swings.

Fig. 2.28 shows the circuit diagram of loop-filter for CIFB implementation.

Signal swings will be maximum at the output of the first integrator. Since integrating resistor R_1 and R_{DAC1} is fixed to 240 kΩ because of noise constraints, we need C_1 as high as 30 pF. If we can somehow cancel the signal component at the output node of first opamp, signal swings will come down greatly, so as the integrating capacitance. Thus, a direct path from input to the second integrator is

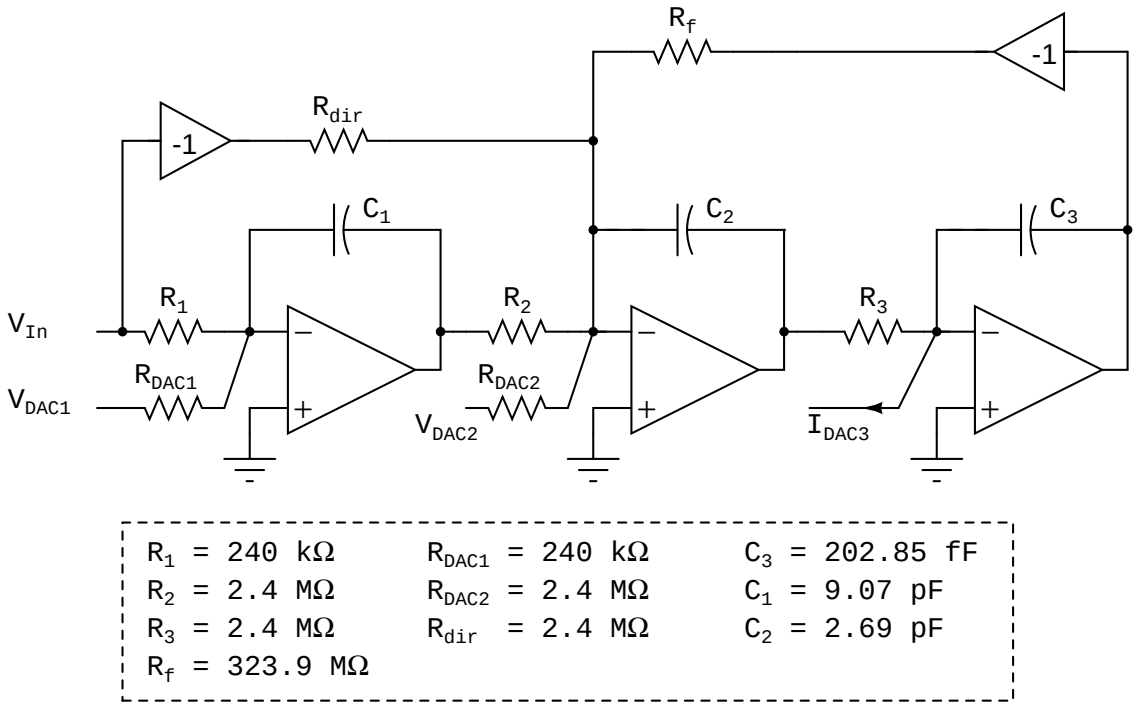


Figure 2.28: Circuit Diagram of CIFB Loop-Filter

given and this makes the C_1 as 9.07 pF. This value of C_1 is comparable to the one used in CIFF loop-filter. Since swings at the first integrating opamp are reducing, swings at other integrating opamp are also reducing.

Resistive feedback was chosen for the first and second integrating opamp. We should keep in mind that choosing a resistive feedback can amplify the input referred noise of the loop-filter. Therefore a current steering feedback DAC was chosen for the final integrator.

Since R_2, R_{DAC2}, R_{dir} and R_3 do not contribute to the input referred noise significantly, they are chosen as 2.4 MΩ. Node scaling is done to ensure maximum swings at output nodes are within 600 $\mathrm{mV_{pp,d}}$. Therefore, capacitors values are

$$C_2 = 2.69\,\mathrm{pF} \tag{2.22}$$

$$C_3 = 202.15\,\mathrm{fF} \tag{2.23}$$

Hence, notch resistor R_f for optimized zero is 323.9 MΩ. It is implement using

t-network having R_{t1} as 1.5 MΩ and R_{t2} as 7.02 kΩ.

Opamp Design

Opamps from the CIFF loop-filter design are reused here. In both the architecture first opamp decides the noise and distortion performance of the loop. Therefore, first opamp is kept same in CIFB loop-filter as well. Second and third opamp are scaled according to the required load current. Tail current of 3 μA in second opamp and a tail current of 2 μA in third opamp is desired.

It so happens that the second and third integrating opamp used in CIFF loop-filter can be used as third and second integrating opamp in CIFB loop-filter respectively. Reader may refer to the previous section 2.2 for the schematics of opamps.

CHAPTER 3

Latch and DAC Design

The quantizer block converts the analog continuous-time signal from the output of the loop-filter into a discrete-time digital signal. Fig. 3.1 shows the block diagram of the quantizer followed by the DAC which feeds the analog signal back into the loop-filter. The quantizer consists of a latch and the output buffer. The feedforward DAC is used to supply the current to the output of the first integrator to avoid slewing of the opamp.

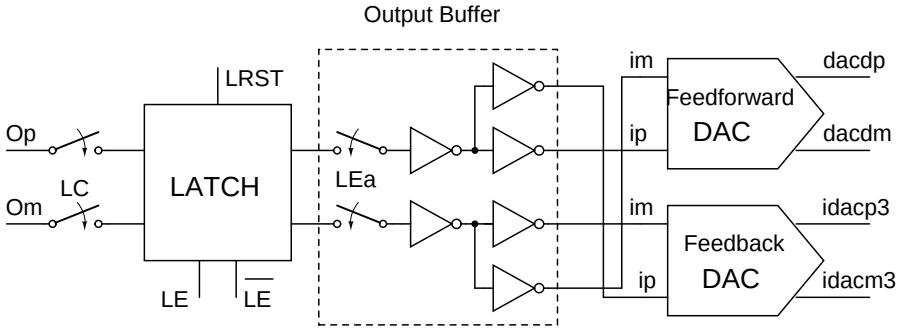


Figure 3.1: Block Diagram of Feedback Path

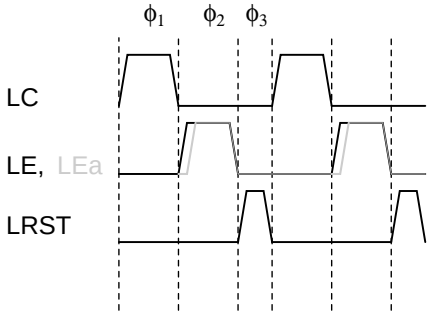


Figure 3.2: Timing Diagram of Clocks

3.1 Latch Design

A standard approach for making a latch is to use positive feedback. Fig. 3.3 shows the circuit diagram of the latch used in the design. It has two back to back

connected inverters in positive feedback which help in regeneration of the sampled signal. Fig. 3.2 shows the timing diagram of the clocks used in the latch.

During phase ϕ_1, clock LC is high and LE is low. In this phase, the latch is in tracking mode, where the outputs of the latch track the input. Since LE is low, in this phase latch is off and burns *zero* static power. In phase ϕ_2, LE goes high and LC goes low. The outputs are disconnected from the input and the latch enters regeneration mode. So, depending on the sign of the input at the time of sampling (falling edge of LC), the two outputs get regenerated to V_{dd} and gnd respectively.

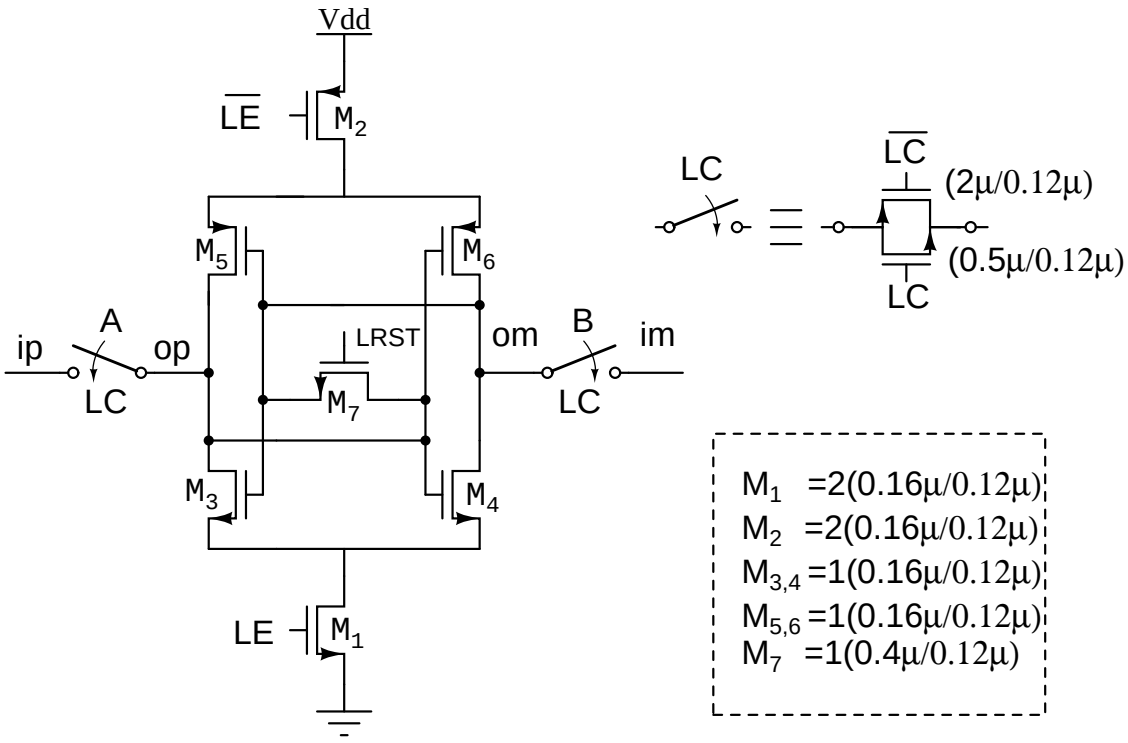


Figure 3.3: Circuit Diagram of Latch

In phase ϕ_3, the latch enters Reset mode, where the two outputs are shorted together. If the Reset phase is not there, then after the regeneration phase ϕ_2, the outputs are at V_{dd} and gnd. This is kind of memory and the latch has a tendency to retain its previous values. This is called as *hysteresis*. Also, the initial part of phase ϕ_1 is wasted in bringing the outputs close to V_{cm} after which the latch starts tracking the input. These problems are solved by using a reset phase which prepares the latch for the next tracking phase ϕ_1.

The time constant of regeneration latch is proportional to $\frac{g_m}{C_L}$ where g_m is the

transconductance of the inverter close to its self bias voltage V_{magic} and C_L is the total capacitance at the output node. The capacitance at the output node of the latch has to be as small as possible to ensure that the tracking and regeneration are fast. Since our frequency of operation is low, we can have minimum sized transistors in latch.

Output Buffer

The output buffer is used to hold the output of the latch stable for the entire duration of a clock period. We see that the output of the latch is tracking the input during ϕ_1 and regenerating during ϕ_2. Buffer tracks the output of latch during LEa (advanced version of LE) and sample output at the falling edge of LEa. Therefore, it holds the regenerated output during the ϕ_1 and ϕ_3.

3.2 Feedback and Feedforward DAC

3.2.1 Feedforward DAC

Fig. 3.4 shows the circuit diagram for the feedforward DAC. Feedforward DAC is used in both the CIFF and CIFB design. It provides the current to first integrating capacitor and hence overcome the slew of the first opamp. Feed-forward DAC is a current-steering. Since V_{dd} is 1.2 V and first stage integrating resistor is 240 kΩ, feed-forward DAC carries a current of $\frac{V_{dd}-V_{cm}}{R}$, 2.5 μA. It feeds current at the output of the first opamp. Therefore, its noise does not contribute to input referred noise, as it is divided by the gain of first integrator.

Fig. 3.4 also shows the biasing circuit for the DAC. It uses a resistor servo loop to bias the current sources to a current of V_{cm}/R.

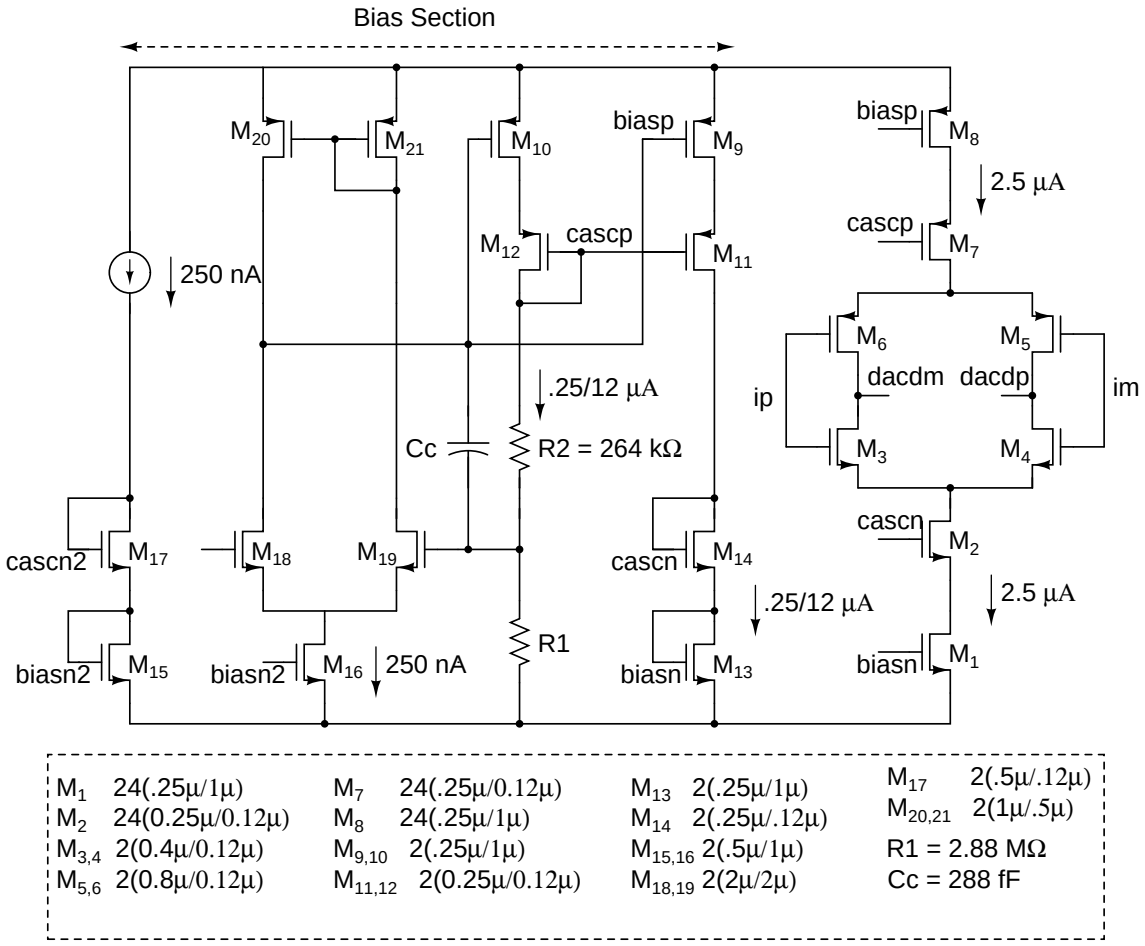


Figure 3.4: Feed-forward DAC

3.2.2 Feedback DAC

For the first integrator in CIFF design and for the first two integrators in CIFB design resistive feedback is chosen. But for the third integrator in CIFB design current steering DAC is chosen because of noise constraints. This feedback DAC is again similar to the feedforward DAC. It carries a current of $\frac{125}{3}$ nA. It is a scaled version of the feedforward DAC.

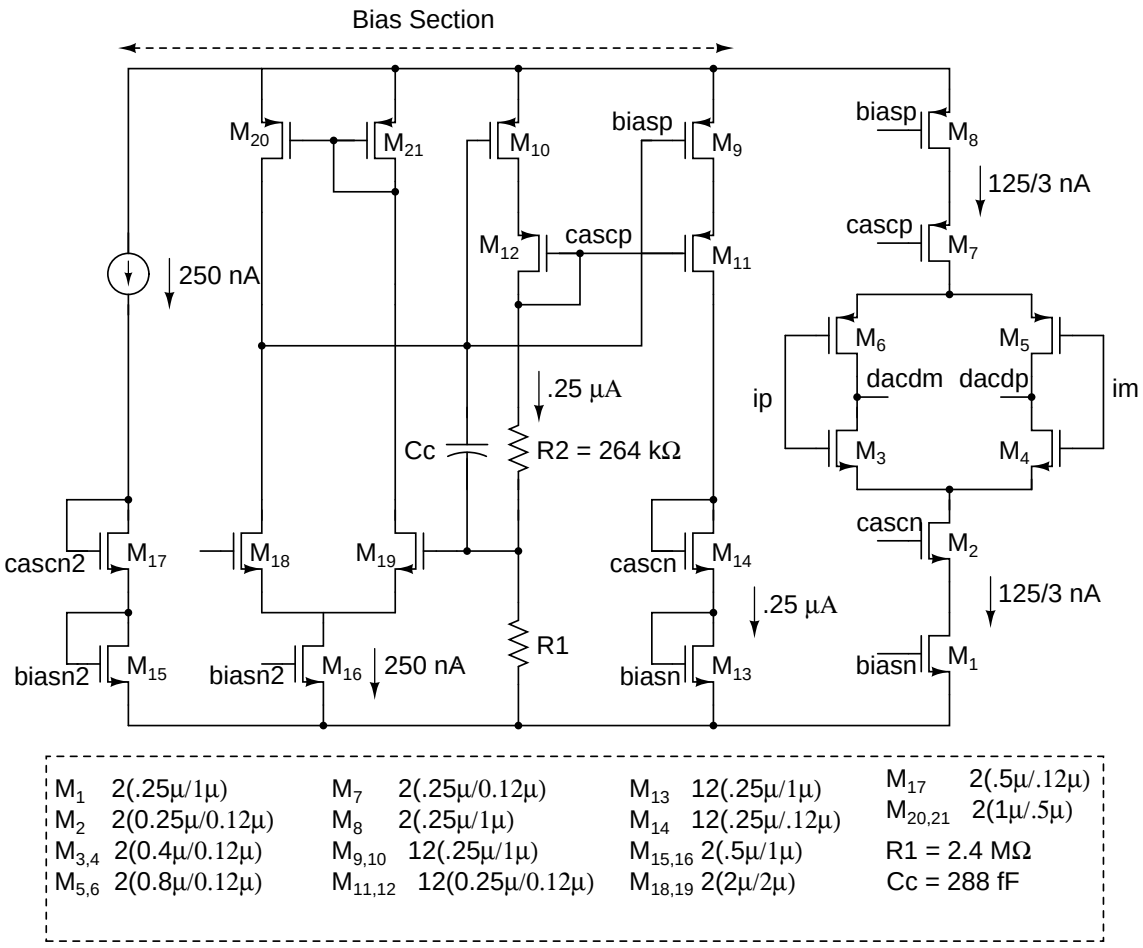


Figure 3.5: Third Integrator Feedback DAC in CIFB Design

CHAPTER 4

Layout, Simulation Results and Conclusion

4.1 CIFF Modulator

The designed CIFF $\Delta\Sigma$ modulator was laid out using CADENCE Virtuoso Tool. Fig. 4.1 shows the layout of the design. The modulator occupies an active area of about 700 μm X 400 μm.

4.1.1 Simulation Results

Simulations of the entire modulator were carried out with the extracted view after layout. An input sine wave of 1.68 $V_{pp,d}$ at a frequency of 2.5 KHz was used for the simulations. Table 4.1 tabulates the SNDR and SFDR obtained across different corners. Fig. 4.2 shows the corresponding Power Spectral Densities.

Table 4.1: Simulation Results for CIFF modulator

Corners			SNR	SNDR	SFDR
MOS	Resistor	Capacitor			
ss	max	max	108.72 dB	107.34 dB	113.55 dB
ss	min	min	103.22 dB	98.65 dB	100.59 dB
tt	typ	typ	111.78 dB	101.17 dB	101.58 dB
ff	max	max	113.74 dB	102.82 dB	103.11 dB
ff	min	min	115.77 dB	108.75 dB	110.35 dB

4.1.2 Conclusion

A third order single-bit continuous time $\Delta\Sigma$ modulator has been designed for 10 KHz bandwidth in 130 nm UMC CMOS technology. The technique of Opamp assistance has been used to reduce the distortion and the power consumption in the modulator. The total dynamic power consumption in the modulator is 36 μW.

4.2 CIFB Modulator

The designed CIFB $\Delta\Sigma$ modulator was laid out using CADENCE Virtuoso Tool. Fig. 4.3 shows the layout of the design. The modulator occupies an active area of about 700 μm X 400 μm.

4.2.1 Simulation Results

Simulations of the entire modulator were carried out with the extracted view after layout. An input sine wave of 1.68 $V_{pp,d}$ at a frequency of 2.5 KHz was used for the simulations. Table 4.2 tabulates the SNDR and SFDR obtained across different corners. Fig. 4.4 shows the corresponding Power Spectral Densities.

Table 4.2: Simulation Results for CIFB modulator

Corners			SNR	SNDR	SFDR
MOS	Resistor	Capacitor			
ss	max	max	107.99 dB	105.08 dB	107.54 dB
ss	min	min	103.58 dB	102.41 dB	110.59 dB
tt	typ	typ	107.37 dB	99.76 dB	100.55 dB
ff	max	max	112.38 dB	100.88 dB	101.19 dB
ff	min	min	116.65 dB	111.05 dB	113.02 dB

4.2.2 Conclusion

A third order single-bit continuous time $\Delta\Sigma$ modulator has been designed for 10 KHz bandwidth in 130 nm UMC CMOS technology. The technique of Opamp assistance has been used to reduce the distortion and the power consumption in the modulator. The total dynamic power consumption in the modulator is 36 μW.

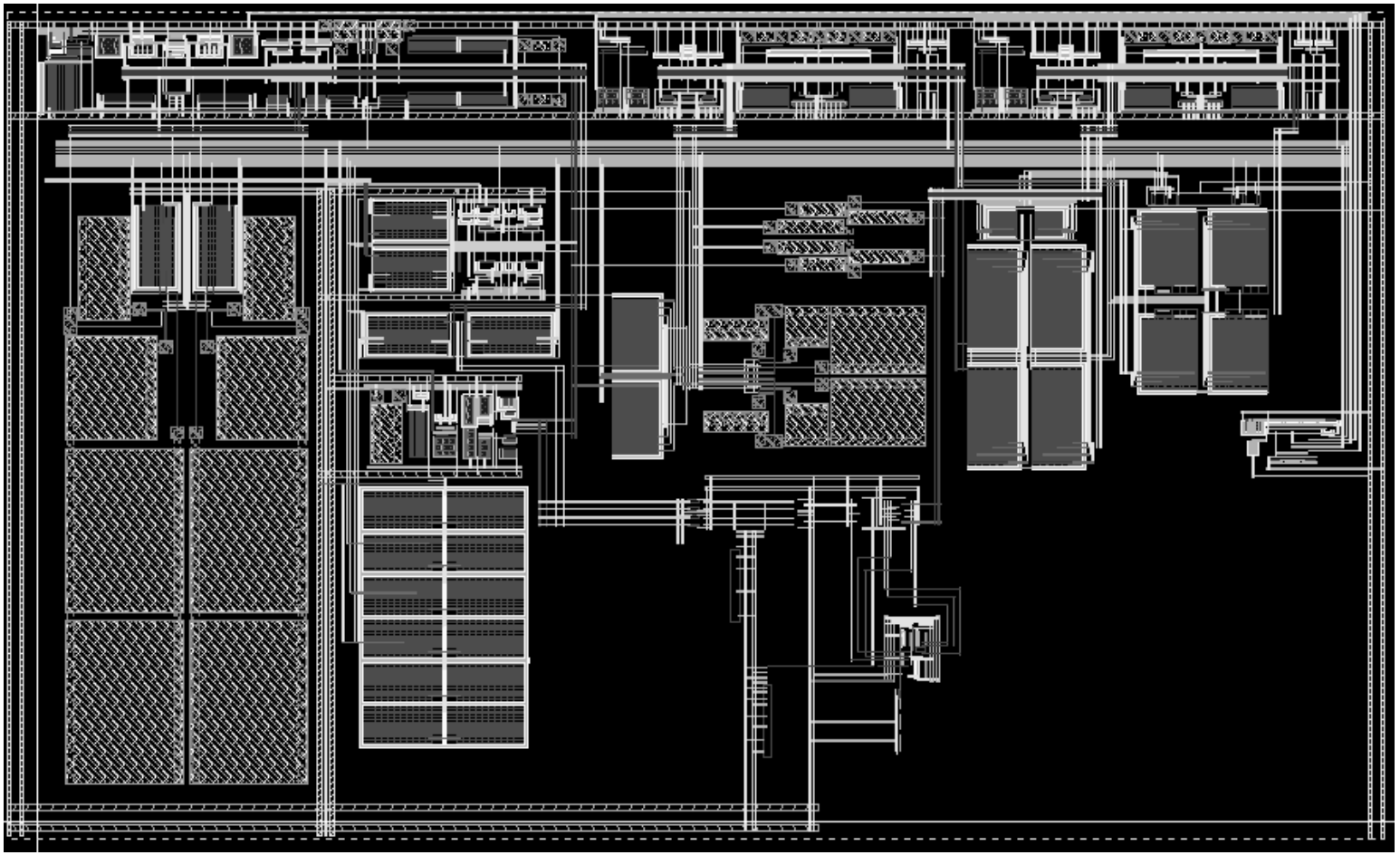


Figure 4.1: Layout of CIFF Modulator

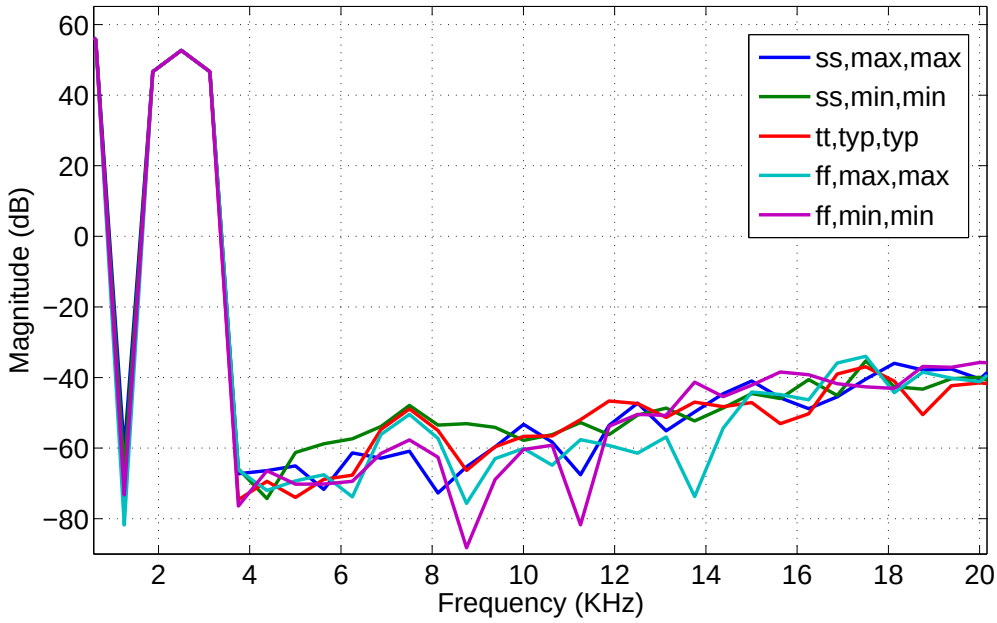


Figure 4.2: PSD of CIFF modulator

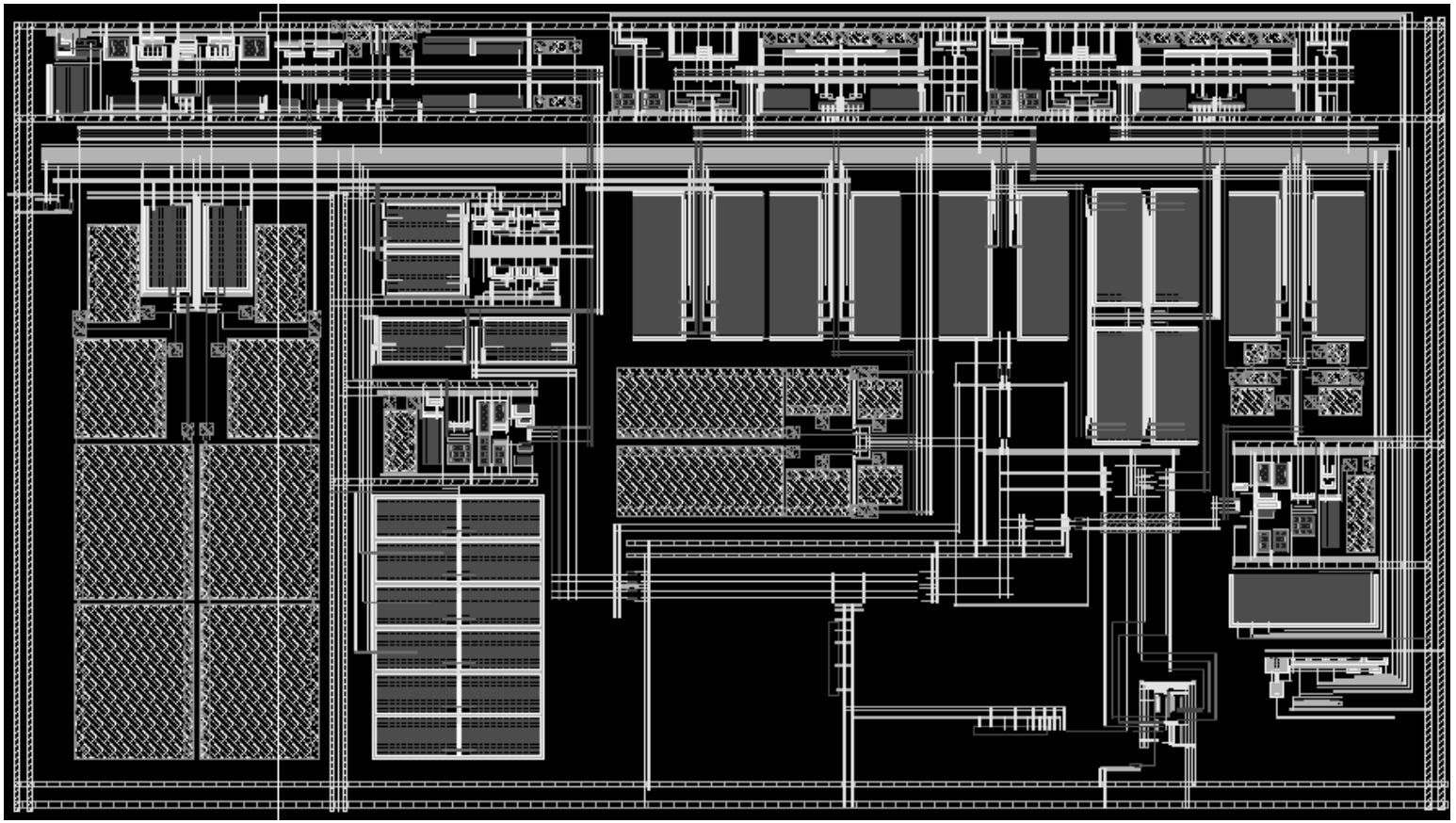


Figure 4.3: Layout of CIFB Modulator

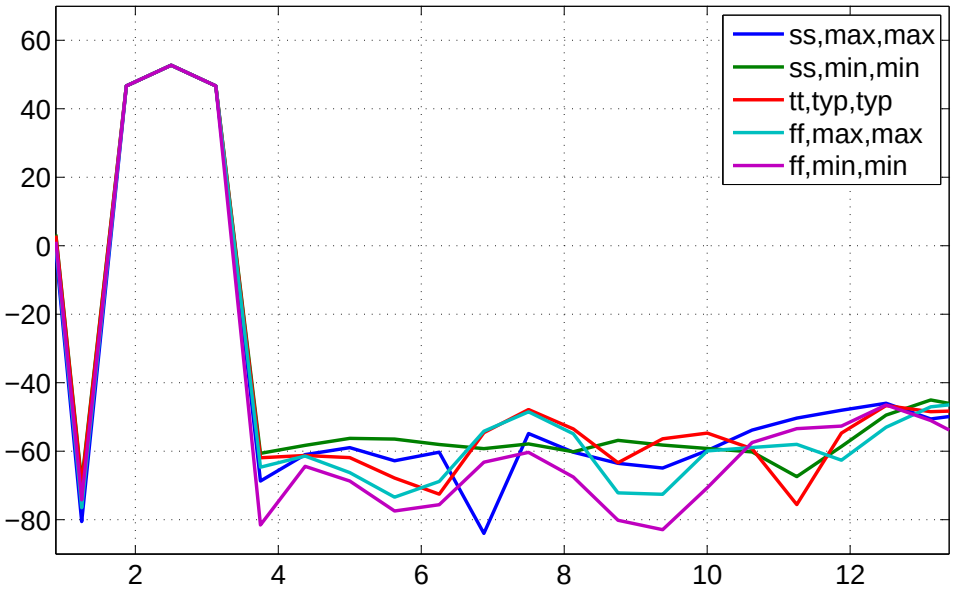


Figure 4.4: PSD of CIFB modulator

CHAPTER 5

Programmable Gain Amplifier

5.1 Introduction

Programmable Gain Amplifier (PGA) is used in the front path of a ADC. It amplifies or compresses the microphone input signal and feed it to the ADC. Gain will be varied depending on the input signal amplitude such that the swings at "Vop" node is always equal to MSA. Since PGA is implemented using an inverting amplifier, gain can be varied by changing resistor values. Fig. 5.1 below shows the block-level schematic of a PGA-ADC front-end.

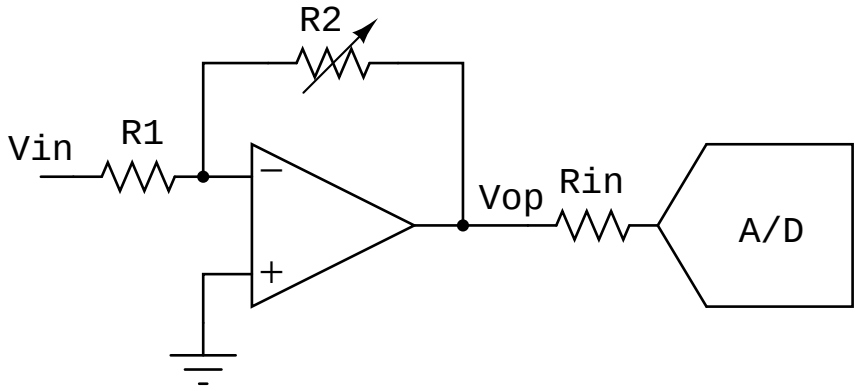


Figure 5.1: Input path

There will be a sensing circuitry which will sense the input signal amplitude and then tweak the bit-settings of R2 to adjust the gain of PGA. PGA should be programmable for the gain range of 0.89 V/V to 100 V/V *i.e.* −1 dB to 40 dB. Therefore, PGA opamp has very tighter specs. It should have the sufficient DC gain & UGF, so that loop gain of PGA is high enough in the band of interest when close loop gain is 40 dB. We would also want the distortion performance to be at least 90 dB at output of PGA.

5.2 PGA Architecture

A two stage cascade of inverting amplifier as shown in Fig. 5.2 was chosen for the PGA architecture. Gain of 20 dB has been alloted to each of the two stages. This architecture is preferable over a single inverting amplifier stage because it relaxes on each opamp's specs. We can achieve the desired distortion performance with a moderate DC gain and UGF.

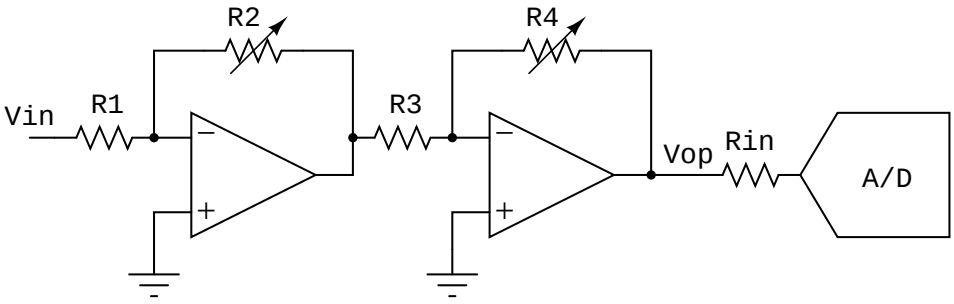


Figure 5.2: Two stage PGA

Gain of -1 dB can be pushed into the ADC block by increasing the input resistance Rin. Therefore we have first stage as $0 - 20$ dB gain; second stage as $0 - 21$ dB gain and ADC block as gain of -1 dB. So, overall we have the gain range of -1 dB to 40 dB. Since Rin has to increase from 240 kΩ to 270 kΩ for -1 dB attenuation, input amplitude at the "Vop" is increased to 945 $\mathrm{mV_{pp}}$ from 840 $\mathrm{mV_{pp}}$. Also to reduce the input current we want to limit the maximum amplitude at "Vin" to half of the MSA *i.e.* 472.5 $\mathrm{mV_{pp}}$ instead of 945 $\mathrm{mV_{pp}}$. Thus, it makes the input amplitude range as [8.4, 472.5] $\mathrm{mV_{pp}}$.

5.3 Circuit Implementation

A two stage PGA with assistance G_m has been implemented. In this section, we will discuss this the architechtural choices for each of the blocks designed for PGA in detail.

5.3.1 Component Selection

We are targeting SNDR of 63 dB in 100 Hz − 10 KHz range. Since the distortion levels due to PGA and CTDSM are way below 63 dB, the SNDR is going to be dominated by thermal and flicker noise component. Input referred contribution to noise is mostly by R_1 and first opamp. So, R1 and first stage g_m has to be chosen carefully. Choosing R_1 low would mean that opamp can have higher noise but input current will also increase, which will in-turn have to be sunk by opamp. Choosing R1 high would mean that we have to burn more power in opamp to reduce the input referred noise.

Aim is to choose R_1 and first stage g_m such that power consumption is optimum. Fig. 5.3 shows the total current consumption w.r.t. different resister values of R_1 for a 63 dB input referred thermal SNR.

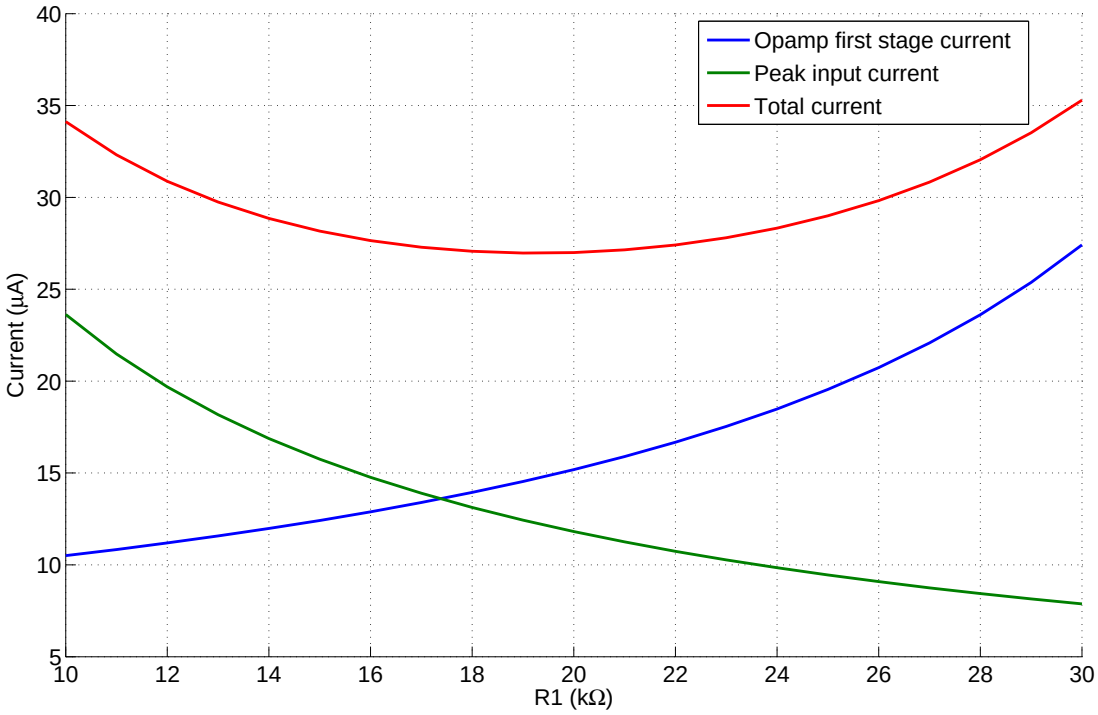


Figure 5.3: Power consumption v/s input resistor R_1

We see that the optimum value of resistor R_1 is 20 kΩ. And at that point input stage current should be 15 μA to have desired input referred SNR. R_2 will have settings from 20 kΩ to 200 kΩ for 0 − 20 dB gain. Noise of R_3 and second opamp

does not come at the input as it is divided by the gain of first opamp. So, R_3 was chosen as 250 kΩ and quiescent current in the first stage of second opamp can be kept at minimum. R_4 will have setting from 250 kΩ to 2.8125 MΩ for $20 - 41$ dB gain.

Noise Simulations

Having chosen the components, input referred thermal noise simulations were carried out in MATLAB. Fig. 5.4 shows the input referred noise and Fig. 5.5 shows the input referred thermal SNR for different PGA gain settings. We see that after gain of 20 dB noise is almost constant becuase after 20 dB gain the noise is predominately due to first opamp and R_1.

Also we see that SNR increases for PGA gain of 0 dB to 6 dB and reduces thereafter. It is becuase that the peak input amplitude is limited to half of the MSA, which is −6 dB of MSA.

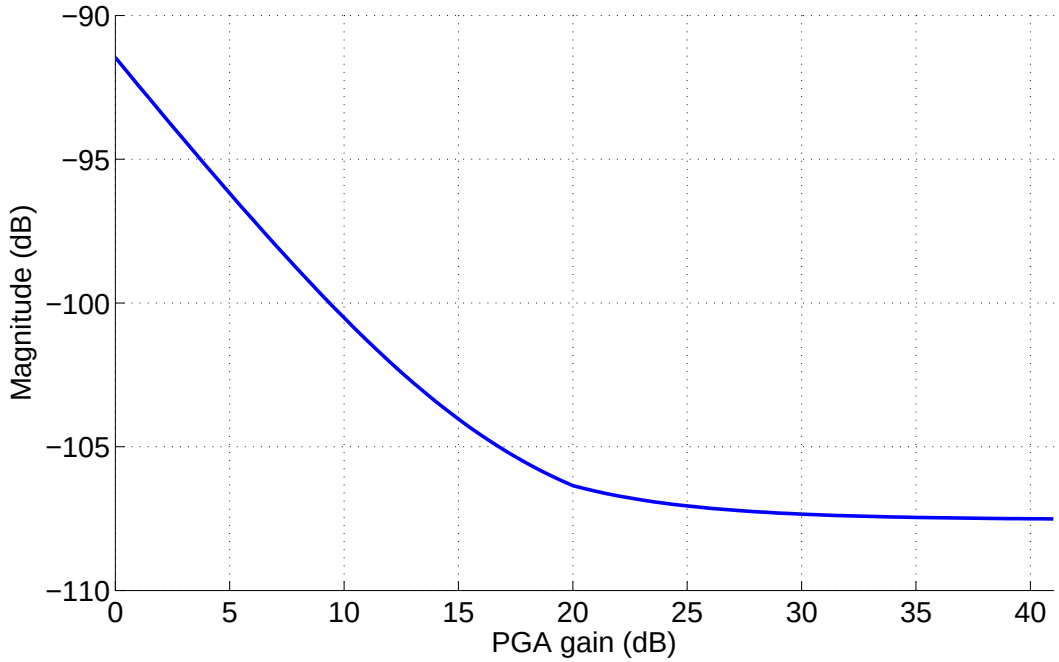


Figure 5.4: Input Referred Noise v/s PGA gain

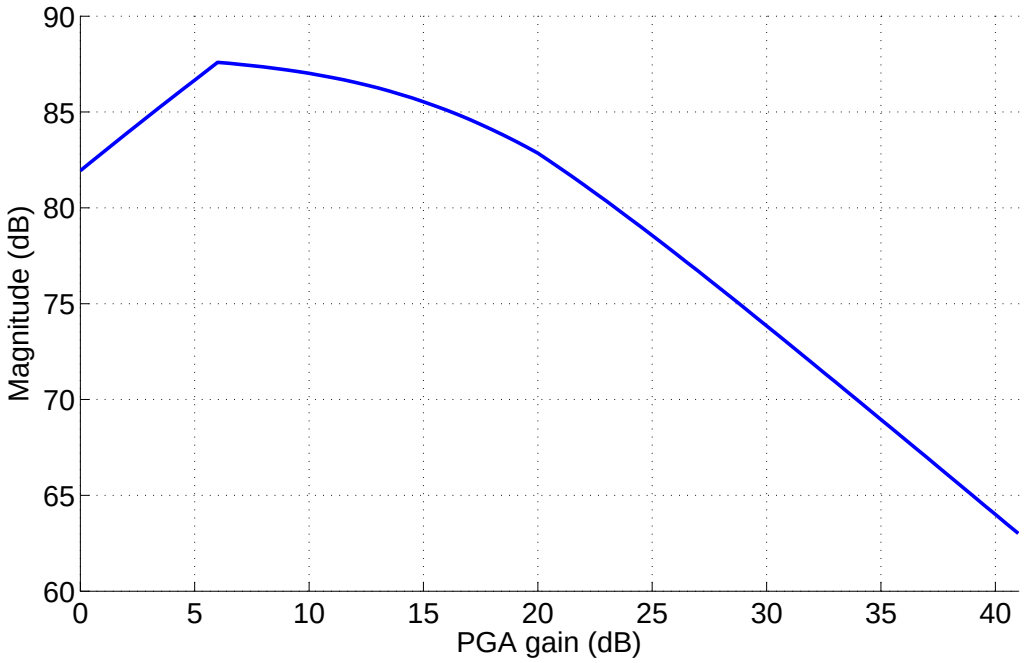


Figure 5.5: Input Referred SNR v/s PGA gain

5.3.2 Technique of opamp assistance

Since the input current can be as high as 25 μA, opamp has to sink all this input current and it can deteriorate the performance of the PGA. Therefore, to reduce the overall power consumption while maintaining the performance of the circuit, we can exploit the technique of assistant opamp. This has been explained earlier in section 2.5.1. Fig. 5.6 shows the PGA block with assistance opamp architecture. g_m is chosen such that i_{in} is equal to i_{gm}. Therefore, $g_m = 1/R1$.

5.3.3 First opamp

This opamp needs to have large signal swings at its output, a sufficient DC gain & UGF. Therefore, it is a two stage miller compensated opamp. Fig. 5.7 shows the circuit diagram for first stage of the opamp. First stage is the main contribution to the total noise. Since the bandwidth of interest is 100 Hz to 10 KHz, flicker noise is of our concern. So, to reduce flicker noise we have PMOS input stage. Furthermore, input PMOS has length of 2 μm and NMOS active load has length of 10 μm. There are cascode for both the NMOS and PMOS side to have a sufficient

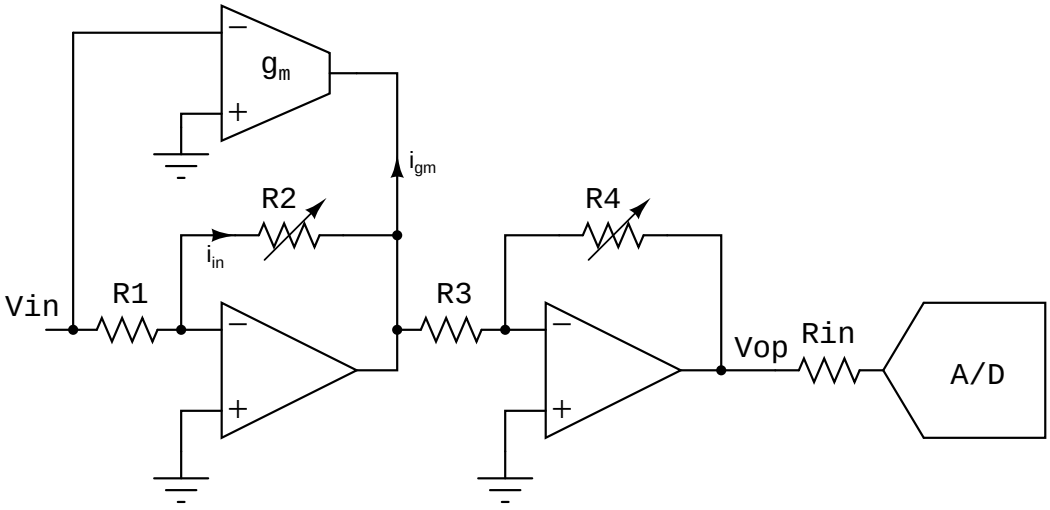


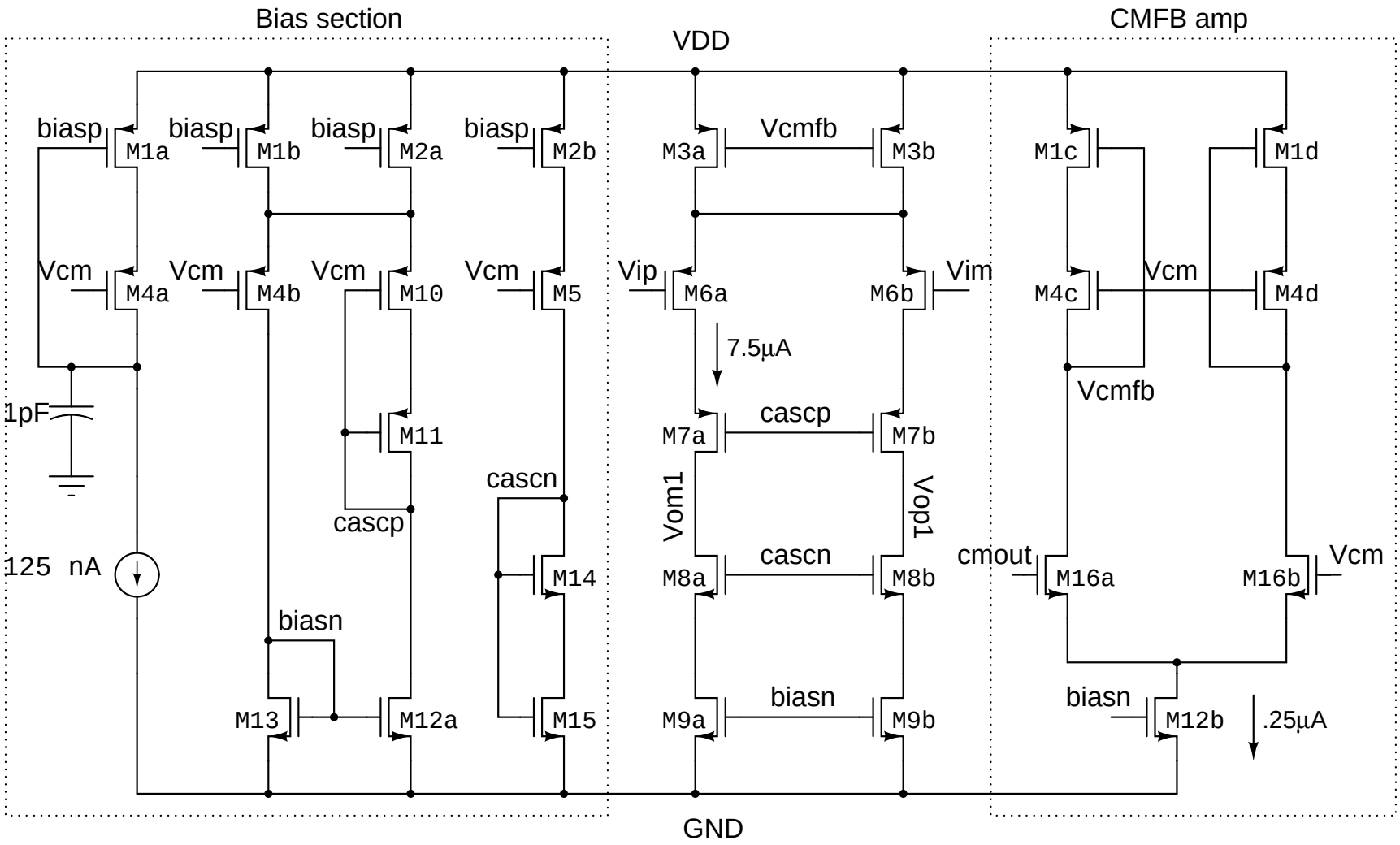
Figure 5.6: Two stage PGA with assistant gm

first stage gain.

The total input referred thermal voltage spectral density of opamp can be roughly written as follows:

$$S_n(f) = \frac{16kT}{3g_{mp}}\left(1 + \frac{g_{mn}}{g_{mp}}\right) + \frac{1}{C_{ox}f}\left(\frac{K_p}{W_pL_p} + \frac{K_n}{W_nL_n}\cdot\frac{g_{mn}^2}{g_{mp}^2}\right) \tag{5.1}$$

where g_{mn} and g_{mp} are transconductances of M9a,b and M6a,b respectively. W_p/L_p and W_n/L_n are there respective sizes and K_p & K_n are flicker noise constants. First term in above expression counts for the thermal noise and second term for the flicker noise. As discussed earlier, quiescent current in the first stage is set to $15\,\mu$A for noise requirements. Thermal noise contribution is 55% and flicker noise contribution is 45%. M1a is high V_T transistor so that M4a can have sufficient headroom over process corners. Since M1b,c,d, M2a,b, M3a,b are scaled versions of M1a, they are also high V_T transistors. Transistors M10 and M15 in bias circuit act as voltage control resistors. They track V_{DS} of M6a,b and M9a,b respectively for the proper replica biasing.



M1a,b = 2(.2µ/.34µ)	M4a,b = 2(2µ/2µ)	M8a,b = 120(1µ/.12µ)	M5 = 4(2µ/2µ)	M13 = 2(.5µ/10µ)
M1c,d = 2(.2µ/.34µ)	M4c,d = 2(2µ/2µ)	M9a,b = 120(.5µ/10µ)	M10 = 2(.16µ/2µ)	M14 = 4(1µ/.12µ)
M2a,b = 4(.2µ/.34µ)	M6a,b = 120(2µ/2µ)	M12a,b = 4(.5µ/10µ)	M11 = 4(1µ/.12µ)	M15 = 2(.16µ/12µ)
M3a,b = 120(.2µ/.34µ)	M7a,b = 120(1µ/.12µ)	M16a,b = 2(.2µ/.12µ)		

Figure 5.7: First stage of opamp 1

CMFB Circuit

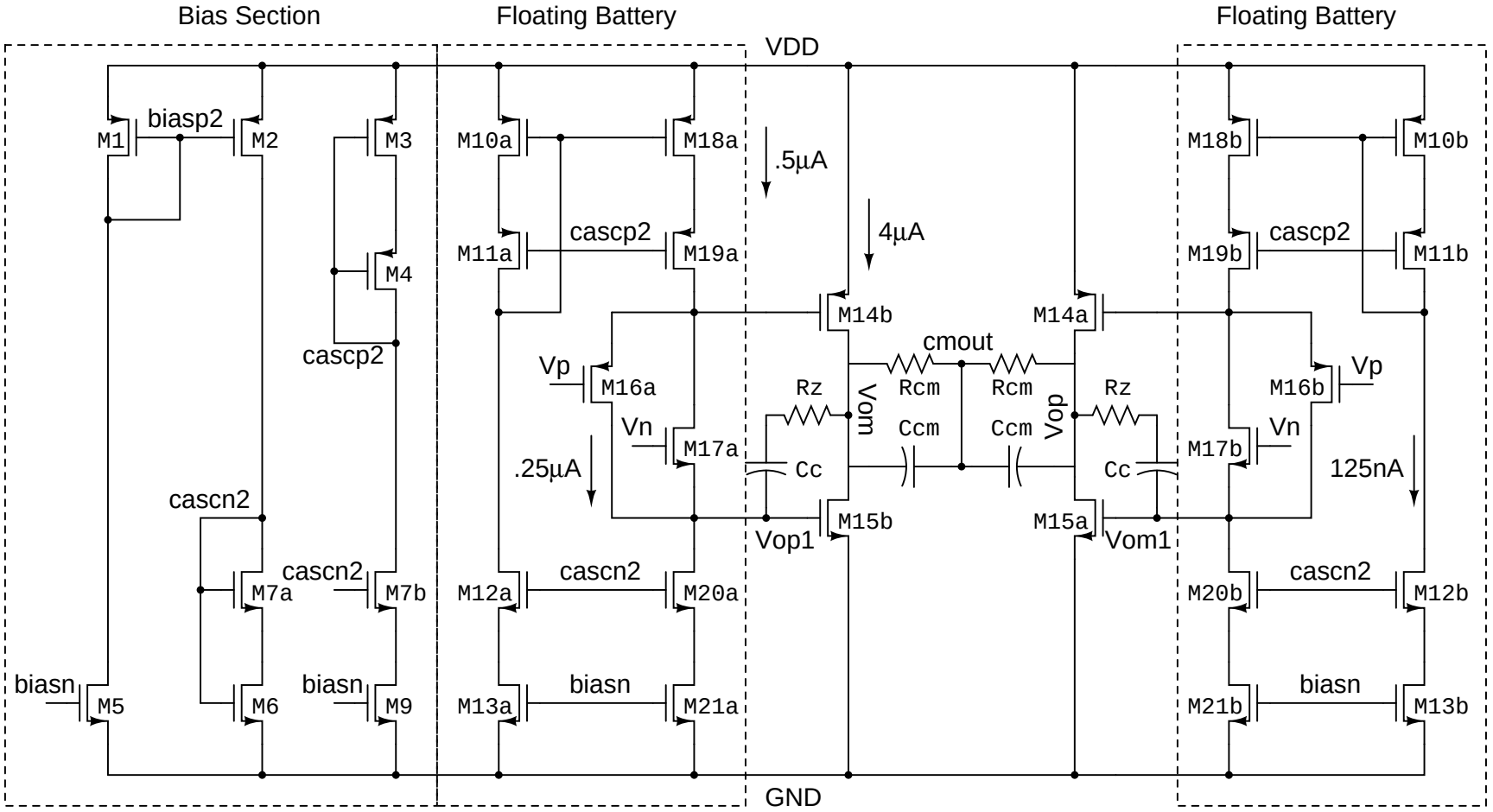
CMFB amplifier is shown in Fig. 5.7. Here we are using only one CMFB circuitry for both the stages. Output common mode is sensed using R_{cm} and then compare with V_{cm}, and accordingly tail current source M3a,b of the first stage is tweaked in the right direction. CMFB amplifier is made very low gain amplifier otherwise CMFB loop will have three high gain stages. An additional capacitance C_{cm} is added in parallel to R_{cm}, which helps in sensing the high frequency common mode steps. Compensation of both the CMFB loop and differential loop is done by the miller capacitance C_c.

Second Stage

It is a class AB stage as it can provide better output g_m than simple class A stage, and also it can source and sink the large current levels. Fig. 5.8 shows the schematic of second stage. It is implemented using floating battery. Transistors M16a,b and M17a,b act as a battery. M15a,b are high V_T transistor such so that the tail current source M20a,b & M21a,b have sufficient headroom. We do not have headroom problem on the PMOS side. Since this stage has to supply only the load current to $R2$, a low quiescent current of $8\,\mu$A is chosen.

Biasing of floating battery is a critical task as it decides the quiescent current in the output stage. Biasing circuitry should be robust across all the process corners. Fig. 5.9 shows the biasing circuitry for the floating battery.

Replica biasing technique is used for biasing floating battery. M5a,b and M1a,b are scaled version of output stage transistors. Amplifiers $A1$ and $A2$ make sure that the drain terminals of M5a and M1b are at V_{cm} to have exact replica of output stage. These transistor sets the value of quiescent current in the output stage. M2 and M8 are copies of floating NMOS and PMOS transistors. Transistor M5b and M1a make sure that V_{DS} of floating NMOS and PMOS transistor are matched exactly. Sizes of M2 and M8 should be chosen such that random mismatches are minimized. This biasing scheme tracks the quiescent current in output stage at all process corners. If there is offset in the V_p and V_n, the quiescent current in



M1 = 2(.5µ/2µ)	M5 = 2(.5µ/10µ)	M10a,b = 2(1µ/2µ)	M18a,b = 8(1µ/2µ)	M14a,b = 64(.25µ/.4µ)	Rz = 12 kΩ
M2 = 4(.5µ/2µ)	M6 = 2(.16µ/12µ)	M11a,b = 2(1µ/.12µ)	M19a,b = 8(1µ/.12µ)	M15a,b = 16(1.5µ/1µ)	Rcm = 620 kΩ
M3 = 2(.16µ/.5µ)	M9 = 4(.5µ/10µ)	M12a,b = 2(1µ/.12µ)	M20a,b = 8(1µ/.12µ)	M16a,b = 4(.5µ/.5µ)	Cc = 3.0 pF
M4 = 4(1µ/.12µ)	M7a,b = 4(1µ/.12µ)	M13a,b = 2(.5µ/10µ)	M21a,b = 8(.5µ/10µ)	M17a,b = 4(.5µ/.5µ)	Ccm = 25 fF

Figure 5.8: Second stage of opamp 1

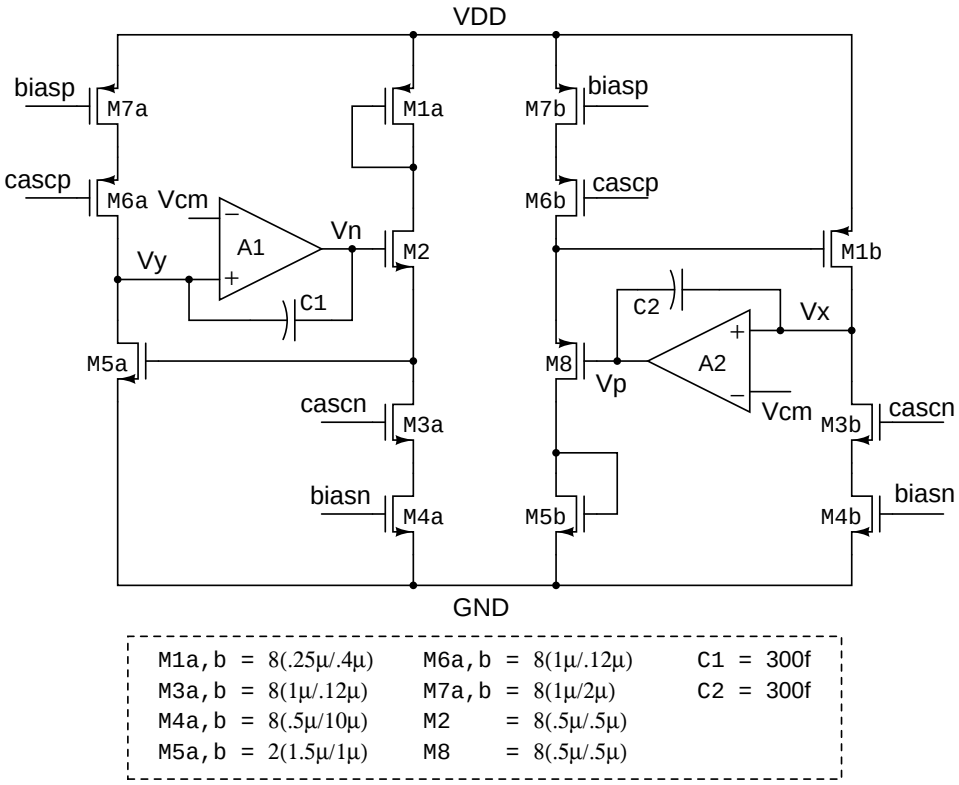


Figure 5.9: Biasing circuit of floating battery

output stage can change. For 10 mV offset in both V_p and V_n, output current can vary by $\pm 15\%$ in worst case.

Amplifier $A1$ and $A2$ are shown in Fig. 5.10. Transistor M1 and M8 are there for proper V_{DS} matching. M2a,b and M7a,b are scaled version of floating PMOS and NMOS transistors respectively.

Fig. 5.11 shows the AC response of first opamp. Table 5.1 summarizes the characteristic of opamp and Fig. 5.12 shows the common mode response of the first opamp.

Table 5.1: First Opamp Characteristics

DC Gain	72.8 dB
UGF	11.07 MHz
Phase Margin	77°
Input Referred Noise	2.6 μV_{rms}
Power consumption	34.2 μW

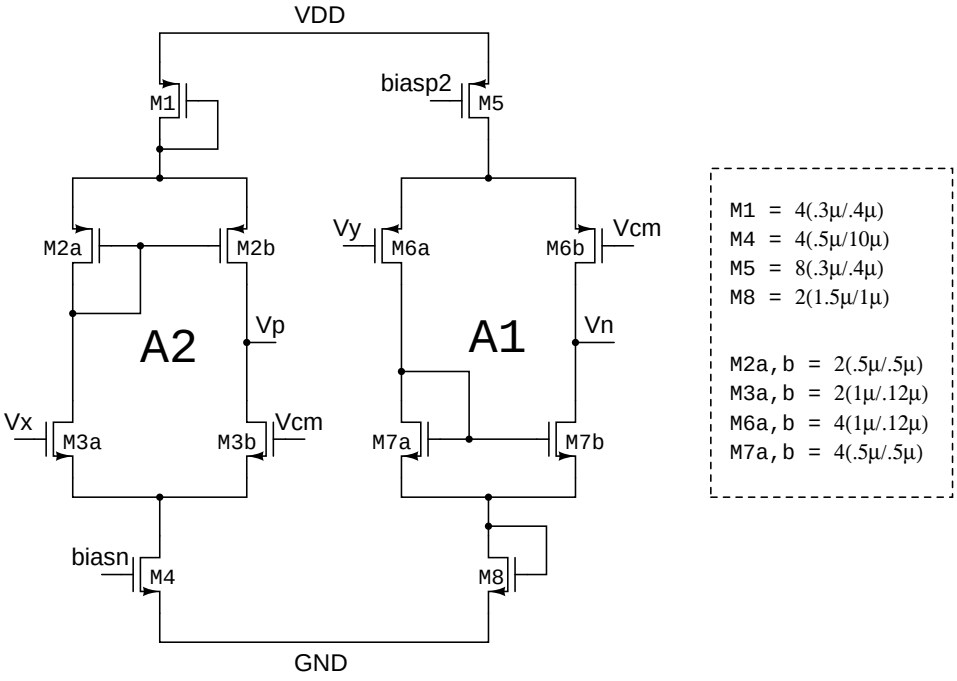


Figure 5.10: Error amplifier A1 and A2

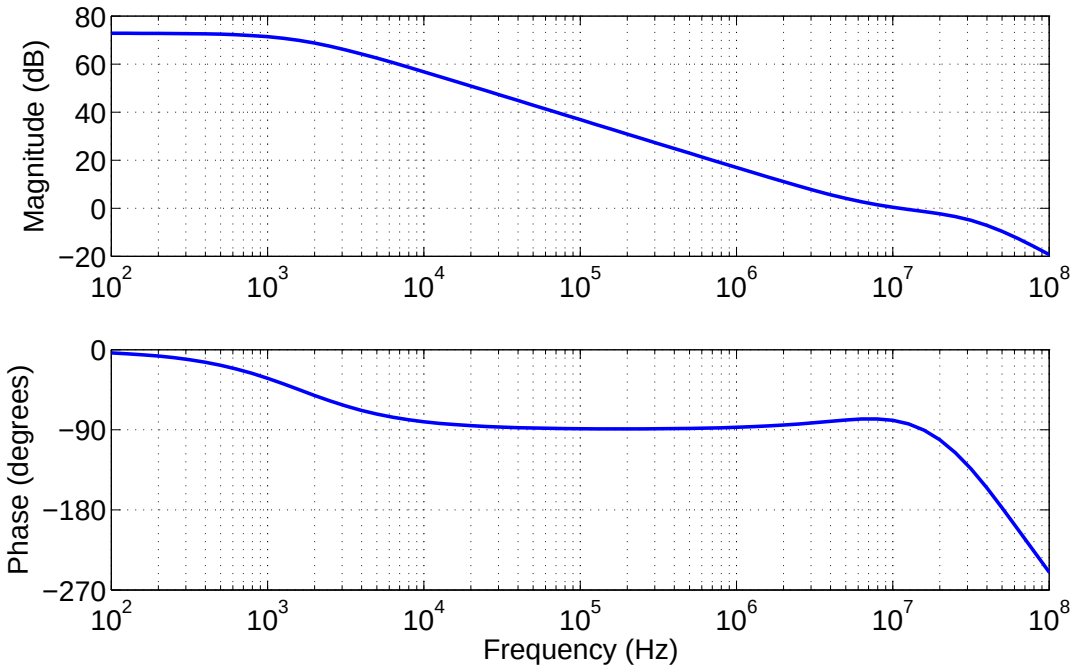


Figure 5.11: AC response of first opamp

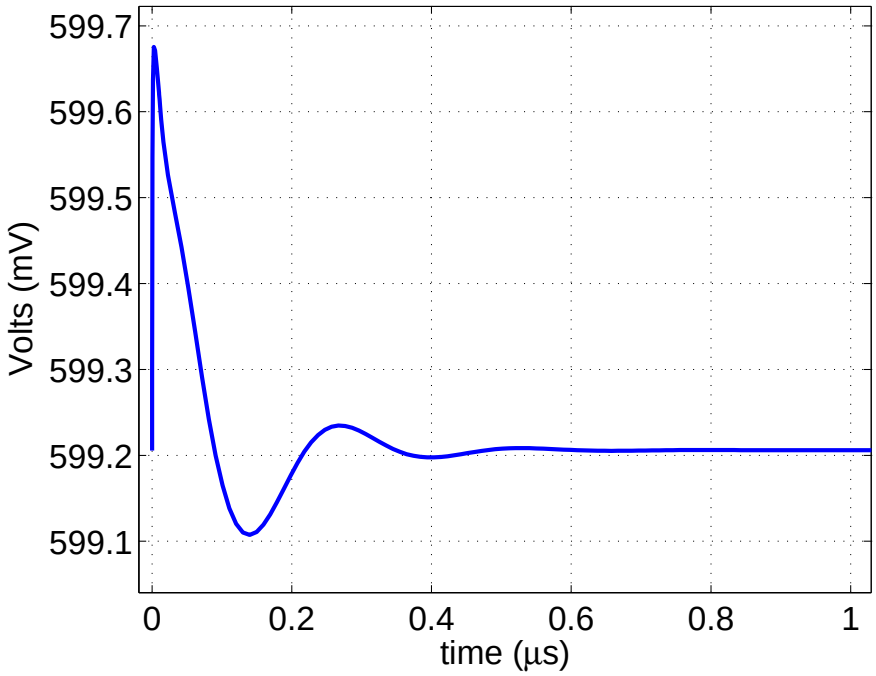


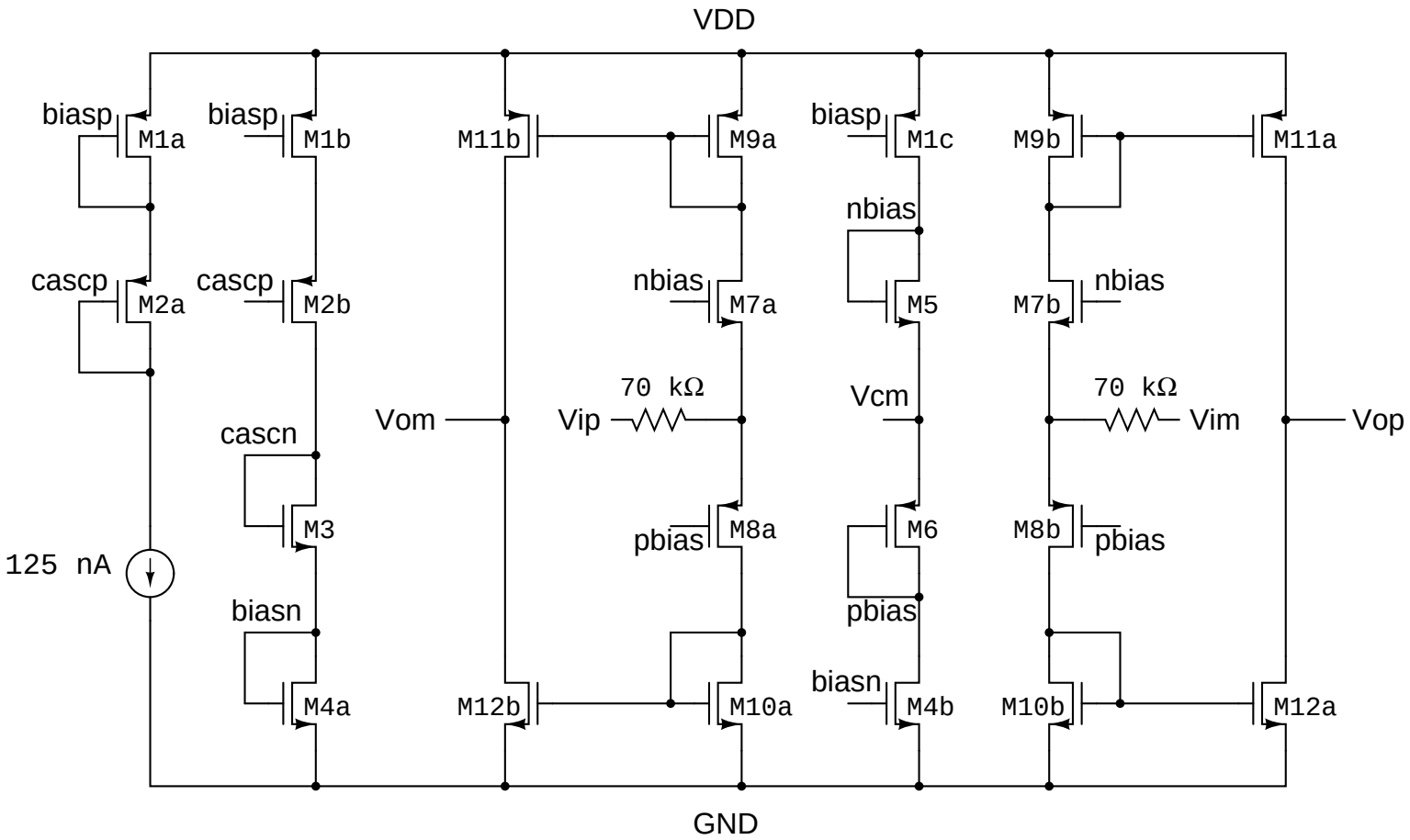
Figure 5.12: Common mode response of first opamp

5.3.4 Assistance G_m

Fig. 5.13 shows the schematic of assistant g_m block. It is designed for a very low quiescent current. We are using the ratio of 1:5 for current mirroring from input to output stage. Therefore it is designed for effective input impedance of $5R_1 = 100\,\mathrm{k\Omega}$. The input impedance of can be written as

$$R_{in} = \frac{1}{g_{mn} + g_{mp}} + R_{series} \tag{5.2}$$

where g_{mn} and g_{mp} are the transconductances of M7a,b and M8a,b respectively. Since $1/(g_{mn} + g_{mp})$ is about $30\,\mathrm{k\Omega}$, R_{series} of $70\,\mathrm{k\Omega}$ is chosen. Since the output swings can be as high as $945\,\mathrm{mV_{pp}}$, transistor sizes in output stage are large so that $\mathrm{V_{DSAT}}$ is minimum even when it is supplying current of $25\,\mu\mathrm{A}$.



M1a,b,c = 10(1µ/.4µ)	M3 = 10(.5µ/.12µ)	M7a,b = 40(1µ/.4µ)	M10a,b = 40(.5µ/.4µ)
M2a,b = 10(1µ/.12µ)	M5 = 10(1µ/.4µ)	M8a,b = 40(4µ/.4µ)	M11a,b = 200(1µ/.4µ)
M4a,b = 10(.5µ/.4µ)	M6 = 10(4µ/.4µ)	M9a,b = 40(1µ/.4µ)	M12a,b = 200(.5µ/.4µ)

Figure 5.13: Assistance Gm

5.3.5 Second Opamp

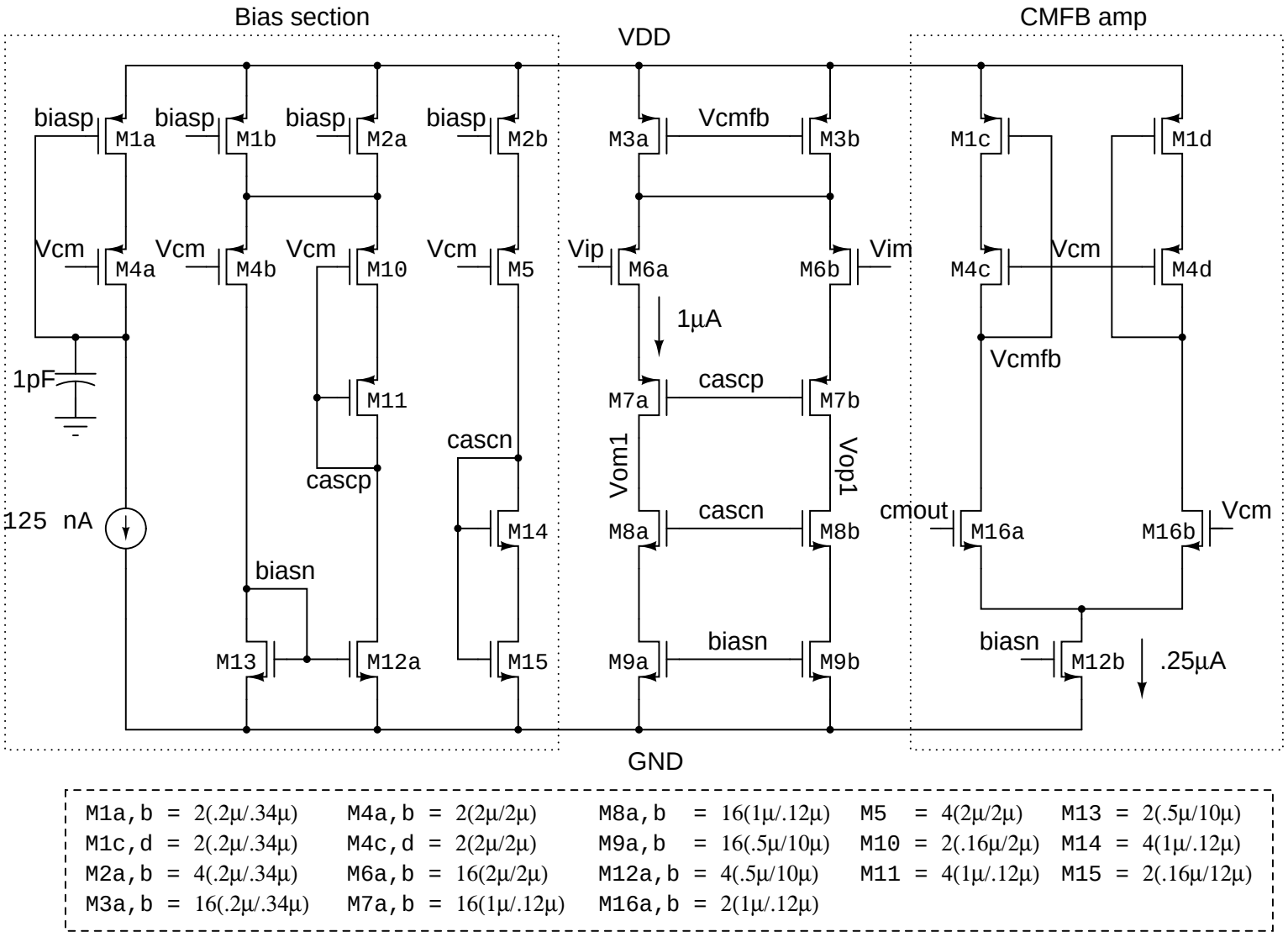
This opamp also needs to have high output swings. Therefore, this is again two stage miller compensated opamp. First stage is telescopic stage to have sufficient DC gain. Since its noise does not come at the input, quiescent current is kept at $2\,\mu$A. Fig. 5.14 shows the first stage of second opamp.

Here the current requirements in the output stage are moderate but linearity of output current should be good as this current is input to the modulator. Therefore for low power consumption this stage is chosen as class AB having quiescent current of $4\,\mu$A.

When implementing the class AB stage using floating battery, we should consider that the floating battery is not loading the first stage branch. Otherwise, first stage DC gain can reduce by a large value. Also the implementing the floating battery is power consuming. Therefore, an another way to implement the class AB output stage is shown in Fig. 5.15

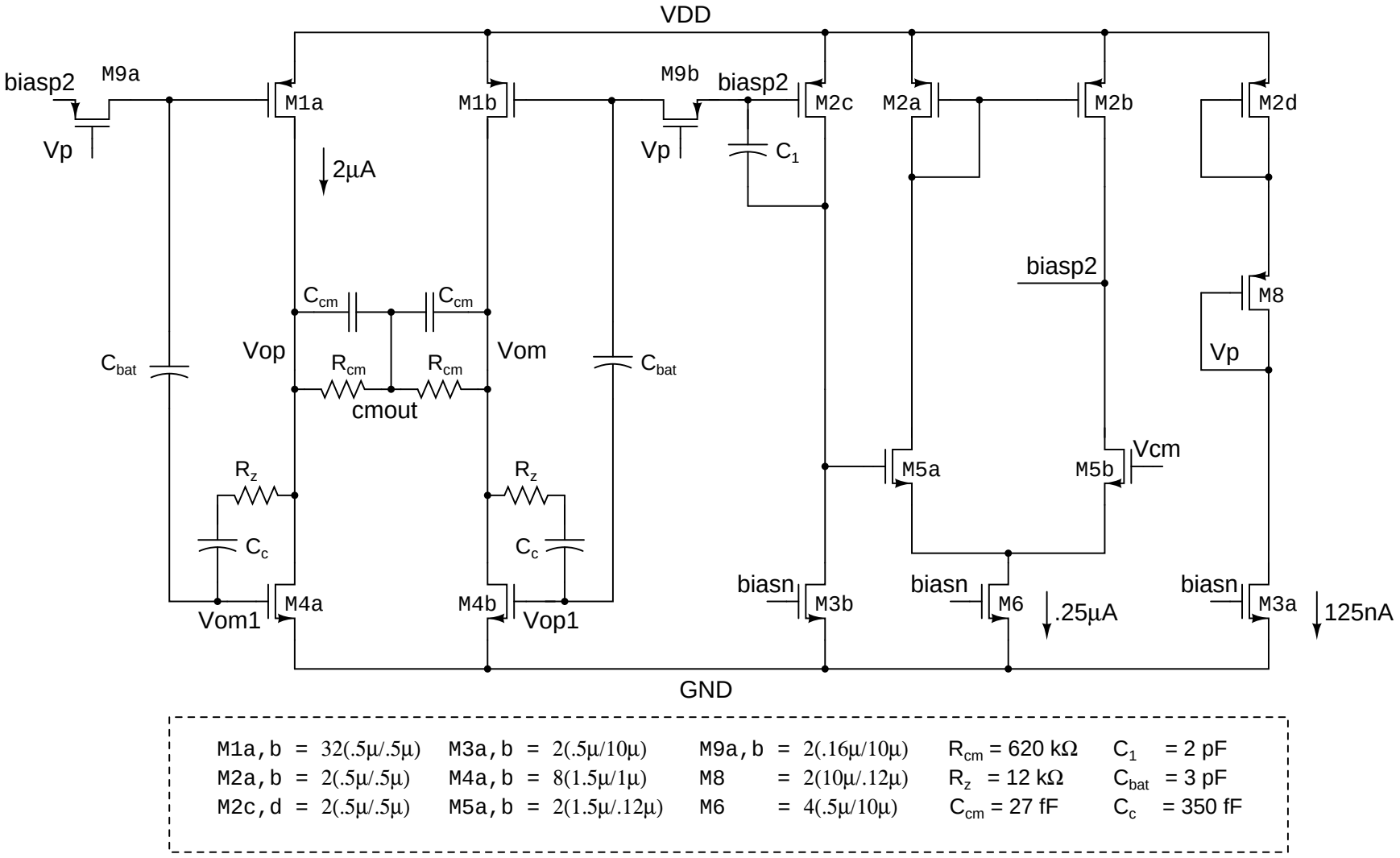
Output of first stage is fed to transistors M4a,b and it is also ac coupled to PMOS side via a capacitor C_{bat}. Transistors M9a,b operate in triode region. M2d and M8 generate the bias for M9a,b. M8 is large width transistor while M9a,b are large length transistors, to achieve high resistance. Thus, a high pass filter is formed, the cut-off frequency $\frac{1}{2\pi RC}$ of this filter is about 1 KHz. So, PMOS side will start contributing to the gain around this cut off frequency. We can observer this effect in the ac response of the opamp. Since DC gain is already high enough, the idea of choosing a cut-off frequency of 1 KHz is to increase the close-loop bandwidth of opamp.

C_{bat} is chosen to be high so that signal gain from NMOS side to PMOS side does not suffer much. Therefore C_{bat} is 3 pF. We would also want the settling of node **biasp2** fast, hence, C_1 of 2 pF is chosen.



M1a,b = 2(.2µ/.34µ)	M4a,b = 2(2µ/2µ)	M8a,b = 16(1µ/.12µ)	M5 = 4(2µ/2µ)	M13 = 2(.5µ/10µ)
M1c,d = 2(.2µ/.34µ)	M4c,d = 2(2µ/2µ)	M9a,b = 16(.5µ/10µ)	M10 = 2(.16µ/2µ)	M14 = 4(1µ/.12µ)
M2a,b = 4(.2µ/.34µ)	M6a,b = 16(2µ/2µ)	M12a,b = 4(.5µ/10µ)	M11 = 4(1µ/.12µ)	M15 = 2(.16µ/12µ)
M3a,b = 16(.2µ/.34µ)	M7a,b = 16(1µ/.12µ)	M16a,b = 2(1µ/.12µ)		

Figure 5.14: First stage of opamp 2



M1a,b	= 32(.5µ/.5µ)	M3a,b	= 2(.5µ/10µ)	M9a,b	= 2(.16µ/10µ)	R_{cm}	= 620 kΩ	C_1	= 2 pF
M2a,b	= 2(.5µ/.5µ)	M4a,b	= 8(1.5µ/1µ)	M8	= 2(10µ/.12µ)	R_z	= 12 kΩ	C_{bat}	= 3 pF
M2c,d	= 2(.5µ/.5µ)	M5a,b	= 2(1.5µ/.12µ)	M6	= 4(.5µ/10µ)	C_{cm}	= 27 fF	C_c	= 350 fF

Figure 5.15: Output stage of second opamp

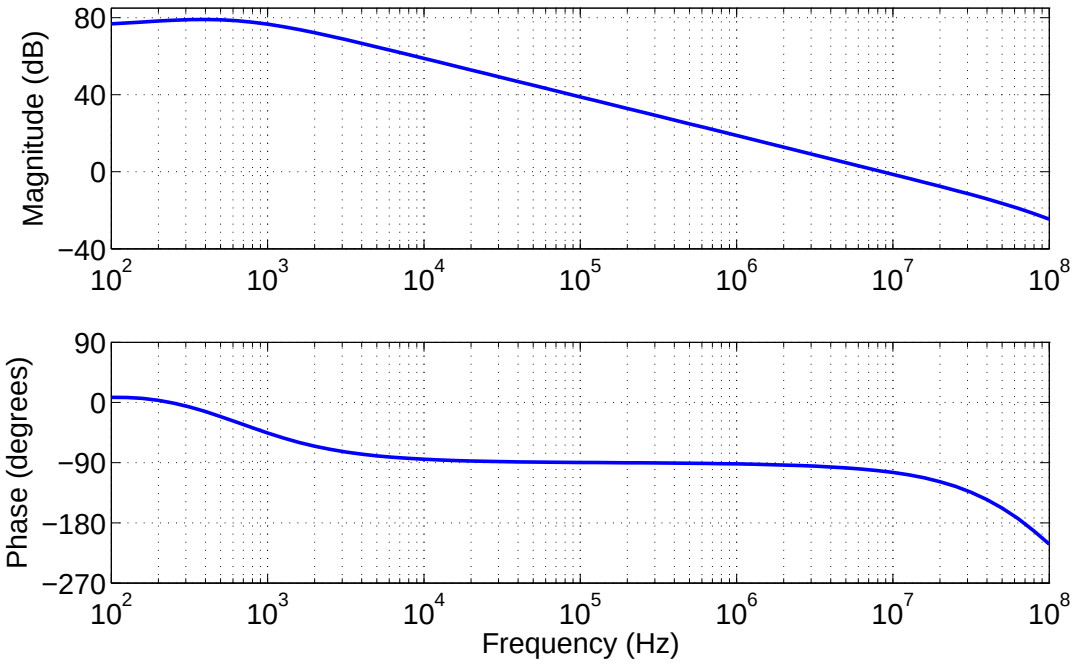


Figure 5.16: AC response of second opamp

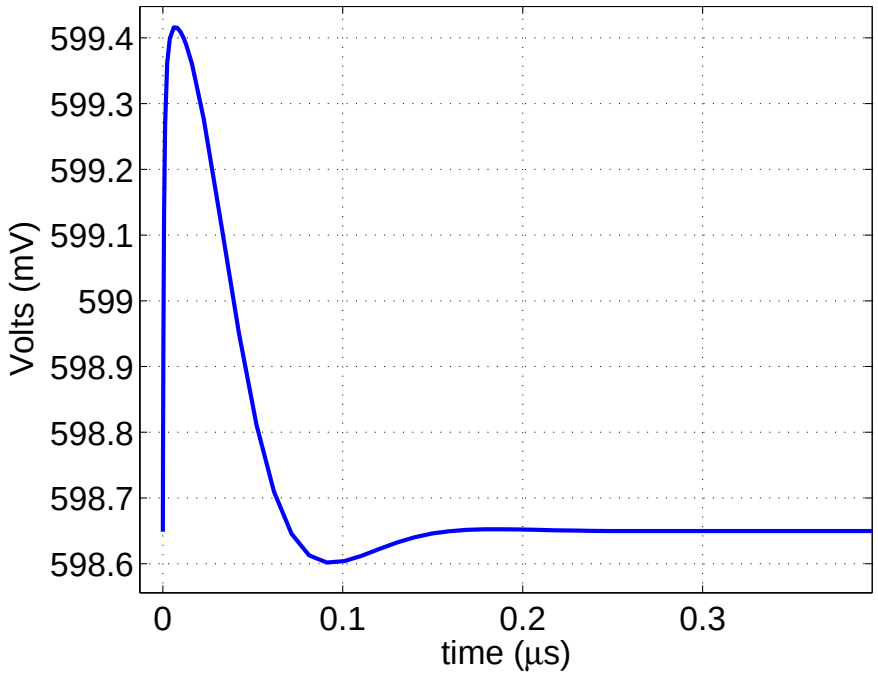


Figure 5.17: Common mode response of second opamp

Table 5.2: Second Opamp Characteristics

DC Gain	77 dB
UGF	8.35 MHz
Phase Margin	76.7°
Input Referred Noise	–
Power consumption	9 μW

5.4 Simulation results

PGA implemented above was tested for different gains settings across the process corners. Only the schematic simulations were carried out. We should wait for the enough time such that node **biasp2** in output stage of second opamp settles and then take the FFT on the output, otherwise low frequency noise will be observed in the output. Worst case scenarios for a PGA can be as follows

- 6 dB $\longrightarrow$ Input current is maximum.
- 20 dB $\longrightarrow$ Loop gain of first stage is minimum.
- 41 dB $\longrightarrow$ Loop gain of both the stages is minimum.

Input tone was given at 1 KHz. Its amplitude is chosen such that swings at PGA output is MSA. A 1024 point FFT with *Hamming* window was taken. Fig. 5.18 shows the output spectrum of load current for a stand alone PGA with load of $R_{in}||R_{dir}$ i.e. $270\,k\Omega||2.7\,M\Omega$.

Table 5.3: Simulation Results for gain settings of PGA

PGA Gain	SNR	SNDR	SFDR
6 dB	105.6 dB	97.9 dB	98.69 dB
20 dB	103.4 dB	96.99 dB	98.12 dB
41 dB	101.45 dB	89.05 dB	89.31 dB

Since the distortion performance is worst at 41 dB gain. PGA was tested with the modulator at 41 dB gain across MOS process corner. Fig. 5.19 shows the output spectrum of a CIFB modulator with PGA at its front. Input tone was given at 2.5 KHz.

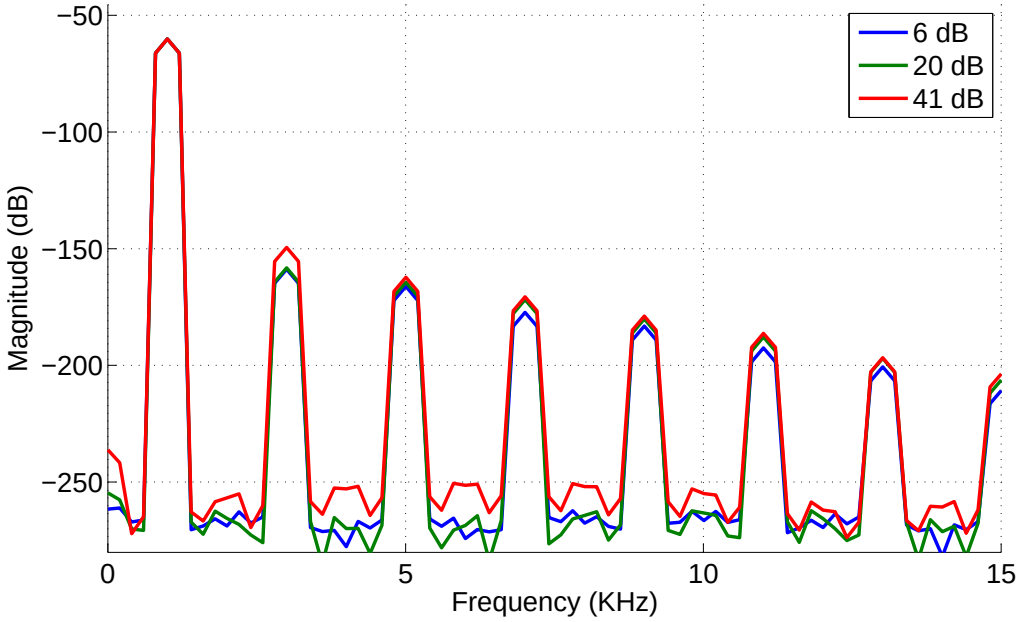


Figure 5.18: PSD for different PGA gain

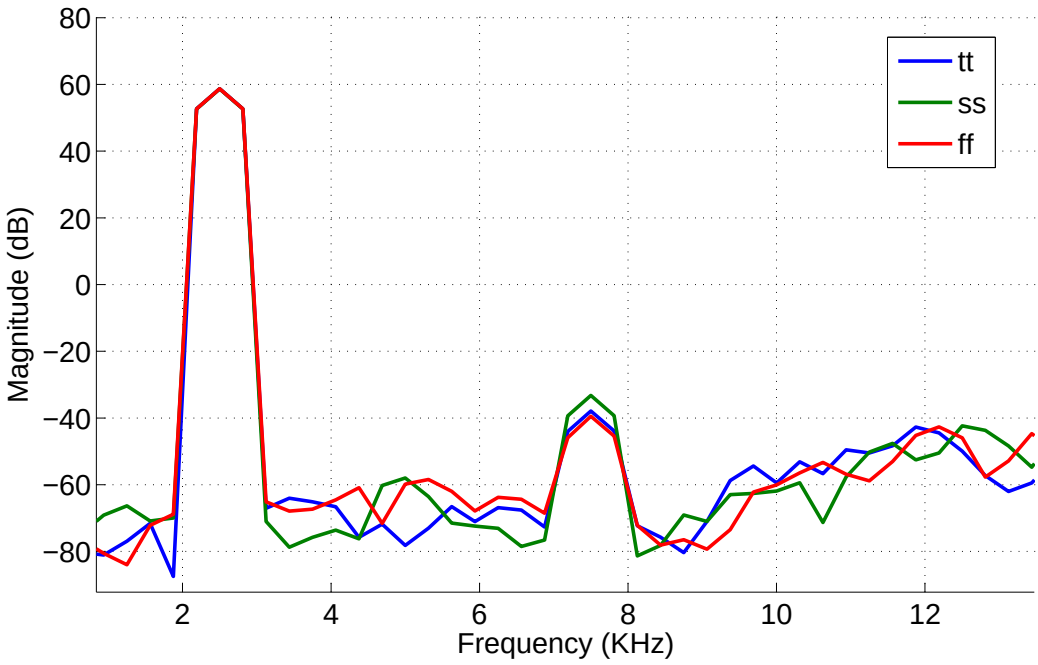


Figure 5.19: Corner simulations at 40dB gain

Table 5.4: Simulation Results for 41 dB gain at different process corners

MOS Corner	SNR	SNDR	SFDR
ss	113.26 dB	91.91 dB	91.94 dB
tt	111.84 dB	96.48 dB	96.61 dB
ff	111.95 dB	98.05 dB	98.17 dB

5.5 Conclusion and Future Work

A PGA with dynamic power consumption of 60 μW was presented above. Since thermal SNR is 63 dB and PGA distortion levels are at -90 dB in worst case, we are safe and we can expect output SNDR to be 63 dB.

To reduce the power even lower, one can try following

- Tweak the ADC input resistor R_{in} for different gain settings. This scheme will use only one inverting stage.
- The resistor R_1 is chosen such that at very low signal amplitudes thermal noise should be minimum. Thus, noise requirements makes the R_1 low and input current is high for input signals near to MSA. We also know from Fig. 5.5 that, at input signal near to MSA we are way above the target SNR to be achieved. So, if we can come with a technique which changes both R_1 and R_2 according the input signal level, we can reduce the dynamic power by a huge factor.

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