Design of Low-pass Anti-aliasing Filter with Variable Bandwidth

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of Low-pass Anti-aliasing Filter with Variable Bandwidth**, submitted by **Abhishek Agrawal**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

The project involves the design of a third order elliptic filter with a tuning circuit to tune it and to be used as part of the wireless LAN chip.

The propose of the low pass filter is to be used as an anti-aliasing filter to remove the adjacent channel components from the signal bandwidth. It has two modes of operation with the bandwidth of 17 MHz and 8.5 MHz, which could be changed depending upon the mode of operation. To avoid variations in the cut-off frequency of the filter across process and temperature variation, the filter is made tunable with a 5 bit control word. The tuning scheme is based on adjusting on chip RC time constant to a precisely known clock period. The power dissipation of the filter is 1.6 mW. The SNDR of 50 dB is achieved for the differential peak to peak signal swing of 1.4 V. To drive the load of the filter a buffer has been designed.

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CHAPTER 1

Introduction

Today is the era of wireless technology, where each electronic gadget we want to be as mobile as possible with low power consumption. The filter design presented here is designed for a wireless application to act as an anti-aliasing filter, where both power and the dynamic range are important. The opamp-RC architecture could provide a higher dynamic range over a Gm-C filter but is mostly restricted by the bandwidth of the opamp for high frequency operation. By using feed forward technique as presented in [1] one can get rid of that restriction. It means for the same bandwidth, the opamp will take lesser amount of power.

As we go into the deep micron process, the components variation is become more important. So there is a necessity for on chip frequency tuning circuit to stabilize it. A very simple way is to tune the capacitance digitally [3]. But when the actual amount of capacitance inside the circuit is so small to make it impossible to get the least capacitor needed in the bank, one way could be to tune both the resistor and capacitor. This concept used here to stabilize the bandwidth of the filter.

The filter has to drive a load so that the filtered signal can be further processed. One way is to increase the sizes of the opamp used in the filter to drive the load, but it consumes a lot of power. An alternative way of designing the buffer is discussed which has the advantage of reduced power dissipation.

1.1 Organization of Thesis

This thesis is organized as follows.

Chapter 2 explains the architecture of the filter.

Chapter 3 explains the design of the opamp, the basic building block, of the filter.

Chapter 4 explains how the automatic tuning circuitry stabilizes the filter ac response and how it is being designed.

Chapter 5 explains the design of the buffer with the off−chip interfacing peripherals of the filter.

Chapter 6 contains the layout of the different parts of the filter.

Chapter 7 gives the simulation results of the filter.

1.2 Specifications

Table 1.1: Specification

Operation Mode	10g/b/a mode	11n mode
Filter droop at band-edge in MHz	less than 3dB at8.75MHz	less than 3dB at8.75MHz
Attenuation more than 18dB	at 16MHz and 21MHz	27MHz and 32MHz
SNDR	more than 45dB	more than 45dB

CHAPTER 2

The Opamp RC Architecture

2.1 The Filter Realization

With specification of the filter characteristic mentioned in the previous chapter, it has been found that by using 3rd order elliptic filter with 2dB pass band ripple and 30 dB attenuation with the bandwidth of 17MHz for 11n mode and 8.5MHz for 11g/b/a mode the filter can be realized. For the 11n mode operation the transfer function is shown below.

$$H(s) = \frac{\left(\frac{s^2}{\omega_z^2} + 1\right)}{\left(\frac{s}{\omega_{p_1}} + 1\right)\left(\frac{s^2}{{\omega_{p_2}}^2} + \frac{s}{Q\omega_{p_2}} + 1\right)} \tag{2.1}$$

Where $\omega_z = 186.24 \times 10^6$, $\omega_{p_1} = 45.653 \times 10^6$, $\omega p_2 = 102.69 \times 10^6$ and $Q = 3.214$.

This transfer function can be realized by a lot of different architectures. The two most common architectures are ladder implementation and cascade of first order section with the second order section. Even though the ladder architecture has low sensitivity for components variations, it is difficult to realize and control the transfer function. On the other hand the cascade of the first and second order section has the advantage that it is easy to realize and debug. This is the reason behind choosing the cascade architecture.

2.1.1 First Order Section

The Fig.2.1 shows the circuit of the first order section. The pole introduced by this lies at$P_1 = \frac{1}{RC}$

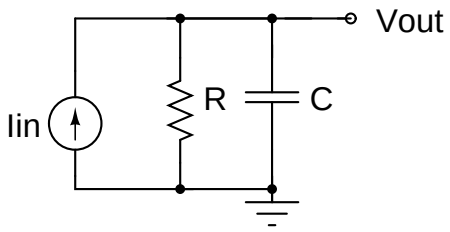

Figure 2.1: The First Order

2.1.2 Second Order Section

The Fig.2.2 shows the band pass second order filter. The transfer function of this filter can be shown as

$$H_2(s) = \frac{\left(\frac{s}{\omega Q}\right)}{\left(\left(\frac{s}{\omega}\right)^2 + \left(\frac{s}{\omega Q}\right) + 1\right)} \tag{2.2}$$

Where $Q = \frac{R}{\sqrt{\frac{L}{C}}}$ is called the quality factor and $\omega = \frac{1}{\sqrt{LC}}$ is called the natural frequency of the filter.

As we can see, for a given transfer function, there is no limit on the number of ways one can choose the values of the resistors and the capacitors, but in practice it is mostly limited by the noise and dynamic range requirements of the filter.

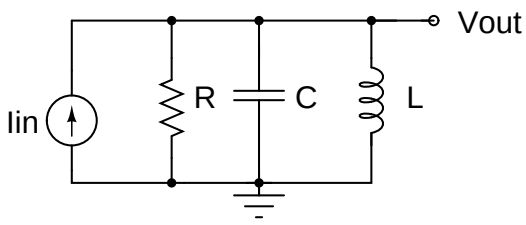

Figure 2.2: The second order section

2.1.3 Node Scaling

Node scaling ensures that the signal swing at all the nodes is maximized. This maximizes the dynamic range at each node. This is done by altering the resistance and capacitance in such a way that it maximizes the signal swing at each node without disturbing the whole transfer function.

2.1.4 Noise

The noise in the circuit consists of thermal and flicker noise. Flicker noise mostly comes from the input transistors of the differential pair and it decreases with increase in the sizes of the transistors. Thermal noise increases with the sizes of the resistors used in the filter. In this design, because of the sizes of the input differential pair, it has been found that the flicker noise, generated by the opamp, is very small compared to the thermal noise generated by the resistors. If the thermal noise generated inside the circuit is very small compare to the SNR requirement of the circuit, one can reduce the power consumption of the whole circuit by increasing the impedances in it. The circuit consumes optimum power when the total noise generated inside the circuit is just equal to the maximum allowed noise.

2.2 The Filter

Using these two concepts, the magnitudes of the different components are chosen and they are shown in Fig.2.4.The input is applied to the first order section of the filter and its output (op1/om1) is applied to the second order section .To introduce a zero in the ac response, the outputs of the second order section (bpp/bpm and lpp/lpm) are added to its input in a proper ratio in the last stage of the filter. The purpose of the last stage is also to drive the output load to the filter. For convenience, through out this thesis we define it as the buffer. The magnitude of the components shown in this figure are for 11n mode(17 MHz bandwidth) of operation. For 11g/b/a mode operation (8.5 MHz bandwidth) each capacitor inside the circuit is doubled by using the switch as explained in the next section. With this structure the thermal noise is found to be 55 dB below relative to 1.4 V differential peak to peak swing.

2.3 Variable Bandwidth

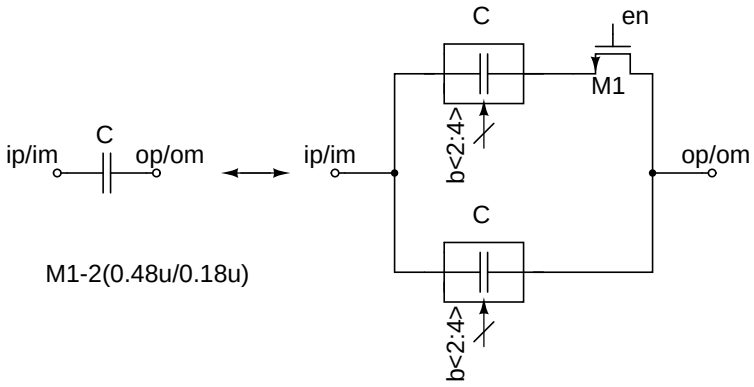

Figure 2.3: The variable capacitor bank

The bandwidth of the filter can be varied without any change in the shape of the

response by scaling each and every capacitor. Hence to reduce the bandwidth to 8.5 MHz from 17 MHz, a variable capacitor bank is used as shown Fig.2.3. it consists of two capacitor banks with a switch. The capacitor bank is used to stabilize the ac response with respect to the process and temperature variations. When the enable signal is switched on the bandwidth of the filter is halved.

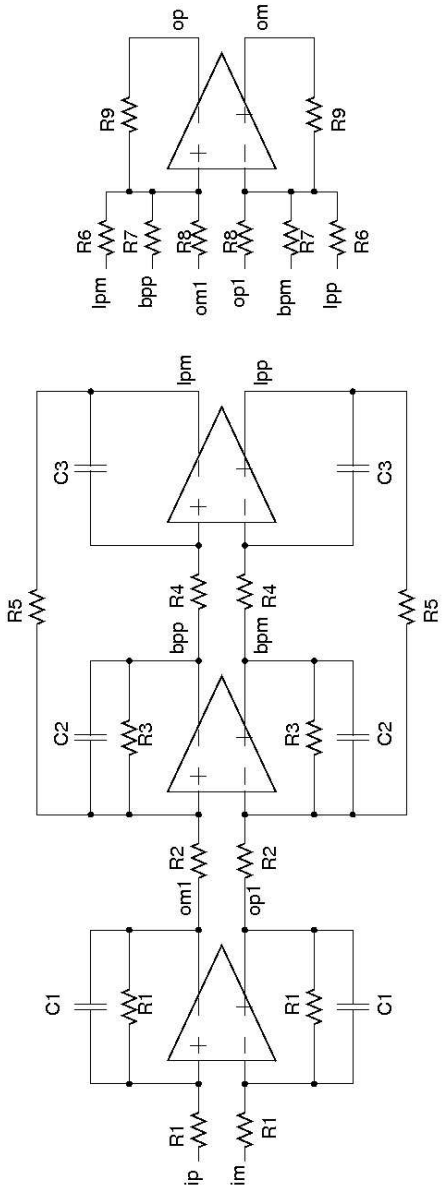

Figure 2.4: The schematic of the filter is shown here. The magnitudes of the components are the following. R1=92 kΩ,R2=74 kΩ, R3=179 kΩ, R4=64 kΩ, R5=54 kΩ, R6=55.7 kΩ, R7=470 kΩ, R8=195 kΩ, C1=236 fF, C2=161.97 fF, C3=159.5 fF.

CHAPTER 3

Opamp Design

3.1 Introduction

The opamp is usually realized by differential pair as the input and with some resistive load. To increase the gain a multi stage opamp is used. More than two stages are difficult to design because of the stability issues.

In the case of a two stage opamp, frequency compensation is necessary to stabilize the opamp. There are two ways in which one can stabilize it. First one is Miller compensation and the other one is the feed forward technique. In the Miller compensation technique we try to make the opamp to look like a first order system by moving the second pole very far away from the first one; whereas in the feed forward technique by adding additional path from input to the output we introduce a zero in the transfer function of the opamp and by doing this it behave like second order system for low frequency signal components and first order system around unity gain frequency components. So in this way we get high gain at the low frequency without compromising bandwidth, whereas in the Miller compensation technique by splitting the two poles of the system it reduces the bandwidth of the opamp by a significant amount. In this work the feed forward technique is being used as the compensation technique because by the feed forward path, it pulls back

the phase to -90 degree and hence it does not reduce the bandwidth by large amount. Originally this method was proposed by J.N. Harrison [1] in his PhD thesis.

3.2 Opamp

As the technology scales down, The NMOS-NMOS opamp is more viable compared to the NMOS-PMOS or PMOS-NMOS opamp. As the threshold voltage of the transistor reaches to $\frac{Vdd}{2}$, the maximum signal swing one can get is $4V_T$ which would be sub-optimal in the higher power supply. With 1.8 volt as the power supply and 0.5 volt threshold voltage the signal swing will be mostly limited by threshold voltage. Also the 1.4 V peak to peak differential signal swing can be easily achievable using NMOS-NMOS opamp. So the NMOS-NMOS opamp topology is used in this design.

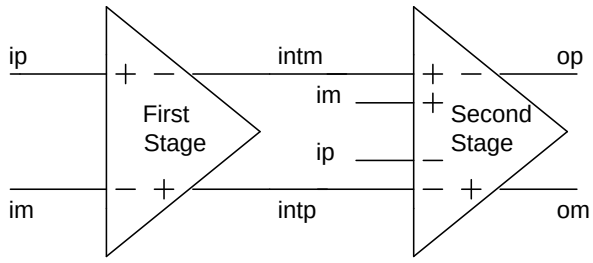

Figure 3.1: The opamp Architecture

The opamp designed here can be thought of as the cascade of two stages as shown in Fig.3.1.The first stage consists of simply a differential pair with a signal differential input and its job is to give a large gain. The second stage consists of two differential inputs. The first input,the output of the first stage,and the second input,the input to the opamp, are summed to add a zero to the transfer function of the opamp.

3.2.1 First Stage

The schematic of the first stage of the opamp is shown in Fig.3.2. It has been realized using a differential pair. The transistors M1 and M2 are the input to the differential pair with M3 and M4 are resistive load. The common mode feedback circuit is shown in Fig.3.3. To sense the common mode voltage of the outputs, the output voltages, intp and intm, are buffered by the source followers and the buffered outputs are averaged. The use of the buffer ensures that the common mode sensor does not load the output terminals but it adds a offset voltage of the V_{gs} of the source follower. Due to this, to compare this common mode voltage with the reference voltage, the reference voltage has to be passed through the replica of the same source follower to cancel out the offset voltage. The common mode voltage is compared with the reference voltage and it is fedback to the resistive load of the differential pair to stabilize the common mode voltage of the output to be around 0.9 volts. The capacitor Cm is used here to stabilize the common mode voltage which could otherwise go into oscillation.

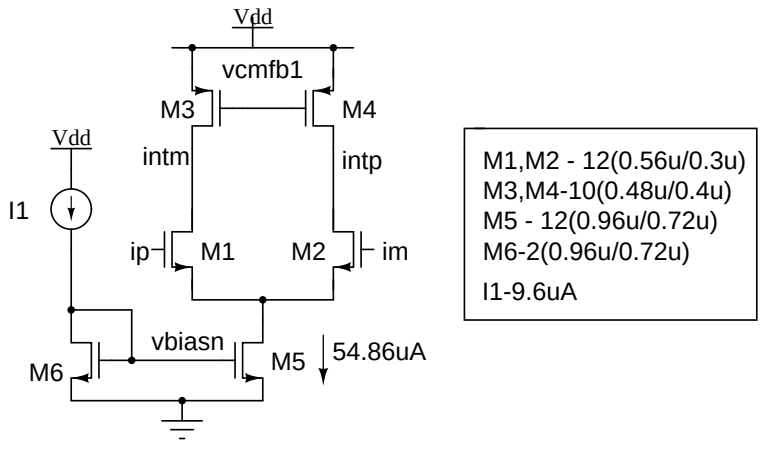

Figure 3.2: The first stage of the opamp

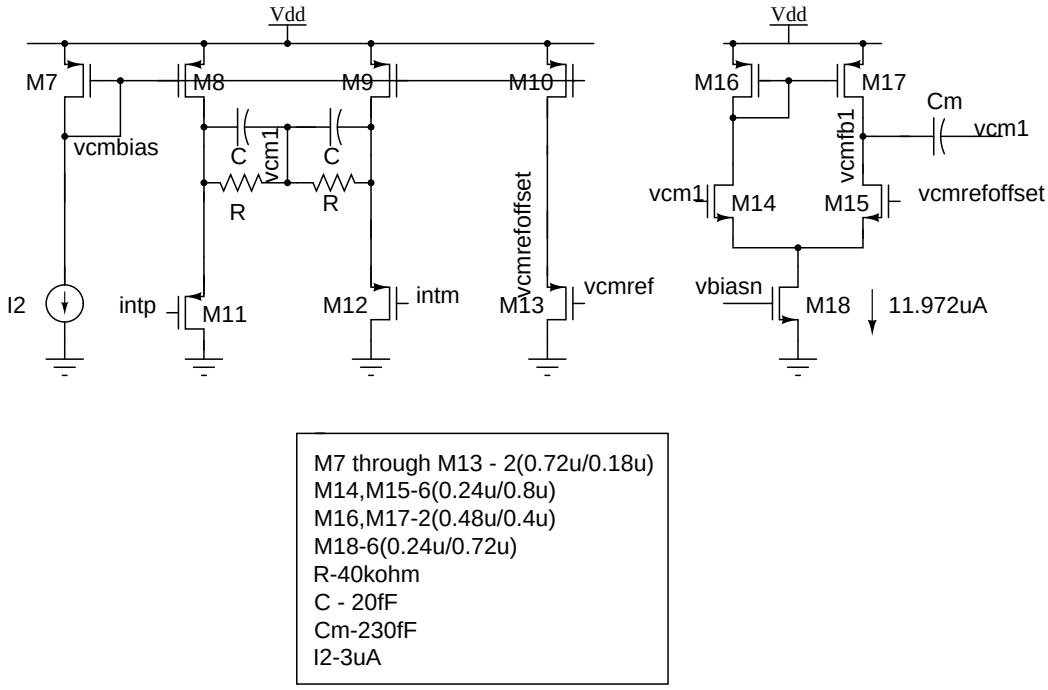

Figure 3.3: The cmfb1

3.2.2 Second Stage

The schematic of the second stage is shown in Fig.3.4 . This stage also works in the same way as the first stage but this stage is having two differential input. The output of the first stage is applied to the NMOS differential pair and the input of the opamp is applied to the PMOS differential pair. The incremental current generated by these two input differential pairs are summed and pumped to the output resistor to generate output voltage. In this way it also introduces the zero to stabilize the opamp from the oscillation. The common mode feedback circuit is shown in Fig.3.5 Here the output common mode voltage is directly sensed by the resistor divider without any need of the buffer because the output impedance of the second stage is much lower compare to the output impedance of the first stage.

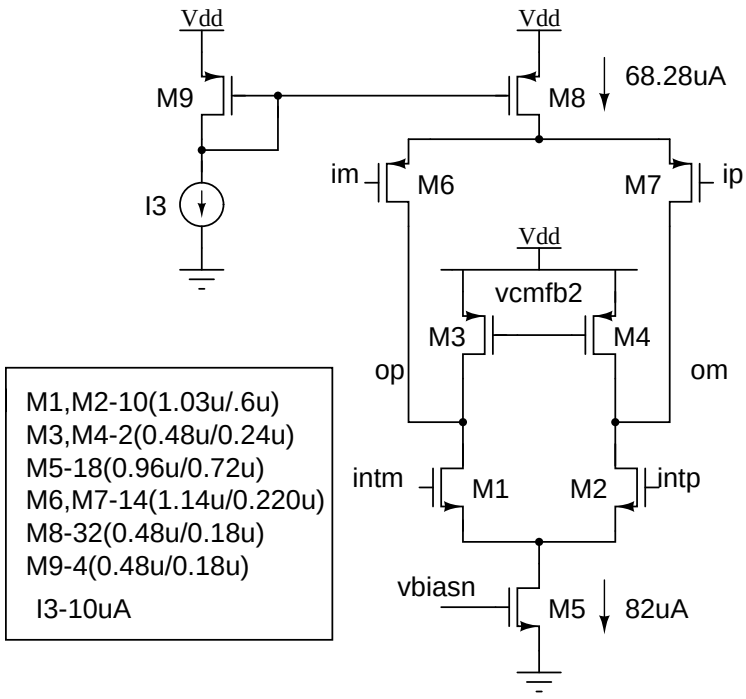

Figure 3.4: The second stage of the opamp

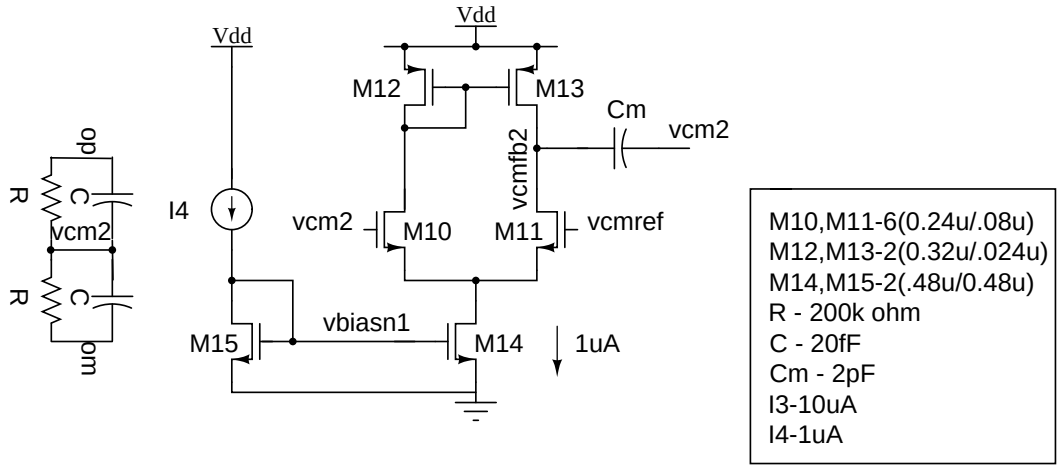

Figure 3.5: The cmfb2

3.3 AC Response of the Opamp

The Fig.3.6 shows the AC response of the opamp when there is not any load at the output. The performance parameter of this opamp is shown below.

1. The DC gain is 58.21dB.
2. The Unity gain frequency is 1.794 GHz.
3. The Phase margin is 52.6 degree.
4. The power consumption is 300 mW.

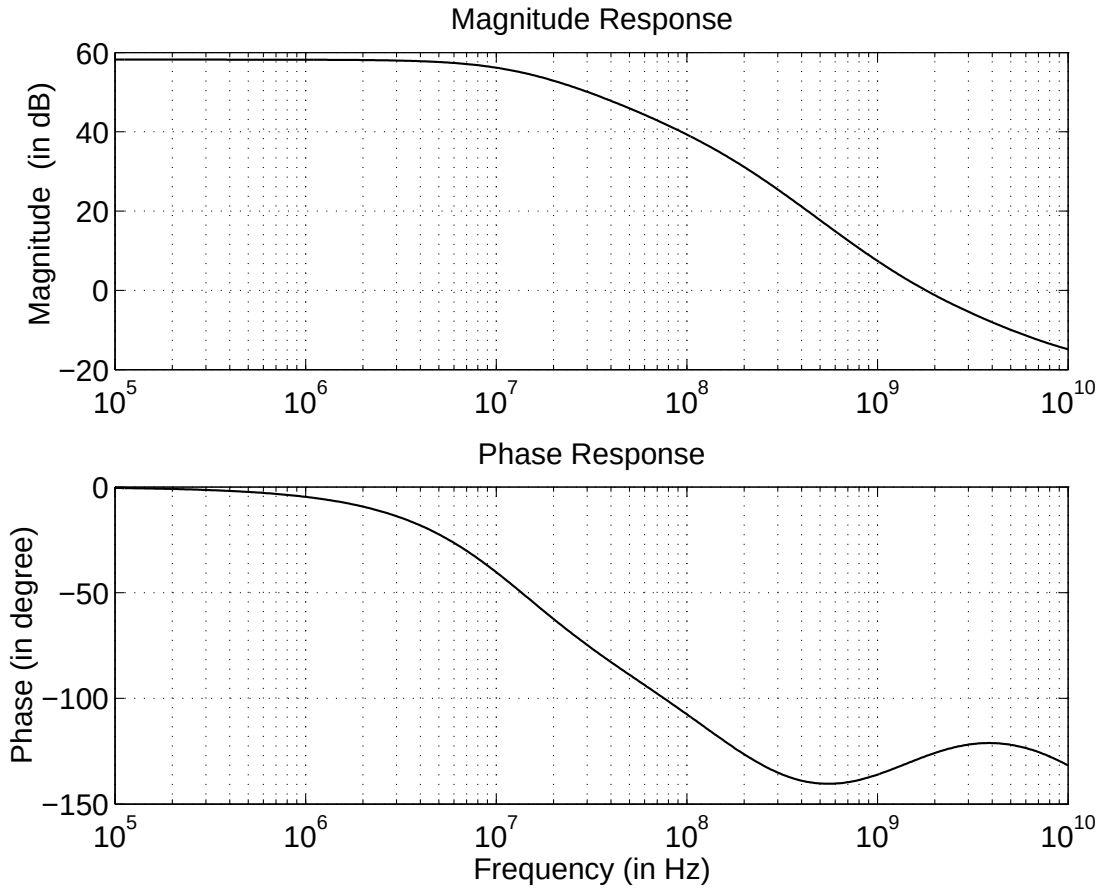

Figure 3.6: The opamp ac response

CHAPTER 4

Tuning Circuit

The frequency characteristic of the Active–RC filter depends upon the product of RC time constant in the filter and that usually changes by variation in the fabrication process, operating temperature, supply voltage, aging and so on. So it is needed to have some kind of tuning mechanism to make AC response stay within the required specification. In order to compensate all this, a fast and accurate on chip tuning mechanism is used here which incorporate the successive approximation register (SAR) scheme [2] & [3]. In this method, the product of the RC is measured by the slope of the step response of the integrator and depending upon the correction needed, it generates a digital code. This method only consumes N clock cycles to get correct N digital bit.

4.1 Tuning Scheme

As the name suggests, this method tries to do successively better approximations to make the variation of the product of the RC to within precision requirement. The Fig.4.1 shows the block diagram of the tuning circuit as originally proposed in [3]. It is based upon the master-slave approach, the slave filter follows the master integrator. All the capacitors, which are associated with the pole of the filter or the integrator, are replaced by the banks of capacitors. When the product RC is

maximum, the tuner chooses the least capacitance (C_{min}) possible from the bank and on the other hand, it chooses the maximum capacitance ($C_{min} + 31C$) possible from the bank when the product is minimum. This way, as the paper[3] claims, the error of the frequency response can be reduced to below $\pm 2.5\%$ with respect to the RC time constant variation of $\pm 40\%$.

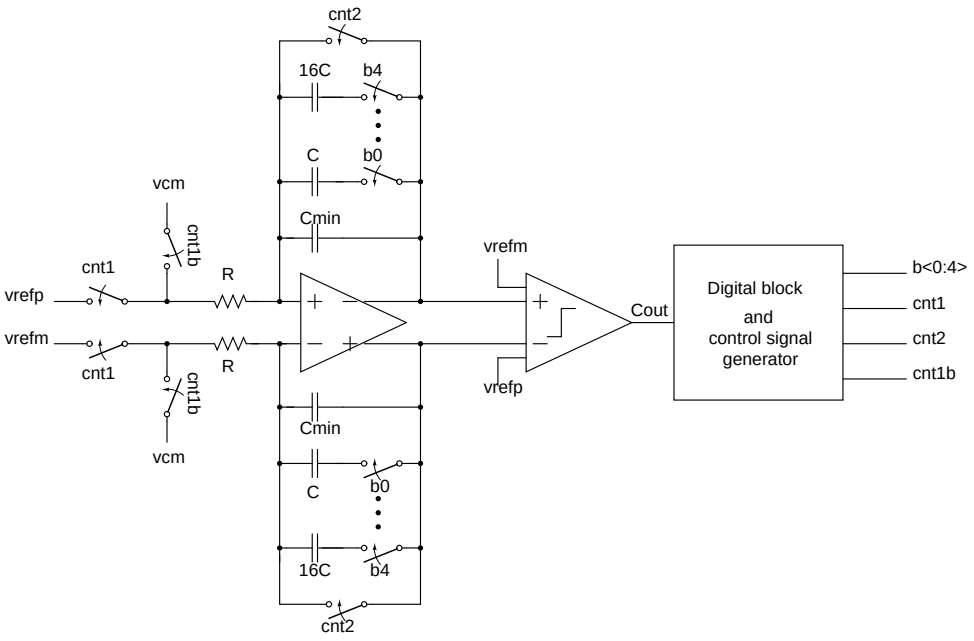

Figure 4.1: The tuner circuit as proposed in the paper [2]

The Fig.4.2 shows the details of this operation. The reset signal initiates the tuning mechanism by setting all the digital control bit to 1 inside the circuit and to complete tuning of the filter, it requires another five clock cycles to get each correct digital control bit per each cycle. In the beginning of each clock cycle, it changes the one of the digital bit from 1 to 0 and compares the output at end of the half clock cycle with the reference voltage and if it results in improvement in the frequency response then it makes that digit to 0 otherwise it stays with 1.

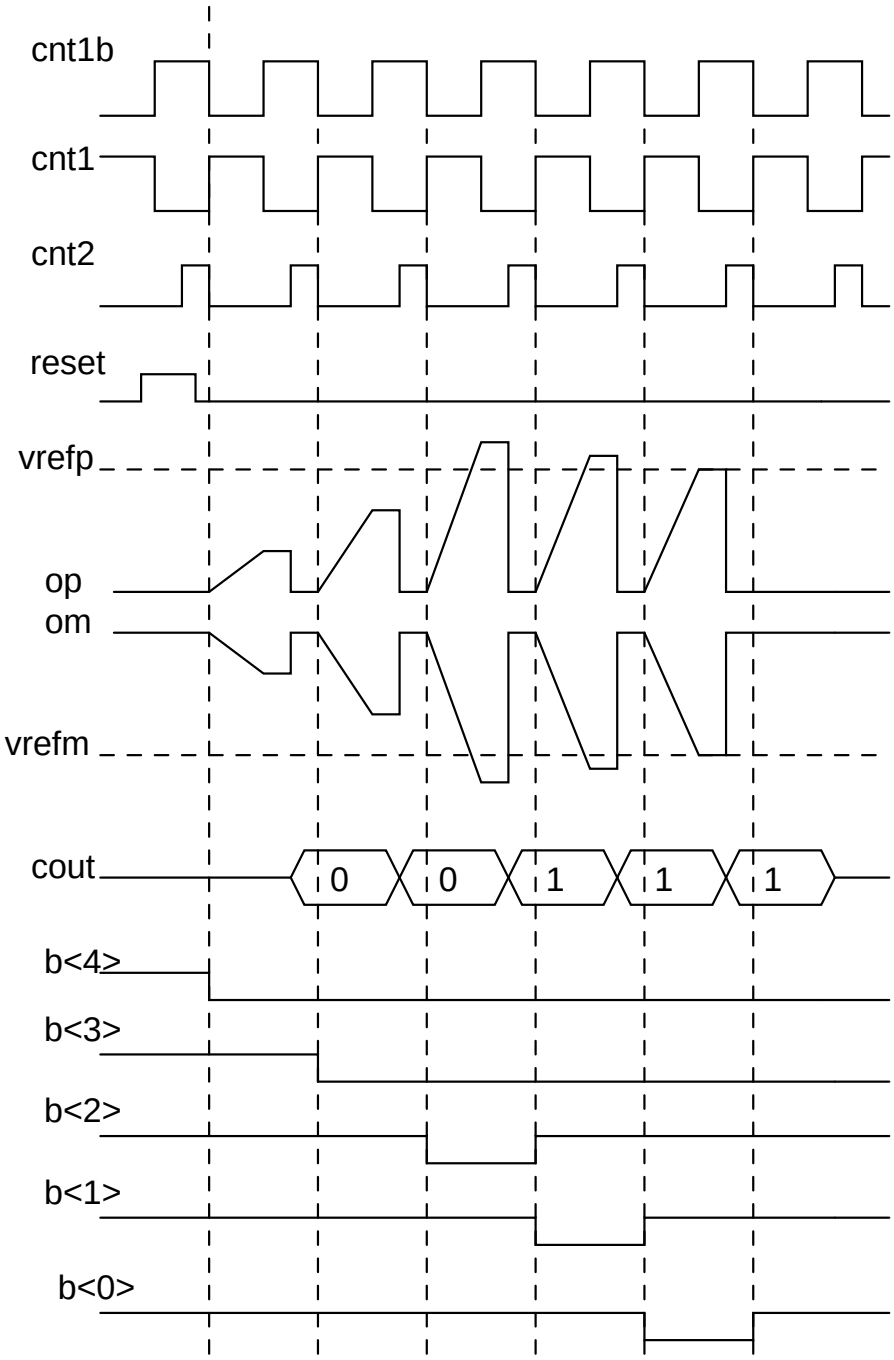

Figure 4.2: Operation example of SAR tuning scheme

The precision to which it is able to stabilize the frequency response depends upon the minimum step size by which RC or (in above case) capacitance can be varied. For the filter designed presented here, the orders of the magnitude of the capacitors is nearby 200 fF and to stabilize the frequency within ±5% the least capacitance required in the capacitor bank would be even smaller than 10 fF, which would be comparable to the parasitic capacitance introduced by the layout of the filter. Hence for this design, by only using capacitor tuning, it is difficult to get the frequency Response to be within less than ±10%. But, if we consider the orders of the magnitude of the resistances inside the filter, they are all more than 50 kΩ, which is really high. As the layout introduces very less additional parasitic resistance inside the filter, if we use resistor bank to tune the RC variation it would be easy to get the product RC within the limit .However, the problem with the resistor tuning is that it is hard to do and it also introduces a lot of distortion compared to capacitor tuning. The design, used here, takes the merits of the both the tuning schemes, it tunes the both resistor and capacitor bank. Using most three significant bits, it tunes the capacitor bank to do coarse tuning and using last two significant bits, it tunes the resistor bank to do fine tuning as shown in Fig.4.3. It also helps to get rid of most of the distortion which could be generated, if only the resistor bank is being used.

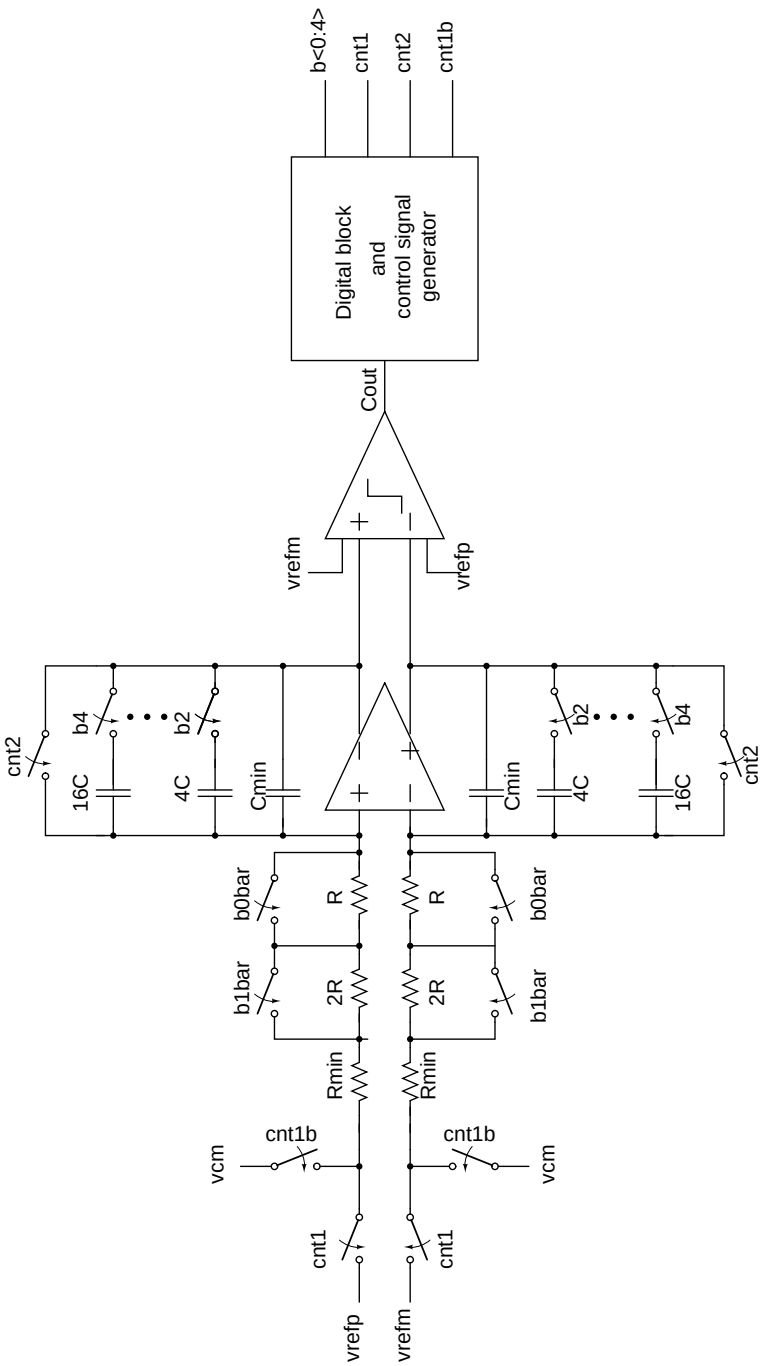

Figure 4.3: The architecture of the proposed tuning circuit

4.2 Implementation

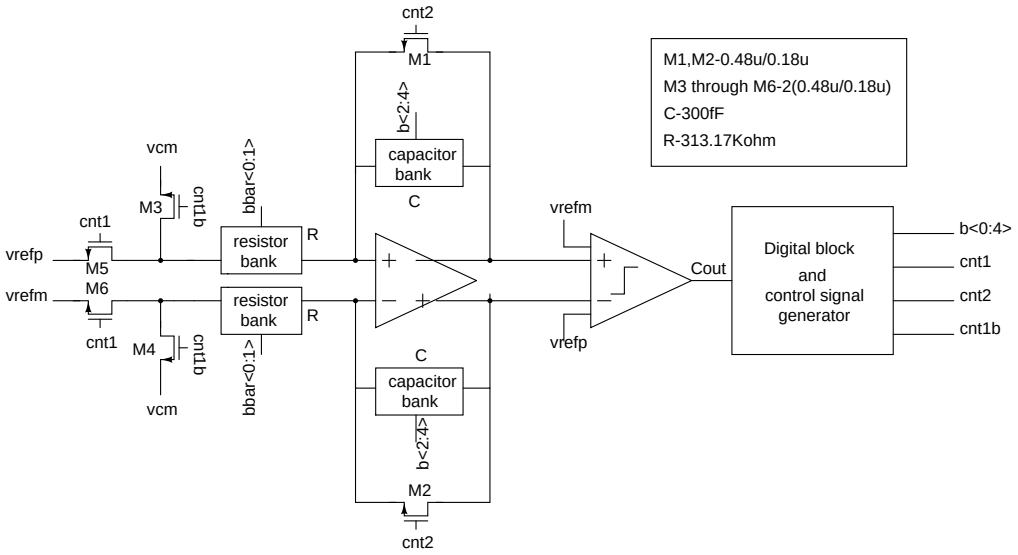

Figure 4.4: The schematic of the tuner circuit

Fig.4.4 shows the implementation detail of the integrator. The sizes of the switches are shown in figure with the actual magnitude of the capacitor and resistor, using which the banks of capacitor and resistor are being made. To turn on and off the switches the gate is being applied with 1.8 Vand 0 V respectively. The Fig.4.5 and Fig.4.6 shows how the capacitor and the resistor bank has been realized respectively. The signal 'bb' is the complementary of the signal 'b'. Note that the ip/im terminal in the both bank is connected to the input terminal of the opamp. The same opamp, which is being used in the main filter, is used to get the advantage of the matching between filter and the integrator. The differential reference voltage is 400 mV and the time period, over which the integrator integrates the input reference voltage, is chosen to be 100 ns and another 100 ns second is required for comparator to do comparison and the digital circuit to generate the digital code. The digital block which makes the decision on the output of the comparator (C_{out} is shown in Fig.4.7).

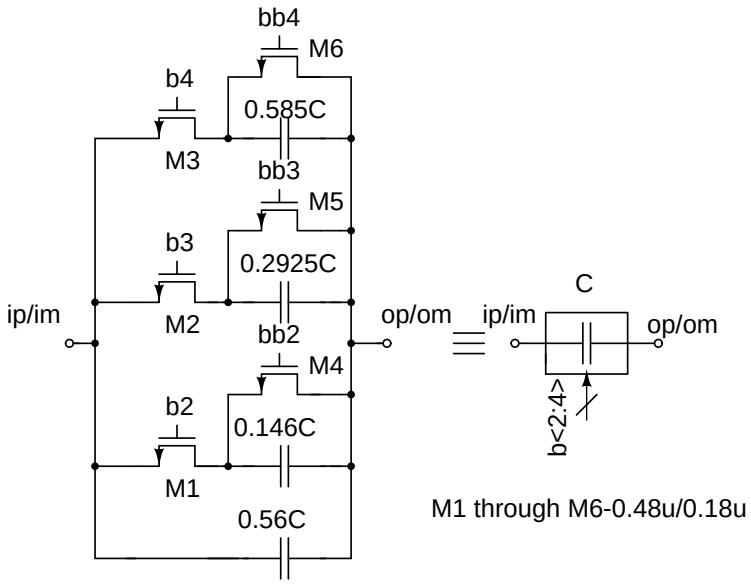

Figure 4.5: The capacitor bank

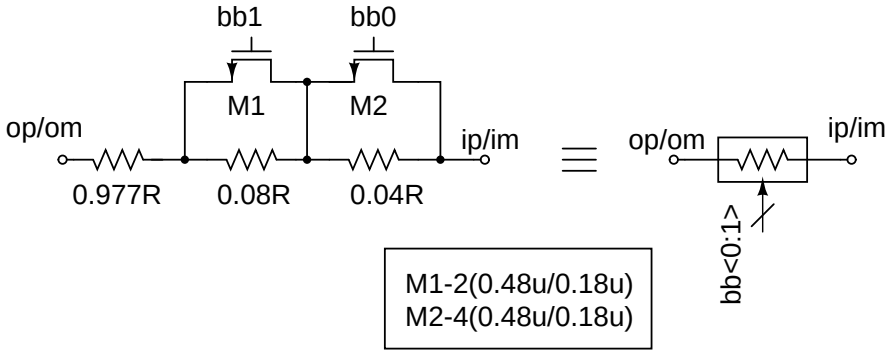

Figure 4.6: The resistor bank

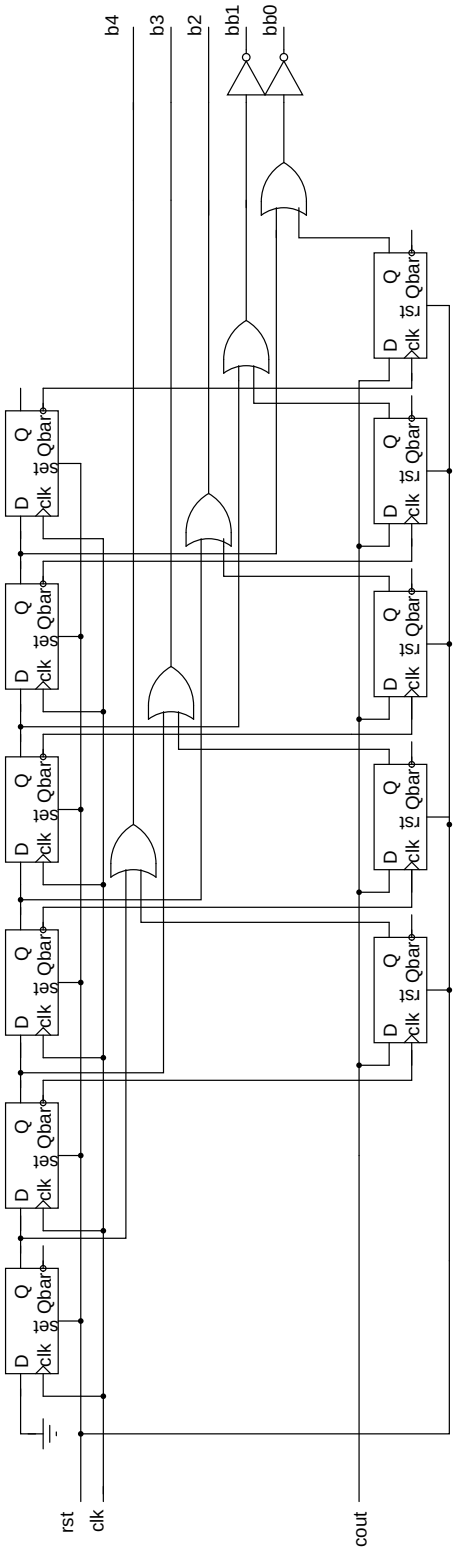

Figure 4.7: The digital block

4.2.1 Comparator

To get correct digital code, the comparator should be as ideal as possible. From the simulation, it has been found that for the proper functioning of the tuning circuit, it is necessary that the comparator should be able to resolve at least 1mV with the frequency of the input is on the order of 10 MHz.

4.3 Results

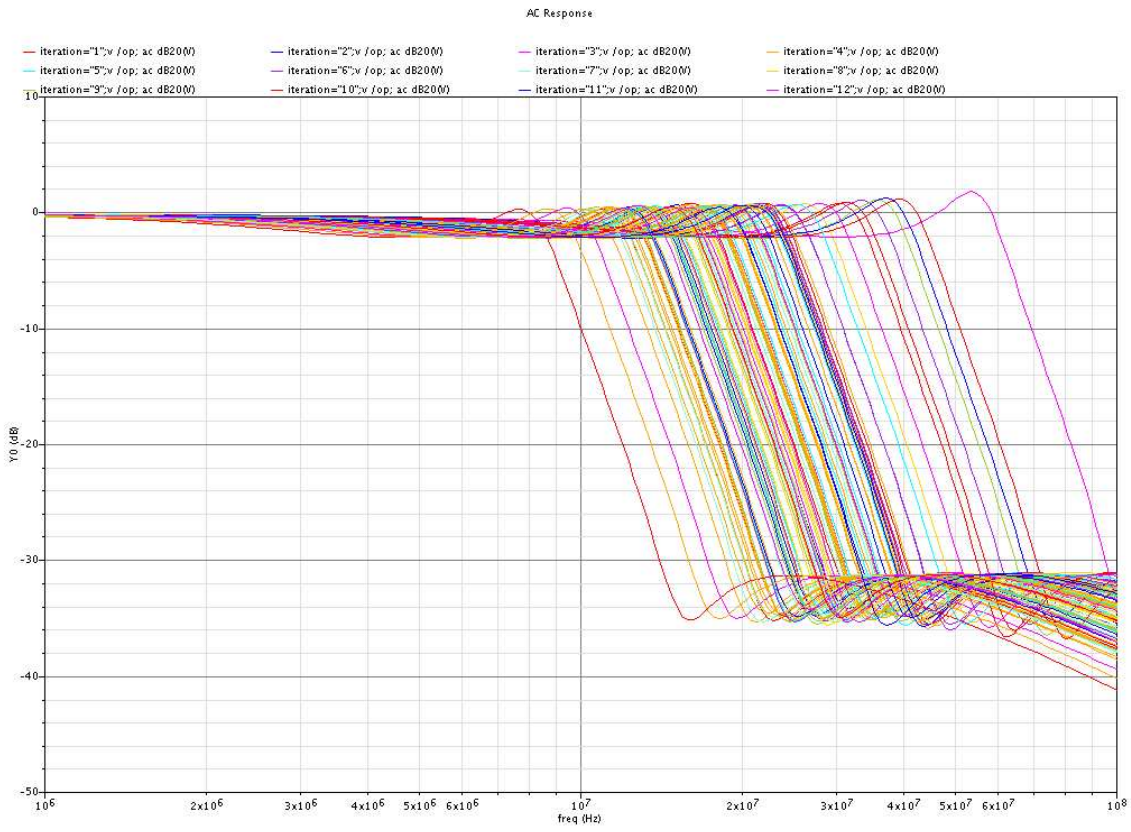

Figure 4.8: The AC response of the filter over 100 Monte-Carlo models with the tuner is OFF

The Fig.4.8 shows the AC response of the filter with the tuner circuit switched off and the Fig.4.9 shows the AC response of the filter with tuning circuit switched on.

In the first case the bandwidth of the filter was varying from -20% to 40% where as in the second case it is within 5%.

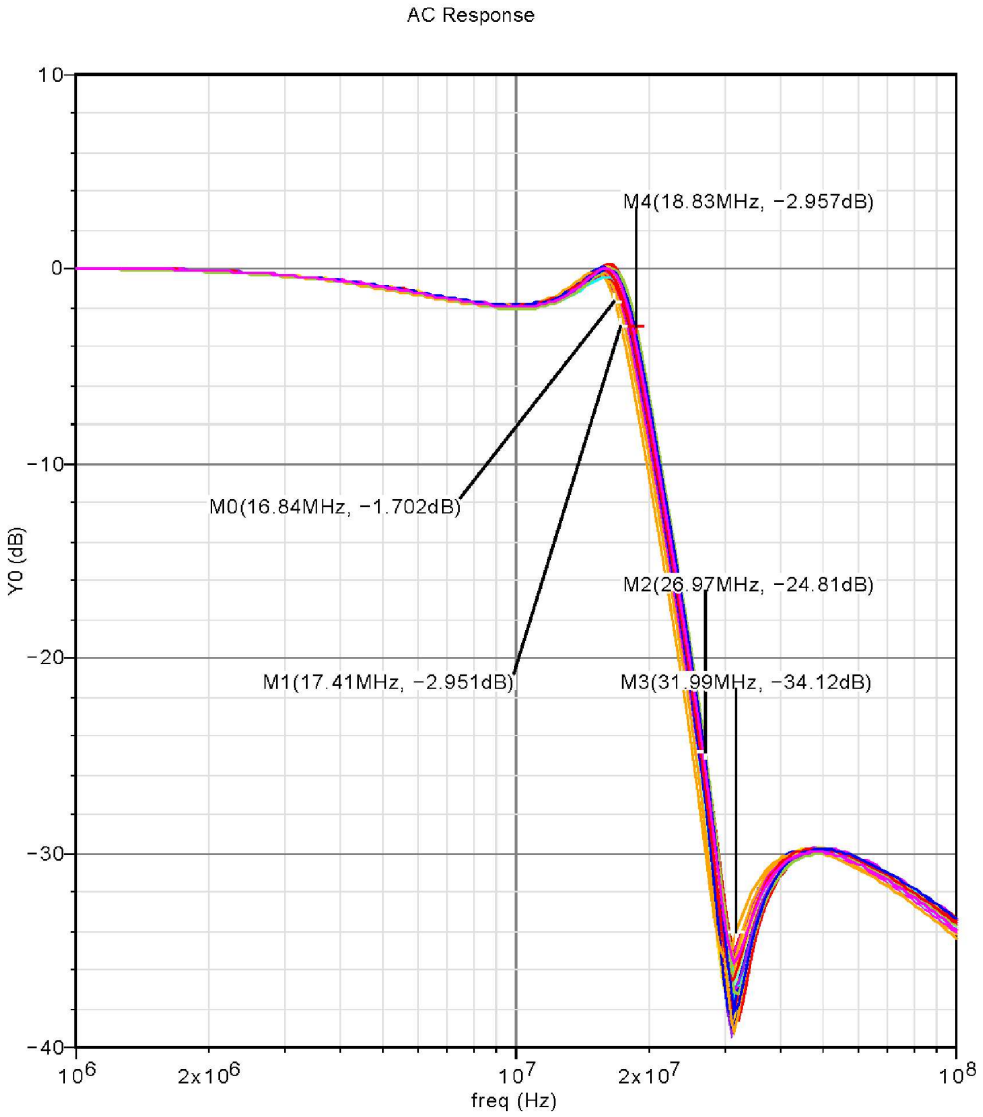

Figure 4.9: The AC response of the filter over 100 Monte-Carlo models with the tuner is ON

CHAPTER 5

Buffer Design and Interfacing with the External World

5.1 Buffer

The opamp designed here is able to support load of 50k Ω over the filter bandwidth of 17 MHz and able to support the load of 20 kΩ over 0-10 MHz frequency range with distortion less than 63 dB. But as the specification requires, the filter has to drive 20 kΩ resistor at the output over the filter bandwidth; it is required to have a good buffer to drive 20 kΩ load resistor. This is because, as the load resistance decreases, the distortion goes up due reduction in the loop gain of the filter.

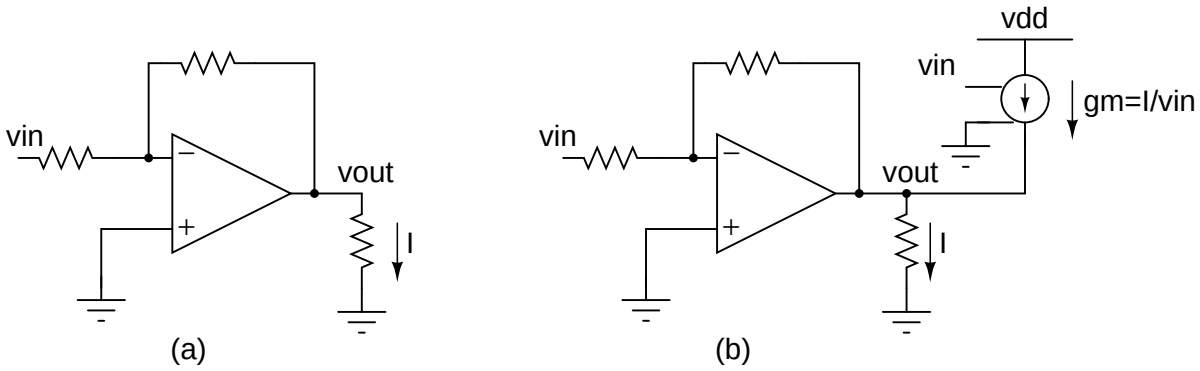

Figure 5.1: The proposed buffer

The Fig.5.1 shown in the left side shows that increased in the distortion comes from the increase in current sucked out of the output node of the opamp because

of the loading effect. To reduce the distortion, one way is to reduce the current supplied by the op amp, as shown in the right Fig.5.1. A voltage controlled current source is used which provide the amount of current required to drive the load. So the transconductance of the of the transconductor has to be $g_m = \frac{1}{R_{load}}$. Even though it generates some amount of distortion, it is being taken care by the feedback network due to high loop gain.

5.1.1 Transconductor Design

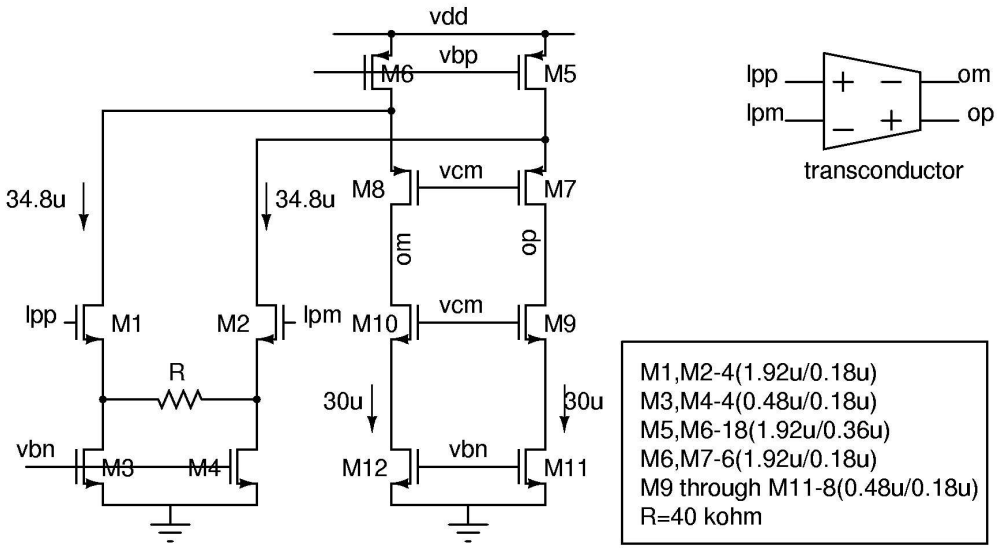

Figure 5.2: The schematic of the buffer is shown

The Fig.5.2 shows the schematic of the transconductor. It behaves as the transconductor only when the output load is much smaller compared to its output resistance and can be model as the voltage control voltage source when the output load is much larger compare to its output resistance. The input stage of the transconductor is source degenerated so that the gm of the transconductor is equal to $\frac{1}{20k\Omega}$. It converts the input voltage into the current and pumps that current

through the transistors M7 and M8, which behave as a current controlled current source, to enhance the output resistance of the current source.

The low pass output of the biquad is applied as the input to the transconductor and the output of the transconductor (op and om) is connected to the output of the filter. The common mode feedback circuitry of the opamp stabilizes the output common mode voltage of the transconductor.

5.2 Complete Filter

With this transconductor the schematic of the filter is shown in Fig.5.3.Each resistor shown in the figure are resistor bank4.6 and each capacitor used are the variable capacitor bank2.3.

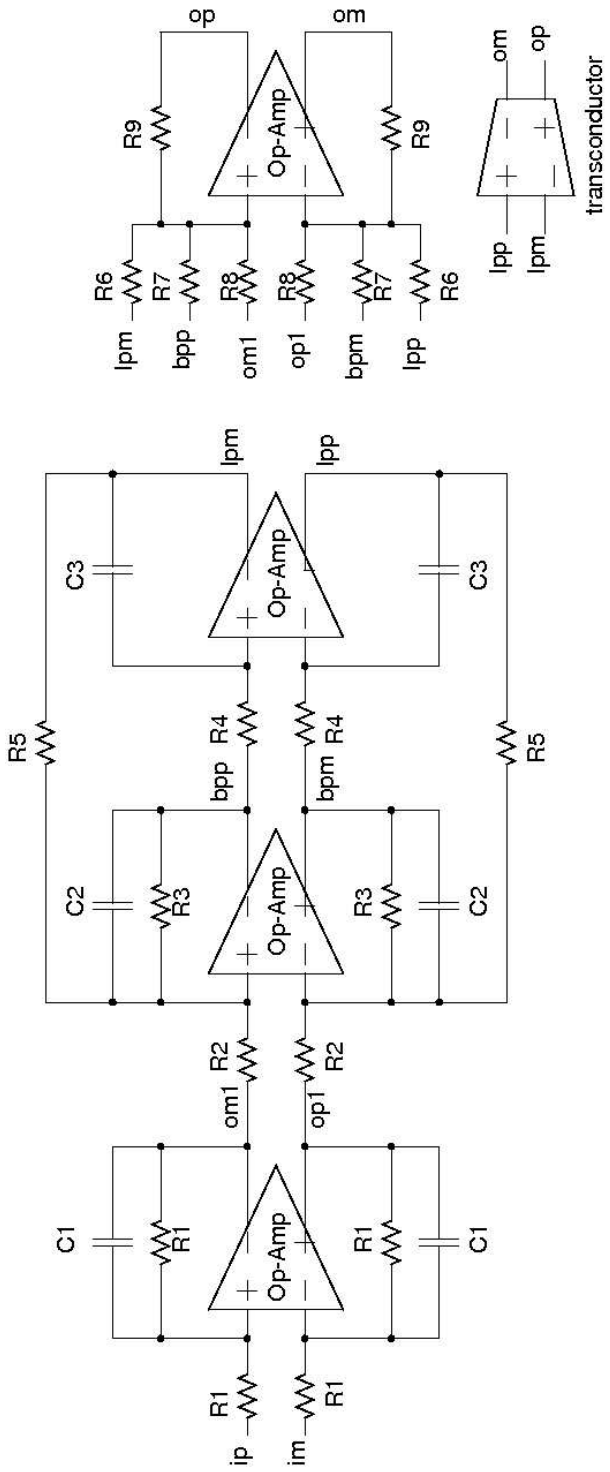

Figure 5.3: The final schematic of the filter is shown here. All the capacitor are has representing the variable capacitor bank2.3 and all the resistor are representing resistor bank4.6 of there corresponding sizes. The magnitudes of the components are the following. R1=92 kΩ, R2=74 kΩ, R3=179 kΩ, R4=64 kΩ, R5=54 kΩ, R6=55.7 kΩ, R7=470 kΩ, R8=195 kΩ, C1=236 fF, C2=161.97 fF, C3=159.5 fF.

5.3 Interfacing with the External World

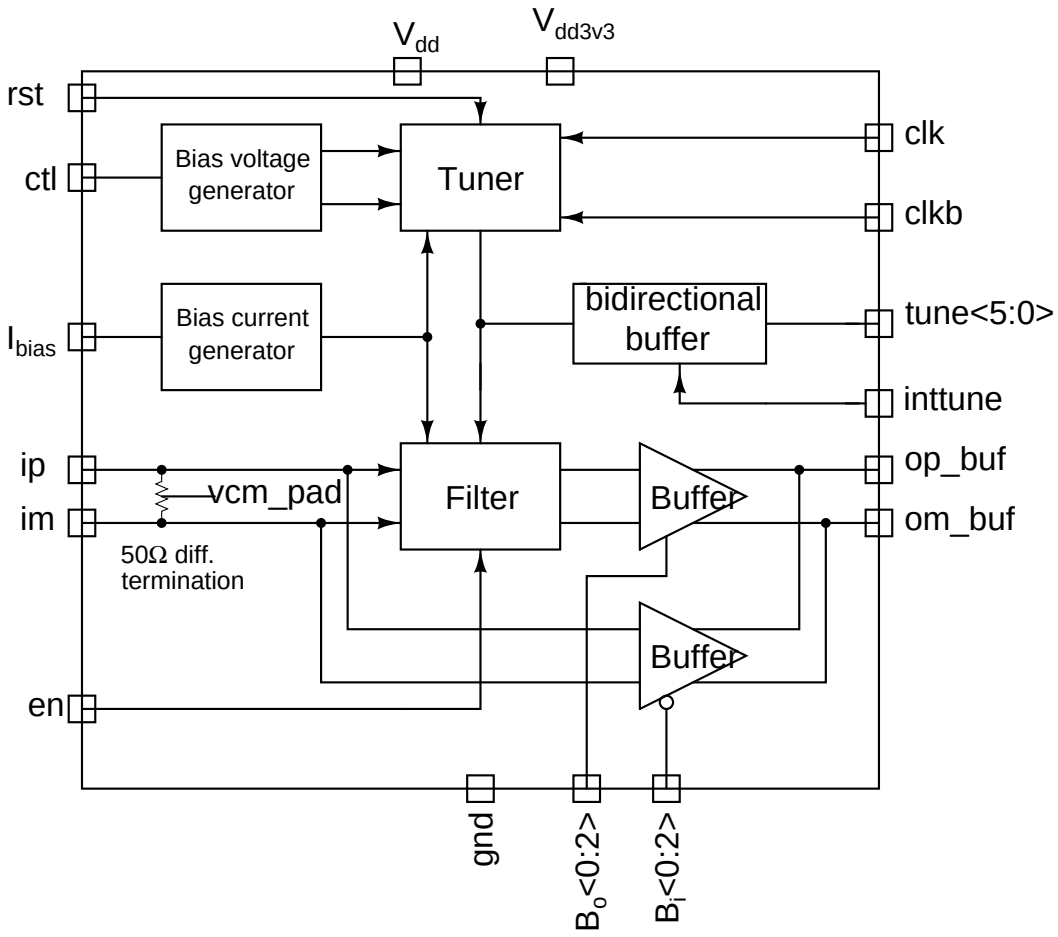

Figure 5.4: Block diagram of chip

The block level description with all the input and output pins of the filter is shown in Fig.5.4. The differential input to the filter is ip and im, which are differentially terminated by 50 Ω resistor. The common mode voltage to the filter is applied through the vcm_pad pin. To test the filter, extra peripheral are added to the chip. The output of the filter is buffered by the test buffer, which in turn drives the off chip load to test the output of the filter, but it changes the transfer function from input to output path due to added AC response of the test buffer. To cancel it the input is also passed through the similar test buffer. The detail of the operation of

the test buffer and the testing technique is given in [4]. The en signal is used to change the bandwidth of the filter. The on chip tuning circuit requires a 100 MHz clock signal with its complement and the tuning operation starts as soon as the reset signal gets activated. Depending upon the digital value of the inttune signal, the bidirectional buffer can be used to either test or control the digital control bits, generated by the tuning circuit.

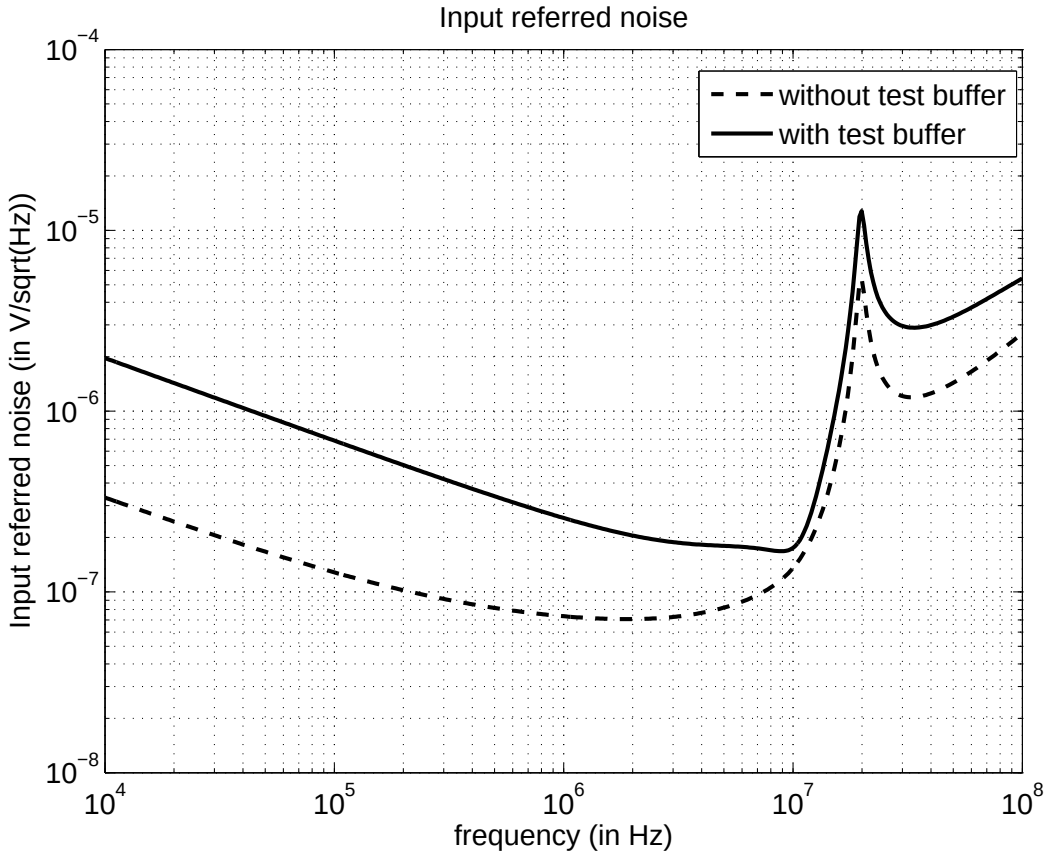

Figure 5.5: Input referred Noise

The total integrated noise at the output of the test buffer is 8dB more compare to that at the output of the filter. Due to noise generated at the output of the test buffer is dominating, to measure the output noise of the filter the noise of the buffer has to be calibrated. Using the noise calibration technique shown in [4], the noise

of the filter can be measured. The spectral density of the input referred noise at the output of the filter and at the output the test buffer in shown in Fig.5.5. The third harmonic distortion at the output of both filter and the test buffer is shown in Fig.5.6. The input applied here is 1.4 V p-p differential with 15 MHz frequency. As we can see, the distortion generated by the buffer is dominating and for this particular case, the distortion generated is 60dB.

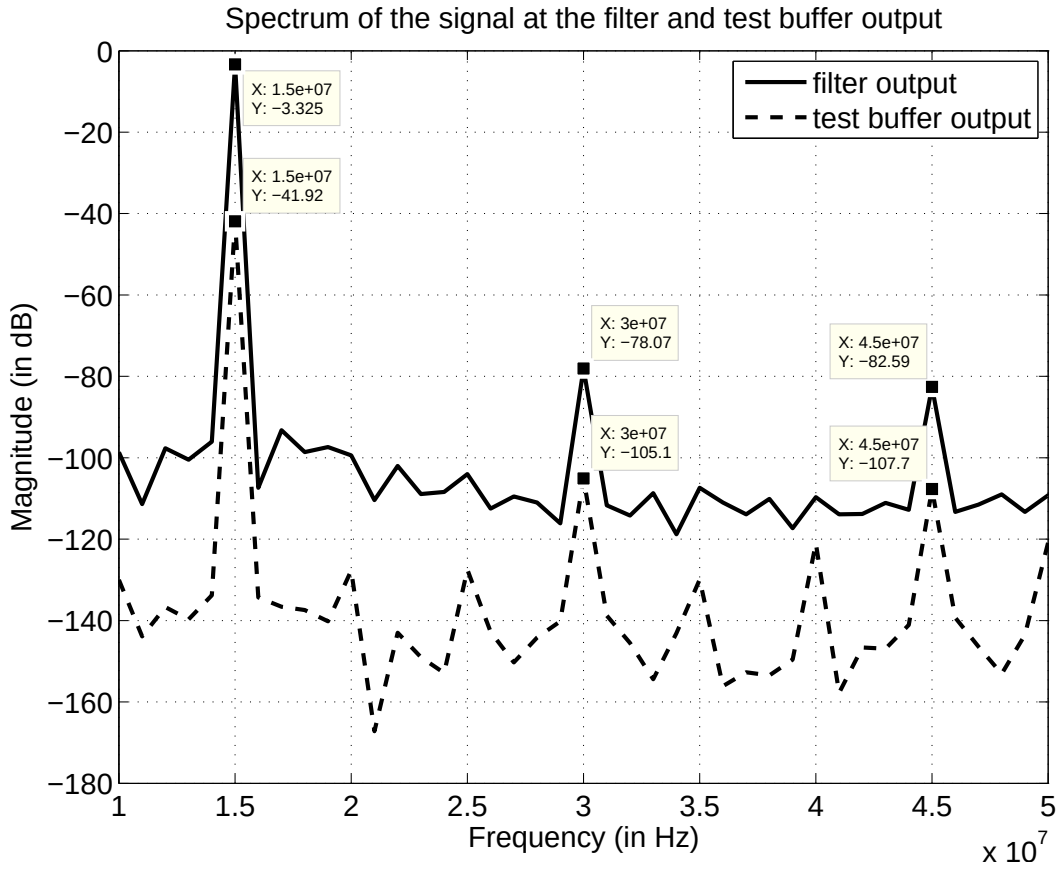

Figure 5.6: Distortion due to test buffer

CHAPTER 6

Layout

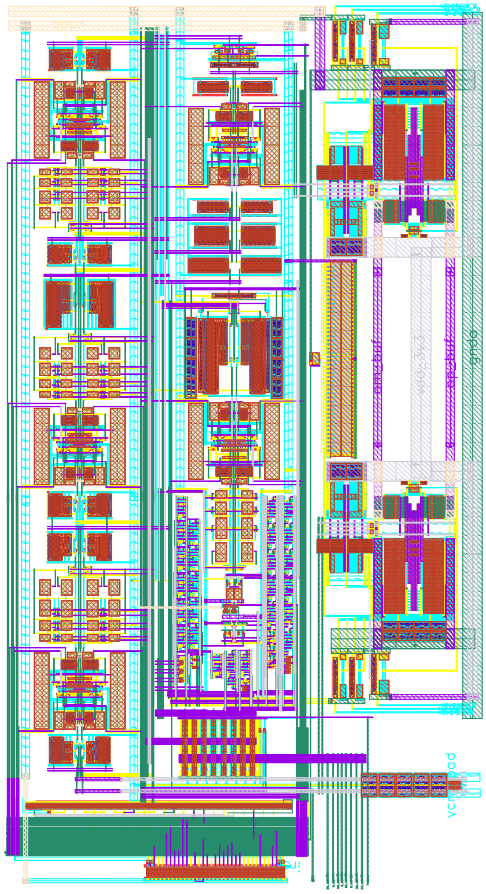

Figure 6.1: Layout

Table 6.1: Layout Area

Circuit	Area
Whole filter	$900\mu m \times 480\mu m$
Opamp	$80\mu m \times 90\mu m$
Tuning circuit	$480\mu m \times 150\mu m$

CHAPTER 7

Results and Conclusion

7.1 The AC Response of the Filter

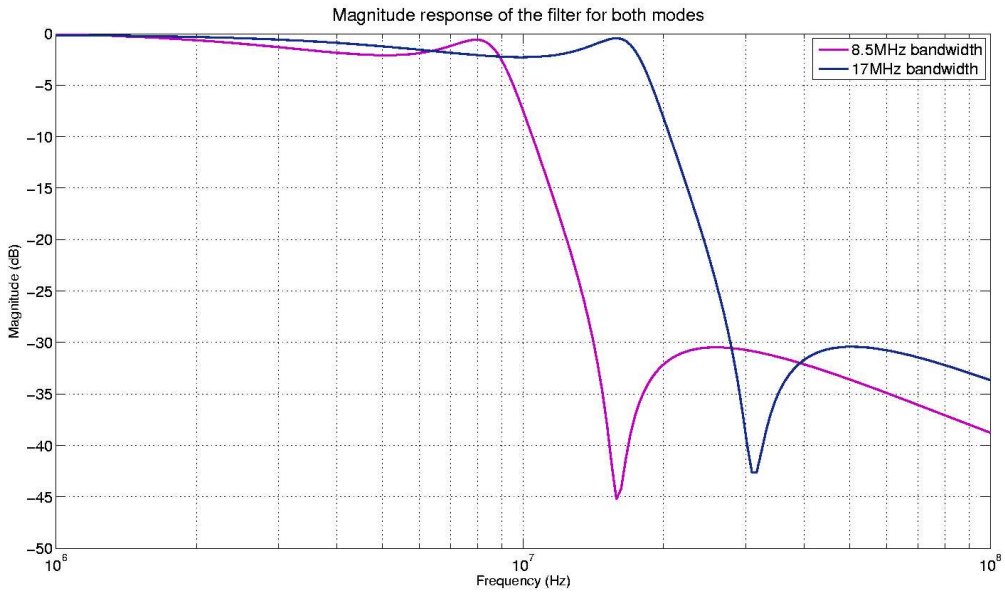

Figure 7.1: AC Response of the filter

The Fig.7.1 shows the AC response of the filter for both mode of the operations. It can be seen that the AC response for 8.5 MHz bandwidth is perfectly scaled version of the filter with bandwidth 17 MHz. After finishing layout, the AC response of the filter layout is simulated over 26 Monte Carlo RC process corners and the plot of the response is shown in Fig.7.2.

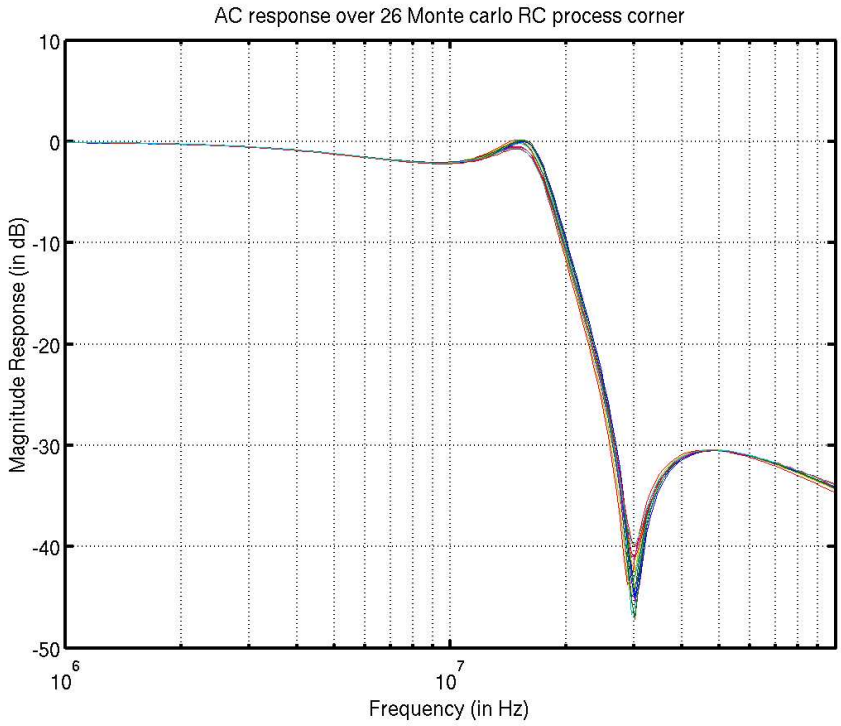

Figure 7.2: AC response of filter layout

7.2 Performance

The third harmonic distortion and the intermodulation distortion of the filter over frequency Range of the operation is plotted in Fig.7.3 and Fig.7.4 respectively. For the peak to peak differential 1.4 V, more than 50 dB SNDR is being achieved. To get intermodulation distortion characteristic, two sine waves of individual signal swing of 0.7 V peak to peak differential with the frequency offset of 0.5 MHz summed and given as a input to the filter. The spectral density of the output noise is shown in Fig.7.5. The most important performance parameter are shown in table 7.1.

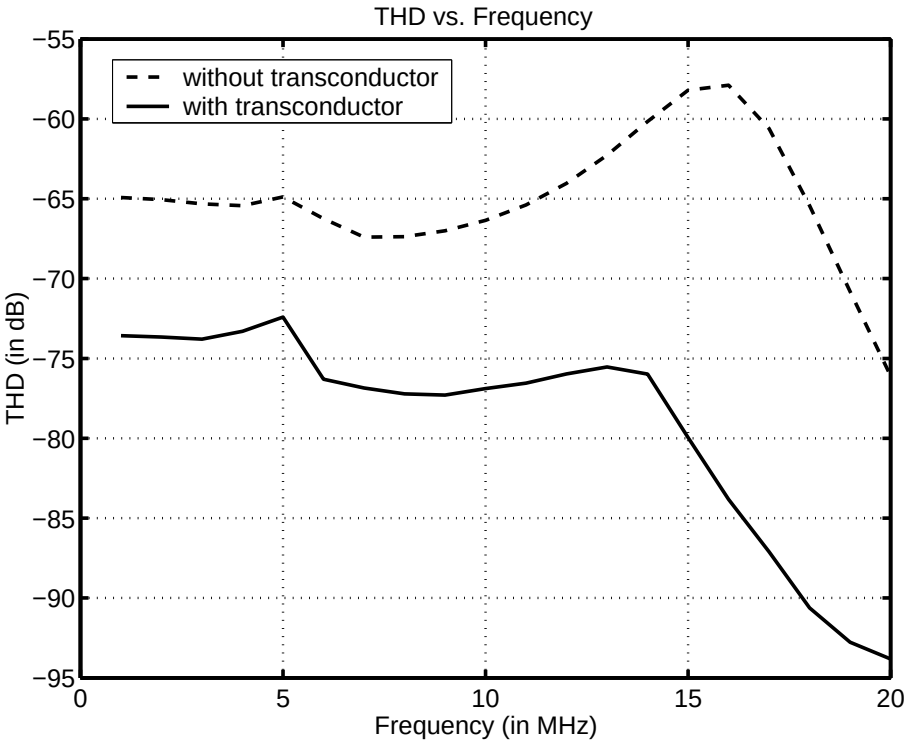

Figure 7.3: THD with and without transconductor

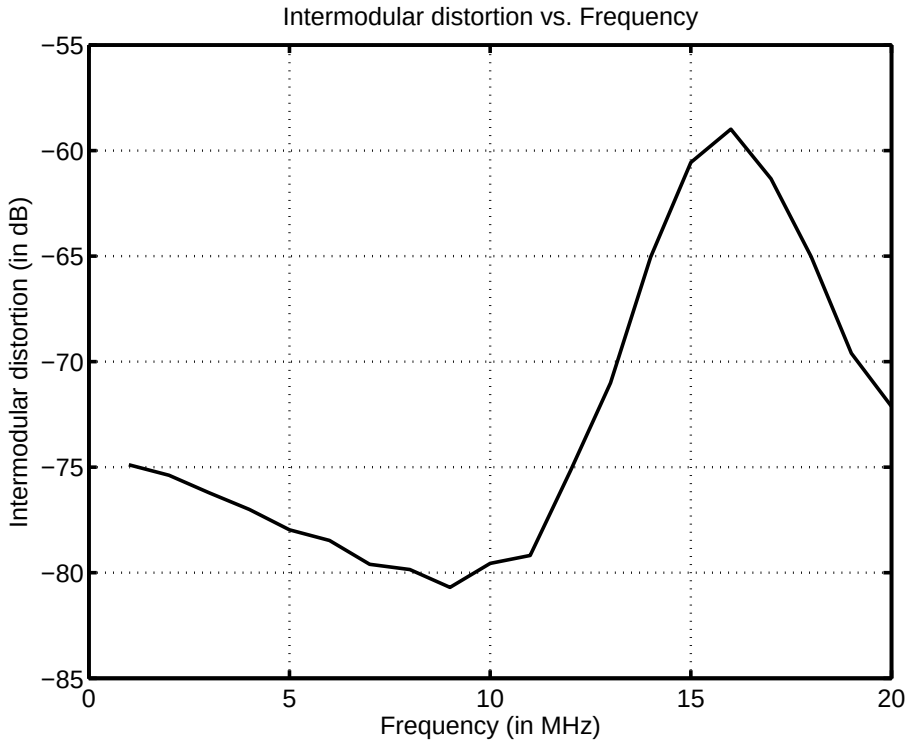

Figure 7.4: Intermodulation distortion

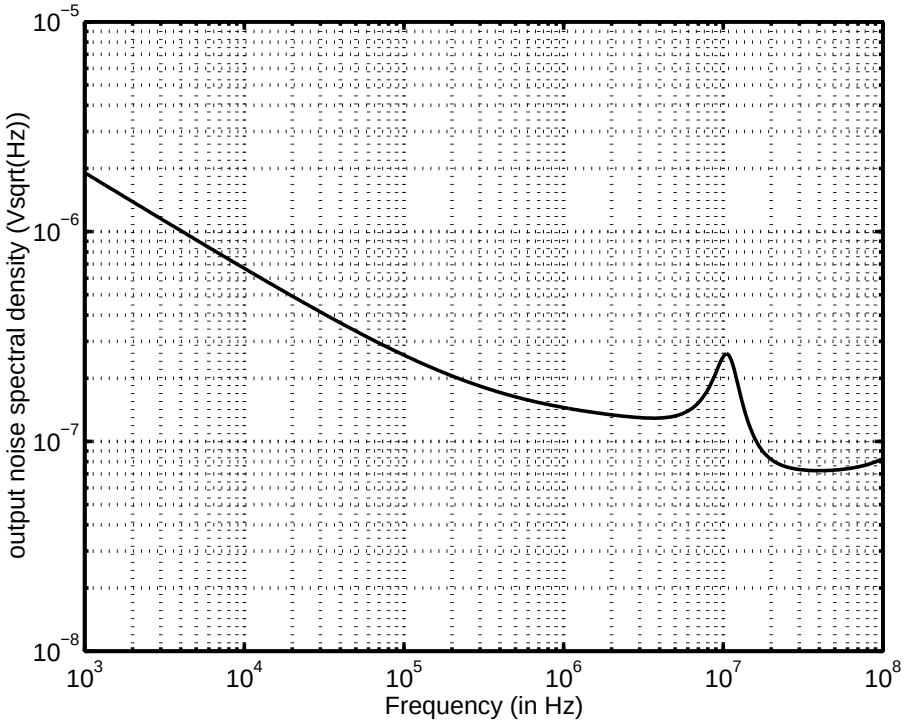

Figure 7.5: Output noise spectrum

Table 7.1: Summary

Type of Filter	Elliptic
Order	3
Technology	$0.18\mu m$
Power Supply	1.8 V
Total Noise	55 dB
SQNR@ 1.4 V peak-peak differential signal swing	50 dB
Power Consumption	1.6 mW

7.3 Conclusion

Design of the lowpass filter with the variable bandwidth is designed. The opamp-RC structured is used with the opamp are optimized for the low power consumption. With the help of the digital tuning circuitry and the intergrator as the sensor,the frequency response is stablized within 5%. Dynamic range of more than 50 dB is achieved with the help of a buffer to drive the 20 kΩ load resistance.

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[3] Youngjoo Cho, Jinup Lim, Kyungsoo Jung, Jongmin Park, Huikwan Yang, Sanghyun Cha, Joongho Choi, *"Fast On-Chip Tuning Circuit for Active-RC Filters using the SAR Scheme"*, IEEE Circuit and Systems, vol. 2, pages 1522-1525, Sept, 2005.

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