Testing and Characterization of a High Speed $\Delta\Sigma$ Modulator

A THESIS

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Testing and Characterization of a High Speed $\Delta\Sigma$ Modulator** , submitted by **Wansagar Rohit Marotirao**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I would like to thank my classmates Anoop, Sreejith, Ravi, Prasad and my friends in the DSDL lab and testing lab for their support and the friendly atmosphere in lab. I would like to thank all my friends in particular Somu, Anand, Sandip, Pravin, Pradip and Bikshu for their help throughout my life.

Finally, I dedicate this thesis to my family members and friends without whom my life has no meaning.

ABSTRACT

This project involves the testing of a High speed $\Delta\Sigma$ Modulator compensated for more than unity feedback delay. The chip tested as part of this thesis contains a fast feedback path to compensate for delays which are greater than one clock cycle. This led to realize very high sampling speeds on 0.18μm technology. The chip tested was a 4-bit modulator with sampling speed of 800 MHz, whose output is decimated by a factor of oversampling ratio (OSR) and also passed through a digital driver. The decimated output is 16-bit digital output which is taken through logic analyzer. The driver output is captured through oscilloscope. The chip consumes $82.07mW$ of power from a 1.8 V supply. The measured dynamic range is 44 dB for OSR of 25.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CT	Continuous Time
CTDSM	Continuous Time $\Delta\Sigma$ Modulator
DAC	Digital to Analog Converter
DR	Dynamic Range
DSM	$\Delta\Sigma$ Modulator
DT	Discrete Time
LVDS	Low Voltage Differential Signaling
MSA	Maximum Stable Amplitude
OBG	Out of Band Gain
OSR	Oversampling Ratio
PSD	Power Spectral Density
PCB	Printed Circuit Board
SMA	SubMiniature version A
SNR	Signal to Noise Ratio
SoC	System-on-chip
SQNR	Signal to Quantization Noise Ratio

CHAPTER 1

Introduction

1.1 Introduction

Due to increase in the use of computers and advancements in other digital media there is a tremendous demand for digital signal processing. One of the main reasons behind this being lesser susceptibility of digital signals to noise and ease of computation. But the actual interfaces to the real world are analog. This imposes need of data converters which forms an interface between analog and digital domain. Hence, analog-to-digital converters (ADCs) have become an essential part in today′s System-on-Chip (SoC) trend.

$\Delta\Sigma$ modulators (DSM) are a special class of data converters, which are oversampled and noise shaped ADCs. They are closed loop negative feedback converters wherein the quantization noise is high pass filtered by the loop without affecting the input signal strength. They are implemented either as continuous time (CTDSM) or discrete time (DTDSM) modulators.

CTDSM has many advantages over DTDSM such as inherent anti-aliasing property, lower power consumption, higher maximum speed in a given technology. Inherent anti aliasing saves both area and power. Also in a given technology the sampling frequency of a CT $\Delta\Sigma$ modulators is limited by the excess loop delay(ELD) present in the loop because of the quantizer and the feedback DAC.

Most of modulators have ELD compensation but they are mostly valid for ELD less than one clock cycle . This again limits the sampling frequency. Thus to realize higher

sampling frequency we need to design the modulator which can compensate for much higher ELD. The chip [3] which is tested as part of this thesis work employs one such technique which can compensate for ELD between one to 2 clock cycle delays [4]. This led to a very high sampling frequency for a 4-bit $\Delta\Sigma$ modulator designed on 0.18μm technology.

$\Delta\Sigma$ modulator along with the decimation filter is tested to work at 800 MHz as a part of this project work.

1.2 Organization

Chapter 2 explains the basic concepts of $\Delta\Sigma$ modulators and provides background knowledge.

Chapter 3 discusses the complete architecture of the $\Delta\Sigma$ analog to digital converter(ADC) after combining the Decimation filter to DSM.

Chapter 4 discusses PCB design, the test setup and the measurement results.

Chapter 5 concludes the thesis.

CHAPTER 2

$\triangle\Sigma$ Modulator Basics

2.1 Nyquist Theorem and Quantization Noise[3]

The Nyquist theorem states that a signal must be sampled at least twice as fast as the bandwidth of the signal (f_B) to accurately reconstruct the waveform; otherwise, the high-frequency content will alias at a frequency inside the spectrum of interest (pass-band). The minimum required sampling frequency, in accordance to the Nyquist Theorem, is the Nyquist Frequency ($f_{s,nyqt}$). Fig. 2.1.a shows the multibit ADC which convert analog input signal $y(t)$ to digital output bit stream $v[n]$. Fig. 2.1.b shows the equivalent quantization noise model. The quantization noise power σ_q^2 added by an ADC sampling at $f_s \geq f_{s,nyqt}$ with V_{lsb} as the level spacing, is given by $V_{lsb}^2/12$. The quantization noise is assumed to be white and has a *Power Spectral Density* (PSD) of $\frac{\sigma_q^2}{f_s/2}\ V^2/Hz$ and is shown in Fig. 2.2(a). Now if the sampling rate is doubled keeping the f_B same, then the noise PSD will reduce to half (Fig. 2.2(b)), as the total noise power is constant. For every doubling of the sampling rate, the noise reduces by a

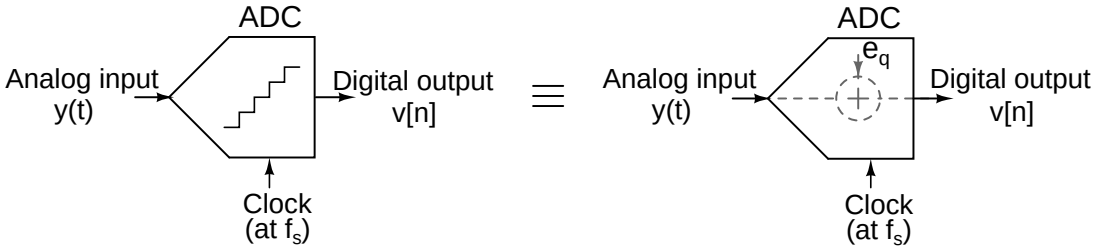


Figure 2.1: (a) ADC (b) Additive quantization noise model.[3]

factor of 3 dB (3 dB/octave). The ratio of sampling frequency f_s to the Nyquist rate $2f_B$ is called the *Oversampling Ratio* (OSR) which is one of the most important parameters

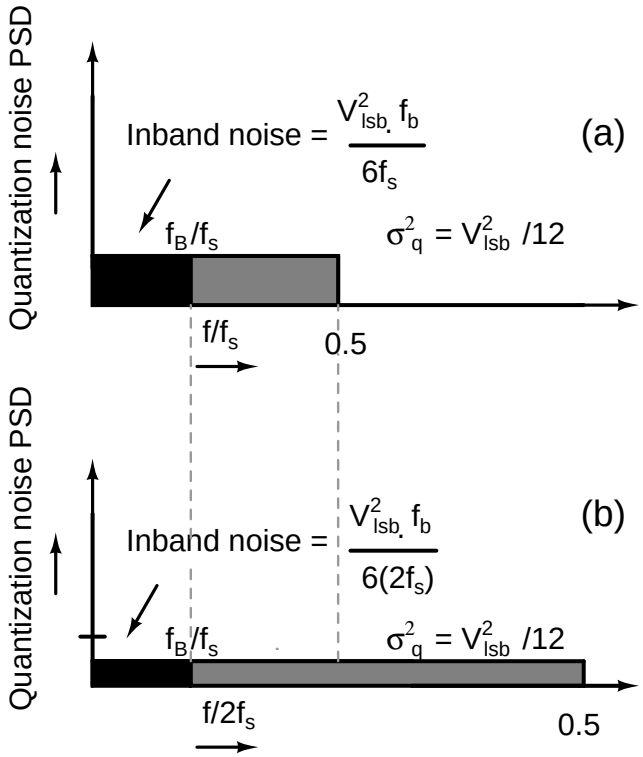


Figure 2.2: Quantization noise spectrum of ADC. (a) Sampling at f_s (b) Sampling at $2f_s$.[3]

used to characterize oversampling data converters. For an N bit ADC with OSR as the oversampling ratio, *Signal to Quantization Noise Ratio* (SQNR) is given by Eq. 2.1.

$$SQNR_{max}\,[dB] = 6.02N + 1.76 + 10log_{10}OSR \tag{2.1}$$

The oversampling can be used to trade speed for resolution of ADC. However, the rate of this trading is only 3 dB/octave with plain oversampling. A better way of utilizing this advantage of oversampling is to filter away the noise in the signal bandwidth to higher frequencies, and this what the $\Delta\Sigma$ modulator accomplishes. The block diagram of a discrete time $\Delta\Sigma$ modulator is shown in Fig. 2.3.a and Fig. 2.3.b shows the discrete time $\Delta\Sigma$ modulator with additive noise model for the quantizer. A discrete time modulator is shown for ease of explaining the operation of the modulator. The closed loop architecture can be linearized by modeling the quantization noise as an additive noise. Again, it is assumed that the quantization noise is uniformly distributed and not

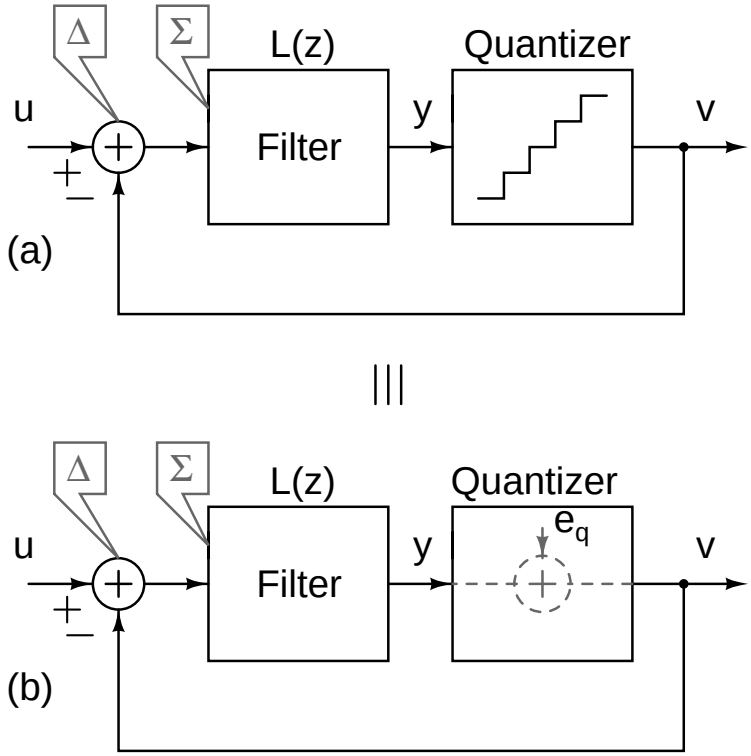


Figure 2.3: $\Delta\,\Sigma$ modulator.[3]

dependent on the input signal u. This system has two inputs, u and e_q, and one output, v. The transfer function from u to v, which is called *Signal Transfer Function* (STF), is given by:

$$STF(z) = \frac{V(z)}{U(z)} = \frac{L(z)}{1 + L(z)} \tag{2.2}$$

The *Noise Transfer Function* (NTF) which is defined as the transfer function from e_q to v, is given by:

$$NTF(z) = \frac{V(z)}{E_q(z)} = \frac{1}{1 + L(z)} \tag{2.3}$$

If the filter $L(z)$ is a low-pass filter with a high DC inband gain, then STF would be unity in signal band and NTF would be a high-pass filter. This high-pass NTF helps in filtering out the in-band quantization noise to out of band region as shown in Fig 2.4. Inside the signal bandwidth, the quantization noise is attenuated approximately by the

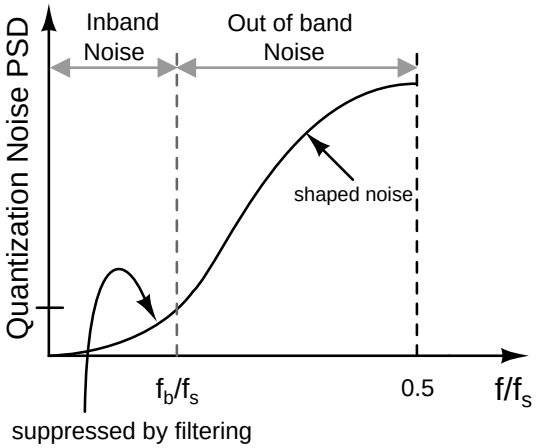


Figure 2.4: Spectrum of the shaped quantization noise.

large gain of the filter $L(z)$. The output spectrum of the modulator is given by,

$$V(z) = STF(z)U(z) + NTF(z)E_q(z) \tag{2.4}$$

As an example, if $L(z) = 1/(z-1)$, then from Eq. 2.4, we get

$$STF(z) = z^{-1} \tag{2.5}$$

$$NTF(z) = 1 - z^{-1} \tag{2.6}$$

From Eq. 2.5, we see that $STF(z)$ is just a delay while $NTF(z)$ has a high pass response. If we want to achieve a very high in-band SQNR, we must choose a sampling rate f_s much higher than the Nyquist rate so that the total quantization noise within the signal band is reduced.

2.2 Continuous-time vs discrete-time[3]

Switched-capacitor (SC) circuits form the building blocks of DT $\Delta\Sigma$ Modulators. SC filters used to be the choice of design for $\Delta\Sigma$ Modulators as they provide high accuracy and linearity. SC filters are unattractive for use in very high speed designs as the settling time and power requirements of opamps used in SC filters pose a serious limitation. Moreover, the need for an anti-aliasing filter before converting the continuous-time input to a discrete-time input has led to an increase in the usage of CT modulators.

The block diagram of a Continuous-time $\Delta\Sigma$ Modulator is shown in Fig. 2.5. A CT

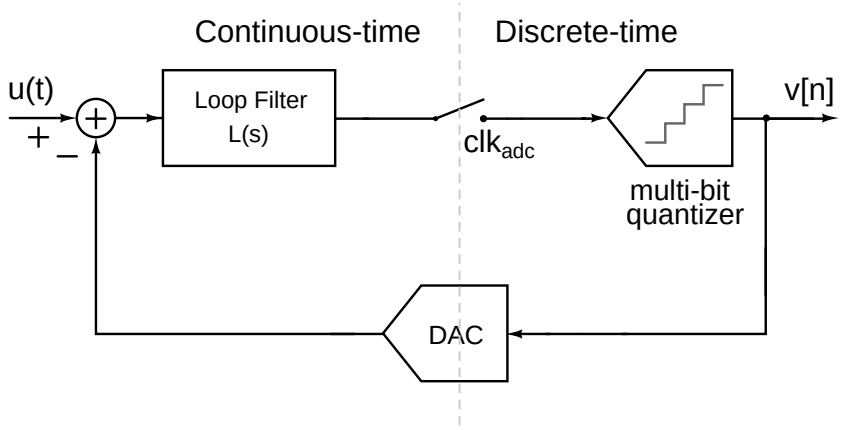


Figure 2.5: Block diagram of a continuous-time modulator.[3]

modulator is derived from its DT counterpart by pushing the sampler from outside the loop to within the loop. A *Digital to Analog* (DAC) is used in the feedback path to convert the digital output $v\,[n]$ to an analog signal, which feeds to the input of the loop filter. CT modulators obviate the need for anti-aliasing filters because the loop filter does inherent anti-aliasing [2]. The maximum frequency of operation in CT modulators is limited by the delay in the quantizer and the feedback DAC while DT modulators are limited by the settling time of the opamps. In general, CT modulators can be operated at a higher frequency than a DT modulator in a given technology.

2.3 Basic components of the CTDSM[3]

2.3.1 Loop filter

The basic circuit blocks of which a CT loop filter consists are the CT integrators. Many kinds of CT integrators are available but the most commonly used ones are active RC integrators and G_m-C integrators. The integrators used in this chip are active RC integrators.

2.3.2 ADC

The ADC quantizes the output of the loop filter to produce the output of the modulator. Any circuit level nonlinearities in the ADC are shaped out of the signal band. Hence the design constraints on the ADC are very relaxed. The only constraint is the regeneration time of the latch in the ADC, which limits the maximum sampling rate. Hence the flash architecture, which implements the fastest ADC, is the common choice for implementing this internal ADC of the modulator.

2.3.3 DAC

The DAC converts the output to analog and feeds back to the input. Hence, any non-idealities in the DAC are expected to appear at the input and hence at the output of the modulator, as the transfer function from input to output is unity in the signal band. The DAC elements are bound to have mismatch, which affects the inband performance of the modulator. Standard practices like data weighted averaging (DWA) mitigate this problem. But at high speeds delay from the DWA block becomes significant. This delay has to be accommodated by appropriately delaying the DAC clock, leading to increase in ELD in the loop.

CHAPTER 3

$\Delta\Sigma$ ADC Architecture

3.1 Architecture

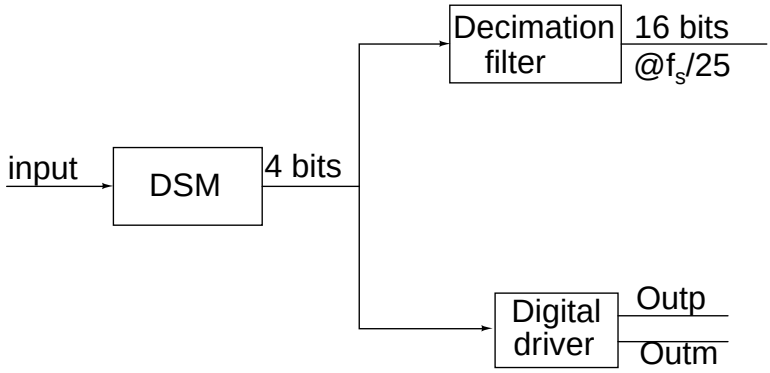


Figure 3.1: Block diagram of ADC

Figure 3.1 shows the complete top level block diagram of the $\Delta\Sigma$ analog to digital converter after combining the decimation filter to the $\Delta\Sigma$ modulator which has been tested as a part of this thesis work. 16 bits are taken as the output of the analog to digital converter. Along with the decimator output of the ADC, there is a provision to collect the output differential signal through a digital driver circuit, which can be viewed using an oscilloscope. The digital driver circuit is explained in the next section.

3.2 Digital driver[1]

A unit cell differential pair current steering DAC cell is as shown in Figure 3.2, which consists of 600 μA cascoded current source, steered using the NMOS differential pair of current switches. The current value is chosen to drive proper current to the load. Since

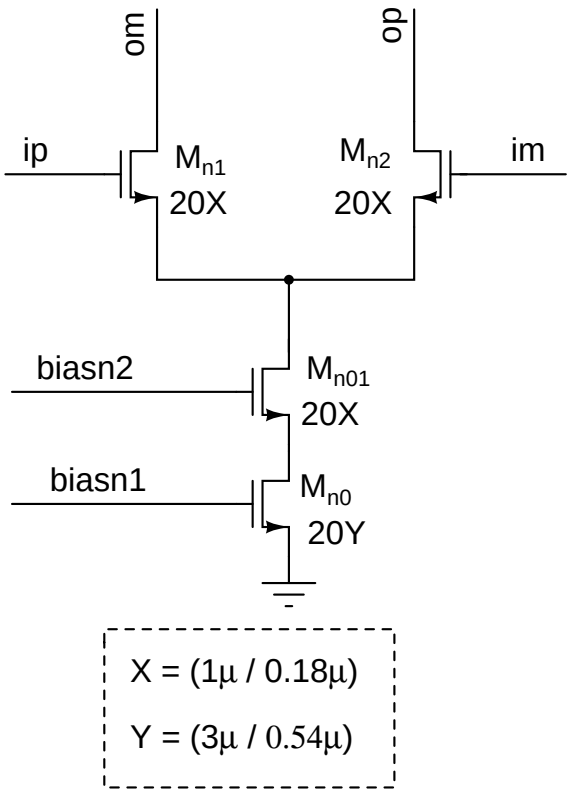


Figure 3.2: Schematic of unit DAC cell[1]

we are using rail to rail drives, the switch transistors may go into triode region, there by losing the advantage of cascode transistor for the tail current source. The switch Transistor sizes are chosen larger to make the overdrive voltage smaller so that, the switches act in a better way. Because of the larger sizes of the transistors the tail node capacitance increases, which increases the current in the capacitor due to variations in the tail node voltage. So the cascode transistor is chosen to be of smaller size, which reduces the parasitic capacitance. The cascode transistor protects the tail current from any voltage variation and also reduces modulation of current source by the output voltage. The bias voltages are generated using a low voltage cascode current mirror as shown in Figure 3.3.

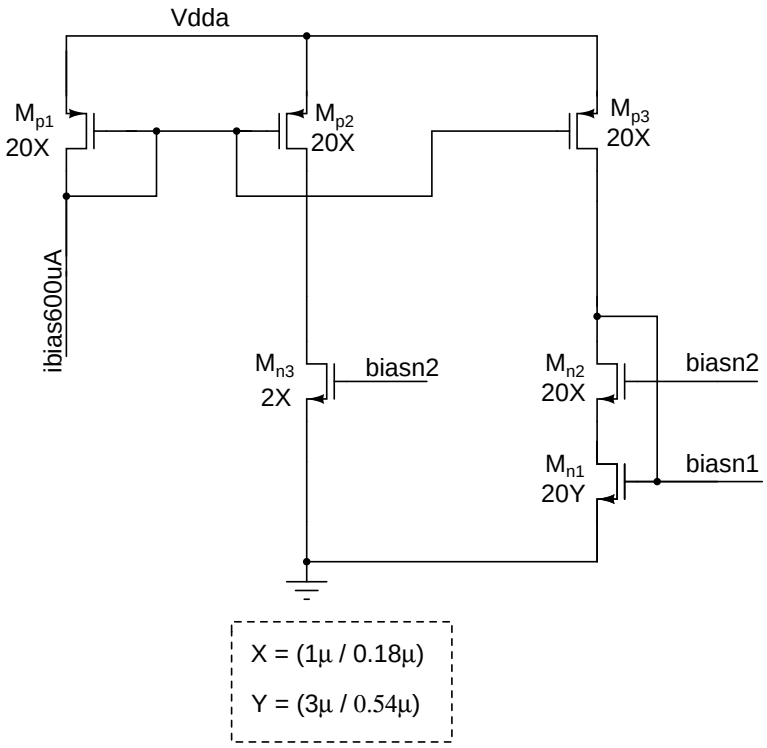


Figure 3.3: Bias generation circuit for DAC cells[1]

CHAPTER 4

Test Board and Measurement Results

4.1 Test Chip

The pin allocation of the test chip is shown in the Figure 4.1. It is in a Quad Flat No leads (QFN) package with 64 pins. Out of the 64 pins, 8 pins are not used. Table 4.1 shows the description of each pin.

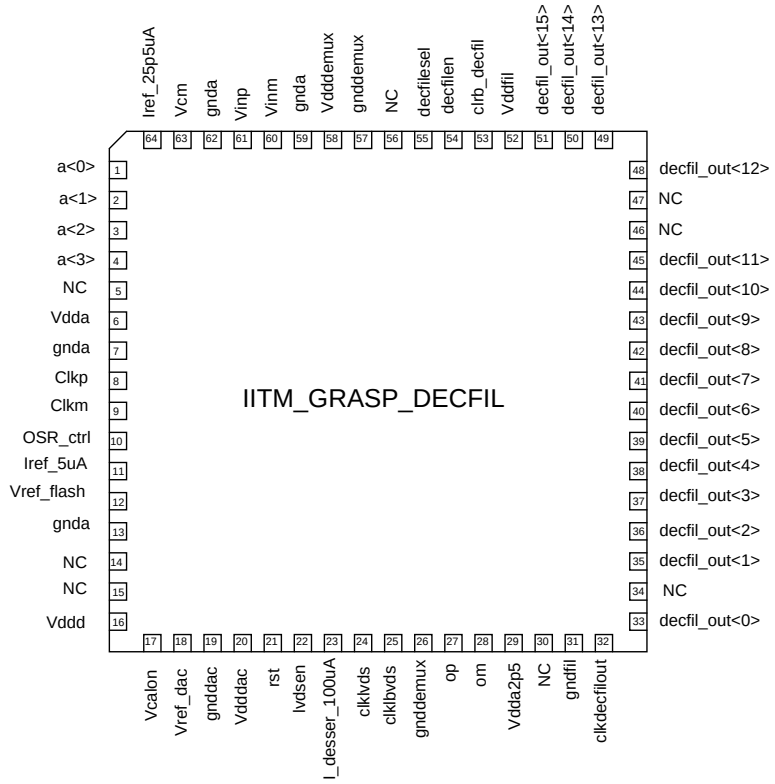


Figure 4.1: Pin details of the chip

Table 4.1: Pin details of the chip

Pin No.	Pin Name	Description
1	a0	Capacitor tuning bit
2	a1	Capacitor tuning bit
3	a2	Capacitor tuning bit
4	a4	Capacitor tuning bit
5	NC	No Connection
6	Vdda	1.8 V supply voltage for the loop filter and biasing
7	Gnda	Ground
8	Clkp	Differential input clock
9	Clkm	Differential input clock
10	OSR_ctrl	Control to chose between OSR =25 (low), OSR =10 (high)
11	Iref_5uA	Reference current source 5 μA(sinking current)
12	Vref_flash	Control for changing input swing of flash ADC.Nominal value = 0.9 V
13	Gnda	Ground
14	NC	No Connection
15	NC	No Connection
16	Vddd	1.8 V supply voltage for the flash ADC
17	Vcalon	Control for making calibration on (high) and off (low)
18	Vref_dac	Control for DAC unit cell current. Nominal value =0.9 V
19	Gnddac	Ground
20	Vdddac	1.8 V supply voltage for the DAC
21	rst	Reset the digital calibration logic (Reset when high)
22	lvdsen	Control for lvds buffers to enable (high) and disable (low)
23	I_desser_100uA	Reference current source 100 μA(source current)
24	Clklvds	Differential output LVDS clock
25	Clkblvds	Differential output LVDS clock
26	Gnddemux	Ground
27	Op	Differential output signal from Digital driver
28	Om	Differential output signal from Digital driver
29	Vdda2p5	2.5 V supply voltage
30	NC	No Connection
31	Gndfil	Ground
32	Clkdecfilout	Output clock of Decimation filter

Pin No.	Pin Name	Description
33	decfil_out<0>	Output data of Decimation filter
34	NC	No Connection
35	decfil_out<1>	Output data of Decimation filter
36	decfil_out<2>	Output data of Decimation filter
37	decfil_out<3>	Output data of Decimation filter
38	decfil_out<4>	Output data of Decimation filter
39	decfil_out<5>	Output data of Decimation filter
40	decfil_out<6>	Output data of Decimation filter
41	decfil_out<7>	Output data of Decimation filter
42	decfil_out<8>	Output data of Decimation filter
43	decfil_out<9>	Output data of Decimation filter
44	decfil_out<10>	Output data of Decimation filter
45	decfil_out<11>	Output data of Decimation filter
46	NC	No Connection
47	NC	No Connection
48	decfil_out<12>	Output data of Decimation filter
49	decfil_out<13>	Output data of Decimation filter
50	decfil_out<14>	Output data of Decimation filter
51	decfil_out<15>	Output data of Decimation filter
52	Vddfil	1.8 V supply voltage for the Decimation filter
53	clrb_decfil	Reset decimation filter(Reset when low)
54	decfilen	Control for Decimation filter to enable (high) and disable (low)
55	decfilsel	Control signal to selct one of the two clocks for Decimation filter
56	NC	No Connection
57	Gnddemux	Ground
58	Vdddemux	1.8 V supply voltage
59	Gnda	Ground
60	Vinm	Differential input signal
61	Vinp	Differential input signal
62	Gnda	Ground
63	Vcm	Common mode reference voltage of 0.9 V
64	Iref_25p5uA	Reference current source of value 25.5 μA(source current)

4.2 Test Board

A PCB was designed for testing the chip in ORCAD. It is four layered with layers namely : Top, Ground, Power and Bottom. Out of these Top and Bottom layers are used for routing and second layer is ground plane and third is power plane. It is manufactured on a copper plate FR-4 dielectric and thickness of board is 1.6mm . The dimensions of the board are 15.55 cmX12.1 cm. The snapshot of the test board with labels is shown in the Figure 4.2.

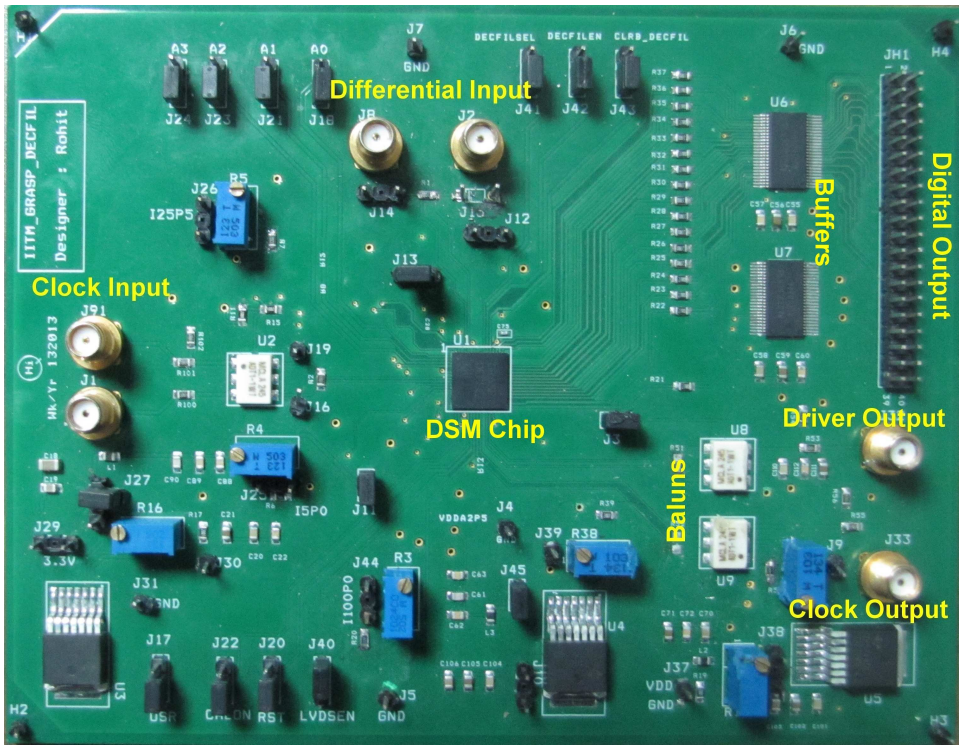


Figure 4.2: Board used for the testing

Power Supply

Board needs different kinds of power supplies. Each of these supplies is regulated through TPS74401 regulator. Regulator output is then filtered using parallel bank of surface mount capacitors and inductor. Ferrite bead inductors are used which filter high frequency supply noise by converting it into a tiny amount of heat. The various supplies

to the chip are connected to this filtered output with the help of jumpers at appropriate places and decoupling capacitors near chip pins.

A solid ground plane and a ground copper pour is used on top and bottom layers of PCB. This helps in reducing crosstalk between two adjacent traces.

Power plane is split to supply different voltages in various regions of the board. This is used to calculate power dissipation in different blocks within the chip by measuring current.

Current References

Chip needs three current sources Iref_ $5\,\mu$A, Iref_ $25\mathrm{p}5\,\mu$A and I_desser_ $100\,\mu$A. Resistive networks consisting of potentiometer and fixed resistor is used for realizing the current references.The values of these resistors are chosen by simulating for different process corners

Digital Buffers

The 16-bit digital output of decimator and output clock of decimator is passed through buffers(SN74AUC16244) and its output is connected to 20-pin connector.

Baluns

An RF transformer (Mini-Circuits ADT1-1WT) is used to convert the differential signals into a single ended and vice-versa.

Control Signals and Other Circuitry

Chip needs different kinds of control signals as listed in Table 4.1. These are given with the help of jumpers. SMA connectors are used for differential clock inputs and signal inputs , driver output and LVDS clock output.

4.3 Test Setup

Figure 4.3 shows the test setup arrangement. Agilent 33250A serves as a signal which drives an input tone to a passband filter(BPS 0500-B). The filter suppresses the harmonics and the wide-band noise of the signal source. Differential input signal to the chip is provided with the help of a balun transformer(North-Hills 100 KHz-20 MHz balun). Balun transformer converts this spectrally purified tone into a differential signal. The clock signal is generated by another signal source (Agilent E4422B), that generates low-jitter sine wave at 800 MHz.

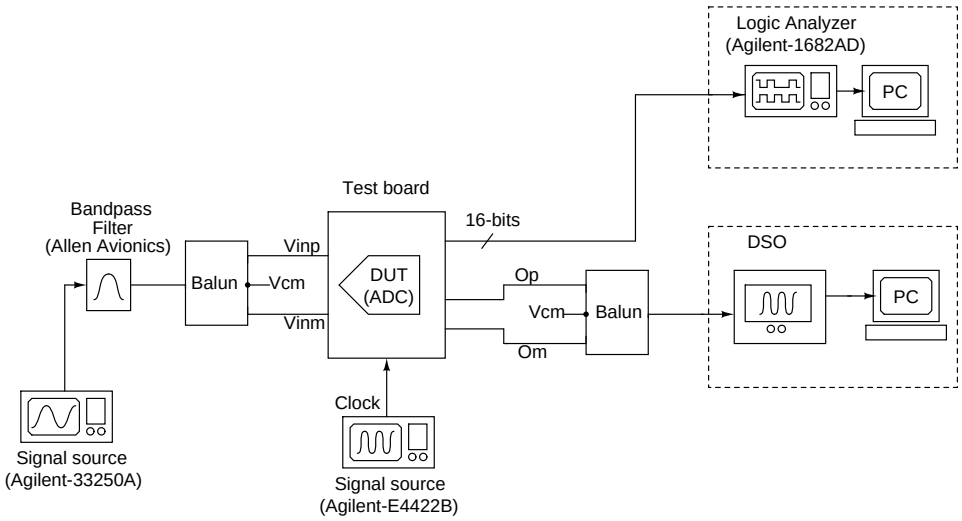


Figure 4.3: Test setup

Again, as chip needs differential clock, RF transformer (Mini-Circuits ADT1-1WT) is used to convert this clock to differential clock. The captured data is transferred to a PC for post-processing. Figure 4.4 shows a snapshot of the test setup.

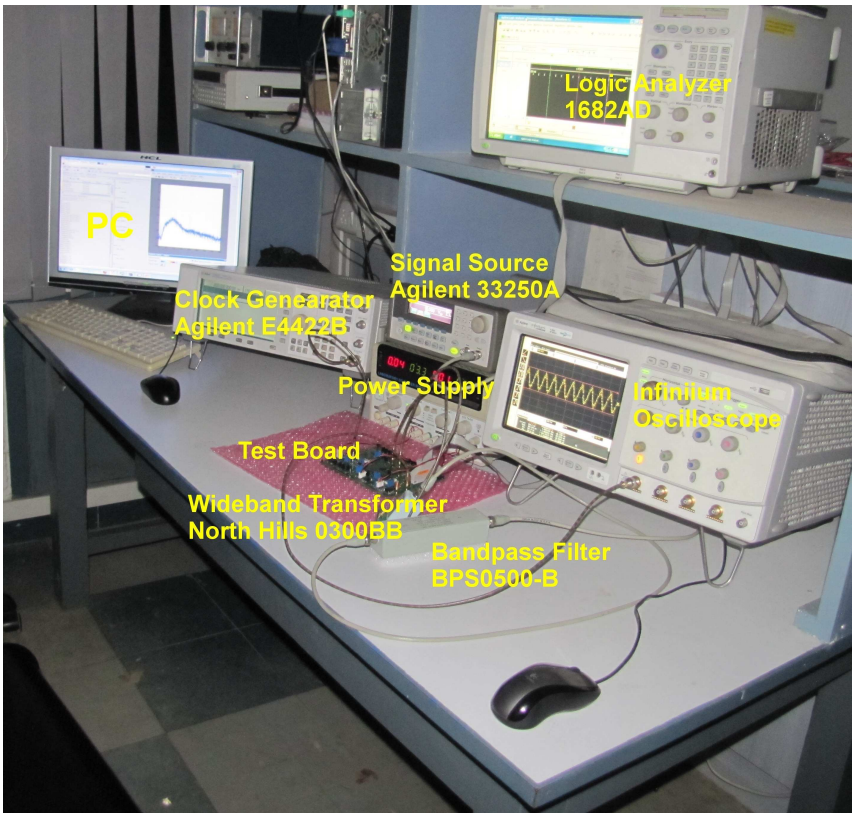


Figure 4.4: Snapshot of test setup

4.4 Measurement Results

The total measured power consumption by chip is $82.07mW$. Table 4.2 shows the power distribution in each block inside the chip.

Idle channel response of the modulator for different sampling rates and their in-band noise values are as shown in figures 4.5 to 4.8. It has tones at $f_s/4$ due to the input reference subtractor used in the flash, which is operating at $f_s/4$.

Table 4.2: Power distribution

Module	Power (mW)
Modulator	48.6
Decimation Filter	8.1
Digital Driver	25.37
Total	82.07

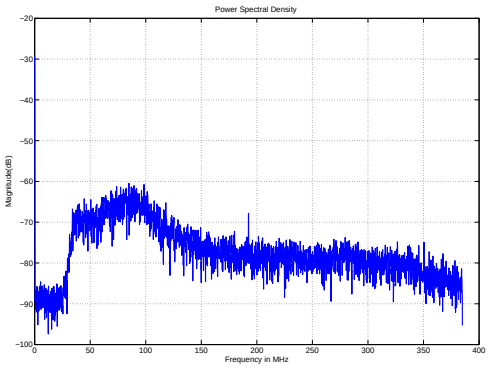


Figure 4.5: $f_s = 770\,MHz$, In-band noise = -67.55dB

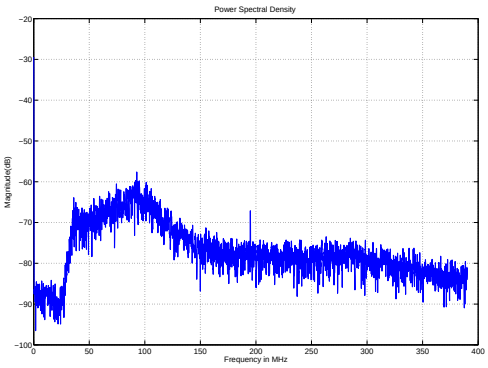


Figure 4.6: $f_s = 780\,MHz$, In-band noise = -67.45dB

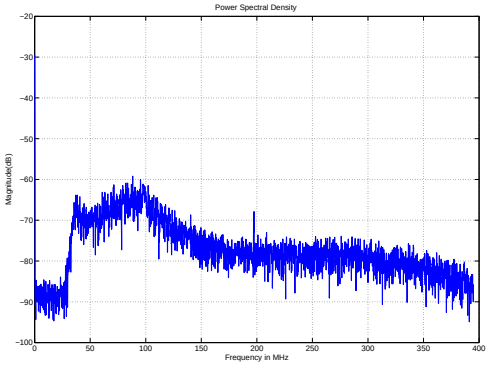


Figure 4.7: $f_s = 790\,MHz$, In-band noise = -67.08dB

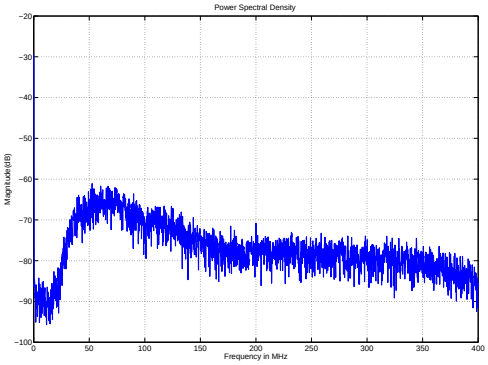


Figure 4.8: $f_s = 800\,MHz$, In-band noise = -67.01dB

Spectrum at the output of digital driver for an input of 5MHz is shown in Figure 4.9.

There is significant reduction in the distortion at the output due to DAC calibration scheme as compared to a case with calibration turned off the plots are as shown in Figure 4.10.

The plot of SQNR for different input amplitudes is shown in Figure 4.11. The measured dynamic range is 44 dB for OSR of 25.

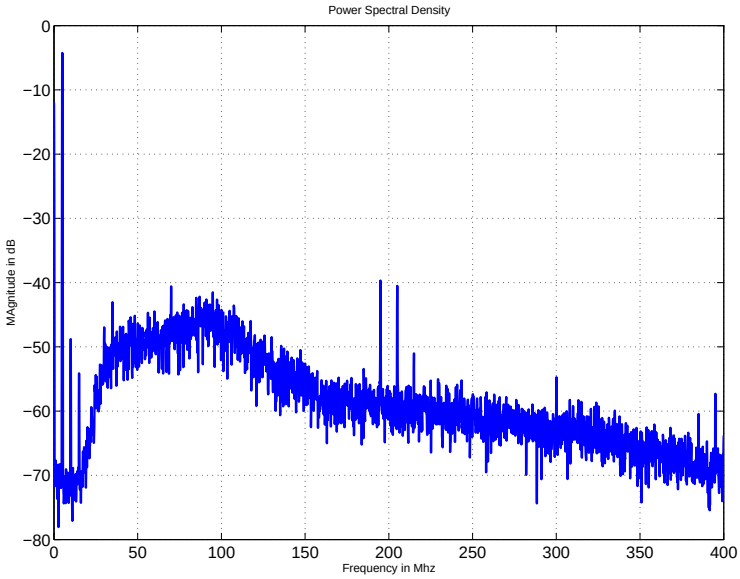


Figure 4.9: Output PSD for OSR of 25 and input of 5 MHz

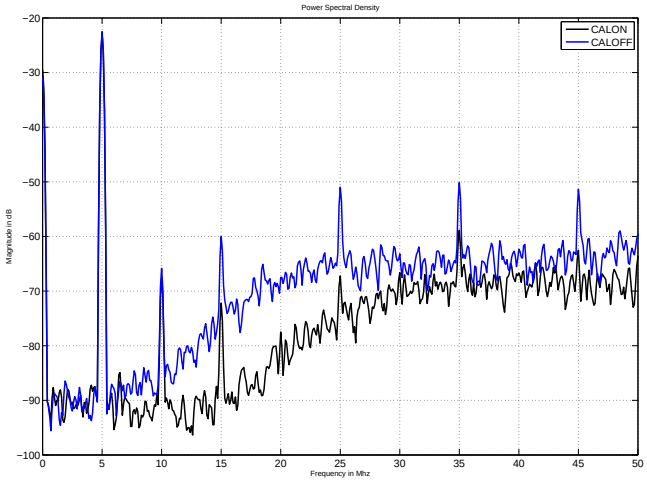


Figure 4.10: PSD with and without calibration

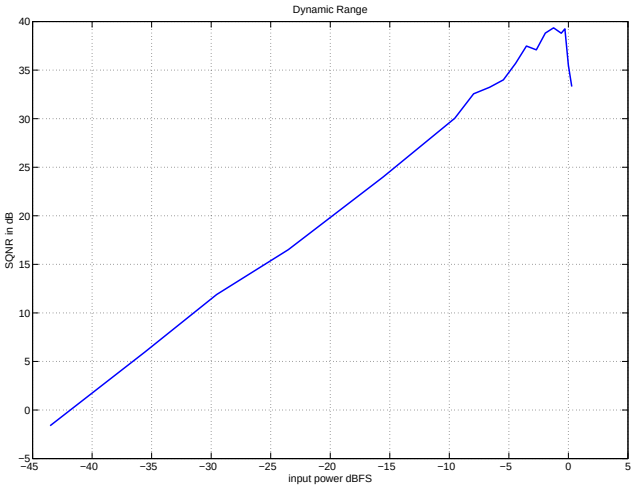


Figure 4.11: SQNR vs input amplitude for OSR= 25 and input of 5MHz

4.5 Problems Faced During Testing

1. Decimation filter was not working for sampling frequencies greater than 250MHz.
2. Swing at the driver output is very less.

CHAPTER 5

Conclusions and Future Work

5.1 Conclusions

The high speed CT $\Delta\Sigma$ modulator was tested to work at 800 MHz and the tested chip had a dynamic range of 44 dB and SNR of 40 dB for a bandwidth of 16 MHz. The total power consumed by the chip is measured as 82.07 mW.

5.2 Future Work

PCB needs to be modified for incorporating a socket and performance of all other chips needs to be tested. Also, the reasons for the problems encountered during course of testing need to be found out.

APPENDIX A

PCB Schematic and Layout

The schematic of the board is split into five portions. The schematic of the board with the Chip is shown in Fig. A.1. The schematic of the board with control Signals and reference voltages and currents is shown in Fig. A.2. The schematic of the board with digital buffers is shown in Fig. A.3. The schematic of the board with the input and output signals is shown in Fig. A.4. The schematic of the board with the power supply part is shown in Fig. A.5 and Fig. A.6 .

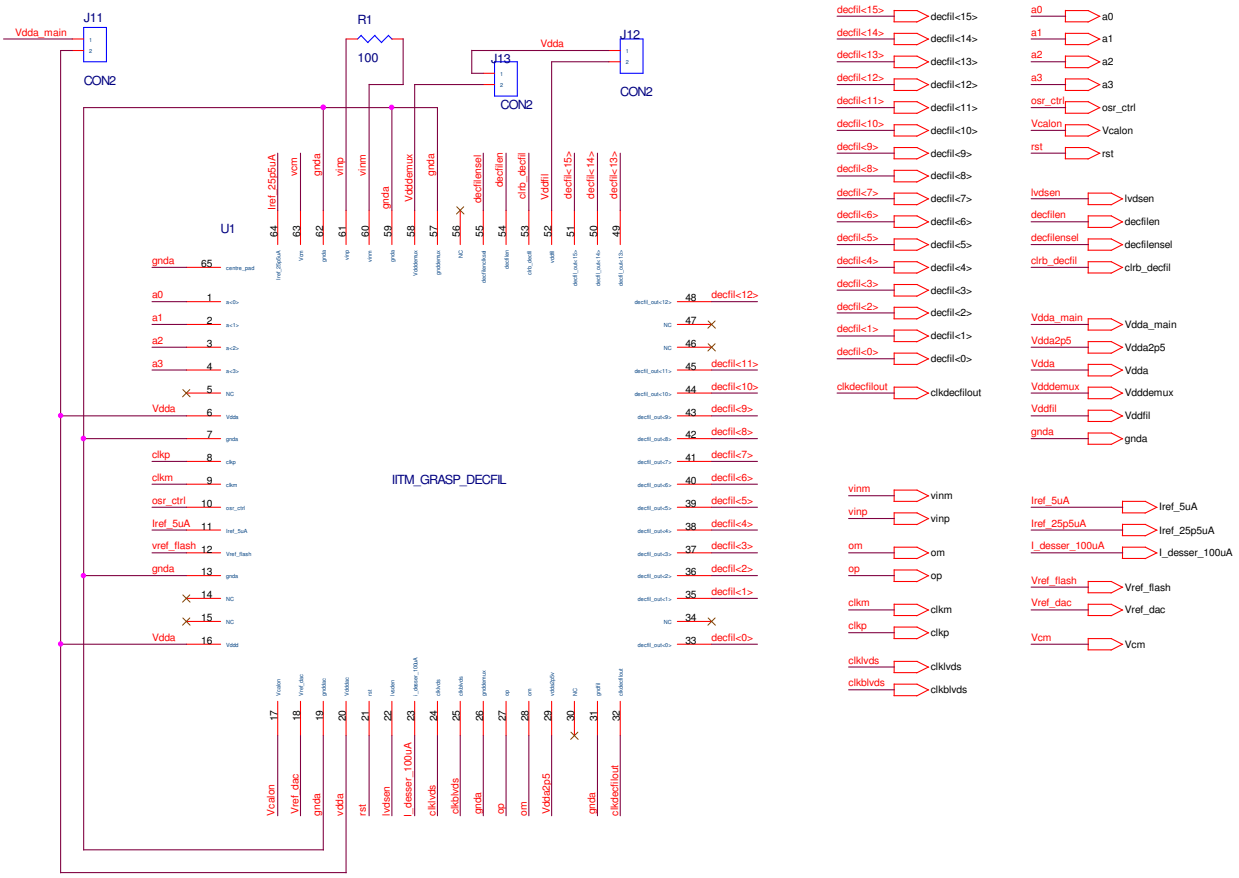


Figure A.1: Chip.

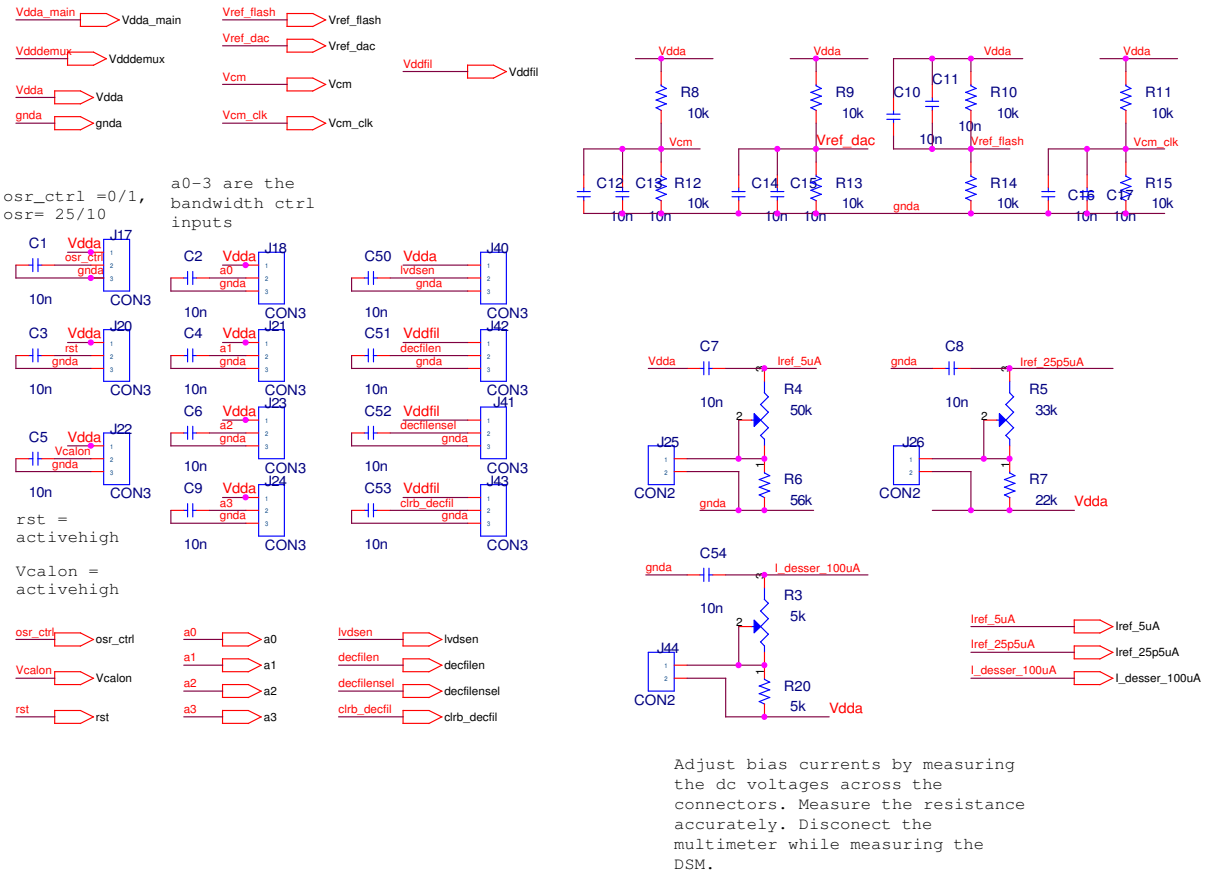


Figure A.2: Control Signals and References.

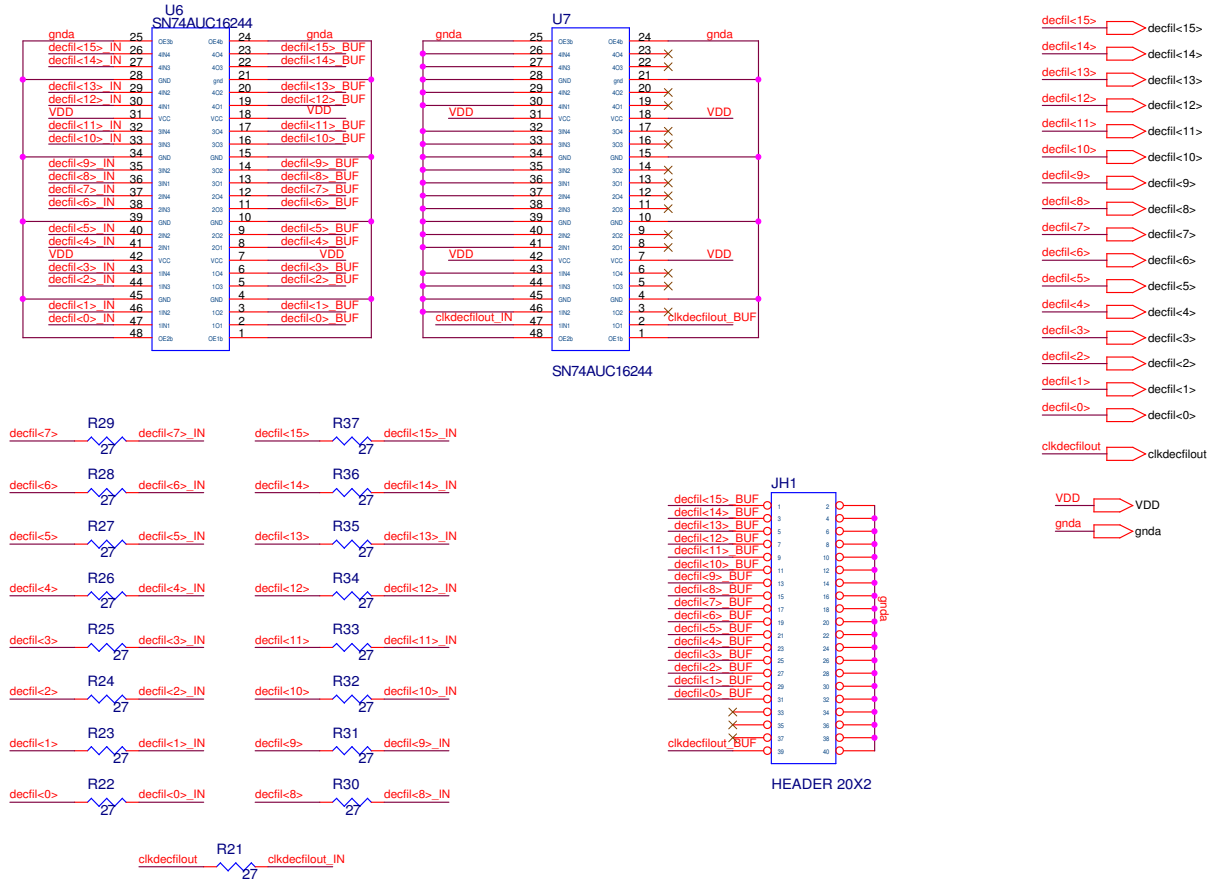


Figure A.3: Digital Buffers.

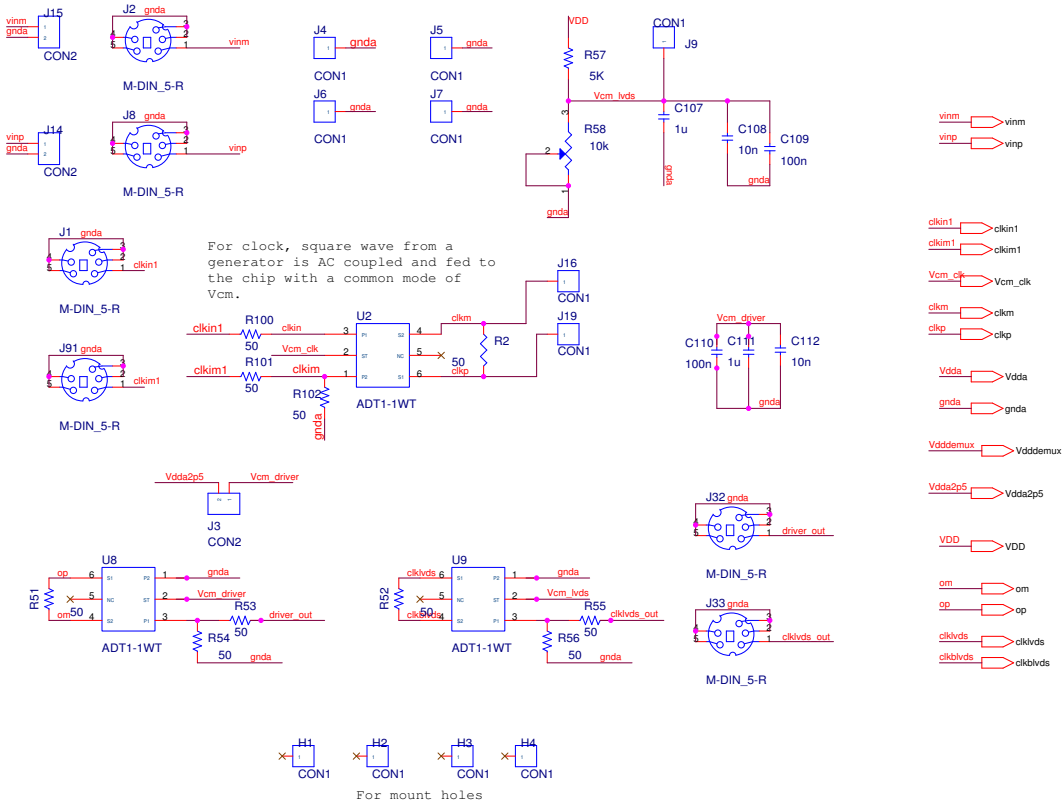
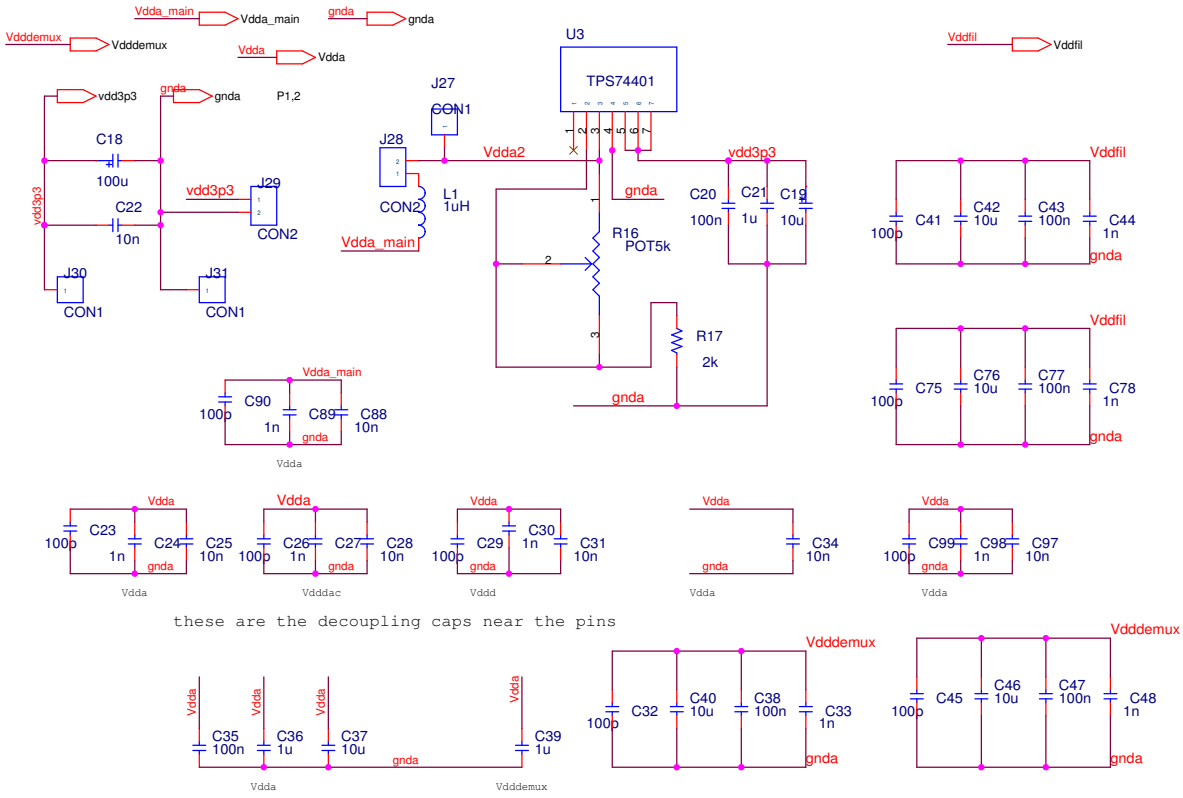


Figure A.4: Input and Output Signals.



TPS74401 is a low dropout linear regulator capable of supplying 3A at 3.3 V (max).

Each output is set to 0.8(1+R1/R2)

Figure A.5: Power Supply.

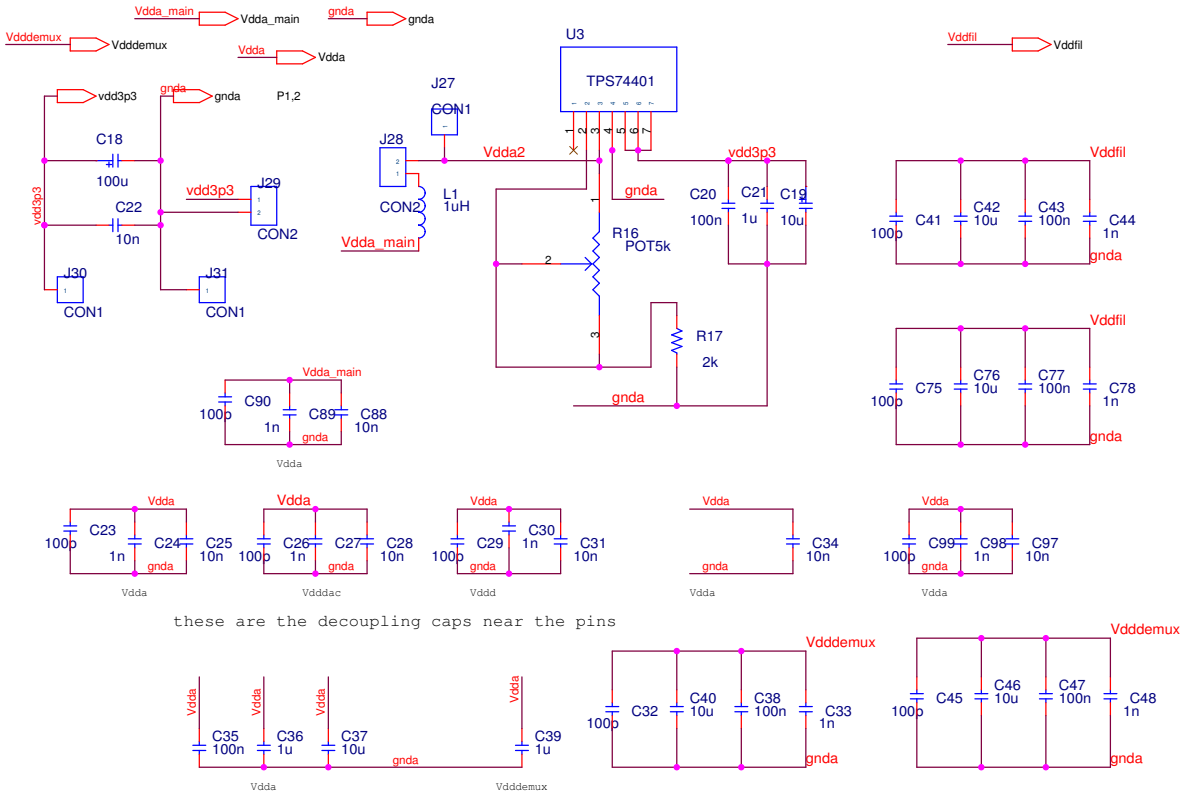


Figure A.6: Power Supply Continued.

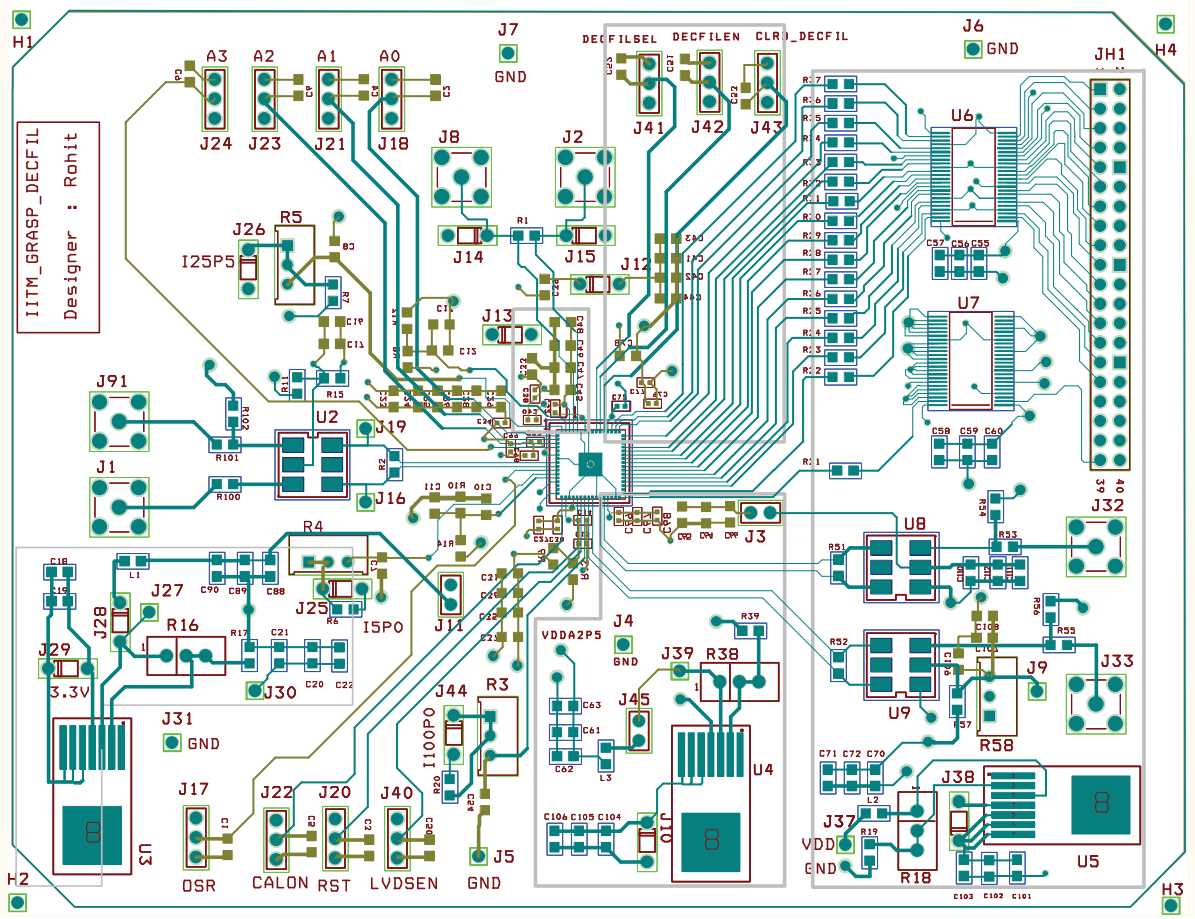


Figure A.7: PCB Layout.

REFERENCES

[1] **Hussainvali, S.**, *Design of a Decimation Filter and Testing of a High Speed Delta Sigma Modulator*. "IIT Madras", 2012.

[2] **Schreier, R.** and **G. Temes**, *Understanding Delta-Sigma Data Converters*. IEEE press, Piscataway NJ, 2005.

[3] **Singh, V.**, *Design of a High Speed High Resolution Continuous-Time Delta Sigma Modulator*. "IIT Madras", 2010.

[4] **Singh, V.**, **N. Krishnapura**, and **S. Pavan** (2010). Compensating for quantizer delay in excess of one clock cycle in continuous-time delta sigma modulators. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, **57**(9), 676–680. ISSN 1549-7747.