Testing and Characterization a Time to Digital Converter

A Project Report

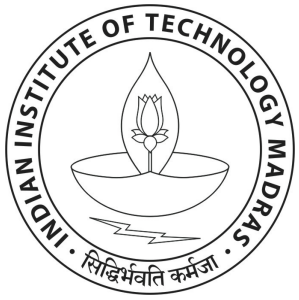
submitted by

RAVITEJA REPAKA

in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2013

THESIS CERTIFICATE

This is to certify that the thesis titled **Testing and Characterization of a Time to Digital Converter**, submitted by **Raviteja Repaka**,to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology** , is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura

Advisor,

Assistant Professor,

Dept. of Electrical Engineering,

IIT-Madras, 600 036

Place: Chennai

Date: 7th June 2013

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere thanks to my project guide Dr. Nagendra Krishnapura for his invaluable guidance and encouragement through out my project work. He is the one who introduced me to real analog design environment. The classes taken by him and the way of his approach to solve the problems ever inspiring for me. Actually this is the reason for me to take the project in analog domain under him. And I would like to express my deepest gratitude for his patience to clarify my silly mistakes and silly doubts and for his understanding of my very bad health.

Even a small span of discussion with him makes a big difference in understanding the things. Nagendra sir is always cheerful, makes the difficult things into very easy things by his innovative ideas. Really I am very proud to work under him.

I would like to express my special thanks to Amrith, Ankesh, Debasish and Radha for helping me continouously during the course of my work. Without their help it would have been difficult to take this project to this extent. And I would also like to thank Vijay Madiwalar for making me familiar with UNIX commands. When ever I face any problem regarding with my system, he is the first person whom I approach to sort it out. And also I would like to thank my senior Praveen Kumar for clarifying my doubts regarding the design and for teaching cadence to me. I really impressed by his systematic way of thinking and for his coolness.

I would like to thank all of my friends in DSDL Lab and testing Lab for their support and friendly atmosphere in lab. I would also like to thank Mrs.Janaki for

her help and support.

I would like to express my sincere and humble gratitude to all of my room mates who took care of me when my health is not good and gave their constant encouragement in completing my project. I would like to say my special thanks to one of my room mate Venkatesh for always being with me in all the situations and for giving me mental strength to do my project even in my bad health.

There are no words to describe my happiness for my parents constant support and their enocuragement. Thinking of their love and care for me, makes me much more joyful. I am always grateful to the Lord for giving me a birth in such a wonderful family.

Finally I would like to dedicate this thesis to my beloved lordships and the divine couple shri shri Radha Krishna for their mercy upon this insincere child.

ABSTRACT

This project involves the testing and validating the Time to Digital Converter chip. This system uses a single clock frequency and chip is designed for 250MHz clock frequency.

The architecture chosen for designing the system was composite coarse-fine architecture. The course TDC has a resolution of 4 ns and a range of 131 μs. The fine TDC has a resolution of 125 ps and a range of 4 ns. A digital backend was designed to combine course and fine TDC outputs to give 20 bit output. This chip includes the selftest block to generate start, stop and reset signals for testing the TDC internally.

To test this chip a PCB board was designed. And the functionality of the chip is verified by giving internally genearated start and stop signals. Baluns are used to convert output start and stop LVDS signals into single ended signals. And the delay between these two signals is measured through oscilloscope. And 20 bit digital output has taken through logic analyzer. It is observed that this 20 bit output almost matches with ideal values. But still there are some issues with the functionality of the chip which needs to be sorted out.

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ABBREVIATIONS

TDC	Time-to-Digital Converter
INO	Indian-based Neutrino Observatory
PVT	Process-Voltage-Temperature
DLL	Delay Locked Loop
VCDU	Voltage Controlled Delay Unit
PFD	Phase Frequency Detector
DNL	Differential Non Linearity
INL	Integral Non Linearity
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
UMC	United Microelectronics Corporation
LVDS	Low Voltage Differential Signalling

CHAPTER 1

Introduction

Neutrino physics experiments in the last several decades have provided many new and significant results(1). Many highly multi-disciplinary research groups are working on neutrino detection and related research. The India-based Neutrino Observa- tory (INO) is one such particle physics research project which primarily aims to study atmospheric neutrinos(1). The neutrino detector of INO consists of a massive magnetized iron calorimeter (3). The primary detection mechanism is via detection of muons produced in charged neutrino interactions. The detector comprises of layers of iron sheets interleaved with planar active detector elements. Each metal sheet contains a mesh of 32 by 32 readout channels. This helps us to determine the (x, y) co-ordinates of the neutrino hit on a given metal sheet. The index of the metal sheet will give us the z coordinate of the neutrino hit. We also need to determine the timing of the neutrino hit with respect to a reference start. Upon determining all these, we can know the (x, y, z, t) profile of the neutrino trajectory. For this, we need to be able to detect the hit on a given plate and process it accurately.

Avalanche mechanisms in the detector array give rise to a voltage spike which needs to be processed using high speed circuits. Fast and high gain amplifier along with latching circuitry is required to generate a digital signal which goes high when a neutrino hit is detected. The time of the neutrino hit also has to be measured with respect to a reference start. The system must be robust and should be low power because high temperatures in the detector render cooling mechanisms less efficient. The TDC chip designed is targeted to be of use in these detectors. The brief design of the system is described below.

1.1 Designed system (1)

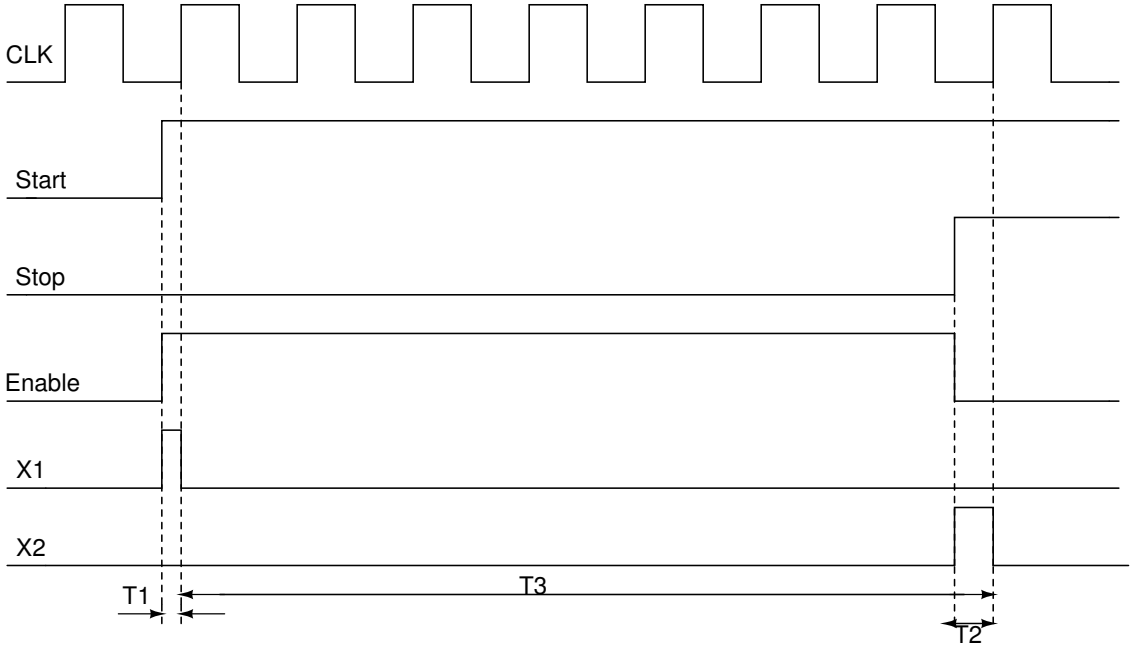


Figure 1.1: Basic operation of a TDC system.

The architecture chosen for designing the TDC is a composite coarse-fine architecture. The main idea is to measure the time as a sum of two parts: one measured by a coarse counter which gives a very high range but low resolution and the remaining part measured using a high resolution method which has a lower range. Consider the two inputs as shown in Fig. 1.1. Let the time interval between the two inputs be ΔT, the time to be digitized. The time interval ΔT can be split into three parts T1 , T2 and T3 w.r.t a system clock as shown in the figure. T1 is the time between the start signal and the next rising edge of the clock. Similarly T2 is the time between the stop signal and the rising edge immediately after it. T3 is time between the two rising edges of the clock mentioned above. Clearly, $T1, T2 < T_{clk}$ and the resolution of coarse TDC cannot be less than T_{clk}. Hence $T1, T2$ have to be measured by a fine TDC whereas $T3 > T_{clk}$ and can be arbitrarily large within the range of the TDC. Hence it is measured using a coarse TDC. Also we have, $\Delta\mathrm{T} = T3 + T1 - T2$.

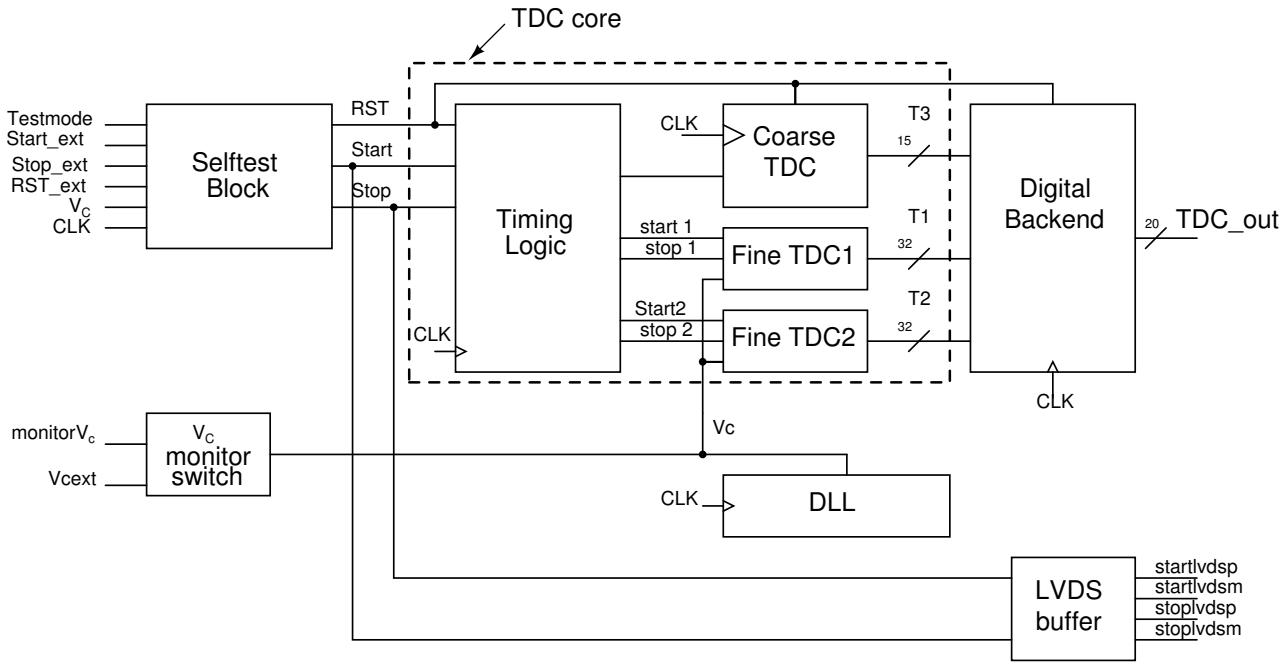


Figure 1.2: Block Diagram of TDC system(1).

The block diagram of the complete design is shown in Fig. 1.2. A timing logic block extracts the signals corresponding to the intervals $T1$ and $T2$ and feeds them to the fine TDCs. It feeds the coarse TDC with a signal corresponding to the interval $T3$. The fine resolution measurement of $T1$ and $T2$ is performed by the fine TDC and $T3$ is measured by the coarse TDC. The thermometer coded output of the fine TDC is converted to binary in the digital back end and ΔT is calculated from $T1$, $T2$ and $T3$. $T1$ and $T2$ are measured with 5 bit resolution and $T3$ is measured with 15 bit resolution. A Delay locked loop (DLL) stabilises the Voltage controlled delay units (VCDUs) in the fine TDC against PVT variations. A built-in selftest block generates start, stop and reset signals for TDC. A switch is used to tap the control voltage of the DLL. LVDS buffers are used to tap the start and stop signal inputs of the core TDC.

1.2 Organisation

Chapter 2 explains the existing TDC chip architecture.

Chapter 3 deals with PCB design and measurement results.

Chapter 4 concludes the thesis and mentions the work to be done.

CHAPTER 2

TDC Chip Architecture

2.1 Built-in selftest(1)

2.1.1 Implementation

The testing of TDC chip needs high frequency equipments to generate start and stop signals. A selftest block included in the chip eliminates this need by internally generating the start, stop and reset signals required to test the TDC. Fig. 2.1 shows the functional diagram of the selftest block.

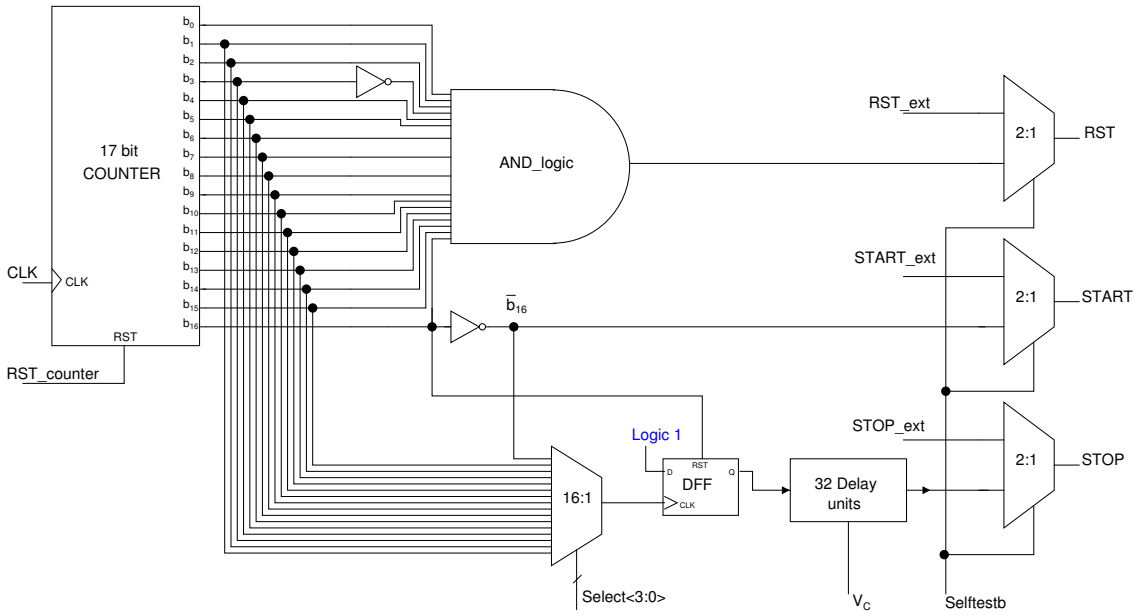


Figure 2.1: Built-in Selftest.

It consists of a 17 bit counter, the output of which is denoted by b. The i^{th} bit b_i of the counter output, toggles with a period of $2^{(i+1)}T_{clk}$. b_{16bar} is used as the internal start signal. By choosing the value of *select* input, various delays for stop signal can be chosen. A flip flop placed before the delay line ensures that

the internal stop signal goes high only once in each cycle of start signal. This is clearly explained in Fig. 2.2. For fine delays in stop signal, a voltage controlled delay line similar to the one used in fine TDC is used.

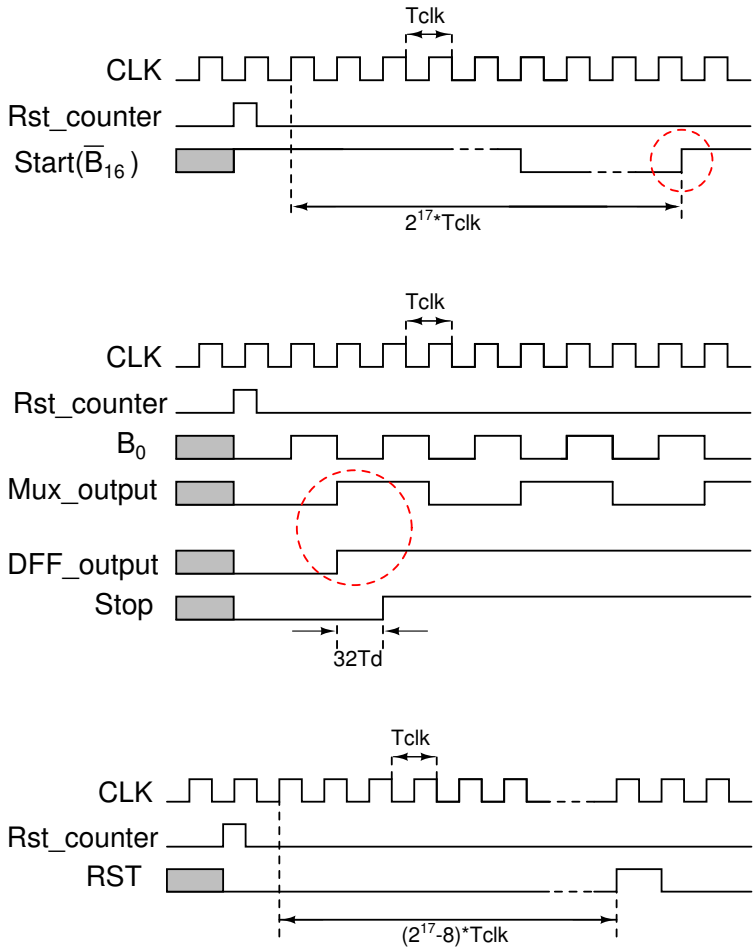


Figure 2.2: Timing diagram for (a) Start signal. (b) Stop signal with select=0 (T_d is the average delay of each delay unit). (c) RST signal

From Fig. 2.2(a), we see that b_{16bar} goes high when the counter is reset. Since the initial state of b_{16bar} is unknown, the first start signal comes only after 2^{17} clock cycles. In Fig. 2.2(b) we see that the output of the flip flop goes high only once in an entire cycle of the counter. If T_d is the average delay of each delay element in the delayline, then the internal stop signal is delayed by $32T_d$ w.r.t flip flop output. A RST signal is generated 8 clock cycles before b_{16bar} goes high in the next cycle. This ensures TDC is properly reset before each cycle of start and stop inputs.

2.2 Fine TDC(2)

The Fine TDC used is a Flash TDC or a single delay line TDC. The delay line architecture (4),(5) is in principle similar to the working of a flash ADC. In a flash ADC, the input voltage is compared to a set of voltages uniformly distributed between the maximum and the minimum voltage. The output thermometer code encodes the input voltage in a digital form. A delay line based TDC works on a similar concept. The input time period is in essence compared to a set of time periods and a thermometer code is generated. Let the time interval between the two signals be T , the time to be digitized. The start signal i.e. the signal which arrives before the other is passed through a delay chain of n delay elements each having a delay Td as shown in Fig. 2.3. So, the output of the i_{th} delay element $(0 \leq i \leq n)$ is delayed by an amount iTd w.r.t the start signal. The D input of each flip flop is connected to stop signal. So the flip flops go high only when stop is high and the delayed start signal clocks the particular flip flop. If the output of the j th element crosses the stop signal for the first time, then

$$(j-1)Td \leq T \leq jTd$$

The output is a thermometer code where the number of 0s in the code represents the number of LSBs in the delay. The delay elements in the simplest implementation can be just a pair of in- verters in series.But in a composite coarse-fine architecture such as this, it is necessary that the range of the fine counter be the same as the resolution of the coarse counter. The range of a simple inverter chain can vary by 60% across the corners, making it infeasible for the coarse-fine architecture to work correctly. So in this this system, a voltage controlled delay unit (VCDU) was used where the control voltages are adjusted so as to give the same delay in spite of process variations. The voltages are tuned by a Delay Locked Loop (DLL) which is locked to a fixed delay.

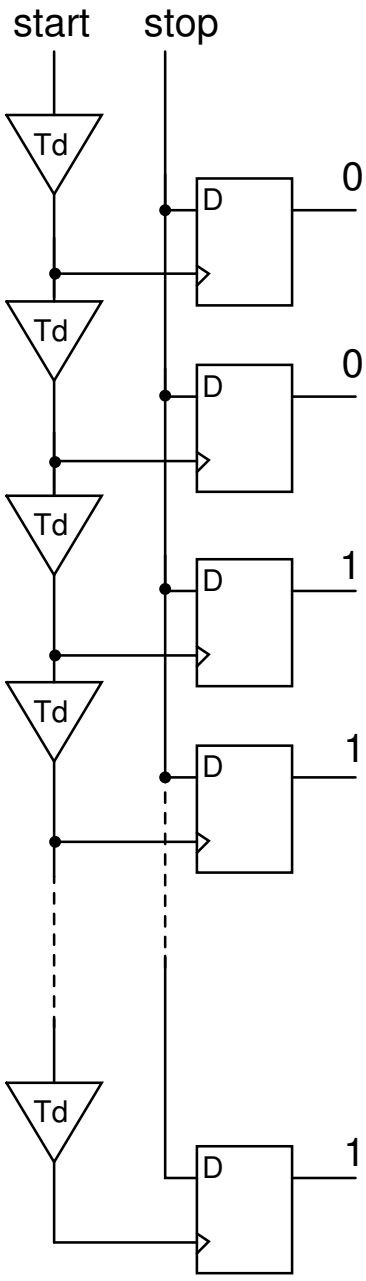


Figure 2.3: Fine TDC.

2.3 Coarse TDC

The coarse TDC is basically a 15 bit digital counter with a clock period of 4 ns. It is enabled with the start signal and disabled with the stop signal. It uses the reference clock running at 250 MHz for its counting.

2.4 Timing logic(1)

The timing logic block extracts the signals which need to be sent to the fine and coarse TDCs. For the coarse TDC, whose implementation essentially involves just a counter, the timing logic block generates an enable signal. This enable signal goes high with start signal and goes low with arrival of the stop signal. The coarse TDC should count the number of clock cycles when this enable is high. This implementation is shown in Fig. 2.4. The timing logic for fine TDC is explained in detail in Fig. 2.5.

T_{Fine} is the time to be measured by fine TDC. For this the interval T_{Fine} between the start/stop signal and the clock has to be extracted into two step signals spaced by the same amount. Three different implementation cases using flip flops are discussed in Fig. 2.5. In case(i) one of the inputs to the fine TDC is the start/stop signal itself. The second input will be the signal X_2 which goes high when clock goes high. But now the spacing between the fine TDC input signals is,

$$T_1 = T_{Fine} + T_{CQ-DFF2}$$

In case(ii) an additional flip flop is used so that now X_1 is given as input to fine TDC in place of start/stop. X_1 is the signal that goes high when start goes high but with a delay of $T_{CQ-DFF1}$. Now the spacing between the fine TDC input

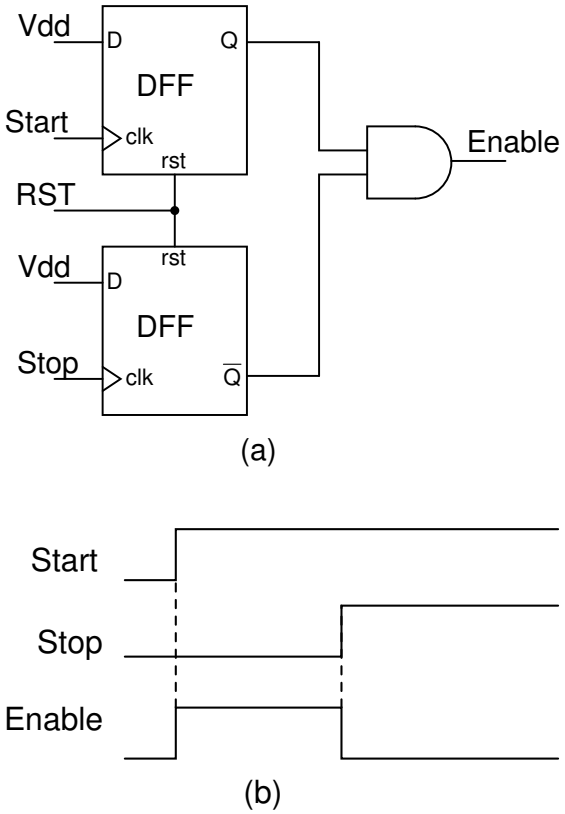
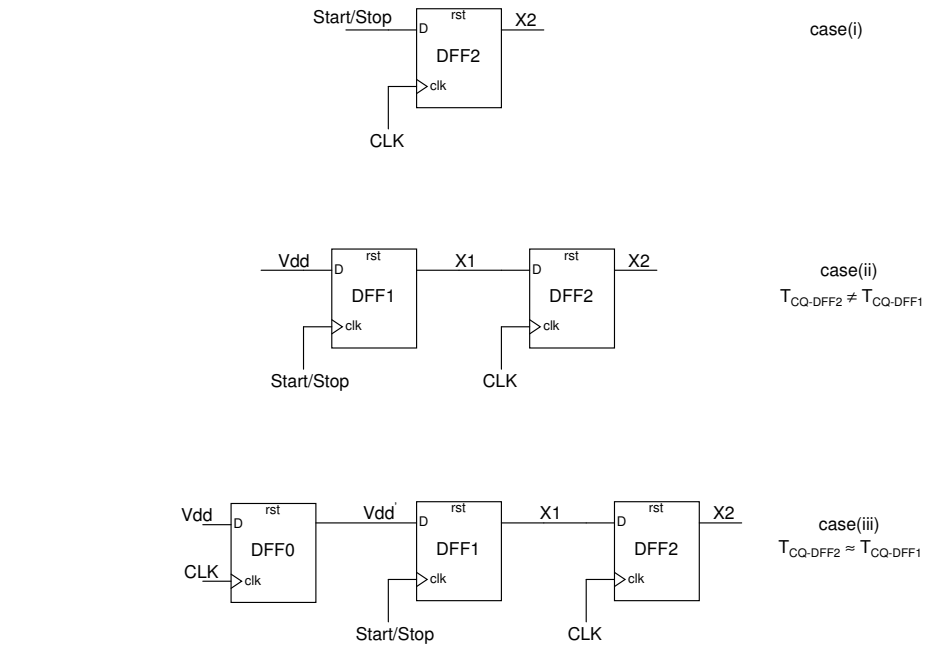
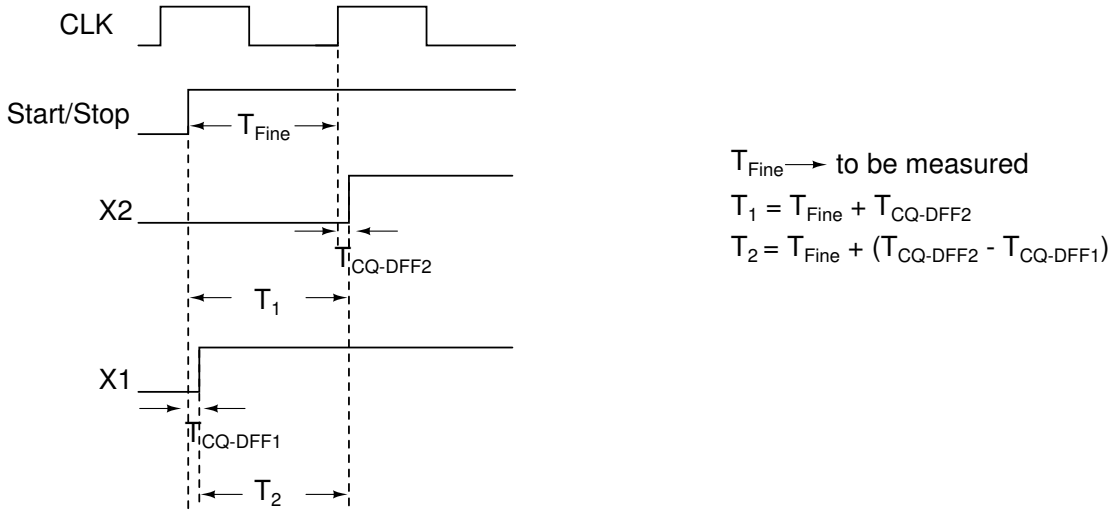


Figure 2.4: Timing logic for coarse TDC. (a) Implementation. (b) Timing diagram.



(a)



(b)

Figure 2.5: Timing logic for fine TDC. (a) Implementation. (b) Timing diagram.($T_{CQ-DFF2}$ and $T_{CQ-DFF1}$ are clock to Q delays of the flip flops)

signals is,

$$T_1 = T_{Fine} + (T_{CQ-DFF2} - T_{CQ-DFF1})$$

The clock-to-Q delays can be made equal by using identical flip flops. (2) mentions that the clock-to-Q delays also depend on the amount of current drawn from the D input of the flip flops. If the D input of DFF1 is connected to the voltage source Vdd , it can draw more current than DFF2 which is connected to the output of DFF1. To rectify this, we connect DFF1 input also to a flip flop output, assuming that the start/stop signals arrive at least one cycle after the reference clock has started. This is shown as case(iii) in Fig. 2.5. The outputs X_1 and X_2 are given to the fine TDC. Since X_1 is loaded by DFF2 as well as the fine TDC whereas X_2 is loaded only by the fine TDC, the delay of flip flops can be different. This can easily be rectified by loading X_2 with a dummy load identical to the input capacitance of DFF2.

2.5 Delay locked loop (DLL)(2)

As mentioned before, we need to ensure that the delay of the VCDU is constant in spite of process variations. For this purpose, we use a DLL which locks the delays of its elements to a fixed value. It does so by altering the control voltages using a feedback loop. If the delay elements in the DLL and the TDC are designed and laid out in an exactly identical manner, the delays in the TDC will also be constant in spite of process variations. Block diagram of a DLL is shown in Fig. 2.6. The working is similar to that of a PLL except that the VCO is replaced by a delay line and no frequency division takes place. The phase frequency detector (PFD) detects the phase difference between the input clock and the feedback signal. Depending on which signal is lagging, the PFD gives UP and DN output signals so as to correct the phase difference. The charge pump changes the control voltage of the delay line appropriately so as to reduce the magnitude of the phase

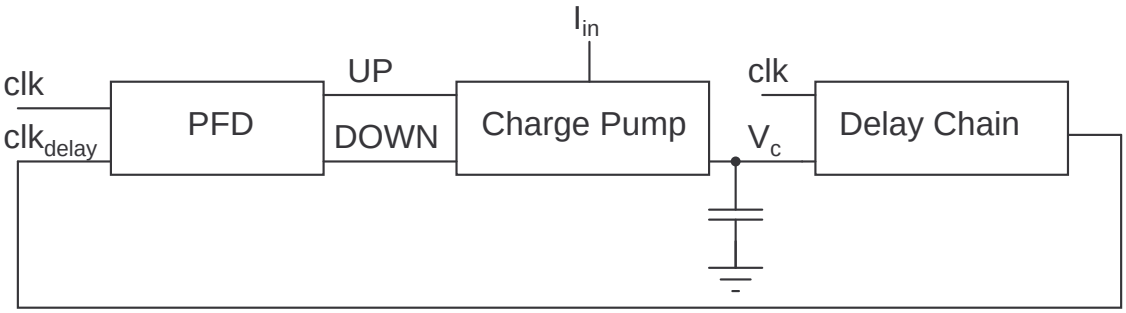


Figure 2.6: Delay Locked Loop(DLL).

difference at the input of the PFD. The DLL used here has 32 delay elements and an input clock of period 4 ns. So, each delay element is locked to 125 ps. This delay is replicated in the delay line of the TDC by using the same control voltage and nominally identical design of delay line. Assuming PVT variations affect the delay line in the DLL and that in the TDC identically, the delays in the TDC will also be 125 ps, independent of PVT variations. The design of each of the components of the DLL is explained in (2).

2.6 Digital backend(1)

The digital back end consists of digital circuitry which combines the output of coarse and fine TDCs to generate the final 20 bit TDC output with a resolution of 125 ps. The output of coarse TDC is 15 bits with a resolution of 4 ns. This is equivalent to 20 bits with a resolution of 125 ps (Because $4\,\text{ns} = 32 \times 125\,\text{ps}$ and multiplication by 32 is same as left shift of a binary number by 5 bits). The output of fine TDC is a 32 bit thermometer code. The number of zeros in this thermometer output gives the the fine delay with a resolution of 125 ps. The thermometer output is converted to a 5 bit binary number by adding the number of zeros. The final output of the backend which is also the output of the overall TDC is calculated as

$$T_{coarse} \times 2^5 + T_{fine2} - T_{fine1}$$

To ensure that the output of fine TDCs are settled, the backend block waits for a 8 clock cycles after stop input is issued(i.e.after the enable signal has gone low). Thus the backend block reads the enable signal, waits for 8 clock cycles after enable goes low and then reads the thermometer outputs. A combinational adder circuit adds the number of zeros in the input thermometer code. The course TDC output is shifted by 5 bits. And the adder/subtracter circuitry adds and subtracts these coarse and fine TDC outputs so as to obtain the final 20 bit output.

2.7 Miscellaneous blocks in the design(1)

This section explains the additional blocks that are there the TDC system. These are blocks that aid in probing some of the intermediate signals, which help in verifying the functionality of the chip during testing.

2.7.1 Switch to monitor or force control voltage V_C

By now we know that the resolution of the fine TDC is totally dependent on the delay of each delay unit, which inturn depend on the control voltage V_C that is set by the DLL. By simulations it is found that the value of control voltage for a delay of 125ps is 551mV. To ensure that the DLL has indeed settled to this value of V_C, a switch shown in Fig. 2.7 has been added. The switch is implemented using a simple transmission gate.

We can see from the figure that, when $monitorVc$ is high the value of control voltage on the DLL can be read at $vcext$ pin. Since the switch is a transmission gate, the $Vcext$ pin can also be used as an input pin wherein the output control

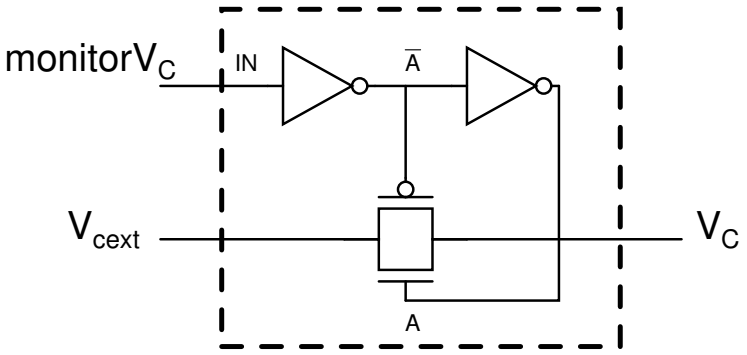


Figure 2.7: Switch to monitor or force V_C.

voltage of DLL can be forced to an arbitrary value so that we can have a control over the resolution of TDC independent of offsets in DLL.

2.7.2 Low voltage differential signalling(LVDS) buffers

During testing we need to ensure that the output of the TDC exactly corresponds to the start/stop signals generated by the internal selftest block. For this, they tap the start and stop signals generated by selftest block and output them as differential signals of low output swings. The design of this is explained in (1).

CHAPTER 3

TDC Chip Measurements

3.1 Pin Description

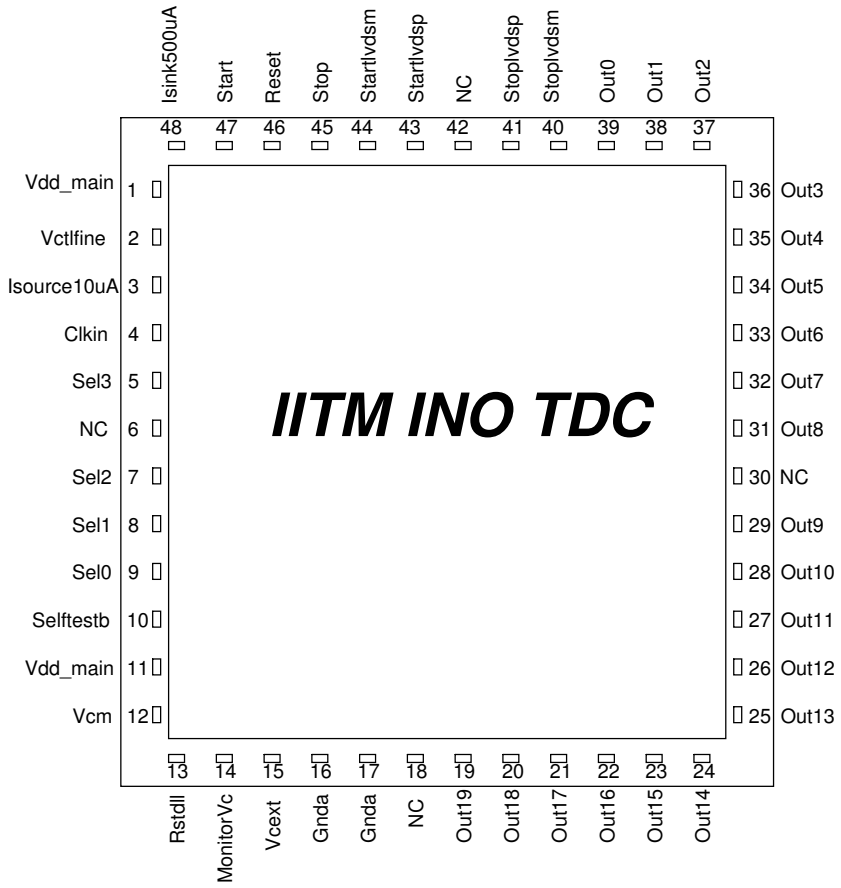


Figure 3.1: Pin Description of the chip

The pin arrangement of the chip is as shown in Fig. 3.1.

Table 3.1: Pin details of the chip

Pin No.	Pin Name	Description
1	Vdd_main	Power supply to chip
2	Vctlfine	Control voltage for VCDU, which varies the arrival time of stop signal generated by Selftest block
3	Isource10uA	current source for charge pump circuit used in DLL
4	Clkin	Input clock signal
5	Sel3	Selection signal for selftest block
6	NC	No Connection
7	Sel2	Selection signal for selftest block
8	Sel1	Selection signal for selftest block
9	Sel0	Selection signal for selftest block
10	Selftestb	control signal which determines start/stop signals are generated by either selftest block or extenally
11	Vdd_main	Power supply to chip
12	Vcm	Used in charge pump circuit
13	Rstdll	Reset signal for DLL and counter in selftest block
14	MonitorVc	Signal to indicate either to monitor the Vc of DLL or to externally controlling the value of Vc of DLL
15	Vcext	External control voltage to apply VC to DLL or to monitor the VC of DLL(Depends on MONITORVC signal)
16	Gnda	Ground to the chip
17	Gnda	Ground to the chip
18	NC	No Connection
19	Out19	Output of the Chip
20	Out18	Output of the Chip
21	Out17	Output of the Chip
22	Out16	Output of the Chip
23	Out15	Output of the Chip
24	Out14	Output of the Chip
25	Out13	Output of the Chip
26	Out12	Output of the Chip
27	Out11	Output of the Chip
28	Out10	Output of the Chip
29	Out9	Output of the Chip
30	NC	No Connection
31	Out8	Output of the Chip
32	Out7	Output of the Chip
33	Out6	Output of the Chip
34	Out5	Output of the Chip
35	Out4	Output of the Chip
36	Out3	Output of the Chip
37	Out2	Output of the Chip
38	Out1	Output of the Chip
39	Out0	Output of the Chip
40	Stoplvdsm	Differential STOP output signal

Pin No.	Pin Name	Description
41	Stoplvdsp	Differential STOP output signal
42	NC	No Connection
43	Startlvdsp	Differential START output signal
44	Startlvdsm	Differential START output signal
45	Stop	External STOP input signal
46	Reset	External reset signal
47	Start	External START input signal
48	Isink500uA	SINK current source used in LVDS buffer

3.2 Board Description

To Test the TDC chip, PCB Board is designed. Orcad software is used to design the PCB. Its a four layer PCB Board, top and bottom layers are routing layers and second layer is power plane and third layer is ground plane. It is manufactured on a copper plate FR-4 dielectric. Board dimensions are 12.325 x 16.5cm.

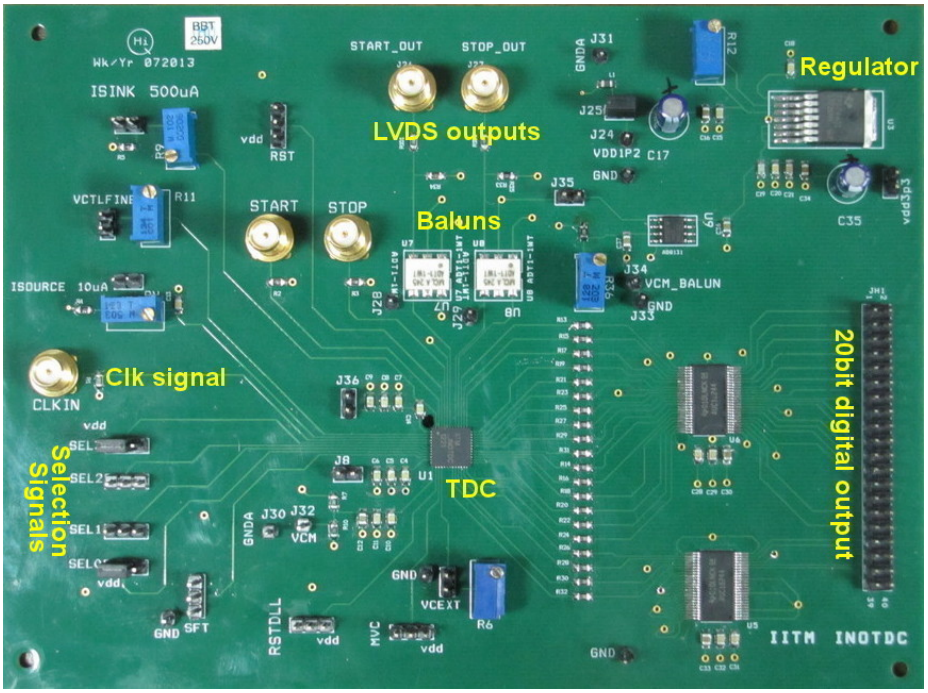


Figure 3.2: PCB Board

Power supply

The two VDD pins of the chip connected to power layer through jumpers to easily find out the current drawn by chip. This VDD supply is regulated through TPS74401 regulator. Before passing supply to chip, it is filtered using parallel bank of surface mount capacitors and through ferrite bead inductor. These ferrite bead inductors filter high frequency supply noise by converting it into a tiny amount of heat.

Current reference

Chip requires two current sources, one is Isource 10 μA and other is Isink 500 μA. We used resistor networks for both the current references. From simulations it is observed that the value of resistor required to generate 10 μA for different process corners varies from 73 KΩ to 85 K$\Omega$and similarly the resistor required to generate 500 μA varies from 800 Ω to 1200 Ω. Depending on this, the resistor values for both the current references are chosen.

Digital Output

The 20bit digital output is passed through buffers(SN74AUC16244) and its output is connected through 20pin jumper.

LVDS Outputs

An RF transformer (Mini-Circuits ADT1-1WT) is used to convert the differential start and stop lvds signals into a single ended outputs.

others

SMA connectors are used for external clock, start and stop signals. And all other control signals are given by using resistor pots. Selection signals are given through jumpers.

3.3 Test setup

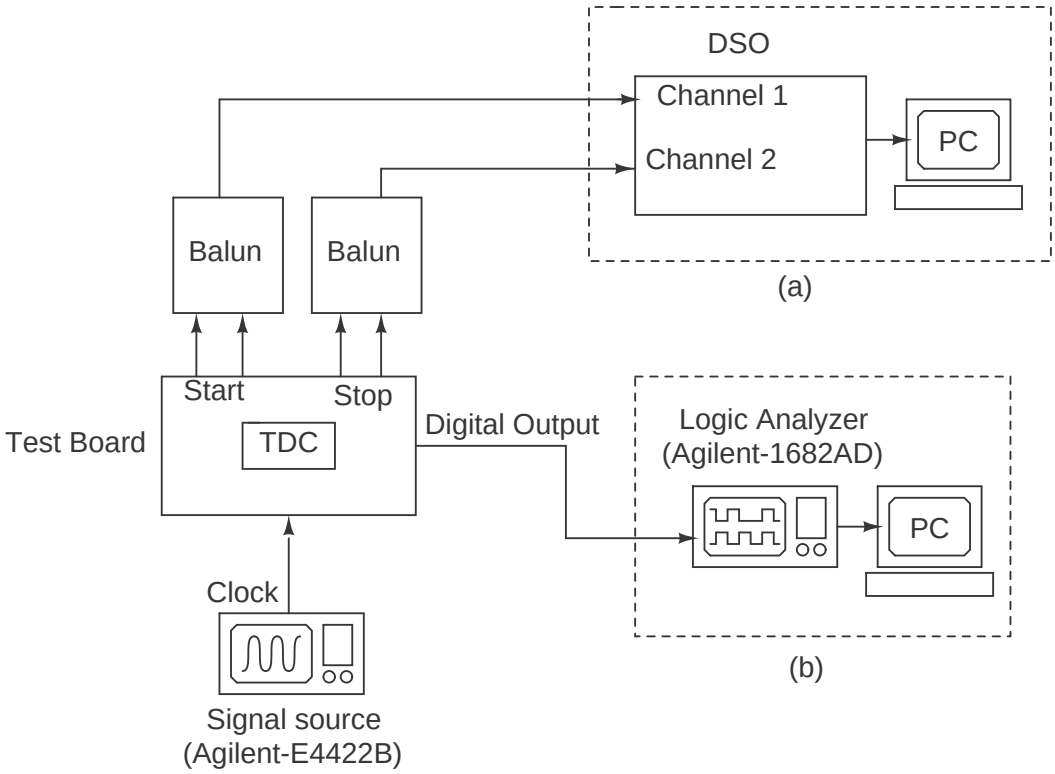


Figure 3.3: Test setup schematic

The top level block diagram of the test setup is as shown in fig. 3.3.

The clock signal is generated by a signal source (Agilent E4422B) which can generate a low jitter sine wave until 4GHz. The lvds outputs of start and stop signals from the chip are passed through a balun to convert into a single ended output. And this outputs are observed by using digital storage oscilloscope(Agilent DSO80204B) and the delay between start and stop signals can be calculated. Digital 20bit out-

put is connected to logic analyzer (Agilent-1682AD).From the logic analyzer and oscilloscope data is transferred to the PC for post processing.

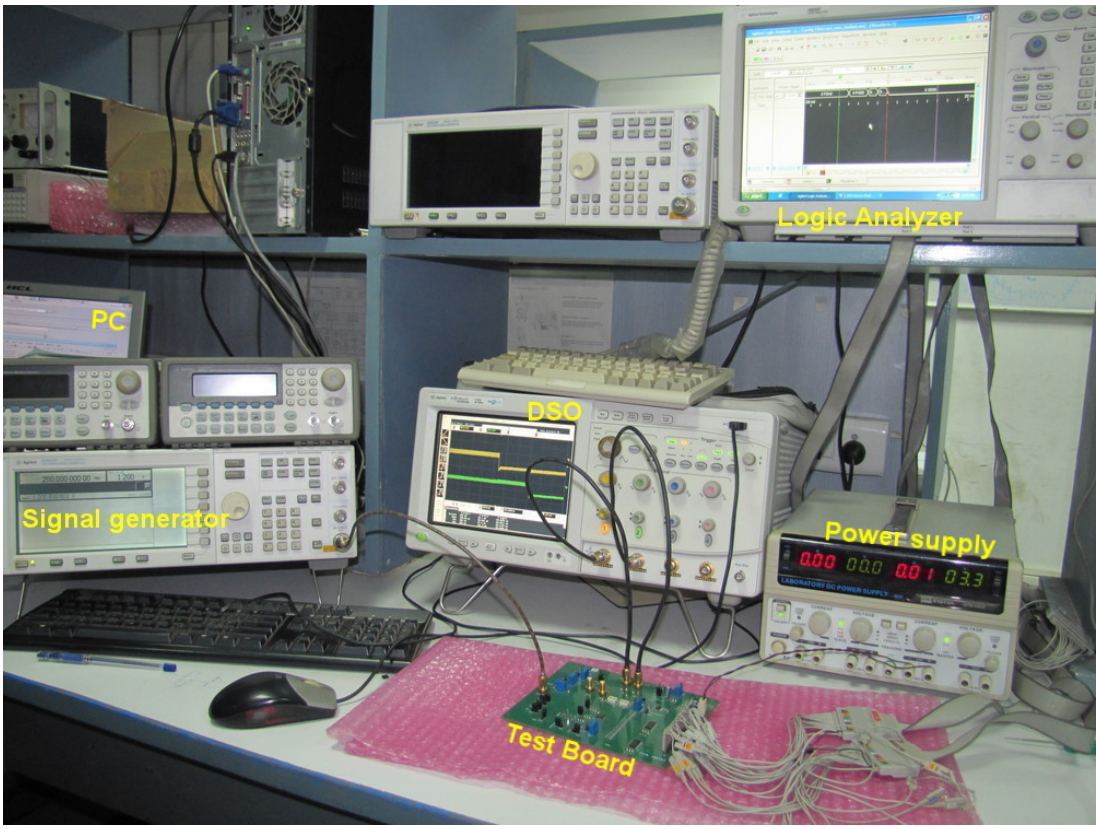


Figure 3.4: Test setup

3.4 Measurement Results

The comparision of simulation results and testing results are made for delay versus control voltage characteristics as shown in fig. 3.5. It is observed that, delay vs control voltage curve is with in simulation limits.

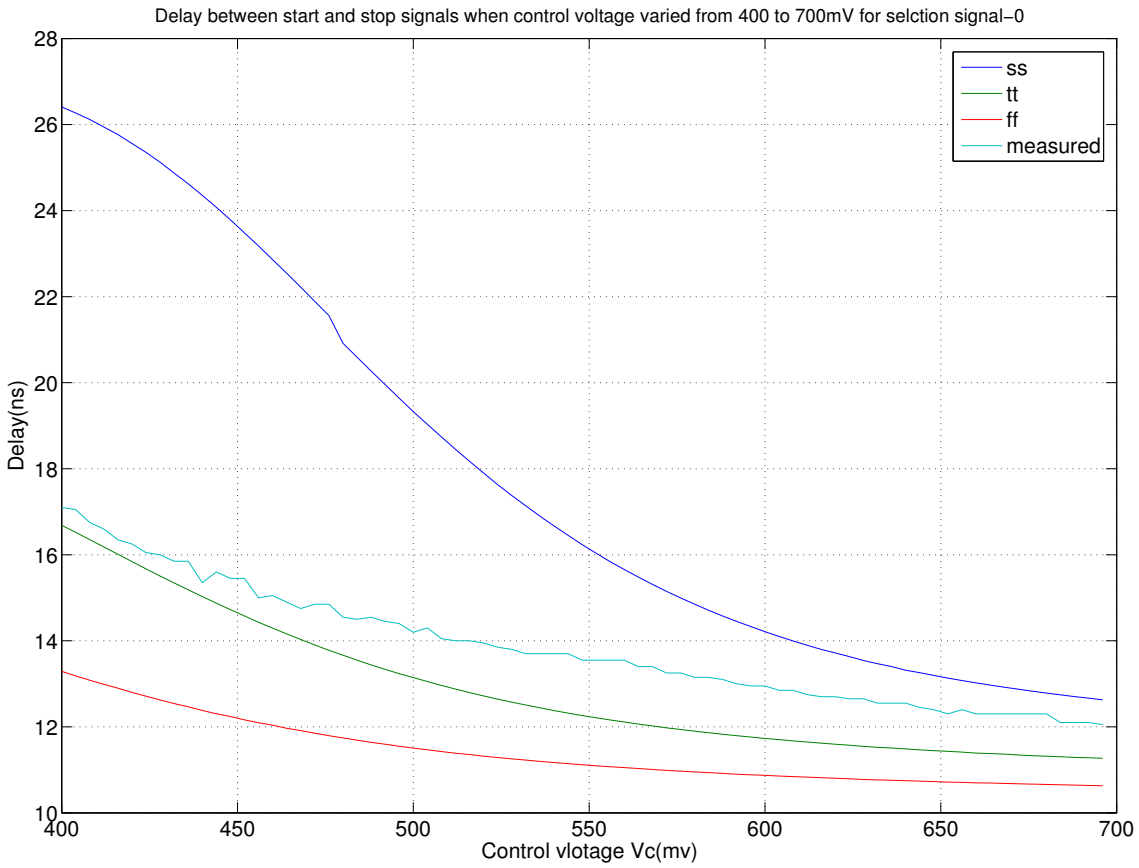


Figure 3.5: Delay between start and stop signals for sel-0 for different control voltages

The simulation results of VCDU delay characteristics are shown below in Fig. 3.6 for various process corners along with the voltages corresponding to a delay of 125ps. In testing, it is observed that the control voltage required to get the delay of 125ps is $650mV$ which is also with in simulation limits.

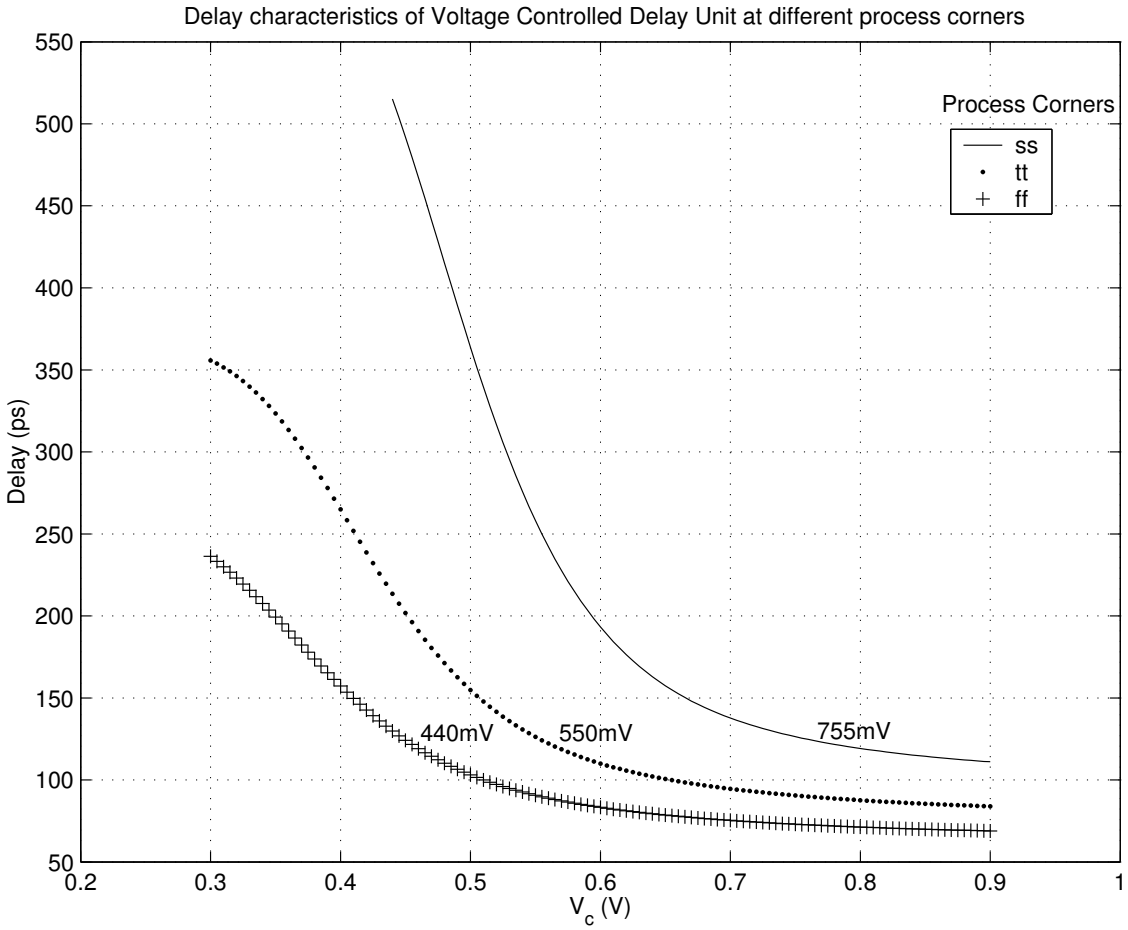


Figure 3.6: VCDU characteristics. The voltages shown correspond to 125ps delay.(2)

The variation of DLL control voltage with frequency is shown in Fig. 3.7

The delay between the start and stop signals is obtained from oscilloscope and 20 bit digital output is obtained from logic analyzer. Thus this 20 bit output is verified with equivalent digital value for the corresponding given delay. These observations are done for different frequencies and for different selection values.

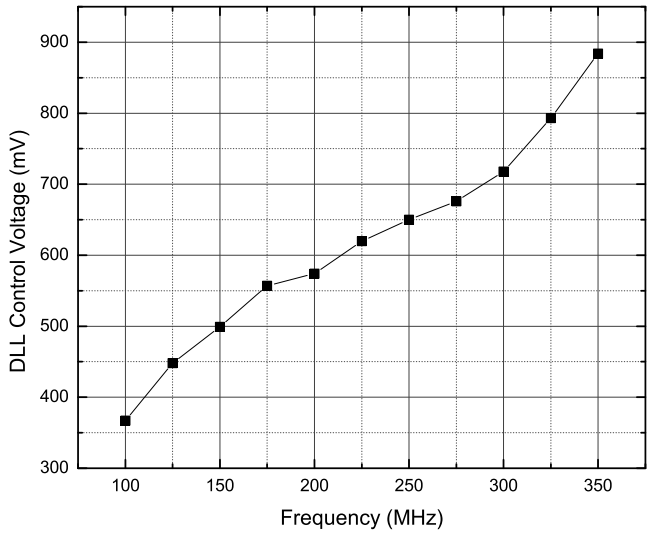


Figure 3.7: Variation of DLL control vlotage with frequency

For 250MHz clock frequency, Delay vs Digital outputs for different selection signals are plotted below.

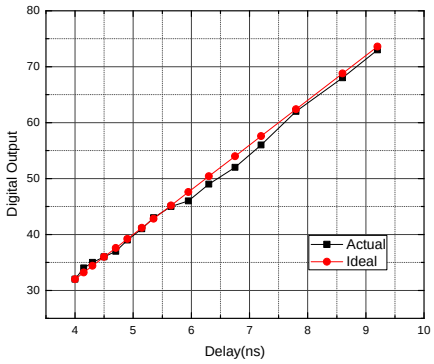


Figure 3.8: 250MHz and sel-15

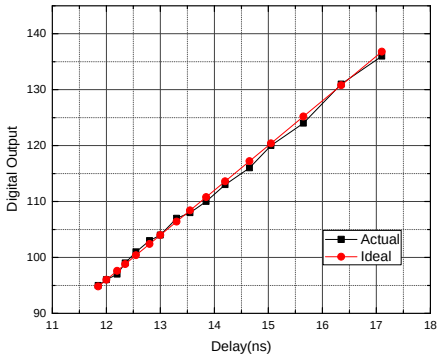


Figure 3.9: 250MHz and sel-0

We can see that the actual output and ideal outputs are fairly same. But it is observed that the outputs for higher selection signals (sel-10 to sel-14) are not matching with ideal outputs. Its because the top 3 most significant bits of 20bit output from chip are Zero. The reason for this is yet to be found out.

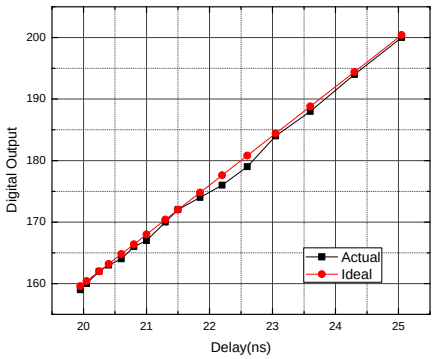


Figure 3.10: 250MHz and sel-1

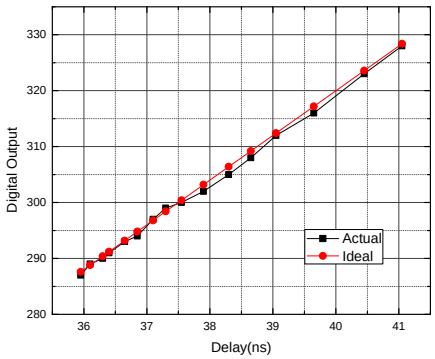


Figure 3.11: 250MHz and sel-2

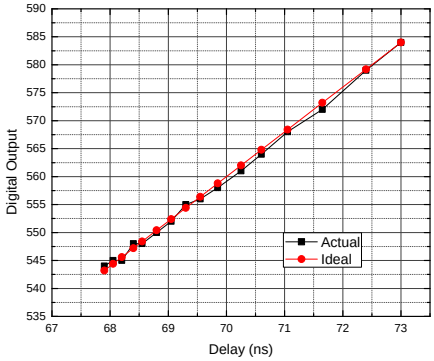


Figure 3.12: 250MHz and sel-3

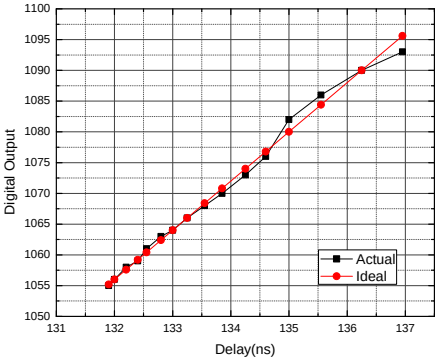


Figure 3.13: 250MHz and sel-4

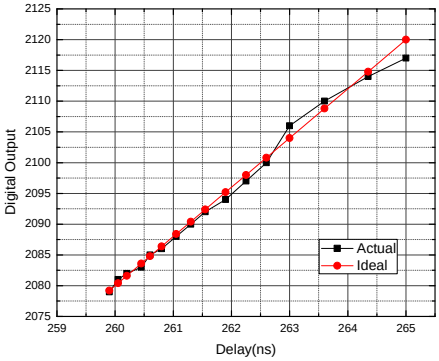


Figure 3.14: 250MHz and sel-5

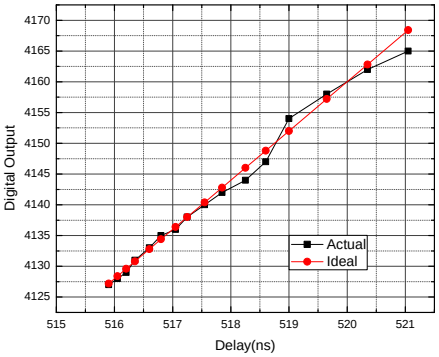


Figure 3.15: 250MHz and sel-6

As frequency increases or decreases from 250MHz, the deviation between actual and ideal value of outputs increases. It is observed that the chip is working for clock frequencies of range from 100MHz to 350MHz.

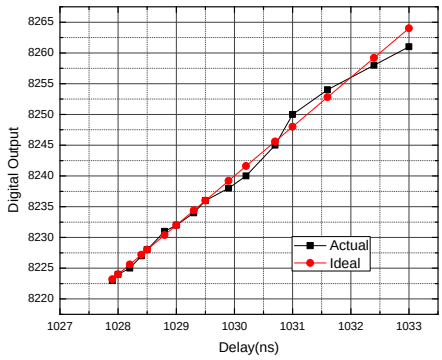


Figure 3.16: 250MHz and sel-7

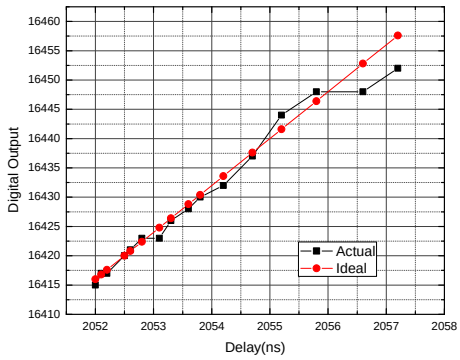


Figure 3.17: 250MHz and sel-8

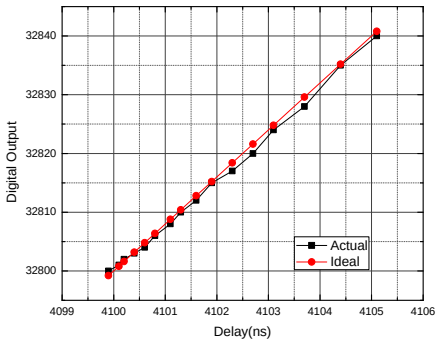


Figure 3.18: 250MHz and sel-9

The delay vs digital output plots for different frequencies and for different selection signals are shown in Fig. 3.19 to Fig. 3.34.

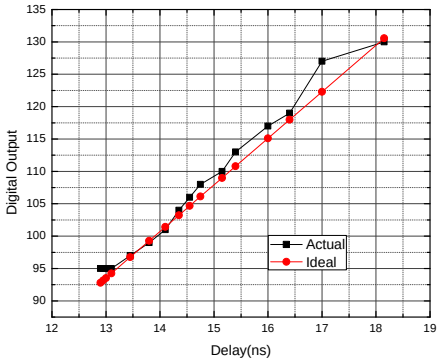


Figure 3.19: 225MHz and sel-0

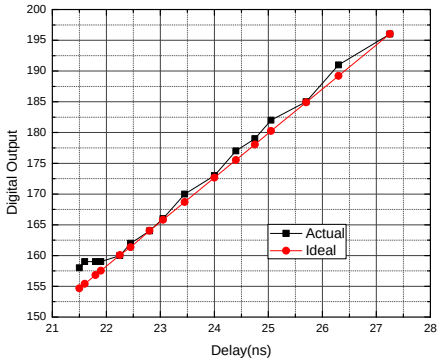


Figure 3.20: 225MHz and sel-1

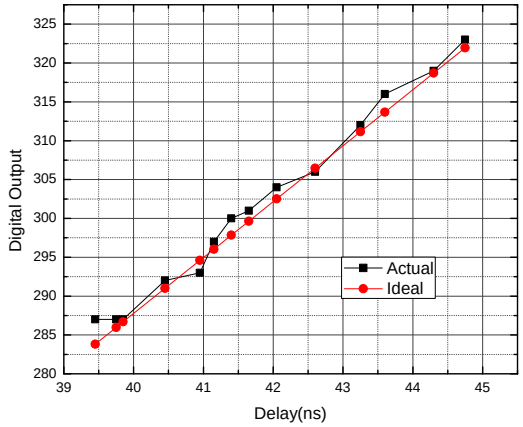


Figure 3.21: 225MHz and sel-2

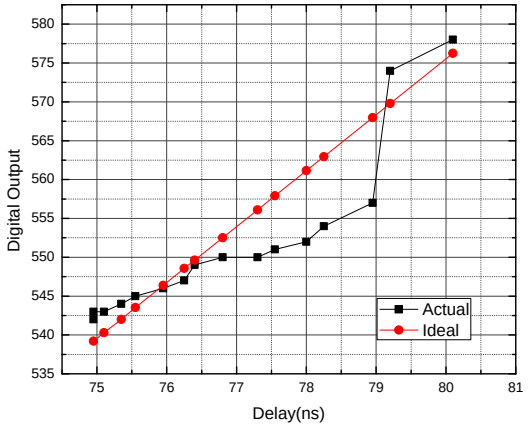


Figure 3.22: 225MHz and sel-3

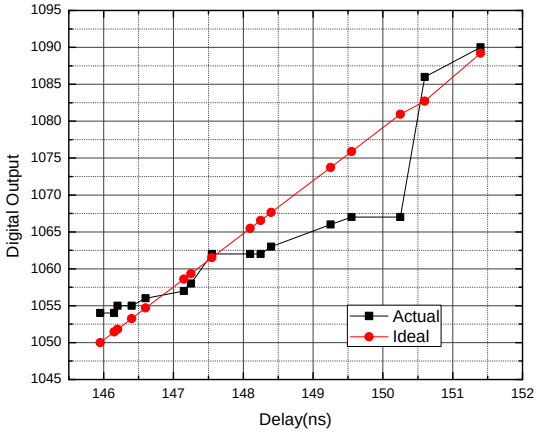


Figure 3.23: 225MHz and sel-4

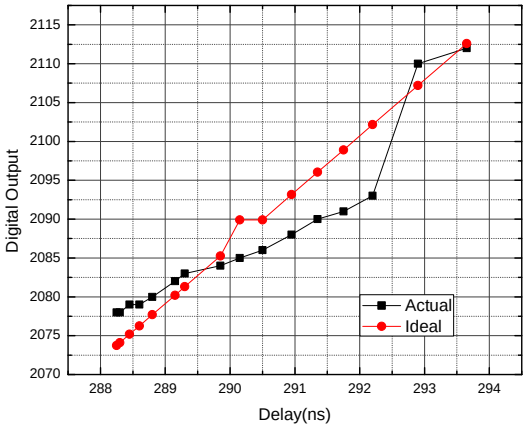


Figure 3.24: 225MHz and sel-5

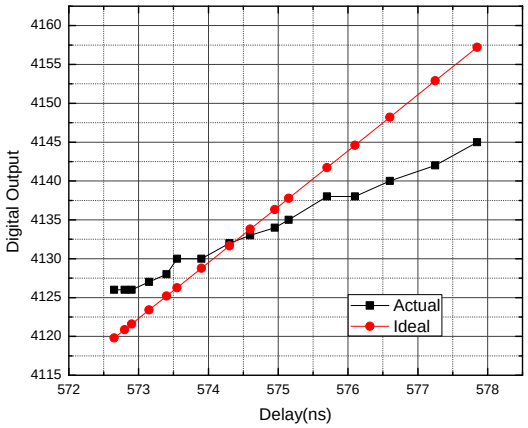


Figure 3.25: 225MHz and sel-6

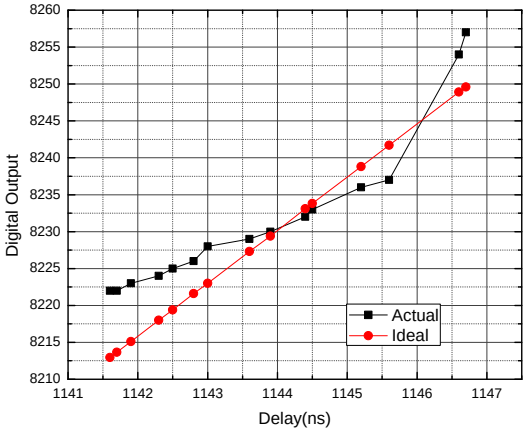


Figure 3.26: 225MHz and sel-7

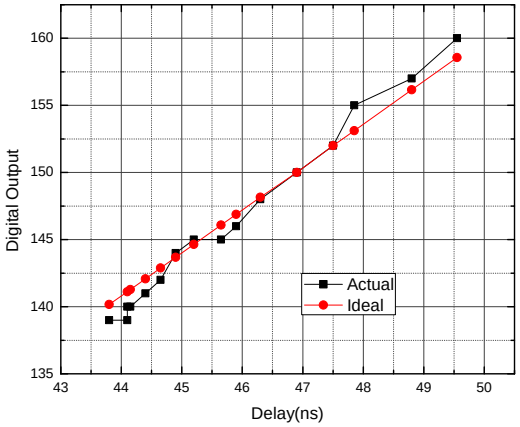


Figure 3.27: 100MHz and sel-1

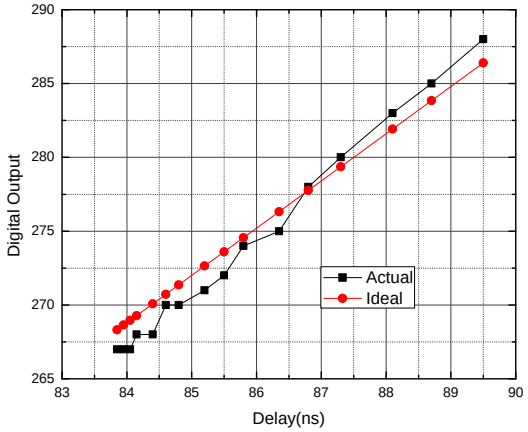


Figure 3.28: 100MHz and sel-2

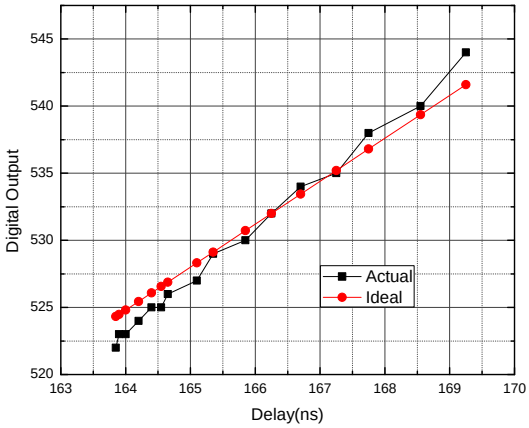


Figure 3.29: 100MHz and sel-3

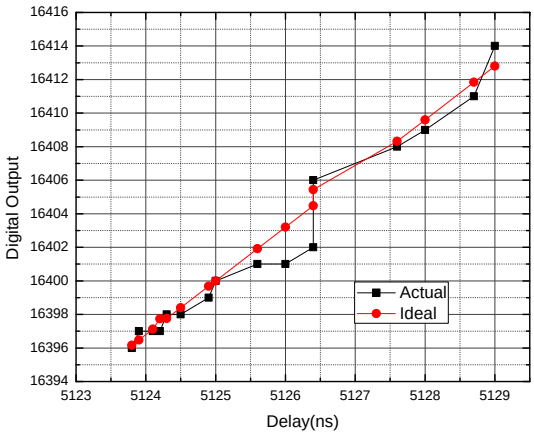


Figure 3.30: 100MHz and sel-8

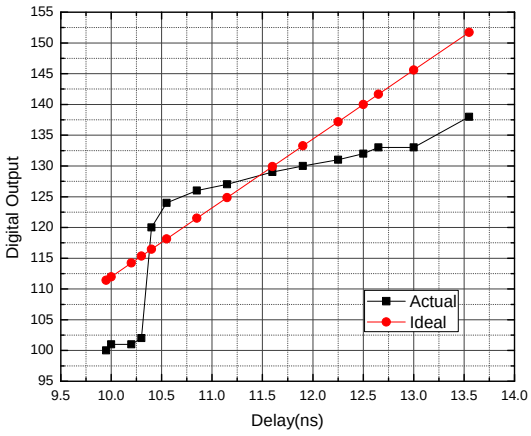


Figure 3.31: 350MHz and sel-0

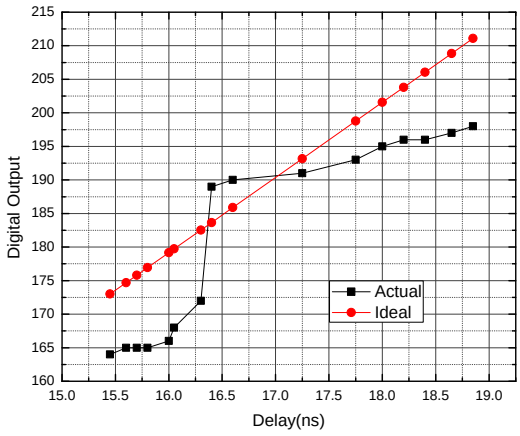


Figure 3.32: 350MHz and sel-1

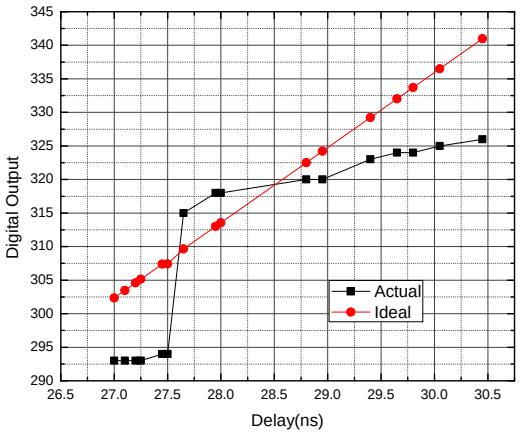


Figure 3.33: 350MHz and sel-2

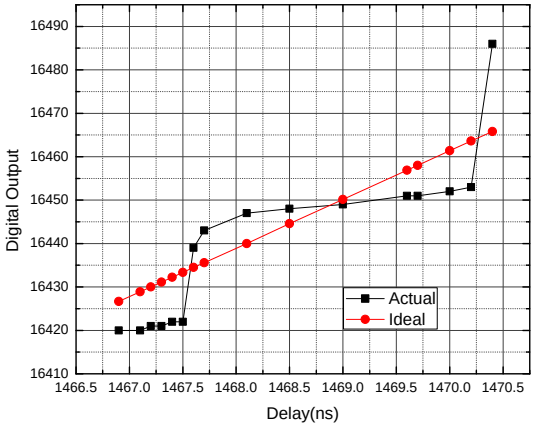


Figure 3.34: 350MHz and sel-8

3.5 Problems encountered with the chip

1. After reset the 20bit digital output is constant only for 10μs instead of being constant until next reset comes.

2. The activity of most significant 3 bits of the chip are always zero. This is the reason for getting wrong outputs for higher selection signals.

CHAPTER 4

Conclusions and future work

In this project, PCB board was designed to test the TDC Chip. we have taken the various readings to check whether the testing results are matching with simulation results or not. We verified the functionality of the chip and found some problems which the chip has. The power consumed by the chip is measured as 8.6 mW.

4.1 Future work

A PCB has to be designed with programmable delay chip so as to give external start and stop signals with finer delays for INL/DNL measurements. And have to findout the reasons for the problems the chip is having.

APPENDIX A

PCB Schematic And Layout

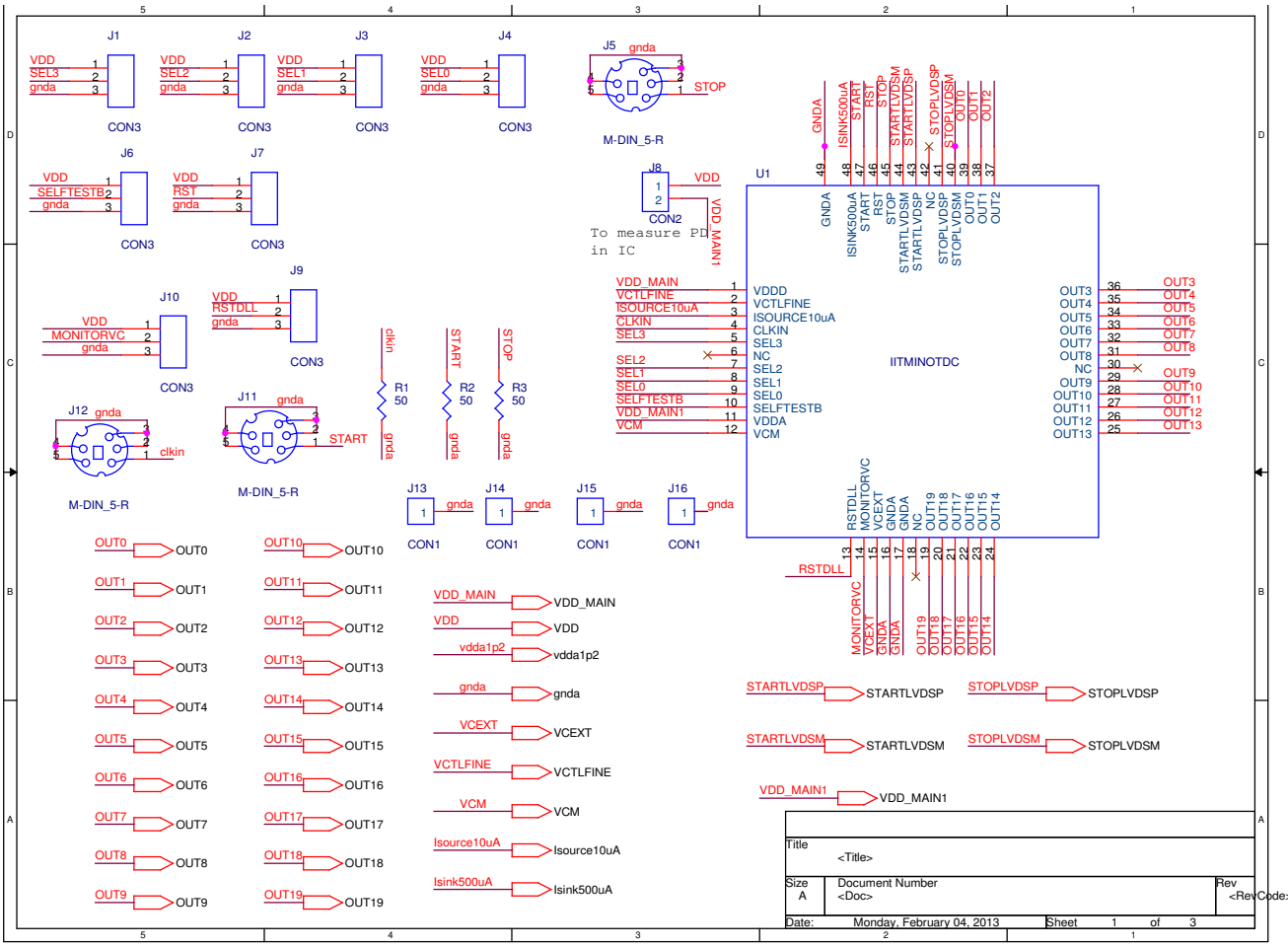


Figure A.1: PCB SCHEMATIC: Page1

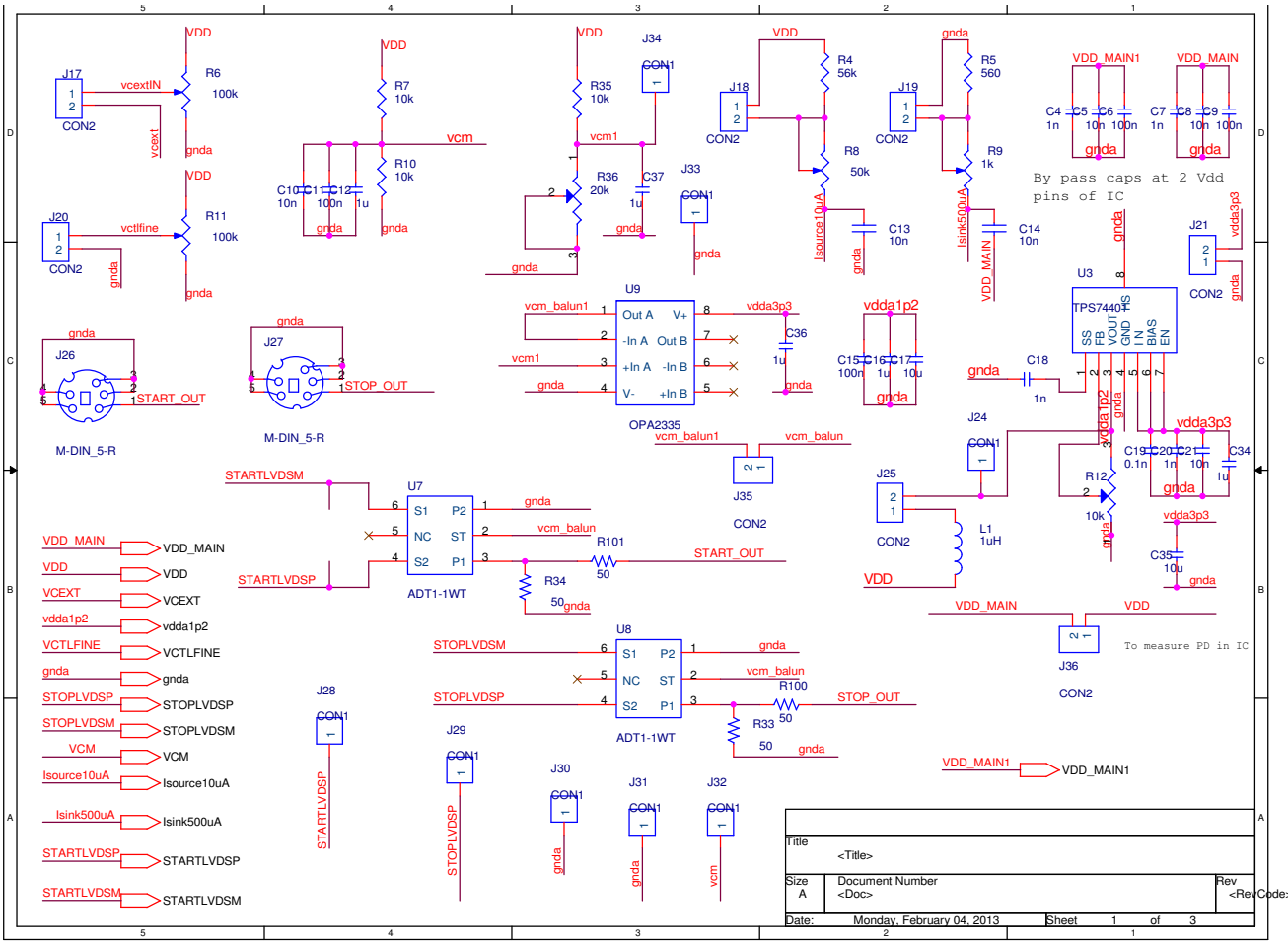


Figure A.2: PCB SCHEMATIC: Page2

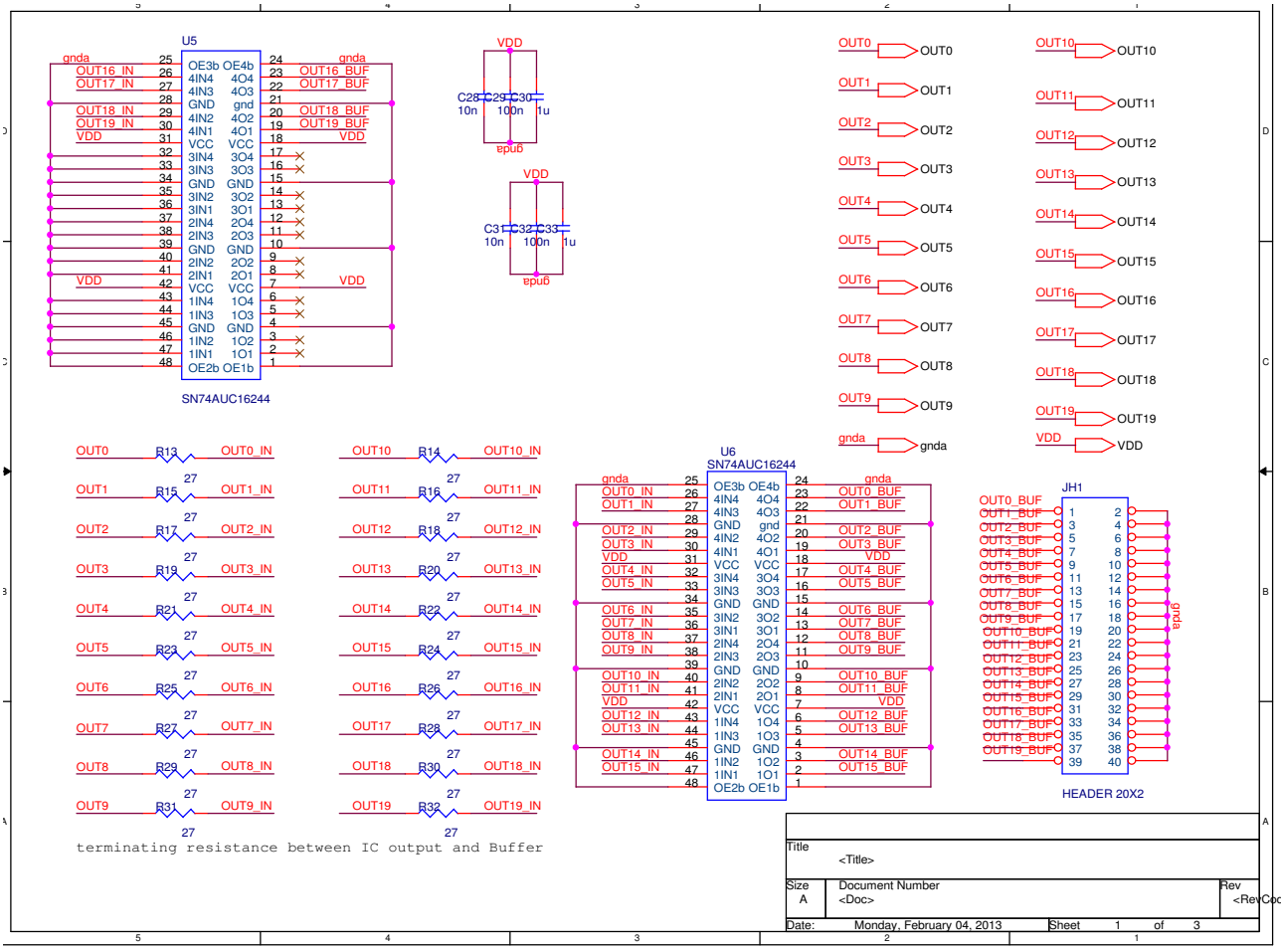


Figure A.3: PCB SCHEMATIC: Page3

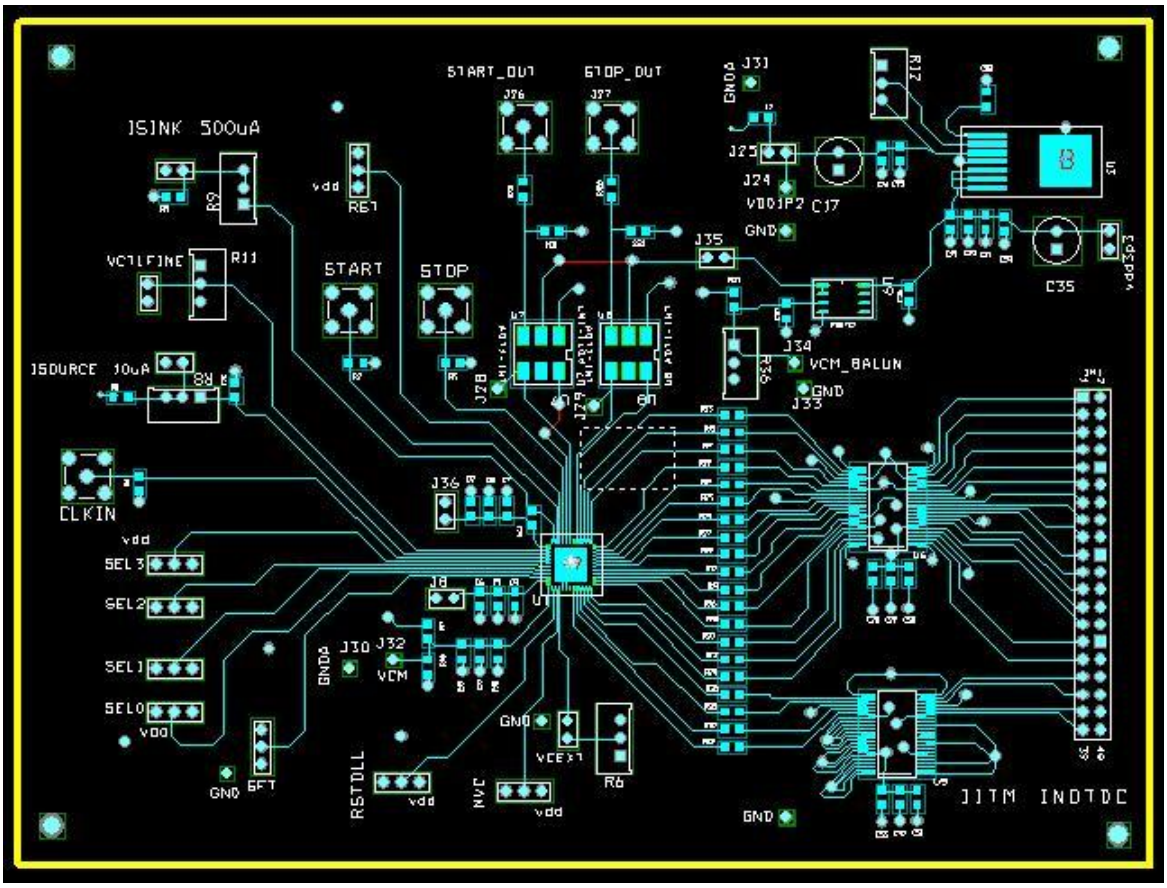


Figure A.4: PCB Layout

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[5] G. Li and H. Chou, "A high resolution time-to-digital converter using two-level vernier delay line technique," *Nuclear Science Symposium Conference Record*, vol. 1, no. 11, pp. 276–280, 2007.