Design of a Time to Digital Convertor for Neutrino Detectors

A THESIS

submitted by

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for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

JUNE 2012

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of Time to Digital Convertor for Neutrino Detectors** , submitted by **Praveen Kumar V**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology** , is a bona fide record of the work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 4th June 2012

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to Dr. Nagendra Krishnapura who kept his cool everytime I did blunders during the project and taught me how to do a clean job. I would also like to thank him for letting me spend time on a lot of extra-curricular activities also along with my project.

I would like to thank Dileep who motivated me to take up project in Analog and Mixed Signal Design. I would like to thank Abhishek, Sudhir, Venki and my Faculty Advisor Nandita Das Gupta for their moral support during my initial days in IIT. I would like to thank Prof. Shanti Pavan, Dr.Nitin Chandrachoodan, Dr. Shankaran Aniruddhan and Dr. Ravi shankar who made me realise that presenting a work is as important as the work itself. Thanks to Harshit, Nimit, Kunal and Amrith for their valuable time in making me familiar with ASIC design tools.

I would like to thank Sandhya, Avinash, Rakshit and Vijay who would help me anytime I run to them for support. Thanks to Sudhakar, Narendra, Amrut and Vijay for those glorious days in second year. Finally I would like to thank my labmates Hussain, Ajay, Rafi and Ram for those fun times in lab.

This thesis is dedicated to my parents, My uncle and Aunt, my twin and my sister.

ABSTRACT

KEYWORDS: Time to digital converter, Selftest.

This thesis presents the design of a time to digital converter (TDC). The architecture chosen for designing the system is a composite coarse-fine archi- tecture. The system uses an existing fine TDC design. The course TDC has a resolution of 4 ns and a range of 131 μs. The fine TDC has a resolution of 125 ps and a range of 4 ns. A delay locked loop (DLL) is used to stabilize the delays against PVT variations. A digital backend is designed to combine course and fine TDC outputs to give 20 bit output. A selftest block is added to generate start,stop and reset signals for testing the TDC internally.

The design is verified and taped out using UMC 0.13 μm CMOS process. The TDC has a resolution of 125 ps and a range of 131μs. The system uses a single clock with a frequency of 250 MHz. It occupies a size of one miniasic block i.e 1.525 mm $\times$ 1.525 mm. The chip has 44 pins and hence packaged using QFN48 package.

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ABBREVIATIONS

TDC	Time-to-Digital Converter
INO	Indian-based Neutrino Observatory
PVT	Process-Voltage-Temperature
DLL	Delay Locked Loop
VCDU	Voltage Controlled Delay Unit
PFD	Phase Frequency Detector
DNL	Differential Non Linearity
INL	Integral Non Linearity
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
UMC	United Microelectronics Corporation
LVDS	Low Voltage Differential Signalling
FPGA	Field Programmable Gate Array

CHAPTER 1

Introduction

Neutrino physics experiments in the last several decades have provided many new and significant results. Many highly multi-disciplinary research groups are working on neutrino detection and related research. The India-based Neutrino Observatory (INO) is one such particle physics research project which primarily aims to study atmospheric neutrinos. The neutrino detector of INO consists of a massive magnetized iron calorimeter [2]. The primary detection mechanism is via detection of muons produced in charged neutrino interactions. The detector comprises of layers of iron sheets interleaved with planar active detector elements. Each metal sheet contains a mesh of 32 by 32 readout channels. This helps us to determine the (x, y) co-ordinates of the neutrino hit on a given metal sheet. The index of the metal sheet will give us the z coordinate of the neutrino hit. We also need to determine the timing of the neutrino hit with respect to a reference start. Upon determining all these, we can know the (x, y, z, t) profile of the neutrino trajectory. For this, we need to be able to detect the hit on a given plate and process it accurately.

Avalanche mechanisms in the detector array give rise to a voltage spike which needs to be processed using high speed circuits. Fast and high gain amplifier along with latching circuitry is required to generate a digital signal which goes high when a neutrino hit is detected. The time of the neutrino hit also has to be measured with respect to a reference start. The system must be robust and should be low power because high temperatures in the detector render cooling mechanisms less efficient. The system proposed in this thesis is targeted to be of

use in these detectors. With this as the motivation for the thesis, we now proceed to describe briefly the design of the proposed system.

1.1 Designed system

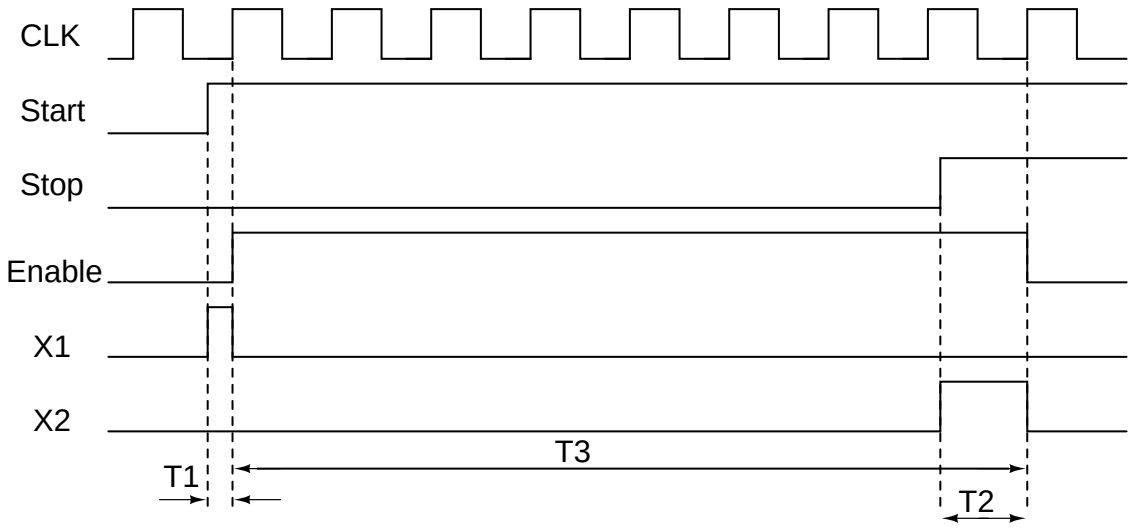


Figure 1.1: Basic operation of a TDC system.

The architecture chosen for designing the TDC is a composite coarse-fine architecture. The main idea is to measure the time as a sum of two parts: one measured by a coarse counter which gives a very high range but low resolution and the remaining part measured using a high resolution method which has a lower range. Consider the two inputs as shown in Fig. 1.1. Let the time interval between the two inputs be ΔT, the time to be digitized. The time interval ΔT can be split into three parts T1 , T2 and T3 w.r.t a system clock as shown in the figure. T1 is the time between the start signal and the next rising edge of the clock. Similarly T2 is the time between the stop signal and the rising edge immediately after it. T3 is time between the two rising edges of the clock mentioned above. Clearly, $T1, T2 < T_{clk}$ and the resolution of coarse TDC cannot be less than T_{clk}. Hence $T1, T2$ have to be measured by a fine TDC whereas $T3 > T_{clk}$ and can be arbitrarily large within the range of the TDC. Hence it is measured using a coarse

TDC. Also we have, $\Delta \mathrm{T} = T3 + T1 - T2$.

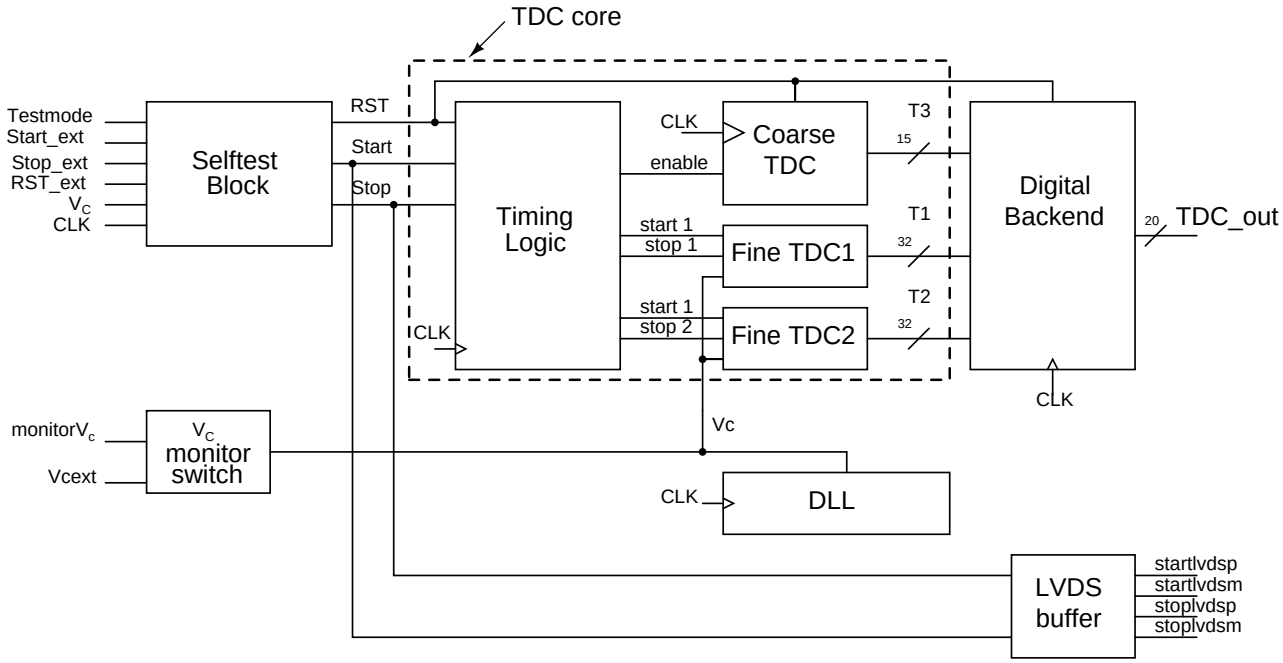


Figure 1.2: Block Diagram of TDC system.

The block diagram of the complete design is shown in Fig. 1.2. A timing logic block extracts the signals corresponding to the intervals $T1$ and $T2$ and feeds them to the fine TDCs. It feeds the coarse TDC with a signal corresponding to the interval $T3$. The fine resolution measurement of $T1$ and $T2$ is performed by the fine TDC and $T3$ is measured by the coarse TDC. The thermometer coded output of the fine TDC is converted to binary in the digital back end and ΔT is calculated from $T1$, $T2$ and $T3$. $T1$ and $T2$ are measured with 5 bit resolution and $T3$ is measured with 15 bit resolution. A Delay locked loop (DLL) stabilises the Voltage controlled delay units (VCDUs) in the fine TDC against PVT variations. A built-in selftest block generates start, stop and reset signals for TDC. A switch is used to tap the control voltage of the DLL. LVDS buffers are used to tap the start and stop signal inputs of the core TDC.

1.2 Organisation

Chapter 2 explains the existing fine TDC that was used in the system.

Chapter 3 explains the additional blocks like that were added to the existing architecture.

Chapter 4 gives the final layout and the simulation results which were used to verify the design.

Chapter 5 concludes the thesis and mentions the work to be done.

CHAPTER 2

Overview of existing TDC design

2.1 Fine TDC [1]

The Fine TDC used is a Flash TDC or a single delay line TDC. The delay line architecture [3],[4] is in principle similar to the working of a flash TDC. In a flash TDC, the input voltage is compared to a set of voltages uniformly distributed between the maximum and the minimum voltage. The output thermometer code encodes the input voltage in a digital form. A delay line based TDC works on a similar concept. The input time period is in essence compared to a set of time periods and a thermometer code is generated. Let the time interval between the two signals be T , the time to be digitized. The start signal i.e. the signal which arrives before the other is passed through a delay chain of n delay elements each having a delay Td as shown in Fig. 2.1. So, the output of the i_{th} delay element $(0 \leq i \leq n)$ is delayed by an amount iTd w.r.t the start signal. The D input of each flip flop is connected to stop signal. So the flip flops go high only when start is high and the delayed start signal clocks the particular flip flop. If the output of the j th element crosses the stop signal for the first time, then

$$(j-1)Td \leq T \leq jTd$$

The output is a thermometer code where the number of 0s in the code represents the number of LSBs in the delay. The implementation of flip flops is explained in detail in [1],[5]. The delay elements in the simplest implementation can be just a pair of in- verters in series. But if the delay elements are chosen to be buffers made

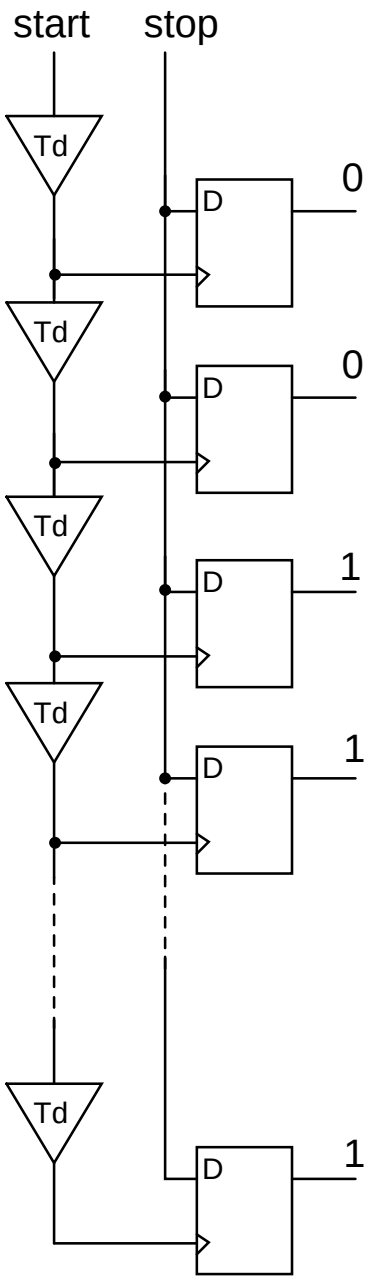


Figure 2.1: Fine TDC.

from inverters, then the delay of each element varies significantly with variations in process, supply voltage and temperature. Simulations show that between the ss (slow) and the ff (fast) process corners, the inverter delay varies by 60% of its value at the tt (typical) corner in the 0.13μm CMOS process. This would result in the LSB resolution being strongly dependent on process variations. Also, in a composite coarse-fine architecture such as this, it is necessary that the range of the fine counter be the same as the resolution of the coarse counter. The range of a simple inverter chain can vary by 60% across the corners, making it infeasible for the coarse-fine architecture to work correctly. So we need delay elements whose delay does not change with process variations.

One approach is to use a voltage controlled delay unit (VCDU) where the control voltages are adjusted so as to give the same delay in spite of process variations. The voltages are tuned by a Delay Locked Loop (DLL) which is locked to a fixed delay.

2.2 Voltage controlled delay unit (VCDU)[1]

The VCDU is basically similar to an inverter with additional transistors to control the current used to charge or discharge the output. The topology shown in Fig. 2.2 is called current starved topology since the top and bottom transistors starve the transistors in the signal path for current.

The transistors $M_{1,2,3,4}$ provide a current to the transistors $M_{5,6,7,8}$ which depends on the control voltages Vc and Vcb . This controls the delay from the input to the output of the VCDU. The transistors $M_{9,10,11,12}$ are used to ensure that there is a finite delay between the input and output in case the control voltage Vc falls below the threshold voltage of $M_{3,4}$. This can happen during the initial cycles when the DLL which generates the voltages Vc and Vcb is yet to lock.

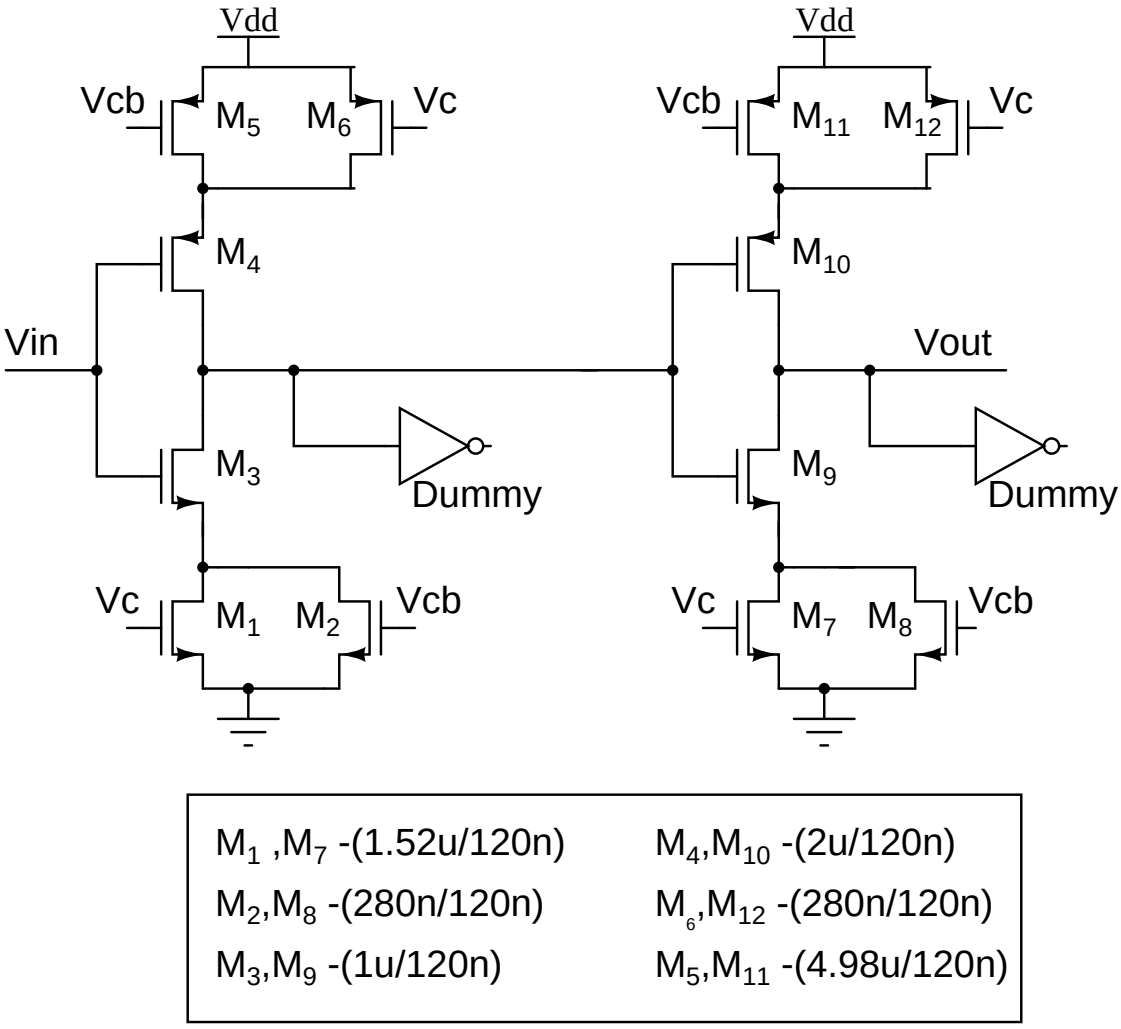


Figure 2.2: VCDU

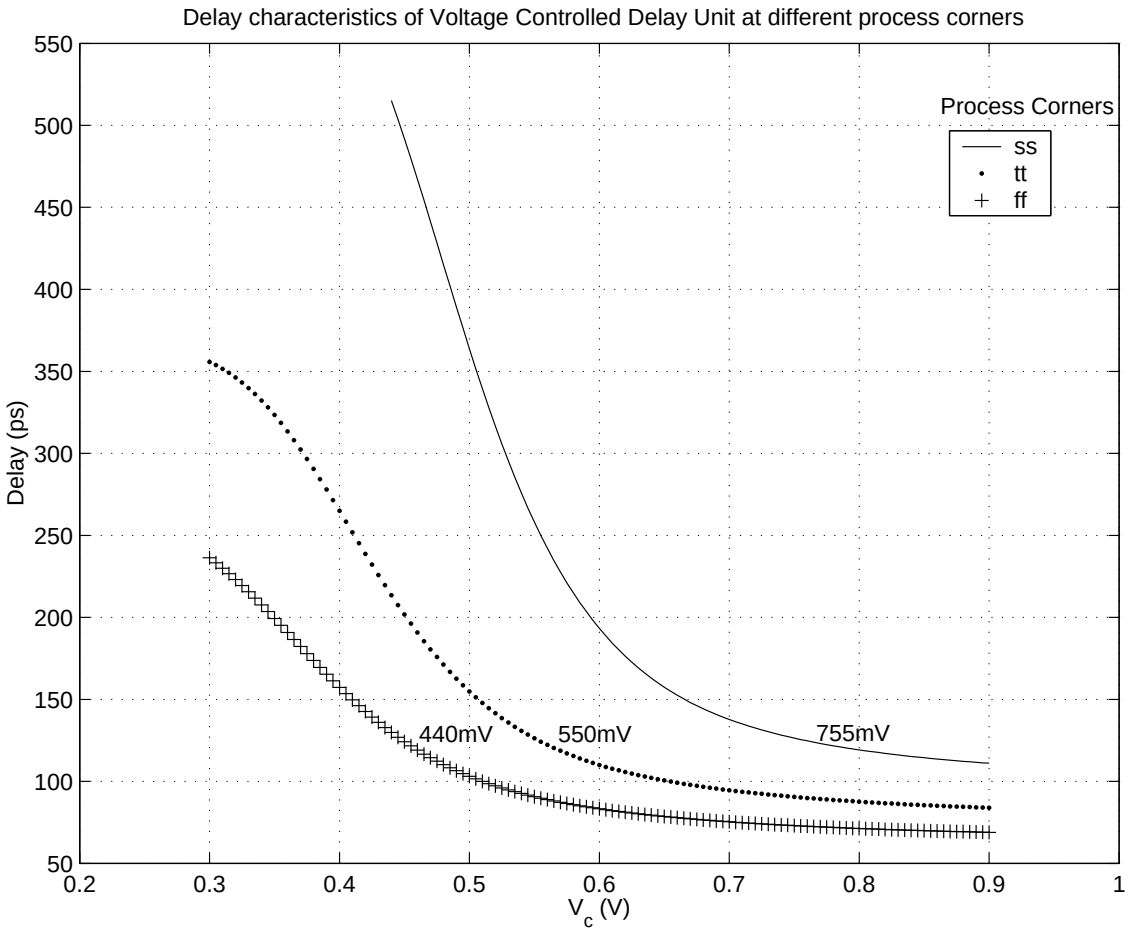


Figure 2.3: VCDU characteristics. The voltages shown correspond to 125ps delay.[1]

An alternative possibility exists for making a VCDU where the supply pin of a standard inverter is replaced by the control voltage. While this does ensure dependence of delay on control voltage, the drawback is that current is drawn from the control voltage node which may result in the control voltage change. The VCDU implemented in this design has only gate capacitance loads at Vc and Vcb and hence current drawn is much lesser.

The VCDU delay characteristics are shown below in Fig. 2.3 for various process corners along with the voltages corresponding to a delay of 125ps. As we can see, all three voltages are well within the swing limits of the charge pump which drives these voltages and also above the threshold voltage of the transistors in the VCDU.

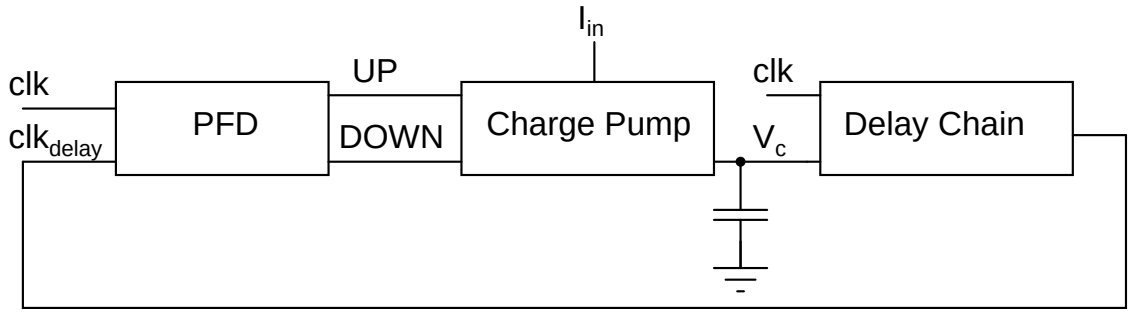


Figure 2.4: Delay Locked Loop(DLL).

2.3 Delay locked loop (DLL)[1]

As mentioned before, we need to ensure that the delay of the VCDU is constant in spite of process variations. For this purpose, we use a DLL which locks the delays of its elements to a fixed value. It does so by altering the control voltages using a feedback loop. If the delay elements in the DLL and the TDC are designed and laid out in an exactly identical manner, the delays in the TDC will also be constant in spite of process variations. Block diagram of a DLL is shown in Fig. 2.4. The working is similar to that of a PLL except that the VCO is replaced by a delay line and no frequency division takes place. The phase frequency detector (PFD) detects the phase difference between the input clock and the feedback signal. Depending on which signal is lagging, the PFD gives UP and DN output signals so as to correct the phase difference. The charge pump changes the control voltage of the delay line appropriately so as to reduce the magnitude of the phase difference at the input of the PFD. The DLL used here has 32 delay elements and an input clock of period 4 ns. So, each delay element is locked to 125 ps. This delay is replicated in the delay line of the TDC by using the same control voltage and nominally identical design of delay line. Assuming PVT variations affect the delay line in the DLL and that in the TDC identically, the delays in the TDC will also be 125 ps, independent of PVT variations. The design of each of the components of the DLL is explained in [1].

CHAPTER 3

Modified TDC system

3.1 Timing logic

The timing logic block extracts the signals which need to be sent to the fine and coarse TDCs. For the coarse TDC, whose implementation essentially involves just a counter, the timing logic block generates an enable signal. This enable signal goes high with start signal and goes low with arrival of the stop signal. The coarse TDC should count the number of clock cycles when this enable is high. This implementation is shown in Fig. 3.1. The timing logic for fine TDC is explained in detail in Fig. 3.2.

T_{Fine} is the time to be measured by fine TDC. For this the interval T_{Fine} between the start/stop signal and the clock has to be extracted into two step signals spaced by the same amount. Three different implementation cases using flip flops are discussed in Fig. 3.2. In case(i) one of the inputs to the fine TDC is the start/stop signal itself. The second input will be the signal X_2 which goes high when clock goes high. But now the spacing between the fine TDC input signals is,

$$T_1 = T_{Fine} + T_{CQ-DFF2}$$

In case(ii) an additional flip flop is used so that now X_1 is given as input to fine TDC in place of start/stop. X_1 is the signal that goes high when start goes high but with a delay of $T_{CQ-DFF1}$. Now the spacing between the fine TDC input signals is,

$$T_1 = T_{Fine} + (T_{CQ-DFF2} - T_{CQ-DFF1})$$

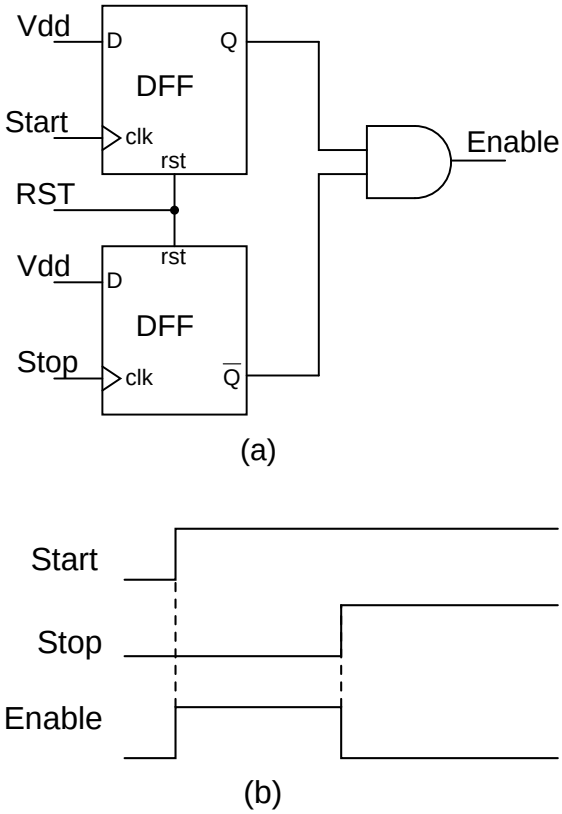
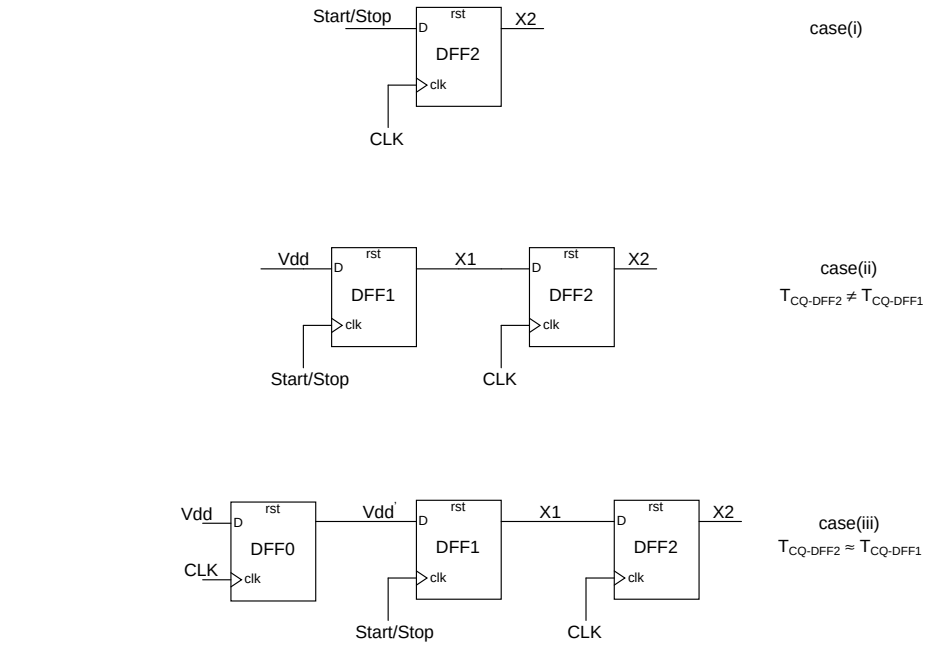
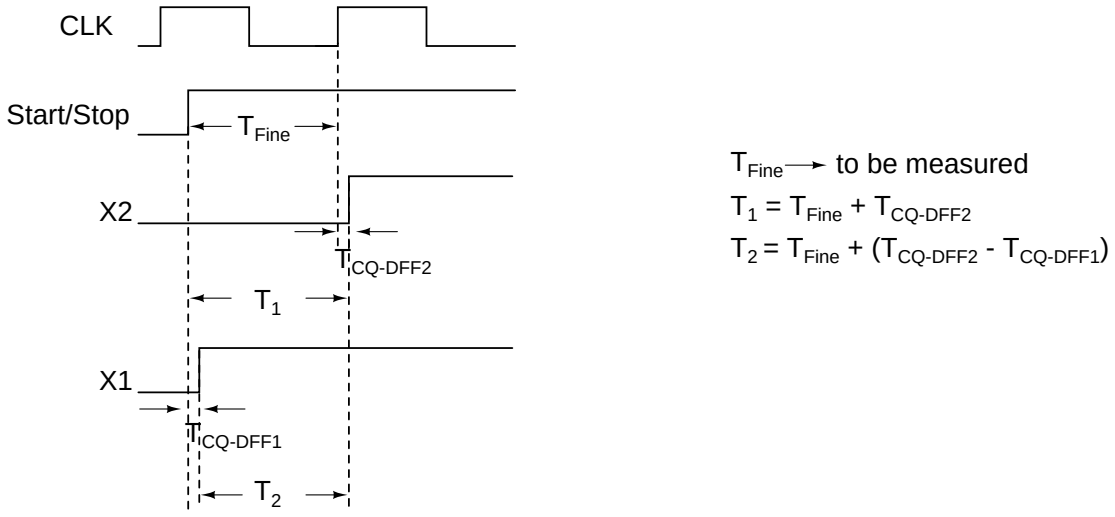


Figure 3.1: Timing logic for coarse TDC. (a) Implementation. (b) Timing diagram.



(a)



(b)

Figure 3.2: Timing logic for fine TDC. (a) Implementation. (b) Timing diagram.($T_{CQ-DFF2}$ and $T_{CQ-DFF1}$ are clock to Q delays of the flip flops)

The clock-to-Q delays can be made equal by using identical flip flops. [1] mentions that the clock-to-Q delays also depend on the amount of current drawn from the D input of the flip flops. If the D input of DFF1 is connected to the voltage source Vdd , it can draw more current than DFF2 which is connected to the output of DFF1. To rectify this, we connect DFF1 input also to a flip flop output, assuming that the start/stop signals arrive at least one cycle after the reference clock has started. This is shown as case(iii) in Fig. 3.2. The outputs X_1 and X_2 are given to the fine TDC. Since X_1 is loaded by DFF2 as well as the fine TDC whereas X_2 is loaded only by the fine TDC, the delay of flip flops can be different. This can easily be rectified by loading X_2 with a dummy load identical to the input capacitance of DFF2.

3.2 Coarse TDC

The coarse TDC is basically a 15 bit digital counter with a clock period of 4 ns. It is enabled with the start signal and disabled with the stop signal. It uses the reference clock running at 250 MHz for its counting. It was implemented in Verilog. Synthesis was done in *DesignVision*. Place and route was done using *Encounter*. The standard cell library used for synthesis and place and route was FSC0H_D_GENERIC_CORE_2009Q1v3p0, which is UMC-Faraday's standard cell library for high speed(HS) process. The simulations on post synthesis and post route verilog netlists were done using Modelsimlib library which is a part of the frontend Faraday libraries mentioned above.

3.3 Digital backend

The digital back end consists of digital circuitry which combines the output of coarse and fine TDCs to generate the final 20 bit TDC output with a resolution

of 125 ps. The output of coarse TDC is 15 bits with a resolution of 4 ns. This is equivalent to 20 bits with a resolution of 125 ps (Because $4\,\text{ns} = 32 \times 125\,\text{ps}$ and multiplication by 32 is same as left shift of a binary number by 5 bits). The output of fine TDC is a 32 bit thermometer code. The number of zeros in this thermometer output gives the the fine delay with a resolution of 125 ps. The thermometer output is converted to a 5 bit binary number by adding the number of zeros. The final output of the backend which is also the output of the overall TDC is calculated as

$$T_{coarse} \times 2^5 + T_{fine2} - T_{fine1}$$

To ensure that the output of fine TDCs are settled, the backend block needs to wait for a few clock cycles before reading the inputs. For this the backend waits for 8 clock cycles after stop input is issued(i.e. after the enable signal has gone low). Thus the backend block reads the enable signal, waits for 8 clock cycles after enable goes low and then reads the thermometer outputs. A combinational adder circuit adds the number of zeros in the input thermometer code. The course TDC output is shifted by 5 bits. We also have adder/subtracter circuitry for adding and subtracting these coarse and fine TDC outputs so as to obtain the final 20 bit output.

3.4 Built-in selftest

3.4.1 Implementation

The testing of TDC chip needs high frequency equipments to generate start and stop signals. A selftest block included in the chip eliminates this need by internally generating the start, stop and reset signals required to test the TDC. Fig. 3.3 shows the functional diagram of the selftest block.

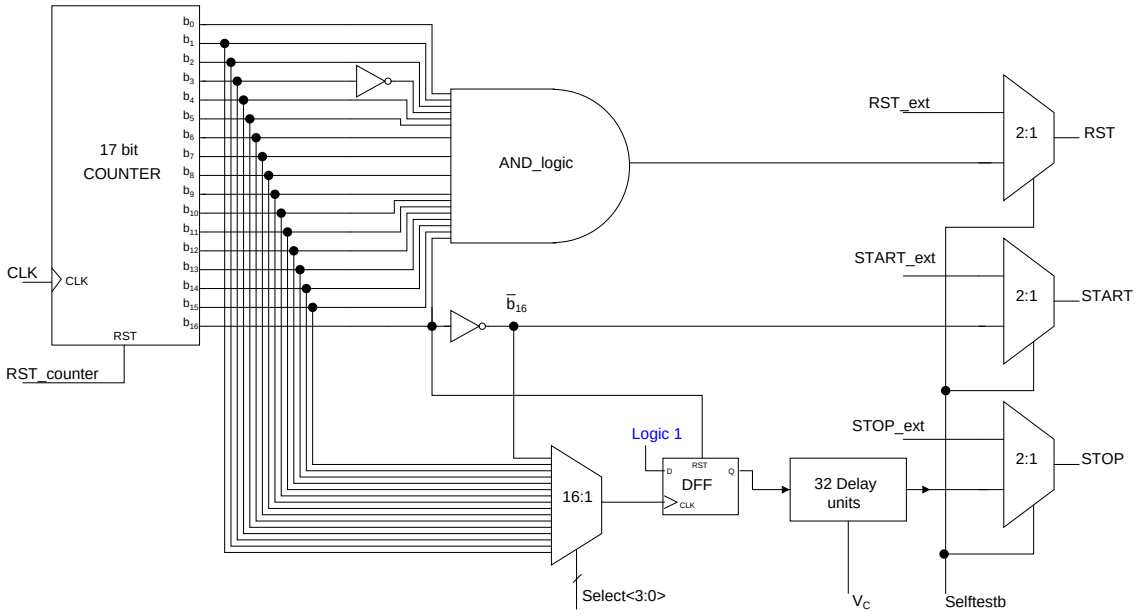


Figure 3.3: Built-in Selftest.

It consists of a 17 bit counter, the output of which is denoted by b. The i^{th} bit b_i of the counter output, toggles with a period of $2^{(i+1)}T_{clk}$. b_{16bar} is used as the internal start signal. By choosing the value of *select* input, various delays for stop signal can be chosen chosen. A flip flop placed before the delay line ensures that the internal stop signal goes high only once in each cycle of start signal. This is clearly explained in Fig. 3.4. For fine delays in stop signal, a voltage controlled delay line similar to the one used in fine TDC is used.

From Fig. 3.4(a), we see that b_{16bar} goes high when the counter is reset. Since the initial state of b_{16bar} is unknown, the first start signal comes only after 2^{17} clock cycles. In Fig. 3.4(b) we see that the output of the flip flop goes high only once in an entire cycle of the counter. If T_d is the average delay of each delay element in the delayline, then the internal stop signal is delayed by $32T_d$ w.r.t flip flop output. A RST signal is generated 8 clock cycles before b_{16bar} goes high in the next cycle. This ensures TDC is properly reset before each cycle of start and stop inputs. The entire selftest block excluding the delayline was implemented in verilog. Synthesis and routing is done using automated CAD tools *Designvision*

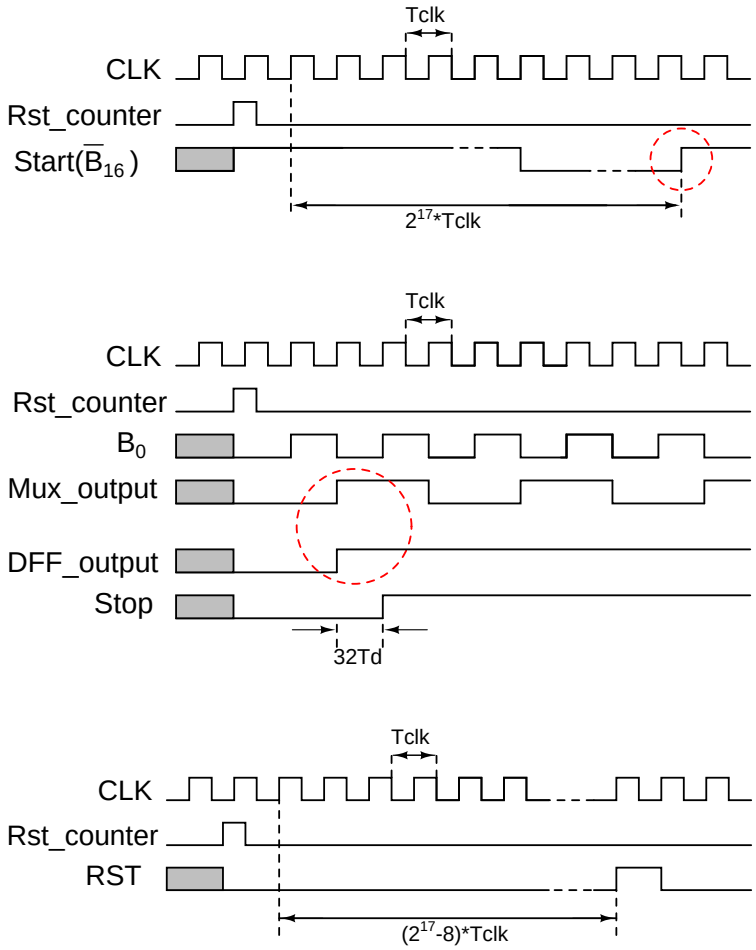


Figure 3.4: Timing diagram for (a) Start signal. (b) Stop signal with select=0 (T_d is the average delay of each delay unit). (c) RST signal

and *Encounter*. It occupies an area of $87\mu\text{m} \times 76\mu\text{m}$.

3.4.2 Simulating selftest in cadence

Since the initial state of b_{16bar} cannot be set to zero in the first cycle, the first internal start signal to test the TDC will arrive after 2^{17} clock cycles which corresponds to 512μs. This is not a problem while testing the chip as 512μs of initial startup delay is fine. But this is a huge simulation time in cadence for testing this design. So to simulate the block in cadence and to generate start signal within the first cycle of selftest block, the following steps have to be followed.

1. Initially set the external start and stop signals to zero. Make $selftestb$ high so that external signals are the initial inputs to the TDC.
2. When RST_counter goes high b_{16bar} goes high and the flip flop(the flip flop placed before delayline in Fig. 3.3) output goes low. This causes the internal stop signal to go low after $32T_d$ ns. The $selftestb$ should be high at least till this time. T_d is the average delay of each VCDU in the delayline.
3. When $selftestb$ goes low, the start output of the block goes high and this can be used as the internal start signal for simulations.
4. Depending on the value of select input and the value of control voltage V_c , the stop signal can be varied.

3.5 Miscellaneous blocks in the design

This section explains the additional blocks that are added to the TDC system. These are blocks that aid in probing some of the intermediate signals, which help in verifying the functionality of the chip during testing. It also explains some of the essential blocks added to make the layout ready for tape-out.

3.5.1 Switch to monitor or force control voltage V_C

By now we know that the resolution of the fine TDC is totally dependent on the delay of each delay unit, which inturn depend on the control voltage V_C that is set by the DLL. By simulations it is found that the value of control voltage for a delay of 125ps is 551mV. To ensure that the DLL has indeed settled to this value of V_C, a switch shown in Fig. 3.5 has been added. The switch is implemented using a simple transmission gate.

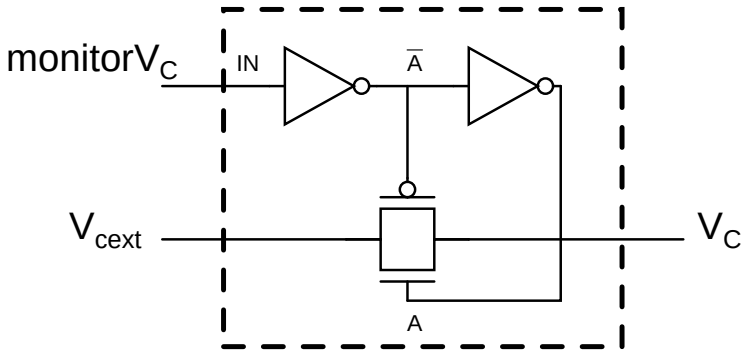


Figure 3.5: Switch to monitor or force V_C.

We can see from the figure that, when $monitorVc$ is high the value of control voltage on the DLL can be read at $vcext$ pin. Since the switch is a transmission gate, the $Vcext$ pin can also be used as an input pin wherein the output control voltage of DLL can be forced to an arbitrary value so that we can have a control over the resolution of TDC independent of offsets in DLL.

3.5.2 Low voltage differential signalling(LVDS) buffers

During testing we need to ensure that the output of the TDC exactly corresponds to the start/stop signals generated by the internal selftest block. For this, two LVDS buffers as shown in Fig. 3.6 are used. They tap the start and stop signals generated by selftest block and output them as differential signals of low output

swings.

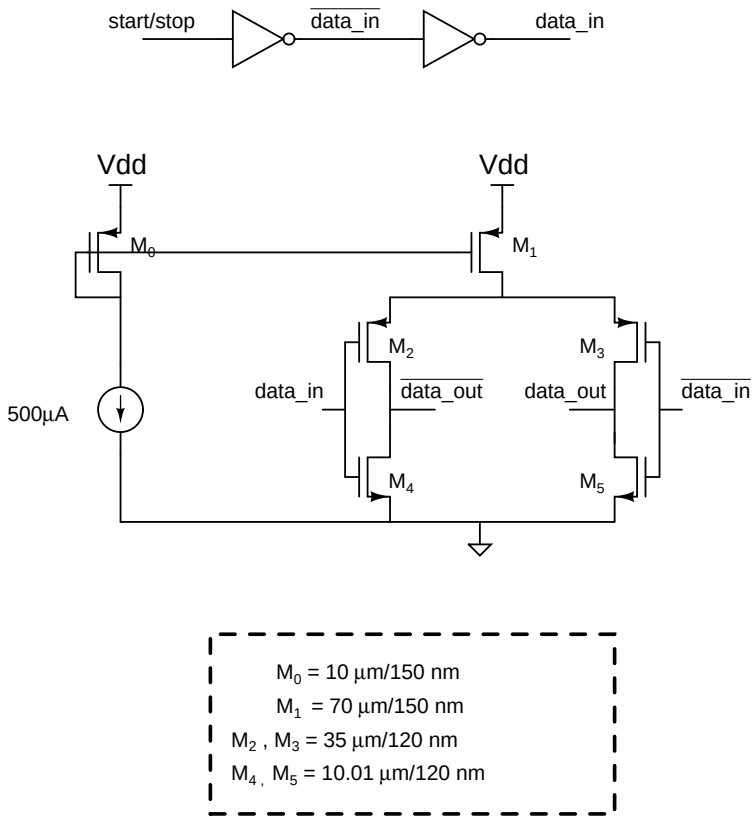


Figure 3.6: LVDS buffer.

CHAPTER 4

Layout and simulation results

4.1 Simulation results

Post layout simulations were done on the delayline of selftest and the fine TDC. The verilog netlist of digital blocks after place and route were simulated in modelsim using ModelsimLib library corresponding to the Faraday library. These netlists were imported to cadence. They were simulated and the functionality was verified using AMS-spectre simulator.

4.1.1 Simulation results for delayline in selftest unit

Initially the DLL was simulated for C-extracted and RC-extracted cases. The value of control voltage after the settling of DLL was found to be 551mV. Ideally,for this value of control voltage, the VCDUs in the delay line should have a delay of 125ps but the delays differ due to mismatch among the delay units. The variation of the delay of each VCDU for C-extraction and RC-extraction is tabulated in Table. 4.1. For making DNL and INL measurements, it is required to vary the delay between start and stop in finer steps for a considerable range. This can be done by varying the control voltage of the delayline. Fig. 4.1 shows how the delay of the delayline varies w.r.t control voltage. From the plot we can see that the delay can be varied from 2ns to 11ns. The fine steps in delay will depend on the fine steps in control voltage.

Table 4.1: Variation in delays of each VCDU in delayline

	C- extraction (in seconds)	RC- extraction (in seconds)
Mean	124.70e-12	124.88e-12
Deviation	2.6068e-12	2.6028e-12
Variance	6.7956e-24	6.7748e-24

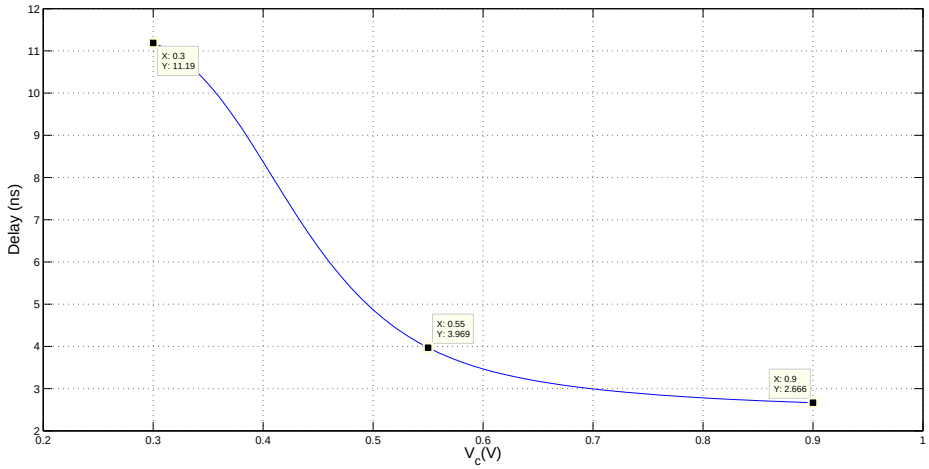


Figure 4.1: Variation of delay with Vc for delay line

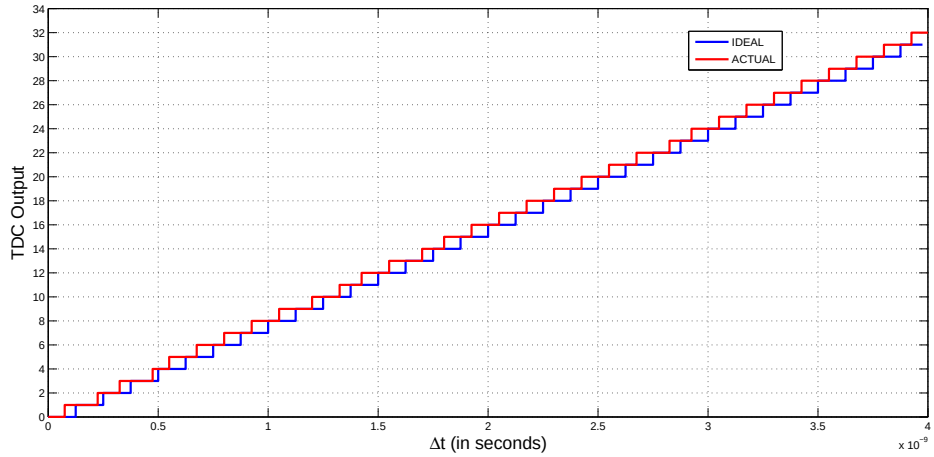


Figure 4.2: TDC characteristics

4.1.2 Simulation results for Fine TDC

The delay between Start and Stop signals is varied from 0 to 4ns in steps of 25ps. The characteristics of fine TDC was plotted as delay vs digital code. It is compared with ideal characteristics. The ideal characteristic has a step width of 125ps and the digital code varies from 0 to 32 for delay between 0 to 4ns as shown in Fig. 4.2. From the plot, maximum DNL error is found to be 0.4 LSB.

4.2 Final layout

The final layout of the chip before tape-out is shown in Fig. 4.3. It occupies an area of one miniasic block i.e. The IO pads used in the padframe are from the libraries

$$FOCOH\_A33\_T33\_ANALOGESD\_IO\_7m1t - 2008Q2v2.2$$

$$FOCOH\_A33\_T33\_GENERIC\_IO\_7m1t - 2009Q1v3$$

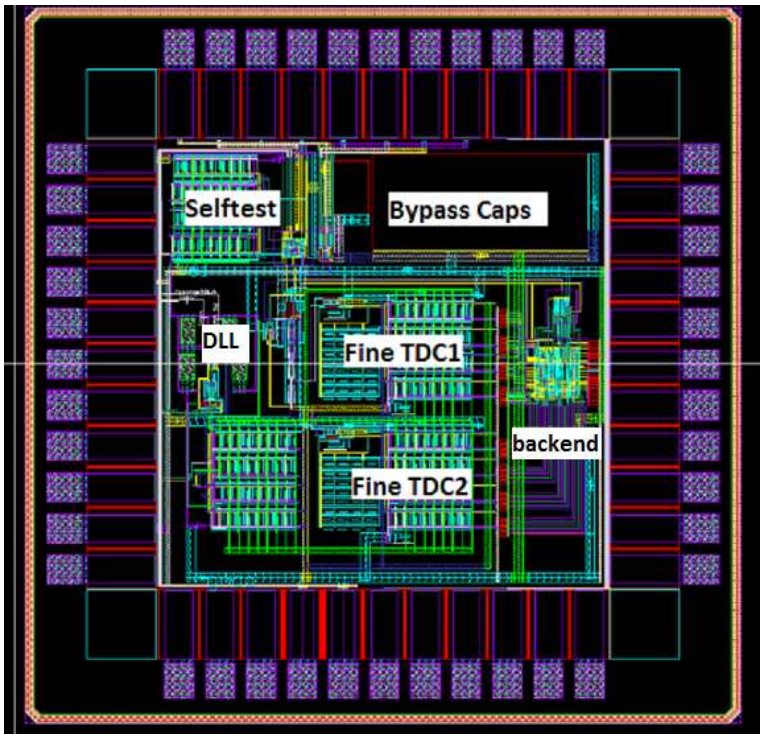


Figure 4.3: Final layout of the TDC.

The layout was checked for DRC and LVS errors using Calibre and Assura tools. The layout was sent for tape out in gdsII format along with electrical rule check (ERC) label file. Some of the ERC warnings were found and these referred to TIE cells in the digital blocks. TIE cells are cells in the standard cell libraries which keep a particular node in the design at logic high or logic low all the time. These warnings were ignored. The fabricated die was packaged using QFN 48 package.

4.3 Bonding Diagram details

- QFN 48 pin package
- 44 pads on chip
- Pin 17 downbonded to cavity
- Pins $6, 18, 30, 42$ are not connected.
- Die size : $1.525\text{mm} \times 1.525\text{mm}$
- Die thickness : $280\mu\text{m}$
- Bond pad pitch : $90.4\mu\text{m}$

- Bond pad opening : $64\mu\text{m} \times 64\mu\text{m}$
- Number of dies packaged : 29

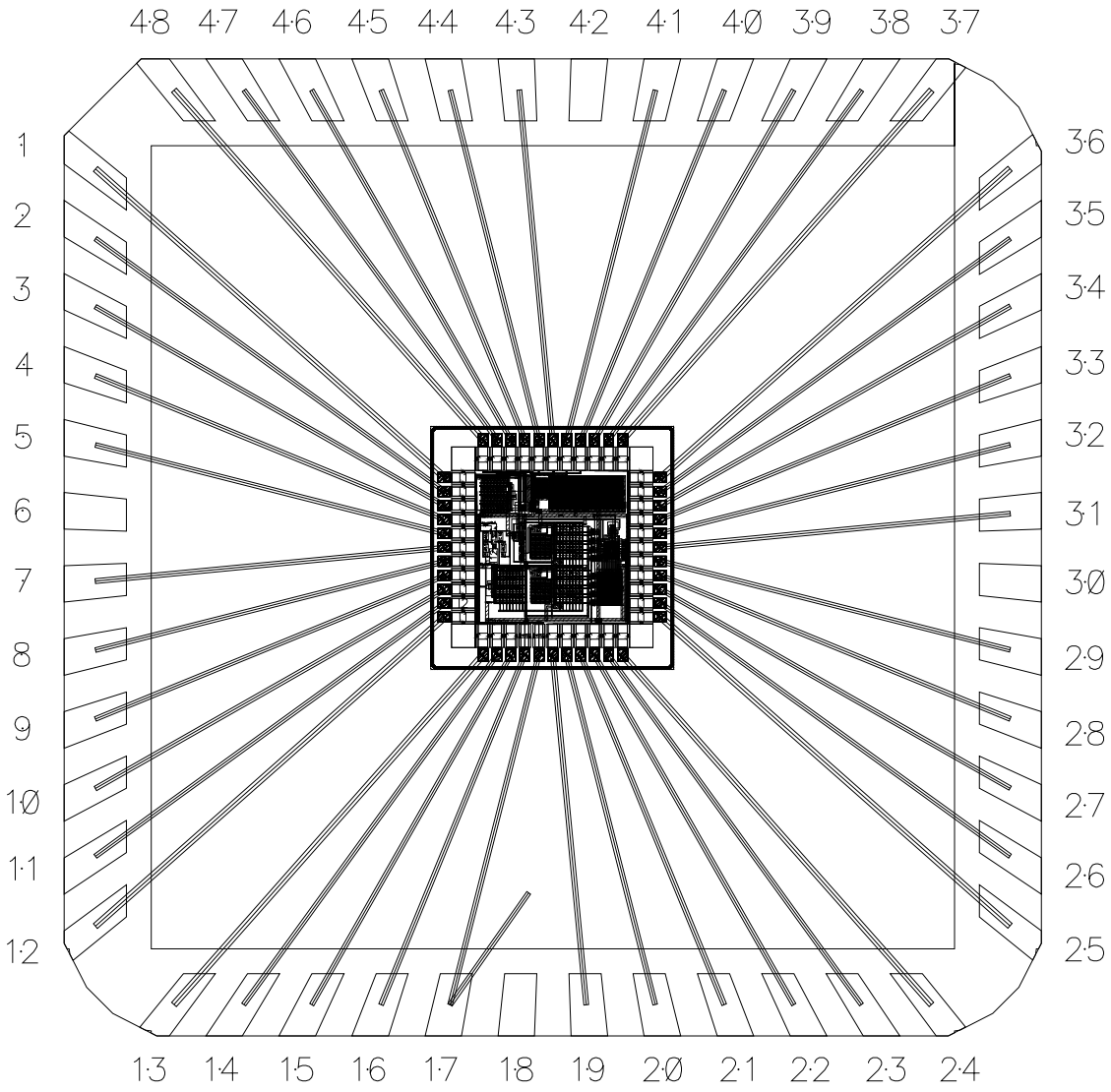


Figure 4.4: Bonding diagram of the chip.

Table 4.2: Detailed chip pin number to package pin number correspondence

Chip pin number	Package pin number	Chip pin number	Package pin number
01	01	23	25
02	02	24	26
03	03	25	27
04	04	26	28
05	05	27	29
06	07	28	31
07	08	29	32
08	09	30	33
09	10	31	34
10	11	32	35
11	12	33	36
12	13	34	37
13	14	35	38
14	15	36	39
15	16	37	40
16	17	38	41
17	19	39	43
18	20	40	44
19	21	41	45
20	22	42	46
21	23	43	47
22	24	44	48

CHAPTER 5

Conclusions and future work

In this project, an existing design of TDC was taken and additions were made to make it a complete TDC system. By simulations, the resolution is found to match the specification of 125 ps. A selftest block in the chip generates start and stop signals internally for testing the chip. The design is verified and taped out in UMC 0.13 μm CMOS process. The chip is packaged using QFN48 package.

5.1 Future work

A PCB has to be designed for testing the chip. The start and stop signals for the chip can be obtained from the selftest block itself. The control voltage input for the selftest can be varied in finer steps to obtain finer delays. The delay between LVDS start and stop outputs should correspond to the output of TDC. By varying delays in finer steps, the DNL and INL measurements can be done.

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