Design of a Decimator, Measurement and Design Improvement of a Delta Sigma Modulator for Audio Bandwidth

A Project Report

submitted by

AJAY EDA

in partial fulfilment of the requirements

for the award of the degree of

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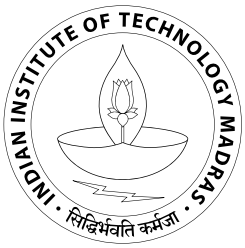

Department Of Electrical Engineering

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CERTIFICATE

This is to certify that the thesis titled **Design of a Decimator, Measurement and Design Improvement of a Delta Sigma modulator for Audio Bandwidth**, submitted by **Ajay Eda**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally, I dedicate this thesis to my favourite actress Smt.Suryakantham(1924 - 1994).

Ajay Eda

ABSTRACT

This project involves the design of a Low power Decimation filter for a 18 bit audio $\Delta\Sigma$ Analog to Digital converter with a sampling frequency of 3.072 MHz. A multistage, multirate approach is used for decimator structure to reduce the order of the filters. Hogenuaer structure is used for SINC section which reduces power consumption. Polyphase decomposition for halfband filter section reduces power consumption approximately by half. The design is implemented in 0.18 μm CMOS process from UMC. The design consumes a total power of about $115\ \mu$W (mostly dynamic power) from a 1.8 V supply.

Other part of this work involves Measurement and fixing the problems of High resolution $\Delta\Sigma$ modulator for audio bandwidth (20 Hz-24 kHz) , which is designed in a 1.8 V, 0.18 μm CMOS process [1]. This work includes changing the DAC structure, implementing the appropriate Dynamic Element Matching technique and also modifications to the first Op-amp. The modulator is designed for an SNR of 108 dB and the simulated SQNR is in excess of 115 dB. The modulator consumes a current of 945.27 μA from a supply of 1.8 V

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ABBREVIATIONS

ADC	Analog to Digital Converter
CAD	Computer Aided Design
CIFB	Cascade of Integrators Feedback
CIFF	Cascade of Integrators Feed Forward
CMOS	Complementary Metal Oxide Semiconductor
CSD	Canonical Signed Digits
CTDSM	Continuous-Time Delta Sigma Modulator
CTS	Clock Tree Synthesis
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non Linearity
DR	Dynamic Range
DSP	Digital Signal Processor
DWA	Data Weighted Averaging
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
INL	Integral Non Linearity
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSA	Maximum Stable Amplitude
NRZ	Non Return to Zero
OBG	Out of Band Gain

OSR	Oversampling Ratio
Op-amp	Operational Amplifier
PSD	Power Spectral Density
PCB	Printed Circuit Board
RTL	Register Transfer Level
RCx	Resistor Capacitance Extraction
RTZ	Return to Zero
RZ	Return to Zero
SDR	Signal to Distortion Ratio
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
SoC	System on Chip
UGF	Unity Gain Frequency
VCD	Value Change Dump

CHAPTER 1

Introduction

There has been a huge emphasis on System on a Chip (SoC) designs over the last decade. In SoCs, all components of an electronic system are integrated into a single chip. E.g. Mobile phone, personal media players, routers. Data and signal processing in such a system is mostly digital in nature. Digital signals are immune to noise, can be stored easily and are easier for processing. A typical SoC contains a core Digital Signal Processor (DSP) for digital data/signal processing, memory blocks to store data, phase locked loops to control timing and data converters (Analog to digital converters, ADCs, and digital to analog converters, DACs) to interface with the real world.

An ADC is characterized by its resolution, speed and power. The design described in this thesis lays emphasis on high resolution and low power. High resolution data converters are used in seismic monitoring, high fidelity audio, high accuracy instrumentation like strain gauges, pressure sensors. $\Delta\Sigma$ ADCs can resolve signals as high as 20 bits in audio bandwidths. $\Delta\Sigma$ ADCs are a class of oversampled converters wherein high resolution is obtained by virtue of oversampling and negative feedback that shapes the quantization noise out of the signal band. A $\Delta\Sigma$ modulator encodes the analog signal with a smaller number of bits (1-4) at the oversampled rate. A decimator (decimation filter) is required to remove the out-of-band noise to a sufficient level and achieve the full resolution at the Nyquist rate of the signal.

This thesis aims at building the components of a $\Delta\Sigma$ data conversion system for audio bandwidth with a low power consumption. Very low power (90 μW), high resolution (15 bit) $\Delta\Sigma$ modulators for digital audio have already been proposed in [2][3]. This necessitates a decimator with a correspondingly low power in order to realize a low power analog to digital data conversion system.

The first part of the thesis deals with the design of a low power decimator for a power optimized continuous-time $\Delta\Sigma$ modulator for digital audio. The second part of the thesis deals with the Measurement and design improvement of a very high resolution, 18 bit (108 dB SNR), continuous-time $\Delta\Sigma$ modulator in the bandwidth 20 Hz - 24 kHz.

1.1 Organization of the thesis

Chapters 2 - 4 form the first part of the thesis about the decimator.

Chapter 2 gives a brief introduction to the concepts of decimation and the design targets for the decimator.

Chapter 3 describes the architecture of the decimator and contains the description of various blocks in the decimator.

Chapter 4 gives information about the digital synthesis of the decimator using standard cells and CAD tools. The simulation results are given in this chapter and concludes the first part.

Chapter 5 gives the measured results from the fabricated $\Delta\Sigma$ modulator chip [1].

Chapter 6 describes the issues that are found in the earlier design [1].

Chapter 7 describes Design improvement techniques and gives the simulation results.

Chapter 8 draws some conclusions from this work.

CHAPTER 2

Introduction to decimators

2.1 $\Delta\Sigma$ modulation

$\Delta\Sigma$ modulators are a class of data converters wherein the signal is oversampled and the quantizer is placed inside a negative feedback loop. The factor by which the sampling frequency (f_s) is greater than the Nyquist rate of the signal (f_{nyq}) is termed as oversampling ratio, OSR=$\frac{f_s}{f_{nyq}}$. Delta-sigma ($\Delta\Sigma$; or sigma-delta, $\Sigma\Delta$) modulation is a method for encoding high-resolution or analog signals into lower-resolution digital signals. The conversion is done using error feedback, where the difference between the two signals is measured and used to improve the conversion. The low-resolution signal typically changes more quickly than the high-resolution signal and it can be filtered to recover the high-resolution signal with little or no loss of fidelity. This technique has found increasing use in modern electronic components such as converters, frequency synthesizers, switched-mode power supplies and motor controllers. Figure 2.1 shows the block diagram of a discrete-time $\Delta\Sigma$ modulator. Both analog-to-digital converters

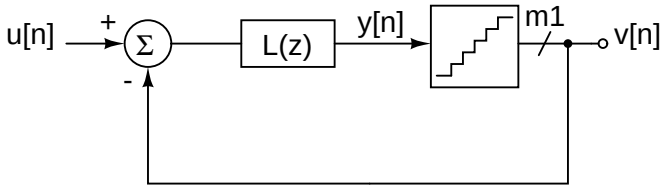

Figure 2.1: Block diagram of a discrete-time $\Delta\Sigma$ modulator.

(ADCs) and digital-to-analog converters (DACs) can employ delta-sigma modulation. A delta-sigma ADC first encodes an analog signal using delta-sigma modulation and then applies a digital filter to form a higher-resolution digital output. On the other hand, a delta-sigma DAC encodes a high-resolution digital input signal into a lower-resolution

signal that is mapped to voltages and then smoothed with an analog filter. In both cases, the temporary use of a lower-resolution signal simplifies circuit design and improves efficiency.

A continuous-time $\Delta\Sigma$ modulator (CTDSM) employs a continuous-time loop filter and the sampling is done within the loop. The loop filter also behaves as an anti-aliasing filter [4]. Figure 2.2(a) shows the block diagram of a continuous-time $\Delta\Sigma$ modulator. The quantizer is modeled as an additive noise source at the input of the quantizer. Figure

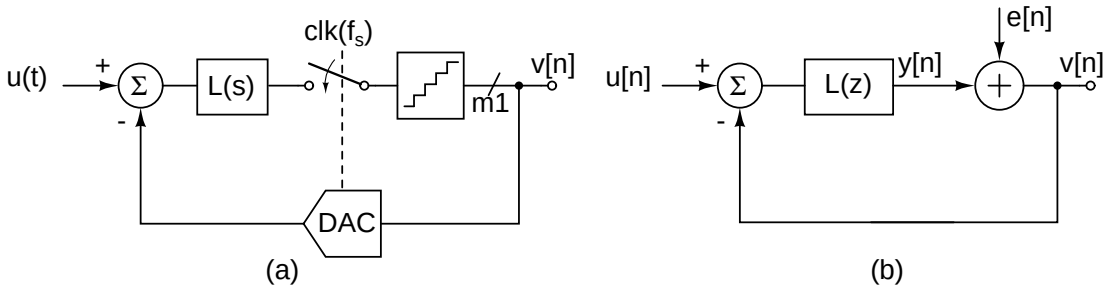

Figure 2.2: CTDSM (a) Block diagram, (b) Discrete time equivalent with additive quantization noise model.

2.2(b) shows the additive noise equivalent. The quantization noise is assumed to be white and possess a uniform distribution. Denoting the quantization noise by $e[n]$, the input signal by $u[n]$ and the output signal by $v[n]$, the transfer function from input to the output of the quantizer is written as

$$V(z) = \frac{L(z)}{1+L(z)} \times U(z) + \frac{1}{1+L(z)} \times E(z) \quad (2.1)$$

$$= \mathrm{STF} \times U(z) + \mathrm{NTF} \times E(z) \quad (2.2)$$

where STF (Signal transfer function) denotes the transfer function from the input signal to the modulator output. NTF (Noise Transfer function) denotes the transfer function from the quantization noise to the modulator output. They are expressed as

$$\mathrm{STF(z)} = \frac{V(z)}{U(z)} = \frac{L(z)}{1+L(z)} \quad (2.3)$$

$$\mathrm{NTF(z)} = \frac{V(z)}{E(z)} = \frac{1}{1+L(z)} \quad (2.4)$$

Usually a coarse quantizer of 1 to 4 bits resolution is used. The order of the modulator is same as the order of the loop filter. The NTF is designed to shape the quantization noise out of the signal band by appropriately choosing the loop filter. A typical spectrum of the output of a $\Delta\Sigma$ modulator in response to a sine wave input is shown in Figure 2.3. The quantization noise is high pass shaped by the loop filter. The in-band signal

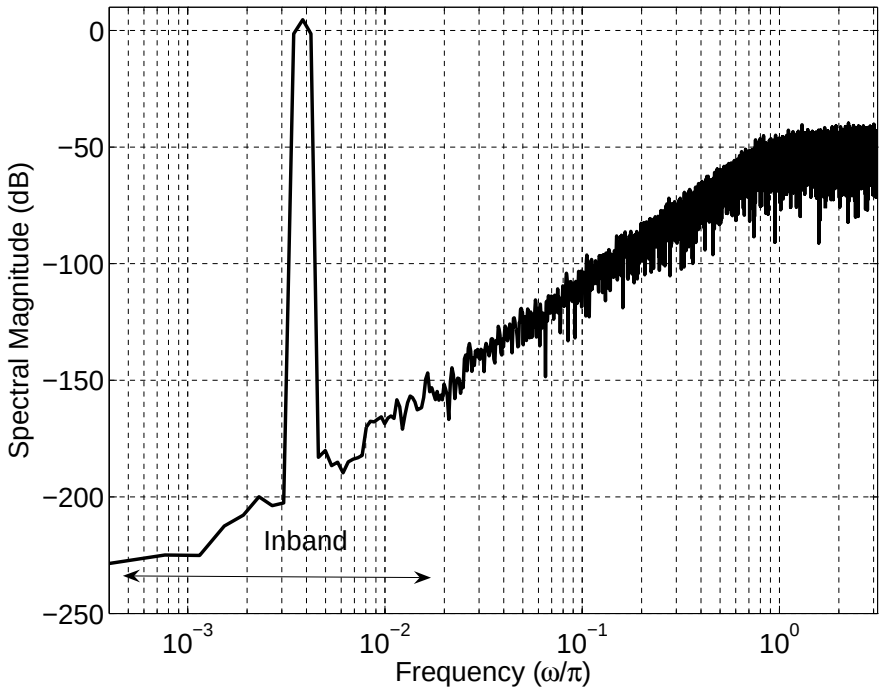

Figure 2.3: Spectrum of a $\Delta\Sigma$ modulator, Order: 3, OSR: 64.

to noise ratio (SNR) of the spectrum is 118 dB. Higher order modulators and higher quantizer resolutions are used to obtain higher resolution for $\Delta\Sigma$ modulators [4].

2.2 Decimation Filter

2.2.1 Introduction

In $\Delta\Sigma$ modulators the quantization noise is shaped out of the passband as shown in Figure 2.4, a low pass filter(LPF) is required to remove the out of band components and a decimator is needed to the bring the sampling rate back to the Nyquist rate from the oversampled rate. Both these tasks are performed by a decimation filter, which as its

name suggests, low pass filters and decimates (brings down the sampling rate) the input signal.

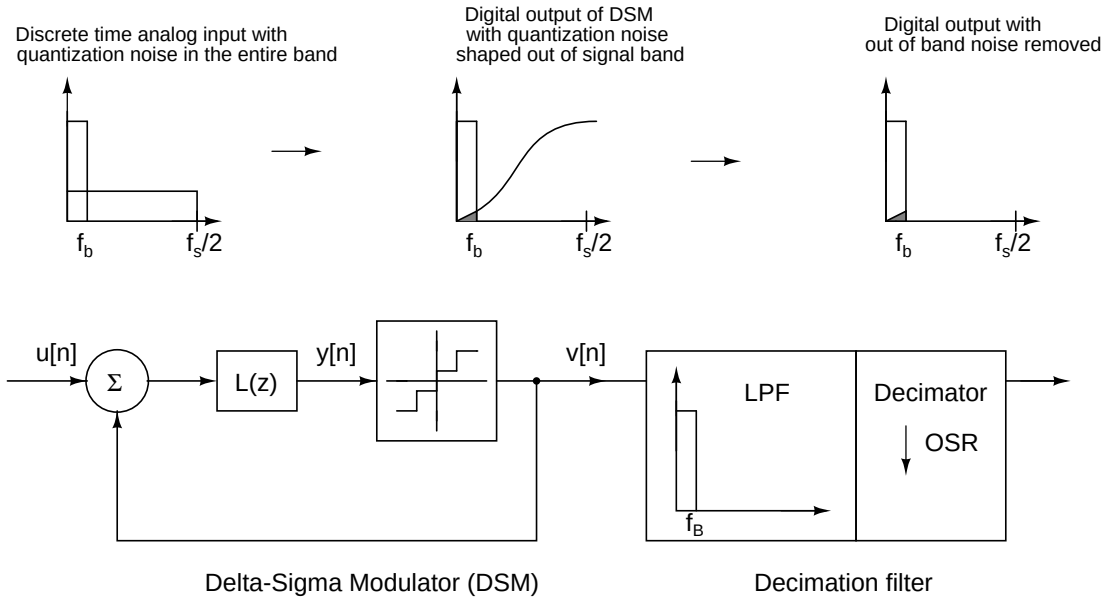

Figure 2.4: Block diagram of decimation filter for a modulator. f_b is the maximum inband frequency. OSR = Oversampling ratio.

Without losing any information in oversampled signals as many samples can be left out until the signal is not oversampled any more. The oversampling sigma-delta modulation is a proven method to realize high and very high-resolution analog to digital converters. Because of the use of oversampling in sigma-delta modulators, the need arises for changing the sampling rate of signal, decreasing it to Nyquist rate in A/D-converters. Thus, the high resolution can be achieved by the decimation (sample reduction). Such sample reduction can be achieved employing high precision FIR filters, usually in cascaded structures. In most of the communication device, we will implement a decimator filter to reduce the data rate in order to reduce the dynamic power consumption.

2.2.2 Downsampling

To recover any sampled signal it is enough if we sample it to its Nyquist rate. In $\Delta\Sigma$ modulators, since the output is oversampled there is a need to reduce the data rate of the output of the $\Delta\Sigma$. Downsampling means reducing the sampling rate. This is done by

dropping the samples of a discrete-time signal. Downsampling by a factor of M implies that out of M consecutive samples, $M-1$ samples are discarded and one sample is retained. Correspondingly the sampling rate of the downsampled signal changes from f_s to f_s/M. This is shown in Figure 2.5.

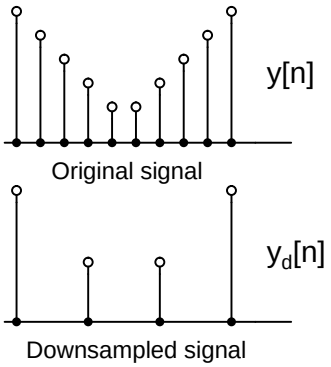

Figure 2.5: Illustration of downsampling by a factor of three.

Mathematically downsampling by a factor of M is expressed as

$$y_d[n] = y[Mn] \tag{2.5}$$

Let $Y(e^{j\omega})$ and $Y_d(e^{j\omega})$ denote the spectrum of the signal $y[n]$ and $y_d[n]$ respectively. The spectrum of the downsampled signal can be written as, [5]

$$Y_d(e^{j\omega}) = \frac{1}{M}\sum_{k=0}^{M-1} Y\left(e^{j\frac{\omega-2\pi k}{M}}\right) \tag{2.6}$$

In the below figure 2.6 the spectrum of downsampled signal and the original one are compared. We can see from the 2.6, that the spectrum of the downsampled signal is expanded. So it may result in aliasing. To prevent the signal, $Y(e^{j\omega})$ has to be restricted to $\frac{\pi}{M}$ or $\frac{f_s}{2M}$. Hence a digital anti-alias filter is necessary to filter out the components that alias into this band. In general, the operation of reducing the sampling rate including any prefiltering will be called downsampling. The block level representation of a decimator which down samples by a factor of M is shown Figure 2.7.

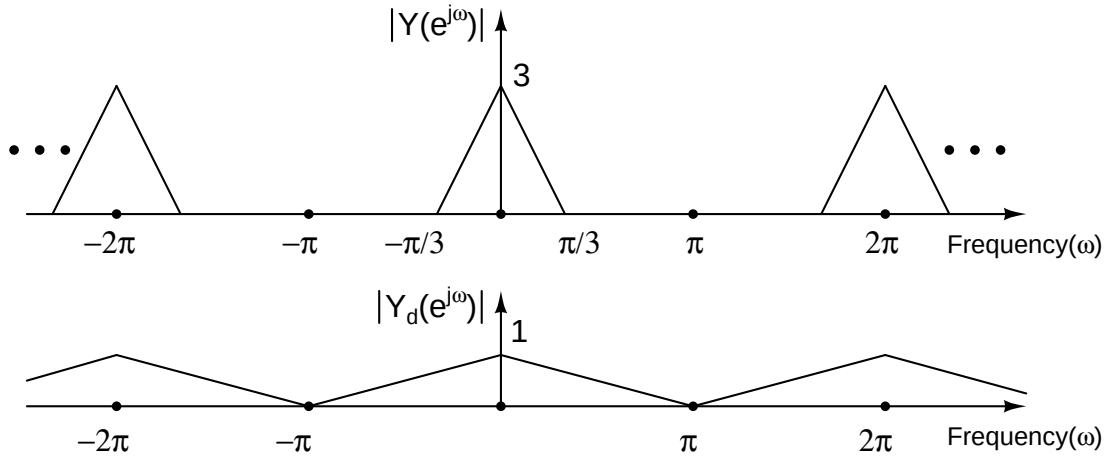

Figure 2.6: Spectrum of the downsampled signal when $M = 3$.

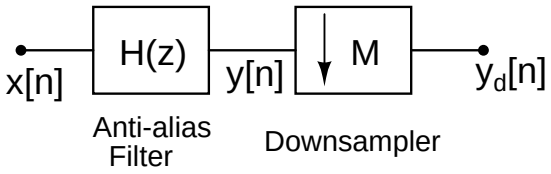

Figure 2.7: A decimator that down samples by M.

2.3 Design targets for the decimator

The decimator described in this thesis is designed for a continuous-time $\Delta\Sigma$ modulator [2] that was designed in a 0.18 μm CMOS process with 1.8 V supply. It was four bit modulator that has an OSR of 64 and operates at the sampling frequency, $f_s = 3.072$ MHz. The modulator has an SNR of 108 dB in the bandwidth 20 Hz to 24 kHz. The characteristics of the $\Delta\Sigma$ modulator and the requirements of the decimator are tabulated in Table 2.1 and Table 2.2 respectively.

Table 2.1: Modulator characteristics

Sampling rate	3.072 MHz
OSR	64
Nyquist rate	48 kHz
Modulator order	3
SNR(20 Hz-24 kHz)	108 dB
Technology	0.18μm CMOS

Table 2.2: Decimator requirements

No. of input bits	4
Input rate	3.072 MHz
Output rate	48 kHz
SNR	18 bits (108 dB)
Passband edge	21.6 kHz
Passband ripple	$< \pm 0.05$ dB

CHAPTER 3

Architecture of the decimator

3.1 Cascade of decimation filter

The main aim of the decimator is to attenuate the aliasing noise before downsampling so that the in-band signal to noise ratio (SNR) is not degraded. The relative bandwidth of a digital signal is defined as the ratio of the bandwidth of the signal to half the sampling rate, from a $\Delta\Sigma$ modulator is $1/(2\mathrm{OSR})$. An ideal anti-alias filter accompanying the decimator has the following characteristics.

$$H(f) = \begin{cases} 1 & 0 \leq f \leq 1/(2\ \mathrm{OSR}) \\ 0 & 1/(2\ \mathrm{OSR}) < f \leq 1/2 \end{cases} \tag{3.1}$$

But all practical filters have a certain transition band width and its stop band gain is not zero. The anti-alias filter to be realized for the decimator needs to have narrow transition band. Such a filter if realized as a single filter has a very high order ($>$1000) [6]. A high order filter operating at a high frequency consumes a very high power.

Therefore, instead of using a single anti-alias filter operating at the input sampling rate and then downsampling to the Nyquist rate, filtering and downsampling is done in multiple stages. This is termed as multistage decimation [6][7]. According to (2.6), when a signal of bandwidth f_b is downsampled from a sampling rate f_s to f_s/M, the aliasing region lies centered at $k\frac{f_s}{M}$ with a bandwidth of $2f_b$. Here k takes values 0,1,2...$\lceil M/2 \rceil$ where $\lceil\ \rceil$ denotes the ceiling function. It is ensured that in each stage, the noise in these aliasing bands are sufficiently attenuated by the filter that precedes the downsampling. The block diagram of this decimator employing multistage decimation is shown Figure 3.1.

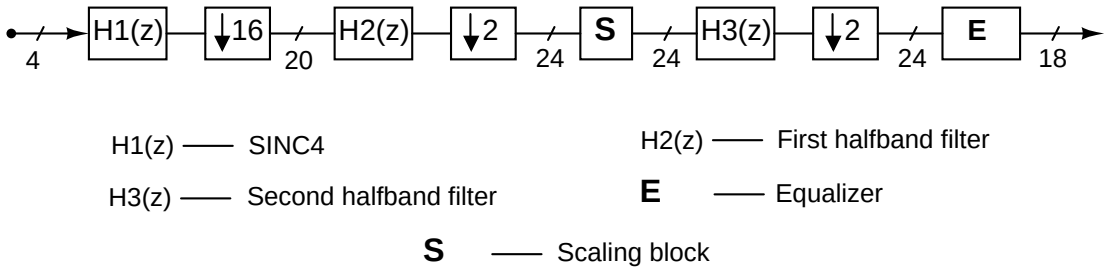

Figure 3.1: Block diagram of the multistage decimator.

The multistage decimator employs three stages of anti-alias filtering. The overall downsampling factor of sixty four is divided as 16, 2, 2 in these three stages [8]. The first stage filter before the initial downsampling (16) is a cascade of four moving average filters (SINC4 filter). This filter operates at the maximum rate, f_s. A moving average filter can be implemented with only adders (without coefficient multipliers) and helps in saving power [9]. The remaining filtering is done with halfband filters and a downsampling factor of two is employed after each filter [7]. The droop caused by the SINC4 filter is corrected by the equalizer. The scaling block restores the signal to fullscale of the $\Delta\Sigma$ modulator. It is intended to have linear phase response for the decimator, hence all filters used in this design have symmetric finite impulse response (FIR) characteristics. Each block and its implementation is described in detail in the rest of this chapter.

3.2 SINC4 filter

It is well known that SINC filter is very efficient for the first stage in decimation filter because of its inherent large attenuation.The simplest form of digital low pass filtering is averaging N consecutive samples. Averaging N samples is done with a moving average filter/SINC filter. A CIC filter is a special class of linear phase, finite impulse response (FIR) filter. CIC filters do not require multipliers and use a limited amount of storage. Therefore, CIC filters are more efficient than conventional FIR filters, especially in fixed-point applications. Furthermore, it can be used to decimate the data by large factor, allowing easier implementation of following stages. The transfer function of an

N tap moving average filter is

$$H(z) = 1 + z^{-1} + z^{-2} + z^{-3} + \ldots + z^{-(N-1)} \tag{3.2}$$

SINC filters can be cascaded so that the attenuation in the stop band can be increased. Since a third order $\Delta\Sigma$ modulator shapes the quantization noise at its output as $(1 - z^{-1})^3$ [4]. Hence the quantization noise power spectral density increases with frequency as f^3. Sufficient attenuation of the shaped quantization noise over the entire band is possible with a cascade of four SINC filters (SINC4) that has a $\frac{1}{f^4}$ roll off [10]. The variation of maximum passband droop value and worst alias rejection for different N values is summarized in Table 3.1. As the number of samples for averaging N increases, the worst alias rejection become better but the passband droop will increase. Usually a maximum passband droop of 3 dB or above is difficult to correct. So it is clear from the above table 3.1 that the fourth order 16 tap SINC filter can be used at the first stage of decimation filter.The frequency response of the cascade of four sixteen tap SINC filters (SINC4) is shown in Figure 3.2. The shaded areas in the frequency response are the noise aliasing bands for the SINC4 filter. The signal is downsampled from 3.072 MHz to 192 kHz by a factor of sixteen after the first stage filtering. According to (2.6) the alias bands are located at integer multiples of $\frac{f_s}{16}$. The tap length of the SINC filter was chosen as $N = 16$ so that the complex zeros that creates nulls are located at the center of these alias bands.

Table 3.1: Variation of maximum droop and worst alias rejection for different N values

Number of samples for averaging	**Passband droop(in dB) at 24 KHz**	**Worst alias rejection(in dB) at 168(192-24) KHz**
N = 16	-0.8941	-67.57
N = 32	-3.6410	-70.51
N = 64	-15.7000	-83.06

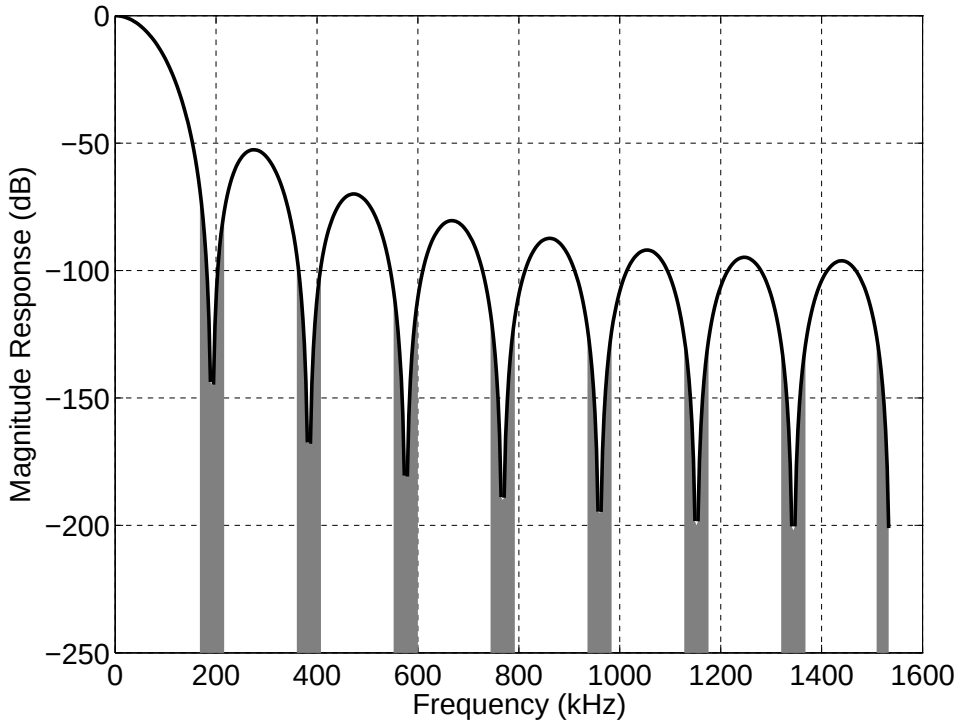

Figure 3.2: Frequency response of the SINC4 filter(aliasing bands in gray).

3.2.1 Hogenauer structure

By simplifying the equation (3.2) we will get

$$H1(z) = \left[\frac{1-z^{-16}}{1-z^{-1}}\right]^4 = \left[\frac{1}{1-z^{-1}}\right]^4 \left[1-z^{-16}\right]^4 \tag{3.3}$$

$H1(z)$ along with the downsampling of sixteen is implemented in two steps as shown

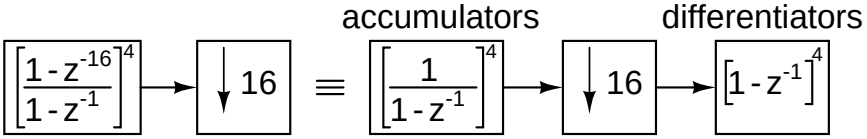

Figure 3.3: Implementation of SINC4 as Hogenauer structure.

in Figure 3.3. At first, the accumulation operations $\left(\frac{1}{1-z^{-1}}\right)^4$ are done at the rate f_s. Then, the operation $[1-z^{-16}]^4$ and the downsampling of sixteen are implemented with cascade of four differentiators $(1-z^{-1})$ working at $f_s/16$. This structure is called Hogenauer structure [9].

3.2.2 Pipelining and retiming of SINC4

The accumulators are first pipelined by inserting a register at the input of each accumulators as shown in Figure 3.4. The registers are then retimed to a single register in the forward path of each accumulators [11]. Hence the glitches in combinational adders in one accumulator are prevented from propagating to the next accumulator, thereby reducing unwanted switching power.

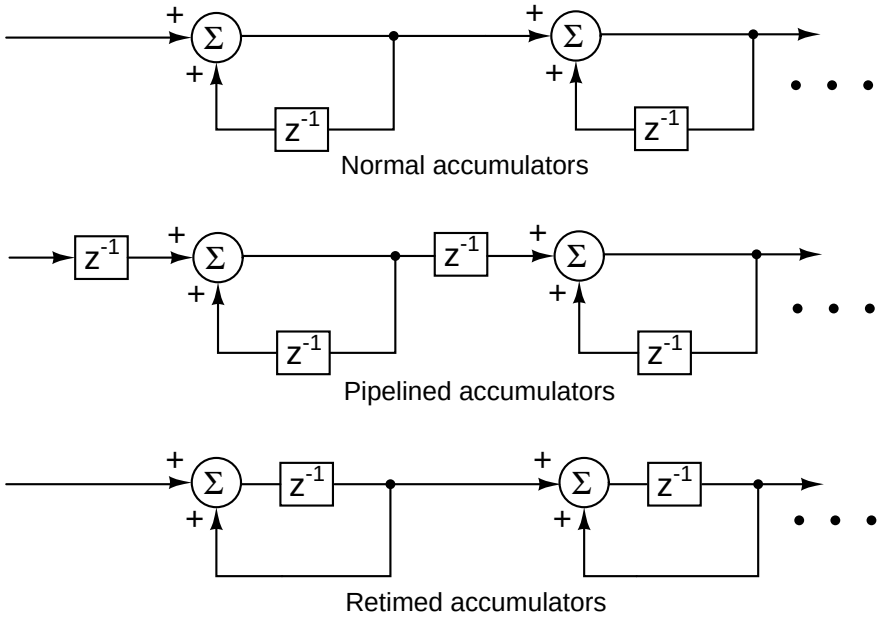

Figure 3.4: Retiming and pipelining of accumulators for power reduction.

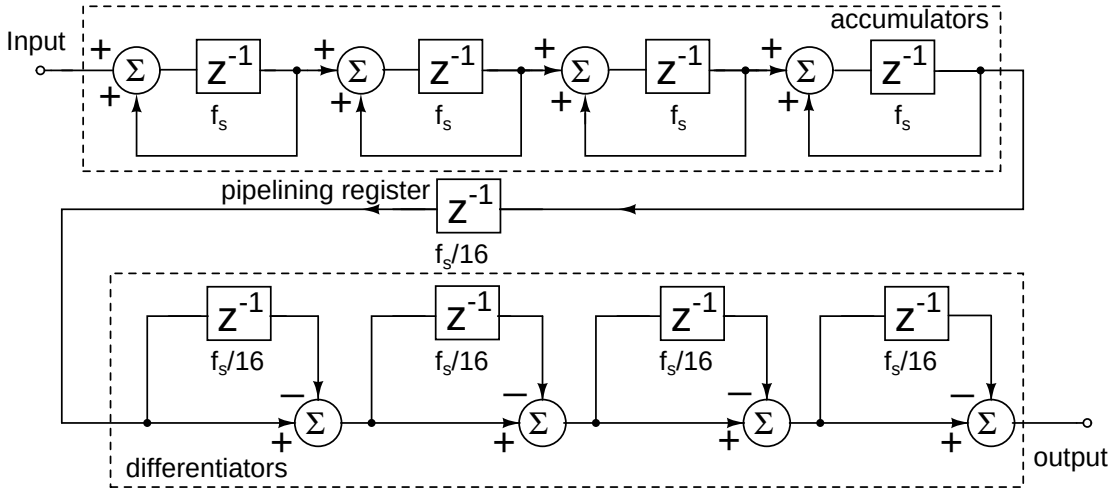

Figure 3.5: Implementation of the SINC4 filter.

Similarly the pipelining register at the output of the fourth accumulator (refer Figure

3.5) prevents the switching data at f_s propagating through the differentiators. It is determined through simulations that retiming of the registers in the accumulators and the pipelined register saves 46 % of power in the SINC4 stage [8]. Overflow in the accumulators does not cause signal distortion if the signal representation is based on wrap around arithmetic (binary, 2's complement) and all register widths are chosen according to the relationship [9].

$$\text{Bit width} \; = \; B_{in} + k \, log_2 N \tag{3.4}$$

Here B_{in} is the input bit width (4 bit binary), k (4) is the number of cascaded SINC stages and N (16) is the tap length of the SINC. Hence all the registers are chosen to be 20 bit wide.

3.3 Halfband filters

Halfband filters are a class of equiripple FIR filters, where the transition region is centered at one quarter of the sampling rate, or f_s/4. Specifically, the end of the passband and the beginning of the stopband are equally spaced on either side of f_s/4. In other words filter exhibits a symmetry with respect to halfband frequecy f_s/4 or $\frac{\pi}{2}$. An important property of the halfband filter is that about 50% of coefficents are zero. This reduces the number of multiplications required in its implementation. The order of the filter N_{ord} = 4P+2 [8], where P ε 1,2,3 ....

- $\frac{N_{ord}}{2}$-1 coefficients are zero.
- Middle coefficient is always 0.5.
- Remaining $\frac{N_{ord}}{2}$+1 coefficients are symmetric about the middle coefficient

Halfband filter have their 6 dB frequency at 0.25*f_s. Hence maximum downsampling that is allowed after filtering is two.

Two halfband filters along with the downsampling by a factor of two after each filter downconverts the signal to its Nyquist rate. The orders of the halfband filters are chosen

such that the overall passband ripple of the decimator is constrained to ± 0.05 dB and the aliasing noise does not cause degradation in the in-band SNR.

3.3.1 Halfband filter-1

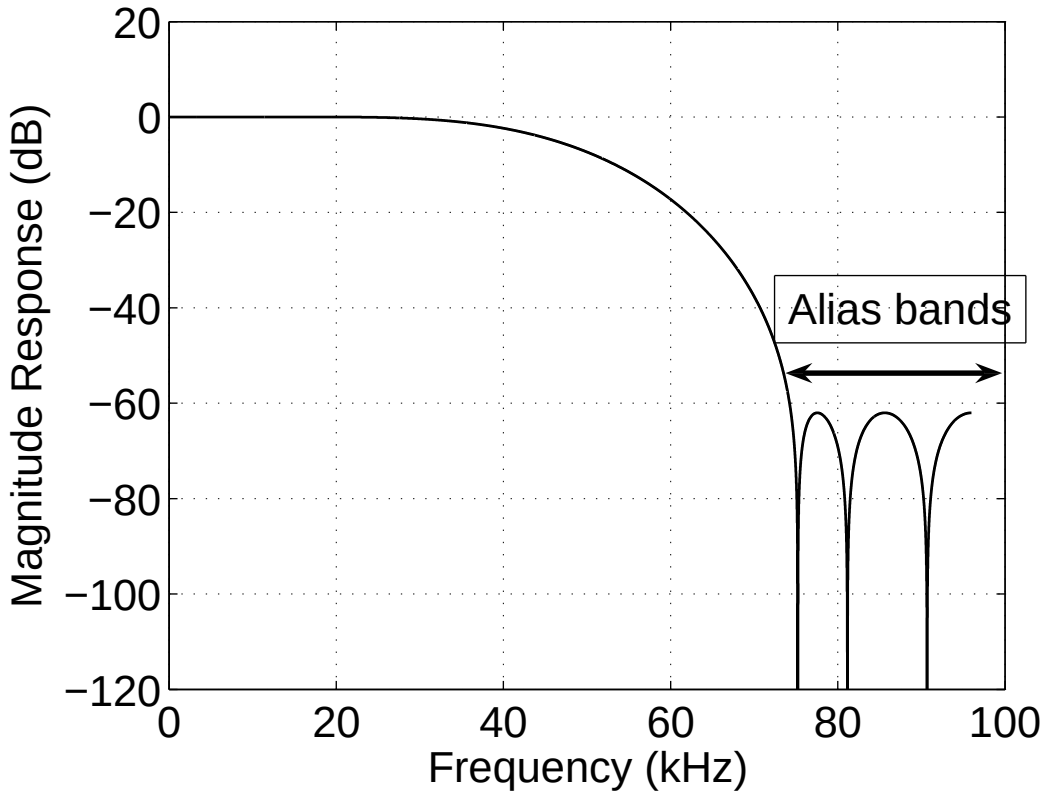

Figure 3.6: Frequency response of the first halfband filter.

The frequency response of the first halfband filter is shown in Figure 3.6.The signal at the output of the SINC4 filter is at four times the Nyquist rate (192 kHz).The first halfband filter is chosen to have a wide transition band. A tenth order halfband filter that has a stop band attenuation of 60 dB is chosen [8]. This filter operates with the clock frequency of 192 kHz. The aliasing band lies in the region 72 kHz to 96 kHz.

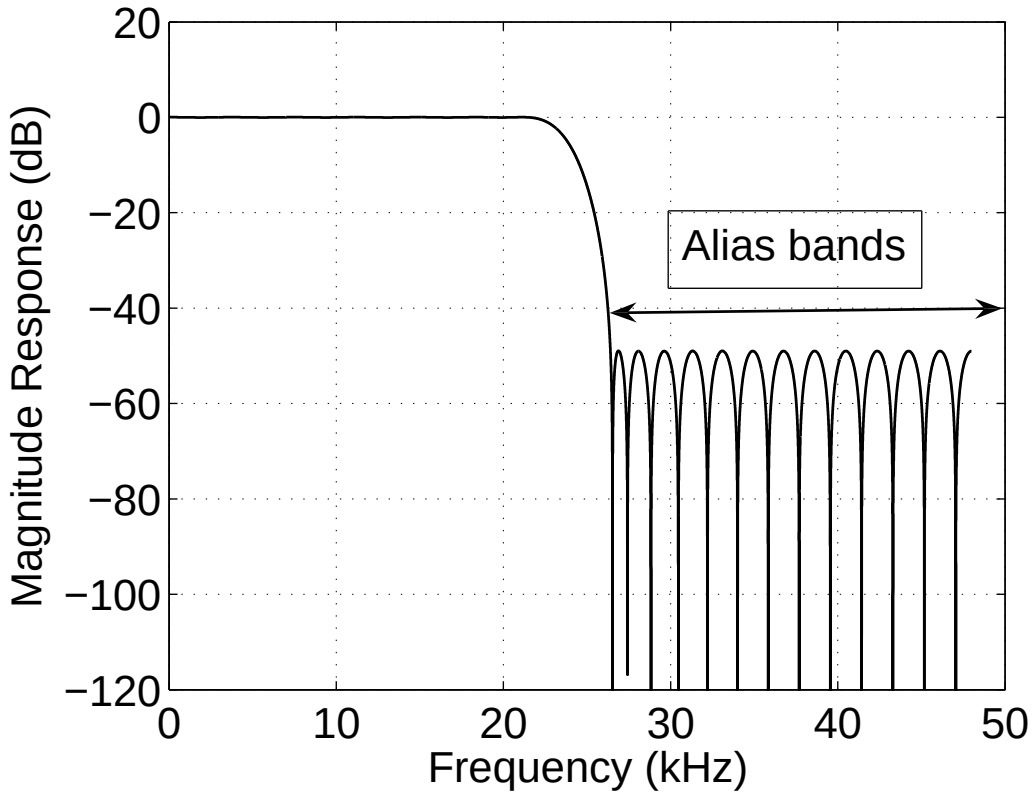

Figure 3.7: Frequency response of the second halfband filter.

3.3.2 Halfband filter-2

. The frequency response of the second halfband filter is shown in Figure 3.8. The second halfband filter provides the final filtering before the signal is downsampled to its Nyquist rate (48 kHz). The filter is designed to have a narrow transition band and a stop band attenuation of 50 dB. A fiftieth order filter is chosen. This filter operates with the clock frequency of 96 kHz. The aliasing band lies in the region 24 kHz to 48 kHz. The frequency response of the first and the second halfband filters are shown in Figure 3.8. The aliasing bands of each downsampling operation is shaded gray.

3.3.3 Implementation of the halfband filters

This section deals with various optimization techniques that are implemented in the halfband filters which aid reduction of power and hardware. The three techniques that

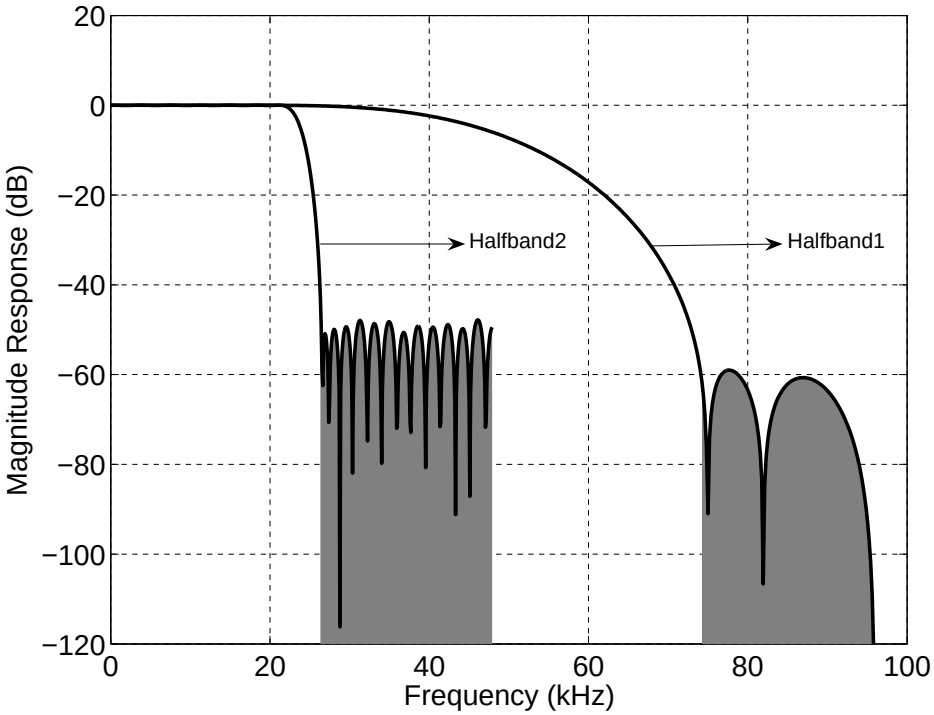

Figure 3.8: Frequency response: The first and the second halfband filters.

are employed in halfband filters are

1. Polyphase structure [8]
2. Canonical signed digits encoding [8]
3. Optimal data width in arithmetic units [8]

The signal in halfband filters and subsequent other blocks are encoded in 2's complement.

3.3.3.1 Polyphase structure

The ployphase decomposition of a sequence is obtained by representing it as a superposition of M subsequences,each consisting of every M^{th} value of successively delayed versions of the sequence. When this decomposition is applied to a filter impulse response, it can lead to efficient implementation structures for linear filters in several contexts. Any filter followed by downsampling can be implemented as a polyphase structure [5][11]. The input data stream is split into multiple phases. The filter transfer function is also split into multiple parts and each transfer function operates on each

phase of the signal. Outputs from all these phases are combined to produce the filtered and downsampled version of the signal. Each individual phase operates at the downsampled rate and hence the effective frequency of operation of the filter is reduced thereby saving power.

Implementation of a halfband filter as a polyphase structure is explained by the following illustration. Let the filter transfer function be $G(z)$ and the downsampling factor be two. Let $G(z)$ be represented as

$$G(z) = \sum_{i=0}^{L} a_i z^{-i} \tag{3.5}$$

The transfer function is split into two phases as given in (3.6).

$$\begin{aligned} G(z) &= \left\{a_0 + a_2 z^{-2} + a_4 z^{-4} + \ldots + a_L z^{-L}\right\} + \\ &\quad z^{-1}\left\{a_1 + a_3 z^{-2} + a_5 z^{-4} + \ldots + a_{L-1} z^{-(L-2)}\right\} \\ &= G_e(z) + z^{-1} G_o(z) \end{aligned} \tag{3.6}$$

Polyphase implementation of the filtering and downsampling is explained in Figure 3.9.

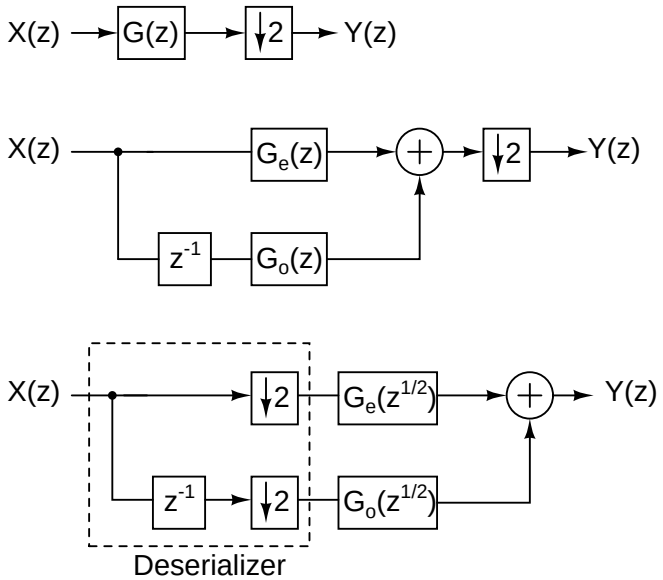

Figure 3.9: Polyphase structure in halfband filters.

The circuit that splits the input data into odd and even data streams is shown in Figure 3.10. It can be seen that the filters $G_e(z^{1/2})$ and $G_o(z^{1/2})$ work at half the clock rate.

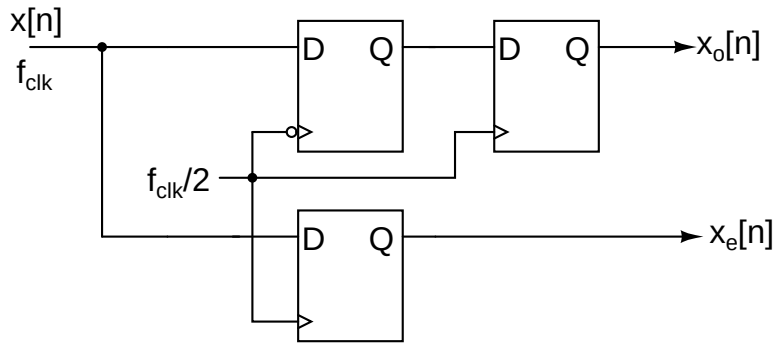

Figure 3.10: Deserializer: Splits data into even and odd streams.

3.3.3.2 Canonical Signed Digits

In a binary representation of a number, digits are either 0 or 1. In signed digit representation of binary numbers, digits belong to the triplet $\{$-1,0,1$\}$. Signed digit representation of a number is not unique [12]. For example, the number 7 can be written in following ways in signed digit representation.

$$\begin{aligned}
(0 \quad 1 \quad 1 \quad 1)_2 &= 7 \\
(1 \quad 0 \quad -1 \quad 1)_2 &= 7 \\
(1 \quad -1 \quad 1 \quad 1)_2 &= 7 \\
(1 \quad 0 \quad 0 \quad -1)_2 &= 7
\end{aligned}$$

Encoding a binary number in signed digits representation such that it contains the fewest number of non-zero bits is called canonical signed digit (CSD) [13]. Hence encoding the tap weights of a filter in CSD reduces the number of multiplication operations that saves hardware and power. Unlike the signed digit representation, the CSD representation of a number is unique.

The CSD representation is also applicable for fractional numbers. For e.g. $0.4375 = 2^{-1} - 2^{-4}$. Truncation of tap weights to finite number of CSD alters the frequency

response of the filter. The number of CSDs in tap weights is decided by the accuracy of the frequency response (passband ripples). In this decimator design, the tap weights are fourteen bits wide.

3.3.3.3 Data width in halfband filters

In order to ensure proper filtering of the quantization noise in halfband filters, the digital signal should support adequate dynamic range. More the number of bits in the filtering operation, higher is the dynamic range of the filtered signal. A high dynamic range filtering is required to ensure adequate suppression of the noise in the aliasing bands. The minimum number of bits required is explained with the help of Figure 3.11.

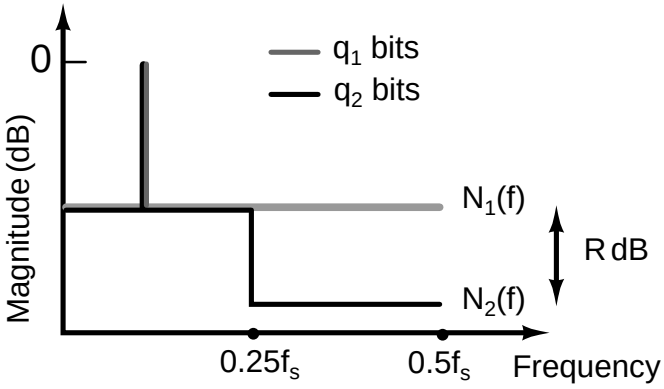

Figure 3.11: Filtering of quantization noise floor.

The quantization noise Power spectral density (PSD) of a digital signal, with fullscale 0 dB, quantized to q_1 bits at a sampling rate 1 Hz is $N_1(f) = 10^{-6q_1/10}$. To attenuate a small band of its quantization noise by R dB, the quantization noise floor has to be lowered by increasing the number of bits to q_2 (Refer Figure 3.11). Hence for the filtered signal the quantization noise PSD is $N_2(f) = 10^{-6q_2/10}$. It can be concluded from Figure 3.11 that

$$R = 10\ log_{10}\frac{N_2(f)}{N_1(f)} \tag{3.7}$$

$$\text{or} \quad q_2 = q_1 + \frac{R}{6} \tag{3.8}$$

It can be seen that every extra bit handles 6 dB more dynamic range in filtering. The

signal to be filtered has a resolution of 96 dB ($q_1 = 16$). It is found that a 48 dB attenuation of aliasing noise (with respect to the in-band noise floor) is sufficient to preserve the in-band SNR [8]. Hence the internal states of the filter (adders and multipliers) are twenty four bit wide ($q_2 = 24$).

3.3.3.4 Implementation details of the halfband filters

The block diagram of the polyphase implementation of the first halfband filter is shown in Figure 3.12. The P_4 block pads four LSBs to the data path to increase the dynamic range to 24 bits. The tap weights of the filter, b_0, b_2, b_4, b_5 are symmetric about the middle sample $b_5 = 0.5$.

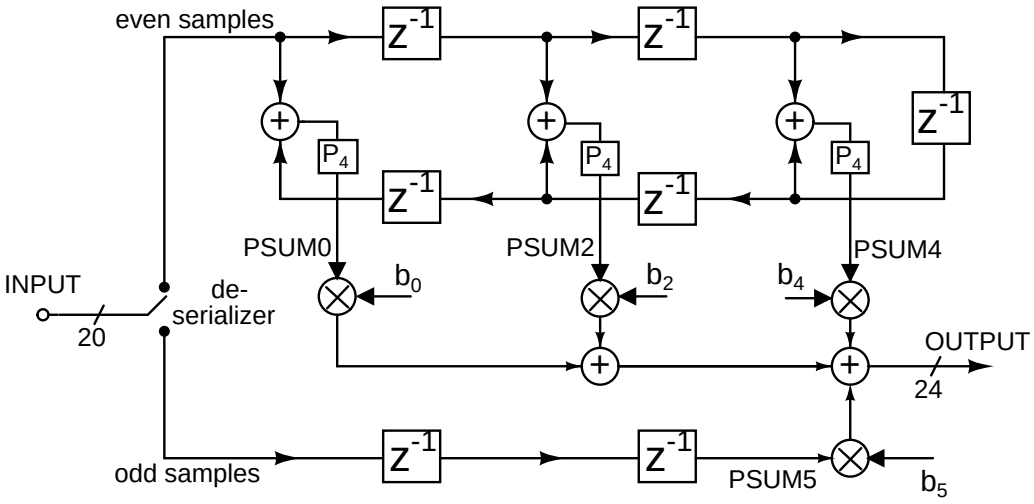

Figure 3.12: Polyphase implementation of the first halfband filter (10^{th} order).

The output of the filter is obtained from the internal states $PSUM0$, $PSUM2$, $PSUM4$, $PSUM5$ as shown in Figure 3.13. The tap weights are less than unity and hence are expanded in powers of 2^{-1} with CSD encoding. A 2^{-m} in the tap weight corresponds to right shifting the signal by dropping its m LSBs. Hence a tap weight multiplication is obtained by adding and subtracting right shifted signals. This multiplication is further nested based on Horner's rule [7]. This reduces the effective right shift operation and hence the effect of truncation noise. For e.g. $2^{-3}-2^{-5}-2^{-7} = 2^{-3}\{1-2^{-1}(2^{-1}+2^{-3})\}$. This nested multiplication requires extra shifting operations compared to the non nested

multiplication. However no explicit hardware is required to implement a shifter because shifting involves dropping LSBs. The coefficients of the first halfband filter are shown

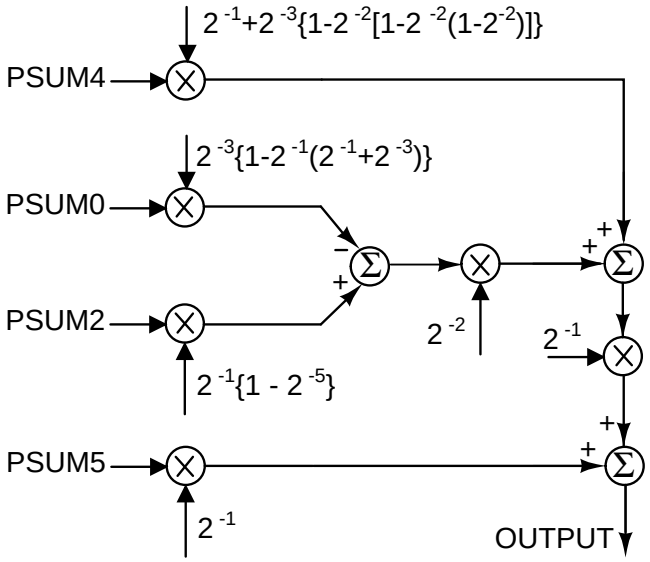

Figure 3.13: Obtaining output from the internal states.

in the table 3.2 and that of second halfband filter are shown in 3.3.

Table 3.2: Coefficients of the first halfband filter (10^{th} order)

Tap weight	**Value**	**CSD**
b0, b10	$+0.0107421875$	$+2^{-6} - 2^{-8} - 2^{-10}$
b2, b8	-0.0605468750	$-2^{-4} + 2^{-9}$
b4, b6	$+0.2998046875$	$+2^{-2} + 2^{-4} - 2^{-6} + 2^{-8} - 2^{-10}$
b5	0.5	$+2^{-1}$
b1, b3, b7, b9 are zero		

3.4 Equalizer

The constrain on the decimation filter is that, it should have passband gain error of ± 0.05 dB. It is a kind of a FIR filter which corrects the passband droop caused by the SINC4 filter [10]. The magnitude response of the equalizer is inverse that of the SINC4 filter in the in-band (0-24 kHz) and it works at the Nyquist rate. A thirty fourth order FIR filter is chosen for equalization [8]. The tap weights of the equalizer are found using *Parks McClellan* method. As in the halfband filters, the tap weights are

Table 3.3: Coefficients of the second halfband filter (50^{th} order).

Tap weight	**Value**	**CSD**
b0, b50	$+0.002929687500$	$+2^{-8} - 2^{-10}$
b2, b48	-0.002929687500	$-2^{-8} + 2^{-10}$
b4, b46	$+0.004394531250$	$+2^{-8} + 2^{-11}$
b6, b44	-0.006103515625	$-2^{-7} + 2^{-9} - 2^{-12}$
b8, b42	$+0.008544921875$	$+2^{-7} + 2^{-10} - 2^{-12}$
b10, b40	-0.011718750000	$-2^{-6} + 2^{-8}$
b12, b38	$+0.015869140625$	$+2^{-6} + 2^{-12}$
b14, b36	-0.021240234375	$-2^{-5} + 2^{-7} + 2^{-9} + 2^{-12}$
b16, b34	$+0.028808593750$	$+2^{-5} - 2^{-9} - 2^{-11}$
b18, b32	-0.040283203125	$-2^{-5} - 2^{-7} - 2^{-10} - 2^{-12}$
b20, b30	$+0.059814453125$	$+2^{-4} - 2^{-8} + 2^{-10} + 2^{-12}$
b22, b28	-0.103759765625	$-2^{-3} + 2^{-5} - 2^{-7} - 2^{-9} - 2^{-12}$
b24, b26	$+0.317382812500$	$+2^{-2} + 2^{-4} + 2^{-8} + 2^{-10}$
b25	$+0.5$	$+2^{-1}$
b1, b3, b7, . . . b21, b23, b27, b29, . . . , b47, b49 are zero		

encoded in CSD and multiplications are nested. Figure 3.14 shows frequency response of the equalizer, the passband frequency response of the unequalized decimator and the equalized decimator. The inset shows that passband ripples of the decimator is constrained to $\pm\,0.05\,$dB. After equalization the signal is rounded from 24 bits to 18 bits by dropping the six LSBs.

3.5 Scaling block

For a $\Delta\Sigma$ modulator the peak signal to noise ratio is obtained at a particular amplitude which is called as maximum stable amplitude (MSA) . If we increase the input to the modulator above this value, the modulator goes to instability and the SNR reduces down to zero [4]. This MSA is expressed in percent of fullscale. After decimation and truncating the signal to appropriate number of bits, to achieve the peak SNR at the Nyquist rate the signal has to swing to its fullscale. Hence the signal is scaled by $\frac{1}{\text{MSA}}$ to obtain fullscale swings at the output of the decimator.

The $\Delta\Sigma$ modulator in [2] has an MSA around 88 % of the fullscale. The output of the

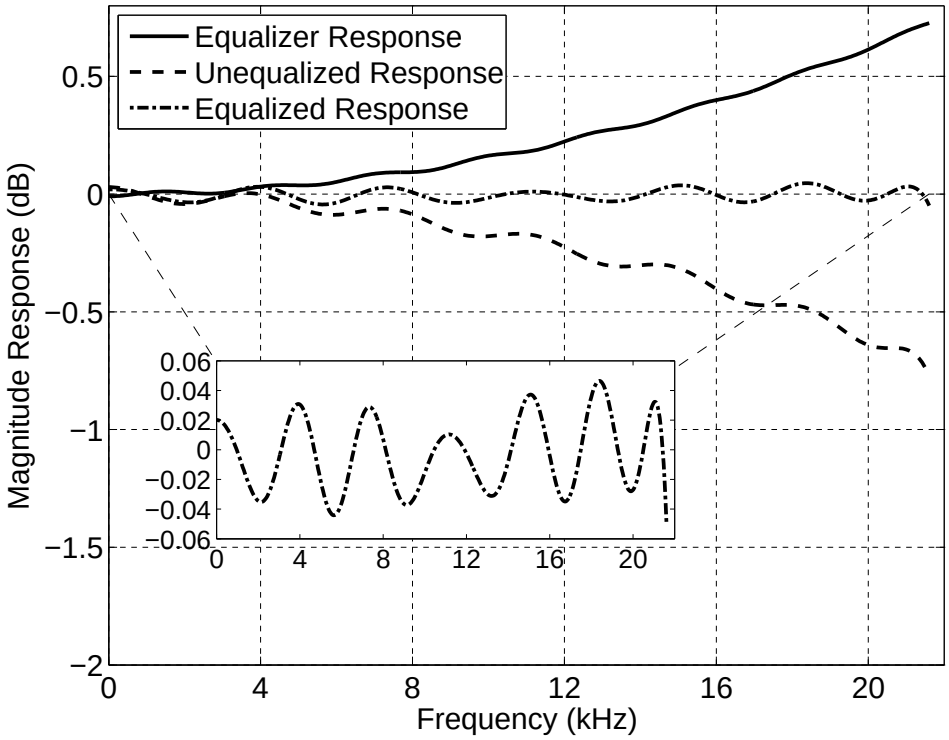

Figure 3.14: Frequency response of the Equalizer, the unequalized & the equalized decimator.

Table 3.4: Coefficients of the equalizer (34^{th} order).

Tap weight	**Value**	**CSD**
b0, b34	-0.00054931640625	$-2^{-11} - 2^{-14}$
b1, b33	$+0.00006103515625$	$+2^{-14}$
b2, b32	-0.00006103515625	-2^{-14}
b3, b31	$+0.00012207031250$	$+2^{-13}$
b4, b30	-0.00012207031250	-2^{-13}
b5, b29	$+0.00012207031250$	$+2^{-13}$
b7, b27	$+0.00018310546875$	$+2^{-12} - 2^{-14}$
b8, b26	-0.00024414062500	-2^{-12}
b9, b25	$+0.00036621093750$	$+2^{-11} - 2^{-13}$
b10, b24	-0.00042724609375	$-2^{-11} + 2^{-14}$
b11, b23	$+0.00061035156250$	$+2^{-11} + 2^{-13}$
b12, b22	-0.00091552734375	$-2^{-10} + 2^{-14}$
b13, b21	$+0.00140380859375$	$+2^{-9} - 2^{-11} - 2^{-14}$
b14, b20	-0.00256347656250	$-2^{-9} - 2^{-11} - 2^{-13}$
b15, b19	$+0.00567626953125$	$+2^{-7} - 2^{-9} - 2^{-12} + 2^{-14}$
b16, b18	-0.02166748046875	$-2^{-5} + 2^{-7} + 2^{-9} - 2^{-12} + 2^{-14}$
b17	$+1.03527832031250$	$+2^{0} + 2^{-5} + 2^{-8} + 2^{-13}$

modulator swings fully in its available range due to the presence of large quantization noise. At the output of the first halfband filter, the maximum output swing is found

to be 85 % of the fullscale, same as the MSA of the modulator. Hence the scaling is done after the first halfband filter where the quantization noise is attenuated to a level comparable to the noise floor in the in-band. The scaling value is kept slightly smaller than $\frac{1}{\mathrm{MSA}}$ to prevent overflow. The presence of passband ripples in other filters and the fact that the decimator operates with a finite number of bits can result in a overflow when the filter processes a signal of amplitude that is close to the fullscale. This scaling value is encoded in CSD and implemented with Horner's rule.

CHAPTER 4

Results and Conclusion

4.1 Description of design flow

The design and implementation details of the decimation filter in three stages using Hogenauer structure and polyphase decomposition are discussed in chapters 2 and 3. The actual circuit is modeled using the Hardware Description Language, Verilog and functional verification is done in Modelsim by writing appropriate test benches. Once this ideal circuit gives the same SNR obtained in Matlab for the same input stream, we can go ahead to the final steps of synthesizing and routing the circuit.

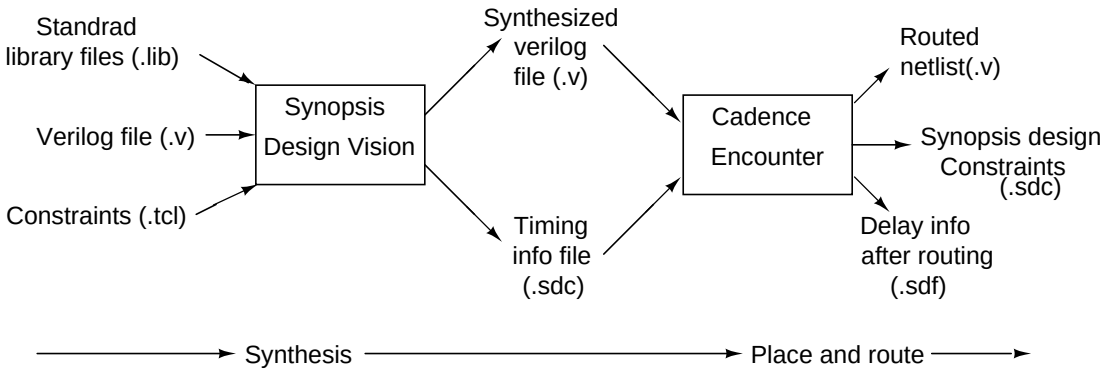

Figure 4.1: Block diagram of the design flow.

The digital circuitry behaviorally modeled in verilog is to be mapped into actual circuit components based on standard cell libraries and constraints. This procedure is called synthesis and is performed using the Synopsis synthesizing tool *Design Vision*. Design vision gives the synthesized verilog file as output by reading three inputs (Figure 4.1).

1. Verilog code for the circuit
2. Standard library files

3. Constraints

The verilog code is a behavioral description of the circuit. The standard cell libraries from UMC provide standard building blocks of the circuit in CMOS 180 nm technology. The constraints are given to the design vision using a .tcl script file.

Once the three input files (verilog, libraries and constraints) are ready, design vision compiles the input and creates a synthesized verilog file which is now based on standard building blocks. Design vision also gives a timing information file (.sdc). These files can be read using *Cadence encounter* to place and route (Figure 4.1). After placement and routing, the routed netlist can be saved as a verilog file and the timing information after routing can be extracted into a .sdf file both of which can be used for the post-route simulations.

4.1.1 Simulation results

The input test stimulus for the decimator is obtained through simulations in MATLAB with the help of the $\Delta\Sigma$ toolbox [4]. The signal is translated to corresponding verilog format for simulating it with the netlist obtained after Place & Route. The spectrum of the output signal is obtained and SNR is evaluated at the Nyquist rate. The decimator is tested for SNR performance with sine wave excitation of different frequencies. A sample spectrum from the output of the modulator is shown in Figure 4.2. The final simulation results are summarized in 4.1.

Table 4.1: Variations of SNR with input tone frequency

Input signal frequency (kHz)	**Output signal SNR** (in dB)
4.5	110.4254
9	108.6879
13.5	110.5582
18	108.4753
22.5	110.1912

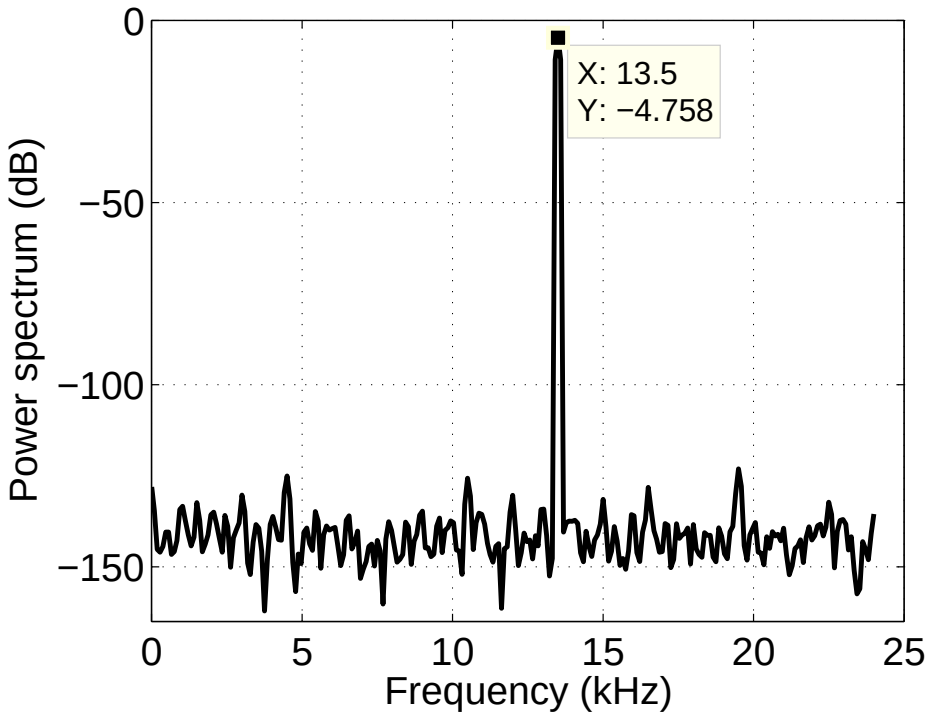

Figure 4.2: Simulated spectrum of the decimator output, SNR=95.8 dB.

4.2 Conclusion

The total power consumed by the entire decimation filter is 115 μW. The power report of the decimation filter is shown in the table 4.2.Thus hogenauer structure for sinc implementation and polyphase implementation for halfband filteres are proved to be very useful for low power decimation filters. In hogenauer structure pipelining and retiming will save 46% of total power. The low power of the halfband filter is attributed mainly to the decrease in the operating frequency of the circuit in polyphase. The decimation filter is completely designed with automated CAD tools, no handcraft circuits used.

Table 4.2: Power report of the decimation filter

Module	**Input Clock**	**Power**	**% Power**
$SINC^4$ filter	3.072 MHz	21.9 μW	19.1
Halfband one	192 KHz	9.78 μW	8.5
Halfband two	98 KHz	43.7 μ W	38.1
Scaling Block	48 KHz	0.552 μW	0.5
Equalizer	48 KHz	37.5 μW	32.5
Total		115 μW	100

CHAPTER 5

Measurement results from the $\Delta\Sigma$ modulator chip

5.1 Test setup

Figure 5.1 shows the block diagram of the test setup for the $\Delta\Sigma$ modulator chip. The

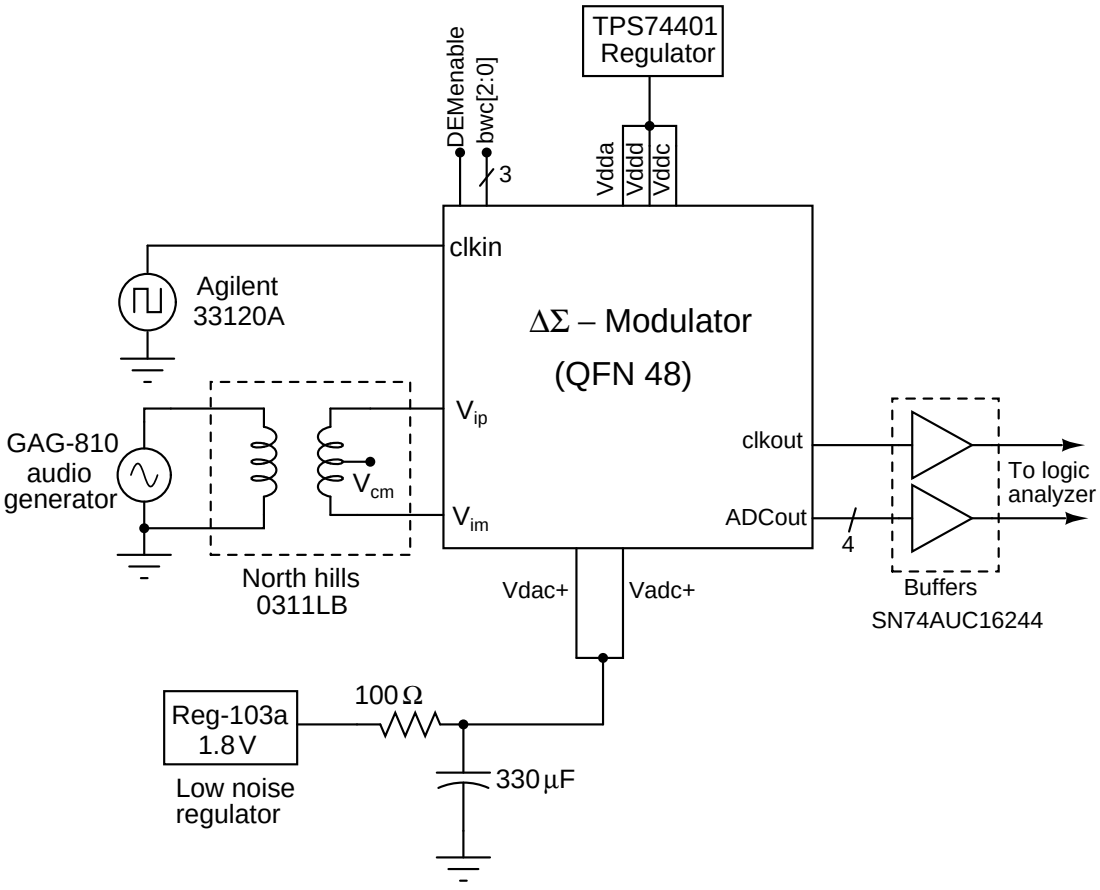

Figure 5.1: Test setup of the $\Delta\Sigma$ modulator.

input sinusoidal signal generated using an audio precision signal source. The Agilent 33120A clock source generates the 3.072 MHz clock for the chip. The reference voltages for the DAC (Vdac+) and flash ADC (Vadc+) are generated using a low noise voltage regulator Reg-103a. The reference voltage is low pass filtered with a first order low

pass filter whose cutoff frequency is 5 Hz. The output integrated noise of the reference voltage after filtering is 0.6 μV in the bandwidth 20 Hz - 24 kHz. The output signal is captured using a logic analyzer. Figure 5.2 shows the snapshot of the four layer PCB designed for the test setup.

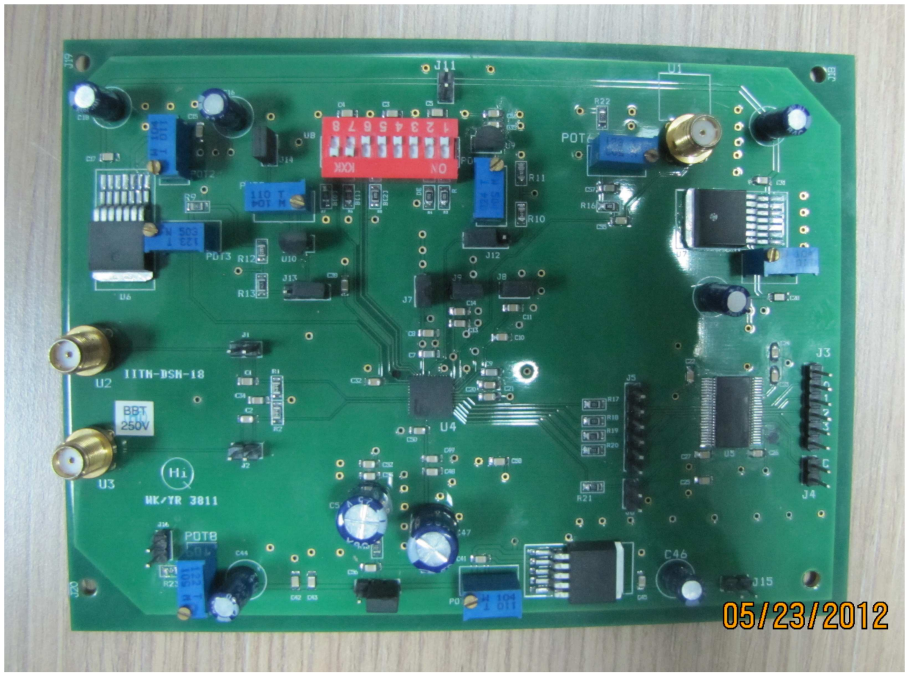

Figure 5.2: Picture of the PCB for testing the $\Delta\Sigma$ modulator.

5.2 Measurement results

Two types of measurements are performed for testing the modulator viz. without signal (Idle channel performance) and with a sinusoidal signal.

5.2.1 Idle channel performance

When no input signal is given to the input of the modulator, the output of the modulator contains only the shaped noise. On integrating the noise power spectral density in the in-

band (20 Hz - 24 kHz) the integrated in-band noise power of the modulator is obtained. The differential input signal is shorted to the common mode voltage and the output spectrum is obtained. Figure 5.3 shows the idle channel performance of the modulator when the input is shorted.

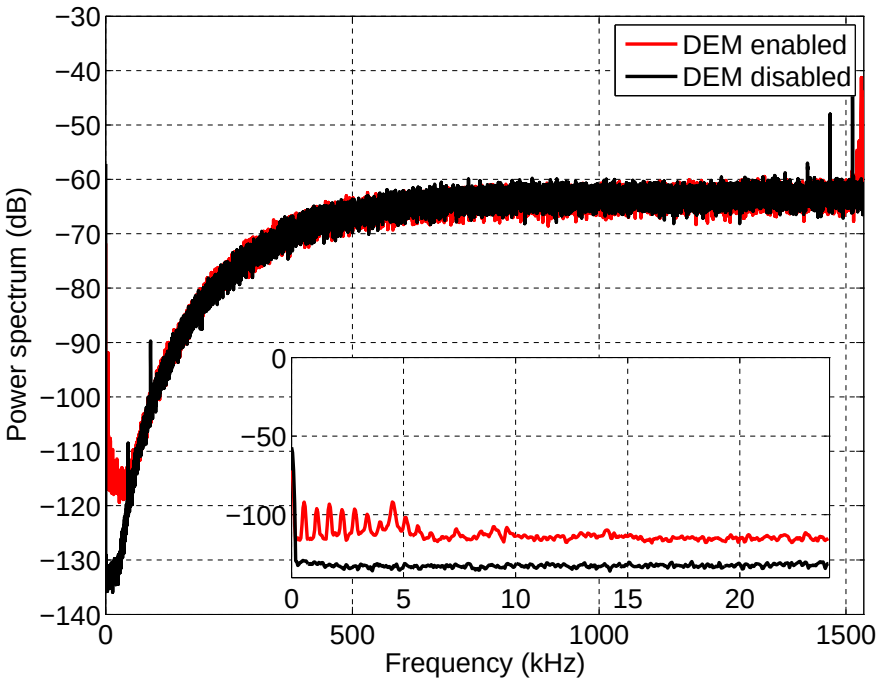

Figure 5.3: Idle channel performance with the differential inputs short circuited.

It is found that the integrated in-band noise when the DEM is disabled is 5.4977 μV_{rms} which is 3.5 dB degradation from the targeted performance of 3.7 μV_{rms}. There are three tones near $f_s/2$ and few tones out of the signal band which have a beat frequency of 18 kHz. When the DEM is enabled these tones vanish due the DEM action and the in-band noise floor increases, because at very low frequency the noise floor at the output of the modulator is decided by the first order mismatch error shaping of the DEM. However, the increase in the noise floor is found to be around 20 dB which is much larger than the simulation estimate [1].

On changing the bias currents of the loop filter, the supply voltage of the loop filter, the clock generation circuits/buffers, the reference voltage for the DAC, the frequency of the sampling clock, all within $\pm$ 5 % of its nominal value, similar performance trends and no

appreciable change in the in-band integrated noise was observed. A possible experiment in which the differential input signals to the modulator are left floating rather than being connected to its common mode voltage. The noise profile remains more or less the same as observed in Figure 5.3. The in-band integrated noise in the open circuit condition is 4.1277 μV_{rms}. Figure 5.4 shows the idle channel performance of the modulator when the input is opened.

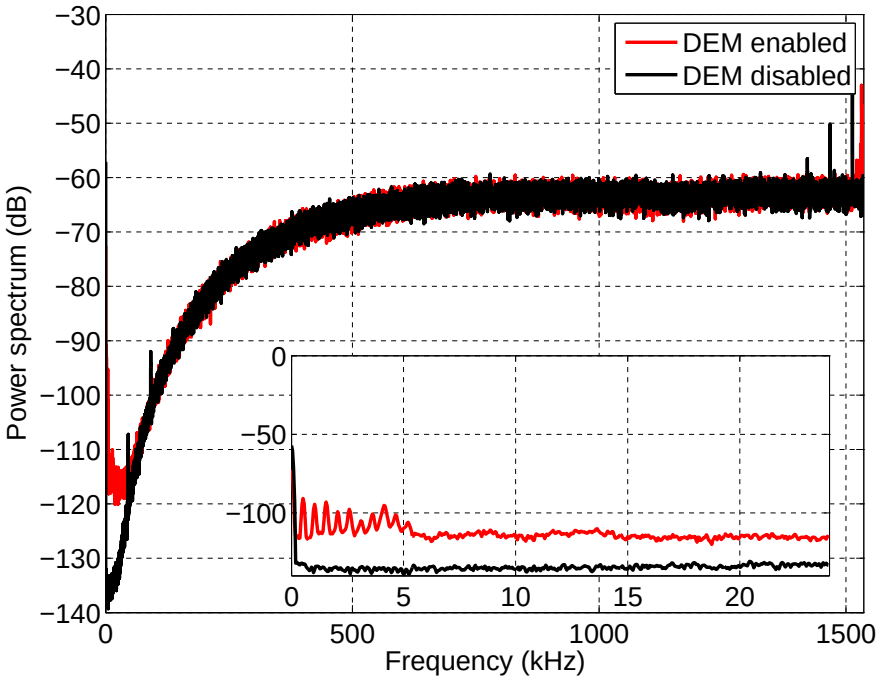

Figure 5.4: Idle channel performance with the differential inputs open circuited.

The integrated noise calculated in the inband for short circuited input and open circuited input are mentioned in the table 5.1

Table 5.1: Integrated Noise

Supply voltage	1.8V
Int noise(short ip)	5.4977μV
Int noise(open ip)	4.1277μV

Figure 5.5 shows the idle channel performance of the modulator when the input is shorted and opened.

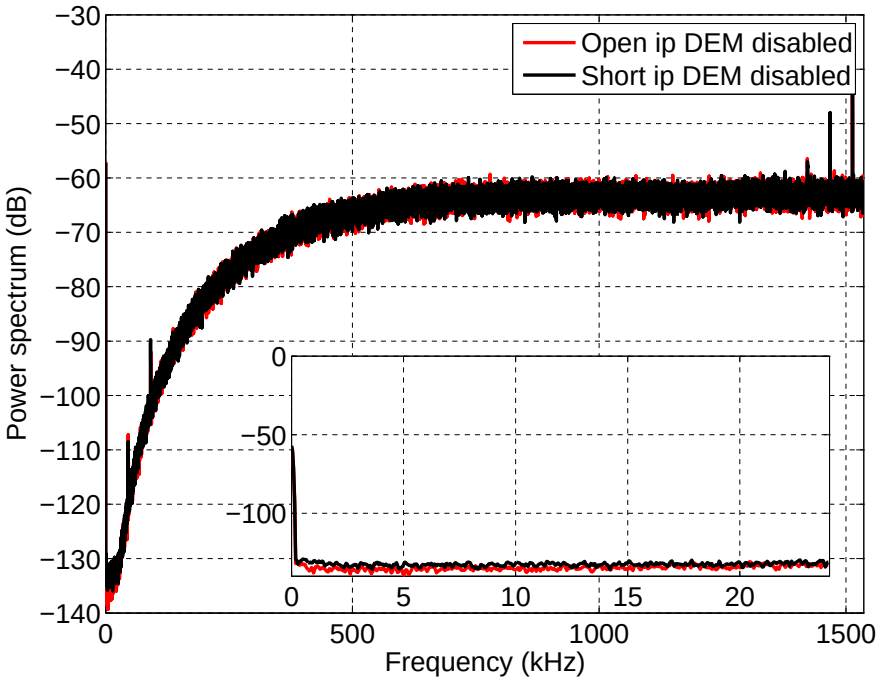

Figure 5.5: Idle channel performance with the differential inputs open circuited.

5.2.2 Performance with sinusoidal input

The $\Delta\Sigma$ modulator chip is excited by a sinusoid at 4.5 kHz. Two million samples are taken from the output of the modulator and a Blackman-Harris window is applied before evaluating the power spectrum of the signal. The signal amplitude is varied from millivolt to amplitudes near fullscale (3 V). It is found that the modulator is stable up to -0.7 dBFS. Figure 5.6 shows the output power spectrum of the signal for various input signal amplitudes when the DEM is disabled. Figure 5.7 shows the output power spectrum of the signal for various input signal amplitudes when DEM is enabled. Very large harmonic distortion of the input sinusoid is found in the output spectrum. Further, the spectrum of the input signal spreads to multiple bins as the signal amplitude is increased. The noise floor of the modulator remains almost constant at smaller input amplitudes.

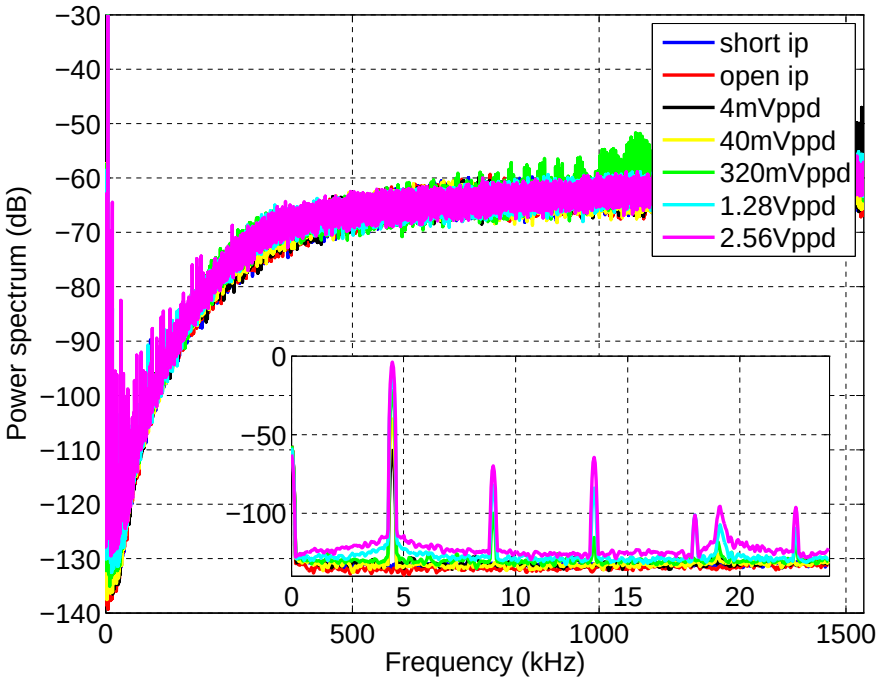

Figure 5.6: Spectrum from the $\Delta\Sigma$ modulator chip for a sinusoidal input at 4.5 kHz.

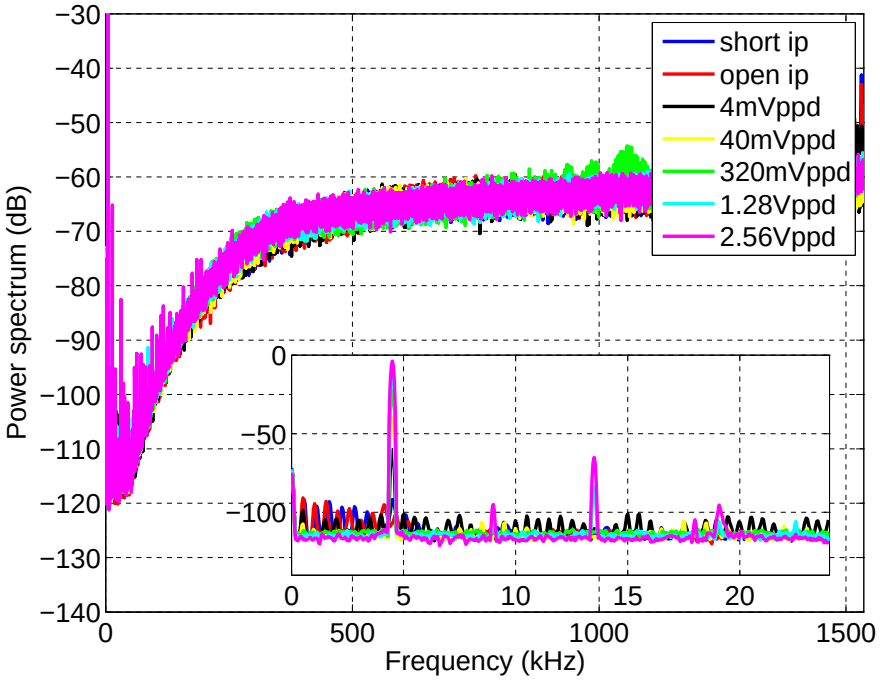

Figure 5.7: Spectrum from the $\Delta\Sigma$ modulator chip for a sinusoidal input at 4.5 kHz.

5.2.3 DEM enabled vs disabled

In this section, two plots are mentioned to show the effect of DEM when the signal is applied. Figure 5.8 is, when the applied signal is $0.64V_{ppd}$.Figure 5.8 is, when the applied signal is $2.56V_{ppd}$.The dynamic range (SNR Vs amplitude) plot is shown in

figure 5.10.

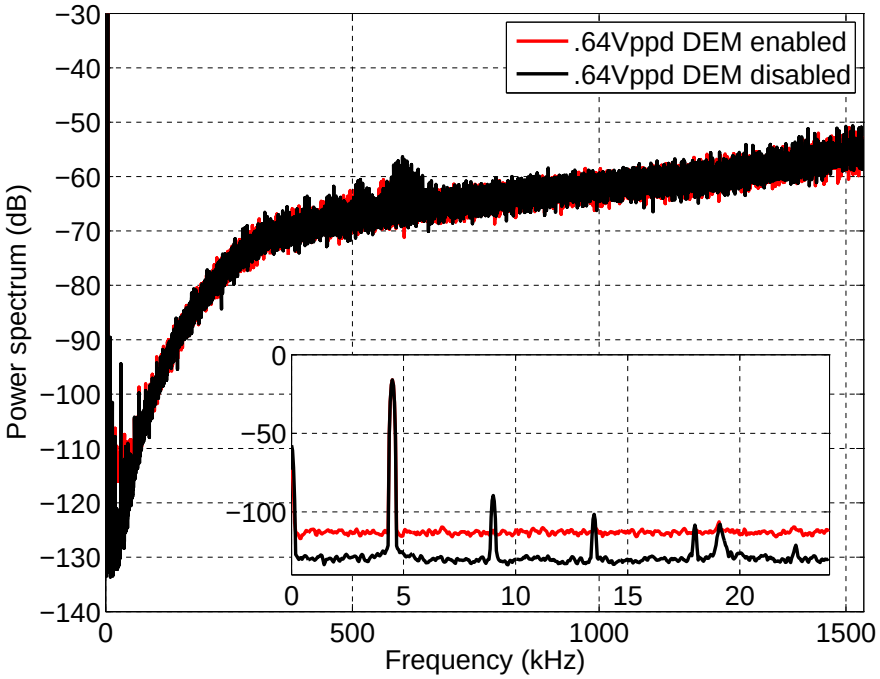

Figure 5.8: Spectrum from the $\Delta\Sigma$ modulator chip for a sinusoidal input at 4.5 kHz.

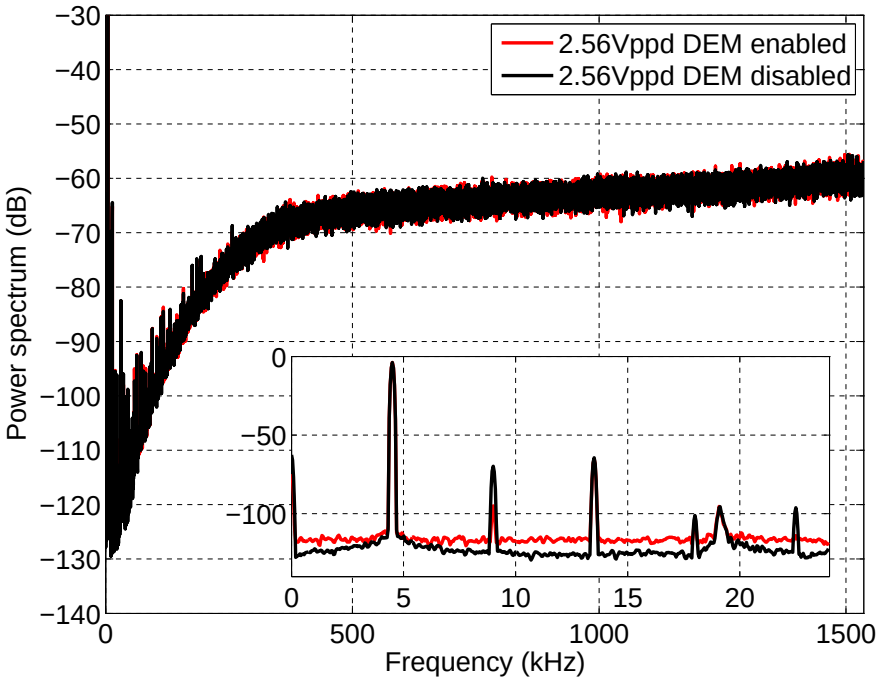

Figure 5.9: Spectrum from the $\Delta\Sigma$ modulator chip for a sinusoidal input at 4.5 kHz.

In the table 5.2 the SNR values are mentioned for both DEM enabled and disabled cases.Similarly in the table 5.3 the SNDR values are mentioned for DEM enabled and disabled cases.

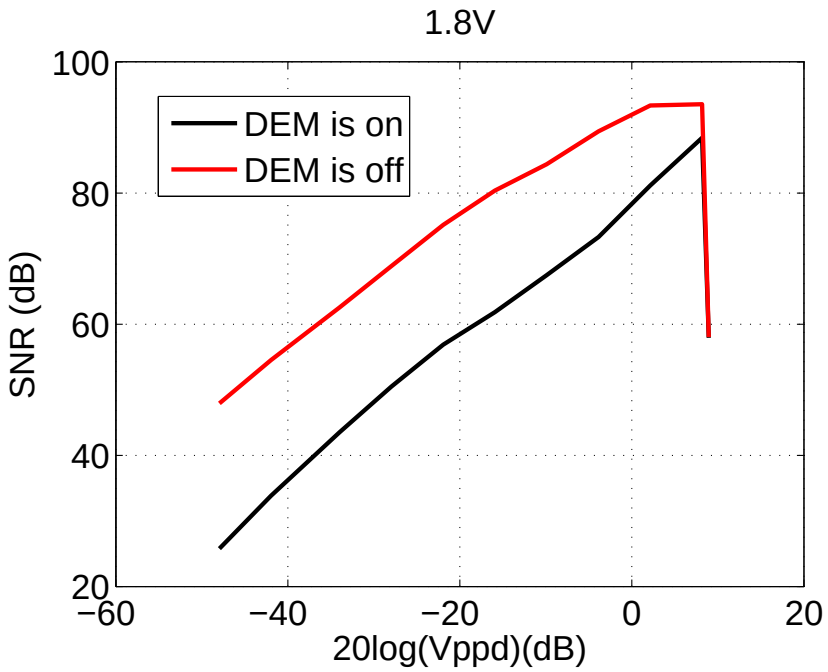

Figure 5.10: Dynamic Range plot.

Table 5.2: Measurement Results - SNR

Differential amp (Vppd)	SNR(DEM disabled)dB	SNR(DEM enabled)dB
.004	47.9292	25.7772
.008	54.5352	33.8541
.020	62.5459	43.5210
.040	68.8527	50.4854
.080	75.1467	56.8609
.160	80.3667	61.8206
.320	84.3943	67.4858
.640	89.4094	73.2897
1.28	93.3387	81.1373
2.56	93.5461	88.4141
2.8	58.0194	57.9289
3	64.2294	63.8054

Table 5.3: Measurement Results - SNDR

Differential amp (Vppd)	SNDR(DEM disabled)dB	SNDR(DEM enabled)dB
.004	47.6159	25.5783
.008	54.2060	33.6276
.020	62.2053	43.2868
.040	68.4057	50.2057
.080	74.6476	56.5884
.160	76.0914	61.4698
.320	76.8151	67.1067
.640	73.0918	72.8302
1.28	69.9463	72.9304
2.56	59.4538	61.2751
2.8	52.2070	52.4029
3	27.3114	27.2976

CHAPTER 6

Issues found in previous Design

6.1 Issues found in previous Design

This chapter will explain the factors degrading the SNDR in the earlier design and the measures to improve it. Considering all the blocks in their schematic form, a simulation was run, and it was found that the SNDR is less in DEM enabled case rather than DEM disabled case. To find further Performance degrading parameters, few blocks like loop filter, ADC and DAC were replaced with their ideal blocks and found that the results were same as earlier. Based on these observations, feed back path, having the elements DEM and DAC, is causing the problem. Hence the focus was put on Feedback path.

6.1.1 Bit Reversal

In the DSM block it was found that the output thermometric bits were connected to the DEM block in the reverse order. Inside the DEM block the logic was implemented in such a way that for every clock cycle the use of DAC element was left shifted. This has been explained through a small example below. Let us say that the ADC output bits are 000000001111111 and in the next cycle it is 000000011111111. Now let us say that in the first cycle the first seven DAC elements are chosen and in the next clock cycle next eight elements will be used according to the algorithm. That is how the DEM block was implemented when the DEM is enabled. So it should use the DAC elements in the first case as 000000001111111 and in the second case as 111111110000000. This is shown in figure 6.1.

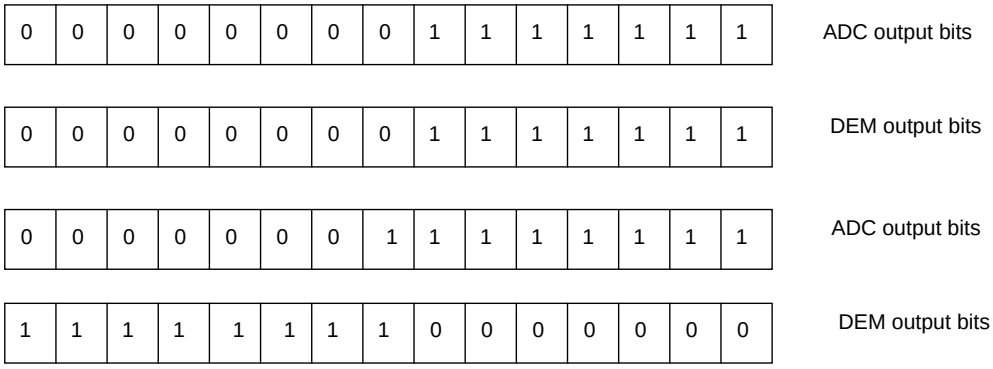

Figure 6.1: Logic of DEM block.

The fault in the previous implementation was, the ADC output bits were connected in the reverse order. So the logic of DEM was lost. This is explained by the same example as above. Due to reverse order the input code to the DEM is 111111100000000 and as the input in the second cycle is 111111110000000. In the first cycle the DAC elements are used as follows 111111100000000. But in the second cycle the input is left shifted by seven and is given by 100000001111111. This is shown in figure 6.2. As we can see clearly that this is using the first element twice. This was one of the problem.

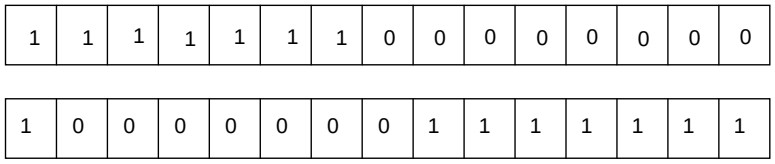

Figure 6.2: DEM output bits.

6.1.2 DEM output waveforms

The signals which were driving the DAC buffers were generated by the DEM block. The output of these DEM block contains true and complementary signals and to avoid causing non linearity, these waveforms should be perfectly complementary to each other. But it was found out that the output waveforms of the DEM block were not exactly complementary. The “demout” and “demoutb” (which were the outputs of DEM block) are generated by an flip-flop which was inside the DEM block. The demoutb was generated by an inverter which was inside the flip-flop, and this was causing some delay between

"demout" and "demoutb". The waveforms of "demout" and "demoutb" are shown in figures 6.3 and 6.4.

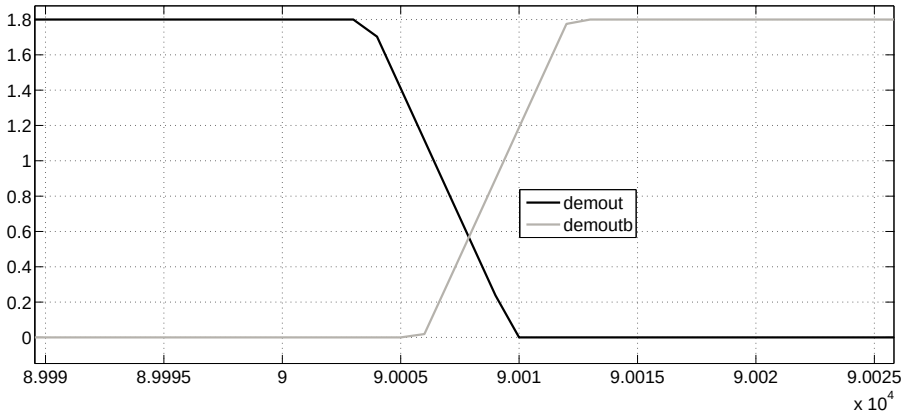

Figure 6.3: DEM Output waveforms.

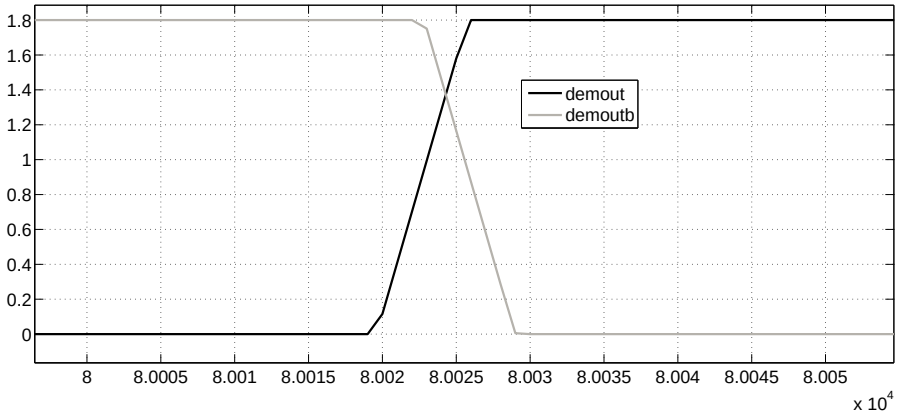

Figure 6.4: DEM Output waveforms.

6.1.3 Simulation Results

The $\Delta\Sigma$ modulator was simulated in cadence and the results are tabulated in table 6.1. It shows that when the DEM is enabled the SNDR is less compared to the DEM disabled case, the 2^{nd} and 4^{th} harmonics are high when DEM is enabled. The spectrum of this is shown in the figure 6.5. This issue is fixed in the current implementation.

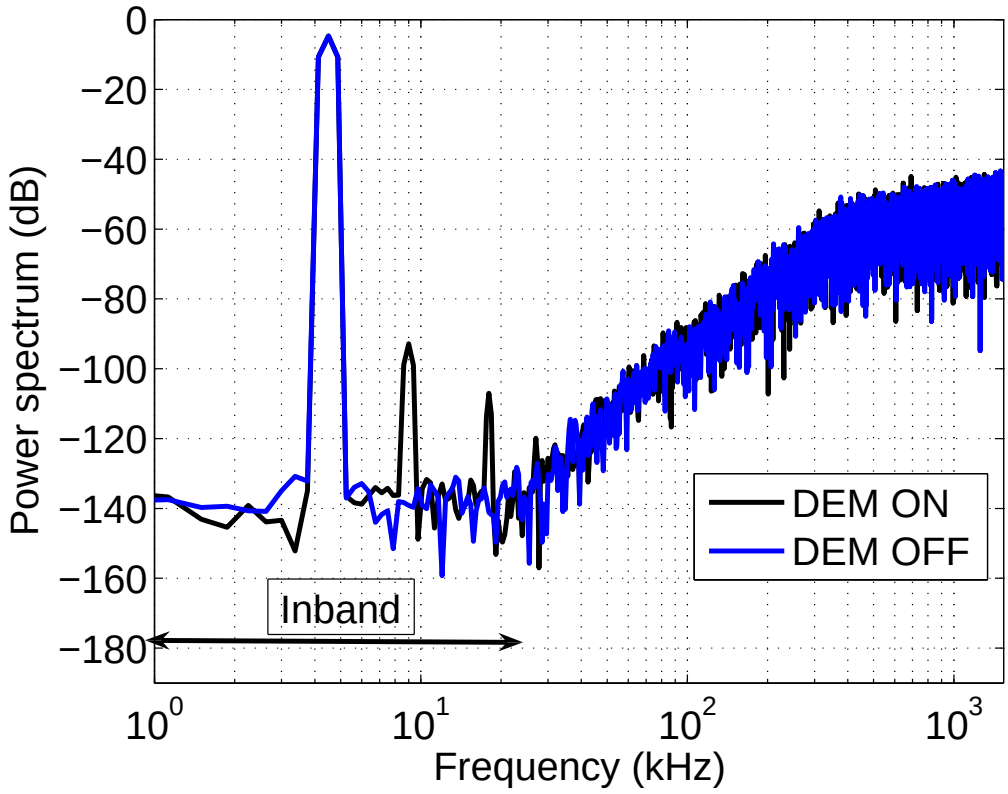

Figure 6.5: Power Spectrum.

dem ON/OFF	Case	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	reversal bit	115.0457	123.0735	115.7899
ON	reversal bit	87.9852	87.9915	116.4083

Table 6.1: SNDR, SDR and SNR

6.2 RC-extraction of DAC-Increase in Noise Floor

When simulation was performed with all the blocks in schematic level, the SNDR was around 115dB for DEM disabled case. This result was even same for the case with capacitance extraction blocks. But having changed the DAC to its RC-extraction level, the SNDR dropped to 90dB which was very high(around 25dB). It can be thought as a mismatch between the DAC elements, the DEM block has to track all of these mismatches and shape the noise as out of band. But in [1] the DEM was failed even with the schematic level itself, so in this case also. From the measurement results, it is clearly visible that in-spite of DEM being enabled the noise floor is high compared with the DEM disabled case. By simulating the DSM, with the DAC in RC extracted view, the

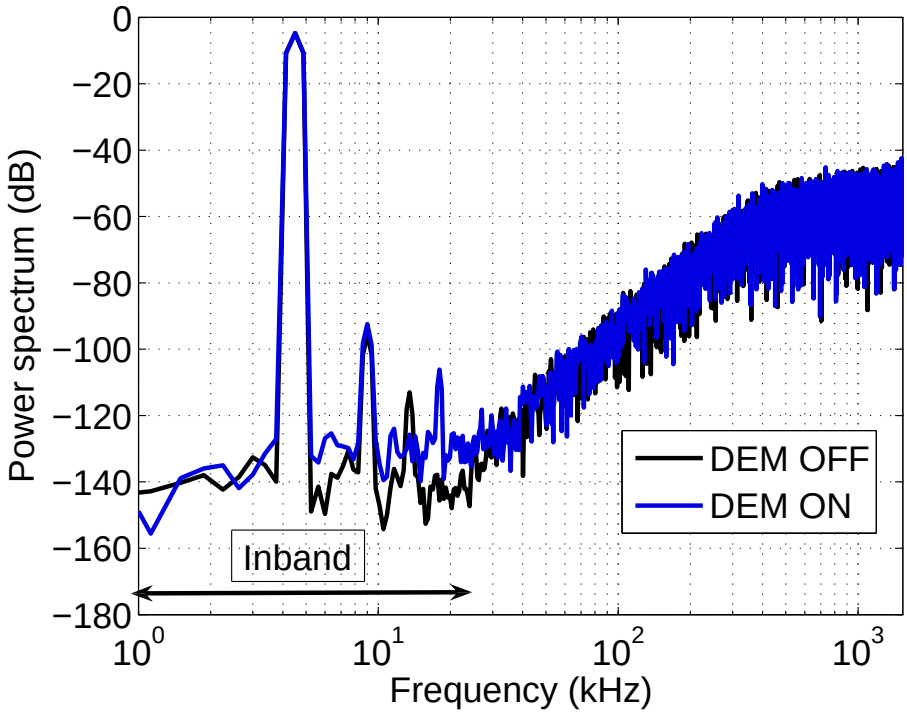

Figure 6.6: Power Spectrum.

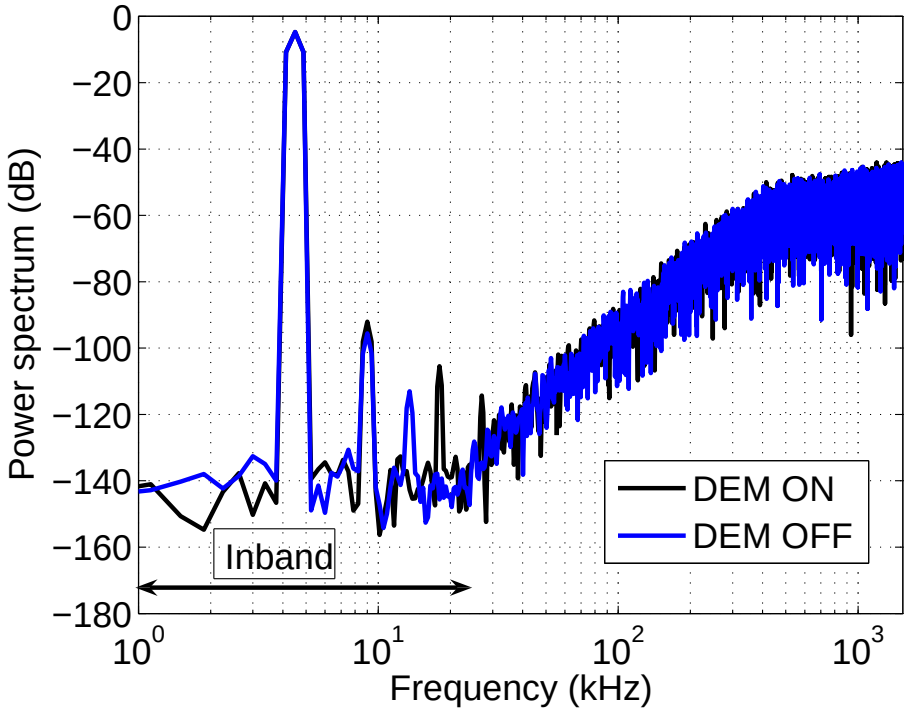

Figure 6.7: Power Spectrum.

noise floor was high, which can be observed in the figures 6.6 and 6.8. In figure 6.6, the blue one represents the DEM enabled case in which the ADC thermometric bits

are connected in the reverse order to the DEM block and the black color represents the DEM disabled case. In this figure it is observed that noise floor is slightly higher with the DEM enabled case. In figure 6.7, black one represents the DEM enabled case when the ADC thermometric bits are connected in the proper order to the DEM block and the blue color represents the DEM disabled case. In figure 6.8, both the curves are for DEM

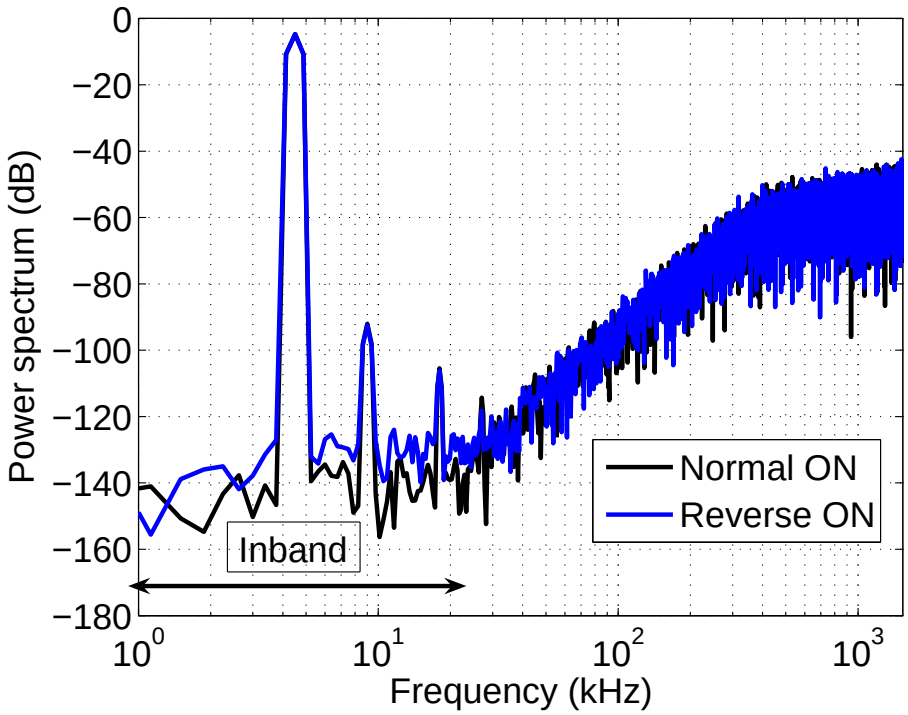

Figure 6.8: Power Spectrum.

enabled case. The blue one is when the ADC thermometric bits are connected in the reverse order to the DEM block and the black color represents when they are connected properly. The table 6.2, reveals that SNR is less when the ADC bits are connected in the reverse order to the DEM block.

dem ON/OFF	Case	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	reversal bit	90.7416	90.7477	119.2547
ON	reversal bit	87.5086	87.5367	109.4140
ON	normal	87.0815	87.0846	118.5179

Table 6.2: SNDR, SDR and SNR when the DAC is in RCx view

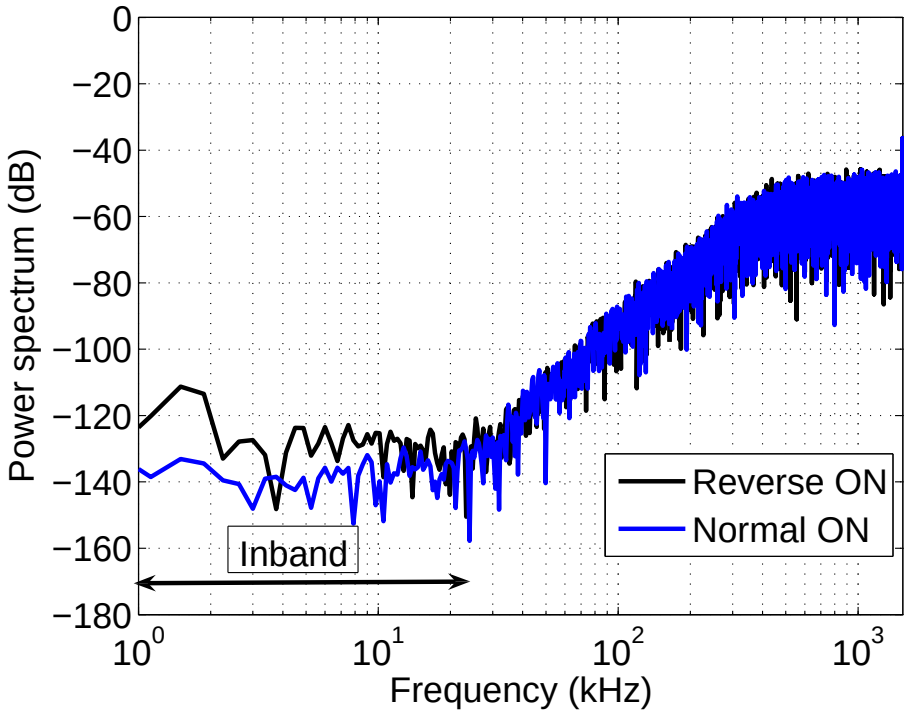

Figure 6.9: Power Spectrum.

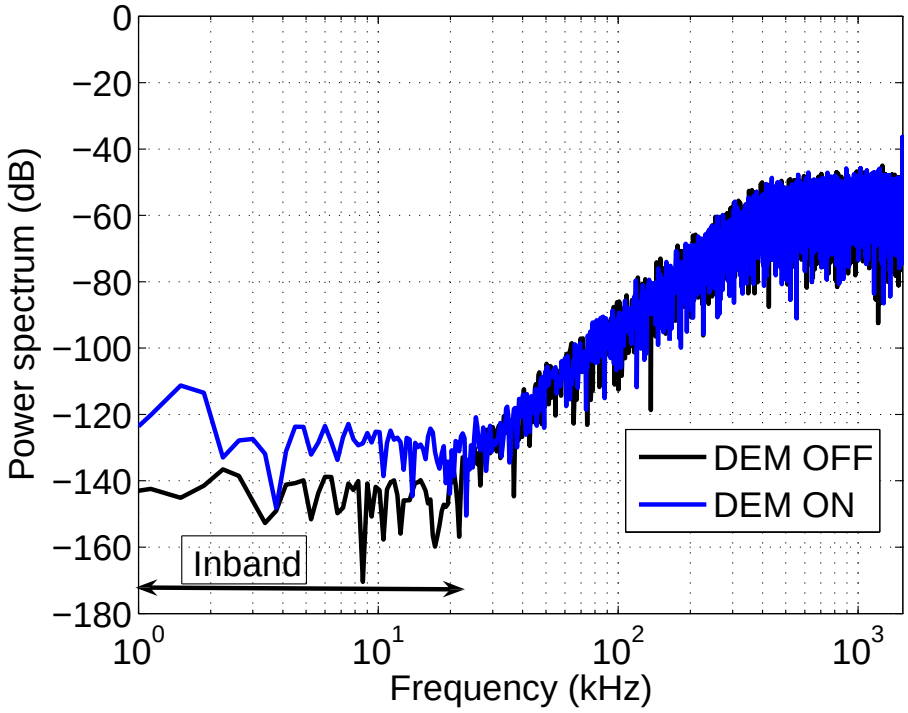

Figure 6.10: Power Spectrum.

The figure 6.9, the two plots are for DEM enabled case. The black one representing the ADC bits connected in reverse order and the blue one representing when they are con-

nected in properly.The figure 6.10, One plot in blue color is for DEM enabled case with the reverse connection and the other in black is when DEM disabled. The remaining one is the plot when DEM is disabled.

6.3 Simulation Results by Introducing mismatch in DAC elements

This section gives the simulation results by introducing mismatch in DAC elements which is mentioned in [1] as $\sigma_{\frac{\Delta R}{R}} = 0.055\,\%$. The simulation was run and the results are tabulated in the table 6.3.

dem ON/OFF	Case	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	reversal bit	84.4058	84.4324	106.5453
ON	reversal bit	87.5212	87.7391	100.6243
ON	normal	87.5874	87.5885	123.6060

Table 6.3: SNDR, SDR and SNR by introducing mismatch

From the table 6.3 it is clear that when the bits are connected in the reverse order the SNR is less compared to the remaining cases. From the figure 6.11 it is visible that when the ADC bits are conected in the reverse order, the noise floor is high. Also in figure 6.12, the black one represents the ADC bits are connected in the reverse order(with DEM enable) and the blue one when DEM is disabled.

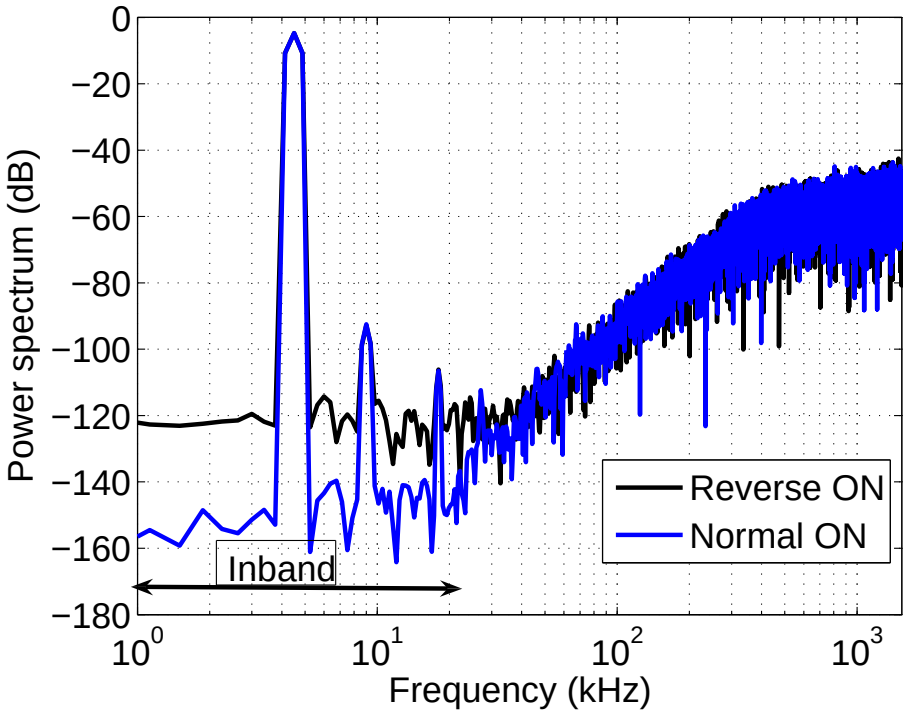

Figure 6.11: Power Spectrum.

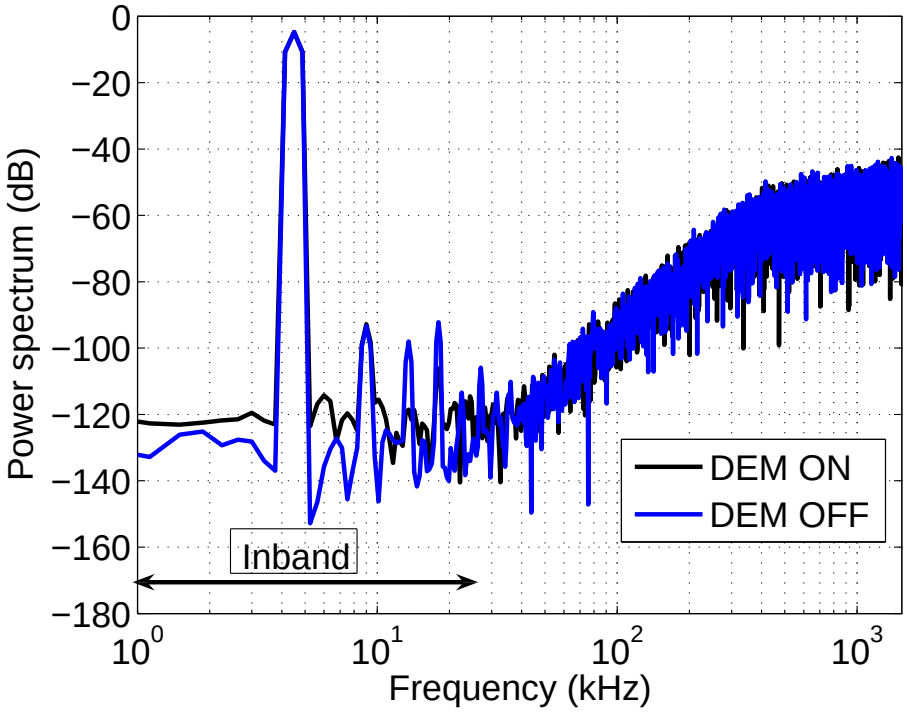

Figure 6.12: Power Spectrum.

6.4 How to improve

In the previous sections issues like ADC bits are connected in the reverse order to the DEM and delay between the complementary waveforms of DEM output signals are mentioned. This section deals with how to fix these issues and tries to achieve the maximum possible SNDR. To make the DEM outputs exactly complementary the verilog codes were modified. In some places of verilog codes, blocking assignments were replaced by non blocking assignments.

6.4.1 Blocking vs Non blocking Assignments

In verilog there are two type of assignments

- Blocking Assignments '='
- Non Blocking Assignments '<='

In blocking assignments the statements are executed sequentially. These assignments block the execution of the following lot of assignments at anytime. Non Blocking assignments are executed concurrently. By using the non blocking assignments the delay between the "demout" and "demoutb" of DEM block was reduced mostly. With this the DSM block was simulated and found that the SNDR was 105dB for the DEM enabled case(120dB when dem was disabled). Still 15 dB off was there between the DEM enabled and disabled cases.The Power Spectrum for this case is shown in the figure 6.13 and the simulation results are shown in the table 6.4. Even with the exactly complementary outputs from the DEM block by using the Voltage controlled voltage source (VCVS), there was no much improvement in the SNDR for the DEM on case.

dem ON/OFF	Case	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	Case	120.8901	127.1057	122.0764
ON	Case	105.6280	105.6858	124.4167

Table 6.4: SNDR, SDR and SNR

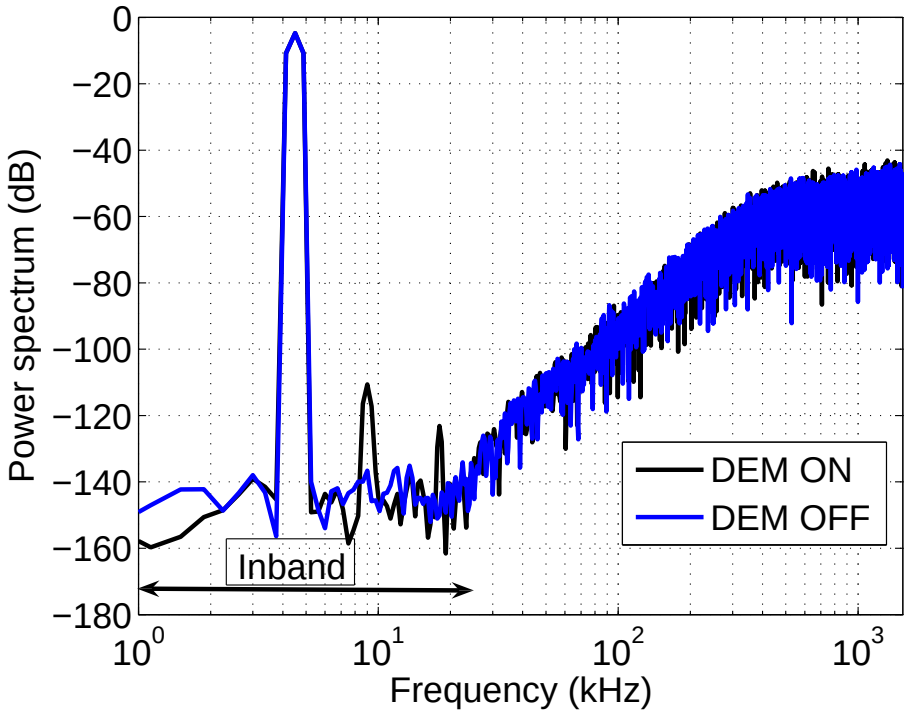

Figure 6.13: Power Spectrum.

Actually the signals from the DEM were driving the buffers before going to the Mos switches. The problem was in the feedback path which consists of DEM, buffers and the DAC. So here due to each block the degradation was found out by running some simulations. In the first case by removing the buffers in the feedback path and the exact complementary signals from the DEM block were driving the Mos switches. So in this case there was no delay in the complementary driving signals. The simulations were ran across different corners and the are tabulated in the table 6.5

DEM	TT	FF	SNFP	FNSP	SS
ON/OFF	[dB]	[dB]	[dB]	[dB]	[dB]
OFF	125	125	123	125	124
ON	116	113	116	113	114

Table 6.5: SNDR(MOS switches-DAC)

Now by inserting the buffers in the feedback path and running the simulations, the

results have been tabulated in the table 6.6.

DEM	TT	FF	SNFP	FNSP	SS
ON/OFF	[dB]	[dB]	[dB]	[dB]	[dB]
OFF	122	126	126	126	123
ON	111	111	111	111	110

Table 6.6: SNDR(MOS switches, Buffers-DAC)

In this case the blocks which were used to generate the exact complementary signals were removed from the test-bench, the simulations were run and results have been tabulated in the table 6.7.

DEM	TT	FF	SNFP	FNSP	SS
ON/OFF	[dB]	[dB]	[dB]	[dB]	[dB]
OFF	124	126	126	126	124
ON	105	105	104	105	105

Table 6.7: SNDR(MOS switches, Buffers-DAC, without VCVS)

6.5 DEM-Fixed Rotation

In case of Data weighted averaging the bits are rotated according to an algorithm, but here just to find out SNDR for different fixed rotation new DEM block was designed. It consists of extra pins as in1, in2, in3. Here the logic is simple, the amount of shifting is fixed and it depends on the in1, in2 and in3. The new DEM block used in this case is shown in the figure 6.14.

Shifting = 4*in3+2*in2+in1

DSM is simulated for different combinations of in1, in2 and in3. The shifting is maximum when all are 1's. The results have been tabulated in the table 6.8.

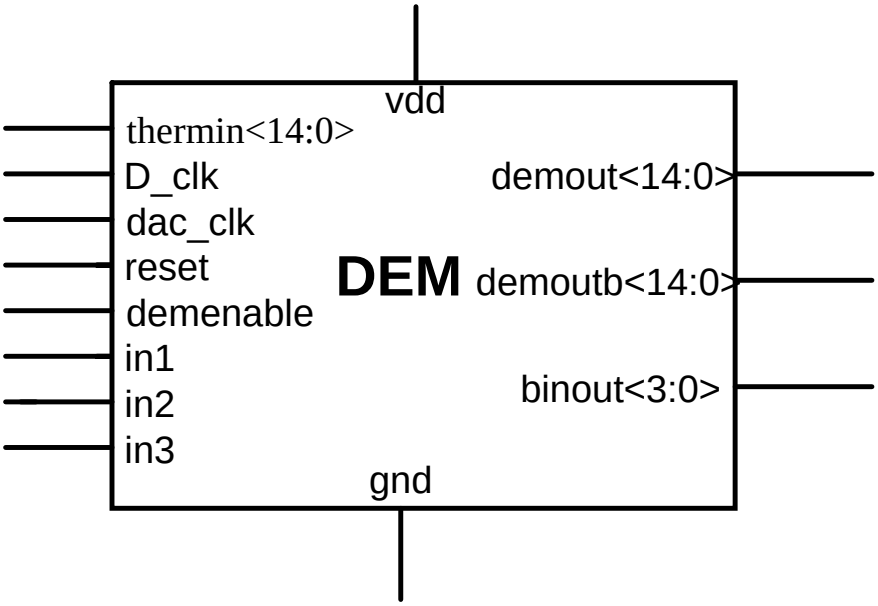

Figure 6.14: Block diagram of a discrete-time $\Delta\Sigma$ modulator.

Rotation	DEM On/Off	SNR(dB)
1	On	124
2	On	124
3	On	117
4	On	112
5	On	108
6	On	107
7	On	106
Normal	On	104
Normal	Off	126

Table 6.8: Simulation Results

From this it is clear that it is not possible to get the SNDR same for both the cases(with DEM enabled and disabled). This is because, the DAC elements sudden switching was more when DEM was enabled compared to the disabled case. This is explained by an example. Take 000000000001111 is the present ADC output and 000000000111111 is the next output of ADC. When DEM is disabled in the second cycle there are 2 transitions(total 4 transitions). But when the DEM is enabled the transitions are 10(total 20 transitions), which causes the increase in asymmetry between the rise and fall times.

6.6 Conclusion

From the above results it is clear that the increase in noise floor is due to the bit reversal of ADC output bits. Also it is clear that by using DEM block for this kind of DAC, the rise and fall time asymmetry causes degradation in the SNDR. The possible solutions are

- Using DAC calibration
- Can use another architecture of DAC

In the following section we deal with the new kind of DAC which is insensitive to the rise and fall time asymmetry.

CHAPTER 7

Design Improvement

7.1 Dual Return to Zero DAC

A classic problem in continuous-time output stage is inter-symbol interference (ISI). This interference occurs because the output pulse does not have equal rise and fall times, and hence each output level is affected by the previous ones.ISI results in inband harmonics and degrades the linearity of the $\Delta\Sigma$ modulator. One solution is to use the return-to-zero (RTZ) scheme so that the circuit does not have any memory of its previous levels. It is well known that the inter-symbol interference problem can be solved by using a return-to-zero (RTZ) code, where each bit cell is turned off during half of the clock period. However, this approach introduces large steps in the DAC output voltage, which again causes problems with jitter sensitivity and linearity in the output stage.

To overcome this problem, a new dual RTZ scheme has been proposed in [14]. In this scheme, two independent return-to-zero signals are generated, with a time offset of half clock period. These signals are then linearly added together to form an output signal that is continuous over the full clock period. The theory of superposition may be used to state that if each RTZ signal is spectrally pure due to the absence of any inter-symbol interference, then the linear sum of two RTZ signals must also be spectrally pure. This can also be explained in the time domain by noting that if the fall of the phase-1 RTZ signal does not match the rise of the phase-2 RTZ signal, the small glitch will occur in the summed output. This glitch contains just the right amount of area to cancel the error caused by inter-symbol interference [14]. The difference between the RZ and NRZ pulse shapes is that, if the bit is 1, then the former exists for half of the time period of

the clock with twice the amplitude compared to that of the NRZ which is occupying the entire clock cycle. Figure 7.1 shows the NRZ DAC output. NRZ pulse suffers from the ISI problem but less prone to clock jitter.

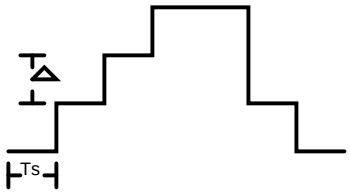

Figure 7.1: NRZ pulse shape

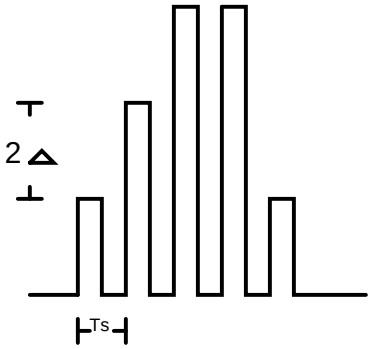

Figure 7.2: RZ pulse shape

Figure 7.2 shows the RZ DAC output of a multibit modulator. It is free of ISI problem but more sensitive to clock jitter as the amplitude of each pulse is double that of NRZ pulse and there are two transitions for every clock cycle. Figure 7.3 shows Dual RTZ wave forms, in which the pulse width of each sub DAC is for half of clock cycle and finally the two sub DAC outputs are added to get the original waveform. In the figure

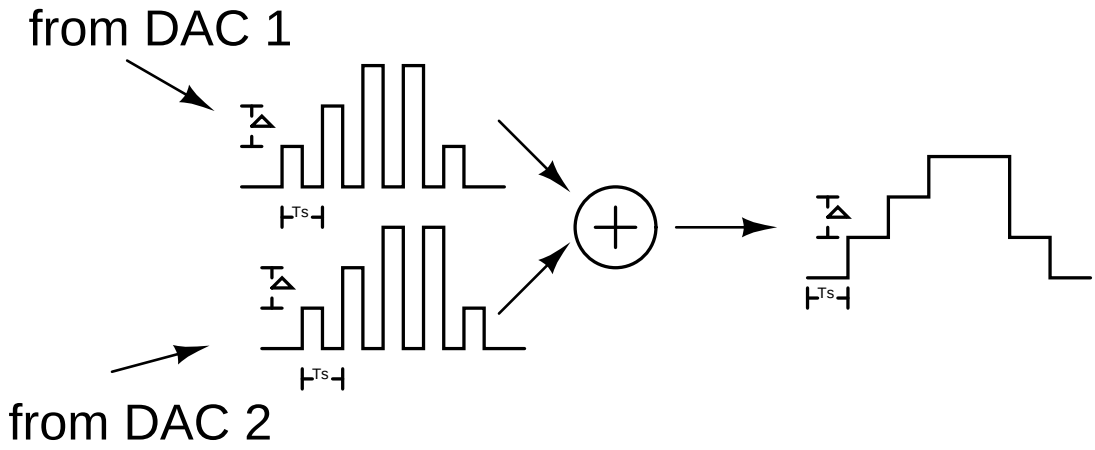

Figure 7.3: Dual RZ pulse shape of multibit modulator.

7.4 the Dual RTZ DAC has been shown. Dual RZ DAC contains 2 DAC's, for half of the clock cycle we are going to use one of the DAC and the other DAC is off i.e. it won't supply any current(feedback). Similarly in the other half of clock cycle the first DAC will be off and the 2nd one will supply the current.

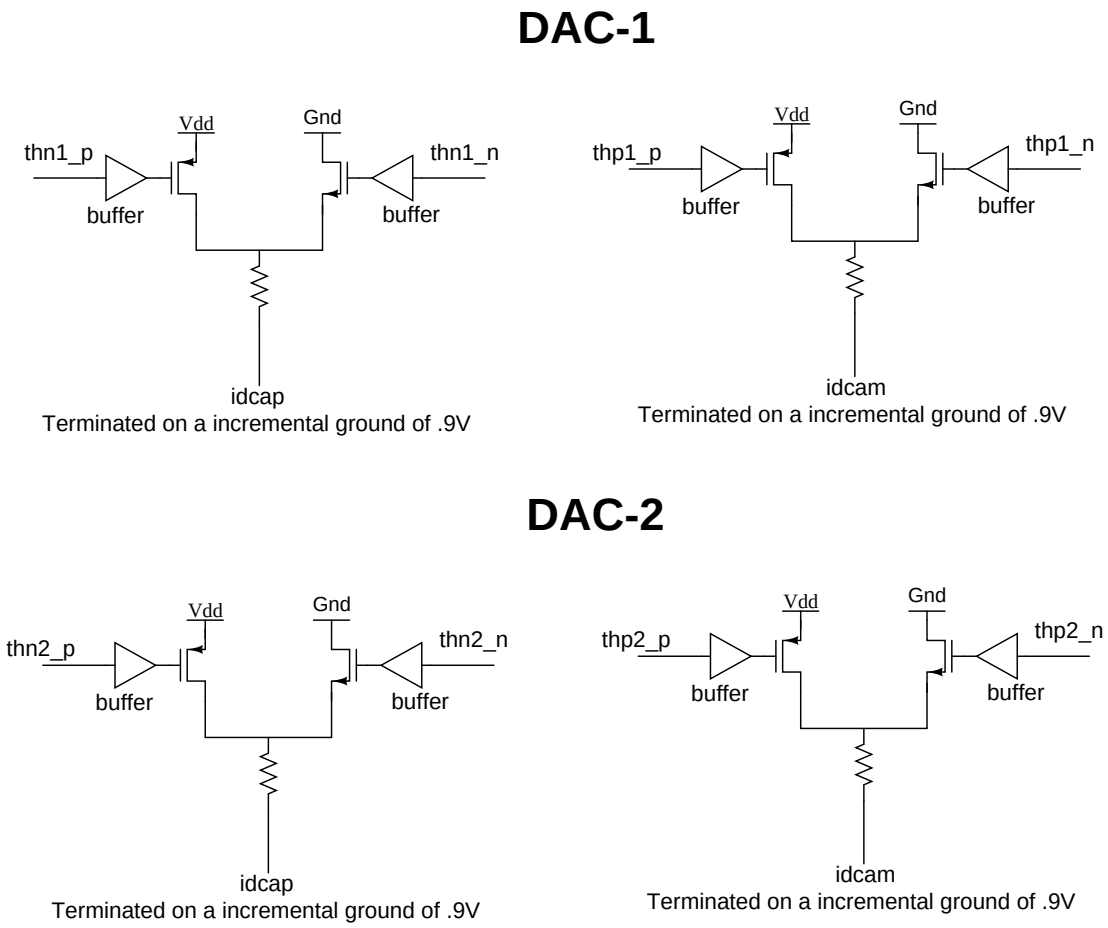

Figure 7.4: Dual RTZ DAC.

7.1.1 Dual RTZ DAC-1 and DAC-2

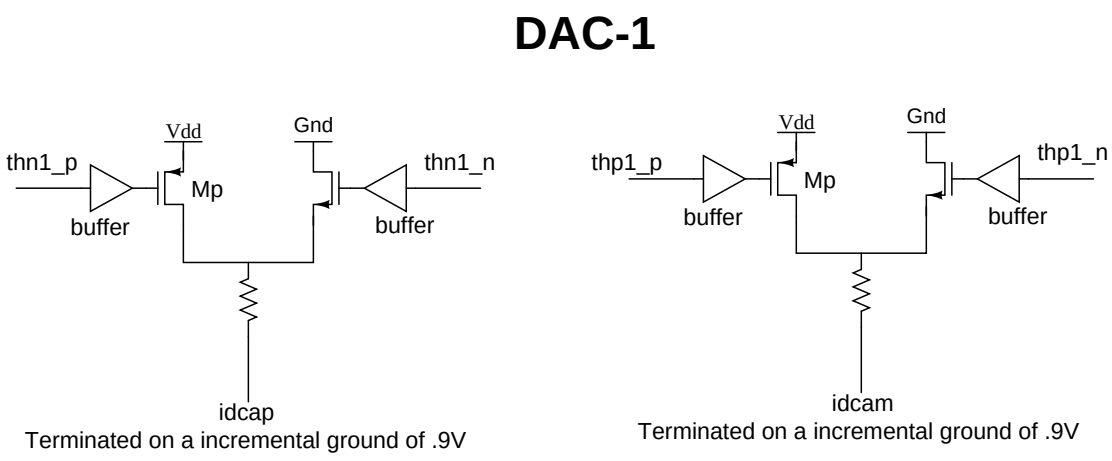

Figure 7.5: Block diagram of a Dual RTZ DAC-1.

Figure 7.5 shows the single DAC-1 element and 7.6 shows the single DAC-2 element. Here for first half of clock cycle DAC-1 will supply the current. In this first half cycle the second DAC is off that is it wont supply any current. In the second half of clock

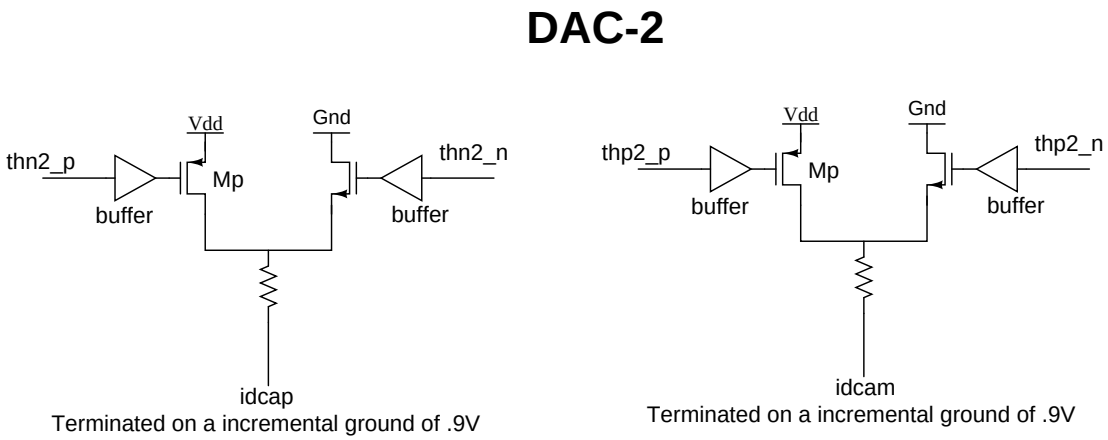

Figure 7.6: Block diagram of a Dual RTZ DAC-2.

cycle DAC-1 is off and DAC-2 will supply the current. Since this is a resistive DAC and we are not using DAC-1 in the 2nd half of clock cycle, different driving signals are used. So that in the 2nd half the driving signals are applied in such a way that these will turn off the mos switches(both pmos and nmos), so that no feedback current flows.

7.1.2 Dual RTZ DAC-1 and DAC-2

7.2 Complexity of DEM

The DAC shown in figure 7.4 is a resistive DAC having Mos switches which are controlled by DEM driving signals. In the earlier design the total number of unit DAC elements were 30, with 30 pmos and 30 nmos switches. The total number of driving signals in the earlier case are 30, but with the Dual RTZ DAC we are supposed to ON and OFF these mos switches for every half of clock cycle and there are two DAC's, which increases the complexity of DEM, since it has to generate those signals. We need 120 driving signals, and the logic also differ from the earlier one which will increase the area and power consumption. The switching action is same irrespective of whether dem is ON or OFF. The new DEM block is shown in figure 7.7

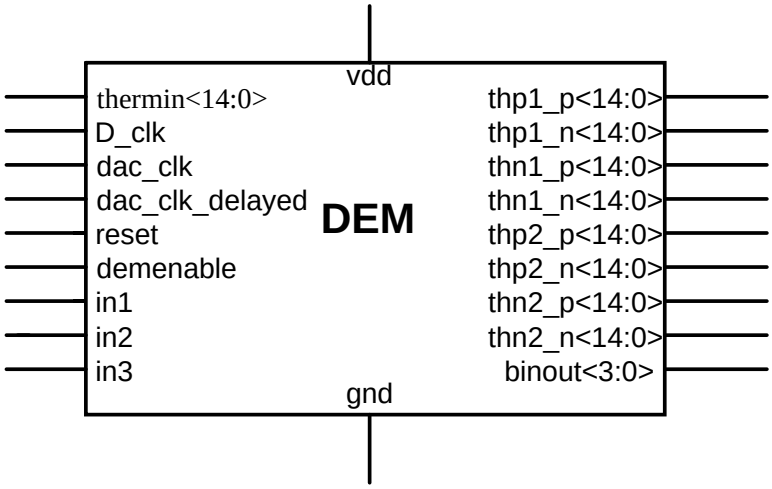

Figure 7.7: Block diagram of a DEM block.

7.2.1 DEM enable vs disable

In the earlier design when DEM was enabled, the switching actions in the DAC were more compared with the disabled case. But with the new DEM technique which suits for Dual RTZ DAC, the switching actions are same irrespective of DEM enabled or disabled. Lets take an example of thermin = 000000000001111 for the first cycle and changes to 000000000011111 in the next cycle. For this case the driving signals of DAC-1 are listed in the below table. In table 7.1 the number of switching actions for

Table 7.1: DEM output signals

DEM (on/off)	1^{st} half cycle1	2^{nd} half cycle1	1^{st} half cycle2	n^{nd} half cycle2
$thp1\_p$(off)	000000000001111	111111111111111	000000000011111	111111111111111
$thp1\_p$(on)	000000000001111	111111111111111	000001111100000	111111111111111

$thp1\_p$(off) and $thp1\_p$(on) from 1^{st} half cycle1 to 2^{nd} half cycle1 are 11, from 2^{nd} half cycle1 to 1^{st} half cycle2 are 10 and from 1^{st} half cycle2 to n^{nd} half cycle2 are 10. So the number of switching actions are same for both, DEM enabled and disabled cases. This is same in the tables 7.2,7.3 and 7.4 also.

Table 7.2: DEM output signals

DEM (on/off)	1^{st} half cycle1	2^{nd} half cycle1	1^{st} half cycle2	n^{nd} half cycle2
$thp1\_n$(off)	000000000001111	000000000000000	000000000011111	000000000000000
$thp1\_n$(on)	000000000001111	000000000000000	000001111100000	000000000000000

Same as the case for DAC-2 driving signals also with a half clock cycle delay. It is

Table 7.3: DEM output signals

DEM (on/off)	1^{st} half cycle1	2^{nd} half cycle1	1^{st} half cycle2	n^{nd} half cycle2
$thn1\_p$(off)	111111111110000	111111111111111	111111111100000	111111111111111
$thn1\_p$(on)	111111111110000	111111111111111	111110000011111	111111111111111

Table 7.4: DEM output signals

DEM (on/off)	1^{st} half cycle1	2^{nd} half cycle1	1^{st} half cycle2	n^{nd} half cycle2
$thn1\_n$(off)	111111111110000	000000000000000	111111111100000	000000000000000
$thn1\_n$(on)	111111111110000	000000000000000	111110000011111	000000000000000

observed from the above tables that the number of transitions for every half cycle and for every driving signal is same irrespective of whether dem is enabled or disabled.

7.3 Simulation Results

In order to evaluate the performance of the modulator transient simulations are performed, with various blocks of the modulator in the ideal view, some are in schematic and some are in extracted view which is obtained after layout. The simulation results in table 7.5 are when all the blocks are in ideal except the DAC which is in schematic view. The simulation results in table 7.6 are when all the blocks are in ideal except the DAC which is in RC extracted view, the corresponding power spectrum is shown in the figure 7.8. The simulation results in table 7.7 are when the mismatch is introduced in the DAC resistors which is in schematic view and all the other blocks are in ideal.The corresponding power spectrum for this is shown in the figure 7.9. The mismatch which is introduced in the DAC elements is of the value which is mentioned in [1] to be $\sigma_{\frac{\Delta R}{R}}$ = 0.055 %.

dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	122.8966	135.4086	123.1473
ON	125.2444	135.3547	125.6899

Table 7.5: SNDR, SDR and SNR when the DAC is in schematic view

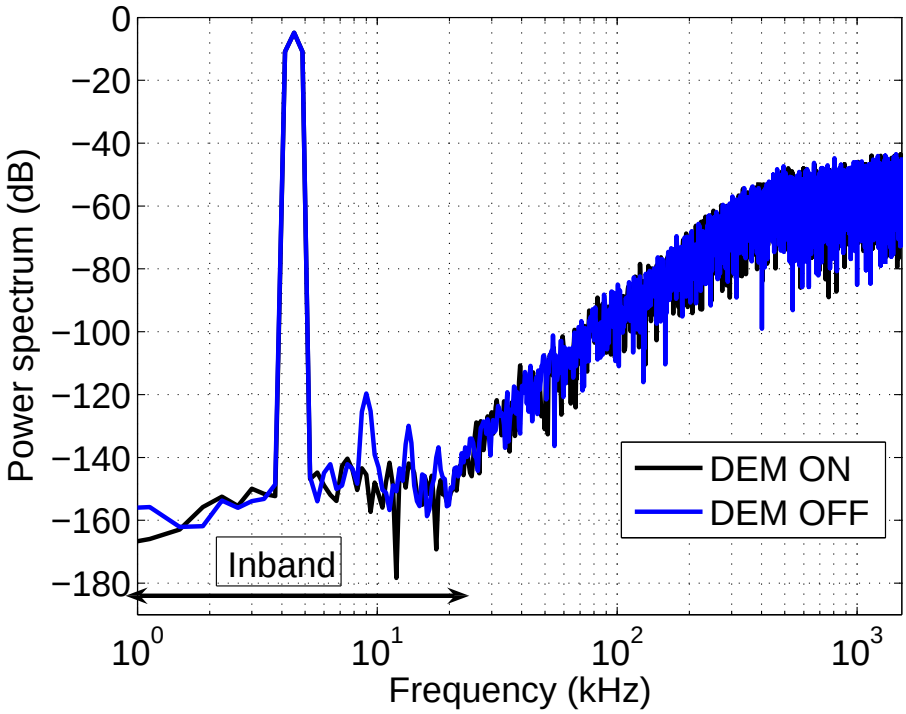

Figure 7.8: Power Spectrum.

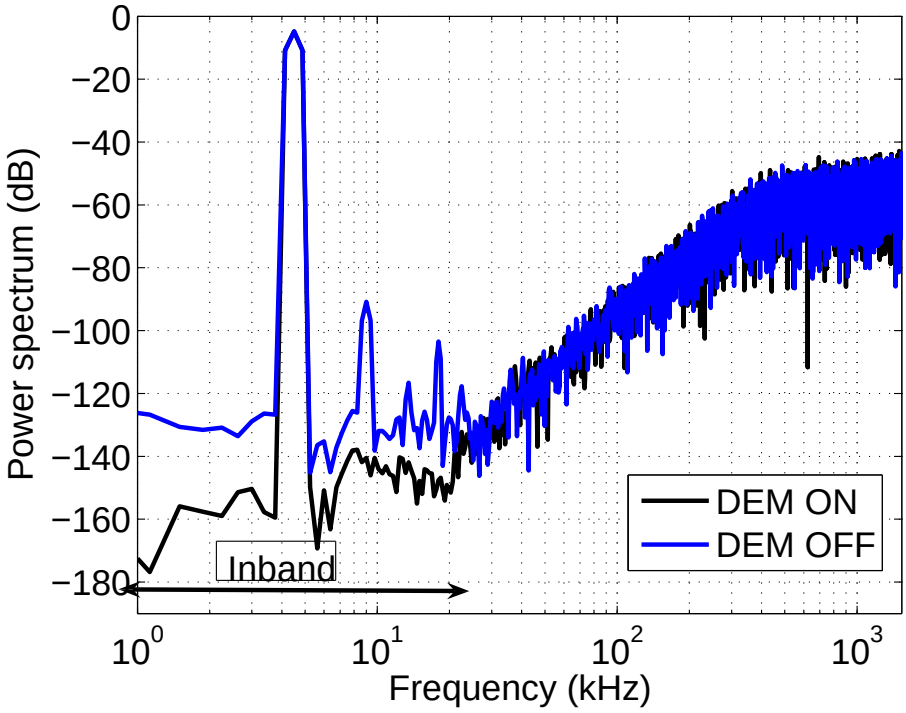

Figure 7.9: Power Spectrum.

dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	113.8745	114.1955	125.3464
ON	125.3025	133.2084	126.0698

Table 7.6: SNDR, SDR and SNR when the DAC is in RCx view

dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
OFF	85.7384	85.7646	107.9551
ON	121.5745	131.4636	122.0446

Table 7.7: SNDR, SDR and SNR by introducing mismatch in the DAC resistors

7.4 Effect of 1^{st} Op-amp

The above simulation results are when the test-bench contains all ideal blocks except the DAC. When the simulations are ran with all the blocks in schematic level, it is found that the problem still persists and that is due to 1^{st} Op-amp. This is found by ideal test-bench, by changing the first Op-amp to its schematic level. When all the blocks are ideal, except Op-amp1 and DAC, the SNDR was around 106dB in both DEM enabled and disabled cases. Almost 20 dB off between the previous results and in this case. In this case third harmonic is dominant and due to this the SNDR is less. There are several methods mentioned below to increase the SNDR.

One option is to increase the bias current of the 1^{st} Op-amp, so that it's slew rate increases. The actual bias current for the 1^{st} Op-amp is 1μA. By increasing the bias current of the 1^{st} Op-amp from 1μA to 1.5μA, and then to 2μA the results are improved and these results are shown in table 7.8. We can see from the figure 7.10 that the 3^{rd} harmonic decreases when the bias current increases. In the below tables the mentioned results are when the test-bench contains all the blocks in ideal except Op-amp1 and DAC. One more technique is to double the sizes of 1^{st} Op-amp and also double the

bias current	dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
1μA	OFF	106.5568	106.6911	121.7215
1.5μA	OFF	114.6961	115.1672	124.5764
2μA	OFF	120.0926	121.6590	125.2811

Table 7.8: SNDR, SDR and SNR for different bias currents of 1^{st} Op-amp

bias current, which results in the increase in the SNDR compared to the above cases.

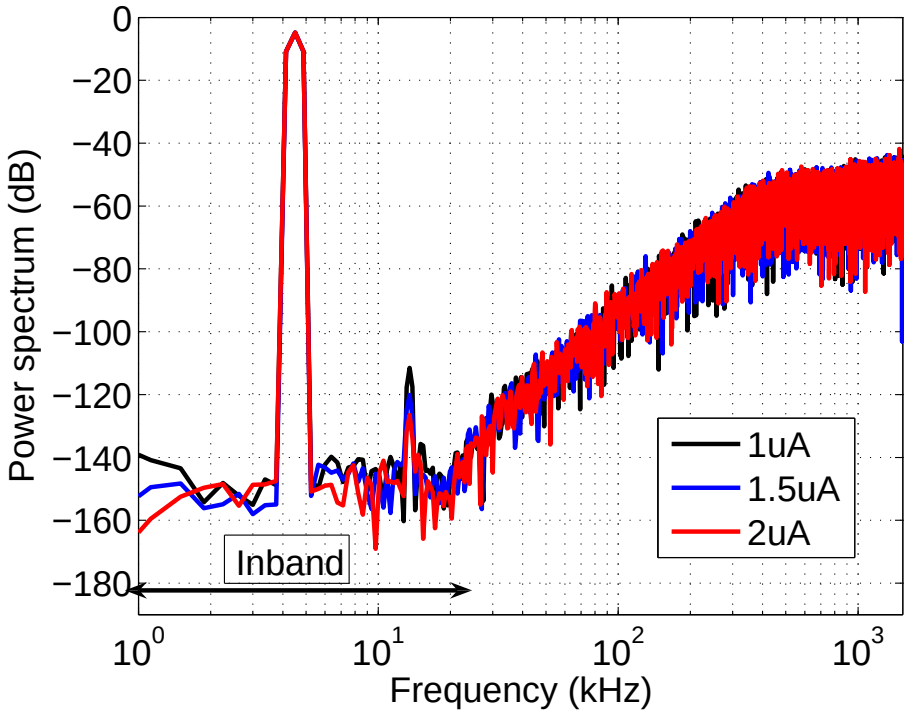

Figure 7.10: Power Spectrum.

The simulation results are shown in the table 7.9 for two different bias currents and the corresponding spectrum is shown in the figure 7.11

bias current	dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
2μA	OFF	120.9149	122.9047	125.2617
2.5μA	OFF	123.7644	127.4143	126.2173

Table 7.9: SNDR, SDR and SNR for different bias currents of 1^{st} Op-amp

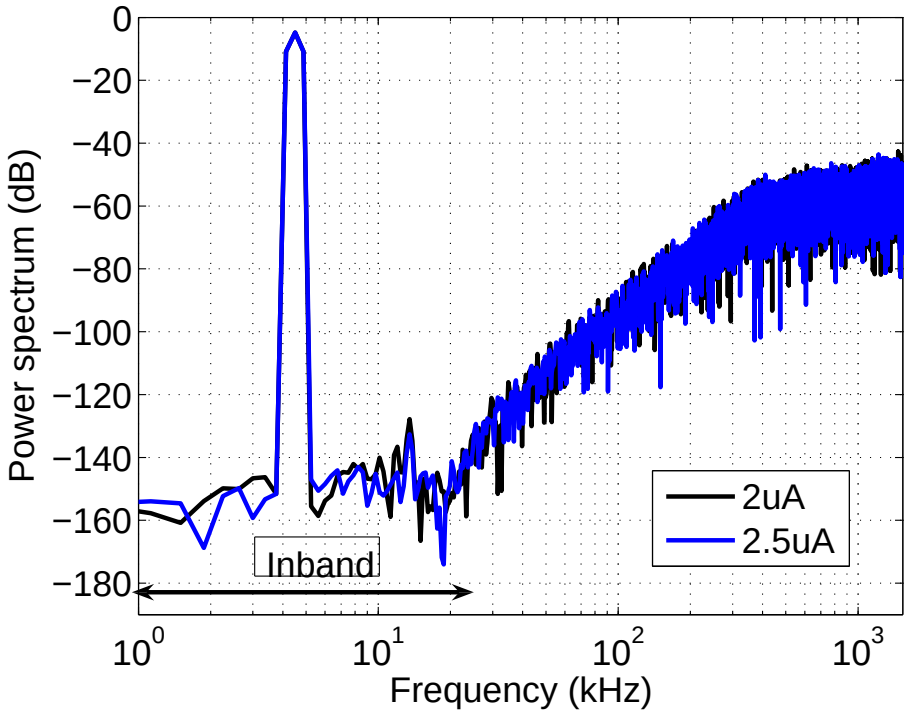

Figure 7.11: Power Spectrum.

7.4.1 Simulation Results

In this subsection the final simulation results when the bias current of 1^{st} Op-amp is doubled and with all the blocks in the schematic view are shown in the table 7.10 and the corresponding power spectrum is shown in the figure 7.12

bias current	dem ON/OFF	SNDR (dB)	SDR (dB)	SNR (dB)
2μA	OFF	116.7492	117.7835	123.4874
2μA	ON	119.7248	121.0936	125.4056

Table 7.10: SNDR, SDR and SNR - schematic view

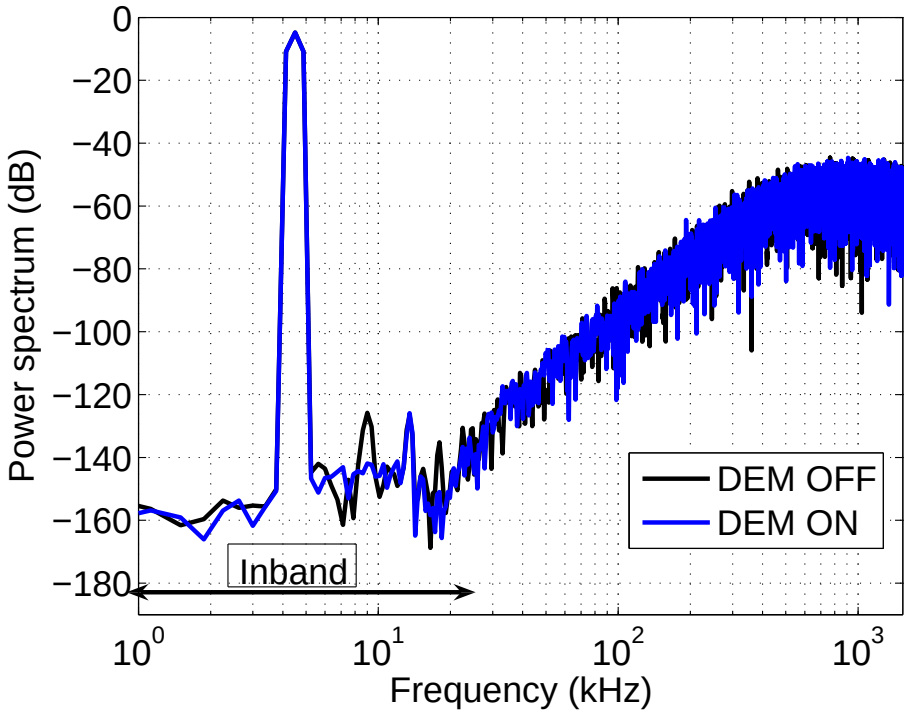

Figure 7.12: Power Spectrum.

7.5 Power consumption

The total power consumption of various blocks is tabulated in Table 7.11. The most power hungry blocks in the design are the first integrator which consumes 64.53 % of the total power, the DAC which consumes 18.59 % of the total power and DEM logic which consumes 10.68 % of the total power of the modulator. The large power consumption in these blocks are attributed to the very small noise contribution from these blocks to attain the 108 dB performance for the modulator. Table 7.12 gives the summary of the $\Delta\Sigma$ modulator design.

Table 7.11: Power consumption of the $\Delta\Sigma$ modulator blocks

Component	**Current (μA)**
Loop Filter	653.5
Flash ADC	4.0
Clock generator	11.0
DEM Logic	100.97
DAC	175.8
Total	945.27

Table 7.12: Summary of the $\Delta\Sigma$ modulator design

Specification	**Value**
Sampling frequency	3.072 MHz
Bandwidth	20 Hz - 24 kHz
Quantizer range	3 Vpp,differential
Peak SNR	108 dB
Power	1701.48 μW(1.8 V)
Supply voltage	1.8 V
Technology	0.18 μm CMOS

CHAPTER 8

Conclusions

A continuous-time $\Delta\Sigma$ modulator targeting a resolution of 18 bits (108 dB SNR) to digitize the signal in the bandwidth of 20 Hz - 24 kHz is designed in a 0.18 μm CMOS process with 1.8 V supply.The issues found in the earlier design [1] are solved by using Dual Return to Zero DAC. The slew-rate of the first Op-amp is improved by doubling the sizes to get the expected simulation results.

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