Power Optimization of a 15 bit Continuous Time Delta-Sigma Modulator for Audio Band Applications

A Project Report

submitted by

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CERTIFICATE

This is to certify that the thesis titled **Power Optimization of a 15 bit Continuous Time Delta-Sigma Modulator for Audio Band**, submitted by **Malepati Srinivasulu**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I would like to dedicate this thesis to my parents and my brother for their support and encouragement through my entire student life.

ABSTRACT

The project involves power optimization of a continuous time delta-sigma modulator for audio band applications. The design Dwani[**?**] is a power optimized 3rd order system with OSR of 64 and uses a quantizer of 4 bits. This modulator operates in $0 - 24kHz$ range consung a power of 121μW. This power includes power consumed by reference generation circuit also. It achieves a resolution of 15 bits.

In the current design the modulator works with an OSR of 32 which cuts down the power consumed by digital circuitry by a factor of 2. The operational amplifiers in loop filter are replaced with feed-forward compensated op amps as they are more power efficient. The current design consumes a power of 90μW including reference generation circuit. There is a provision to deactivate DEM block in order to activate calibration unit vice-versa to minimize the errors due to DAC elements effectively. Appropriate design techniques are used to make the design robust with respect to process and temperature variations. The design is implemented in 0.18μm CMOS process from UMC with a supply voltage of 1.8V.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CIFB	Cascaded Integrators with distributed feedback
CIFF	Cascaded Integrators with distributed feedforward
CMFB	Common Mode Feed-Back
CT	Continuous Time
DT	Discrete Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DSM	Delta Sigma Modulator
DWA	Data Weighted Averaging
GBW	Gain Bandwidth
LSB	Least Significant Bit
MSA	Maximum Stable Amplitude
MSB	Most Significant Bit
NTF	Noise Transfer Function
OBG	Out of Band Gain
PSD	Power Spectral Density
RNS	Residual Number System
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
STF	Signal Transfer Function
$V_{pp,diff}$	Peak to Peak Differential Voltage

CHAPTER 1

Introduction

1.1 Motivation

In System-on-a-chip(SoC) design most of the processing is done in digital domain as the digital signals are less susceptible to noise and VLSI process are optimized for high density digital design. But the real world signals are all analog in nature and hence data converters are required to interface analog world signals with the digital signal processors. So, analog to digital converters plays important role in SoC design.

Data converters are characterized by conversion speed, resolution and power consumption. The motive of the present work is to minimize the power consumption of an earlier design named Dhwani [1] which is continuous time $\Delta\Sigma$ modulator designed for audio band applications with 16-bit resolution. It employs a third order modulator with OSR of 64 and consumes a power of $121\mu W$. The decimation filter folling the modulator consumes a power of $100\mu W$. The current design is targetted to minimize the power consumption. This could be achieved by reducing the OSR to 32 which decreases the power consumed by the digital circuitry as the switching rate is reduced. The OSR can be lowered because the earlier design over-achieved the requied SQNR. By implementing power efficient design of op amps in the loop filter, the power consumed by the analog circuiry can be brought down.

1.2 Organization

Chapter 2 explains the design of the loop filter which plays a major role in modulator.

Chapter 3 explains the design of the operational amplifiers used in the loop filter.

Chapter 4 explains the generation of reference voltages and bias currents for the flash, feed back DAC and the loop filter op amps.
Chapter 5 concludes the thesis with the simulation results.

CHAPTER 2

Loop Filter

In a $\Delta\Sigma$ modulator the in band SQNR is improved by shaping out of quantization noise. The quantization noise is shaped out of the signal band by the loop filter by the virtue of its high gain in the signal band. This chapter discusses the design of a third order loop filter with zeros optimized for a multibit $\Delta\Sigma$ modulator. The block diagram a $\Delta\Sigma$ modulator is shown in figure 2.1

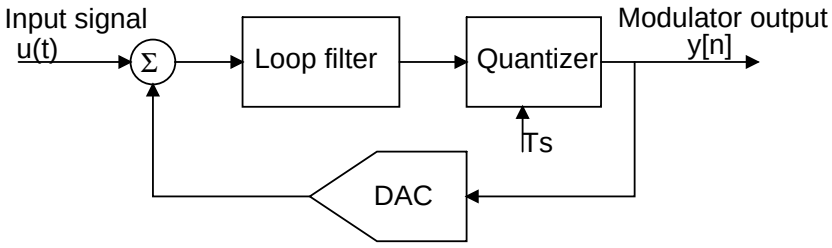


Figure 2.1: Block diagram of $\Delta\Sigma$ modulator

2.1 Selection and implementation of loop lilter transfer function

In the design of a $\Delta\Sigma$ modulator the first step is the choice of the modulator order and its noise transfer function(NTF) [1]. A third order modulator with an OSR of 32, 4-bit internal quantizer and zeros optimized gives a signal-to-quantization noise ratio of around 109 dB. The NTF of the modulator has an out-of-band gain (OBG) of 3. OBG is defined as the gain of the NTF at frequencies close to $\omega = \pi$. The NTF zeros are optimised to achieve an inverse Chebyshev characteristic, thus introducing a higher SNR. The modulator with required characteristics is simulated using MATLAB tool.

The following steps were followed to find the transfer function of the CT loop filter:

1. Using the $\Delta\Sigma$ toolbox in MATLAB the NTF of a 3rd order descrete time $\Delta\Sigma$ modulator with an OBG of 3 with zeros optimization is determined.

$$NTF(z) = \frac{(z-1)(z^2 - 1.994z + 1)}{(z - 0.3556)(z^2 - 0.6603z + 0.304)} \tag{2.1}$$

2. The DT loop filter transfer function $L(z)$ is given by:

$$L(z) = \frac{1}{NTF(z)} - 1 \tag{2.2}$$

3. The impulse invariance transformation is used to determine the transfer function $L(z)$ of the equivalent CT modulator. The normalized sampling interval is 1 s.

$$L(s) = \frac{1.367s^2 + 1.087s + 0.415}{s^3 + 0.005783s} \tag{2.3}$$

The above equation for $L(z)$ can implemented by a cascade of three integrators with 2^{nd} and 3^{rd} integrators connected to form a resonator and a summer. Figure 2.2 shows the block diagram for the implementation of $L(z)$.

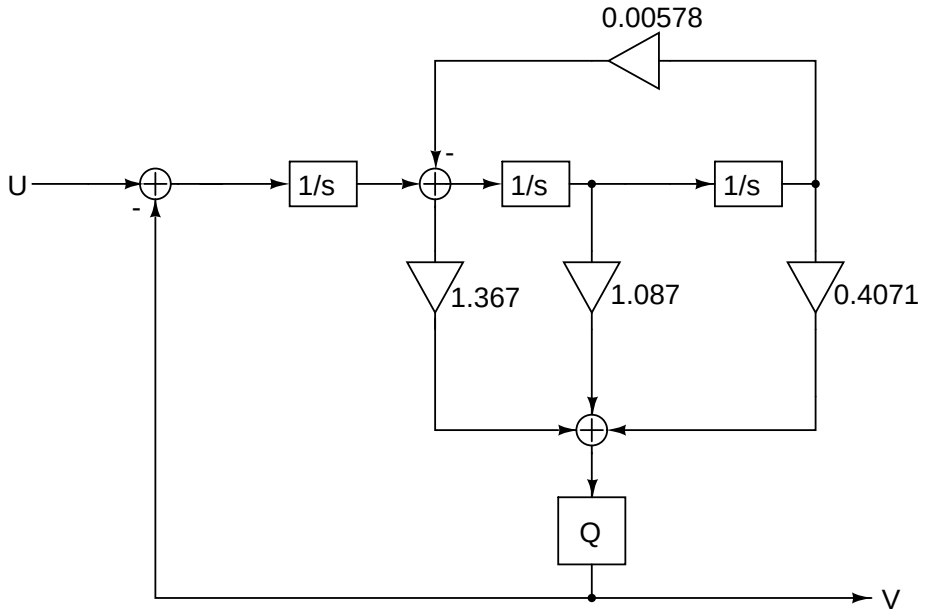


Figure 2.2: Block diagram of 3rd order CT loop filter for $T_s = 1s$

It is now necessary to perform dynamic range scaling. Dynamic range scaling is necessary to ensure that all nodes have approximately the same voltage swing, so that all nodes will clip at same level. After dynamic range scaling all nodes have the same maximum output level. Dynamic range scaling is done as follows: The maximum output level of each integrator is determined by MATLAB simulation. The maximum outputs of all integrators are set to the same level by adjusting their gains. To increase the output level at a node by a factor of k, the input branches should be multiplied by k while the output branches should be divided by k. The block diagram of loop filter after dynamic node scaling is shown in figure 2.3.

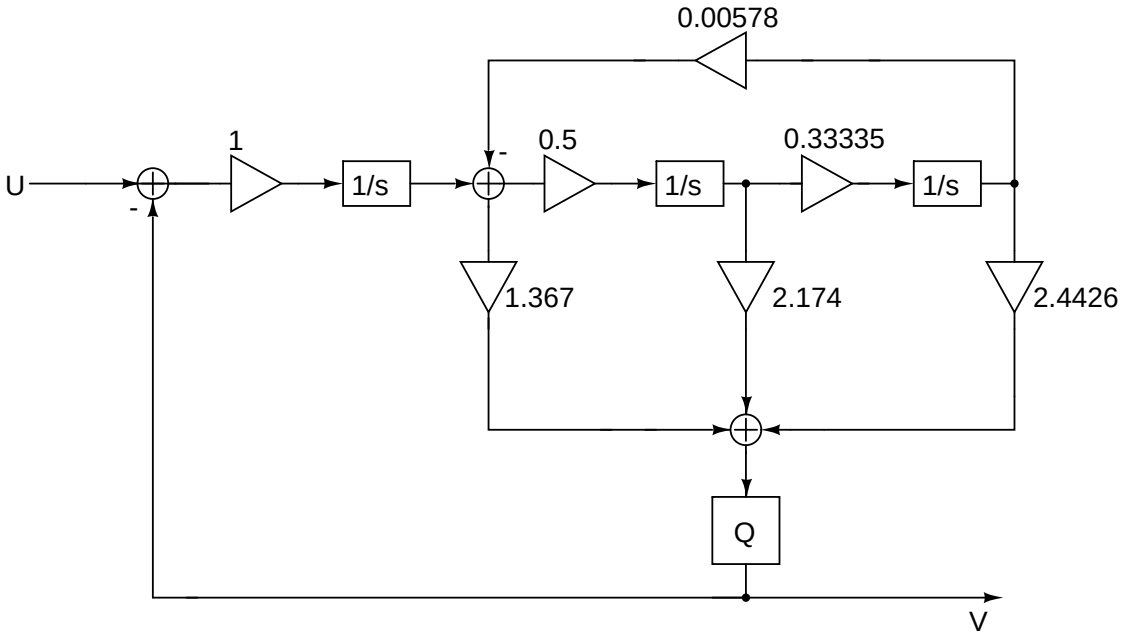


Figure 2.3: Block diagram of 3rd order CT loop filter after dynamic-range scaling for $T_s = 1s$

Figure 2.4 shows the prototype model of the CT loop filter implemented using ideal opamps for $T_s = 1s$.

The CT model shown in figure 2.4 needs to be frequency scaled to the frequency of operation of the modulator i.e $f_s = 1.536MHz$. The loop filter obtained after frequency scaling and node scaling is shown in figure 2.5. The 1^{st} integrator input resistance is kept at $200K\Omega$ to constrain the in band noise so that the in band SNR due to random noise is 93 dB.

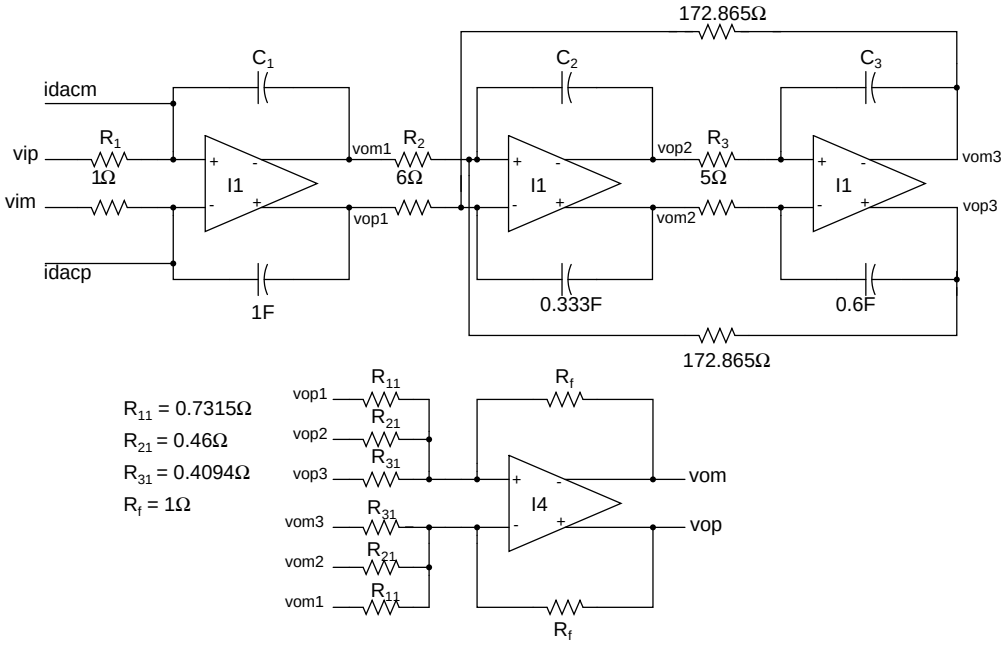


Figure 2.4: Loop filter with ideal op amps after dynamic-range scaling for $T_s = 1s$

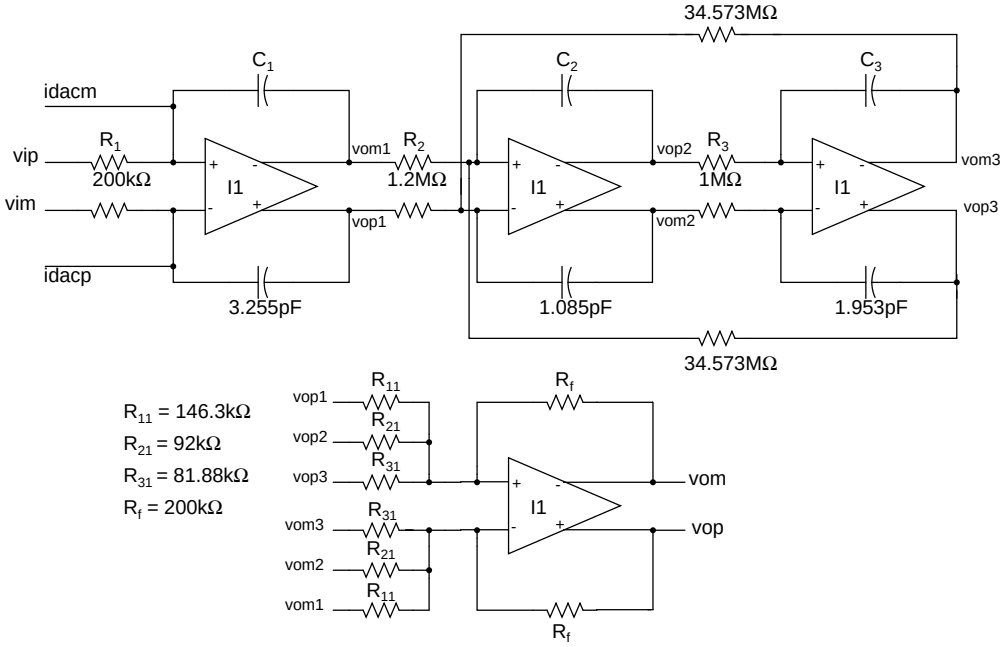


Figure 2.5: Loop filter with ideal op amps for $f_s = 1.536MHz$

2.1.1 Reduction of NTF zero optimization resistance

From figure 2.5 It is observed that R_{31} is excessively large for an on chip resistance ($34.573M\Omega$). This is because we are generating a current $\frac{v_{op3}}{R_{31}}$ from a large swinging node v_{op3}. If the node voltage is scaled down by factor of k by means of a potential divider and if we generatye current from the low swing node, then R_{31} can be reduced by k times. If we reduce the voltge by a factor of 10 then the required R_{31} is $3.573M\Omega$. The Thevenin equivalent of the resistive divider is $0.09M\Omega$. So externally, $3.3673M\Omega$ should be connected. Resistive divider circuit is shown in figure 2.6. The final structure after scaling the resonator resistance is shown in figure 2.7. The potential divider network can be realized in practice using the resistors used for sensing the common mode voltage of the 2nd stage of the 3rd op-amp.

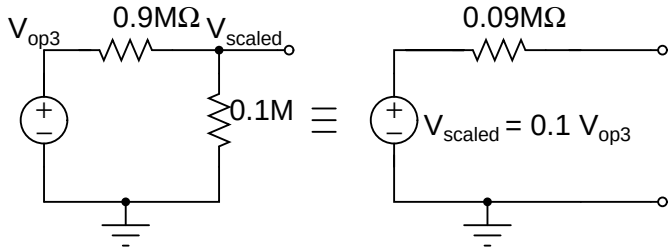


Figure 2.6: Thevenin equivalent of the resistive divider circuit

The loop filter shown in the figure 2.7 is realized using ideal opamps and a sigma delta modulator schematic is built. 4-bit flash converter and resistive DAC are realized using VerilogA codes. Figure 2.8 shows the frequency spectrum of the output of the modulator. The notch in the audio band can be observed in the plot. The SQNR is computed and it matches with the ideal SQNR obtained from the initial MATLAB simulations (109 dB).

The capacitor Cs which is in parallel with R_{11} in figure 2.7 provides direct path for compensating excess loop delay. The equivalent gain of the direct path provided by this capacitor is $\frac{C_s R_f}{C_1 R_1}$[2].

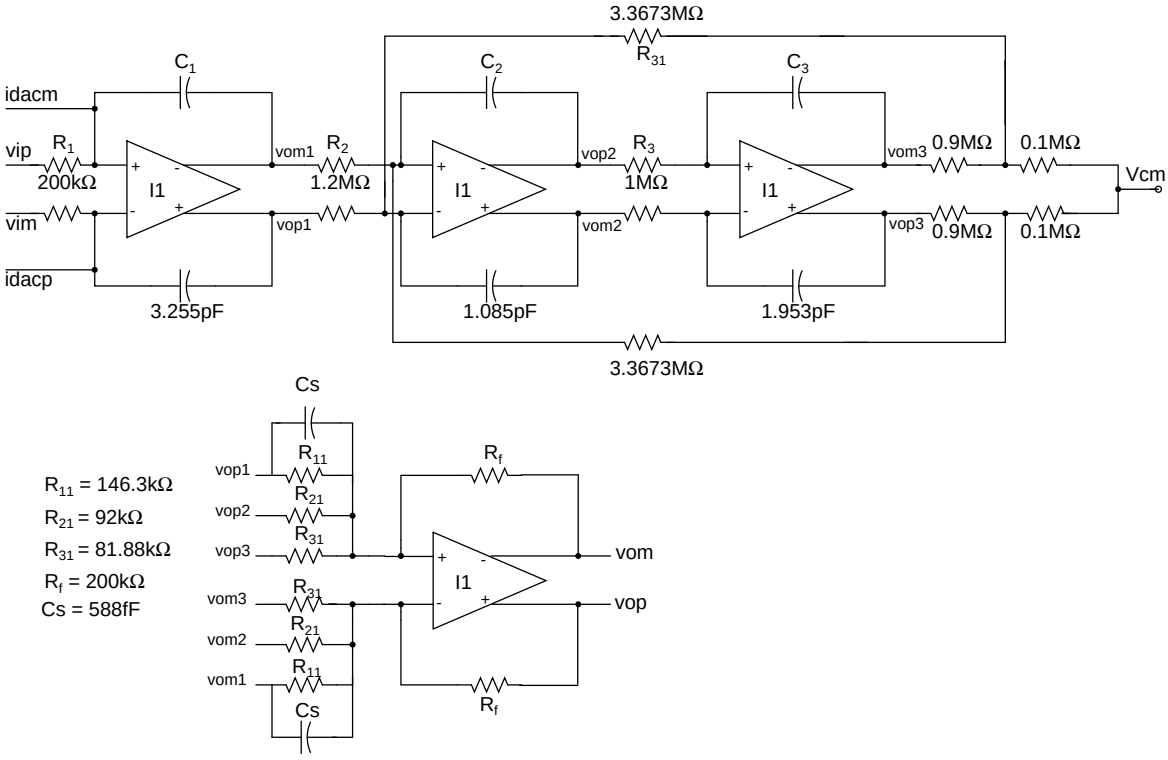


Figure 2.7: Loop filter with ideal op amps and scaled NTF zero optimization resistance

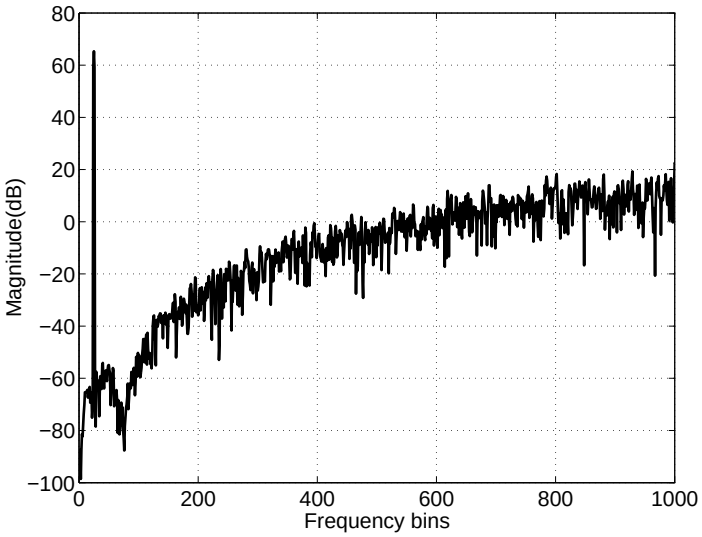


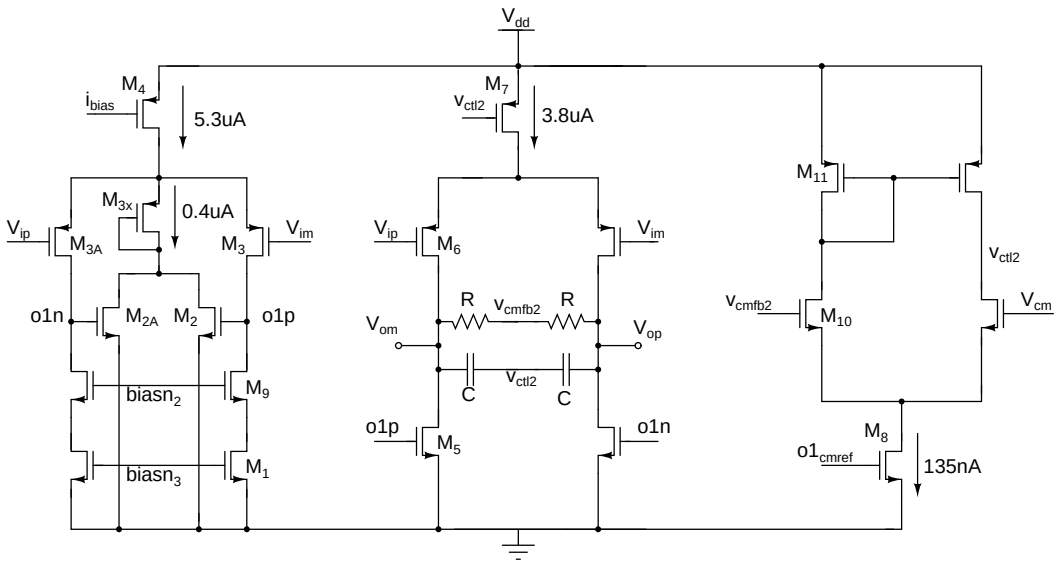
Figure 2.8: PSD of the modulator output

CHAPTER 3

Op-amps used in the loop filter

3.1 First Integrator Op Amp

The first integrating op amp needs to be designed carefully as it determines the overall distortion and noise of the data converter. Noise and non-linearities of the succeeding op amps becomes insignificant when referred back to the input. Hence the design of first opamp is critical. It is a two stage opamp and is implemented using a feedforward topology as it is more power efficient than Miller compensation. Figure 3.1 shows the schematic of the first op amp.



M_1-40(3/12)	M_4-84(1/1)	M_8-2(0.5/2)	C = 200fF
M_2-4(0.5/2)	M_5-24(1/4)	M_9-12(1/1)	R = 1MΩ
M_3-24(2/2)	M_6-10(1/1)	M_{10}-24(0.5/2)	
M_{3X}-8(1/1)	M_7-80(1/1)	M_{11}-2(0.5/0.4)	

Figure 3.1: First Integrator Op Amp

First stage of the opamp is telescopic differential pair. Noise contribution of the first stage is major consideration while choosing the op amp input stage. Flicker noise or $\frac{1}{f}$ noise is the major source of noise at low frequencies. P-channel

transistors have less flicker noise when compared to N-channel transistors so we have chosen P-channel transistors for the input stage. It therefore minimizes the overall input referred noise of the loop filter. In the first stage cacode current mirror load is used for differential pair. Cascoding increases the gain of the first stage.

The second stage of the op amp is a class A amplifier. Feed forward compensation is implemented in this stage. A feedforward stage is added by current reuse method. The linear model of the feedforward amplifier is shown in figure 3.2.

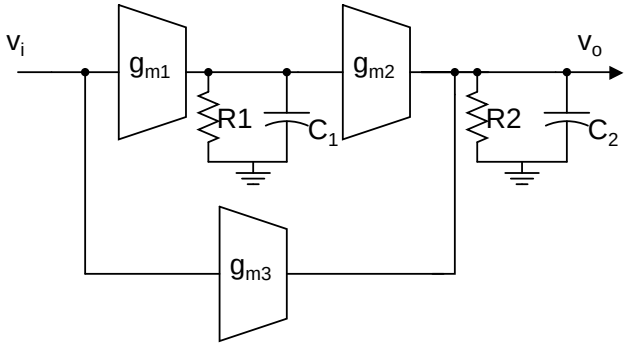


Figure 3.2: First Integrator Op Amp

Feedfrorward compensation adds a left half plane zero near the second pole of the op-amp which makes the system look like a first order system at the unity gain frequency .i.e, the magnitude response rolls off at 20dB/decade at the unity gain frequency. The approximate zero location is given by the following expression.

$$w_z \cong \left(\frac{g_{m2}}{g_{m3}}\right)\left(\frac{g_{m1}}{C_1}\right) \tag{3.1}$$

If g_{m3} is large enough then effect of one pole is cancelled and system acts as if it is first order system.

This type of topology, wherein the feedforward stage and second stage share the bias current is optimal in terms of power consumption. However, this architecture limits the output swing of the op-amp. In the current application of using this op-amp in the loop filter, this problem could be alleviated by appropriate node scaling to ensure that the output swings are within the swing limits of the op-amp.

3.2 Comparison

The following table compares the various performance parameters of the first opamp in the current design with that of Dhwani's.

Parameter	Current design	Dhwani
Gain (dB)	87	84.82
Unity Gain Frequency (MHz)	25.2	27.73
Phase Margin (degrees)	54	42
First Stage Current(micro amps)	5.3	5.3
First Stage CMFB Current(micro amps)	0.4	1.4
Second Stage Current(micro amps)	3.8	6.5
Second Stage CMFB Current(micro amps)	0.135	0.55
Total current(micro amps)	9.7	13.6

Table 3.1: First integrating opamp - current design Vs Dhwani[1]

The frequency response of fully differential output is shown in figure 3.3.

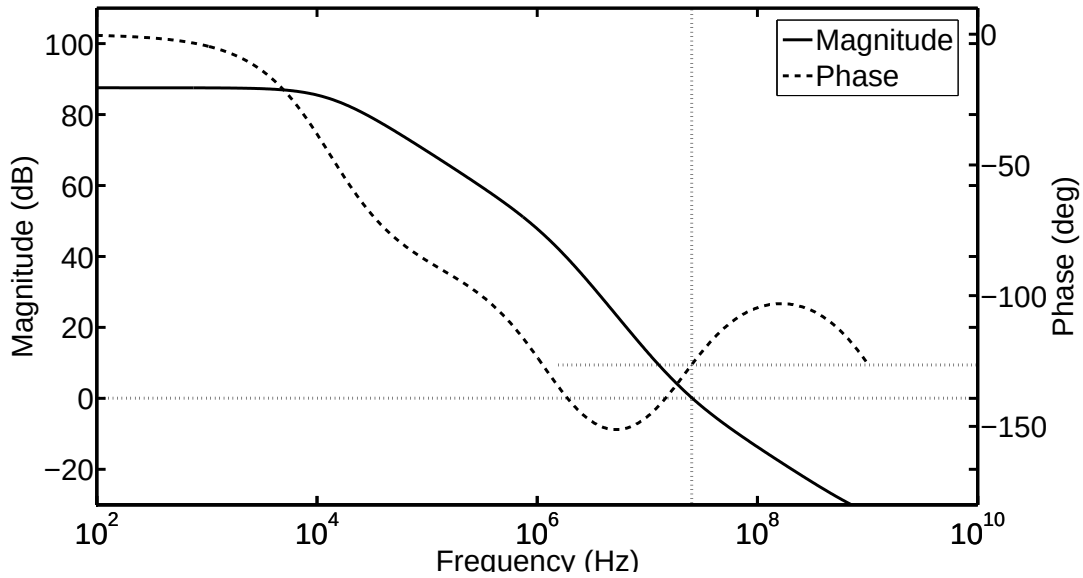


Figure 3.3: 1st integrator op amp frequency response

3.2.1 Common-Mode feedback circuits

In order to attain high gain the load resistances are replaced with current sources implemented using MOS transistors. In single ended topologies we can use current

mirroring and the overall feedback sets the output bias voltage. In fully differential topologies, the feedback network controls the differential output and additional circuitry is needed to control the common mode voltage . This circuitry is called *common-mode feedback (CMFB) circuitry.*

First stage CMFB circuitry

1st stage CMFB circuitry employs a current mode feedback to set the first stage output common mode voltage. CMFB circuit for first stage is shown in figure 3.4.

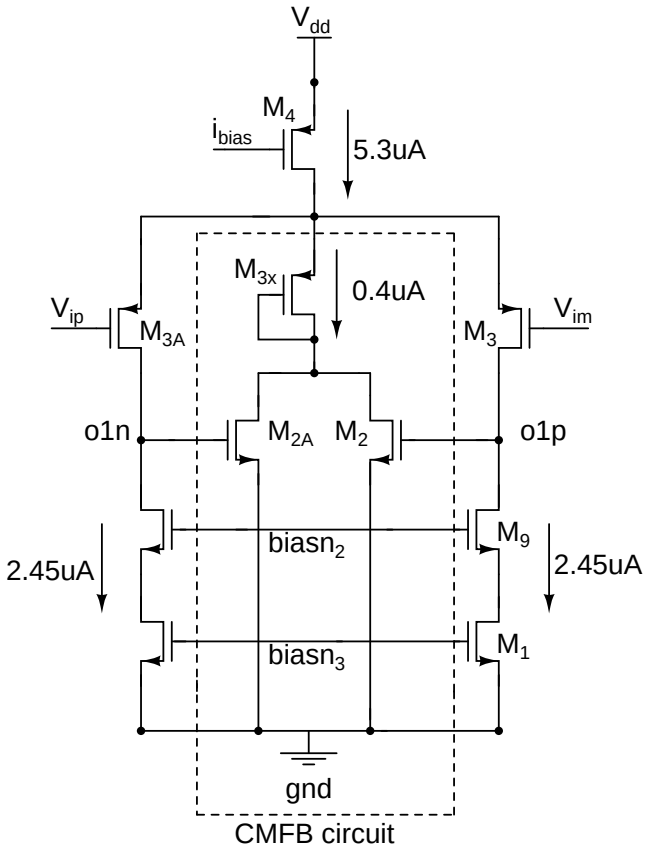


Figure 3.4: First stage CMFB circuit

Transistors M2,M2A and M3x consitutes to the common mode feed back circuit for the first stage. The total bias current through M4 is a constant(as set by i_{bias}). As long as the first stage outputs o1p and o1n are at expected common mode voltage and the change in voltages are equal and opposite the current through M3x is always constant. If output common mode voltage of 1st stage increases, current through M2 and M2A increases which in turn results in the reduction of

current through M3 and M3A. As M1 and M9 are biased at a constant current, when the current through M3 pair reduces from the expected level, the current flowing into the output node is lower that the current that is being sucked from the output node. Therefore, the output common mode voltage falls and settles to the desired voltage for which CMFB circuitry was designed. If the output common mode voltage falls below the expected value, then current through M2 and M2A decreases which causes an increase of current in M3 and M3A pair and hence the output comode voltage increases as the current flowing into the node is higher than the current flowing out.

Second Stage CMFB circuitry

The second stage CMFB circuit is a simple single ended differential amplifier. CMFB circuit for second stage is shown in figure 3.5.

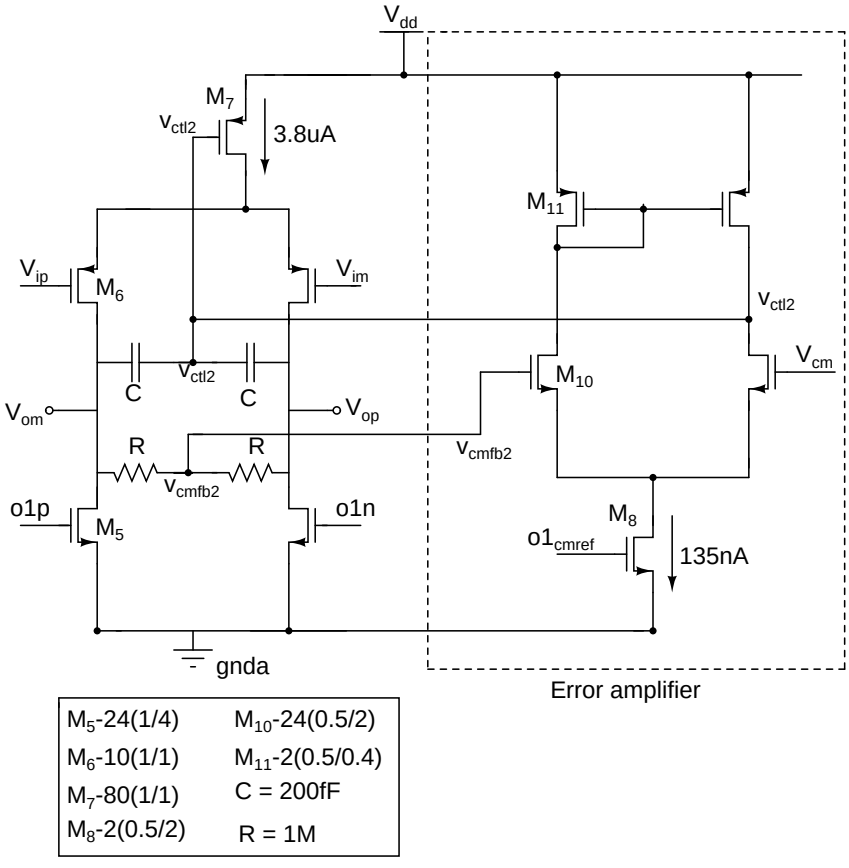


Figure 3.5: Second stage CMFB circuit

It employs sensing using resistors. Resistor value is chosen such that it does not

load the op-amp in the differential picture. The common mode voltage is detected using the resistors and is compared with the desired common mode voltage, V_{cm}. The differential amplifier's output controls the bias current of the second stage such that the output common mode voltage settles to V_{cm}. E.g., if the output common mode voltage exceeds V_{cm}, the differential amplifier output increases. This decreases the bias current of the second stage. Hence, the current that is pumped into the output node is less than that being drained out. Therefore the output voltage increases and comes back to V_{cm}. Op-amp stage and CMFB circuit together make another loop with two significant poles. So again this loop has to be freqency compensated and hence the capacitors.

The CMFB circuit's step response is shown in figure 3.9.

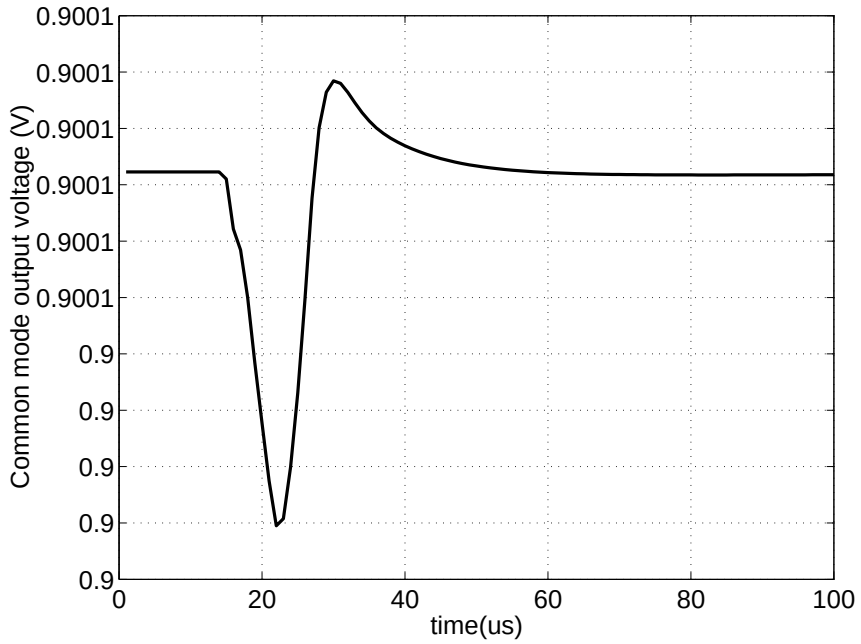


Figure 3.6: Second stage common mode feedback response of 1st integrator op amp

3.3 Noise analysis

The op amp designed is a two stage op amp where the second stage is a class A amplifier which has low output impedence and hence, the gain of the second stage is very less and first stage gain is very high. So the noise contribution of the

second stage can be neglected when referred back to the input as it is preceded by a very high gain stage. A noise analysis is run on first op-amp used in the design of Dwani [1] and it is observed that most of the noise in the first stage of the op-amp is due to the flicker noise and thermal noise of the transistor pair M1 (figure 3.1) as shown in the following table. The total input referred noise voltage at a temperature of 300K is 19.16uV.

Component	noise type	percentage contribution
M1 pair	flicker noise	15.74
M1 pair	thermal noise	9.45
Resistors	thermal noise	6.88
M3 pair	flicker noise	6.76
M3 pair	thermal noise	4.1

Table 3.2: First integrating op amp noise of Dhwani[1]

To lower the flicker noise, the dimensions of NMOS transistor pair are scaled and to lower the thermal noise the input transistor pair is pushed into subthreshold region. Transconductance is maximum for a given current in this region. The reduction in the noise gives a room to increase the resistance and yet have the same overall input referred noise of the loop filter. The resistance has been increased from 100kΩ to 200kΩ. This gives a two fold advantage. Firstly, the second stage current comes down and secondly the DAC reference current comes down by a factor two. The following table gives the noise distribution of the first integrating opamp used in the design. The total input referred noise voltage at a temperature of 300k is 14.96uV.

Component	noise type	percentage contribution
Resistors	thermal noise	23.92
M3 pair	flicker noise	14.71
M1 pair	flicker noise	7.51
M1 pair	thermal noise	1.8
M3 pair	thermal noise	1.3

Table 3.3: First integrating op amp noise in the current design

3.4 Second Integrator Op Amp

The specifications of the second stage op-amp are not so stringent because its input referred noise and distortion will come down to a large extent by virtue of the high gain of the first integrator preceding it.

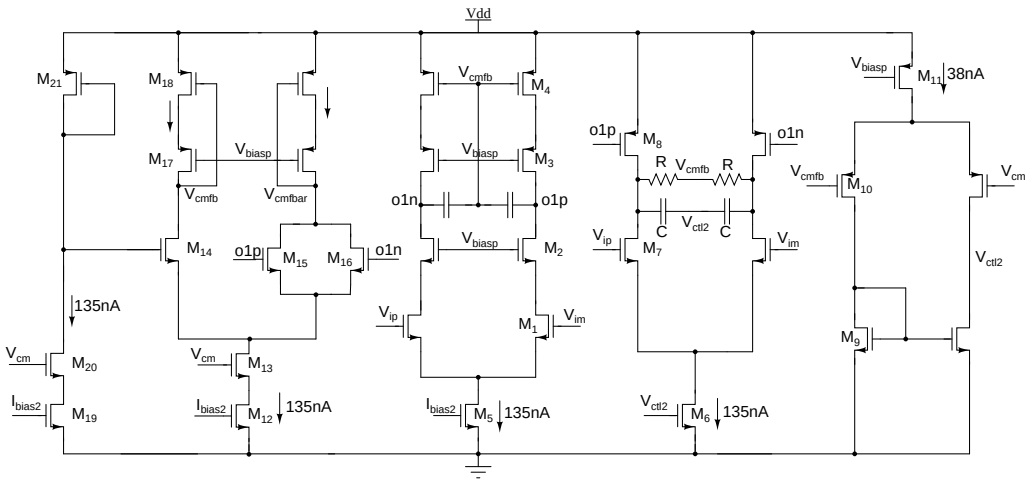


Figure 3.7: Second Integrator Op Amp

Transistor	Size	Transistor	Size
M1, M2, M7	1(0.6/0.25)	M21	16(0.5/0.5)
M3	1(0.5/0.25)	M15, M16	(0.25/4)
M4, M17, M18	2(0.5/0.25)	M14	2(0.25/4)
M5, M12, M19	2(0.5/2)	M13, M20	2(0.6/0.25)
M6	3(0.5/2)	M11	1(0.5/10)
M8	8(0.5/0.5)	M10	6(0.5/0.2)
M9	1(0.5/2)		

Table 3.4: Second integrating opamp transistor sizing

This op-amp also employs feedforward topology. Since the requirements on this op-amp are not stringent, n-channel transistors can be used as input pair. The first stage is a simple differential pair. The bias current is shared between the feedforward stage and the second stage. The CMFB circuit of the first stage is a differential pair which senses the common mode voltage and compares with the diode connected PMOS whose current density is same as the second stage input pair PMOS. It sends a correction voltage to the top PMOS pair of the first stage in a way that makes the common mode voltage nearly equal to the gate voltage of

the diode connected PMOS. The second stage employs a resistive sensing CMFB whose operation is same as in the first op-amp. The diffrential frequency response of the op-amp is shown in figure 3.8.

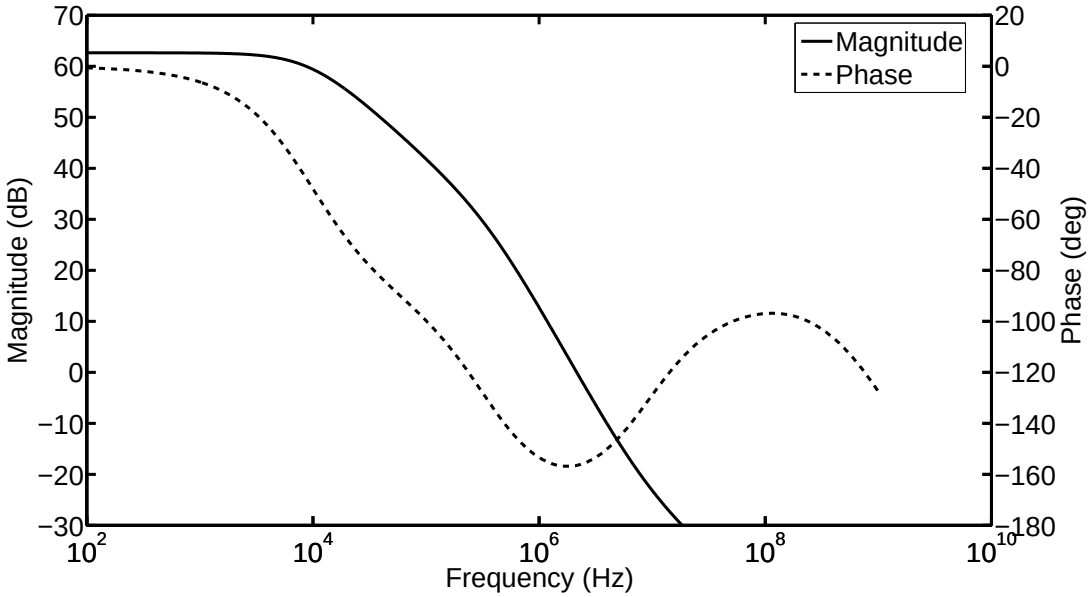


Figure 3.8: Second and third integrator op amp frequency response

The CMFB circuit's step response is shown in figure 3.9.

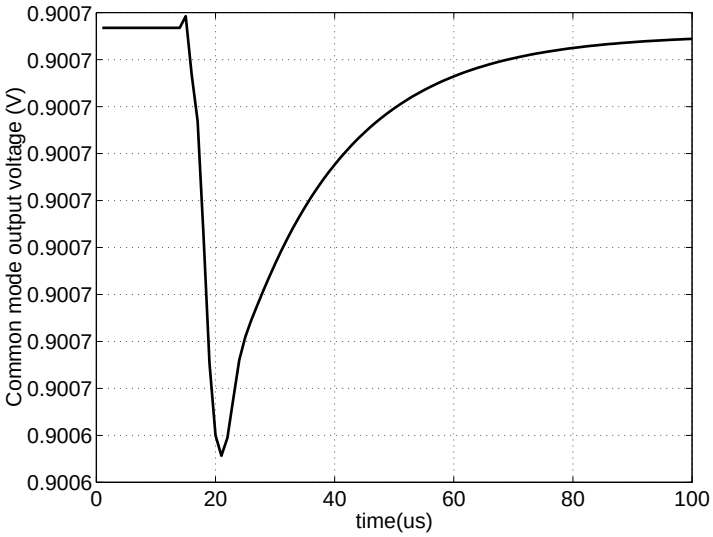


Figure 3.9: Common mode feedback response of 2nd and 3rd integrator op amp

3.5 Comparision

The following table compares the various performance parameters of the second opamp in the current design with that of Dhwani's.

Parameter	Current design	Dhwani
Gain(dB)	62	80
Unity Gain Frequency(MHz)	2.1	13
Phase Margin (degrees)	24.5	3
First Stage Current(micro amps)	0.270	0.824
First Stage CMFB Current(micro amps)	0.135	0.135
Second Stage Current(micro amps)	0.135	1
Second Stage CMFB Current(micro amps)	0.038	0.43
Total current(micro amps)	0.72	2.4

Table 3.5: Second integrating opamp - current design Vs Dhawani[1]

The third integrator uses the same op-amp as that in second integrator except that, the CMFB resistors are connected to form a series combination of 900k and 100k in order to scale down the output voltage at a node as discussed in chapter 3. The summer op-amp should have a large swing. Since feedforward compensation in current reuse topology cannot give large swings, it cannot be used. A miller compensated opamp that can swing from 0.15V to 1.65V is used[1].

CHAPTER 4

Reference Generator

In this chapter we discuss the generation of the required reference voltages and currents for the designed modulator. The references that need to be generated are:

1. The reference voltages for the internal flash ADC. The top and bottom node of the resistive ladder are held at 1.65 V and 0.15 V respectively.

2. The references for the feedback DAC. The feedback DAC must be capable of sourcing as well as sinking a current of around $3.5\mu A$.

3. The reference currents for the loop filter op amps. The first op amp of loop filter has an input bias current of $125nA$, second and third op amps require bias current of $135nA$ and the summing op amp needs $125nA$ as bias input current.

4.1 Generation of Reference Currents

Figure 4.1 shows the schematic of the reference generation circuit which is used for generating reference currents and reference voltages for the various blocks of the modulator. The inputs to the reference generator are bias current of $500nA$ and an input voltage of $900mV$ referred as V_{cm} in the figure 4.1. The op amps in the figure 4.1 are all simple differential pairs. The input current of $500nA$ is used to generate the tail current for the op amp OP1. The input voltage of $900mV$ is connected to the positive input of the op amp, and the negative feed back around the op amp OP1 forces the voltage across the $1.8M\Omega$ resistor to be equal to $900mV$. So a current of $500nA$ flows in this resistor as well as in transistor

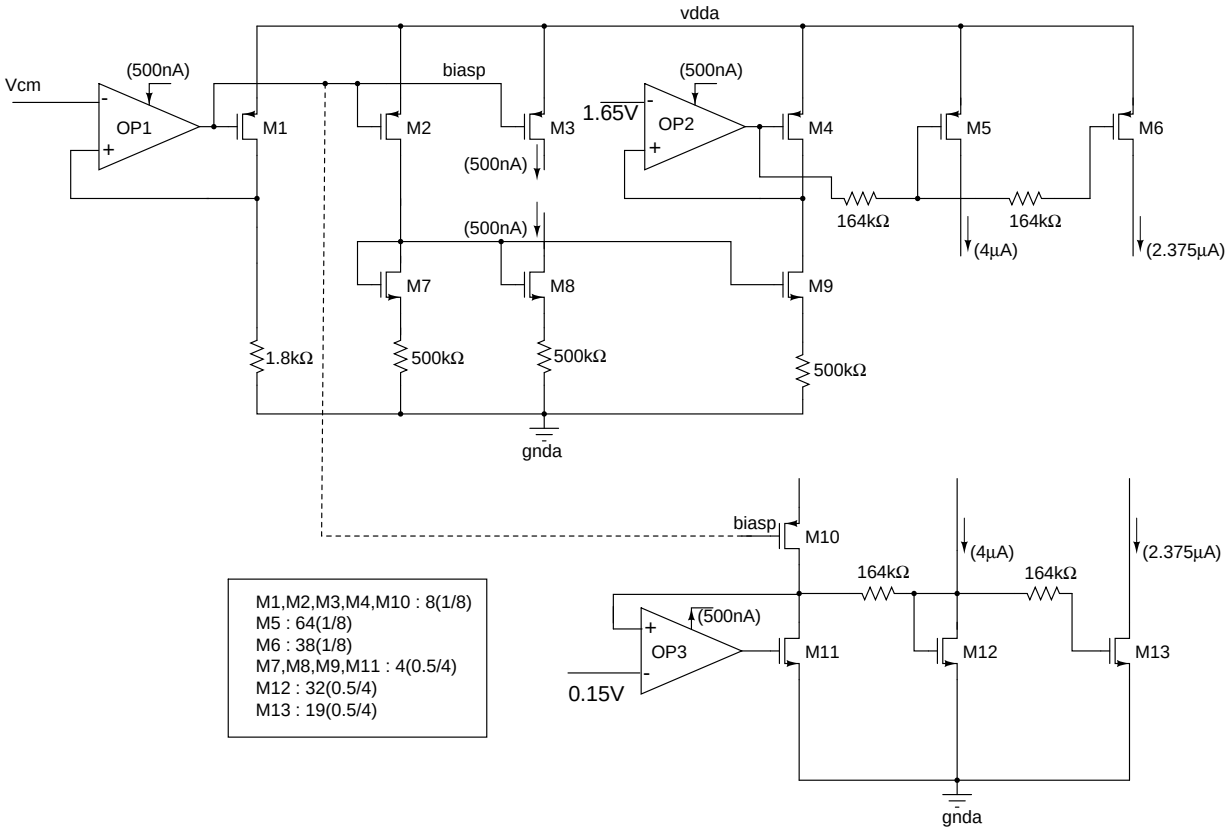


Figure 4.1: Generation of reference currents

M1. The current through M1 is mirrored to M3 via M2 and to M8 via M7. So, M3 is a current source of $500nA$ and M8 is a current sink of $500nA$. The currents through transistors M2 and M7 can be mirrored to generate any number of current sources or current sinks respectively. Also by changing the sizes of the mirrored transistors different current values can be achieved[3].

Two voltages of values $1.65V$ and $0.15V$ are generated using resistor dividers and used as references for op amps OP2 and OP3 respectively. The current through M7 is mirrored to M9 and the same current flows through M4. The drain of M4 is forced to be at $1.65V$ by the negative feed back of the op amp OP2 in order to avoid the changes in the currents through M5 and M6 which should act as current sources with their drains at $1.65V$. So the drain of M4 is maintained at $1.65V$ to avoid channel length modulation effects. The current through M4 is mirrored to M5 and M6 to generate current sources of $4\mu A$ and $2.375\mu A$ which are assistance current sources for feedback DAC reference generator and flash ADC reference generator respectively. Similarly, the negative feed back of op amp OP3 forces the

drain voltage of M11 to $0.15V$. M12 and M13 serve as current sinks of $4\mu A$ and $2.375\mu A$ respectively.

Op amps R2 and R3 are single stage op amps. They require a tail current of $500nA$ which is generated internally. The resistors connected to the gate of M5, M6, M12 and M13 form a low pass filter with the gate source capacitors of the corresponding transistors. This helps in filtering out the noise in the reference generator.

4.2 ADC References

The reference voltages for the flash ADC are generated using the arrangement shown in figure 4.2. The op amp shown in the figure 4.2 is a miller compensated op amp.

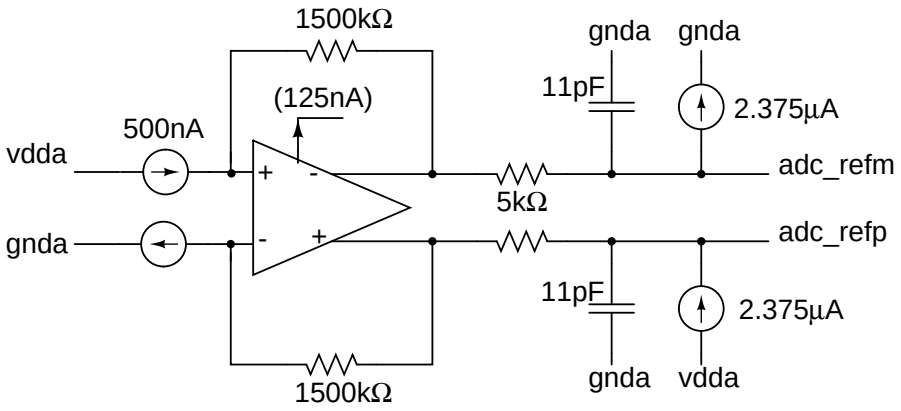


Figure 4.2: Generation of ADC references

The voltage drop across the 1500K resistors is $0.75V$. The CMFB loop of the op amp forces its output voltages to $1.65V$ and $0.15V$. A low pass filter is connected at the output of the op amp to filter out any noise present in the ADC references. Since, the flash ladder requires a current of $2.375\mu A$ the opamp ideally need not supply any current. The currents used in the generation of ADC references are generated by the current generators discussed in the previous section.

The ADC references are noisy due to the periodic switching of the flash comparator. The flash comparator is connected to the resistive ladder for only one

phase of the input clock as explained in chapter 5. Whenever the comparator connects to the ladder it draws a small amount of current from it. The noise generated by the switching of the comparator is noise shaped by the loop filter.

4.3 DAC References

Even though the flash and the DAC require the same references they are generated separately. This is because if the flash references were used for the DAC then any noise in the flash references will appear directly at the output of the DAC. The noise of the feed back DAC is directly added at the input of the modulator. So, the internal DAC should have the same resolution as the overall resolution of the converter. Hence, the references for the ADC and the DAC are generated independently.

The DAC references are generated using the arrangement shown in figure 4.3. The op amp used in the schematic is identical to the first op amp of the loop filter.

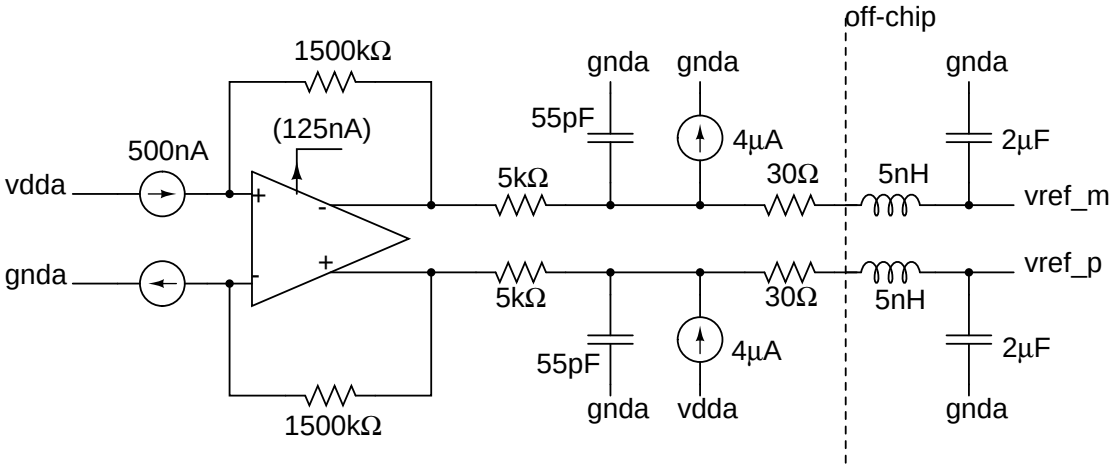


Figure 4.3: Generation of DAC references

The CMFB loop of the op amp forces its output voltages to $1.65V$ and $0.15V$ as the drop across the resistance $1500k\Omega$ is $0.75V$. The output node vref_p sources a current of $7.5I_{LSB}$ to the DAC while the node vref_m sinks the same amount of current, where I_{LSB} is the DAC LSB current. The DAC references need to be precise and should have minimum noise due to the switching of the DAC. This is because this noise is directly added at the input of first integrator op amp and

this noise in the DAC references is not shaped away from the signal band by the loop filter. Hence, an off-chip capacitor of $2\mu F$ is connected to ground from both DAC reference voltages. This forms a low pass filter with the internal $5K$ resistor which has a cut-off frequency of $16Hz$. Thus, any noise in the frequency range of interest, 20Hz - 24kHz, gets filtered out.

The off-chip inductor of $5nH$ is due to the bond pads and the packaging interconnects. At high frequencies this inductor forms a LC circuit with the internal $55pF$ capacitor because of which the reference generator begins to oscillate. To reduce the Q of the resulting tank circuit a 30Ω resistor is connected in series with the off-chip capacitor.

The op amp OP2 in the reference current generation section is necessary to ensure that the drain voltage of transistor M4 is set to $1.65V$. This is because transistors M5 and M6 which source currents to the DAC and ADC respectively have their drains held at $1.65V$ by the output CMFB loop of the op amp. The matching of the drain voltages is necessary to ensure exact mirroring of currents. Similarly op amp OP3 ensures that the drain voltage of M11 is equal to the drain voltage of M12 and M13 which sink currents from the DAC and ADC respectively. Without op amps OP2 and OP3 there will be large errors in the currents sourced and sinked to the ADC and the DAC.

The op amp OP2 is necessary in the reference current generation circuit to set the drain voltage of transistor M4 to $1.65V$. This is because the transistors M5 and M6 source currents to feed back DAC and ADC respectively and their drains are at $1.65V$ set up by the CMFB circuit of the op amp. The currents through these transistors are attained by mirroring via M4. To ensure the exact mirroring of the currents the drain voltage of M4 should match with that of M5 and M6. The same argument holds for the current sinks M12 and M13 which sink currents from feed back DAC and ADC respectively. The current is mirrored via M11 and op amp OP3 ensures the drain voltage of M11 equal to that of M12 and M13 i.e. $0.15V$. Without these op amps there will be large errors in the currents sourced to and sinked from DAC and ADC.

4.4 Op Amp Bias Currents

The op amps in the loop filter and the op amps used to generate DAC and ADC references needs a tail current of $125nA$. This currents are generated using the circuit shown in the figure 4.4.

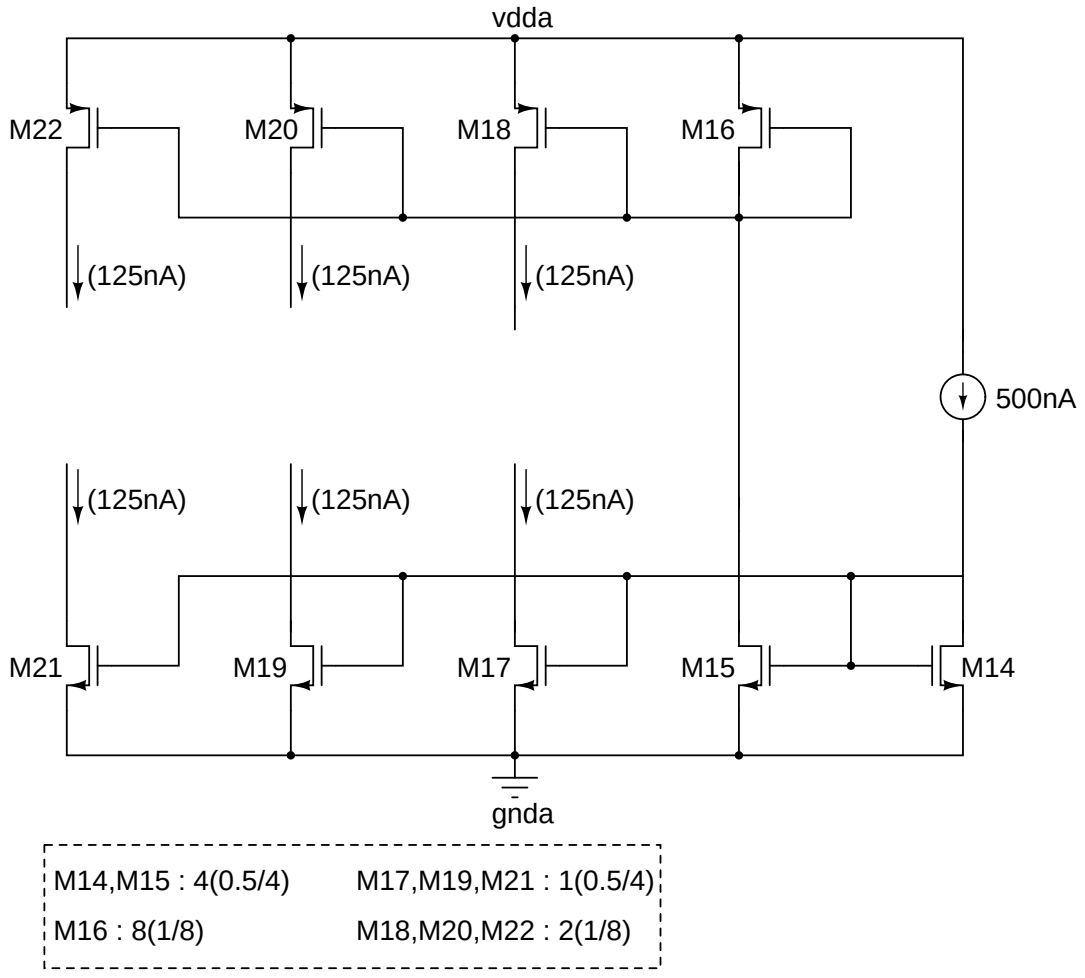


Figure 4.4: Generation of op amp bias currents

Transistors M18, M20 and M22 provide the bias current to op amps I2, I3 and I4 of the loop filter, M17 supplies the tail current to op amp I1 of the loop filter and M19 and M21 provide the reference current to the op amps used in the generation of ADC and DAC references.

4.5 Startup circuit for reference generation module

The reference generation circuit requires a voltage reference of $0.9V$ and a bias current of $500nA$ for the op amp OP1. The voltage can be generated from a simple potential divider setup. A simple and power efficient way of generating the bias current has been implemented by utilising the reference generation circuit as shown in figure 4.5.

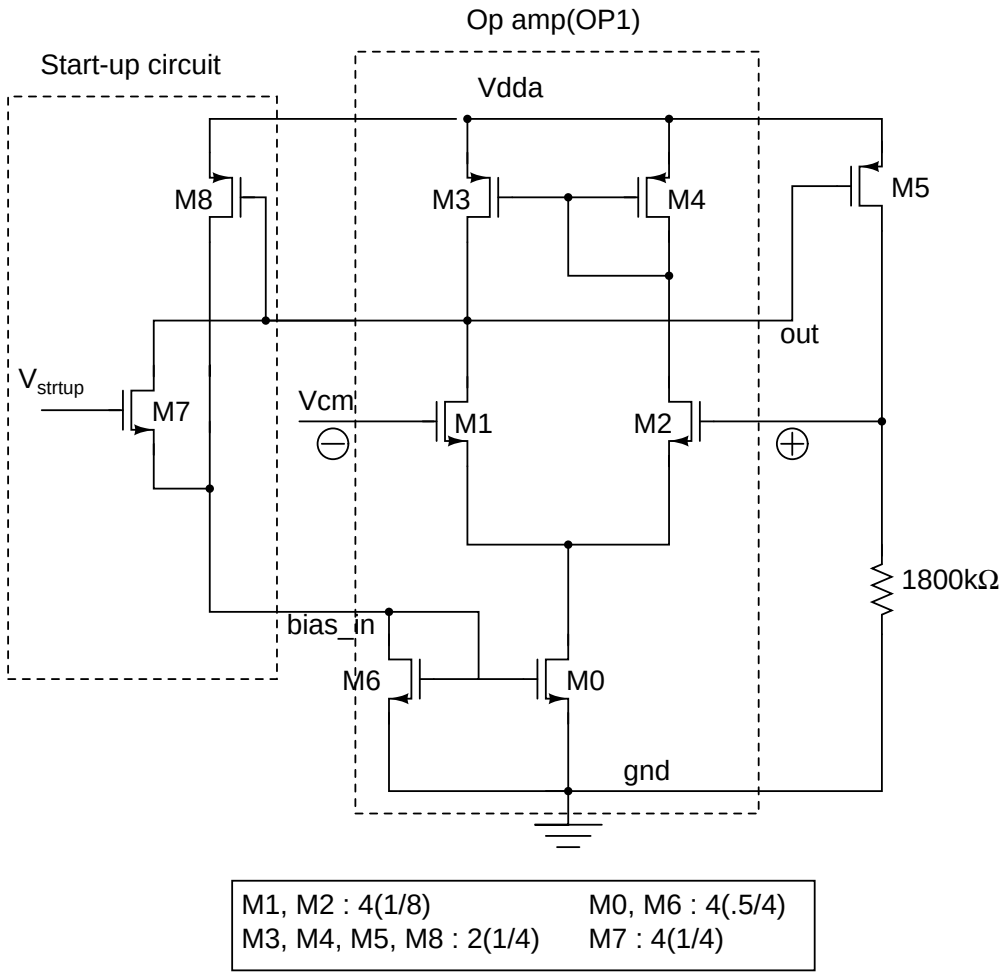


Figure 4.5: Start-up circuit for Reference generation module

Figure 4.5 shows the start up circuit and internal circuit of op amp OP1. The transistors M7 and M8 form the required start up circuit.

4.5.1 Working of start up circuit

The base of transistor M7 is connected to a constant DC voltage of $0.35V$ generated from a simple potential divider. The purpose of this transistor is to discharge the base voltage of transistor M8 if the initial voltage of the base is high. When the base of transistor M8 is lower than power supply voltage then this transistor allows current to flow through and the drain of the transistor M6 will rise as there is current flowing into the node and hence the current starts flowing in M6. The tail current of differential pair of op amp OP1 is mirrored from transistor M6 and so the tail current follows the current in M6 and the op amp OP1 starts working. The virtual short circuit of op amp inputs causes current of $500nA$ in transistor M5 and so in M8 as the current in M8 is mirrored from M5. Transistor M6 is in series with M8 and so the same current flows in M6 which is the required bias current current for the op amp. When there is a current of $500nA$ in transistor M6, the drain voltage rises to approximately $0.42V$ and so transistor M7 turns off as its gate voltage is $0.35V$ which is less than source voltage.

When the initial base voltage of transistor M8 is at ground then it starts dumping large current into op amp OP1 but when the op amp starts working the virtual short of op amp causes a current of $500nA$ in M5 and so the same current in M8 due to the mirroring and base voltages adjust according to the currents.

This circuit has been tested in different process corners and with different temperatures. This circuits takes no extra current but gives required bias current. The drawback of this circuit is that it will take few milliseconds to generate required bias and this time is maximum when the initial voltage of the base of transistor M8 is high. The transient bias currents have been plotted for different initial conditions and are shown in figure 4.6

In figure 4.6 Vgp indicates the starting voltage at the gate of transistor M8. These plots are by using typical corner of the library models for both NMOS and PMOS transistors. The worst case settling time is $2.4ms$ and is when slow-slow corner of library models is used for transistors.

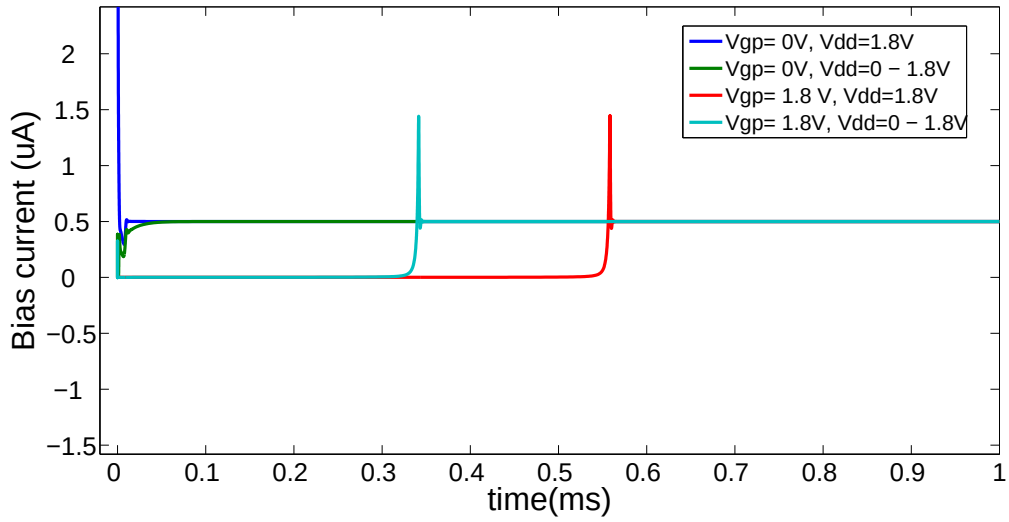


Figure 4.6: Transients of bias current for different initial conditions

CHAPTER 5

Simulation Results and Conclusions

5.1 Layout

The designed 3rd order modulator has been laid out in cadence. The top level layout is shown in figure 5.1. It occupies an area of $0.6mm^2$ without including bias capacitors.

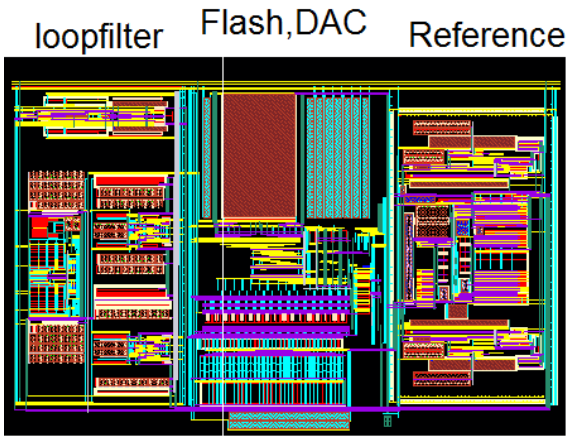


Figure 5.1: Layout of the modulator

5.2 Simulation Results

The CT delta-sigma modulator takes a lot of time for simulations when all the blocks are implemented with transistors. to reduce the duration of the simulations some blocks are realized with ideal models. Verilog-A realization is used for

flash,DEM and DAC and ideal models are used for reference,op amps and clocks had associated with ideal active models.

The results of the various simulations run on the design are tabulated below. The input signal to the modulator is a $2.4V_{pp,diff}$ sinusoid at a frequency of $5.25kHz$. 8192 point fft of the output of the modulator is taken and tabulated.

Loop Filter	Flash ADC	Clk generator	DAC	reference	SNDR	HD2	HD3
Ideal	VerilogA	Ideal	VerilogA	ideal	109	130	132
Schematic	VerilogA	ideal	Schematic	Schematic	108	130	121
Schematic	VerilogA	ideal	Extracted	ideal	109	131	120
Extracted	VerilogA	ideal	Schematic	Schematic	108	124	117
Ideal	Schematic	Schematic	Schematic	ideal	107.6	128	112
Schematic	VerilogA	ideal	Schematic	Extracted	109	127	121
extract	extract	Schematic	extract	ideal	105	123	115

Table 5.1: Simulation Results

The SNR in each of the above simulation setups was found to be in excess of 100 dB. Since every 6dB increases the resolution of the data converter by 1 bit, 91.8dB SNR corresponds to effective number of bits of 15 bits. The designed ADC hence, has a resolution of 15-bits. The output PSD of the modulator when extracted view of loop filter and feedback DAC is used, schematic of reference and ideal view for flash, is used is shown in figure 5.2.

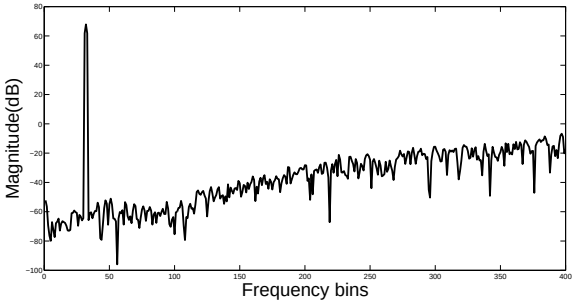


Figure 5.2: PSD of modulator output

The power consumption statistics of the designed modulator is presented below. The current design burns about $16\mu A$ lesser current. The power saved is about $28\mu W$. This is mostly from the loop filter and reference generation circuit. The power consumed by the digital circuitry is reduced by a factor two because

of the reduction of oversampling ratio from 64 to 32. . The percentage saving of power is 23%.

Block	Dhwani	Current Design
Flash, DEM	$6\mu A$	$6\mu A$
Ref.Gen.circuitry	$22\mu A$	$18\mu A$
Clocks	$11\mu A$	$5.5\mu A$
Loop Filter	$28\mu A$	$21\mu A$
Total current	$67\mu A$	$50.5\mu A$
Power Consumption	$120.6\mu W$	$91\mu W$

Table 5.2: Comparison of ADC power consumption

The achieved specifications of the ADC are tabulated below:

Feature	Achieved Specification
Resolution	15-bits
SNDR	103 dB
Sampling rate	$1.536MHz$
Signal bandwidth	$24kHz$
Power Consumption	$91\mu W$

Table 5.3: Achieved ADC specifications

5.3 Conclusions

A 3rd order, zero optimized CT $\Delta\Sigma$ modulator has been designed for audio band applications. It operates at OSR of 32 and achieves a resolution of 15 bits. Feed forward compensation technique is used for the op amps in loop filter to reduce the power consumption. The flash ADC of design Dwani[**?**] has been used which consumes almost zero static power. Resistive DAC with switches on virtual ground side has been used. It is provided with switch to activate or deactivate the DEM module. The layout of the design is done and tested with different modules extracted and performance was measured.

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[2] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time delta-sigma adc for audio applications," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 2, pp. 351 –360, feb. 2008.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. TATA McGraw-Hill Publishing Company Limited, 2002.