Optimization of Power Consumption of a 15 bit Audio Continuous Time Delta-Sigma Modulator

A Project Report

submitted by

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CERTIFICATE

This is to certify that the thesis titled **Optimization of Power Consumption of a 15 bit Audio Continuous Time Delta-Sigma Modulator**, submitted by **Sreelakshmi Penmetsa**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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The credit of me doing this work goes to my father. He taught me all the important courses in electronics and communications throughout my undergraduation. It is on his shoulders I stand today. I dedicate this thesis to my family - parents, brother and tawny, our dog. Their love had cushioned and supported me throughout my education.

ABSTRACT

The project involves power optimization of a continuous-time delta-sigma modulator for analog-to-digital conversion. The design that is power optimized is a 3rd order system with OSR=64. It uses a four bit quantizer, operates in 0-24 kHz range and consumes a power of 121μW. It achieves 15 bit resolution. In the current design, the OSR is lowered to 32 to cut down the power consumed by the digital circuitry by a factor 2. The opamps in the loop filter are replaced by feedforward compensated opamps as they are more power efficient. The current design consumes a power of 90μW. The handcrafted DEM block has been replaced by HDL coded DEM block. Calibraion technique to minimize errors due to DAC elements mismatch has also been implemented. There is a provision to deactivate DEM block and activate calibration block and vice-versa. Appropriate design techniques are used to make the design robust with respect to process and temperature variations. The design is implemented in 0.18μm CMOS process from UMC with a supply votlage of 1.8V.

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ABBREVIATIONS

ADC	Analog to Digital Converter
CIFF	Cascaded Integrators with distributed feedback
CIFF	Cascaded Integrators with distributed feedforward
CMFB	Common Mode Feed-Back
CT	Continuous Time
DT	Discrete Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DSM	Delta Sigma Modulator
DWA	Data Weighted Averaging
GBW	Gain Bandwidth
LSB	Least Significant Bit
MSA	Maximum Stable Amplitude
MSB	Most Significant Bit
NTF	Noise Transfer Function
OBG	Out of Band Gain
PSD	Power Spectral Density
RNS	Residual Number System
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System on Chip
STF	Signal Transfer Function
$V_{pp,diff}$	Peak to Peak Differential Voltage

CHAPTER 1

Introduction

1.1 Motivation

The main motive is to optimize power consumption of an earlier design named Dhwani [1]. It is a continuous time $\Delta\Sigma$ modulator designed for audio applications with 90dB dynamic range. It is a third order modulator with OSR=64. It consumes a power of $121\mu W$. The decimation filter at the output of the modulator consumes a power of $100\mu W$. The current design is targetted for a four fold power optimization. This could be acheived by lowering the OSR to 32 which cuts down the power consumed by the digital circuitry. The OSR can be lowered because the earlier design over-acheived the required the SQNR. For a 90dB dynammic range, it is sufficient if the SQNR is around 102dB and the SQNR of Dhwani is 120dB. By using power efficient design of opamps in the loopfilter, the power consumed by the analog circuitry can be brought down.

DEM block in Dhwani is handcrafted. Handcrafting the DEM block consumes a lot of time and effort of the designer. Hence it can be coded using a hardware description language and synthesized. An alternative to DEM approach is using calibraion techniques. One advantage of calibration over DEM is that it can be done outside the loop and hence loop delay can be avoided which deteriorates the performance of the modulator. On the other hand, typically a calibration technique needs reconfiguring the modulator. This consumes an additional area on the chip and calls for more effort and time of the designer. The technique presented in [3] does not need a reconfiguration of the modulator and hence is efficient. This technique is implemented using Verilog HDL and synthesized.

1.2 Organization

Chapter 2 explains the design of the loop filter.

Chapter 3 explains the design of the operational amplifiers used in the loop filter.

Chapter 4 gives the design of the internal DAC used in the circuit.

Chapter 5 gives the design of the dynamic element matching block

Chapter 6 explains the design and implementation of the calibration technique.

Chapter 7 concludes the thesis with the simulation results.

CHAPTER 2

Loop Filter

Loop filter is the heart of a $\Delta\Sigma$ modulator. The quantization noise is shaped out of the signal band by virtue of its high gain in the signal band. This chapter discusses the design of a third order loop filter with zeros optimized for a multibit $\Delta\Sigma$ modulator.

2.1 Selection and Implementation of Loop Filter Transfer Function

The first step in the design of a $\Delta\Sigma$ modulator is the choice of the modulator order and its noise transfer function(NTF) [1]. A third order modulator with an OSR of 32, 4-bit internal quantizer and zeros optimized gives a signal-to-quantization noise ratio of around 109 dB. The NTF of the modulator has an out-of-band gain (OBG) of 3. OBG is defined as the gain of the NTF at frequencies close to $\omega = \pi$. The NTF zeros are optimised to achieve an inverse Chebyshev characteristic, thus introducing a higher SNR.

The following steps were followed to find the transfer function of the CT loop filter:

1. Using the Sigma-Delta toolbox in MATLAB the NTF of a 3rd order DT $\Delta\Sigma$ modulator with an OBG of 3 is determined.

$$NTF(z) = \frac{(z-1)(z^2 - 1.994z + 1)}{(z - 0.3556)(z^2 - 0.6603z + 0.304)} \tag{2.1}$$

2. The DT loop filter transfer function L(z) is given by:

$$L(z) = \frac{1}{NTF(z)} - 1 \tag{2.2}$$

3. The impulse invariance transformation is used to determine the transfer function L(s) of the equivalent CT modulator. The normalized sampling interval is 1 s.

$$L(s) = \frac{1.367s^2 + 1.087s + 0.415}{s^3 + 0.005783s} \tag{2.3}$$

The above equation for L(s) can implemented by a cascade of three integrators with 2^{nd} and 3^{rd} integrators connected to form a resonator and a summer. Figure 2.1 shows the block diagram for the implementation of L(s).

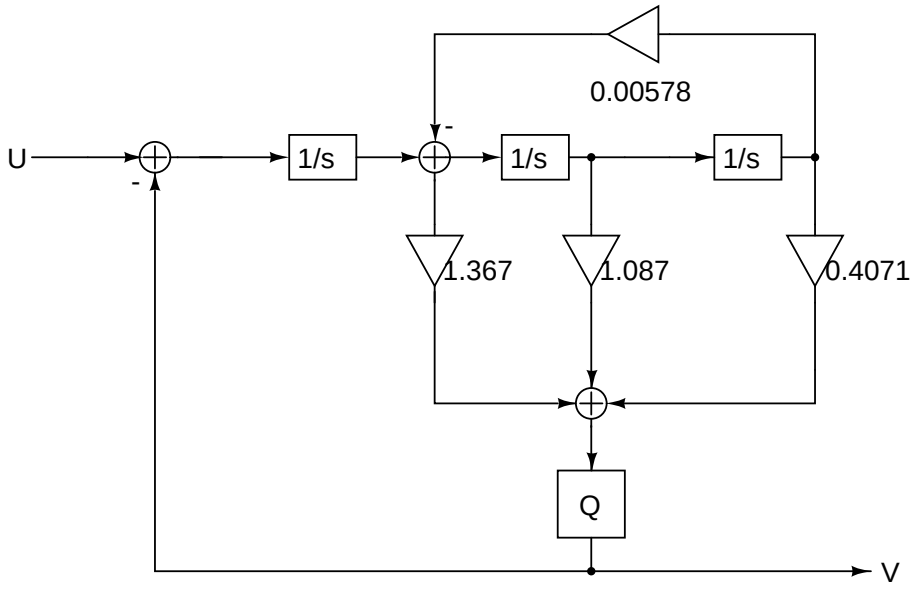


Figure 2.1: Block diagram of 3rd order CT loop filter for $T_s = 1s$

It is now necessary to perform dynamic-range scaling. Dynamic scaling is necessary to ensure that all nodes have approximately the same power level. After dynamic scaling all nodes have the same maximum output level. Dynamic scaling is done as follows: The maximum output level of each integrator is determined by MATLAB simulation. The maximum outputs of all integrators are set to the same level by adjusting their gains. To increase the output level at a node by a factor of

k, the input branches should be multiplied by k while the output branches should be divided by k.

The CT model shown in figure 2.1 needs to be frequency scaled to the frequency of operation of the modulator i.e $f_s = 1.536MHz$. The loop filter obtained after frequency scaling and node scaling is shown in figure 2.2. The 1^{st} integrator input resistance is kept at $200K\Omega$ to constraint the in band noise so that in band SNR due to total input referred noise is 93 dB.

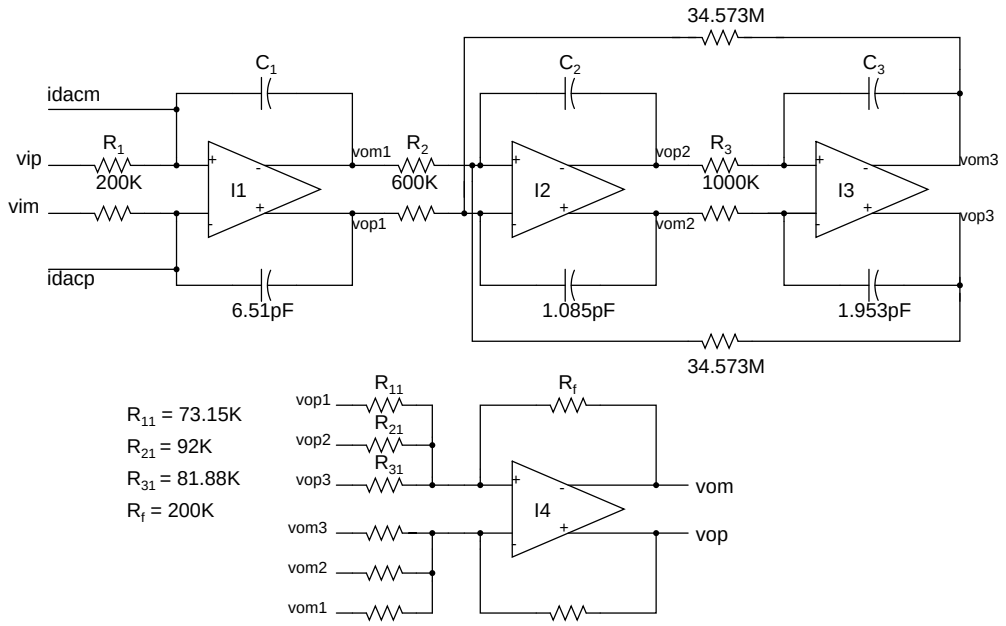


Figure 2.2: Loop filter with ideal op amps for $f_s = 1.536MHz$

2.1.1 Reduction of NTF zero optimization resistance

It is observed from figure 2.2 that R_{31} is excessively large for an on chip resistance ($34.573M\Omega$). Here, we are generating a current $\frac{v_{op3}}{R_{31}}$ from a large swinging node v_{op3}. If the node voltage is scaled by means of a potential divider and we take the voltage from the low swing node, R_{31} can be reduced. The Thëvenin equivalent of the

R_{31} is now $0.34573M\Omega$. From the resistive divider we get $0.0099M\Omega$. So externally, $0.33583M\Omega$ should be connected. Final structure is shown in figure 2.4. The T network in practice, can be realized using the resistors used for sensing the Common mode voltage of the 2nd stage of the 3rd op-amp.

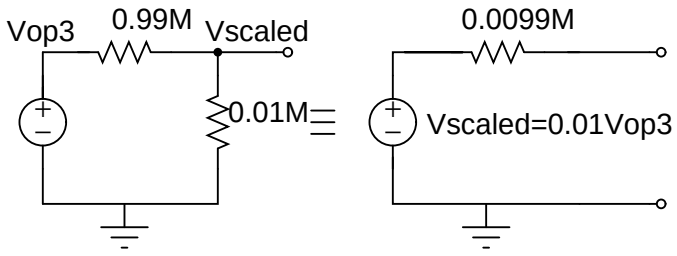


Figure 2.3: Thëvenin equivalent of the resistive divider circuit

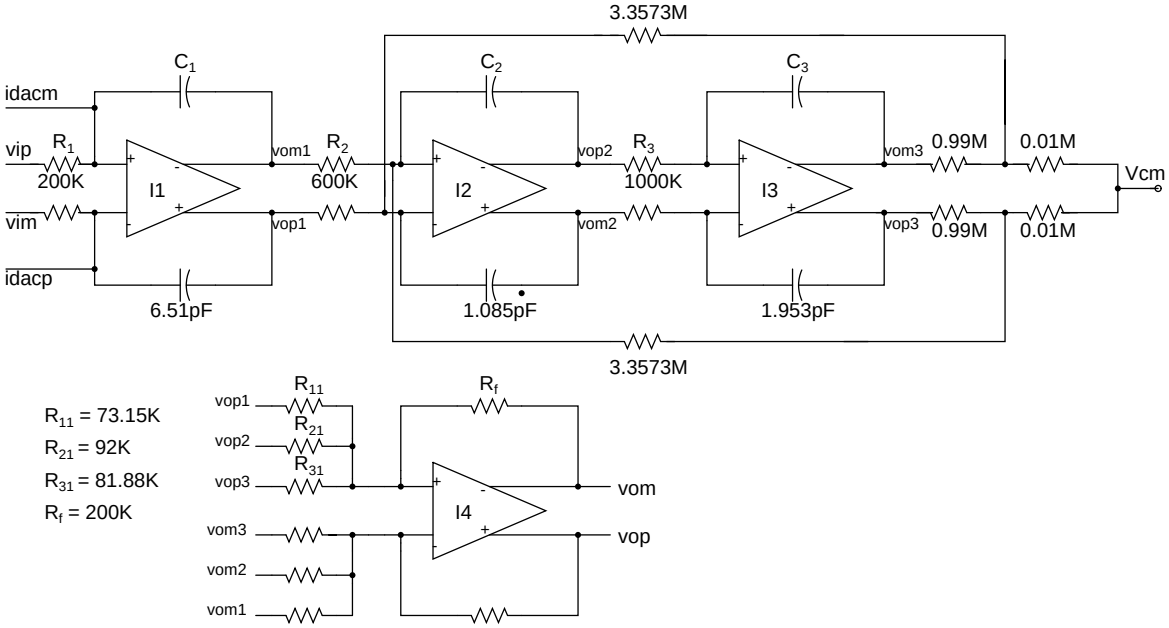


Figure 2.4: Loop filter with ideal op amps and scaled NTF zero optimization resistance

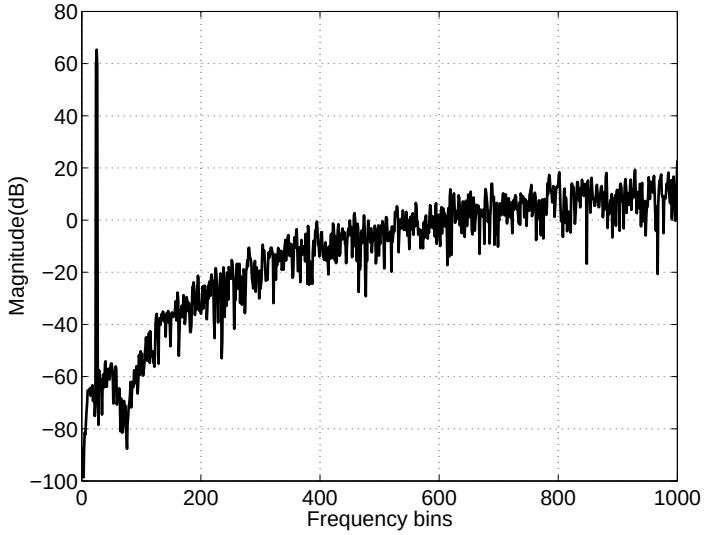


Figure 2.5: PSD of the modulator output

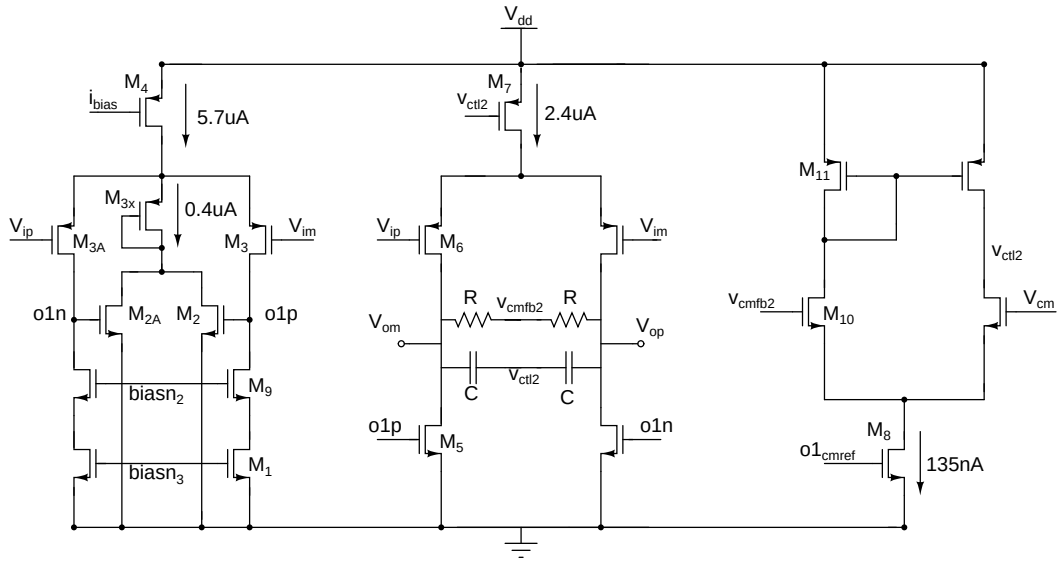
The loopfilter shown in the fig 2.4 is realized using ideal opamps and a sigma delta modulator schematic is built. 4-bit flash converter and resistive DAC are realized using VerilogA codes. Fig 2.5 shows the frequency spectrum of the output of the modulator. The notch in the audio band can be observed in the plot. The SQNR is computed and it matches with the ideal SQNR obtained from the initial MATLAB simulations (109 dB).

CHAPTER 3

OP-AMPs Used in Loop Filter

3.1 First Integrator Op Amp

The first integrating op amp determines the overall distortion and noise of the data converter. Noise and non-linearities of the succeeding op amps becomes insignificant when referred back to the input. Hence the design of first opamp is critical. It is implemented using a feedforward topology because it is more power efficient than Miller compensation. Figure 3.1 shows the schematic of the first op amp.



M_1-40(3/12)	M_4-84(1/1)	M_8-2(0.5/2)	C = 200fF
M_2-4(0.5/2)	M_5-24(0.5/2)	M_9-12(1/1)	R = 1M
M_3-24(2/2)	M_6-10(0.5/0.2)	M_{10}-24(0.5/2)	
M_{3X}-8(1/1)	M_7-80(1/1)	M_{11}-2(0.5/0.4)	

Figure 3.1: First Integrator Op Amp

While choosing the op amp input stage, noise is the major consideration. We have chosen P-channel transistors for the input stage, as it has low Flicker noise when compared to N-channel transistor which is a major source of transistor noise

at low frequencies. It therefore minimizes the overall input referred noise of the loop filter.

Feed forward compensation is implemented in the second stage. The second stage of the op amp is a class A amplifier. A feedforward stage is added by current reuse method. This adds a left half plane zero near the second pole of the op-amp which makes the system look like a first order system at the unity gain frequency .i.e, the magnitude response rolls off at 20dB/decade at the unity gain frequency. This type of topology, wherein the load PMOS pair is used for frequency compensation is optimal in terms of power consumption. However, this architecture limits the output swing of the op-amp. In the current application of using this op-amp in the loop filter, this problem could be alliviated by appropriate node scaling to ensure that the output swings are within the swing limits of the op-amp.

3.2 Comparision

The following table compares the various performance parameters of the first opamp in the current design with that of Dhwani's.

Parameter	Current design	Dhwani
Gain	82 dB	84.82 dB
Unity Gain Frequency	33.7 MHz	27.73 MHz
Phase Margin (degrees)	30	42
First Stage Current(micro amps)	5.3	5.3
First Stage CMFB Current(micro amps)	0.4	1.4
Second Stage Current(micro amps)	2.4	6.5
Second Stage CMFB Current(micro amps)	0.135	0.55

Table 3.1: First integrating opamp - current design Vs Dhwani[1]

3.3 Optimization of Power

A noise analysis is run on first op-amp used in the design [1] and it is observed that most of the noise in the first stage of the op-amp is due to the flicker noise and thermal noise of the transistor pair M1 (figure 3.1) as shown in the following table. The total input referred noise voltage at 300k temperature is 19.16uV.

Component	noise type	percentage contribution
M1 pair	flicker noise	15.74
M1 pair	thermal noise	9.45
Resistors	thermal noise	6.88
M3 pair	flicker noise	6.76
M3 pair	thermal noise	4.1

Table 3.2: First integrating op amp noise of Dhwani[1]

To lower the flicker noise, the dimensions of transistor pair M1 are scaled and to lower the thermal noise the input transistor pair is pushed into subthreshold region. Transconductance is maximum in this region. So, the overall noise comes down. This gives a room to increase the resistance and yet have the same overall input referred noise of the loop filter. The resistance has been increased from 100kΩ to 200kΩ. This gives a two fold advantage. Firstly, the second stage current comes down and secondly the DAC ref current comes down by a factor two. The following table gives the noise distribution of the first integrating opamp used in the design. The total input referred noise voltage at 300k temperature is 19.99uV.

Component	noise type	percentage contribution
Resistors	thermal noise	19.61
M1 pair	thermal noise	5.81
M3 pair	thermal noise	2.66
M1 pair	flicker noise	0.68
M3 pair	flicker noise	0.48

Table 3.3: First integrating op amp noise in the current design

The frequency response of fully differential output is shown in figure 3.2.

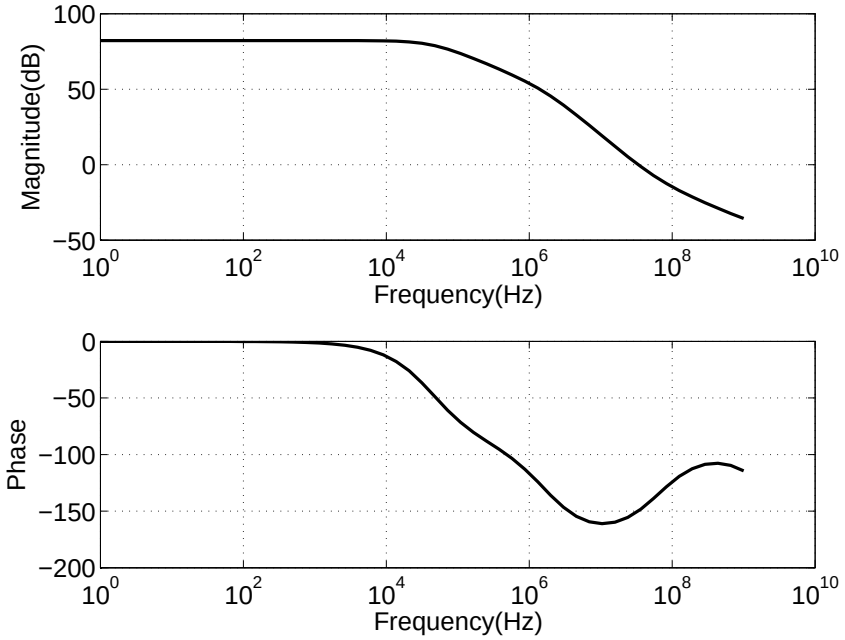


Figure 3.2: 1st integrator op amp frequency response

3.3.1 Common-Mode feedback circuits

In op-amp topologies that are fully differential, we need circuits that set the common-mode voltages at the output of both the stages. This is because, in each stage, to attain high differential voltage gain, the load resistors are replaced by PMOS current sources which results in a circuit with NMOS as input pair and PMOS as load pair. They are two current sources connected to a node and hence the node voltage cannot be predicted. This circuitry is called *common-mode feedback (CMFB) circuitry.*

First stage CMFB circuitry

1st stage CMFB circuitry employs a current mode feedback to set the first stage output common mode voltage. The total bias current through M4 is constant(as set by i_{bias}). If output common mode voltage of 1st stage increases, current through M2 and M2A increases which in turn results in the reduction of current through M3 and M3A. when the current throught M3 pair reduces from the expected level, the current flowing into the output node is lower that the current that is being sucked from the output node. Therefore, the output common

mode voltage falls and settles to the desired voltage for which CMFB circuitry was designed.

Second Stage CMFB circuitry

The second stage CMFB circuit is a simple single ended differential amplifier. It employs sensing using resistors. Resistor value is chosen such that it does not load the op-amp in differential picture. The common mode voltage is detected using the resistors and is compared with the desired common mode voltage, V_{cm}. The diffencial amplifier's output controls the bias current of the second stage such that the output common mode voltage settles to V_{cm}. For eg, if the output common mode voltage exceeds V_{cm}, the diffencial amplifier output increases. This decreases the bias current of the second stage. Now, the current that is pumped into the output node is less than that being sucked out. Therefore the output voltage increases and comes back to V_{cm}. Op-amp stage and CMFB circuit together make another loop with two significant poles. So again this loop has to be freqency compensated and hence the capacitors.

The CMFB circuit's step response is shown in figure 3.6.

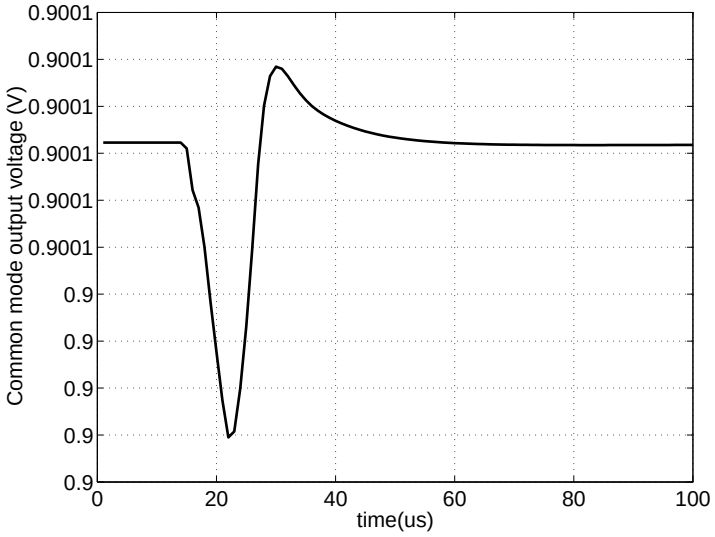


Figure 3.3: Common mode feedback response of 1st integrator op amp

3.4 Second Integrator Op Amp

The specifications of the second stage op-amp are not so stringent because it's input referred noise and distortion will come down to a large extent by virtue of the high gain of the stage preceeding it, first op-amp.

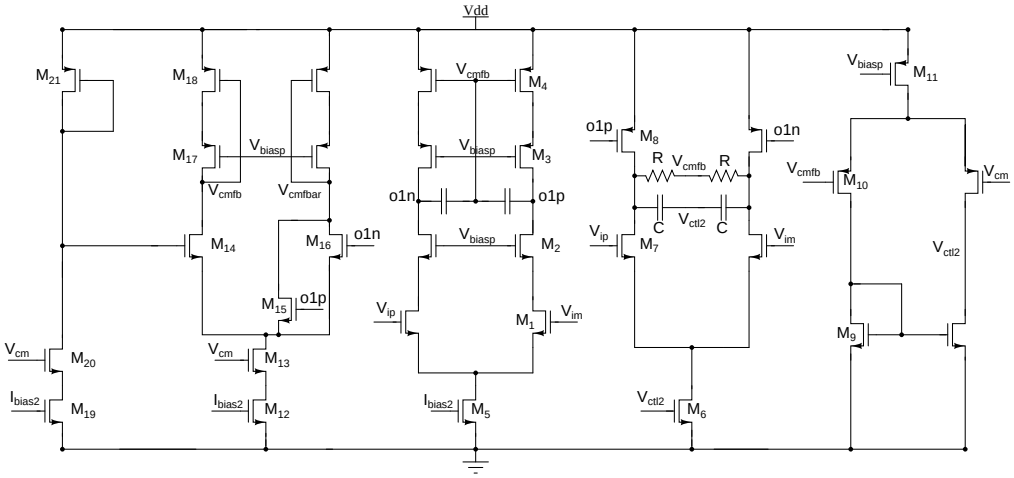


Figure 3.4: Second Integrator Op Amp

Transistor	Size	Transistor	Size
M1, M2, M7	1(0.6/0.25)	M21	16(0.5/0.5)
M3	1(0.5/0.25)	M15, M16	(0.25/4)
M4, M17, M18	2(0.5/0.25)	M14	2(0.25/4)
M5, M12, M19	2(0.5/2)	M13, M20	2(0.6/0.25)
M6	3(0.5/2)	M11	1(0.5/10)
M8	8(0.5/0.5)	M10	6(0.5/0.2)
M9	1(0.5/2)		

Table 3.4: Second integrating opamp transistor sizing

This op-amp also employs feedforward topology. Since the requirements on this op-amp are not stringent, n-channel transistors can be used as input pair. The first stage is a simple differential pair. Second stage is a class A amplifier and feedforward compensation using current reusing technique. The CMFB circuit of the first stage is essentially a differencial pair which senses the common mode voltage and compares with the diode connected PMOS whose current density is same as the second stage input pair PMOS. It sends a correction voltage to the top PMOS pair of the first stage in a way that makes the common mode voltage

nearly equal to the gate voltage of the diode connected PMOS. The second stage employs a resistive sensing CMFB whose operation is same as that of the first op-amp. The frequency response of fully differential output is shown in figure 3.5.

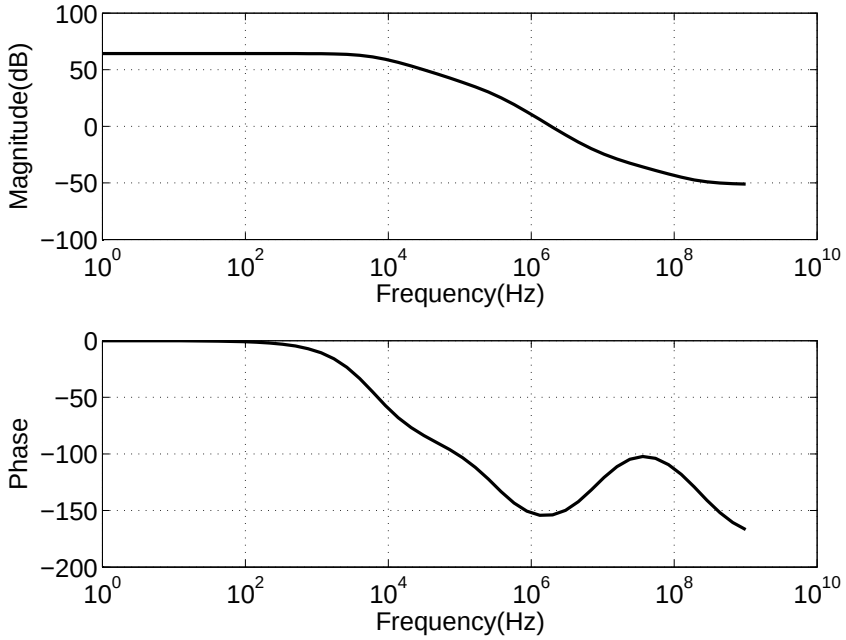


Figure 3.5: Second and third integrator op amp frequency response

The CMFB circuit's step response is shown in figure 3.6.

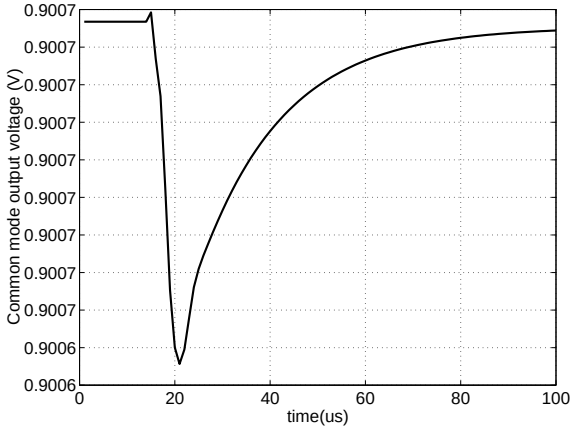


Figure 3.6: Common mode feedback response of 2nd and 3rd integrator op amp

3.5 Comparision

The following table compares the various performance parameters of the second opamp in the current design with that of Dhwani's.

Parameter	Current design	Dhwani
Gain	60 dB	80 dB
Unity Gain Frequency	2 MHz	13 MHz
Phase Margin (degrees)	26	3
First Stage Current(micro amps)	0.135	0.824
First Stage CMFB Current(micro amps)	0.135	0.135
Second Stage Current(micro amps)	0.135	1
Second Stage CMFB Current(micro amps)	0.038	0.43

Table 3.5: Second integrating opamp - current design Vs Dhawani[1]

The third integrator uses the same op-amp as that in second integrator except that, the CMFB resistors are connected to form a series combination of 900k and 100k as discussed in chapter 3. The summer op-amp should have a large swing. Since feedforward compensation in current reuse topology cannot give large swings, it cannot be used. A miller compensated opamp that can swing from 0.15V to 1.65V is used.

CHAPTER 4

Feedback DAC

4.1 Introduction

Sigma delta modulator needs a Digital to Analog Converter (DAC) in the feedback loop to convert digital or binary data to its equivalent analog quantity. This quantity is subtracted from the input to the sigma delta modulator and fed to the loop filter. In noise shaping modulators, quantization noise comes down by 6dB for every additional bit in the quantizer. The maximum stable ampliude (MSA) also improves with increase in number of bits in the quantizer. On the other hand a multibit quantizer introduces non-linearity due to mismatchs in the DAC elements. It should be noted that any non-linearily in the DAC will be directly reflected at the output. Since a four bit flash A/D converter is used in the forward path of the modulator, a four bit DAC has to be embedded in the feedback loop. This chapter discusses the design of the four bit resistive DAC used in $\Delta\Sigma$ modulator.

4.2 Internal DAC topology

The most common architecture for the internal N-bit DAC employs $2^N - 1$ parallel unit elements. In such a DAC, the kth output level is generated by turning on k equal valued elements and summing up their currents.

A resistive DAC has been implemented in the design. One way of implementing resistive DAC is shown in the figure 4.1. The switches that connect V_{refp} to the resistors are realized using P channel transistors and the switches that are used to connect V_{refm} to the resistors are realized using N channel transistor. Both P channel transistors and N channel transistors are of minimum size.

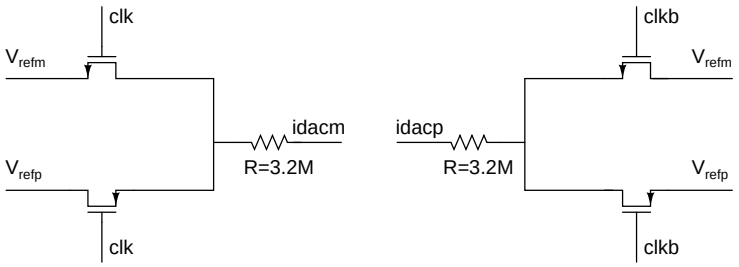


Figure 4.1: Internal DAC schematic

Another way of implementing the DAC is to move the switches to the virtual node side as shown in the figure 4.2. By moving the switches to virtual ground node side the voltages that the switch has to conduct are around 900mV, unlike the earlier case wherein, the switches had to conduct voltages at two extremes - 1.65V and 0.15V. Now, all the four switches can be realized either using N channel or P channel transistors. In the current design all the four switches are realized using minimum size N channel transistors.

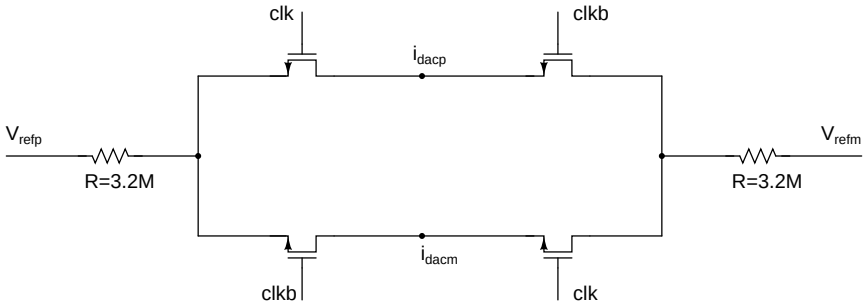


Figure 4.2: DAC schematic with switches at the virtual ground node side.

It could be expected that when the switches are moved to the virtual ground node side, the SNR approaches the ideal value. The reason being - when two types of switches (P channel and N channel) are used, the rate of charging(or discharging) are no longer identical. This results in distortion and hence deterioration of SNR. Both the architectures are tested in the setup of the current design. The SNR obtained is around 109dB which is the ideal value. Thus, it can be concluded that there is no advantage in moving the switches to the virtual ground node side.

In the design of DAC, in order to implement calibration of DAC feature, there is a provision to deactivate every individual DAC cell by means of a switch as shown in the fig 4.3. These switches are realized using N channel transistors.

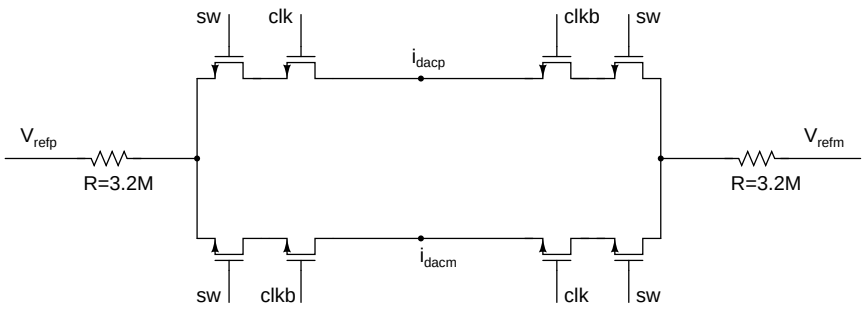


Figure 4.3: DAC schematic with provision for deactivating

The DAC resistance is 3.2M as against the DAC resistance of Dhwani design[1](=1.6M). Hence, for this setup, the reference generation circuitry of Dhwani design[1] has to changed such that the DAC current is halved.

CHAPTER 5

Dynamic Element Matching

5.1 Introduction

DAC non-linearities as discussed in chapter 4 directly appear at the output of the modulator. Hence DAC non-linearities have to be minimized. Dynamic Element Matching(DEM) and calibrating the DAC are two approches to minimize the DAC non-linearities. In DEM technique, additional circuitry is added in the loop that can do an intelligent averaging of the DAC element mismatches. This increases the delay in the loop which is undesirable. On the other hand, calibration of DAC can be done outside the loop in digital domain. Both DEM and calibration unit can be coded using a hardware description language, synthesized and integrated with the rest of the circuitry. In the design, there is an option of disabling the DEM and activating calibration unit. This chapter discusses the architectures of DEM. Calibration of DAC is discussed in the next chapter.

5.2 DEM Algorithms

The purpose of DEM is to move the errors due to mismatch away from the signal band. There are several approaches for doing this. Two common techniques are Randomization and Data Weighted Averaging.

1. Randomization - In this technique, for a given input thermometer code, randomly the required number of DAC elements are chosen and turned on. This results in no correlation between the mismatch errors at different instants of time. As a result, when these errors are averaged out by the decimation filter (ideally a brick wall low pass filter) the noise becomes uniformly distributed in the entire frequency range. In other words the noise becomes white.

2. Data Weighted Averaging (DWA) - Data weighted averaging makes use of all the available DAC elements one by one. When the first input thermometer code arrives, the required number of DAC elements are turned on starting from zeroth dac element. For the next thermometer code, the dac units are turned on starting with the next unused element. In Figure 5.1 a four bit thermometer dac is used to demonstrate the algorithm for data weighted averaging. Let the first input code be 0011. First three DAC elements are turned on as shown in the figure 5.1. When the input sequence 0111 is applied the next seven elements are turned on. Finally when 1000 is applied the last five and first three DAC elements are turned on. In this manner the DWA algorithm covers all the DAC elements a very high rate therby summing the DAC errors quickly and moving the distortion to higher frequencies.

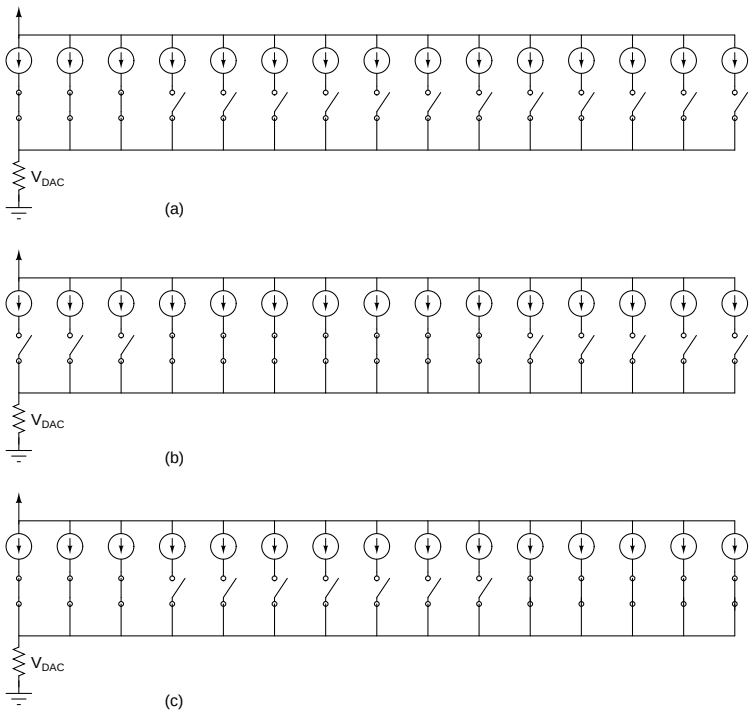


Figure 5.1: DWA element selection for a 4-bit DAC with an input sequence of 0011,0111,1000

5.3 DWA Implementation

Figure 5.2 shows the implementation of DWA algorithm. The following are the basic building blocks that are coded using a HDL.

1. Thermometer to Binary Converter
2. Accumulator
3. Barrel Shifter
4. Latch

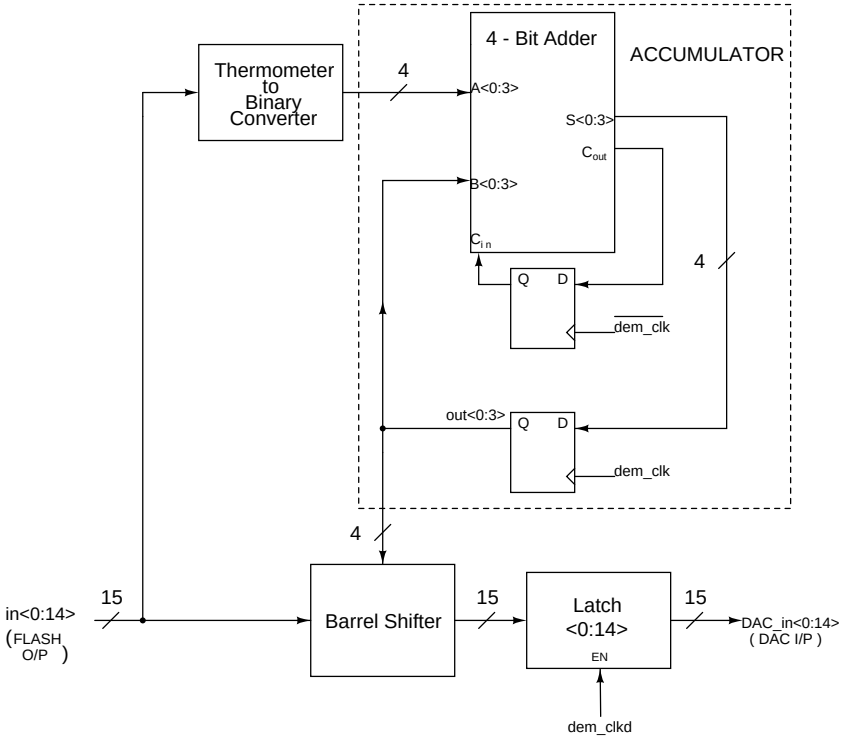


Figure 5.2: Schematic for the DWA implementation

5.3.1 Thermometer to Binary Converter

The output of a flash ADC is a 15-bit thermometer code. A thermometer code can be converted to its binary equivalent by counting the number of ones in it. This can be accomplished by adding all the bits in the thermometer code. The

Verilog code implements this block by instantiating 1-bit full adders, 2-bit adders and 3-bit adders.

5.3.2 Accumulator

The accumulator generates the control signals to the barrel shifter such that the pointer points to the next available unused element.

5.3.3 Barrel Shifter

The input to the barrel shifter is the 15-bit thermometer code generated by the internal flash ADC. The control signals for the barrel shifter are generated by the accumulator. The barrel shifter shifts the incoming thermometer code to the location pointed by the control signals from the accumulator.

5.3.4 Latch

The output of the barrel shifter will contain glitches since each input bit pattern gets delayed differently by the chain of full adders in the accumulator. A latch samples the output of the barrel shifter after it has settled to its final value. The clock to the latch is a delayed version of the clock applied to the accumulator. The outputs of the latches are the control signals that turn ON and OFF the basic cells of the resistive DAC.

CHAPTER 6

Calibration of DAC

6.1 Introduction

The basic concept of a digital correction or calibration is illustrated in fig 6.1. The correction block is simply a RAM that contains the corrected values of all the possible output codes of the modulator [2]. For correct operation, the data stored in the RAM should be simply the accurate digital equivalent of actual output levels of N-bit DAC. To see this, assume that the RAM does contain these values and the quantizer resolution is 3 bits. Let the code that appears at the output of the modulator, v(n), be 110. As a result, a dc analog quantity proportional to (6/8)Vref is fed by the DAC. However, in reality slightly different value is fed back due to the inevitable imperfections of the DAC circuit. Simultaneously, an M-bit digital word w(n) that is a very accurate representation of this (imprecise) DAC output analog quantity is retrieved from the RAM and fed to the decimation filter. Thus, for the case of a 10-bit accurate DAC and a required linerity of 16-bits, it may be of the form w(n)=1100000000101100. In the signal band, wherein loop filter gain is very high, the spectrum of the actual DAC output, v'(n) closely follows that of the input with excellent linearity. Since at the same time w(n) is an accurate digital representation of the DAC output, its baseband spectrum must also correspond very accurately to the input spectrum [2].

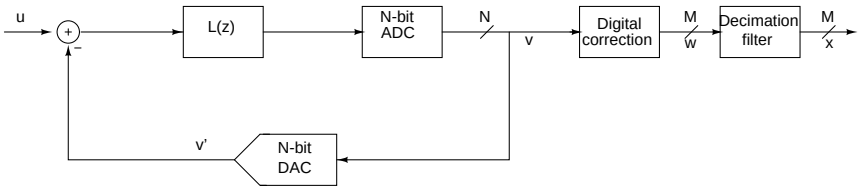


Figure 6.1: General scheme of a digitally corrected delta sigma ADC [2]

6.2 Principle

One way of calibrating the DAC is to reconfigure the loop as a single bit modulator and measure all the elements of the multibit DAC against a single element. But this reconfiguration requires modifying the loop filter because a single bit modulator is unstable with the high OBGs typical of multibit modulators resulting in overhead in the design of the loop filter and additional simulation effort for verifying the circuit in all modes.

The method used to implement the calibration in the current design overcomes the above mentioned shortcomings. The technique presented here is based on observing the idle channel output with DAC units removed one at a time. The modulator's output settles to D_{off}, offsets of the loop filter and imperfect disabling of the input, when the input to the modulator is zero.

The current design has a 16 level DAC, $D_{0...6,7,8...14}$. In the idle state, $D_{0..5,8..14}$ are not switched i.e., $D_{0..4}$ contribute with a positive sign and $D_{9..14}$ contribute with a negative sign. Initially an offset of 4 LSB is added to move the swiching activity from $D_{5..8}$ to $D_{9..12}$. First D_0 is removed from the circuit. When an element is removed, its contribution is zero. Since D_0 does not change its sign (the switching is in $D_{9..12}$ range), and the DAC output is subtracted from the input, this is equivalent to providing an input of D_0 to the modulator. The average digital output $V_{av,0}$ equals $D_0 + D_{off} + NL|_{D_0+D_{off}}$ is the input referred nonlinearity of the DAC at an average output of $D_0 + D_{off}$. Next, remove D_1 from the circuit. This is equivalent to providing an input of D_1 to the modulator. The average digital output $V_{av,1}$ equals $D_1 + D_{off} + NL|_{D_1+D_{off}}$. Since D_0 and D_1 differ by a very small amount, the nonlinear contributions $NL|_{D_0+D_{off}}$ and $NL|_{D_1+D_{off}}$ can be considered identical to a first order [3].

Thus, the difference between D_0 and D_1 can be calculated very simply by taking the difference between the corresponding average digital outputs. Similarly the diffences between D_2 and D_1 upto D_7 and D_6 can be stored without changing the

offset voltage at the input to the modulator [3].

$$D_{k+1} - D_k = V_{av,k+1} - V_{av,k} K = 0, 1...6 \tag{6.1}$$

Now, a negative input offset of 4 LSB is added to the modulator. This will move the switching to $D_{1..4}$. Now, since $D_{8..14}$ are not switching i.e. they are always switched negatively, they can be removed one by one.

$$D_{k+1} - D_k = V_{av,k} - V_{av,k+1} K = 7, 8...14 \tag{6.2}$$

Thus all the difference errors of successive DACs are obtained. From the successive differences obtained, difference w.r.t. one DAC element, D_0 is obtained. The correction values $E_0....E_1$ are given by the below expression.

$$\begin{bmatrix} E0 \\ E1 \\ . \\ . \\ . \\ E15 \end{bmatrix} = \begin{bmatrix} -1 & -1 & ... & -1 \\ +1 & -1 & ... & -1 \\ . & & & \\ . & & & \\ . & & & \\ +1 & +1 & ... & +1 \end{bmatrix} \begin{bmatrix} 0 \\ D_2 - D_1 \\ . \\ . \\ . \\ D_N - D_1 \end{bmatrix} \tag{6.3}$$

6.3 Implementation

The architecture to implement the calibration is shown in the fig 6.2. Since the operations are done one after the other, the same hardware can be used to accomplish all the three steps - obtaining the difference DAC element errors, Finding the DAC element errors with respect to one DAC element and obtaining the correction values.

The time period of the clock that is common with the modulator is 0.651micro seconds. Slow clock module slows down this clock rate. This module essentially is a set of five toggle flip flops. A slower version of the clock is needed so as to give the decimation filter sufficient time to settle and give out the correct digital code corresponding to the input applied to the modulator.

All the control signals are derived from a counter that operates with slow clock. To generate all the control signals, 9 toggle flip flops are needed. Counter-ctl-gen module contains the assembly of 9 negative edge triggered toggle flip flops. This unit also contains a set of four positive edge triggered toggle flip flops. The control signals generated from this second set of flip flops are used to turn off the DAC units one after the other.

There are two sets of sixteen registers whose size is 16 bits, namely, a and b. The other hardware blocks are multiplexer, demultiplexer, 16 bit adder, two's complement generators and a delay flip flop as shown in the fig 6.2. The process of obtaining the calibration values is accomplished in three steps - step0, step1 and step2.

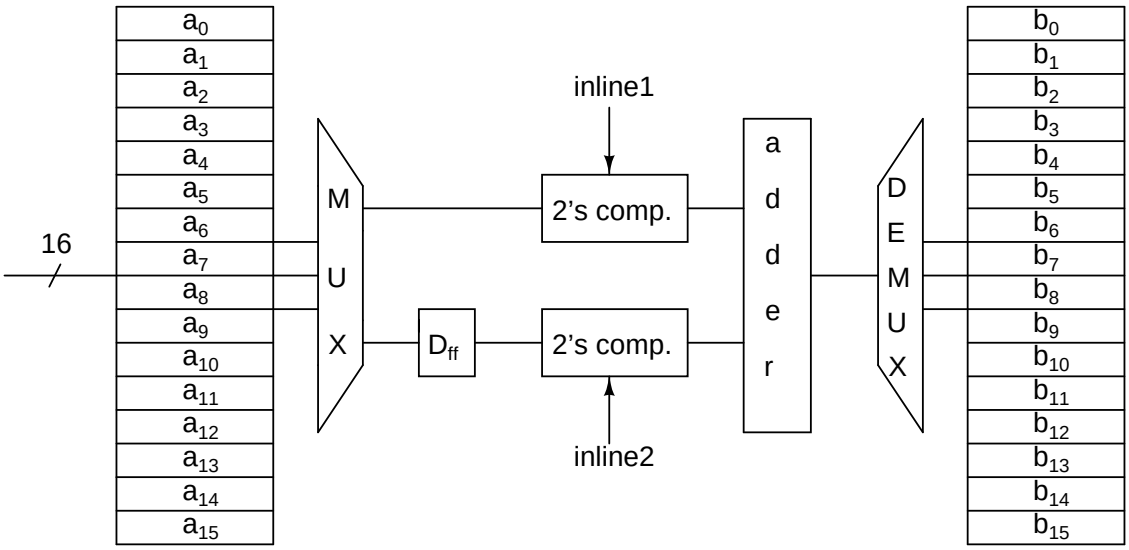


Figure 6.2: Step0: Obtaining the differences between successive DAC element errors

In step0, outputs of the decimation filter when each DAC element is removed one by one, are to be stored in register set a. Further, in the same step, these values are processed and difference between successive values, stored in the register set a, are obtained and stored in register set b. The hardware configuration of this step is shown in the fig 6.2. Initially, after resetting the calibration unit, the counter starts generating ctl-calib and ctl-dac signals. Ctl-dac signal is generated from positive edge triggered flip flops and so, it arrives before ctl-calib which is negative edge triggered. For eg when ctl-dac is 0000, DAC0 is turned off and the

decimation filter settles to the appropriate value. later, when the negedge of the slow clock arrives, ctl-calib becomes 000000000. From ctl-calib signal the other signals - freeze-valid and freeze signals , that are needed to freeze the decimation filter output when DAC0 is turned off are generated and the value is stored in first register in the register set a. Similarly all the 15 values are stored. The differences of successive elements are obtained and stored in reg set b. During this phase, step0-valid is high. Inline1 and inline2 are the control signals which when high activate the two's complement generator blocks. In this step, for obtaining the first half set of sucessive differences, inline1 is low and inline2 is high and for obtaining the second half set of sucessive differences, inline1 is high and inline2 is low.

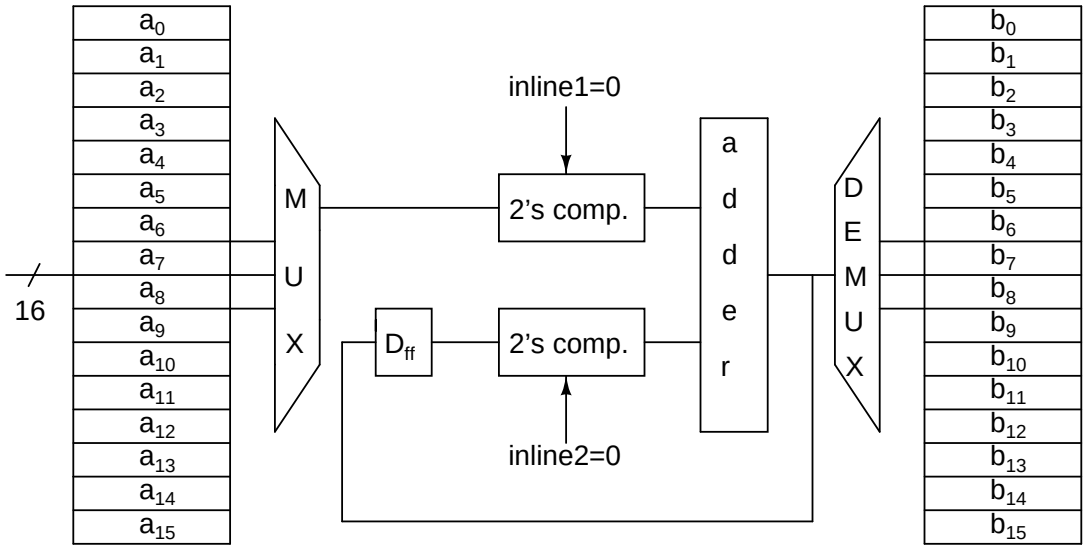


Figure 6.3: Step1: Obtaining the errors of DAC elements w.r.t. the first DAC element

After step0, step1-transfer signal is made high during which the contents of register set b are transfered to register set a. Register set b can be reused. In step1 differences w.r.t one DAC element, DAC0 have to be obtained. Now, step1-valid is made high and as a result, the hardware is configured as shown in the fig 6.3. In this step both the two's complement gernerators are turned off by setting the signals inline1 and inline2 to zero.

After step1, step2-transfer signal is made high during which the contents of register set b are transfered to register set a. In step2 the error due to mismatches

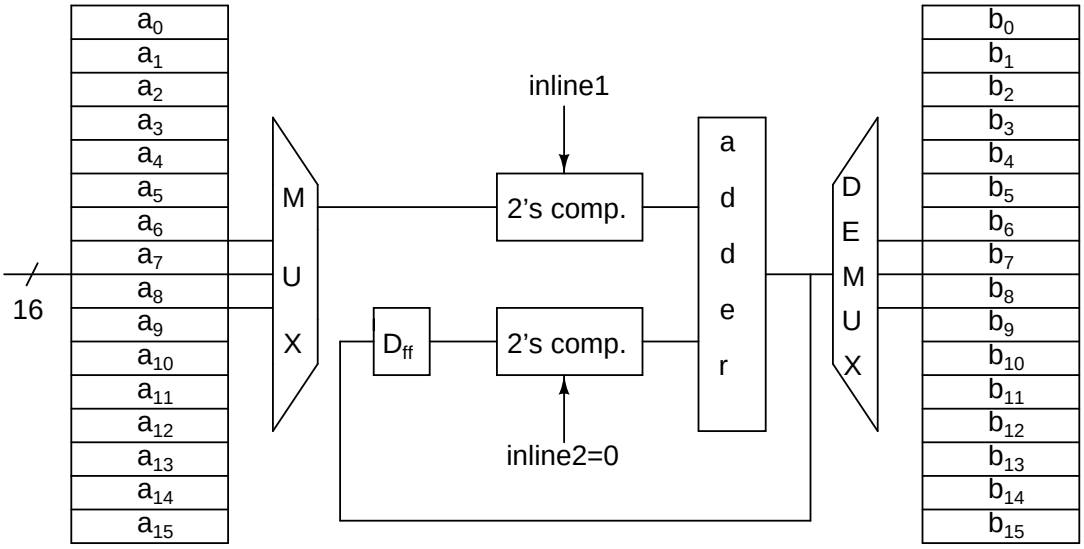


Figure 6.4: Step2: Obtaining the errors of output codes

of each code has to be computed and stored in register set b. step2-valid is made high and as a result the hardware is reconfigured as shown in the fig 6.4. A 15 bit register, inline-reg, with all its bits high initially, is used. This register is left shifted by one bit after each iteration i.e. computing the error of one code. During the computation of error due to a code, inline1 signal starts following the bits of the inline-reg starting from the LSB for processing the contents in the first register in the register set a, a0 and goes on till it reaches the MSB during which it will process the data in the register a14. Thus all the correction values are obtained and stored in register set b.

CHAPTER 7

Simulation Results and Conclusions

7.1 Simulation Results

The power optimized feedforward compensated op-amp is laid out in CADENCE. It occupies an area of 0.015mm^2. The DAC with switches on the virtual ground node side and a provision to deactivate for calibration purpose has been laid out and it occupies an area of 0.025mm^2. DEM block is coded in verilog language and synthesized. It's power consumption is 11.8μW and it occupies an area of 0.0013mm^2. The calibration unit is also coded in verilog language and synthesized. It consumes a power of 21.81 μW and occupies an area of 0.0148mm^2.

The flash converter and DAC have an associated verilog-A view. The fuctionlity of the loop filter is realized using ideal elements. Therefore, while checking any block's performance, other blocks can be realized using ideal or verilog-A modules. This greatly reduces the simulation time.

The results of the various simulations run on the design are tabulated below. The input signal to the modulator is a $2.4V_{pp,diff}$ sinusoid at a frequency of $6KHz$. 8192 point fft of the output of the modulator is taken and tabulated.

Loop Filter	Flash ADC	Clk Generator	DAC	SNDR	SHD2	SHD3
Ideal	VerilogA	Ideal	VerilogA	109	130	132
Ideal	Schematic	Schematic	VerilogA	109	122	125
Ideal	VerilogA	Ideal	Schematic	107	117	134
Ideal	VerilogA	Ideal	Extracted	107	120	134
Schematic	VerilogA	Ideal	VerilogA	106	121	120
Extracted (1st opamp)	VerilogA	Ideal	VerilogA	107	121	122

Table 7.1: Simulation Results

The SNR in each of the above simulation setups was found to be in excess of 90 dB. Since every 6dB increases the resolution of the data converter by 1 bit, 90dB

SNR corresponds to effective number of bits of 15 bits. The designed ADC hence, has a resolution of 15-bits. The output PSD of the modulator when extracted view of opamp is used and ideal views for flash, DAC, bias and reference generator is used is shown in figure 7.1.

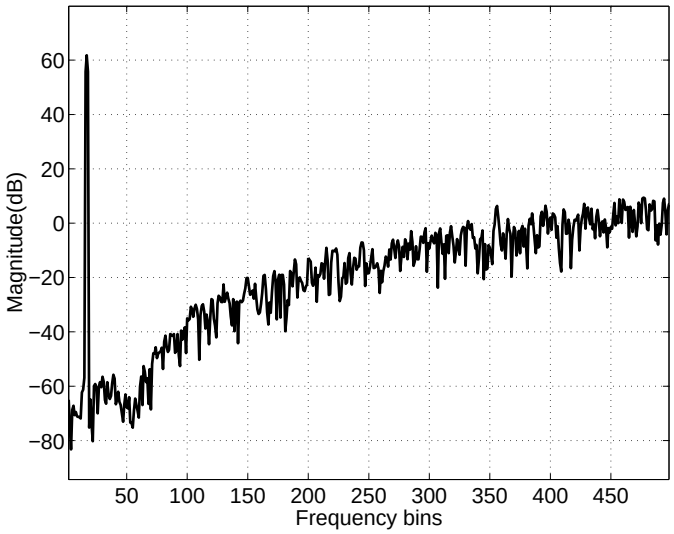


Figure 7.1: PSD of modulator output

The power consumption statistics of the designed modulator is presented below. The current design burns about $17\mu A$ lesser current. The power saved is about $29.4\mu W$. This is mostly from the loop filter and reference generation circuit. The power consumed by the digital circuitry is reduced by a factor two because of the reduction of oversampling ratio from 64 to 32. On the other hand the DEM block consumes little more power than the handcrafted DEM in Dhwani[1]. The percentage saving of power is 24.38%.

Block	Dhwani	Current Design
Flash, DEM	$6\mu A$	$7\mu A$
Ref.Gen.circuitry	$22\mu A$	$18\mu A$
Clocks	$11\mu A$	$5.5\mu A$
Loop Filter	$28\mu A$	$19.5\mu A$
Total current	$67\mu A$	$50\mu A$
Power Consumption	$120.6\mu W$	$90\mu W$

Table 7.2: Comparision of ADC power consumption

The achieved specifications of the ADC are tabulated below:

Feature	Achieved Specification
Resolution	15-bits
SNDR	105 dB
Sampling rate	$1.536MHz$
Signal bandwidth	$24KHz$
Power Consumption	$90\mu W$

Table 7.3: Achieved ADC specifications

7.2 Conclusions

A 3rd order, zeros optimized, 15 bit resolution CT $\Delta\Sigma$ modulator for audio band applications has been designed with reduced OSR (=32). Feed forward architecture is used for the opamps used in the loop filter to reduce the power consumption. The flash ADC consumes almost zero static power. Resistive DAC with switches on the virtual ground node side has been implemented. The DWA algorithm has been implemented using a HDL in the design of DEM which reduces the matching requirements across the various DAC levels. Calibration of DAC unit has been coded in Verilog language and tested for proper functioning using a testbench.

7.3 Future Work

A decimation filter that is compatable with the modulator has to be designed and the calibration unit has to be integrated and tested for its performance. Currently an off chip bypass capacitor is used to filter out the noise from the reference generator circuit and prevent it from reflecting at the input of the modulator. The reference generator circuit can be redesigned for low noise and the bypass capacitor can be avoided. All the blocks have to be integrated and laid out.

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