Feedforward opamp for Pipeline A/D converters & Audio drivers and 16 bit R-2R Digital-to-Analog Converter for Audio applications

A Project Report

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Under the guidance of
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THESIS CERTIFICATE

This is to certify that the thesis titled Feedforward opamp for Pipeline A/D converters & Audio drivers and 16 bit R-2R Digital-to-Analog Converter for Audio applications, submitted by **Sandeep Monangi**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

A 16 bit R-2R digital-to-analog converter for audio band is presented in this work.The advantage of this type of converter is the absence of sharply rising out of band noise and low OSR.

The conventional R-2R ladder structure is modified to get desired distortion performance of DAC. A high voltage generator to generate 2.7V is used in DAC which helps in increasing swing of all clock signals driving switches of ladder to 0 V-2.7 V. Even a voltage of 2.7 V can be supplied from outside the chip. I-V converter is designed with optimization in noise and area. Provision for compensating offset of OPAMP is also there. A calibration scheme using 10 bit current steering DAC is employed for 8 MSB branches of both ladders. The comparator along with digital block runs at low frequency (384kHz) during calibration of ladders. A clock MUX is used for multiplexing both 384kHz clock and 6.144MHz clock. The high voltage generator needs a clock of 6.144MHz clock. The clock MUX gives 384kHz clock during calibration period and gives 6.144MHz clock once calibration is completed.

The power dissipation in opamp(360μW) and comparator(147μW) are dominant in the DAC. Since digital blocks are running at low frequency, their swithcing power is not high. Major contribution of noise for the DAC is from opamp which is used for I-V conversion. The reference generator is optimized to redece its noise contribution. The area occupied by the design 1050 μm x 1094 μm. The reference voltage generator is not included in final design which is sent for fabrication. Rather, those voltages are supplied from outside.

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CHAPTER 1

Introduction

A 16 bit R-2R D/A converter for audio band is presented in this thesis. Oversampling sigma-delta architectures are preferred for such low-speed, high dynamic range applications because of their immunity to mismatch in the components used. However, a recent concern has been with the use of delta sigma converters which have large out of band noise with class D switching amplifers. Some of the out of band noise of the delta sigma D/A converters can be modulated by the switching frequency of the class D amplifer and fold into the audio band, thus deteriorating the signal to noise ratio. This has motivated research in traditional nyquist rate D/A converter architectures which do not have sharply rising out of band noise spectral density.
An additional benefit of the nyquist rate D/A converter is the reduced oversampling ratio. Digital circuitry running at the high oversampled rate dissipates large amount of power in delta sigma D/A converters. Digital circuitry in a nyquist rate D/A converter consumes less power because of reduced oversampling ratio.

A simple R-2R DAC consists of a resistive ladder which depending input code word can produce current output. The ladder performs a successive division by two of the reference current I_{Ref}.The left-most node has two paths for the current: one is through the 2R rung, the other is through the rest of the network, whose resistance is also 2R. The same holds for the next right node and again until the last cell divides the remaining current by two using the 2R termination resistance. An I-V converter followed by ladder will convert that code-dependent current to voltage.

The resistors contribute only thermal noise to the converter. This eliminates the flicker noise contribution from the current sources. However, matching between resistors is 0.1%. Therefore calibration technique has to be employed to achieve 16-bit resolution.
The Current to Voltage converter in the D/A converter has to be highly linear without

adding noise. Multi-stage amplifiers are needed with the advance in technologies, due to the fact that single-stage cascode amplifier is no longer suitable in low-voltage designs. The reduction of the power supply and the need for a rail-to-rail swing has given rise to multi-stage amplifiers. The short-channel effect of the sub micron CMOS transistor causes the output-impedance degradation and hence the amplifier gain is reduced dramatically.

The organization of thesis is as follows.
Chapter2 is discusses design of interstage amplifier for a 10-bit pipeline ADC based on feedforward compensation technique. This chapter also gives a brief introduction about feedforward compensation scheme. The design was discontinued as gain error coming could not be fixed.

Chapter3 discusses basic R-2R ladder architectures and modification to them to suit to current design. The R-2R ladders in the DAC uses two reference voltages $\mathrm{V_{refp}}$ and $\mathrm{V_{refm}}$. These two reference voltages along with bias currents needed by both opamp and comparator are generated in reference generator circuit. This chapter also discusses reference voltages generation and calibration principle used in brief. Both noise and distortion performances of DAC are presented. The comparator which is main part of DAC (Used for both offset calibration of opamp and calibration of ladder) is also given in this chapter.

chapter4 discuss design of opamp which is used as I-V converter in R-2R DAC and its offset calibration. The opamp used in this design makes use of feedforward compensation scheme which is dicussed in chapter2.

Chapter5 has final opamp and D/A simulation results and final layout.

CHAPTER 2

Pipeline ADC

2.1 Principle of operation

A pipelined converter divides the conversion task into several consecutive stages. The figure shows a simple 2 stage pipelined A/D converter 2.1. In general each stage consists of a sample and hold circuit, an M-bit ADC (e.g., a flash converter), and an M-bit D/A converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The m-bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an M-bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution.

In principle, a pipelined converter with P pipeline stages, each with an M-bit flash con-

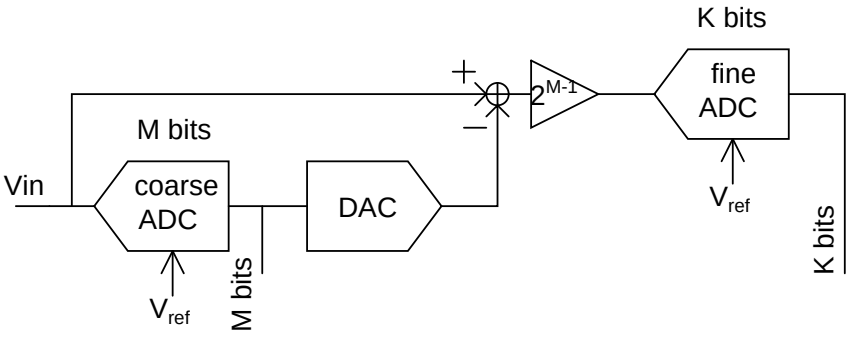

Figure 2.1: Modified architecture of pipeline ADC

verter, can produce a high-speed ADC with a resolution of N = P * M bits using $P(2^m - 1)$

comparators. In practice,however, a few additional bits are generated to provide for error correction. Pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of increasing the total conversion time from one cycle to P cycles. But since each stage samples and holds its input, P conversions can be underway simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e., one conversion per cycle. The difference is that for the pipelined converter, we have now introduced latency equal to p cycles.

2.2 Interstage amplifier design

A simple SC amplifier which can be used as a interstage amplifier is shown in figure 2.2.The operation of this is explained below.

During ϕ_2, C1 connected to ground.C2 is reset.Reset switch provides around opamp.

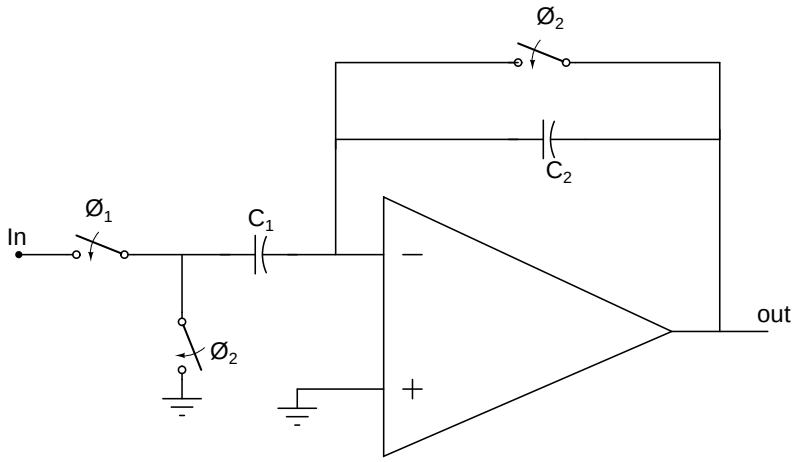

Figure 2.2: SC amplifier which can be used as interstage amplifier

During ϕ_1, input sampled on C1 , C2 is in feedback.

$\phi_2 \longrightarrow \phi_1$, charge at virtual ground node has to be preserved.

$\therefore Vout = -(\frac{C1}{C2}) * Vin.$

Our target was to design a 10 bit pipeline ADC with 500Mbps speed. The specifications of the opamp which was to be used in interstage amplifier are obtained as follows. Let M bits are resolved in first stage and k bits have to be resolved in remaining stages.

- **DC gain** The finite gain of opamp used in SC amplifier give gain error at output. This error should be less than $V_ref/2^{k+2}$ (7). From this argument open loop DC gain required for opamp is calculated as 72dB.

- **Unity loop gain frequency**

  Depending on amplifier topology, reset and amplifying phases may pose different constraints on unity loop gain frequency (7).

  In reset phase : $\omega_u \geq 2ln(2)(k+1)f_s$

  In amplifying phase : $\frac{\omega_u}{1+2^M-1} \geq 2ln(2)(k+1)f_s$

  If first stage resolves 3 bits above condition implies that opamp should have a unity loop gain frequency of 5.5GHz.

- **Choosing capacitors**

  Capacitor values have to be decided based on noise considerations. The SC amplifier with noise sources shown in the figure2.3. In these calculations noise from amplifier is ignored. During $\boldsymbol{\phi_2}$

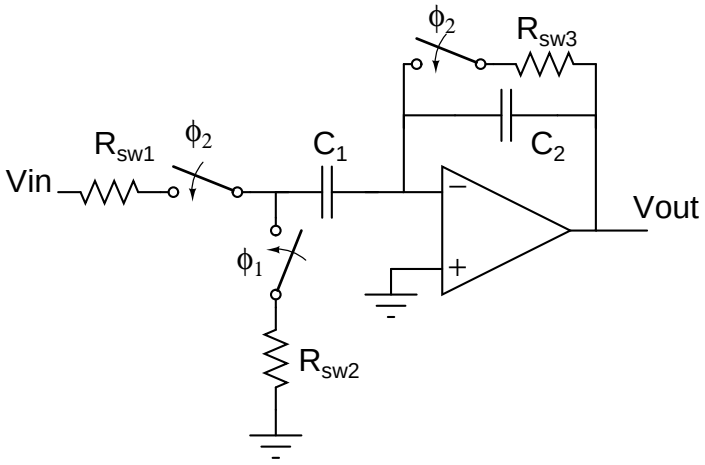

Figure 2.3: Noise sources in a switched capacitor amplifier

– Because of R_{sw1} : C_1 has a noise voltage variance of KT/C_1

– Because of R_{sw2} : C_2 has a noise voltage variance of KT/C_2

During $\boldsymbol{\phi_1}$

– Because of R_{sw1} : Its contribution in ϕ_1 will be amplified to $\frac{KT}{C_1}\left(\frac{C_1}{C_2}\right)^2$.

– Because of R_{sw2} : Its contribution in ϕ_2 will be held.

– Because of R_{sw3} : Results in a noise of KT/C_1 on C_1 and $\frac{KT}{C_1}\left(\frac{C_1}{C_2}\right)^2$ at output.

Total output noise is approximately $\frac{2KT}{C_1}\left(\frac{C_1}{C_2}\right)^2$

$\therefore$ Input referred noise will be approximately 2KT/C_1. This input referred noise should be much less compared to LSB of ADC.

$3\sigma < 1/4(LSB) \Rightarrow \sqrt{2KT/C_1} < 1/12(V_{ref}/2^{10})$

From above considerations C_1 is calculated as 300fF and C_2 as 37.5fF (For closed loop gain to be 8, C_1 must be eight times that of C_2).

2.3 Feed forward compensation

The block diagram of feedforward scheme is shown in the figure 2.4. The main concept of feedforward technique can be explained by assuming a single-pole response for the three blocks (5).A_{v1},A_{v2},A_{v3} are the dc gains of first, second and feedforward stages of amplifier. The pole of the first stage is located at ω_{p1} ($= \frac{g_{01}}{c_{01}}$) and the second and third stages have a common pole at ω_{p2} ($= \frac{g_{02}}{c_{02}}$).

The overall amplifier voltage gain is

$$\begin{aligned} H(s) &= -\frac{A_{v1}A_{v2} + A_{v3}(1+\frac{s}{\omega_{p1}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \\ &= -\frac{(A_{v1}A_{v2} + A_{v3})(1+\frac{sA_{v3}}{(A_{v1}A_{v2}+A_{v3})\omega_{p1}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \end{aligned} \tag{2.1}$$

The OTA transfer function has two poles and a LHP zero created by the feedforward path. The dc gain is given by $A_{v1}A_{v2}+A_{v3}$ and the dominant pole is located at ω_{p1}. The location of LHP zero is

$$Z_1 = -\omega_{p1}(1 + \frac{A_{v1}A_{v2}}{A_{v3}}) \tag{2.2}$$

If the zero is well before unity gain frequency of opamp, phase margin will improve. In general, the number of LHP zeros created by the feedforward path is equal to the order of the first stage. This compensation scheme can be extended for a generic n-stage amplifier as shown in figure 2.5.

2.3.1 Effect of pole-zero mismatch

Even we designed to cancel a pole by the zero created from feedforward path, because of process variations there can be a pole-zero mismatch resulting in a pole-zero doublet. The pole-zero doublet can degrade phase margin from 90^o. Except that frequency response may not change much. But time response may effect substantially depending in spacing between pole-zero doublet and zero frequency (6).

To understand effect of pole-zero doublet on time response following simple feedback system has been considered 2.6.

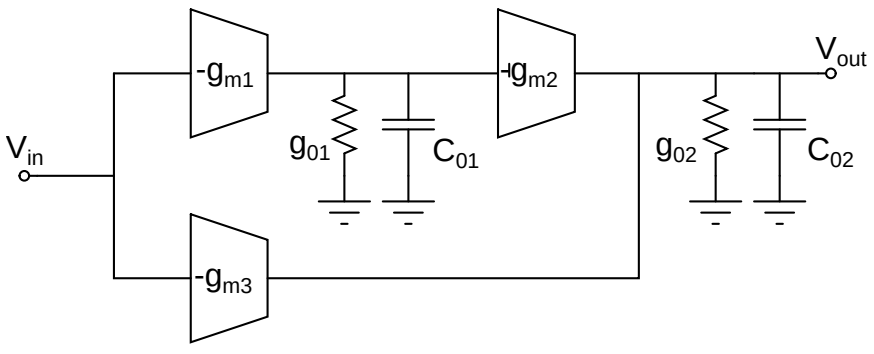

Figure 2.4: Basic Block Diagram of Feed forward compensated amplifier

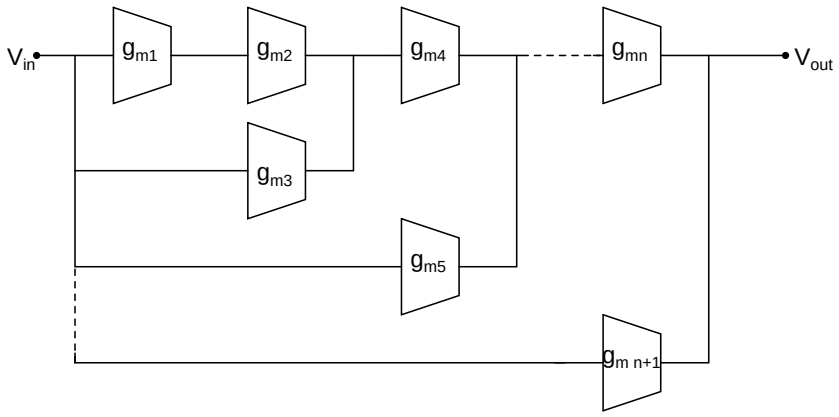

Figure 2.5: Feed forward compensation for n-stage amplifier

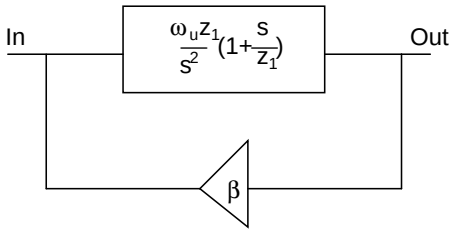

Figure 2.6: A simple feedforward system

$$\text{The closed loop transfer function for above system} = \frac{\omega_u s + \omega_u z_1}{s^2 + \beta\omega_u s + \beta\omega_u z_1}$$

$$\text{The step response of above system} = L^{-1}\left(\frac{\omega_u s + \omega_u z_1}{s(s^2 + \beta\omega_u s + \beta\omega_u z_1)}\right).$$

$$= \frac{1}{\beta} - \frac{X}{\beta\sqrt{\Delta}}e^{-Xt} + \frac{Y}{\beta\sqrt{\Delta}}e^{-Yt} \quad (2.3)$$

$$\text{where}\Delta = \beta\omega_u(\beta\omega_u - 4Z_1) \quad (2.4)$$

$$X = \frac{\beta\omega_u}{2} + \frac{\sqrt{(\beta^2\omega_u^2 - 4\beta\omega_u Z_1)}}{2} \quad (2.5)$$

$$Y = \frac{\beta\omega_u}{2} - \frac{\sqrt{(\beta^2\omega_u^2 - 4\beta\omega_u Z_1)}}{2} \quad (2.6)$$

From above equations for slow settling component ,magnitude proportional to doublet frequency and time constant inversely proportional to doublet frequency. So low frequency doublets will give a response which persists for a long period but with smaller amplitude. When 0.01% settling time is the constraint, lower frequency doublets cause more degra-

dation in settling time because of higher time constant. When 1% settling time is the constraint, higher frequency doublets cause more degradation because of large amplitude ,though it decays faster.

The schematic of amplifier used is given below 2.7. The opamp is constructed from three cascaded NMOS differential pairs with local common mode feedback and feedforward compensation.

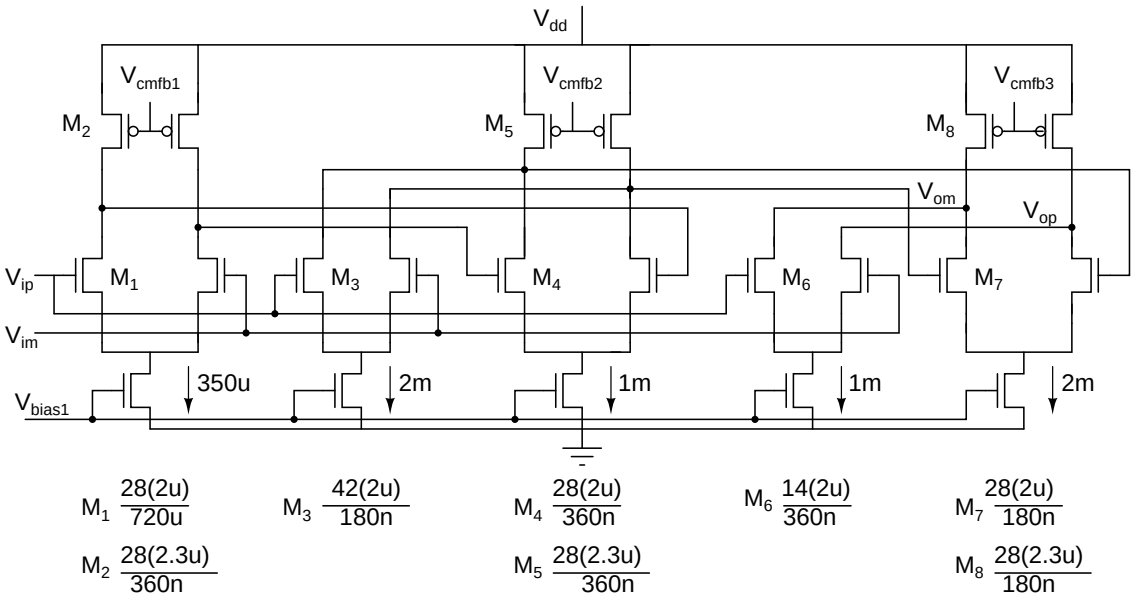

Figure 2.7: Feedforward compensated opamp

The frequency response of above feedforward compensated amplifier with a capacitive load of 300fF is shown in figure 2.8. This amplifier is used in fully differential version of SC amplifier described above. But the problem is since the transistors in last feedforward path are from input to output, their C_{gd} is across feedback capacitor of SC amplifier resulting in decreasing gain from 8 2.9. Above problem can be solved by adding cascode devices to transistors in feedback path as shown in the figure 2.10 or by trying to nullify effect by providing same parasitic capacitor to other output 2.11.The equivalent circuit

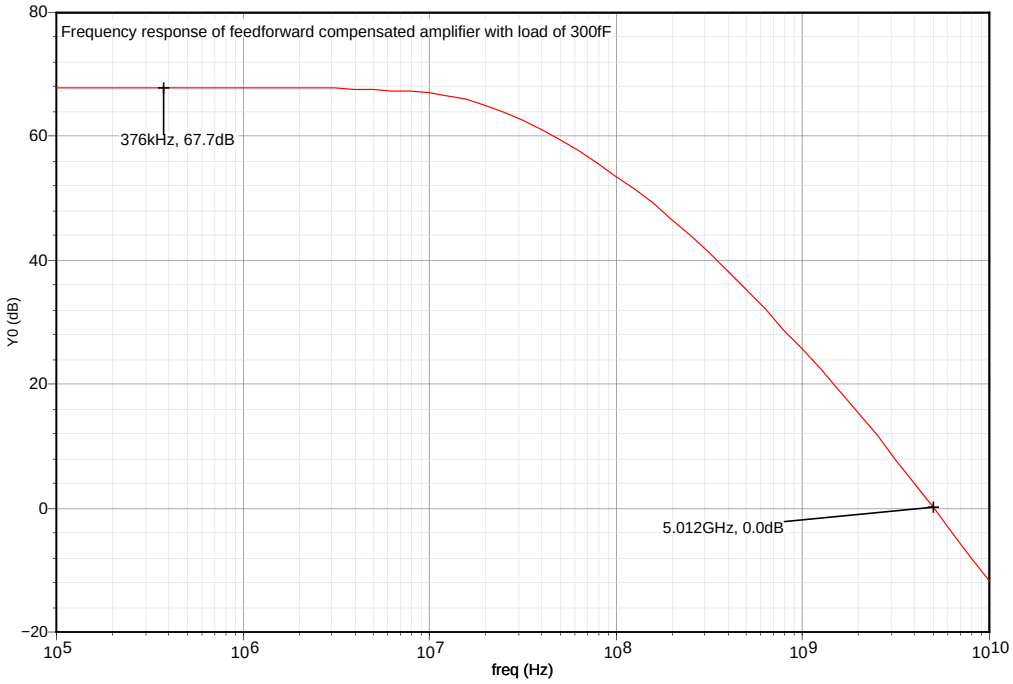

Figure 2.8: frequency response of Feed forward compensated opamp

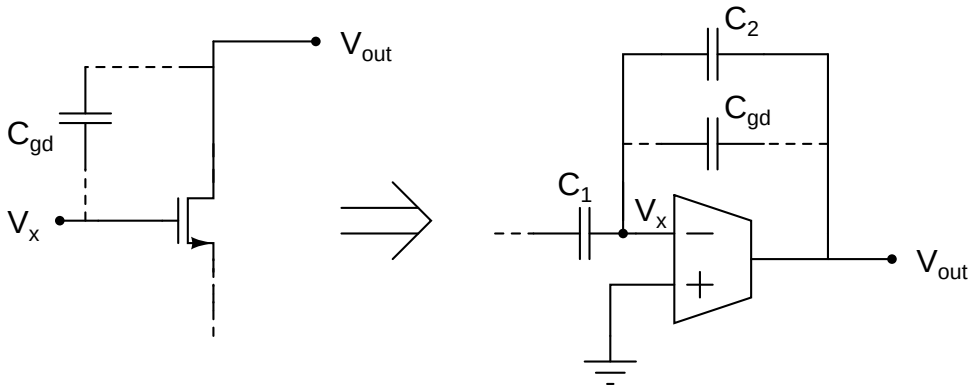

Figure 2.9: Problem with feedforward amplifier when used in SC applications

after doing above modifications is also shown in the figure. The step response of SC

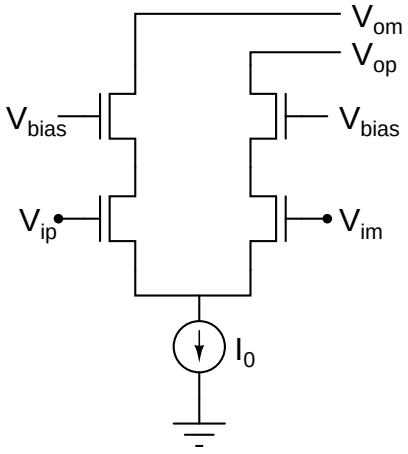

Figure 2.10: Adding cascode devices to feedforward path

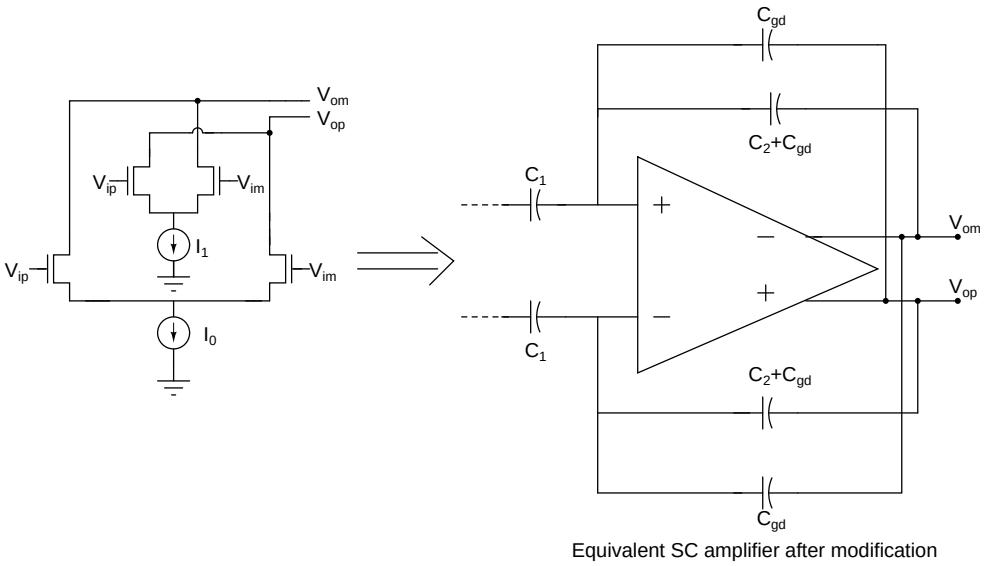

Figure 2.11: Nullifying effect of parasitic capacitor

amplifier after doing these modifications is shown below 2.12. With DC gain it is designed for, output should be 159.4mV for a step of 20mV.But the output is able to reach only 145mV. The source of gain error has to be found.

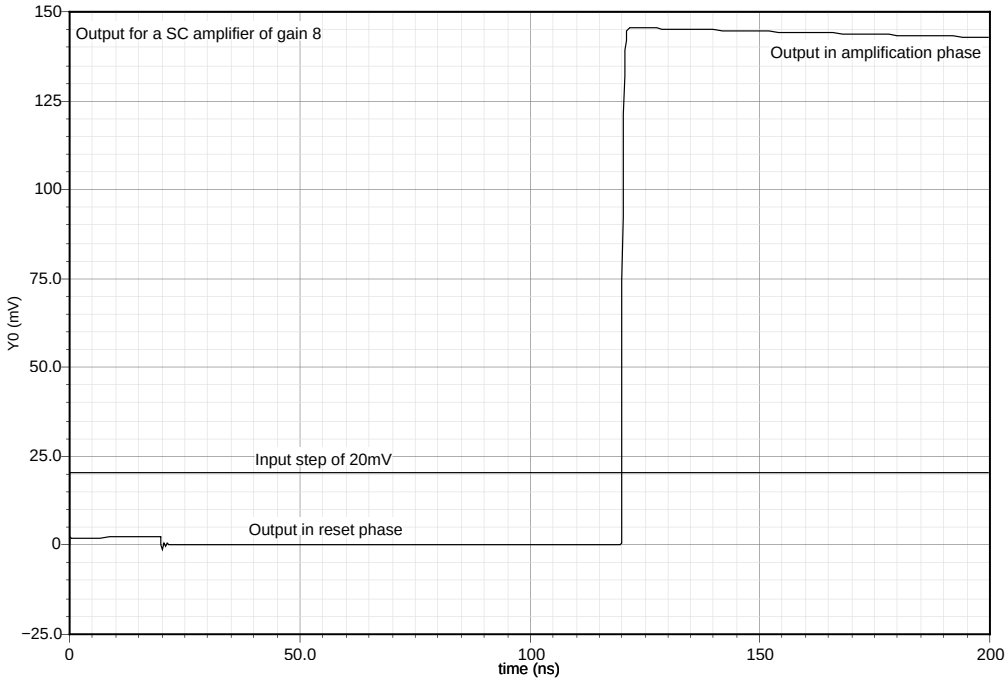

Figure 2.12: Step response of SC amplifier of gain 8

CHAPTER 3

DAC architecture

The Audio Digital-to-Analog Converter has the following specifications.

Sample Frequency	6.144 MHz
Load	1 kΩ,100 pF
Distortion	$<$-80 dB
Idle Channel Noise	5μV
Power	$< 2\ mW$

3.1 R-2R Ladder structures

Assuming $\mathrm{V_{dsat}}$ of transistors 0.15 V, the opamp can give output from 0.15 V to 1.65 V with power supply of 1.8 V. The conventional R-2R ladder structure is shown in figure 3.1. With common mode voltage of 0.9 V and $\mathrm{V_{ref}}$ 1.65 V, the output voltage ranges from 0.15 V to 0.9 V. The swing from this type of architecture is very low.

With appropriate current offset, we can get a swing of 0.15 V to 1.65 V. But the current

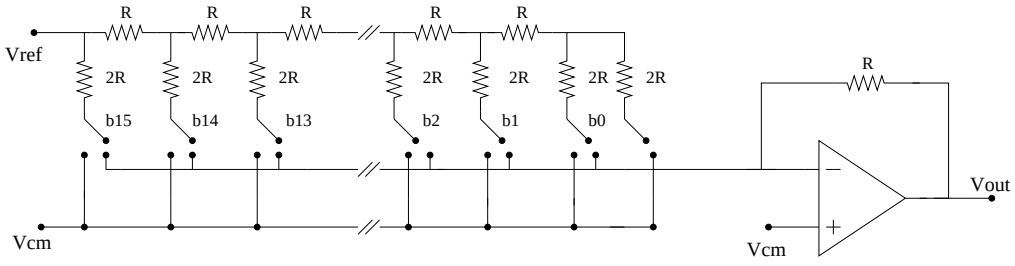

Figure 3.1: Conventional R-2R ladder architecture

sources used to get the offset will introduce flicker noise 3.2.

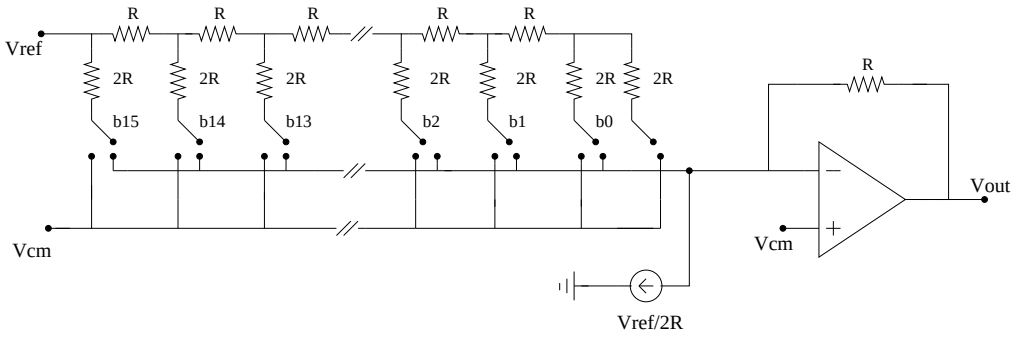

Figure 3.2: R-2R ladder with dc offset

To get a wide swing i.e., from 0.15 V to 1.65 V, the current source should not be of fixed value and should be dependent on input code. The differential ladder structure with complementary controls is shown in the figure 3.3. With V_{refp} 1.65 V and V_{refm} 0.15 V ,the possible swing from this type of architecture is from 0.15 V to 1.65 V.

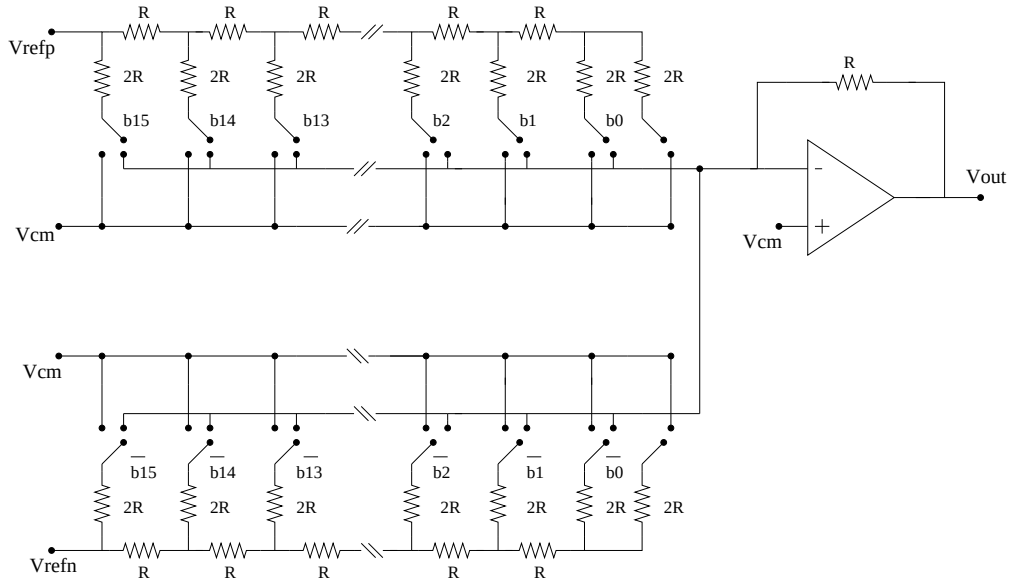

Figure 3.3: R-2R ladder with differential architecture

3.1.1 Switch-Sizing

MOS transistors are used as control switches. The common mode voltage of 0.9 V is used. To obtain a relatively small value of small signal resistance for a given size, a boosted supply voltage of 2.7 V was used. The ladder resistor was fixed at 20 kΩ to meet distortion and noise specification. The resistor value and MOS switch sizes were fixed through simulations. The MOS switches were sized for a small signal ON resistance of 3.6 Ω. In the ladder, we get binary weighted current in each arm. To maintain, constant voltage drop across the switch, the switch sizes were progressively decreased from MSB. The switch sizes are tabulated.

Control Bit	Switch Size
MSB	$\frac{128\mu}{0.18\mu}$
MSB-1	$\frac{64\mu}{0.18\mu}$
MSB-2	$\frac{32\mu}{0.18\mu}$
MSB-3	$\frac{16\mu}{0.18\mu}$
MSB-4	$\frac{8\mu}{0.18\mu}$
MSB-5	$\frac{4\mu}{0.18\mu}$
MSB-6 to LSB	$\frac{4\mu}{0.18\mu}$

Table 3.1: Ladder Switch Sizes

3.2 Switching Schemes

The main ladder and complementary ladders can be operated using following switching schemes in the R-2R DAC.

Complementary switching : The main ladder and complementary ladders can be switched using complementary signals. Even if there is mismatch between LSBs of two ladders, output will experience smooth switching over whole input code range causing no degradation in distortion performance. The disadvantage in this scheme is that there will be noise from ladders at mid code, although there is no current flowing to output.

Switching in middle : Main ladder is used for positive values of input and comple-

mentary ladder is used for negative values of input. If LSBs of two ladders are different, output transition at midcode won't be smooth which degrades distortion performance. The idle channel noise requirement can be very easily met with this scheme because at midcode there won't be any noise coming from ladders.

3.3 Calibration principle

The working of R-2R DAC very much depends on accuracy of resistors used. Because of mismatch in resistors in an uncalibrated DAC, INL can be as high as 35LSBs (8). Clearly to address these mismatch there should be a calibration scheme. The principle used in calibration of R-2R DAC is explained below.

First 8 branches of each ladder are calibrated using a current steering DAC of 10 bit resolution. In the ladder the current will divide into equal parts at each branch. This principle is used in calibration. Output of I-V converter due to these two current are compared and any difference that is occurring due to mismatch in resistances is pumped using current steering DAC. The calibration starts in the main ladder with 8th branch from MSB branch being calibrated first and it continues upto MSB branch. These same steps are repeated for complementary ladder also. The details of this calibration scheme are in (2). A clockMUX is used to multiplex clocks of frequency 384kHz and input frequency. The MUX output gives 384kHz clock during calibration period so that the process of calibration runs at a clock frequency 384kHz. After calibration is over, the MUX output gives clock of input frequency.

3.4 Distortion performance of DAC

The switches in same branch are operated by complementary signals. If the clocks have overlapping period then it is equivalent to having a finite resistance path between inverting and non inverting terminals of opamp which reduces loop gain and hence total harmonic

distortion. To avoid this the clocks driving switches in same branch are made to have a non overlapping period of 2.5ns. There is an improvement of 4dB in 2nd harmonic after driving switches with non overlapping clock.

With sampling frequency of 6.144MHz, input frequency of 1.5kHz the DAC is simulated in complementary switching mode. An 8th order butterworth filter with cutoff frequency 100KHz is used at output to smoothen the waveform. For simulation purpose an error current of 20nA is introduced externally in first eight branches of both ladders. The input bits of calibration DAC are chosen to compensate for the error current.4096-pt DFT of output is shown below 3.4. Under the same conditions the DAC is simulated in

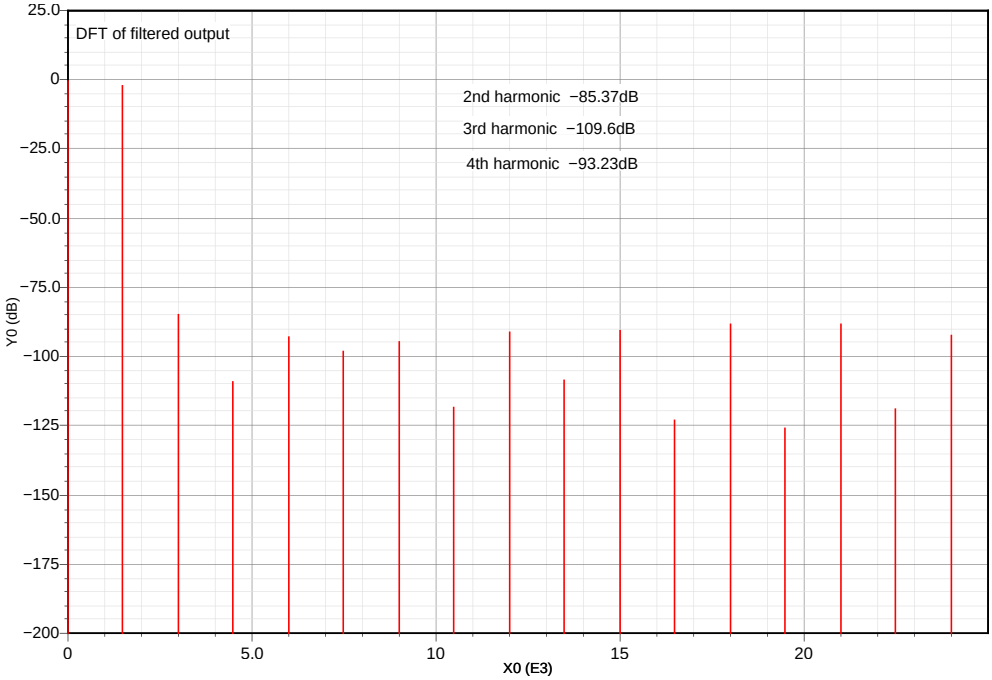

Figure 3.4: DFT of filtered output of DAC with OSR 128 in complementary switching mode

switching in middle mode. In both modes THD (-78dB and -75dB respectively) is found to be much less than ideal case (In which ideal switches used instead of MOS switches).

In switching in middle mode, only one of ladder is operating at any time. When a bit is going from 2.7 V to 0 V, some of the charge stored on C_{gs} of switch can go to I-V converter feedback resistor which can distort output waveform 3.3. To reduce this

effect and hence improving distortion performance of DAC, dummy ladders are added to both ladders. These dummy ladders are going to be operated with signals, which are complementary of corresponding switch signals in the main ladders. Since the switch connecting the branch to $\mathrm{V_{cm}}$ in dummy ladder isn't for any performance enhancement, it can be driven by $\mathrm{V_{cm}}$. The R-2R ladder after introducing the dummy ladders along with their switching signals are shown in below figure for the case of switching in middle mode 3.5.Signals a16 to alast and b16 to blast are generated by digital block according to mode of operation.The above problem is not an issue in case of complementary switching mode.Because in this mode, when one transistor's driving signal going from 2.7 V to 0 V there is another transistor in complementary ladder which is driven by signal going from 0 V to 2.7 V.So for these mode,switches in the dummy ladders are driven by constant voltage i.e., 2.7 V. The structure of R-2R ladder in this mode shown in below figure 3.6.

With above modifications, distortion performance of DAC is verified again and it found to be improved. The DFT of output in switching in middle mode 3.7 and complementary switching mode 3.8 are shown in following plots.The DFT of DAC output for an OSR of 8 is shown below for switching in middle mode 3.9 and complementary switching mode 3.10. The THD values for different OSR in both modes are tabulated in 5

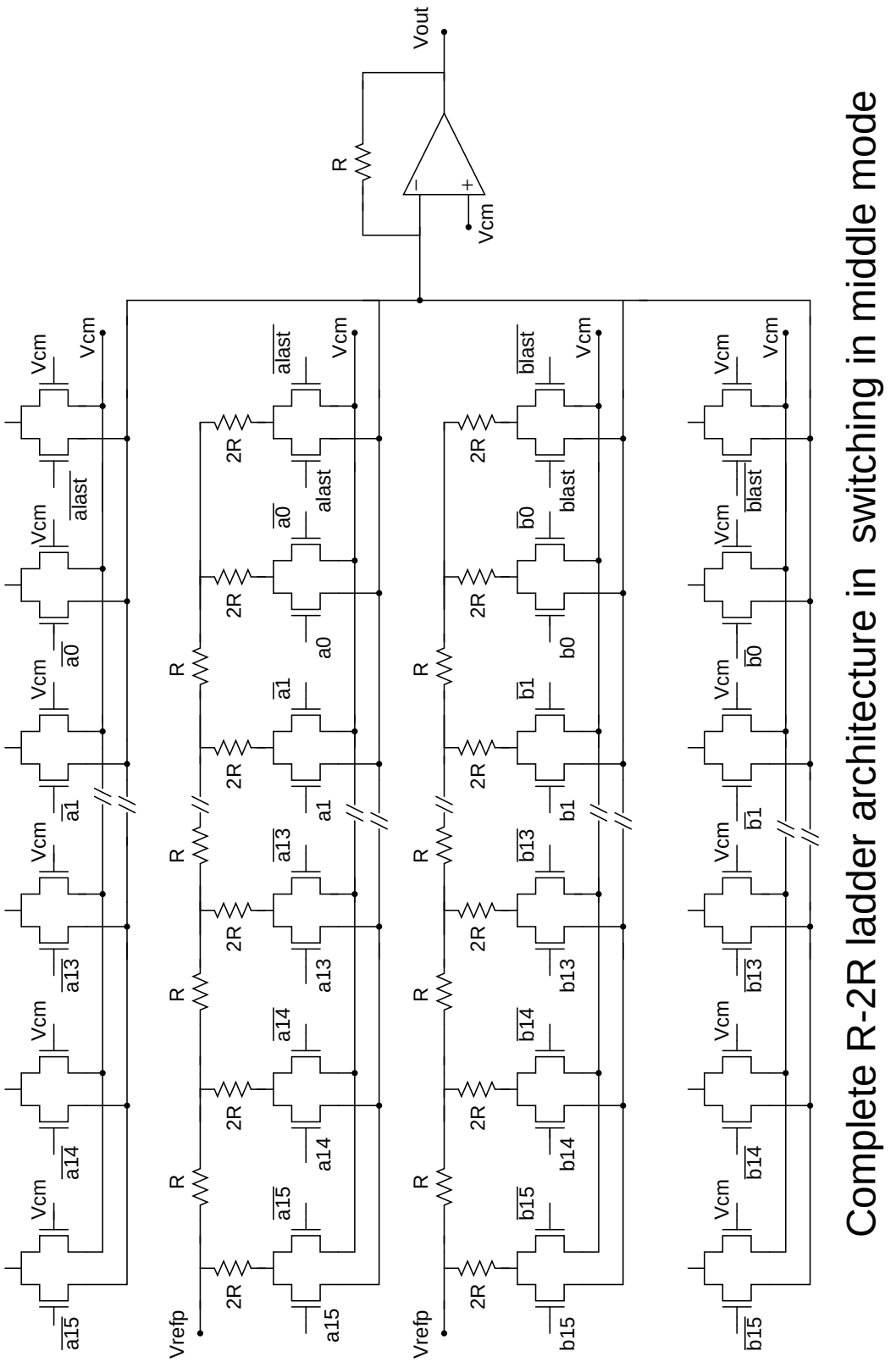

Figure 3.5: Complete R-2R ladder structure in switching in middle mode

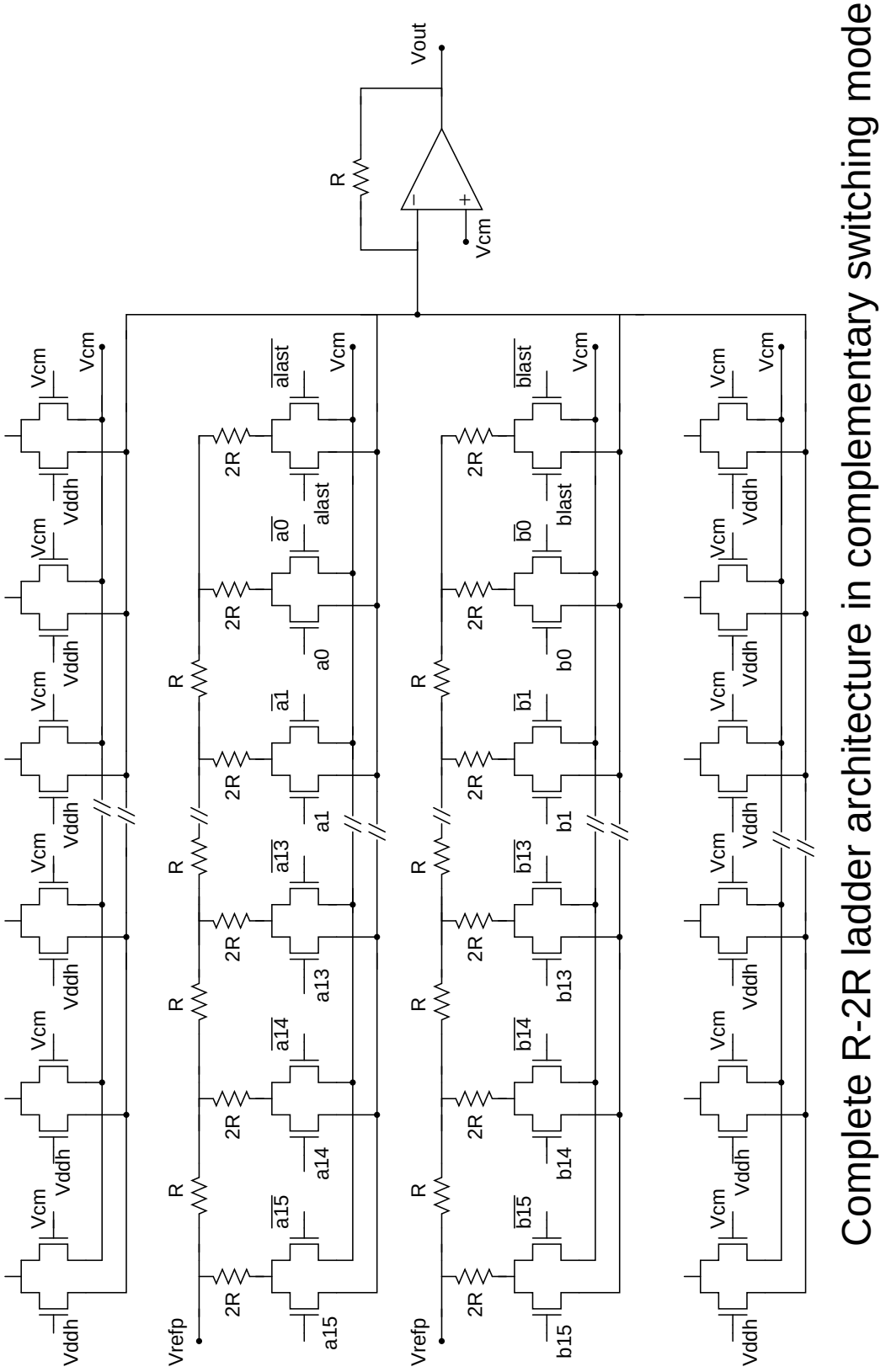

Figure 3.6: Complete R-2R ladder structure in complementary switching mode

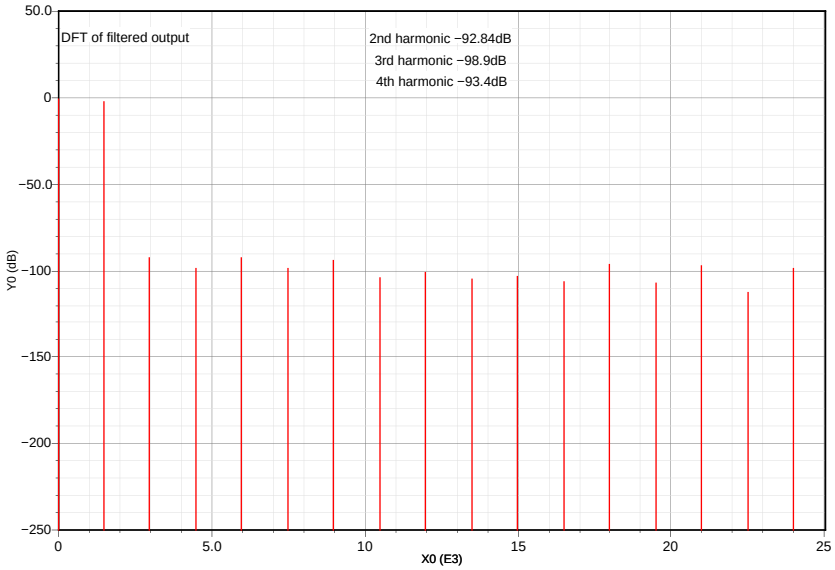

Figure 3.7: DFT of filtered output of modified DAC with OSR 128 in switching in middle mode

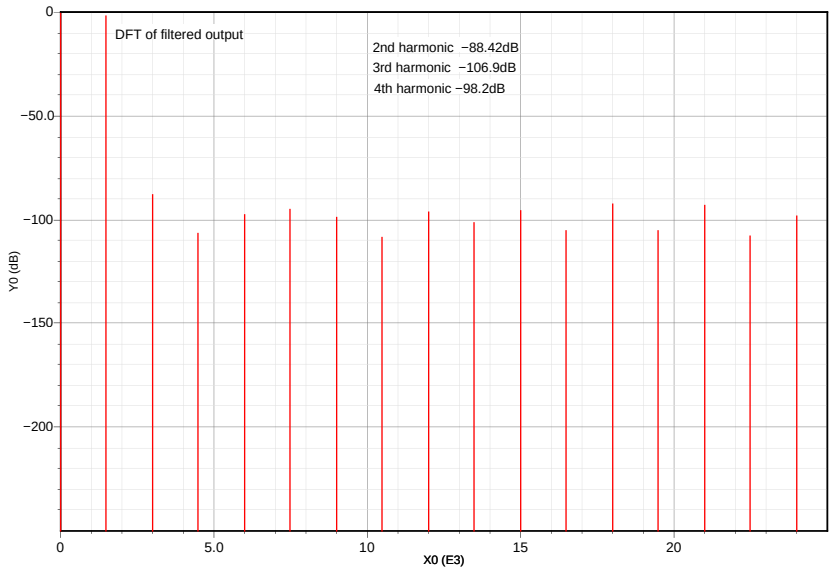

Figure 3.8: DFT of filtered output of modified DAC with OSR 128 in complementary switching mode

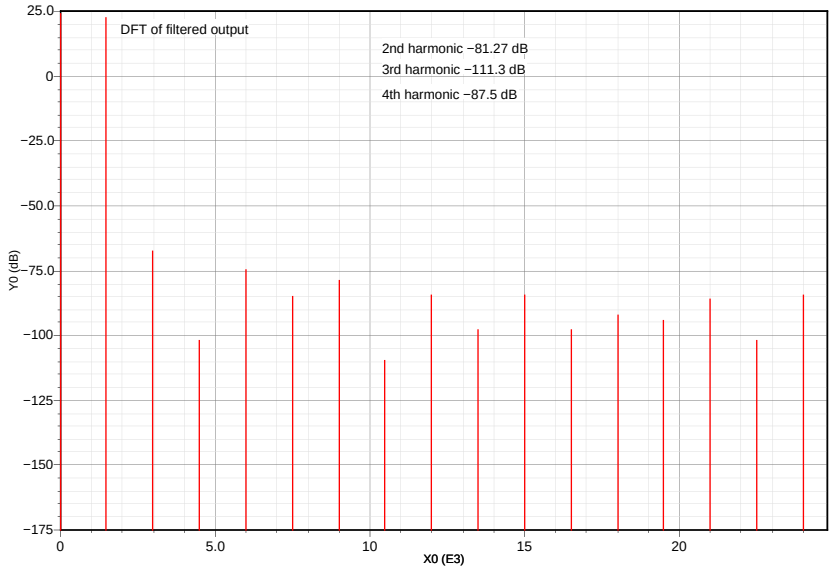

Figure 3.9: DFT of filtered output of modified DAC with OSR 8 in swithing in middle mode

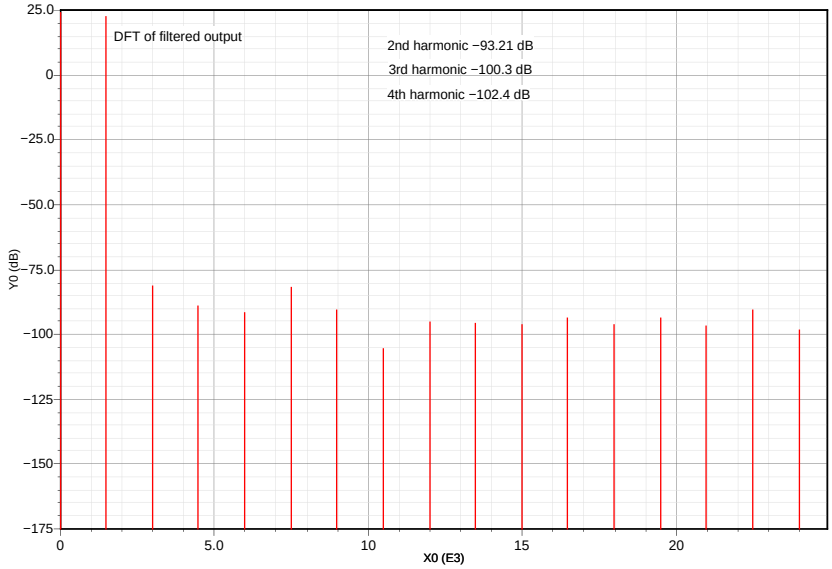

Figure 3.10: DFT of filtered output of modified DAC with OSR 8 in complementary switching mode

3.5 Reference voltages generation

The reference voltages used in DAC are generated using scheme shown in the figure 3.11. The opamp used follows same principle as that used in (9). The voltage drop across the

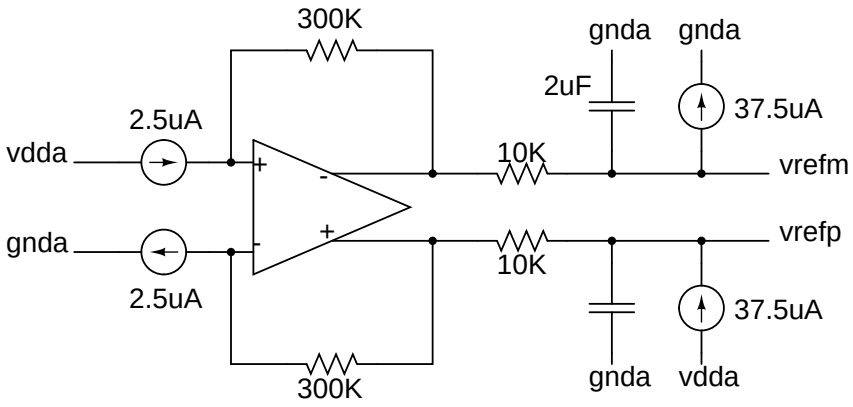

Figure 3.11: Generation of references

300k resistors is 0.75V. The choice of resistor value is defined by noise requirement. The CMFB loop of the opamp forces its output voltages to 1.65V and 0.15V. A low pass filter is connected at the output of the opamp to filter out any noise present in the references. Each ladder consumes 37.5μA for any input code and it is provided so that opamp ideally need not supply any current. The input current sources and the extra 37.5μA current sources must be resistance dependent. Otherwise, output voltage can change drastically along 3 corners of resistance value.

Figure 3.12 shows the schematic that is used for generating reference currents. The inputs to the reference generator are - a bias current of 2.5 μA and an input voltage of $0.9V$ denoted as $\mathrm{V_{cm}}$ in figure 3.12. The input bias current is mirrored to generate all the tail currents. The negative feedback around R1 forces the voltage across the $180\mathrm{k}\Omega$ resistor to be equal to 0.9V. Since the $\mathrm{V_{ds}}$ across 2.5μA and 37.5μA current sources are going to be different, two separate resistor servos have to be used for generating them. The degeneration resistors are used instead of cascode transistor so as to reduce noise contribution of this circuit.

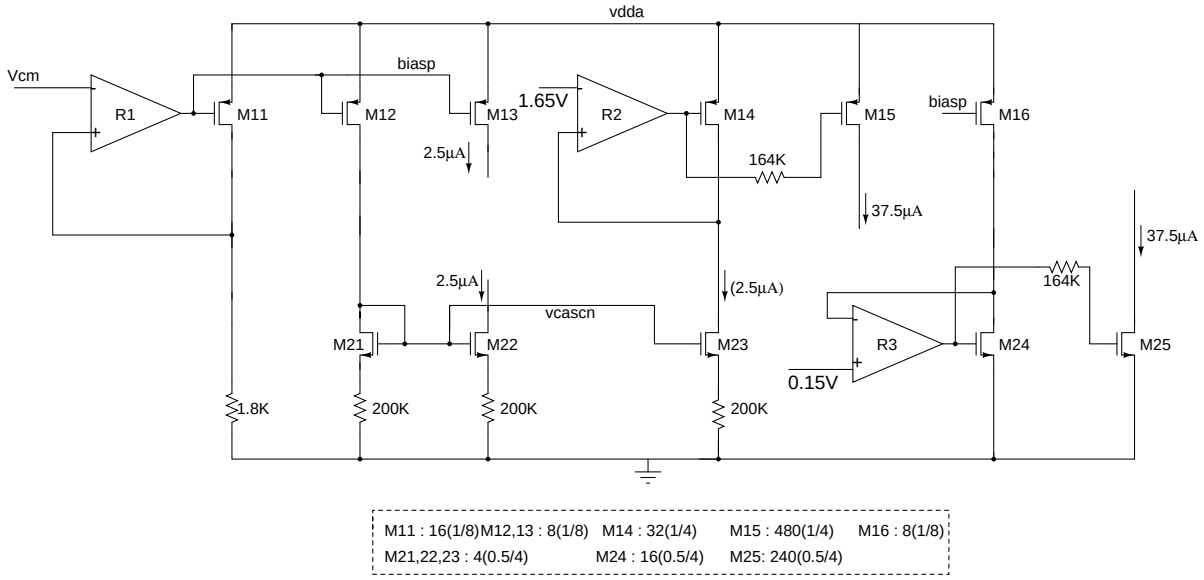

Figure 3.12: Resistor servos used to generate current sources

3.6 Noise analysis of DAC

The equivalent circuit of simple R-2R DAC is shown with all noise sources in the figure 3.13, where R_i is impedance of ladder as seen from inverting terminal. R_i is input code dependent and its maximum,minimum values being ∞ and R.

The output noise of DAC is given by

$$\begin{aligned} RMS(V_{n,out}) &= \sqrt{V_{n,ref}^2(\frac{R_f^2}{R_i^2}) + V_{n,amp}^2(1+\frac{R_f}{R_i})^2 + I_{n,Rf}^2 R_f^2 + I_{n,Ri}^2 R_f^2} \quad (3.1) \\ &= \sqrt{V_{n,ref}^2(\frac{R_f^2}{R_i^2}) + V_{n,amp}^2(1+\frac{R_f}{R_i})^2 + 4KTR_f(1+\frac{R_f}{R_i})} \end{aligned}$$

Where $V_{n,ref}$ is noise from reference voltages generator,$V_{n,amp}$ is Input referred noise of I-V converter,$I_{n,Rf}$ is noise due to feedback resistor and $I_{n,Ri}R-2R$ is noise due to ladder.

Idle channel noise in switching in middle mode is only due to opamp and is equal to 3.36μV_{RMS}. In complementary switching both ladders and reference generator also

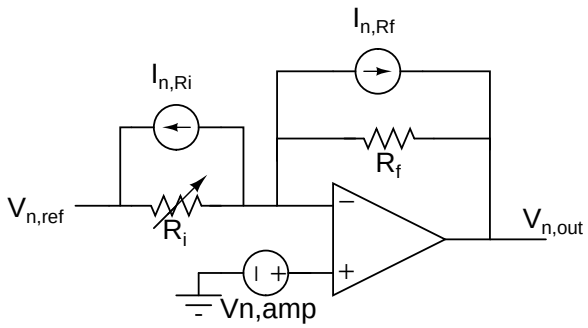

Figure 3.13: R-2R DAC with all noise sources

contributes to idle channel noise. The output RMS noise in this case obtained as $6\mu V_{RMS}$. Percentage contribution of different blocks are shown below.

Block	% of noise contribution
opamp	37.34
Both R-2R ladders	24.24
Feedback resistor	24.18
Reference generator	11.6

Table 3.2: Noise contribution by different blocks in complementary switching mode

3.7 Comparator

Comparator is very important block as it is used in both ladder calibration and offset calibration. This section discusses design of comparator. A simple comparator makes use of positive feedback. Two inverters connected back to back when biased at trip point and driven by small signal differential inputs can act as differential VCVS. The transistor level circuit for regenerative latch is shown in the figure 3.14.The clock generator which is used to genearate all clock signals is taken from (9). During ϕ_3, the parasitic capacitance at the inputs of the latch get charged to the differential input voltages ip and im. In this case since there is no path between vddd and gnda, latch doesn't consume any static power. In the regeneration phase, ϕ_1, the latch can be represented by a simplified circuit consisting of two back-to-back inverters.

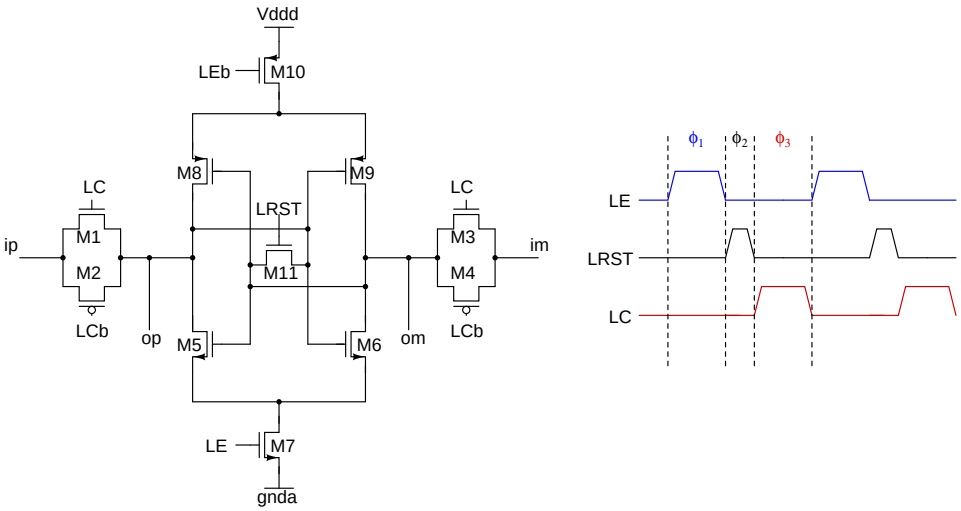

Figure 3.14: Regenerative latch

Transistor	W/L
M1,M2,M3,M4	1(0.24/0.18)
M5,M6,M7,M8,M9,M10	1(0.5/0.18)
M11	1(0.48/0.18)

Table 3.3: Transistor sizes used in latch

Due to random mismatches in the threshold voltages of the transistors in the latch, the latch can have an offset voltage. The offset of this latch is calculated and it is about 11.83 mV (10). To reduce offset of comparator, two preamplifiers are used. Autozeroing technique is employed to nullify offset of preamps. Total comparator block digram is shown in the figure 3.15.

Preamp1 is having same noise requirements as that of first stage of opamp used in R-2R

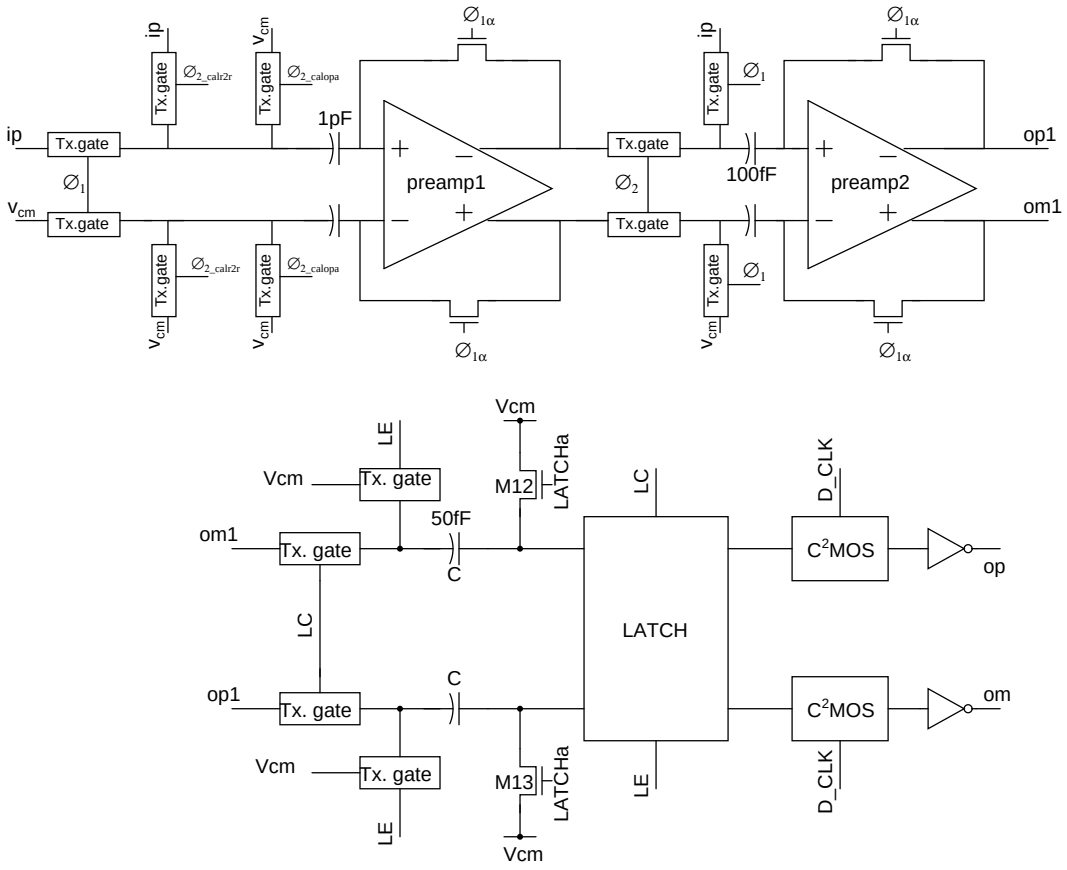

Figure 3.15: Comparator block diagram

DAC. So to meet the noise specification differential version of opamp first stage is used as preamp1. Since gain of preamp1 is very high noise constraint on preamp2 is not that much stringent. So in preamp2 quiescent current can be reduced along with large sizes of transistors. Both preamp1 and preamp2 uses same bias circuit which is similar to that of opamp 1st stage bias circuit. The schematics of both preamps along with their CMFB

circuit shown in the figure 3.16. The CMFB circuit for both preamps works based on

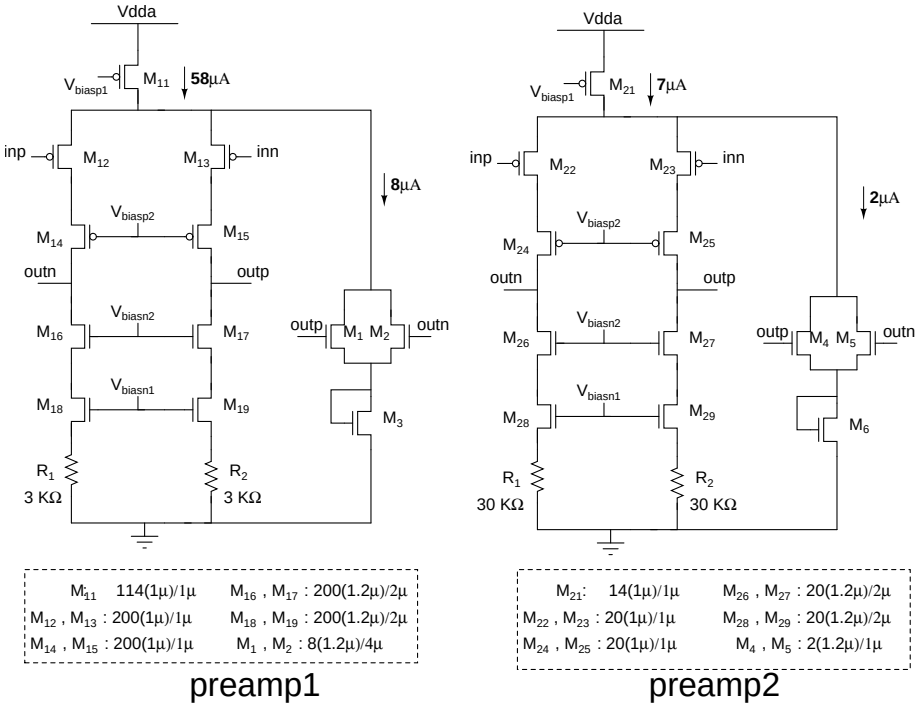

Figure 3.16: Preampifiers used in comparator

current mode feedback. The total bisa current through M_{11} is constant.If output common mode voltage of preamp1 is increasing, current through M_1 and M_2 increases. Therefore current through M_{12} and M_{13} decreases. This inturn decreases common mode voltage of preamp1. Preamp2's CMFB circuit also works on same principle. The signals ϕ_{2_calr2r} and ϕ_{2_calopa} signals indicates, whether the comparator is used for offset calibration or ladder calibration. Only one of those two signals is ON at any time.

- In case of opamp offset calibration, it should compare output of opamp to V_{cm}.
- In case of R-2R ladder calibration, it should compare input sampled at end of ϕ_{1a} to input at next rising edge of ϕ_2.

A ramp waveform is given to comparator in opamp offset calibration mode and its corresponding waveforms are shown in the plot 3.17. The detailed clocking waveforms during calibration can be found in (2).

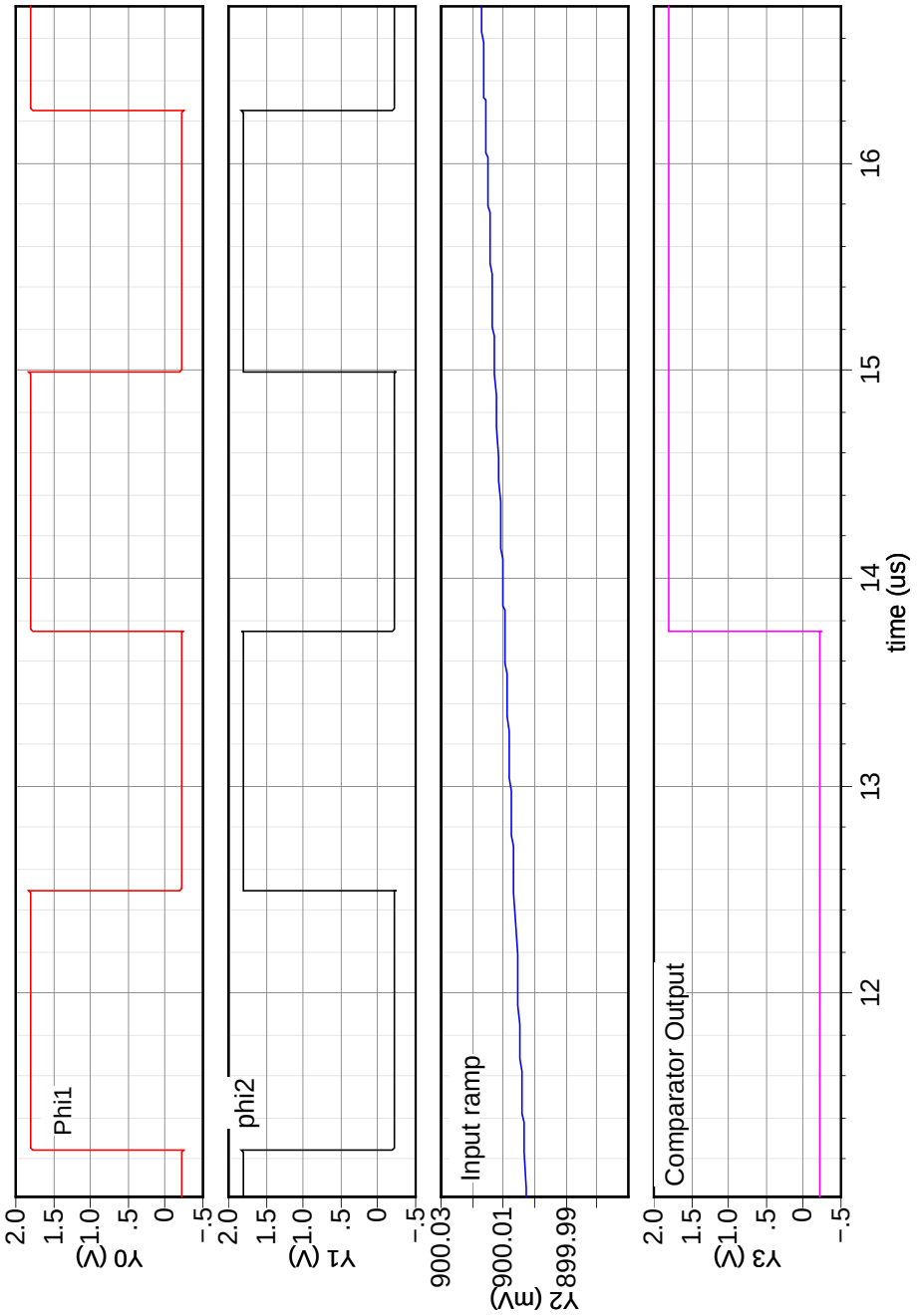

Figure 3.17: Comparator operation in r2rladder calibration mode

CHAPTER 4

Operational Amplifier - Design

Design of a three stage class AB operational amplifier is discussed in this chapter. Multi-stage architecture was chosen to obtain the high gain required for the I-V conversion of the R-2R ladder current source. Feed forward compensation technique is used for compensating the three stage amplifier. The design involves optimization of noise, power, distortion and bandwidth. The following sections discusses the above in detail.

4.1 Specification

Supply	1.8V $\pm 5\%$
Sample Rate	6.144MHz
Single-ended Output	1.5V P-P
Load	1kΩ & 100pF
Idle Channel Noise	5μV (20Hz-24kHz)
THD + N	-80dB
DC Offset	$\leq$ 5mV
Gain	$\geq$ 100dB

4.2 Design Considerations

4.2.1 First stage

The first stage was optimized for noise performance and gain. Since the gain of first stage is going to be very high ,noise contribution from remaining stages can be neglected.

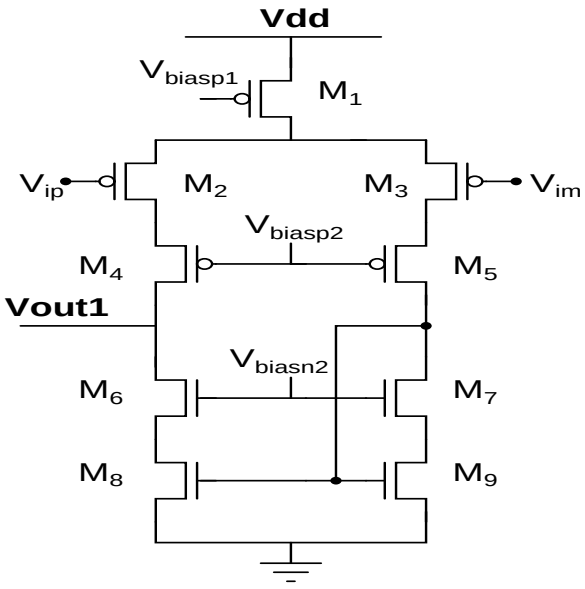

Figure 4.1: Noise analysis of single stage amplifier

At very low frequencies (20-20 kHz), the flicker noise contribution from MOSFET is maximum. Hence, this should be minimized.

The equivalent input voltage noise spectral density (only due to flicker noise) is

$$v_n^2 = 2v_{n2}^2(1 + (\frac{K_N^{'}B_N^{'}}{K_P^{'}B_P^{'}})(\frac{L_2}{L_8})^2) \tag{4.1}$$

$$\text{where } v_{n2}^2 = \frac{B}{fW_iL_i}$$

Since PMOS transistors have lower flicker noise coefficient (B_P) ,PMOS based input stage has been chosen. To minimize equivalent input noise , W_2L_2 (W_3L_3) has to be large. L_2 should be less than L_8 to remove influence of second term in brackets.

The equivalent input voltage noise spectral density (only due to thermal noise) is

$$v_n^2 = 2v_{n2}^2(1 + \frac{g_{m8}}{g_{m2}}(\frac{v_{n8}^2}{v_{n2}^2})) = 2v_{n2}^2(1 + \sqrt{\frac{K_NW_8L_2}{K_PW_2L_8}}) \tag{4.2}$$

$$\text{where } v_{n2}^2 = \frac{8KT}{3g_{mi}}$$

So the choices that reduce flicker noise also reduces thermal noise.Further noise can be reduced by degenerating load transistors.

4.2.2 Other stages

The second stage was implemented as a folded cascode opamp with a translinear output stage (3). A current mirror biasing scheme was followed to bias the folded cascode stage 4.4. Class AB output stage was chosen to minimize the quiescent power consumption. The ratio of peak current to the quiescent current controls the distortion. The following translinear stage was implemented for the output stage 4.2. For large overdrive of $M_{1(2)}$, $M_{3(4)}$ turns off and $M_{4(3)}$ acts as a cascode transistor. The cascode transistor serves to pin down the current flowing through the weakly conducting transistor $M_{2(1)}$ to a minimum value. But when above circuit 4.2 is used, because of difference in V_{ds} of bias transistors and output transistors current is not equally divided between M_3 and M_4. To take this into account the bias circuit of floating battery modified as shown in figure 4.5.The transistors

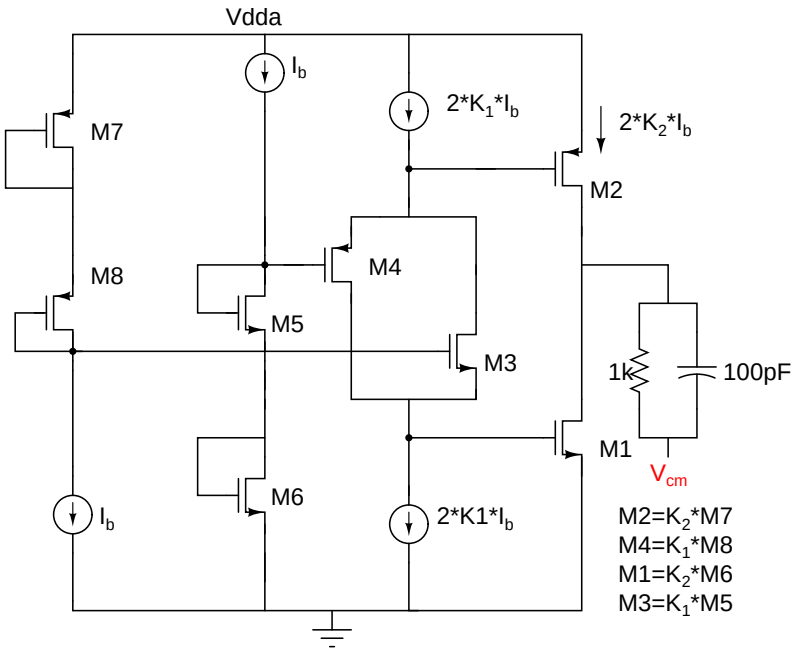

Figure 4.2: Monticelli Driver

that are replicated are highlighted in the figure.

4.2.3 Compensation scheme

Operational amplifier for same purpose is designed using miller compensation with nulling resistor architecture (1). However, the load capacitance of 100pF required compensation capacitors to be as large as 50pF which occupied a large area. So to reduce area feed forward compensation scheme is being opted. The principle of feed forward compensation scheme described in section 2.3. In amplifiers using feed forward compensation scheme there can be a substantial reduction in area, especially as compared to multistage amplifiers, which use two or more capacitors for phase compensation.

The compensation in final structure makes use of one feed forward path and miller compensation across final stage. Even though compensation using one feed forward path is sufficient under load of 1kΩ and 100pF, the varying load conditions requires phase to not vary over wide range of frequencies. So to make sure that amplifier is stable under all load conditions, miller compensation around last stage used. The final amplifier structure is shown in figure. The zero introduced by feed forward path depends on dominant pole of first stage and current through feed forward path. But increase in feed forward path current results in decrease in gain contributed by second stage because it will increase $\mathrm{g_{ds}}$ of load transistors of that stage.

To move zero introduced by feed forward path to lower frequencies, $\mathrm{g_m}$ has to be reduced but it is made high to meet noise constraints. The frequency of dominant pole in first stage is decided by parasitic capacitance at output node. To move that pole to low frequencies an external capacitance of 7pF is used at output of stage. If this dominant pole is moved to lower frequencies, the zero introduced by feed forward path also will move to lower frequencies (Eq 2.2). By using this external cap, the current requirement in feed forward path can be relaxed to some extent. The capacitance used is of MOSCAP so it doesn't occupy much area. The schematic of final opamp is shown in the figure 4.3 and the compensation used is highlighted in the figure.

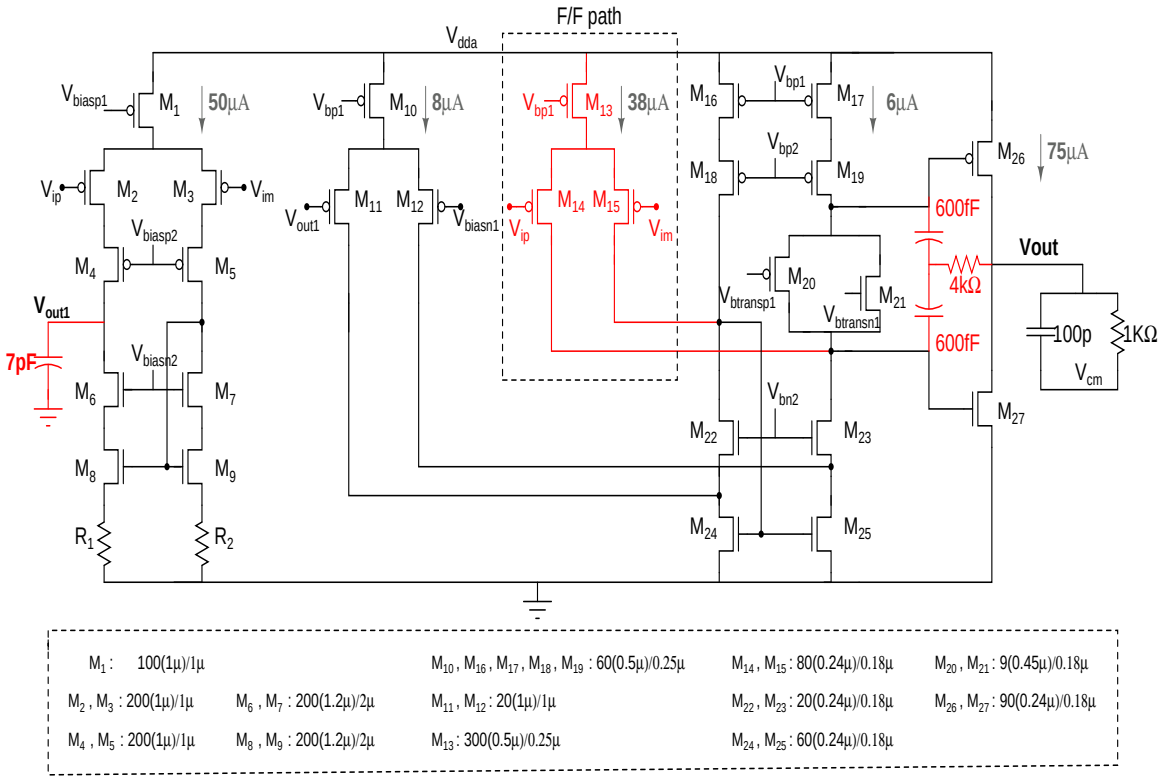

Figure 4.3: Opamp schematic

4.3 Simulation results

4.3.1 Frequency response

The frequency response of opamp for a load of 1kΩ and 100pF under nominal corner is shown in below figure.The variation of gain and phase margin with different loads under all corners are given in 5.

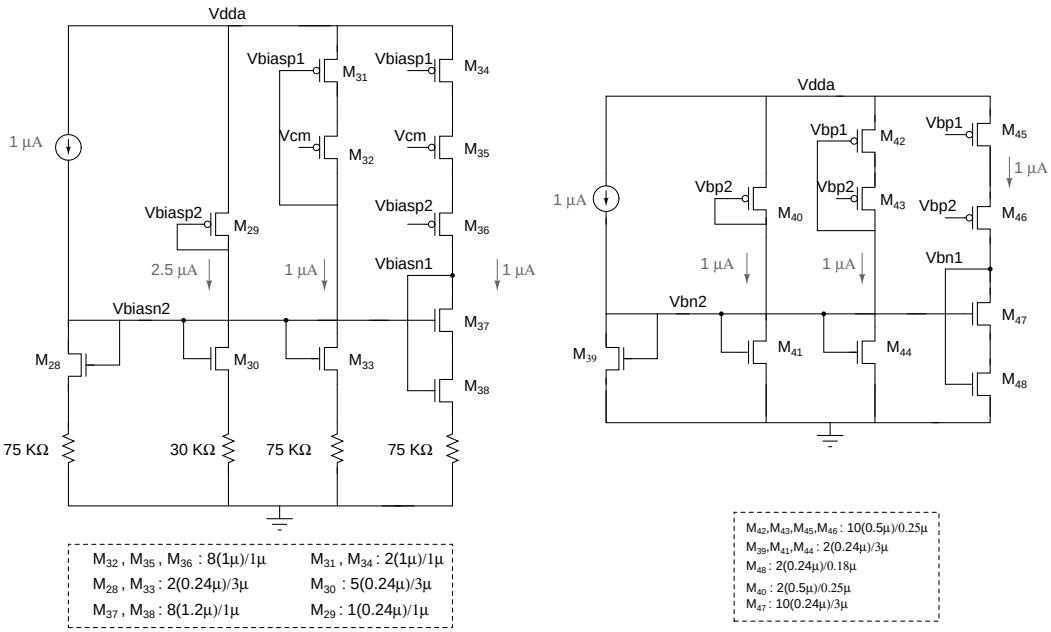

Figure 4.4: First and second stage bias circuits

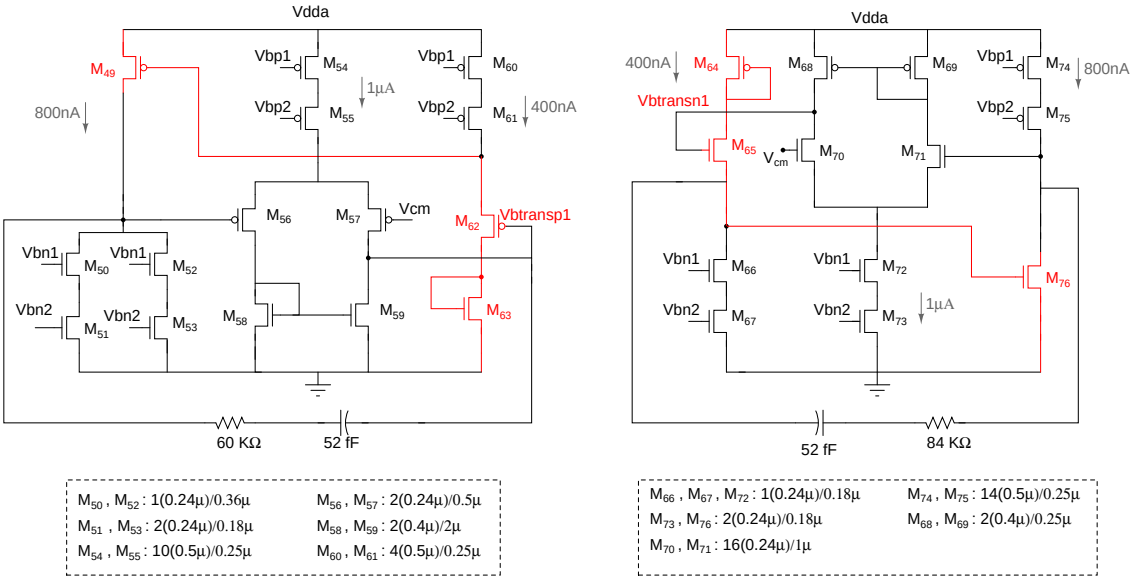

Figure 4.5: Bias circuit for class AB driver

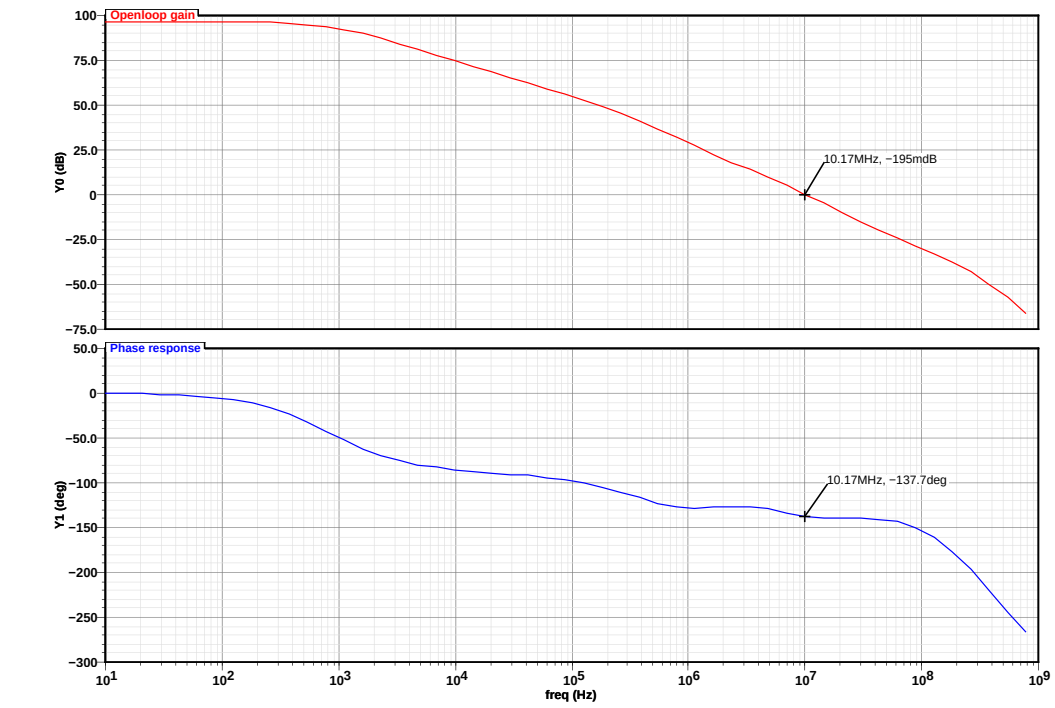

Figure 4.6: Frequency response of opamp

4.3.2 Distortion performance

The operational amplifier was connected in a inverting gain configuration with feedback resistors equal to the ladder resistance. A full swing sinusoid of 0.7 V peak at 1 kHz was given as input. The 64 point DFT of output for a load of 1kΩ and 100pF under nominal corner is shown in figure 4.7. The variation of THD under different load conditions tabulated in 5.

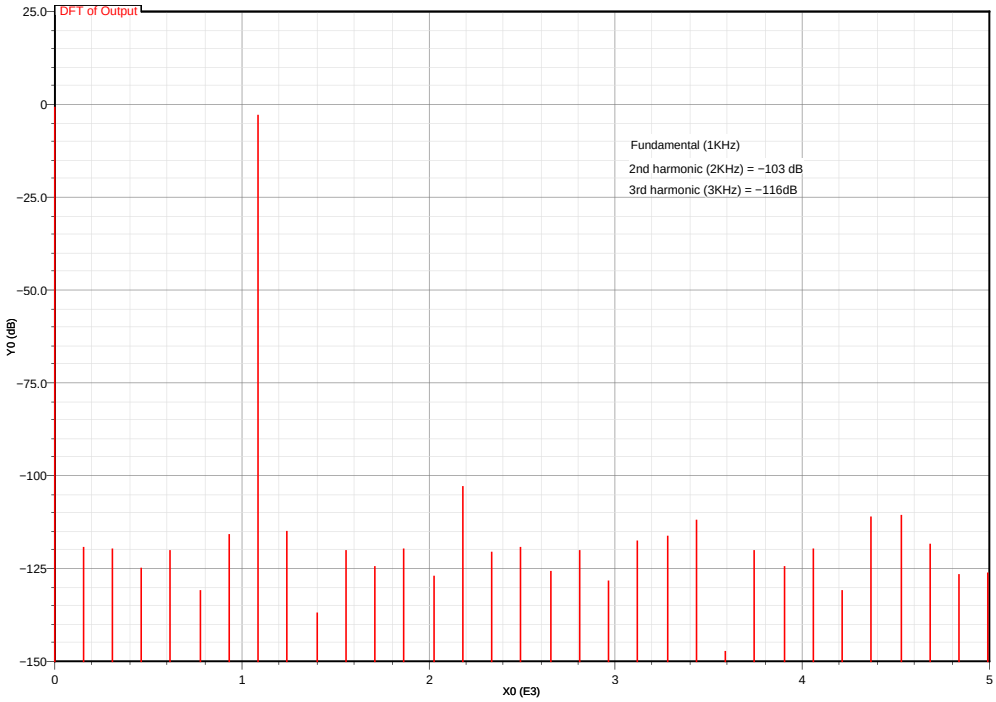

Figure 4.7: DFT of output of opamp

4.3.3 Noise results

Input referred noise is measured in inverting amplifier configuration with both input and feedback resistors of value 20K. At nominal corner with a resistive load of 1kΩ and capacitive load of 100pF, total RMS input referred noise (Integrated from 20Hz to 24kHz) of opamp 3.36μV. The noise due to feedback resistors is not considered in this case. The

contribution of input pair(51%) to total noise of first stage is dominant compared to load transistors(25%) and degeneration resistors(20%).

4.4 Layout considerations

The layout of cascode device can be simplified if the input device and cascode device have equal widths (12). The drain of M_1 and the source of M_2 can share same junction.More importantly, since this junction is not connected to any other node, it need not accommodate a contact window and can be therefore be quite small. Consequently the capacitance at the drain of M_1 is reduced substantially, improving high frequency performance. The layout of cascode devices present in first and second stage are done in this way and layout of bias circuit is also changed to take this into account.

There may be a significant routing resistance from the supply pins to the actual layout of the opamp in the chip. Wide metal lines (as much as area constraint allows) are used and multiple metal layers are augmented to minimize resistance.

4.5 Offset compensation

Effect of opamp offset on DAC performance is explained below. The simple architecture of R-2R DAC shown in figure 4.8 (4). In the figure, $\mathrm{R_{out}}$ is impedance of ladder seen from inverting terminal of opamp and Voff is input referred offset of opamp. $\mathrm{R_{out}}$ is input code dependent and it is "R" when all input bits are HIGH and it is ∞ when all input bits are LOW.

From above figure ,

$$V_{out} = \frac{R}{Rout}(V_{cm} + V_{off} - V_{ref}) + (V_{cm} + V_{ref}) \quad (4.3)$$

$$= V_{out}|_{V_{off}=0} + V_{off}(1 + \frac{R}{R_{out}}) \quad (4.4)$$

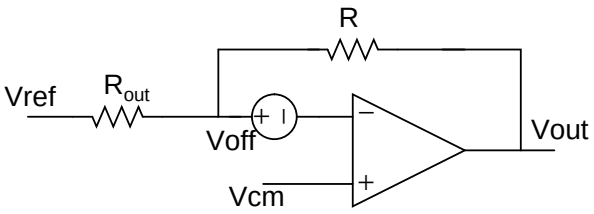

Figure 4.8: R-2R DAC modelling offset of opamp

So in R-2R DAC input referred offset of opamp will appear at the output with a multiplication factor which is nonlinearly dependent on input code. Since the gain of opamp is very high the systematic offset is not significant. The random offset is the one which matters. Because of high gain of first stage, random offset of remaining stages won't contribute much to input referred offset.

At nominal corner,input offset is calculated as follows.In following calculations,mismatch due to current factor (β) is not considered.

$$\begin{aligned}
\text{Offset because of } V_T \text{ mismatch between } M_2 - M_3,\ \sigma_1 &= \frac{A_{Vtp}}{\sqrt{WL}} + C_{p0} \\
&= \frac{4.68}{\sqrt{200}} + 0.189 \text{ mV} \\
&= 0.51 \text{ mV} \\
\text{Offset because of } V_T \text{ mismatch between } M_8 - M_9,\ \sigma_2 &= \left(\frac{g_{m8}}{g_{m2}}\right)\left(\frac{1}{1+g_{m8}R_1}\right)\left(\frac{A_{Vtn}}{\sqrt{WL}} + C_{n0}\right) \\
&= 0.339 \text{ mV} \\
\text{Offset because of mismatch between } R_1 - R_2,\ \sigma_3 &= \frac{I\left(\frac{g_{m8}}{g_{m2}}\right)\left(\frac{\Delta R}{R}\right)}{\frac{1}{R1} + g_{m8}\left(1+\frac{\Delta R}{R}\right)} \\
&= 0.354 \text{ mV} \\
\text{Overall I/p referred offset},\ \sigma &= \sqrt{\sigma_1^2 + \sigma_2^2 + \sigma_3^2} \\
&= 0.707 \text{ mV}
\end{aligned}$$

Depending on process variations,above value can be as high as 0.8 mV. In worst case depending on input code, a voltage of 0 V to 1.6 mV can appear at output because of opamp

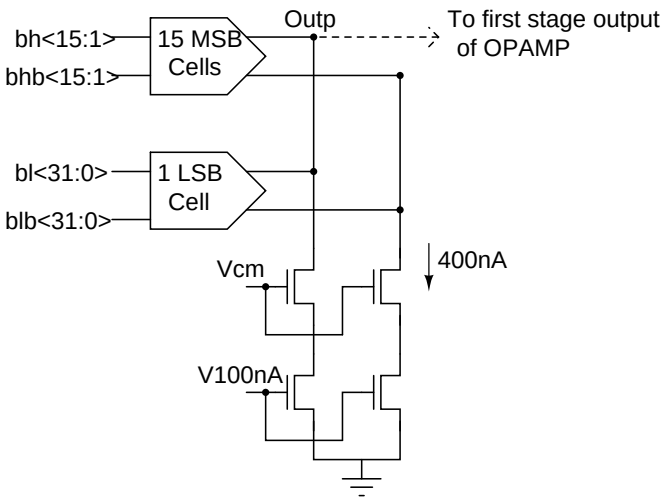

Figure 4.9: Compensating offset of opamp

offset. This can give upto 70 LSBs of INL for highest input code. So opamp offset has to be compensated for proper operation of DAC. More over the value stated above represents only magnitude. It can be of either sign in practice. If offset is positive (negative),current will be pumped(sucked) into(out of) the output of first stage of opamp using DAC shown in figure 4.9. During calibration of opamp, the R-2R ladders are disconnected and the exact value of current needed will be decided with help of comparator and digital calibration block.

It has been observed that the current required for compensating 0.707mV is around 330nA. For calibrating purpose a 4-bit current steering DAC (thermometer based)is used.The last bit is segmented into 5 bit DAC(Also thermo meter based). The LSB of DAC is 50nA.So full scale current of DAC is 800nA. The common mode current sources will sink 400nA always.Depending on input bits calibration DAC can source or sink 400nA current. With this maximum amount of current calibration DAC can compensate offset upto 0.84mV. The MSB and LSB cells that are used shown in the figure 4.10. The bias circuit used is shown in the figure 4.11.

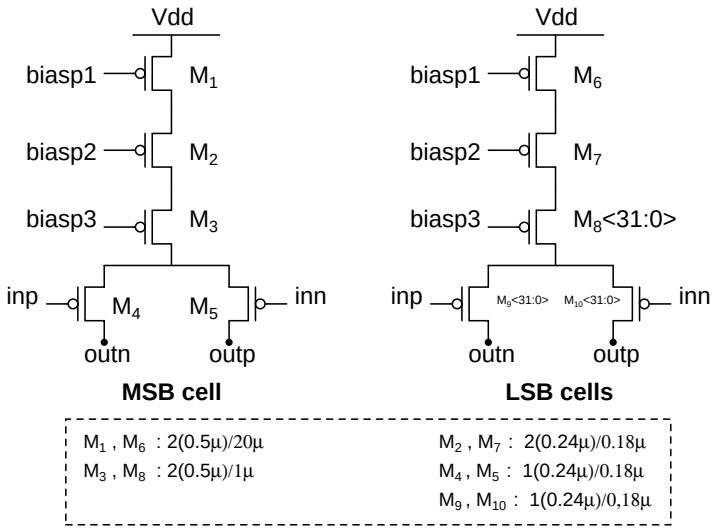

Figure 4.10: MSB and LSB cells of calibrating DAC

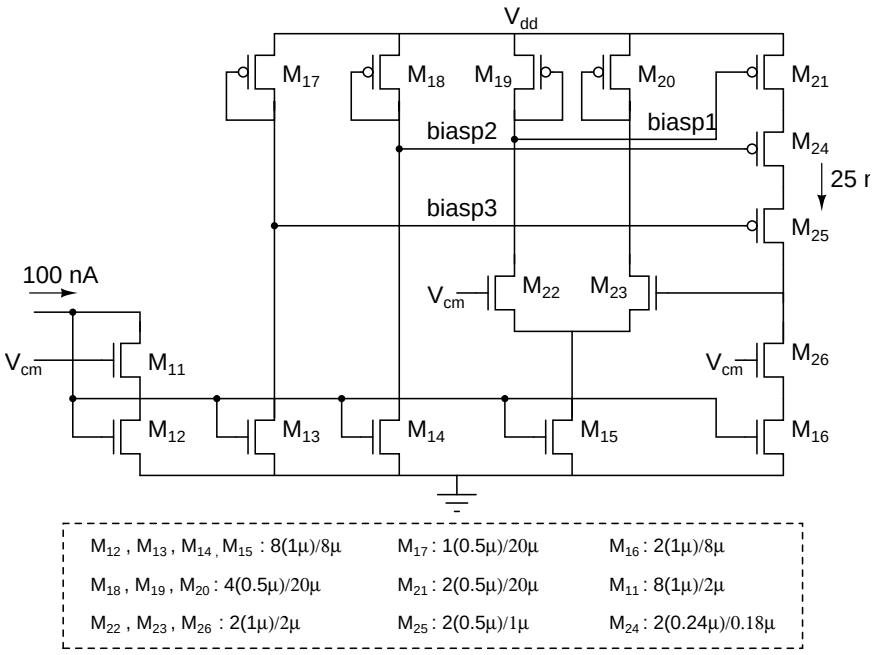

Figure 4.11: Bias circuit for calibrating DAC

CHAPTER 5

Simulation and Layout results

5.1 Opamp results

The three stage class AB stage operational amplifier was laid out in UMC 0.18μm, 6 metal poly technology. The opamp performance should be good for wide range of loads (The capacitive load can vary from 100pF to 1pF and resistive load can vary from 1kΩ to 100kΩ). The extracted RC netlist was simulated for process and load variations.

5.1.1 DC gain and Phase margin

The variation of DC gain and phase margin over all process and load conditions are tabulated below 5.1.

5.1.2 Area and Power

The feed forward based opamp is using two 600fF capacitors around last stage and another two 50fF capacitors in bias circuits for compensation purpose. Area occupied by this opamp is around 21336 μm^2 (168μm X 127μm). The area occupied by opamp compensated using nested miller compensation with nulling resistor is around 71461 μm^2(239μm X 299μm) (1). The area is reduced by 70% which is a clear advantage gained by using feed forward compensation.

Under nominal conditions the current consumed by opamp is around 200 μA. In this 50 μA is used by first stage, 75 μA is used by output stage and 38 μA is used by feed forward

Load Resistance	Load Capacitance	Gain @ Nominal corner	PM @ Nominal corner	Gain @ Worst case	PM @ Worst case
1 kΩ	100 pF	95.14 dB	45.6^0	82.48 dB	37.5^0
10 kΩ	100 pF	107.8 dB	38.89^0	95.7 dB	30.2^0
100 kΩ	100 pF	112 dB	38.19^0	99.57 dB	29.83^0
1 kΩ	10 pF	95.14 dB	95.31^0	82.48 dB	82.87^0
10 kΩ	10 pF	107.8 dB	82.55^0	95.7 dB	69.43^0
100 kΩ	10 pF	112 dB	81^0	99.57 dB	67.74^0
1 kΩ	1 pF	95.14 dB	128^0	82.48 dB	87.08^0
10 kΩ	1 pF	107.8 dB	76.8^0	95.7 dB	39.09^0
100 kΩ	1 pF	112 dB	68.41^0	99.57 dB	35.39^0

Table 5.1: Gain and Phase margin of opamp over process and load corners

stage. The power consumption at nominal corner is around 360 μW. The first stage current should be high so as to meet noise requirements. Bias currents should not be reduced further because it can result in large current variation if mismatch is taken into account.

5.1.3 Distortion results

The variation of THD over process and load variations are tabulated below 5.2.

Load Resistance	Distortion @ Nominal corner	Distortion @ Worst case
1KΩ	-99.38 dB	-95.35 dB
10KΩ	-111.1 dB	-105.8 dB
100kΩ	-116.2 dB	-111 dB

Table 5.2: THD of opamp over process and load corners

5.2 DAC results

5.2.1 Distortion performance

The distortion performance summary of DAC in different modes are given below. In both cases the output has a swing of 1.5 V p-p. At the output of DAC an ideal 8th order Butterworth filter of cutoff frequency 100kHz has been used. An error current of 20nA has been introduced in first eight branches of both ladders and calibration DACs are turned ON to compensate for that error. In both cases input is of same frequency(Number of points in DFT are different).

OSR	No of DFT points	Mode of Operation	2nd harmonic	THD
128	4096	Switching in middle	-92.8dB	-84dB
128	4096	Complementary switching	-89.2dB	-82dB
8	256	Switching in middle	-81dB	-77dB
8	256	Complementary switching	-93.2dB	-86dB

Table 5.3: THD of filtered DAC output

5.2.2 Area Occupied

Area occupied by entire DAC 1050 μm x 1094 μm. Percentage of areas occupied by different blocks in final R-2R DAC is given below 5.4.

5.2.3 Power Consumption

Power consumed by different blocks in R-2R DAC is tabulated below 5.5.

Block	Percentage of area occupied
Digital blocks	22
Total calibration DACs including binary to thermo converters	21
OPAMP + R-2R ladder + Level shifters	6.5
HV generator	5
Comparator including clock generation circuit	2.6

Table 5.4: Areas occupied by different blocks in DAC

Block	Power Consumption
OPAMP	360μW
Comparator	146.7μW
ladder Calibration DACs OPAMP offset calibration DAC	23μW
Digital calibration engine (Dynamic power)	25μW

Table 5.5: Power consumed by different blocks in DAC

5.2.4 Noise

Idle channel noise at output of DAC 3.3μV_{RMS} in switching in middle mode and 6 μV_{RMS} in complementary switching mode.

5.3 Complete layout of R-2R DAC

The complete layout of R-2R DAC including digital blocks and bond pads are shown here 5.1.

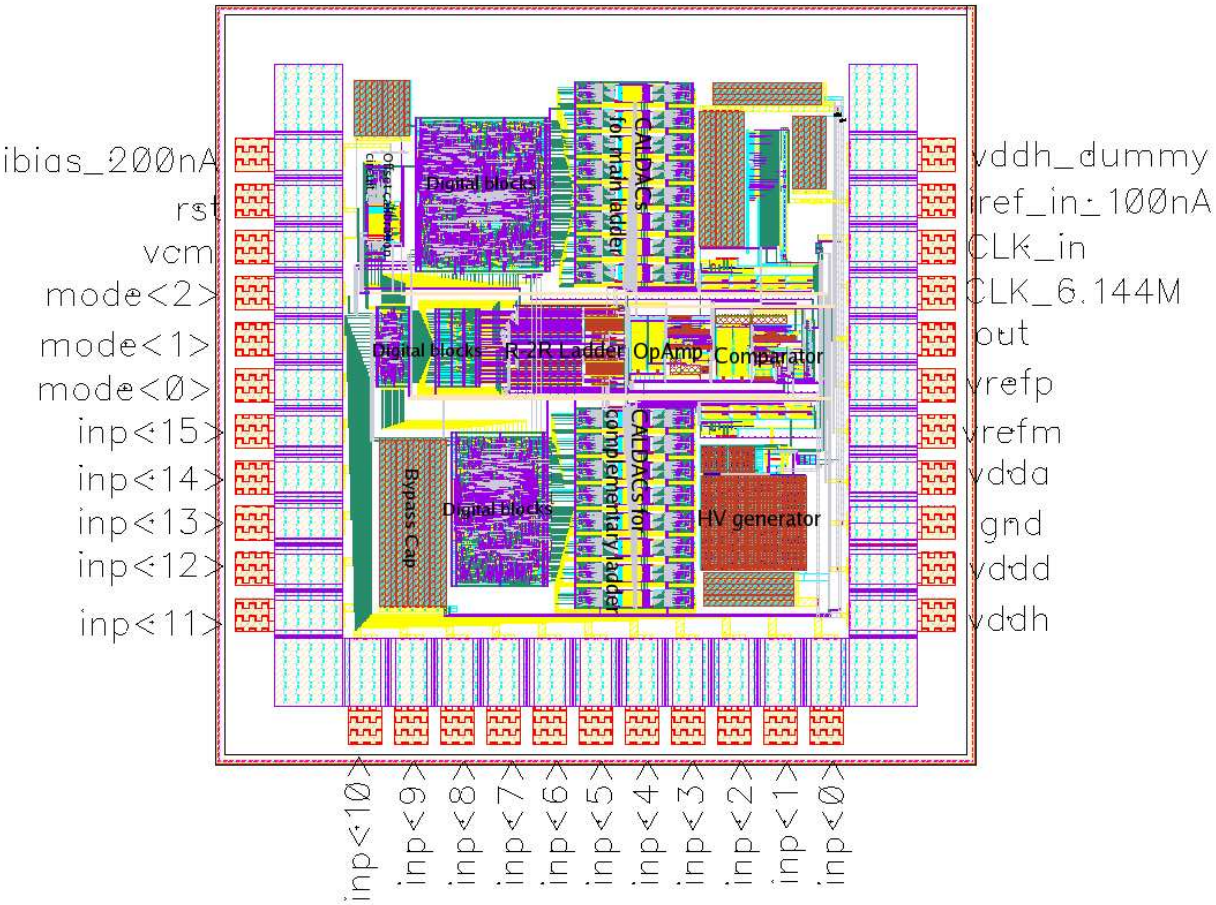

Figure 5.1: Complete layout of 16 bit R-2R DAC

CHAPTER 6

Future scope

The calibration scheme only compensates for mismatch in a ladder. There can be mismatch between two ladders i.e., LSB of two ladders can be quite different. This can be a problem in switching in middle mode where in each half cycle only one ladder operates. So the calibration should take care of mismatch between two ladders also.

The non overlapping block (which is a digital block) generates complementary non overlapping waveforms of voltage swing from 0 V to 1.8 V. These clocks have to be converted to 0 to 2.7 V waveforms. For that purpose two level shifters, one for normal output and another for complementary output is used. If level shifter can generate non overlapping waveforms, number of level shifters can be reduced by a factor of 2.

The comparator and digital blocks will run at a clock frequency of 384kHz. The input frequency is multiplexed with 384kHz so that during normal operation DAC works with input frequency. But the HV generator needs a clock of 6.144MHz. So in current design, if it is desired to test with a OSR other than 128, 2.7 V has to be supplied externally.

Since the calibration is one time process in this design, the comparator works only during calibration time for calibrating R-2R ladder and calibrating offset of opamp. Once calibration process is over, the comparator is no more used. But still it dissipates power. If comparator can be turned off after calibration process is over, the power dissipation in comparator (about 147 μW) can be saved.

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