Calibration Circuit for a 16-bit R-2R Digital to Analog Converter

A Project Report

submitted by

SUKUMAR BANDI

in partial fulfilment of the requirements
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MASTER OF TECHNOLOGY
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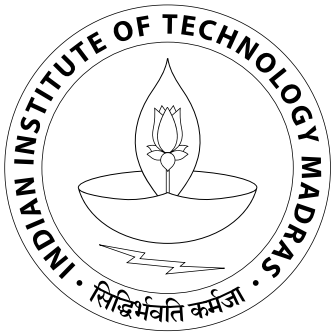

DEPARTMENT OF ELECTRICAL ENGINEERING
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CERTIFICATE

This is to certify that the thesis titled **Calibration Circuit for a 16-bit R2R Digital to Analog Converter**, submitted by **Sukumar Bandi**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Research Guide
Assistant Professor
Dept. of Electrical Engineering
IIT-Madras, 600036

Place: Chennai
Date: 22nd June 2009

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ABSTRACT

R2R Ladder structures are simplest of Digital to Analog Converters (DACs) having no complex feed back loops or requiring large area. Though R2R ladders are simple to design and debug, these structures cannot be used for high resolutions. Resistors made in CMOS technology suffer from very high mismatch, mismatch being as high as 1%. Such high mismatch introduces a lot of non linearity. With simple calibration the R2R ladders can be used for high resolution also. A 16-Bit ladder has been used here with first 8 most significant branches calibrated. And two such ladders are used here to get double the output swing. The calibration is done digitally with a 10 bit current steering DAC supplying the correction current. There are sixteen such 10 bit DACs each for the branch calibrated. All these DACs are controlled by a digital calibration block.

The output of the DAC is driven though a Current to Voltage (I-to-V) converter. The offset in this converter introduces huge non linearity in the DAC degrading the performance. Unless this is corrected, calibration effect is mitigated. OpAmp offset correction can be done by supplying the sufficient correction current. This can also be done using digital control of the correction current supplied by a current steering DAC.

The advantage of using digital control is that the present DAC can used in different modes. The input to the DAC can be used to switch DAC in different ways. One such way is 'switching in the middle'. This eliminates the noise generated from part of the reference generator. This is because only one of the two ladders is switched on for any given input digital code. The choice of selecting the method of switching and the modes of calibration are included in the digital control block.

Single digital control block, with all these functionalities, occupies a huge area. Also 16 10-bit DACs requiring control from this block, the routing of the wires is

highly complex. This single digital control block is divided into different blocks to reduce complexity of the routing the wires and reduce the power and area of the total blocks.

TABLE OF CONTENTS

LIST OF FIGURES

ABBREVIATIONS

DAC	Digital to Ananlog Converter
ADC	Analog to Digital Converter
I-to-V	Current to Voltage
LSB	Least Significant Bit
MSB	Most Significant Bit
INL	Integral Non-Linearity
DNL	Dynamic Non-Linearity
ENOB	Effective Number Of Bits

CHAPTER 1

Introduction

1.1 DACs

Processing, transmitting and storing the data in digital form is easy and better than the analog form. But physical signals are essentially analog in form. This requires the basic conversion of the real signals from Analog to Digital form to be processed, transmitted or stored in the digital form. This is done by Analog to Digital Converters (ADCs). To be able to use the processed data in the real world domain we need the Digital to Analog Converters (DACs). For instance, digital audio players (say, mp3 players) need DACs to give the audio output through the speakers or the head phones. The precision or the resolution of the DAC defines the quality of the sound heard. Hence high resolution DACs are essential to be able to utilize the well processed digital data. Let the Digital input given to the N-bit DAC be $b_{N-1}, b_{N-2}, b_{N-3}...b_1, b_0$. According to the convention used here b_{N-1} is MSB and b_0 is LSB. The analog equivalent output then is

$$v_{out} = \sum_{i=0}^{N-1} b_i * 2^i * V_{ref} \tag{1.1}$$

V_{ref} is the resolution or the precision of the DAC. The details of the resolution for the DAC used here are in chapter 5

1.2 Types of DACs

DACs can be Nyquist rate DACs or the Oversampled DACs.

1.2.1 Nyquist Rate DACs

Nyquist rate DACs are characterized by the incoming data rate. Here the data rate is just more than twice the input bandwidth. Nyquist rate DACs are essentially used where the input bandwidth is high.

Binary Weighed DACs

Output of a Binary weighed DAC is given by equation 1.1. These are simple systems with very few components. Binary DACs can be current output or the voltage output DACs. With capacitor ladders even charge sharing DACs can be formed [1]. Current output DACs are either R2R ladders structures or the Binary weighed current steering DACs as shown in figures 1.1 and 1.2. The output current is added based on the no. of switches on.

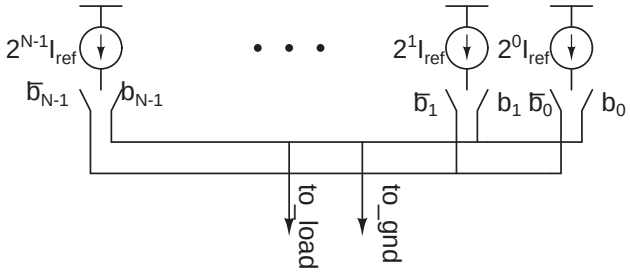

Figure 1.1: Binary Weighed Current Steering DAC

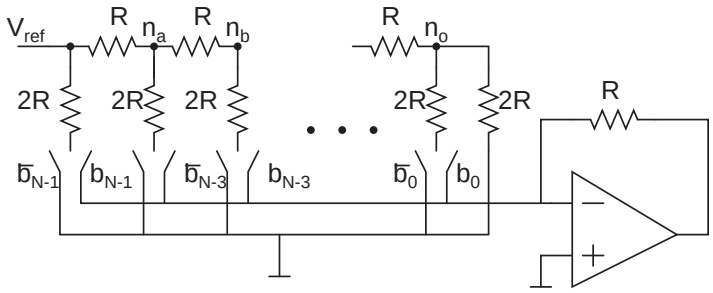

Figure 1.2: R-2R Ladder Structure

Node voltage n_a in figure 1.2 is $\frac{V_{ref}}{2}$ and n_b is $\frac{V_{ref}}{4}$. Current is steered either to the load or to the ground is binary weighted fraction of the V_{ref} and the resistance used. Binary weighed DACs suffer from the major code transition DNL for high resolution DACs as explained in Appendix A. R2R ladder structures are simplest

of all the DAC designs. But realizing resistors in CMOS technology comes with inherent mismatch and parasitics. For higher resolutions it is not possible to realize a linear DAC using resistor ladders. But with calibration as mentioned in this thesis can give a fairly good linearity to the R-2R ladder DAC. Calibration method used here is explained in chapter 3.

Thermometer Coded DACs

The output of a thermometer coded DAC is given by

$$v_{out} = \sum_{i=1}^{M} i * V_{ref} \tag{1.2}$$

v_{ref} is the resolution or the LSB of the DAC. M is the total number of the sources each with a weight of V_{ref}. Here the sources are identical as shown in the figure 1.3. For higher number of bits these structures are complex as the input binary code

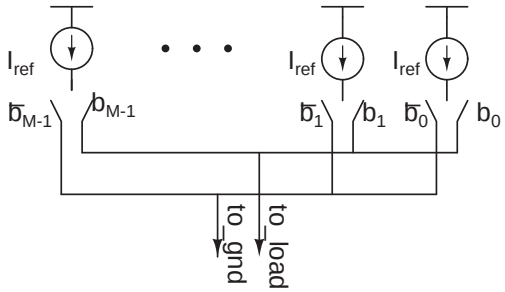

Figure 1.3: Thermometer Coded DAC

needs to be converted to its equivalent thermometer code before being fed to the DAC. This conversion occupies space exponentially as the resolution increases. But the thermometer coded DACs have the DNL advantage over the the binary coded DACs as explained in Appendix A.

Binary and Thermometer code Segmented DACs

The binary and thermometer code segmented DACs have lesser non linearity than the binary DACs and lesser complexity than the thermometer coded DACs. These are more complex than the binary DACs and more non linear than the thermometer coded DACs.

1.2.2 Oversampled DACs

Oversampled converters use sampling periods much higher than the Nyquist rate of the input signal. By pushing the signal frequencies far away from the signal band, by oversampling, reduces the constraint on the analog filter that follows the DAC. Also the oversampled converters employ noise shaping techniques by the use of closed loop structures. Noise shaping pushes the quantization noise away from the signal band. This will essentially improves the SNR in the band of interest. Especially when the input bandwidth is small the oversampling converters are very useful. Since the ENOB of a oversampled and noise shaped converter increases, one can use components with much less matching. Over sampled DACs up convert the signal so as to over sample the data. The images produced this way are filtered prior to noise shaping. Feedback in these systems can make the system unstable. The feed back, the filtering and the quantization make these systems complex [2].

This thesis discusses the 16-bit R2R with complementary ladder so as to double the output swing. The main motive of using R-2R DAC is that it has no flicker noise. The complementary ladder also enables the DAC to be used in both complementary input mode and the switching in the middle mode as discussed in chapter 3.

1.3 Digital Calibration and Control

Figure 1.4 shows the complete DAC with calibration control. Digital calibration DAC is also used to operate DAC in various modes as explained in chapter 3. There are separate digital blocks to control the calibration of the two ladders. One control block also contains control for the offset cancellation of the OpAmp. In all these calibration mechanisms the comparator plays a major role. The current steering DAC used to supply the correction current is explained in chapter 2. Chapter 3 gives the complete description of the digital blocks used. The comparator is discussed in chapter 4.

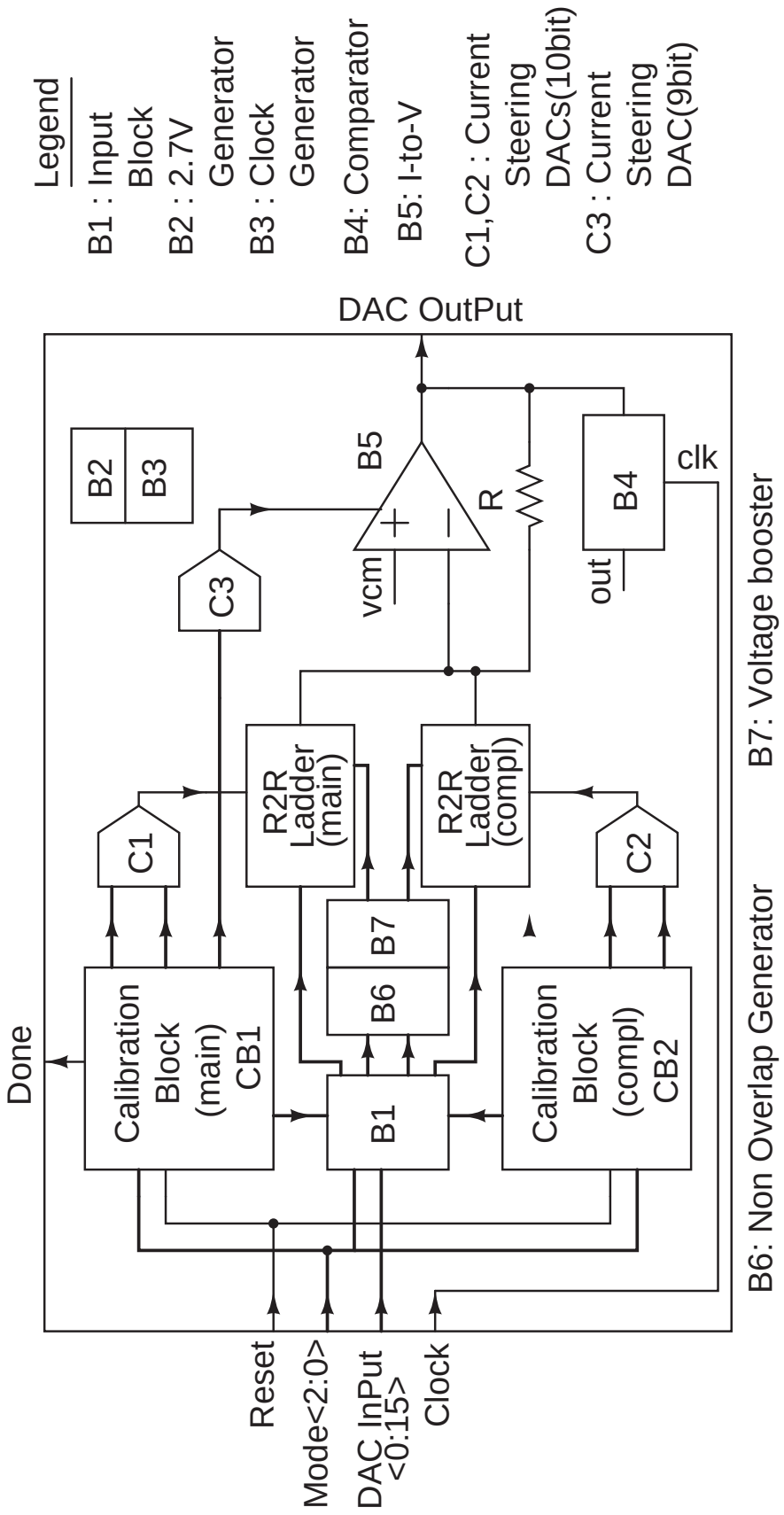

Figure 1.4: 16-Bit R2R DAC with Digital Calibration

CHAPTER 2

R2R Ladder and Digital Calibration

2.1 Introduction

R2R Ladders are simplest of DAC structures. For frequency range in the audio band, 20Hz to 20KHz, these DACs introduce no flicker noise unlike the DACs implemented using MOS transistors. Figure 2.1 shows a resistor ladder with 16 branches. For a ladder with 4 branches (as shown in figure 2.2) the node voltages can be calculated as

$$v_{n1} = \frac{V_{ref}}{R_1||R_{A1}} \frac{R_{A1}}{R_1 + R_{A1}} R_2||R_{A2} \tag{2.1}$$

$$v_{n2} = \frac{v_{n1}}{R_2||R_{A2}} \frac{R_{A2}}{R_2 + R_{A2}} R_3||R_{A3} \tag{2.2}$$

$$v_{n3} = \frac{v_{n2}}{R_3||R_{A3}} \frac{R_{A3}}{R_3 + R_{A3}} R_{A4}||R_{A5} \tag{2.3}$$

where

$$R_1 = (R_{A5}||R_{A4}) + R_{B3}$$

$$R_2 = (R_3||R_{A3}) + R_{B2}$$

$$R_3 = (R_2||R_{A2}) + R_{B1}$$

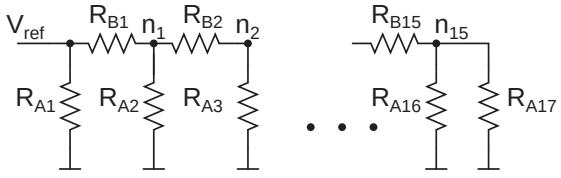

Figure 2.1: Resistor Ladder 16 branches

For all $R_B = R$ and $R_A = 2R$, $R_1 = R_2 = R_3 = 2R$ and $v_{n1} = \frac{V_{ref}}{2}$, $v_{n2} = \frac{V_{n1}}{2} = \frac{V_{ref}}{4}$ etc. Hence, shown in figure 1.2, for a perfect R-2R ladder all the nodes

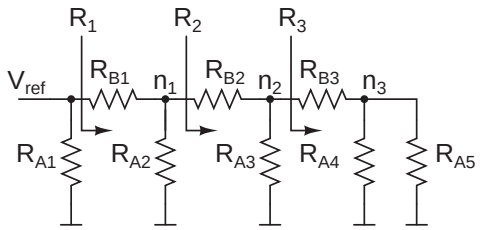

Figure 2.2: Resistor Ladder 4 branches

are binary weighed. The current from any node to the output or the ground is also binary weighed. R-2R ladder when used as DAC, these binary weighed currents, thus, are switched to the output according to the digital input. The various ways of making resistors in CMOS technology are mentioned previously. As mentioned in the Appendix B, high valued resistors are RNHR, Non-salicide High Resistance, type.

The variations in the resistor values can high as 20% in the resistor values over process and temperature. To see the mismatch effect on 16-bit DAC, random mismatch simulations are done in the previous works. For 1% variance in the resistors used the INL can be as high as 35 LSBs. This degrades the performance of the DAC as a linear unit, which requires the INL to be within 0.5 LSBs.

2.2 External Calibration

Since, for an ideal R2R DAC, the current entering any node n_r (figure 2.2) divides equally between the two branches, the two branch currents can be compared for any discrepancies in the branch currents and the required current can be added externally to compensate the exact discrepancy. This is the idea behind the external calibration. In the first place the output due to the main branch is measured (V_{out1} in the figure 2.3). This is compared to the other equal current by switching ON all the branches which have got lesser weightage. Switching ON all the lower branches would still add up to an LSB lesser current. This is compensated by using the reminiscent branch current I_t as shown in the figure. The resulting output (V_{out2} in the figure 2.4) is compared to V_{out1}.

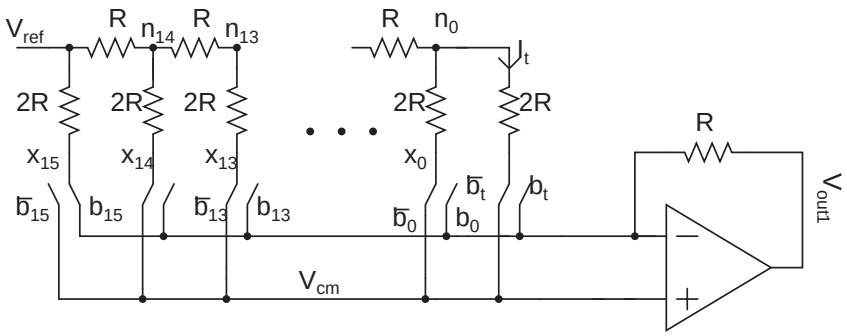

Figure 2.3: Main vertical branch ON

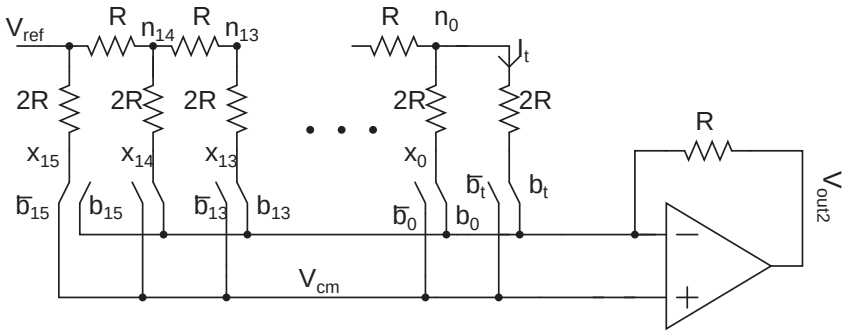

Figure 2.4: All lower branches ON

Depending on the compared output the required current is either sourced or sinked in the node x_r. For instance, if $V_{out1} > V_{out2}$ the current needs to be sourced into the node x_r in order to make the current from the main branch equal to the other reference current. To obtain the accuracy of 1 lsb in the INL, the correction current sourced or sinked needs to make the branch current equal to the reference current upto 1 lsb accuracy.

2.2.1 External calibration current sources

To supply the external required current, 10 bit current steering DACs are employed. This would correct the discrepancy upto 512 lsbs both ways. To reduce the INL and DNL in the current steering DAC, 5 bit thermometer coded and 5 bit binary segmentation is used. 5 bit binary coded DAC is realized in the thermometer coded fashion to reduce the major code transition DNL. Hence there are 31 current sources each with 32 lsb (lsb of the 16 bit R2R dac) current and 32

current sources with each equal to 1 LSB current.

The topology of the two current sources is shown in the figure 2.5 below. The table 2.1 gives the sizes of the individual transistors. The current steering transistors (M_s and M_{sb})are minimum size. The current source is sized to so as to restrict the random mismatch, between any two current sources, to 1 LSB.

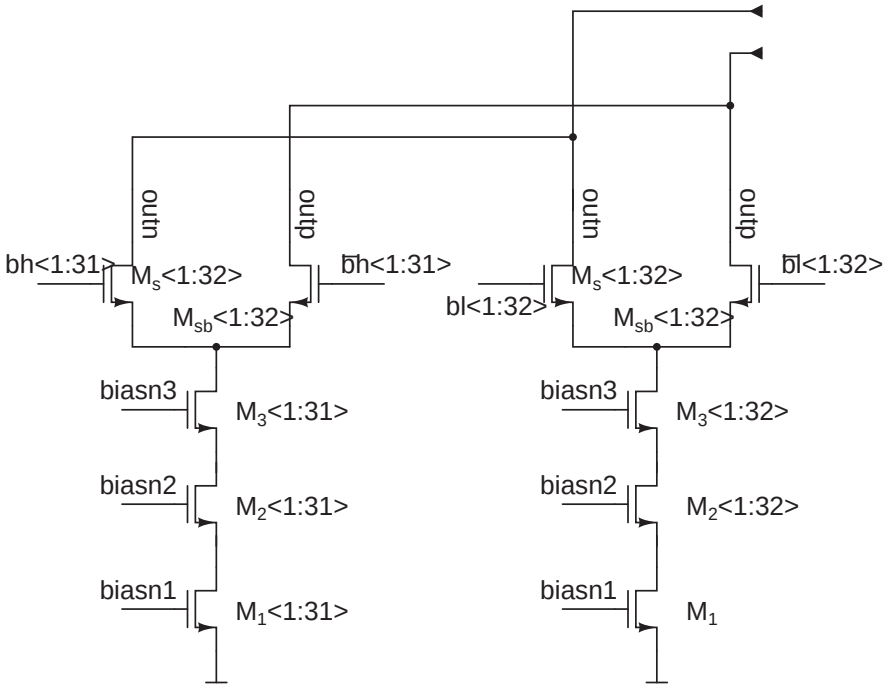

Figure 2.5: Current sources topology

	M_1	M_2	M_3	M_s	M_{sb}
W	500n	500n	500n	240n	240n
L	20μ	500n	500n	180n	180n
nf	2	2	2	1	1

Table 2.1: Sizes of the Current Steering DAC

Any current source can be modeled with a current value centered around the, supposed, nominal value and varies both ways randomly. For most of the cases, this radom variation can be modeled by a gaussian distribution in which case the current value is centered around nominal value, I, but the actual value can be any where in the range of I+3σ_I and I-3σ_I. σ_I, is the standard deviation of the current source. The DNL caused due to the switching ON a current source, $I_A = N(I, \sigma_I)$,

and switching off another current source, $I_B = N(I, \sigma_I)$, is $\sqrt{2}\sigma_I$ as explained in the appendixA

The current mismatch between two current sources is the cumulative effect of the threshold mismatch and the current factor mismatch. The threshold mismatch between two transistors with size W and L is given by $\sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}}$. And the current factor mismatch is given by $\sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$. Usually it is the threshold mismatch that contributes to the maximum of the current mismatch. Both A_{VT} and A_β are technology dependent. In the technology used here the mismatch values are given by, for NMOS transistor,

$$\begin{aligned} \sigma_{VT} &= \frac{A_{VT}}{\sqrt{WL}} + k \\ &= \frac{4.2E-03}{\sqrt{WL}} + 0.45E-03 \quad V \end{aligned}$$

for PMOS transistor,

$$\begin{aligned} \sigma_{VT} &= \frac{A_{VT}}{\sqrt{WL}} + k \\ &= \frac{4.68E-03}{\sqrt{WL}} + 0.19E-03 \quad V \end{aligned}$$

Where as the current mismatch due to the current factor (in % terms) is given by, for NMOS,

$$\begin{aligned} \sigma_{I_D} &= \frac{I_D}{\sqrt{WL}} \quad \% \\ &= \frac{3.1}{\sqrt{WL}} \quad \% \end{aligned}$$

for PMOS,

$$\begin{aligned} \sigma_{I_D} &= \frac{I_D}{(WL)^{.405}} \quad \% \\ &= \frac{2.8}{(WL)^{.405}} \quad \% \end{aligned}$$

With the sizes used, as mentioned, in the the table 2.1 random mismatch sim-

ulations are done for over 100 cases. The histogram of the INL obtained is given in the figure 2.6. When the sizes are modified to $W = 2 * 250n$ and $L = 10\mu$ the

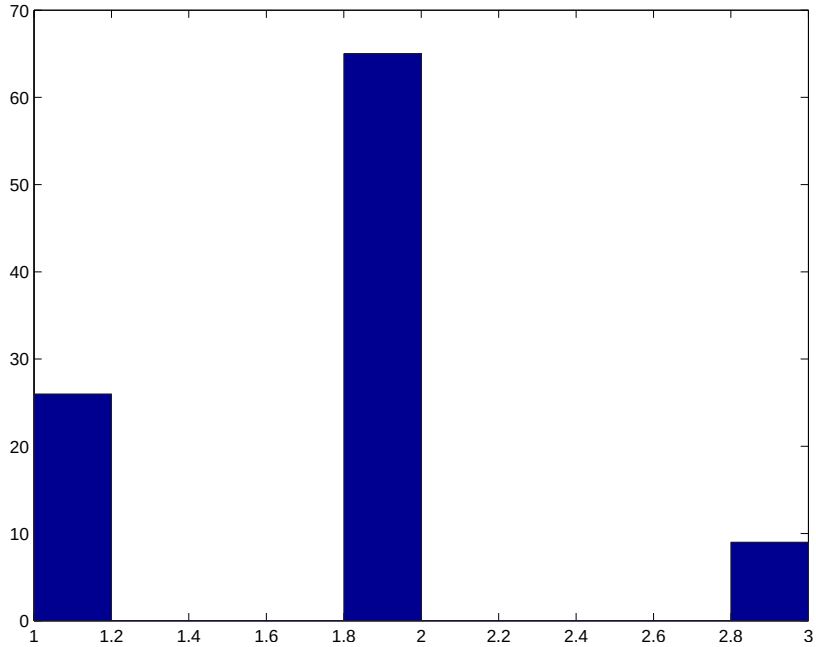

Figure 2.6: INL $W = 2 * .5\mu \quad L = 20\mu$

INL variation was distributed between 2 and 4 LSBs as seen in the figure 2.8

2.2.2 Calibration Control

Once the external calibration current source values are in the required premises as per the mismatch is concerned, the sourcing or sinking is done by adding a constant current source of the appropriate value, as per the swing required, as shown in the figure 2.10 and the sizes are same as in table 2.1. The current sources ,I_A and I_B, are equal to 512 LSBs. Each LSB current source is formed by dividing the "high-current" source (or the MSB current source) into 31 sources as shown. The 10-bit binary digital input is first converted into its equivalent thermometer code using the b2t blocks as shown. With all these bottom current sources swinging from 0 to 1023 LSBs, the out put current swings from -511 LSBs to 512 LSBs. The top constant current sources are realized using PMOS transistors to source the current.

As mentioned in the previous section, the current sourcing or sinking can now be

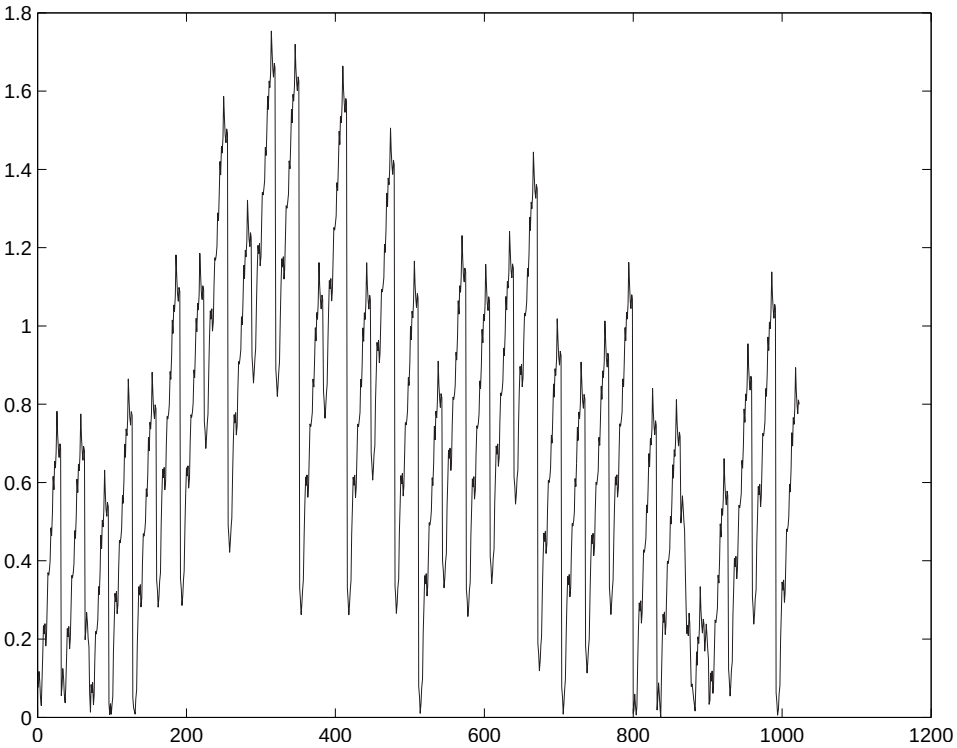

Figure 2.7: INL $W = 2 * .5\mu \quad L = 20\mu$

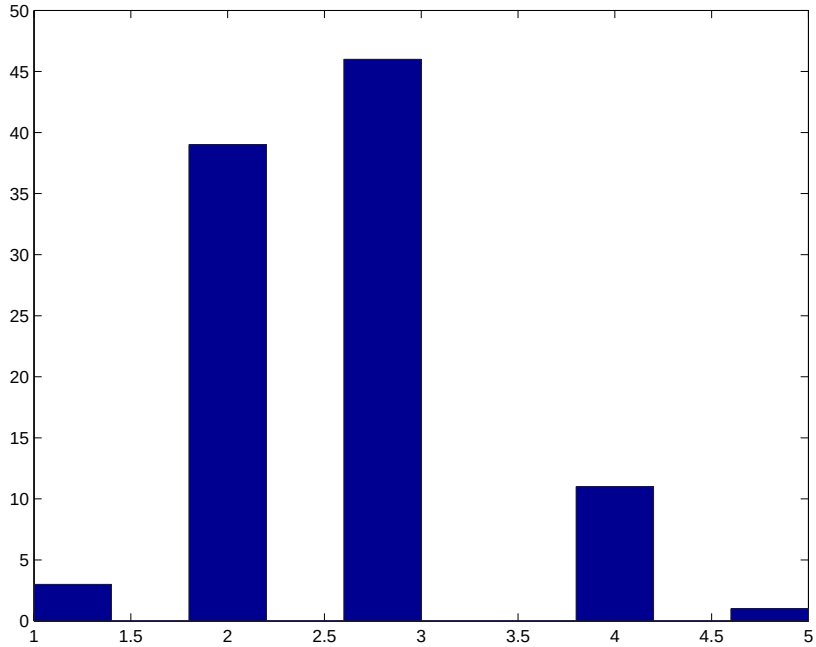

Figure 2.8: INL $W = 2 * .25\mu \quad L = 10\mu$

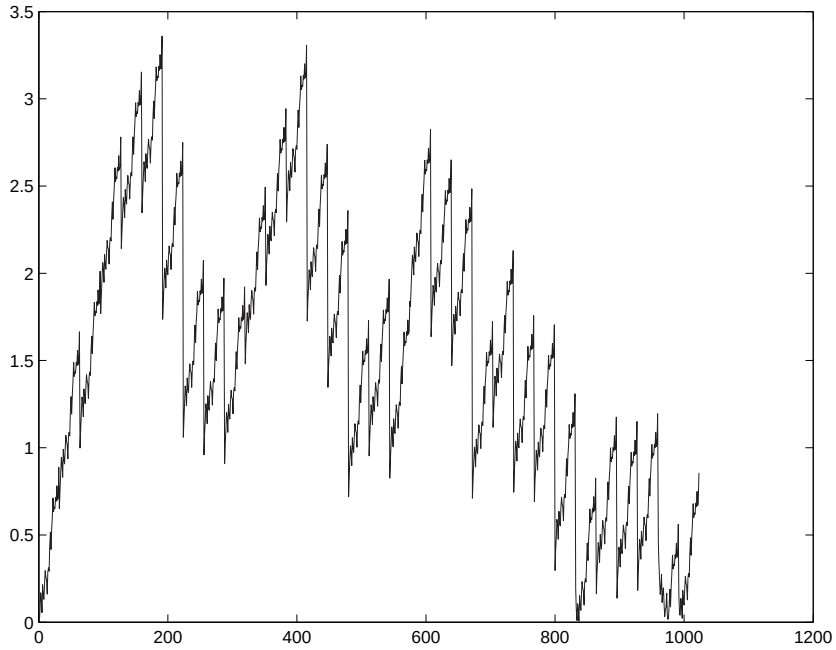

Figure 2.9: INL $W = 2 * .25\mu \quad L = 10\mu$

done into the node x_r (figure 2.3) depending on the comparator output. This would require a digital block which controls the calibration DAC input accordingly taking the comparator output and an analog comparator to compare the two outputs as mentioned earlier. The Digital block is explained in the next chapter and the comparator in the chapter that follows the next.

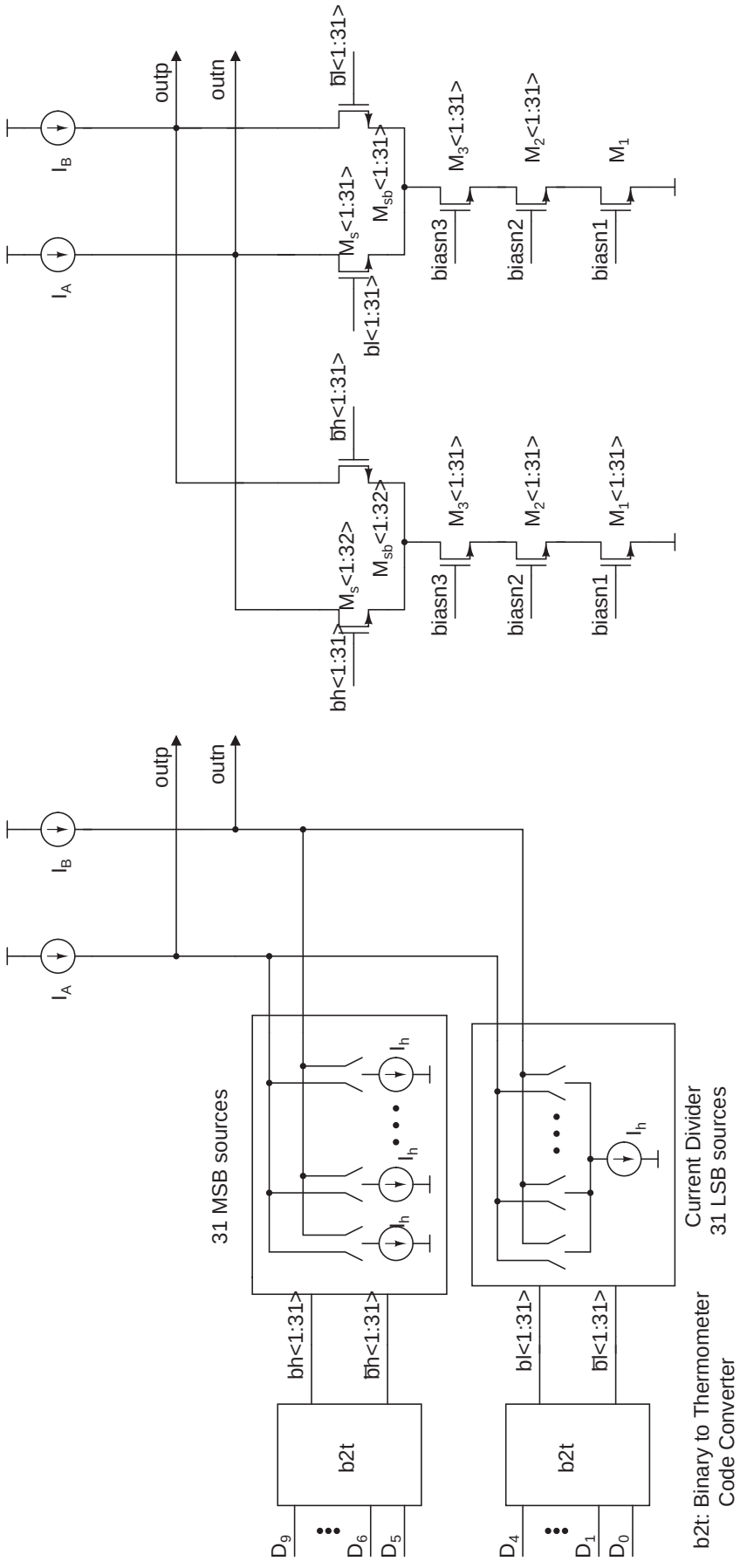

Figure 2.10: Calibration DAC with dual swing

CHAPTER 3

Digital Control Block

3.1 Introduction

As explained in the previous sections the entire calibration of the R2R DAC is centered around making the branch current equal to the reference current such that there is binary division of the current at each node, n_r (figure 2.1), that the current enters. Hence the main functions of the digital block is to find out how much current is to be sourced or sinked and retain the correct digital input to the calibration DAC in registers. Digital block used here is not a single block which controls the calibration of both the, the main and the complementary, ladders. It is mainly divided into five blocks. This division is done primarily to reduce the otherwise huge routing from the digital block to the rest of the blocks like the R2R ladders, calibration DACs, comparator and the other circuitry like the non overlapping generator. This dividing the functionality also gives good layout pattern.
The five digital blocks are

1. The Input Block
2. The Digital Calibration Block-1
3. The Digital Calibration Block-2
4. The Non Overlapping Generator
5. The Binary to Thermometer code Converter Block

3.2 The Input Block

This block is an asynchronous block, not clock controlled. The inputs and outputs are shown in the figure 3.1.

3.2.1 Inputs

The inputs to this block are

1. **Mode**: Mode is a three bit input. The entire R2R DAC can work in six different modes depending on the mode selected as explained below.

   (a) Mode 00x: This mode makes leaves both the OpAmp and the R2R DAC uncalibrated. The last bit suggests the DAC switching type, as explained in the later sections.

   (b) Mode 01x: This mode calibrates the OpAmp offset only. The need for the OpAmp offset cancellation and the method for the offset cancellation is explained in the later sections.

   (c) Mode 10x: This mode first calibrates the OpAmp to remove its offset. Then the main ladder is calibrated followed by the calibration of the complementary ladder.

   (d) Mode 11x : This mode is set to the default mode of 00x.

   (e) Mode xx0 : In any of the modes just mentioned the last bit suggests the kind of switching to be taken up in the R2R ladders, once the calibration is over in the 01x and 10x modes and without calibration in the 00x and the 11x modes. For 0 in the last bit suggests that the switching is complementary fashion switching. Here the Digital input to the DAC is applied directly to the main ladder and input's complement to the complementary ladder. In xx0 mode both the ladders are ON for all the input codes. The disadvantage with this mode is that the noise from the reference generators, both V_{refp} and V_{refm} as shown in

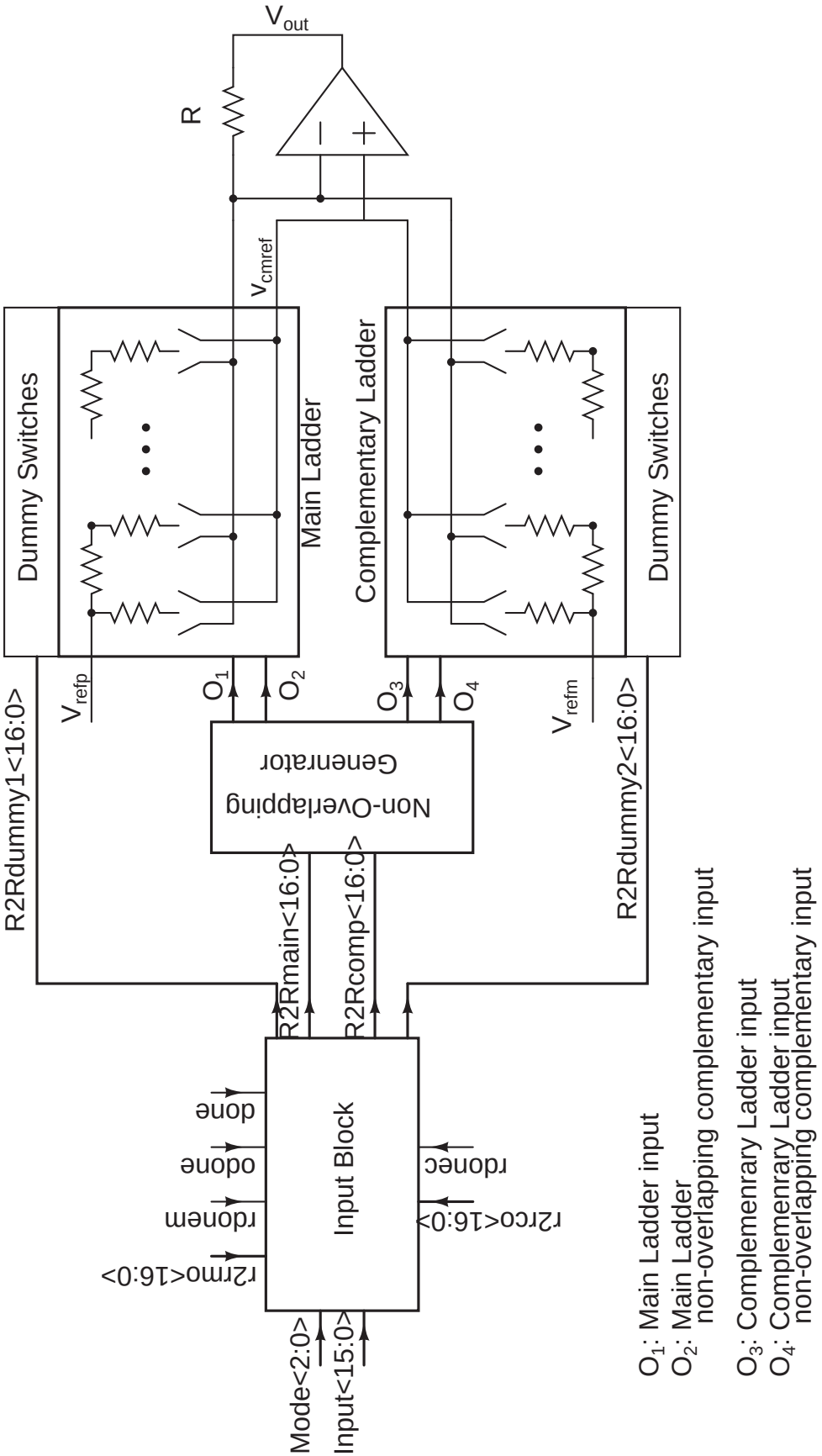

Figure 3.1: The Input Block

figure 3.1, directly affects the output. This is because both, the main and the complementary, ladders are operating for any given input code. The noise from the reference generators is significant.

(f) Mode xx1 : If the last bit in the input mode is 1 then the DAC input switching is done in the "switching in the middle" fashion. Here only one ladder, either the main or the complementary, is ON for any given input code. This eliminates the noise coming from one of the references for any given input code. For our 16 bit DAC, input codes 0x0000 to 0x7FFF make the main ladder off, i.e no output is given from the main ladder. All these codes operate on complementary ladder only eliminating the noise contribution of the reference V_{refp}. In all these codes, transition in 1 LSB bit corresponds to 2 LSB change in the output from the complementary ladder. Input codes 0x1000 to the 0xFFFF operate only on the main ladder and keep the complementary ladder off, eliminating the noise coming from the reference V_{refm}.

2. **Input** : This is the 16 bit input to the R2R DAC. This input is given to the ladder once the done signal is high. Done signal high implies that the calibration is complete and the ladder can function as a normal DAC.

3. **odone** : This is the signal that notifies the input block about the completion of the OpAmp offset calibration completion in the 01x and the 10x modes. Till the calibration is not complete this signal is low in these modes. For the rest of the modes this signal is low always as the offset cancellation is done for the OpAmp. This signal is the output signal from the "Digital Calibration block-1" that controls the calibration of the main ladder and the OpAmp offset calibration.

4. **rdonem** : This signal is low till the main ladder calibration is over in the 10x mode. Once the calibration is over this signal goes high, in the 10x mode. For the rest of the modes this signal is low as the calibration of the main ladder is not done in these modes. This signal is, also, an output from the "Digital Calibration block-1".

5. **rdonec** : This signal is given from the "Digital Calibration block-2" that controls the calibration of the complementary ladder. It is low till the calibration of the complementary ladder is not complete in the 10x mode. For the rest of the modes this signal is low always.

6. **r2rmo** : This is a 17 bit input to the Input Block. This input comes from the "Digital Calibration block-1". This input is not passed to the output in the 00x mode. This is all low for the 01x and 10x modes till the odone is high. Low from this input makes the main ladder turn off while the offset calibration is being done in the 01x and 10x modes. This input is given to the output while main ladder is being calibrated , i.e when odone is high and the rdonem is low in the 10x mode. This is all low again once the main ladder is calibrated and the complementary ladder is being calibrated, i.e when odone and rdonem both are high and rdonec is low.

7. **r2rco** : This is also a 17 bit input to the Input Block. This input comes from the "Digital Calibration block-2". This input is not passed to the output in the 00x mode. This is also all low till the offset calibration is finished, i.e odone is not high in the 01x and the 10x modes. For the 10x mode, till the main ladder calibration is done, i.e rdonem is low, this signal is low again. This input is passed to the output once the main ladder calibration is complete. This input, thus, has significance in the 10x mode only.

3.2.2 Outputs

The outputs to the Input Block are

1. **R2Rmain** : This is a 17 bit output given to the non overlapping generator. This output is multiplexed result of the Input<15:0>,1'b0 (This notation means that the 16 bit input code is appended with an extra 0 bit in the lsb position) and r2rmo$< 16 : 0 >$ as explained in detail in this section. This is, primarily, the input to the main ladder.

- 000 Mode: R2Rmain is equal to Input< 15 : 0 >,1'b0. This mode equal to 110 mode.
- 001 Mode: R2Rmain is all low for all the Input codes from 0x0000 to 0x7FFF. For the Input codes from 0x8000 to 0xFFFF this output is 1 bit left shifted Input added with an extra bit 0 in the 0th (lsb) position. The same happens in the 111 mode.
- 010 Mode: R2Rmain is all low till odone is high. And then it is equal to Input<15:0>,1'b0.
- 011 Mode: R2Rmain is all low till odone is high and also for the Input codes from 0x0000 to 0x7FFF. For the Input codes from 0x8000 to 0xFFFF it is 1 bit left shifted Input added with an extra bit 0 lsb position.
- 100 Mode: R2Rmain is all low till odone is high. Then for odone high it is equal to r2rmo< 16 : 0 > till rdonem is high. Once rdonem is high it is all low again till rdonec is high. Once rdonec is high, R2Rmain is equal to Input< 15 : 0 >,1'b0.
- 101 Mode: R2Rmain is same as the 100 mode except that once the rdonec is high it all low for the input codes 0x0000 to 0x7FFF and for input codes 0x8000 to 0xFFFF this output is 1 bit left shifted Input added with an extra bit 0 in the 0th position.

2. **R2Rcomp** : This is, primarily, the input to the complementary ladder. This is also a 17 bit output given to the non overlapping generator. This output is multiplexed result of the Input< 15 : 0 >,1'b0 and r2rco< 16 : 0 > coming from "Digital Calibration block-2".

   - 000 Mode: R2Rcomp is equal to the complemented Input< 15 : 0 >,1'b0. This mode equal to 110 mode.
   - 001 Mode: R2Rcomp is equal to 1 bit left shifted Input code appended with a zero in the lsb position for all the Input codes from 0x0000 to

0x7FFF. For the Input codes from 0x8000 to 0xFFFF this output is all zero. This mode equal to 111 mode.

- 010 Mode: R2Rcomp is all low till odone is high. And then it is complement of the bits Input$< 15:0 >$,1'b0.
- 011 Mode: R2Rcomp is all low till odone is high and also for the Input codes from 0x8000 to 0xFFFF. For the Input codes from 0x0000 to 0x7FFF it is 1 bit left shifted Input added with an extra bit 0 lsb position.
- 100 Mode: R2Rcomp is all low till rdonem is high. Then equal to r2rco$< 16:0 >$ till rdonec is high. Once rdonec is high it is complement of Input$< 15:0 >$,1'b0.
- 101 Mode: R2Rcomp is all low till rdonem is high. Then equal to r2rco$< 16:0 >$ till rdonec is high. Then it is all zeros for the input codes 0x8000 to 0xFFFF and for input codes 0x0000 to 0x8000 this output is 1 bit left shifted Input added with an extra bit 0 in the 0th position.

3.2.3 Area

Size of this Block for a 70% density is 50μ x 150μ. The size is set so as to fit the net routing from this block to the non overlap generation block. The area is $7500\mu m^2$.

3.3 The Digital Calibration Block-1

This is a clock controlled, synchronous, block. This block controls the OpAmp offset calibration and calibration of the main R2R ladder. Figure 3.2 shows this block with inputs and outputs. Following sections explain the method of calibration and the in/outs of this block.

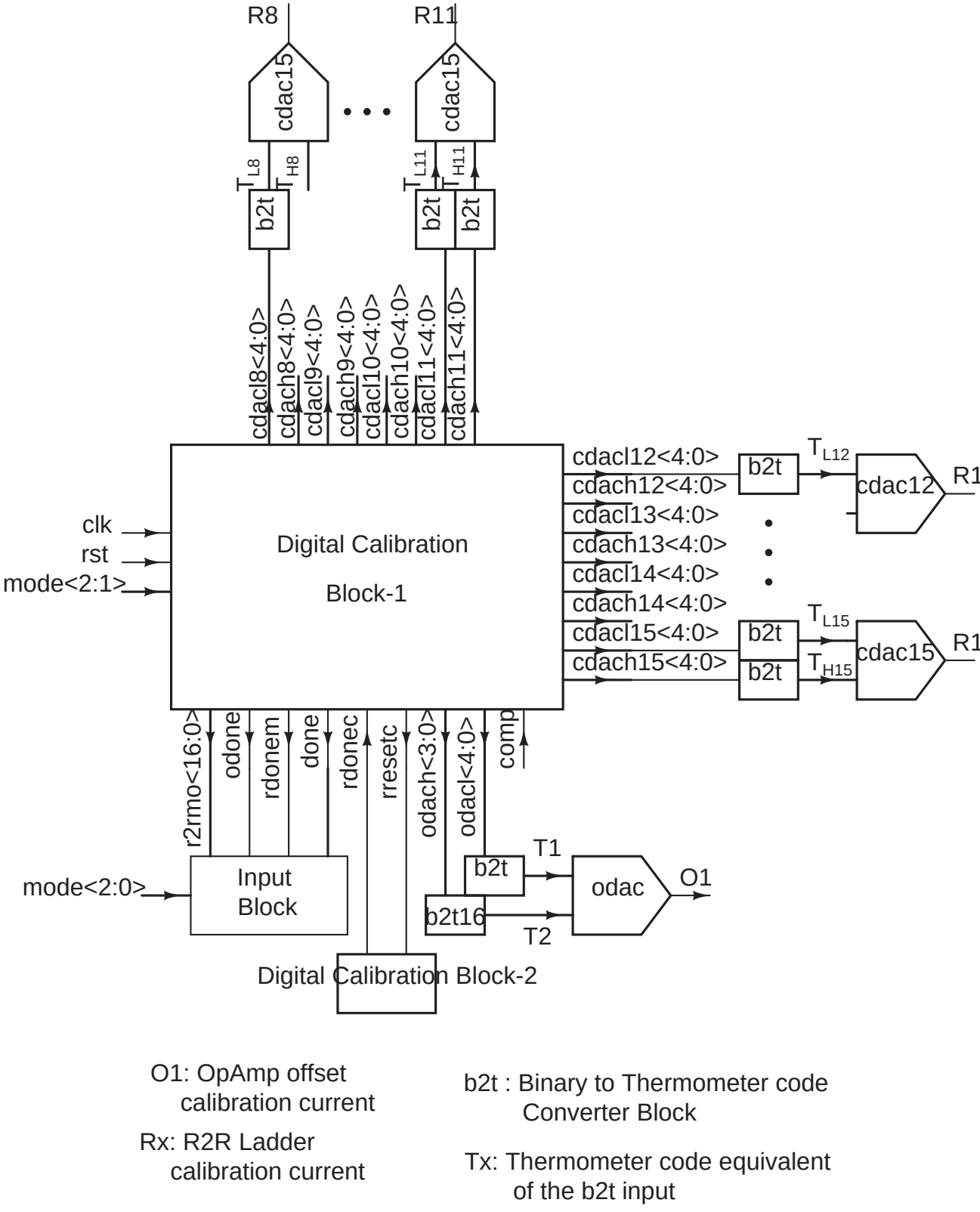

Figure 3.2: The Digital Calibration Block-1

3.3.1 Inputs

The inputs to this block are

1. **clk** : This is the clock input to the digital block.
2. **mode** : This is first two MSBs of the three bit mode input. 00 in in the mode keeps this block in the default reset mode. 01 would make the block to calibrate only the Offset of the OpAmp. 10 in the input would make the block calibrate the OpAmp offset first then calibrate the main ladder.
3. **rst** : This is the reset signal that would initialize the digital block. This signal has to be high initially then it should be made low for the proper initialization of all the digital blocks.
4. **comp** : This is the comparator output.
5. **rdonec** : This signal notifies Digital Calibration block-1 that calibration of the complementary ladder is complete in the 10x mode.

3.3.2 Outputs

The Outputs from The Digital Calibration Block-1 are

1. **r2rmo** : This 17 bit output is the control inout for for the main ladder while the main ladder is being calibrated. As explained in the section 3.2.1 this is given to the Input block as input.
2. **odach** : This is a 4 bit output given to the binary to thermometer code converter block which inturn controls the calibration current of the OpAmp offset calibration. This input controls the current of the "high-current" cells (each with value equal to 32 LSBs). This is a memory output in the sense that it retains the value once a value is set to it in the calibration process so as to keep the calibration current supplied always while the DAC functions.

Default value of this output is 1000. This makes half the "high-current" cells ON.

3. **odacl** : This is a 5 bit output. This is fed to the "lower-current" cells (each with value equal to 1 LSB current) through Binary tp thermometer code converter. This is a memory output as well. Default value of this output is 00000 making all the "lower-current" cells off. In the default state both odach and odacl supply zero calibration or correction current to the OpAmp.

4. **odone** : This is high when the Offset of the OpAmp is calibrated in the 01x and 10x modes. As explained in the earlier section this is an input to the Input Block.

5. **rdonem** : This is also an input to the Input Block. It is explained in that section.

6. **done** : This is high in 00x mode, low till odone is low in 01x mode and low till rdonec is low in 10x mode. High on this signal implies the completion of the calibration.

7. **rresetc** : This is the reset signal to the Digital Calibration Block-2. This is high in all the modes except in 10x mode when the calibration of the main ladder is complete (i.e rdonem is high).

8. **cdachxx** : This is a five bit output given to the high-current cells of the calibration DAC through the binary to thermometer code converter block. This is a memory output. There are 8 such outputs each to control the calibration current of each MSB branches of the R2R DAC. The default value on this output is 10000, equivalent to 16 current cells being ON.

9. **cdaclxx** : This is also a five bit output. It controls the lsb-current cells of the calibration DAC through the binary to thermometer code converter block. This is also a memory output. The default value of this output is 00000, making all the lsb-current cells switch off. Combined with default value of 10000 on cdahxx the current supplied to the node x of the R2R

ladder is zero in the reset state. There are 8 such outputs each for the one branch of the R2R ladder.

3.3.3 OpAmp Offset Calibration

The calibration method for both the OpAmp (details of the structure and functioning of which can be referred from [3]) Offset calibration is explained here. Figure 3.3 shows simplified view of the OpAmp with offset. When $I_{DAC} = 0$ with offset voltage v_{OS}, $v_{out} = V_{cm} + v_{OS}$. Making the output voltage equal to the common mode voltage by injecting (+/-) the current at the node n_x calibrates the Offset of the OpAmp. Here i_c is the correction current that is supplied from the calibration DACs and controlled by the outputs odach and odacl through binary to thermometer code converter block. $i = g_{mp} \times \frac{v_{OS}}{2}$, where g_{mp} is the transconductance of the input transistors. For instance, if the offset, v_{OS}, is positive then i_c has to be positive and equal to $g_{mp} \times v_{OS}$.

The minimum correction current is limited by the comparator resolution, i.e

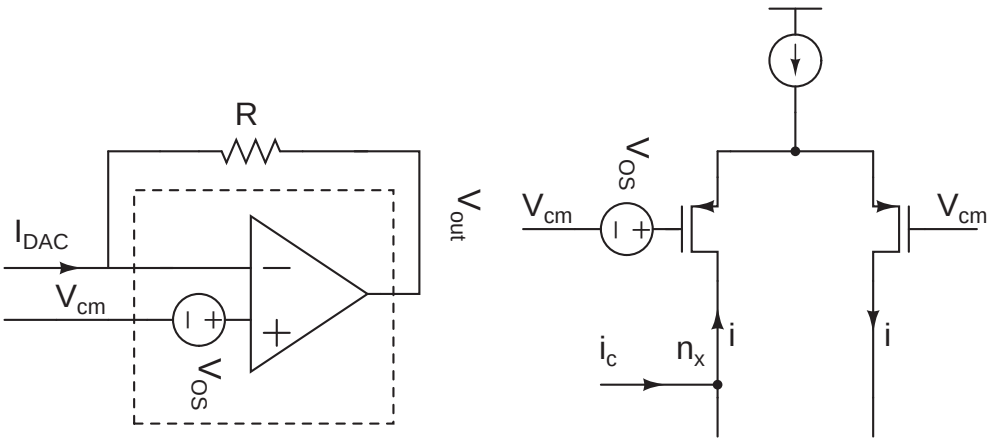

Figure 3.3: OpAmp with Offset

the least difference in the comparator input voltages that would flip the comparator output. For instance, if the comparator resolution is d volts, then the OpAmp offset can be corrected to d volts. The correction current required, then, is $i_c = g_{mp} \times d$. This is the minimum current and forms the lsb norm for the calibration DAC. It is mentioned as 50nA. With the given technology parameters,

the maximum offset for the given OpAmp was mentioned as 700μ A [3]. Given the LSB current limited by the comparator resolution and the maximum required current set by transistor sizes, the required number of bits for the calibration DAC was established as 9 [3].

The calibration block starts with mid code so as to supply zero current at i_c. If the comparator output is high, signifying that the offset is positive, the LSB cells keep switching ON supplying the current to the OpAmp. Once all the LSB cells are ON then one higher-current cell is ON along with that the LSB cells go off in the next clock to make the change in each cycle to be one LSB.

In the same way, if the comparator output is low, the calibration block makes the current cells go off one LSB cell at a time. In this manner total number of clock cycles taken for the Offset calibration is 512. After the OpAmp offset calibration is complete the control goes to the R2R main ladder calibration by making the reset signal to the ladder calibration block low, in the 10x mode.

3.3.4 R2R Ladder Calibration

As explained in the section 2.2, V_{out1} is the reference voltage formed by switching all the lower branches of the ladder ON. Since the significance of the calibration is so little for the lower ladder branches, only first eight MSB branches are calibrated. So the reset input,r2rmo, for the ladder is 0x000FF. This forms the reference voltage, V_{out1}, for calibrating the eighth branch of the ladder. Figures 3.4 and 3.5 show the calibration waveforms. ϕ_1 and ϕ_2 are the non overlapping clocks given to the comparator. co is is the control signal for all switching the reference and the branches at the correct instances. pre is the comparator output delayed by a clock cycle. cnt is the signal to note the changes in the comparator output at the clock edges. change is the XORed signal of comp and pre signifying the change in the comparator output. It is to be noted here that this signal keeps toggling every clock cycle (not shown in the figure) as the comparator output toggles for each falling edge of ϕ_2. But the correct value is taken by considering the value at the rising edge of the signal co only. h and l are the number of "higher-current" cells and LSB current cells ON, respectively. It is shown in the figure 3.4 that

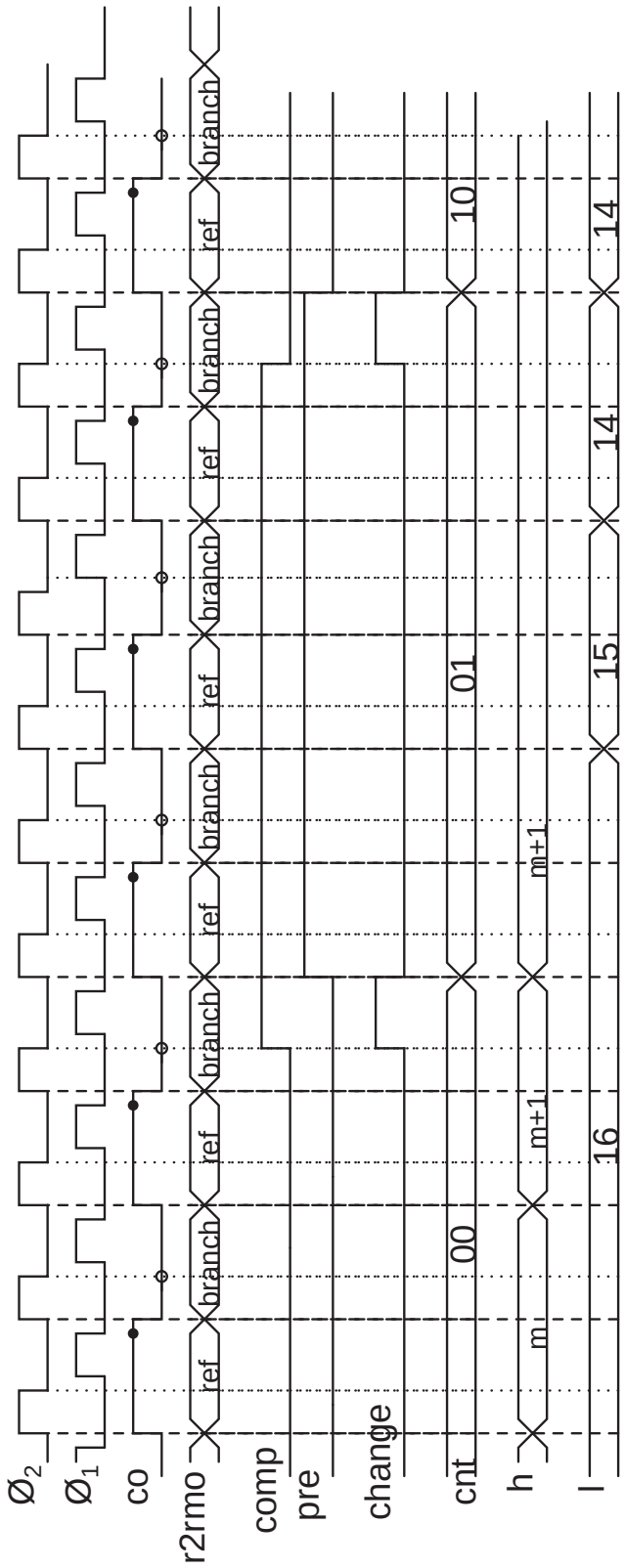

Figure 3.4: Calibration Waveforms

the reference and the branch are switched alternately. ϕ_2 is the clock input signal to The Digital Calibration Block-1. ϕ_1 and ϕ_2 are two non-overlapping clocks required by the comparator as explained in the next chapter. Comparator correct output is given by comparing the OpAmp output voltages at the dotted instances. These instances are the falling edges of the two non overlapping clocks ϕ_1 and ϕ_2. The correct comparator output is obtained when the value at the instance of the open circle is compared to the value at the filled circle. Comparator output is exactly the opposite for the other falling edges of the clocks ϕ_1 and ϕ_2 but this is discarded by considering the output at the rising edge of the signal co. Calibrating the ladder by changing one LSB current at time would take 1024 clock cycles. This would require a lot of time to calibrate all the branches. This also would consume a lot of power. Hence, the "higher-current" cells are changed, accordingly, first then the LSB current cells. This can be seen in the figure 3.4. For instance, if the current number of the "higher-current" cells is m then for a low in the comparator output would increase that number to m+1. If this causes a change in the comparator output (here from low to high) the number of "higher-current" cells remain as it is keeping the comparator output in the same state. This would call for a change and increase in signal cnt so that LSB current cells start changing now. Here the number of LSB current cells starts decreasing as the comparator output is high. A change in the comparator output again (here from high to low) would mean that branch current is within one LSB of the reference current. This stops the branch calibration as shown in the figure 3.5 and the values are reset in the next clock edge. This also starts the calibration of the next branch. Another point to note here is that at the reset instance the reference current has to be that of the next branch (since the reset values are edge clocked this would still keep previous reference but the present branch) . This is made sure by forcing the correct reference at that instance. It is also made sure that signal cnt does not change when there is a change in the comparator output once the branch changes. This makes the calibration to continue in the right way.

Calibration of the ladder starts from the eighth branch and proceeds to the higher branches of the ladder. Calibration is complete once the MSB branch, 16^{th} is calibrated. This would make the rresetc, the reset signal to The Digital Calibration

Block-2 go low. As mentioned the calibration of the ladders happens in the 10x mode only. Once the calibration of the complementary ladder is also complete, done signal sis set high stopping all the switching activity in the digital calibration blocks. This way dynamic power is reduced in this digital blocks.

3.3.5 Power

The highest switching happens when the comparator output does not change at all while the calibration is being done. For this highest switching activity the power consumed is obtained to be 186μW. The break up is as in the table 3.1. This is for the 6MHz clock. The power consumed in the Offset calibration is 35μW. For the slower clock (corresponding to OSR 8 of the audio band width 48KHz) of

Total Power (μW)	Dynamic Power (μW)	Leakage Power (μW)	Switching Power (μW)	Internal Power (μW)
186	181.9	4.3	49.3	132.5

Table 3.1: Power for clock frequency of 6MHz

384KHz the power obtained is shown in the table 3.2. The power contribution of the Offset calibration is 3.3μW.

Total Power (μW)	Dynamic Power (μW)	Leakage Power (μW)	Switching Power (μW)	Internal Power (μW)
13.4	9.1	4.3	2.5	6.6

Table 3.2: Power for clock frequency of 384KHz

3.3.6 Area

The size of The Digital Calibration Block-1 for 70% core density is 261μ x 304μ. Hence the area is 79344μm^2. The height of 304μm is chosen so as to keep the routing of the cdachx and cdaclx outputs proper. These outputs are given to the

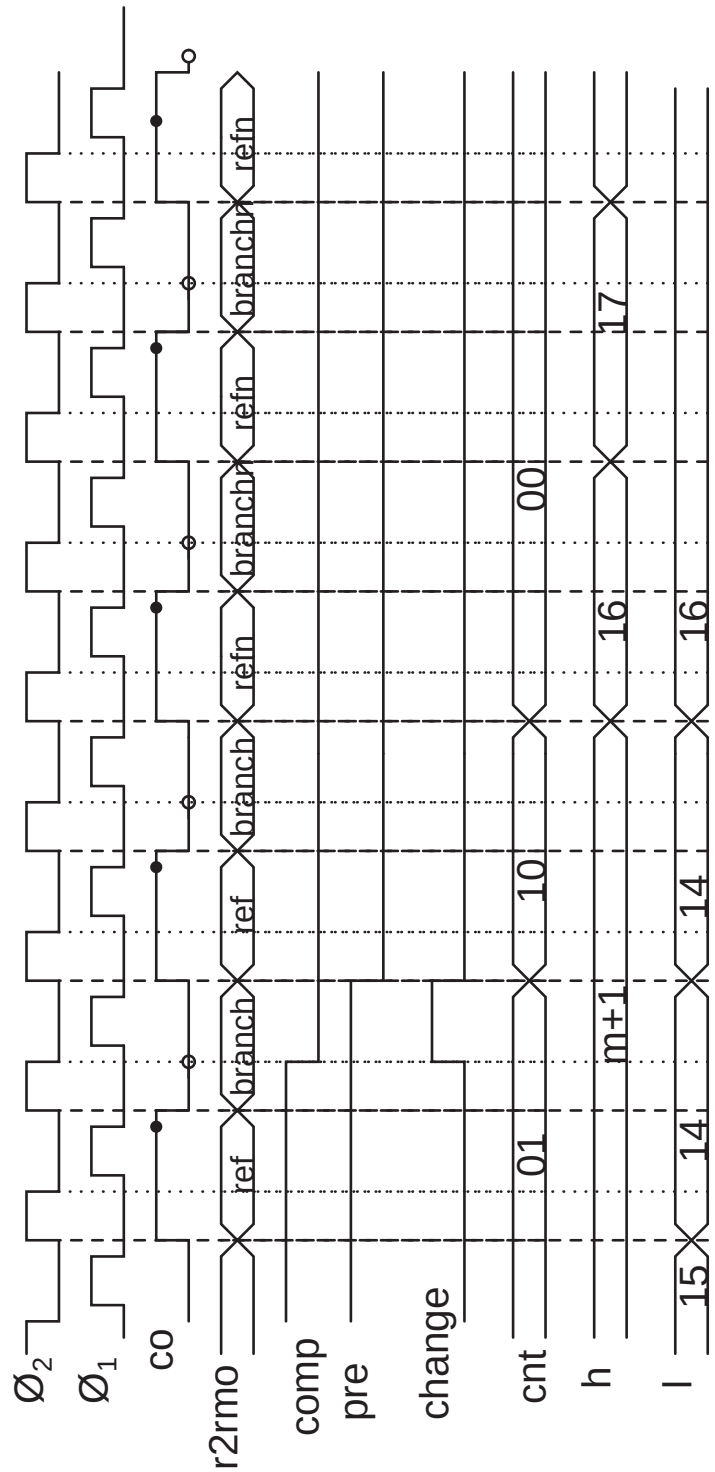

Figure 3.5: Calibration Waveforms

binary to thermometer code converter blocks. There are eight such blocks with the height of 38μ each.

3.4 The Digital Calibration Block-2

The Digital Calibration Block-2 controls the calibration of the complementary ladder in the mode 10x only. This is shown in the figure 3.6. This block is in reset

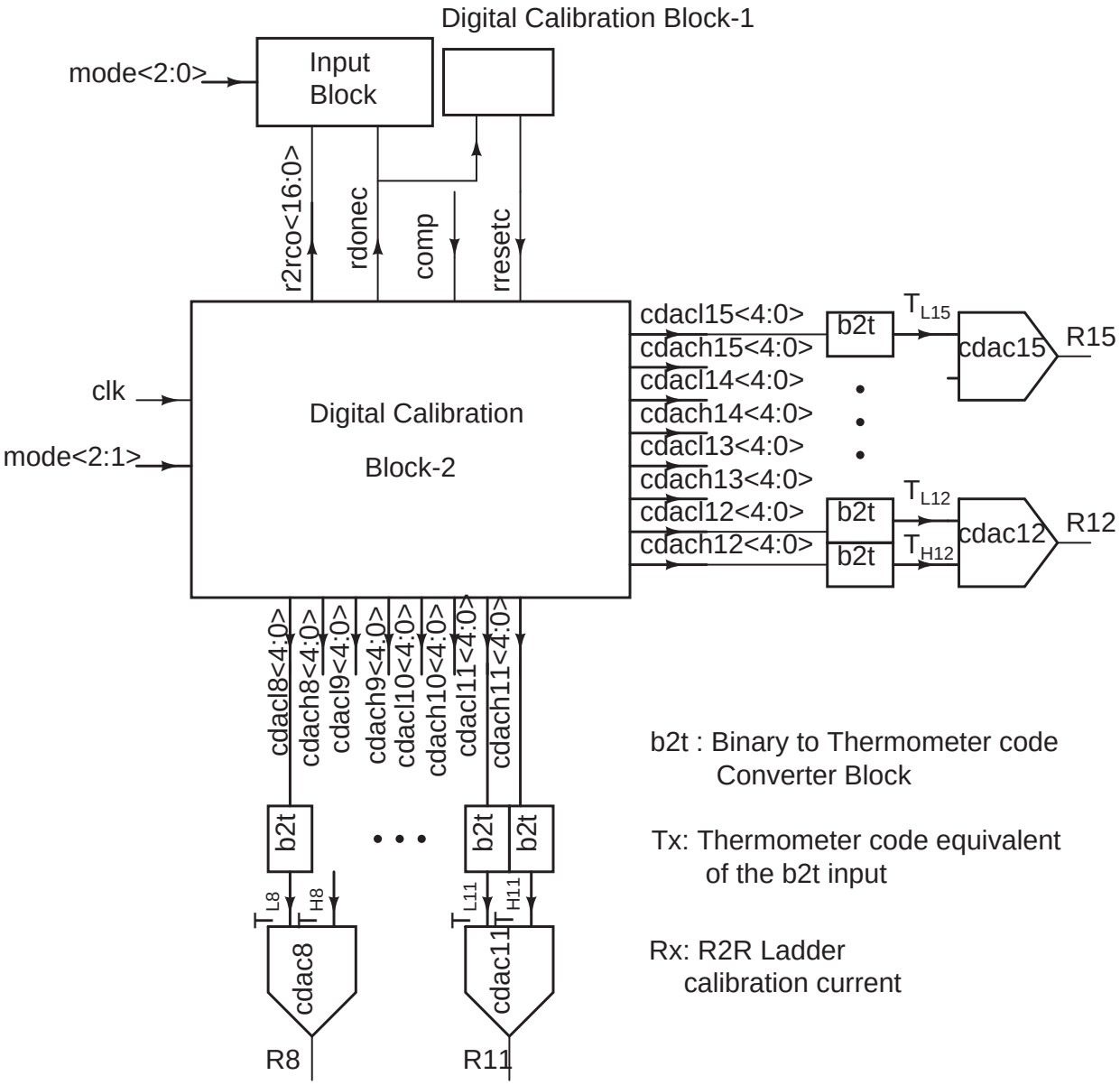

Figure 3.6: The Digital Calibration Block-2

state till the control is given to it from the Digital Calibration Block-1 by making

rresetc signal low. In the reset state this block supplies zero calibration current to the complementary ladder. The inputs and outputs function same as the Digital Calibration Block-1.

3.4.1 Power

For the highest switching (when the comparator output does not change) the power consumed is obtained to be 184μW. The break up is as in the table 3.3. This is for the 6MHz clock. For the slower clock of 384KHz the power obtained is

Total Power (μW)	Dynamic Power (μW)	Leakage Power (μW)	Switching Power (μW)	Internal Power (μW)
184.6	184	0.6	53.5	130

Table 3.3: Power for clock frequency of 6MHz

9.5μW. The break-up is shown in the table 3.4.

Total Power (μW)	Dynamic Power (μW)	Leakage Power (μW)	Switching Power (μW)	Internal Power (μW)
9.5	8.5	0.6	2.5	6.3

Table 3.4: Power for clock frequency of 384KHz

3.4.2 Area

The total of the Digital Calibration Block-2 area is 55328μm^2 for the core density of 70%. The size is 182μ x 304μ. The cdachx and cdaclx outputs go to the binary to thermometer converter block here, also, each with a height of 38μ. So the height of this block is also chosen as 304μ.

3.5 The Non-Overlapping Generator

The non-overlapping generator block is used as shown in the figure 3.1.

Inputs : The inputs are r2rmo and r2rco, both 17 bit, as explained in the previous section3.2.1.

Outputs : The outputs O_1 and O_2 are non overlap with each other, so are O_3 and O_4. The non overlap time is set as 3ns. These outputs are the switch inputs of the R2R ladder. Non overlap in the switch inputs is needed as, otherwise, there will be a low impedance short between the input terminals of the OpAmp during the overlap period. This increases the non linearity in the the system and hence the output.

3.5.1 Area and Power

Size of this block is 80μ x 150μ and the area is $12000\mu m^2$.

The power consumed when all the bits of both the inputs go from low to high is 1.5μW.

The delay from input to output is around 2ns.

3.6 The Binary to Thermometercode Converter Block

This is a non clocked digital block which converts given five bit digital input to its equivalent thermometer code. Separation of this functionality from the main calibration blocks has reduced the net routing. It also gave the flexibility of generating a proper layout. The height of this block is made equal to the height of the calibration DAC, which is $38\mu m$. This gave the flexibility in routing the cdacx outputs from the Digital Blocks 1 & 2. Size of this block is 62μ x 38μ.

CHAPTER 4

Comparator & The High Voltage Generator

4.1 Comparator

This chapter briefly explains the comparator and the high voltage generator. Basic comparator is the regenerative latch shown in the figure 4.1. Voltages v_1 and v_2 are stored (on the parasitic capacitances) on the nodes n_1 and n_2 respectively in the clock phase ϕ_2. ϕ_1 is the regeneration phase. ϕ_1 and ϕ_2 are two non overlapping clocks as shown in figure 4.1. These are the same clocks mentioned in figures 3.4 and figure 3.5. 4.2), A, is $\frac{14.5mV}{11.44\mu V} = 62dB$. Each inverter being a negative gm block,

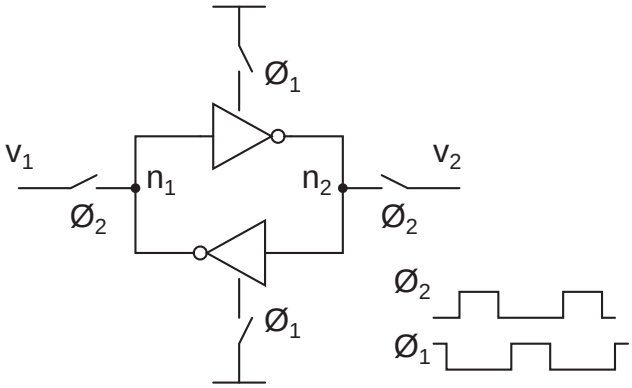

Figure 4.1: The Regeneration Latch

the higher of the two node voltages regenerates to the supply voltage and the other to the supply ground in ϕ_1 phase, the regeneration phase. The minimum voltage difference required for the regeneration is set by the threshold mismatch between the two inverters. For the sizes used here, the mismatch can be as high as 14.5mV. This is over come by giving inputs via a pre-amplifier. With the least voltage difference in v_1 and v_2 being the LSB of the R-2R ladder, 11.44μV, the minimum gain required by the pre-amplifier (shown in figure 4.2), A, is $\frac{14.5mV}{11.44\mu V} = 62dB$.

But the pre amplifier itself will have the mismatch. This is canceled by storing

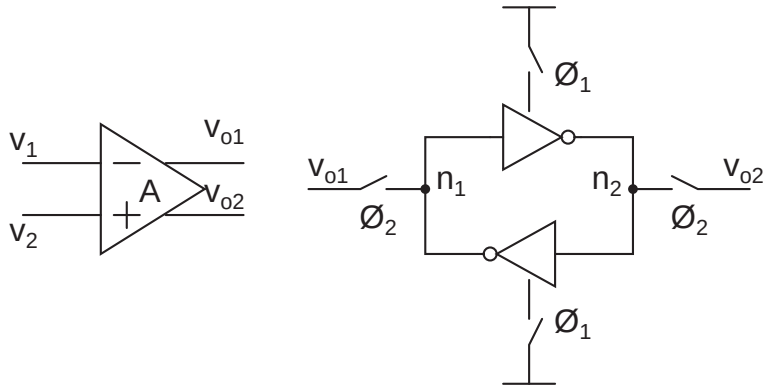

Figure 4.2: The Regeneration Latch with Pre-Amplifier

the mismatch in one phase and canceling it in the other phase as shown in the figure 4.3. Here ϕ_{2r} is same as ϕ_2 when the ladder calibration is ON other wise it is zero. In the same way, ϕ_{2o} is same as ϕ_2 when the OpAmp offset calibration is ON other wise it is zero. As showed earlier(figure 4.1), ϕ_1 and ϕ_2 non overlapping clocks. As mentioned earlier in the section 2.2, the R-2R ladder output voltages

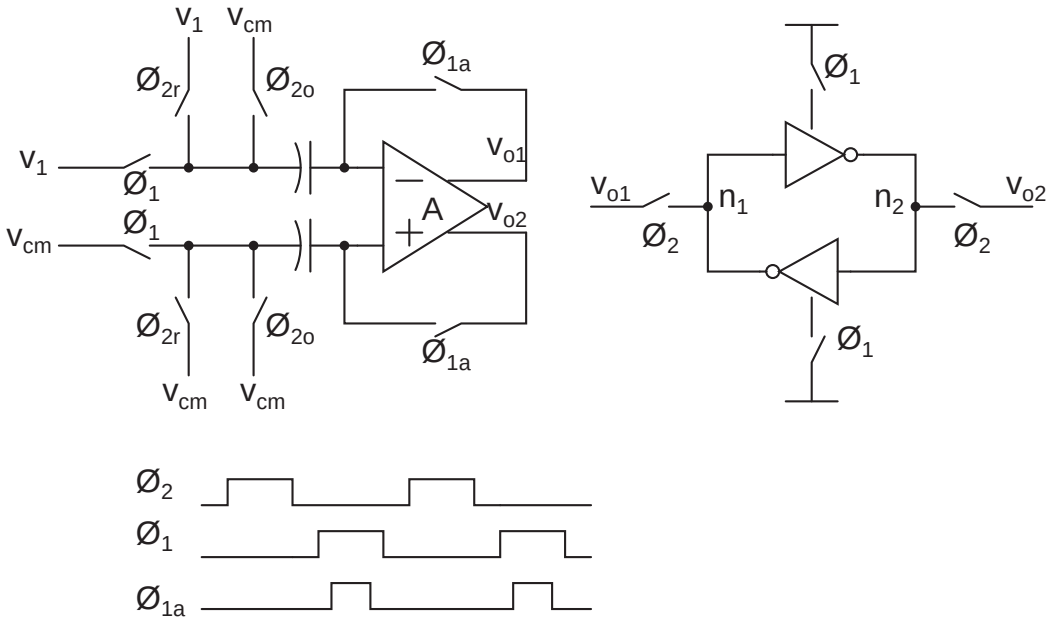

Figure 4.3: Pre-Amplifier Offset Cancellation

V_{out1} and V_{out2} are formed in these clock instances. With the arrangement shown in the figure 4.3, in ϕ_1 phase the capacitor stores the pre-amp offset and the ladder reference voltage. This is compared to the branch voltage added with the offset of the preamp in the ϕ_2 phase. This is regenerated in the next ϕ_1 phase. This

compared output needs to be ready by the next rising phase of ϕ_2.

For the Offset of the OpAmp calibration, the capacitor stores the pre-amp offset and the Opamp output voltage in the ϕ_1 phase. It is compared to the common mode voltage combined with the preamp offset.

Comparator used here was designed to be a very high gain comparator to overcome the mismatch issues. The frequency of the clocks used here is set to be 384KHz, so as to relax the constraints on the phase response of the pre-amplifier. Also the settling time for the voltage on the capacitor is more with 384KHz clock compared to 6.144MHz clock.

The clock fed to the digital blocks ϕ_2.

4.2 The High Voltage Generator

As mentioned in the section 5, te R-2R ladder switches are driven by 1.8Vto 2.7V converters. Required 2.7V is generated locally. This generation was done using 6.144MHz clock. The peak-to-peak ripple in the design was seen to be 300μV after the layout was done.

As mentioned comparator runs at 384KHz and the high voltage generator requires a high frequency clock, around 6MHz. After the calibration is complete, to make he DAC work at any required frequency a clock multiplexer is used.

CHAPTER 5

Conclusion

R-2R ladder structures are simple in structure and operation. For frequencies in the audio band, these DACs introduce no flicker noise. 16-Bit R-2R DAC used here has two ladders, the main ladder and the complementary ladder, to double the output swing. V_{refp}, the reference voltage for the main ladder, is 1.65V and V_{refm}, the reference voltage for the complementary ladder, is 0.15V. Hence the total voltage swing at the output is 1.5V. Resistance, R, in figure 1.2 was chosen to be 20KΩ for layout and mismatch considerations. This would set the minimum current, or the LSB current, from each branch to be 522.2pA. For 20KΩ resistance in the feedback would make this 11.44μV. The switch sizes were progressive to reduce the resistance in the switch path as mentioned in[3]. Non overlap in the switch inputs increases the performance by 4dB as shown in[3]. There is a 1.8V to 2.7V generator which converts all the switch inputs from 1.8V to 2.7V before being fed to the switches. This decreases the switch resistanceas the overdrive is increased by 900mV.

For the audio bandwidth of 48KHz, the digital blocks were synthesized for an OSR of 128 or a frequency of 6.144MHz. As mentioned in the chapter 4, the comparator switching is done at an OSR of 8, i.e 384KHz. For this reason even the digital blocks were clocked at this frequency. The worst case time taken for calibration in mode 01x is 1.3ms. For the mode 10x it is 2.7ms. The total power due to the digital blocks is around 25μW in the worst case. The split up is as shown in the table 5.1.Total area due to the digital blocks is 242892μm^2. The area split up is shown in the table 5.2. Complete layout with the output driver and comparator is shown in figure 5.1. The digital blocks are marked in red.

1. Digital Calibration Block-1
2. Digital Calibration Block-2

Block	Total Power (μW)
Digital Calibration Block-1	13.4
Digital Calibration Block-2	9.5
Non Overlap Block	1.5
Input Block	0.1
Binary to Thermometer Conveter Block	0.9

Table 5.1: Worst case Power Requirement of Each Block

Block	Total Area (μm^2)
Digital Calibration Block-1	79344
Digital Calibration Block-2	55328
Non Overlap Block	12000
Input Block	7500
Binary to Thermometer Conveter Block	2356

Table 5.2: Area of Each Block

3. Input Block

4. Non-Overlap Block

5. Binary to Thermometer Conversion Block

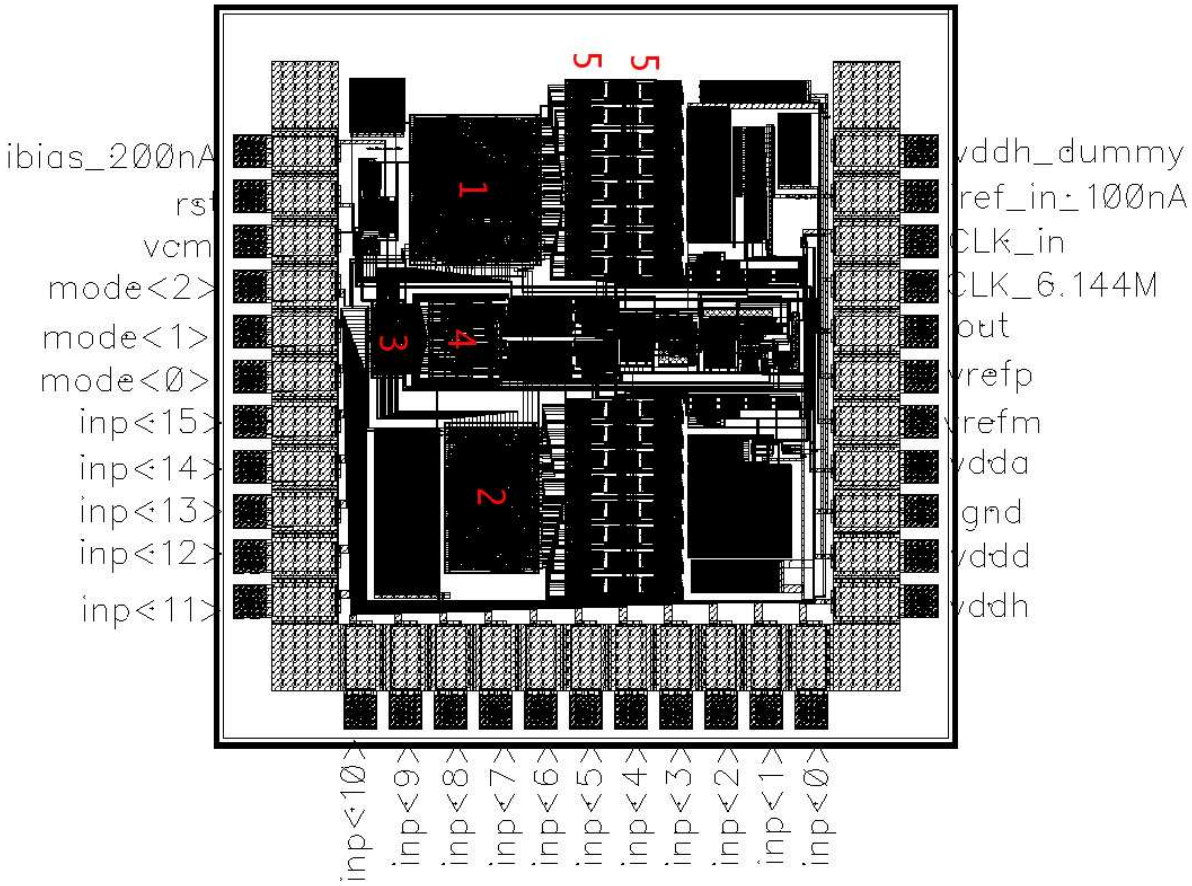

Figure 5.1: Layout

APPENDIX A

Binary and Thermometer coded DACs

A.0.1 Binary DAC

In a , let us say, 3 bit Binary DAC, the current sources (as shown in the figure A.1) are

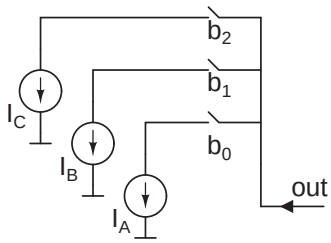

Figure A.1: 3 bit binary DAC (alternate paths for current sources not shown)

$$\begin{aligned} I_A &= N(I, \sigma_I) \\ I_B &= N(2I, \sqrt{2}\sigma_I) \\ I_C &= N(4I, 2\sigma_I) \end{aligned}$$

DNL between, say, input 010 and 001 comes from switching the LSB current cell, I_A off and switching I_B ON. Hence,

$$\begin{aligned} DNL_{010} &= \frac{I_B - I_A - I}{I} \\ &= \frac{N(2I, \sqrt{2}\sigma_I) - N(I, \sigma_I) - I}{I} \\ &= N(0, \sqrt{3}\sigma_I) \end{aligned}$$

In this way, switching some cells off and some ON, the maximum switching occurs at the mid code transition, where, the MSB cell, here I_C, is switched ON and the

rest of the lower cells, I_A and I_B, are switched off. So the maximum DNL for a 3 bit binary DAC is given by,

$$\begin{aligned} DNL_{100} &= \frac{I_C - (I_B + I_A) - I}{I} \\ &= \frac{N(4I, 2\sigma_I) - (N(2I, \sqrt{2}\sigma_I) + N(I, \sigma_I)) - I}{I} \\ &= N(0, \sqrt{7}\sigma_I) \end{aligned}$$

Where as, INL for input code 010 is given by

$$\begin{aligned} INL_{010} &= \frac{I_B - 2I}{I} \\ &= \frac{N(2I, \sqrt{2}\sigma_I) - 2I}{I} \\ &= N(0, 2\sigma_I) \end{aligned}$$

The maximum INL occurs when all the current sources are ON, i.e for the input code 111.

$$\begin{aligned} INL_{111} &= \frac{I_C + I_B + I_A - 7I}{I} \\ &= \frac{N(4I, 2\sigma_I) + N(2I, \sqrt{2}\sigma_I) + N(I, \sigma_I) - 7I}{I} \\ &= N(0, \sqrt{7}\sigma_I) \end{aligned}$$

A.0.2 Thermometer coded DAC

In a , let us say, 3 bit thermometer coded DAC, the current sources (as shown in the figure A.2) are

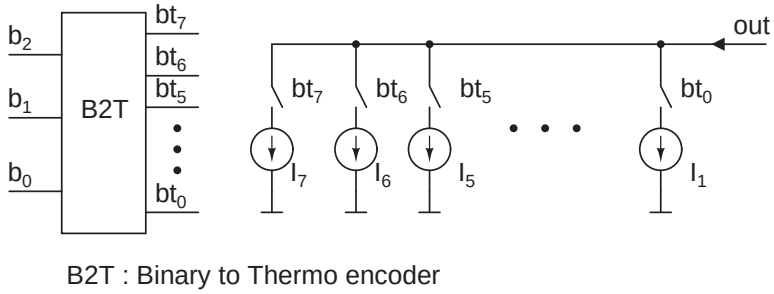

Figure A.2: 3 bit Thermometer coded DAC (alternate paths for current sources not shown)

$$
\begin{aligned}
I_1 &= N(I, \sigma_I) \\
I_2 &= N(I, \sigma_I) \\
&\cdot \\
&\cdot \\
&\cdot \\
I_7 &= N(I, \sigma_I)
\end{aligned}
$$

Like wise, the DNL between any input code transition is given by,

$$
\begin{aligned}
DNL_{010} &= \frac{I_1 + I_2 - I_1 - I}{I} \\
&= \frac{N(I, \sigma_I) - I}{I} \\
&= N(0, \sigma_I)
\end{aligned}
$$

The DNL or the major code transition is given by,

$$
\begin{aligned}
DNL_{100} &= \frac{I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 - (I_1 + I_2 + I_3 + I_4 + I_5 + I_6) - I}{I} \\
&= \frac{N(I, \sigma_I) - I}{I} \\
&= N(0, \sigma_I)
\end{aligned}
$$

This way the thermometer coded DACs eliminate the DNL caused, in the binary DACs, due to the major code transition. This is at the cost of increased complexity

of th binary to thermometer encoding block. This encoding block increases in size exponenetially ad the number of bits increase. And alsothe INL for the maximum input is, still, the same as shown below.

$$\begin{aligned} INL_{111} &= \frac{I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7 - 7I}{I} \\ &= \frac{N(7I, \sqrt{7}\sigma_I) - 7I}{I} \\ &= N(0, \sqrt{7}\sigma_I) \end{aligned}$$

APPENDIX B

Resistors in CMOS Technology

Resistors in the modern CMOS Technology are implemented using poly layers, metal layers, n or p diffussed areas or the n (or p) wells. Poly layers have higher sheet resistance, R_{sh}, than the n or p well areas. Again, these wells have higher sheet resistance than the diffusion areas. Metal layers have the least of the sheet resistance in the category. Hence the high value resistors are usually made with poly resistors, mid value resistors using wells and lower value resisistors using diffusion areas or the metal layers. Salicide layer on any of these resistors greatly reduces the sheet resistance. Hence the higher value resisistors are, ususally, non salicide poly layer resistors.

Diffusion and well resistors have greater voltage coefficients, hence huge non linearity exists with the voltage across the resistors. Salicide diffusion resisitors are lower value resistors with large variations hence not used for making resistors. Poly resitors are the common resistors used in CMOS technology. These resistors have good linearity with temperature and voltage. With varying diffusion the sheet resistance can be varied to get good almost linear resistors.

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