Design of Three-Stage Class-AB $16\,\Omega$ Headphone Drivers having $0.9\,\mathrm{V}$ and $0\,\mathrm{V}$ common mode voltages and a Negative Voltage Converter for $16\,\Omega$ load

A Project Report

submitted by

SILADITYA DEY

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of Three-Stage Class-AB** $16\,\Omega$ **Headphone Drivers having** $0.9\,\mathrm{V}$ **and** $0\,\mathrm{V}$ **common mode voltages and a Negative Voltage Converter for** $16\,\Omega$ **load**, submitted by **Siladitya Dey**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

The work reported here is a project to design audio amplifier for 16 Ω, 100 pF load. Two amplifiers have been designed, one with a 0.9 V common mode voltage and the other with 0V common mode voltage. A negative voltage converter is also designed to supply the negative voltage to the ground centered opamp. Methods to reduce distortion in the direct drive amplifier(combination of ground centered opamp and negative voltage converter) are also discussed. The amplifiers designed are three stage nested Miller compensated amplifiers and are designed in 0.18 μm UMC-CMOS 6 metal layer technology. The opamp with 0.9 V common mode voltage occupies an area of 73125 μm^2 and have power consumption of 1.39 mW. DC-gain is 95.13 dB, phase margin is 81.83^0, UGF is 1.752 MHz, output swing is $0.15V \leq Vout \leq 1.65V$, integrated opamp noise@70^0(20 Hz − 24 kHz) is 3.28 μV, slew rate is ± 100 mV/μs, THD@ 1 kHz input is −89.08 dB and compensation capacitor is 30 pF. The opamp with 0 V common mode voltage occupies an area of 90710 μm^2 and have power consumption of 2.65 mW while using $\pm 1.8V$. DC-gain is 106.3 dB, phase margin is 71.9^0, UGF is 2.177 MHz, output swing is $-1.6V \leq Vout \leq 1.6V$, integrated opamp noise@70^0(20 Hz − 24 kHz) is 3.42 μV, slew rate is ± 150 mV/μs, THD@ 1 kHz input is −85.28 dB and compensation capacitor is 30 pF. The negative voltage converter is based on switched capacitor architecture. With two capacitors of 2 μF and 4 μF and clock frequency of 500 kHz the output voltage is −1.6 V with 88.5 % efficiency. It is shown that the two external capacitor values can further be reduced by using higher clock frequency without degrading the efficiency much.

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CHAPTER 1

Introduction

The work reported here is a project to design audio amplifier for 16 Ω load. Two amplifier have been designed, one with 0.9 V common mode voltage which is operated using single 1.8 V supply and the other have 0 V common mode voltage and thus need to be operated using dual supply. A negative voltage converter is designed to supply the negative voltage to the ground centered opamp. Methods to reduce distortion in the direct drive amplifier(combination of ground centered opamp and negative voltage converter) are also discussed in subsequent chapters. The technology used for the design is UMC 0.18 μm CMOS process.

1.1 Organization of the thesis

Chapter 2 discusses different inductor based negative voltage converter architectures.

Chapter 3 discusses different charge pump based negative voltage converter topology comparison, design issues and simulation results.

Chapter 4 discusses the modeling of three stage opamp for required specification.

Chapter 5 discusses the design of single supply opamp with 0.9 V common mode voltage.

Chapter 6 discusses the simulation result of single supply opamp with 0.9 V common mode voltage.

Chapter 7 discusses the design of dual supply ground centered opamp.

Chapter 8 discusses the simulation result of dual supply ground centered opamp.

Chapter 9 discusses the simulation result for the direct drive amplifier.

Chapter 10 concludes the thesis with future scope discussion.

CHAPTER 2

Analysis of different inductor based negative voltage converters

2.1 Buck-boost converter

In a step-down/step-up or buck-boost converter, a negative polarity output with respect to the common terminal of the input voltage is obtained. The output voltage magnitude can either be higher or lower than the input voltage depending upon the duty cycle(D) of the switch. [1]

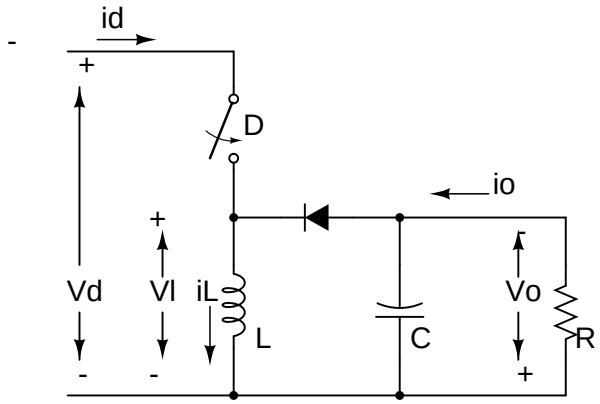


Figure 2.1: Buck-boost converter.

2.1.1 Continuous-conduction mode (CCM)

Fig. 2.2 shows the waveform for continuous-conduction mode(CCM) where the inductor current flows continuously(i.e it never goes to zero). Equating the inductor voltage over one period of time to zero gives

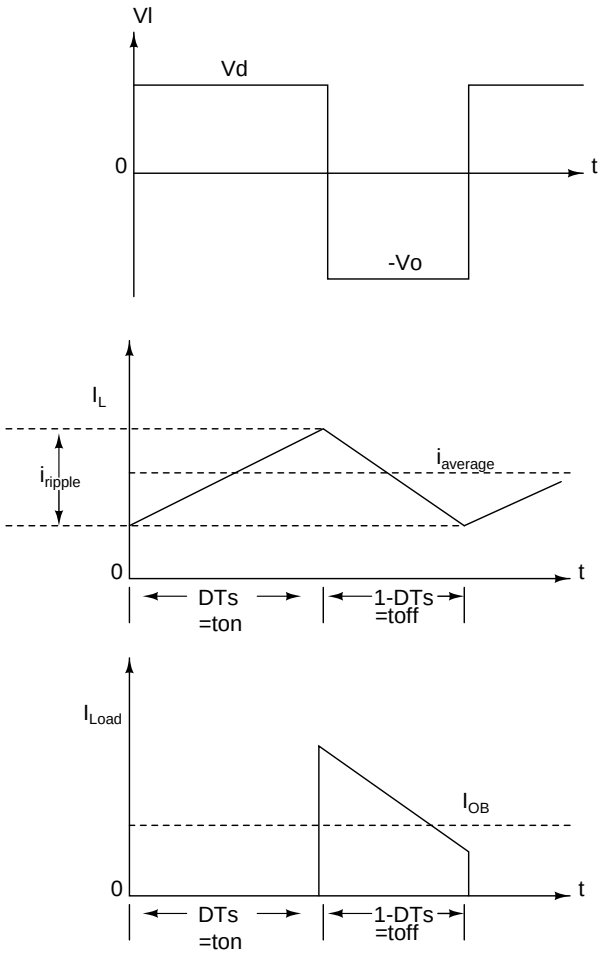


Figure 2.2: Buck-boost converter waveforms in continuous conduction mode.

$$V_d D T_s + (-Vo)(1-D)T_s = 0 \tag{2.1}$$

$$\frac{V_o}{V_d} = \frac{D}{(1-D)} \tag{2.2}$$

Also, equating input and output power gives

$$\frac{I_o}{I_d} = \frac{(1-D)}{D} \tag{2.3}$$

$$i_{ripple} = \frac{V_d D}{2Lf} \tag{2.4}$$

The inductors that can be integrated is of nH range. Assuming the following

$$V_o = -V_d = -1.8\,\mathrm{V} \tag{2.5}$$

$$L = 5\,\mathrm{nF} \tag{2.6}$$

$$f = \frac{1}{T_s} = 500\,\mathrm{MHz} \tag{2.7}$$

we get

$$D = 0.5 \tag{2.8}$$

$$i_{ripple} = 360\,\mathrm{mA} \tag{2.9}$$

2.1.2 Boundary between continuous and discontinuous conduction

Fig. 2.3 shows the waveform at the edge of continuous-conduction mode(CCM) where the inductor current(i_L) goes to zero at the end of off interval. I_{LB} and $I_{LB,max}$ are the average and maximum inductor current and I_{OB} and $I_{OB,max}$ be the average and maximum output current.

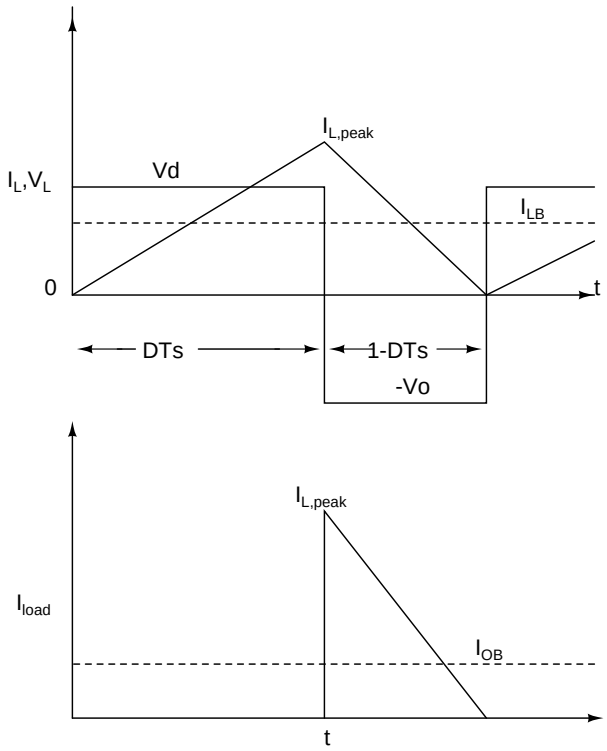


Figure 2.3: Buck-boost converter : Boundary of continuous and discontinuous conduction

From the Fig. 2.3

$$
\begin{aligned}
I_{LB} &= \frac{i_{Lpeak}}{2} && (2.10)\\
&= \frac{T_s V_d}{2L} D && (2.11)\\
&= \frac{T_s V_o}{2L}(1-D) && (2.12)\\
I_{OB} &= \frac{T_s V_o}{2L}(1-D)^2 && (2.13)
\end{aligned}
$$

from the previous example, $i_{ripple} = i_{Lpeak}$, so the minimum average inductor current to keep it in CCM is

$$
\begin{aligned}
I_{LB} &= I_{LB,max}(1-D) && (2.14)\\
I_{LB} &= \frac{360\,\mathrm{mA}}{2} = 180\,\mathrm{mA} && (2.15)
\end{aligned}
$$

and minimum average load current in this mode is

$$I_{OB} = I_{OB,max}(1-D)^2 \tag{2.16}$$

$$I_{OB} = 90\,\text{mA} \tag{2.17}$$

For average load current greater than 90 mA, the diode will always be forward biased for the entire off duration, thus it can be replaced by a switch which has complementary state of the main-switch.

2.1.3 Discontinuous conduction mode

Fig. 2.4 shows the waveform in discontinuous-conduction mode(DCM) where the inductor current(i_L) is zero for a finite time.

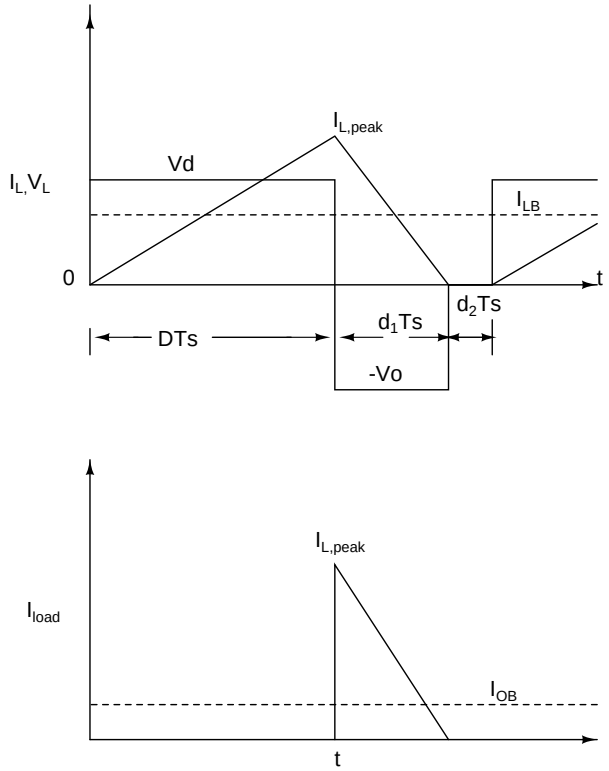


Figure 2.4: Buck-boost converter : Discontinuous conduction mode

Integrating the inductor voltage over one time period to zero gives

$$V_d D T_s + (-Vo) d_1 T_s = 0 \tag{2.18}$$

$$\frac{V_o}{V_d} = \frac{D}{d_1} \tag{2.19}$$

Also, equating input and output power gives

$$\frac{I_o}{I_d} = \frac{d_1}{D} \tag{2.20}$$

and from Fig. 2.4 the average inductor current is given by

$$I_{LB} = \frac{V_d}{2L} D T_s (D + d_1) \tag{2.21}$$

From the previous example, for average inductor current less than 180 mA the diode will not be forward biased for the entire off duration. As it gradually become reverse biased and stay reversed biased during the duration d_2, it cannot directly be replaced by a switch if the converter operates in this mode.

In Buck-Boost converter we see that the output current does not flow for the entire time period. At the output we need an output capacitor to sink the load current when the converter does not sink any current. The value of this capacitor is chosen such that the output voltage ripple is within the limit specified. In the next subsection, a modified Buck converter architecture is considered which eliminates the ripple in the output current an thus the output capacitor can be made very small and thus can be made onchip.

2.2 Buck converter

The buck converter is used to step-down any voltage. Simple buck converter operating in continuous conduction mode(CCM) is shown in Fig. 2.5. In CCM the diode can be replaced by a complementary switch. Equating average voltage

across the inductor to zero we get

$$(V_d - V_o)T_{on} = (-V_o)T_{off} \tag{2.22}$$

$$V_o = V_d \frac{T_{on}}{T_{off}} = V_d D \tag{2.23}$$

The output current I_O is equal to the inductor current I_L.

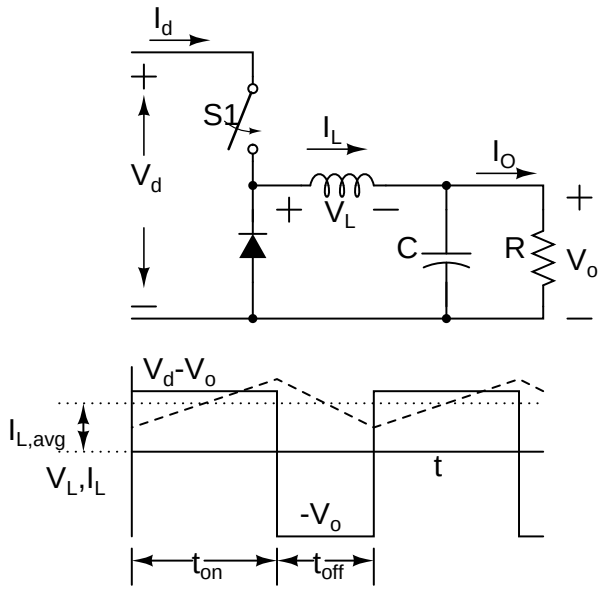


Figure 2.5: Buck converter in continuous conduction mode

The ripple in the output current can be canceled using a secondary inductor branch as shown in the figure Fig. 2.6[2]. The series capacitor C_s blocks any dc current to flow through the secondary branch. Thus only the ripple current with average value of zero will flow through the secondary branch. Also the primary and secondary branch have complementary clocking. Thus the ripple at the output current I_O become zero. Thus the output capacitor C_p can be made very small and made onchip. Another advantage of this topology is that the two inductors can be designed to have strong coupling. Thus the effective inductance per unit area can be increased.

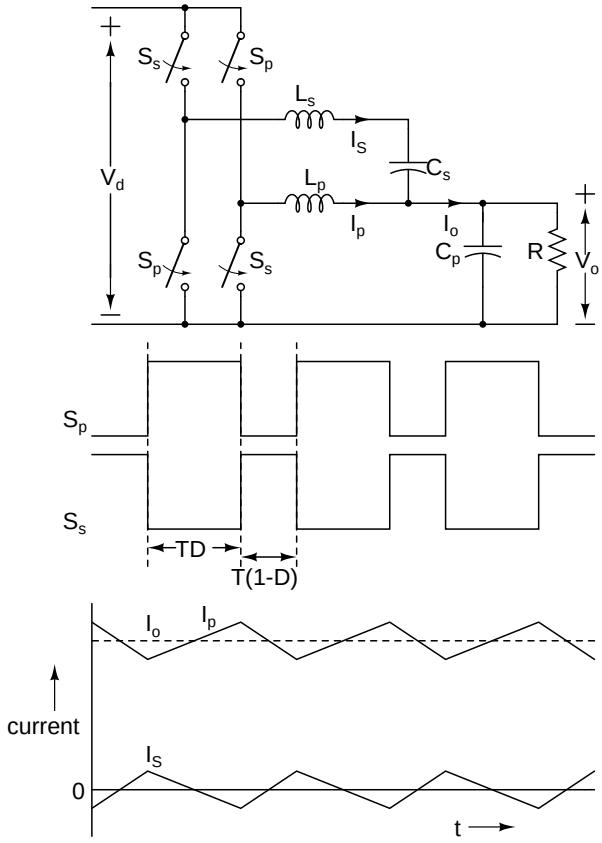


Figure 2.6: Stacked buck converter

2.3 Buck-boost converter modified architecture

In this section the different architectures for implementing ripple cancelation in buck-boost converter is discussed. The modified architectures were implemented using the same principle of current cancelation using a secondary branch as in the buck converter discussed previously. In this modification a secondary branch

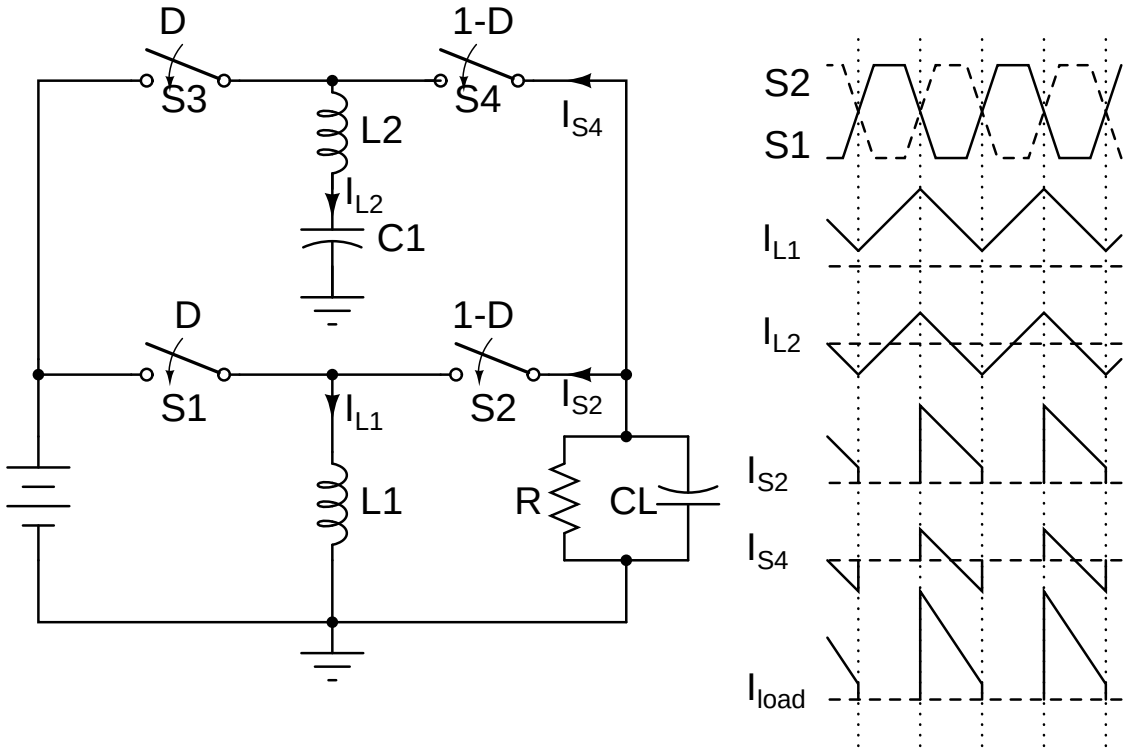


Figure 2.7: Modified buck-boost

consisting of S_3,S_4,L_2 and C_1 is introduced as shown in the Fig. 2.7. The average inductor current through L_2 is zero. Here S_1 and S_3 are operated using same clock and also S_2 and S_4 are operated using same complementary clock. In this architecture the ripple in the output current is doubled instead of getting canceled. Now, if S_3 and S_4 clocks are interchanged as shown in the Fig. 2.8 it also introduces extra ripple. It is clear from the above analysis that current through S_2 is decreasing in nature. Current ripple cancelation require increasing nature of current through S_4 during this period. Since in the above modified architectures I_{s4} is of decreasing nature, ripple cancelation is not possible. Thus addition of an additional inductor serves no improvement.

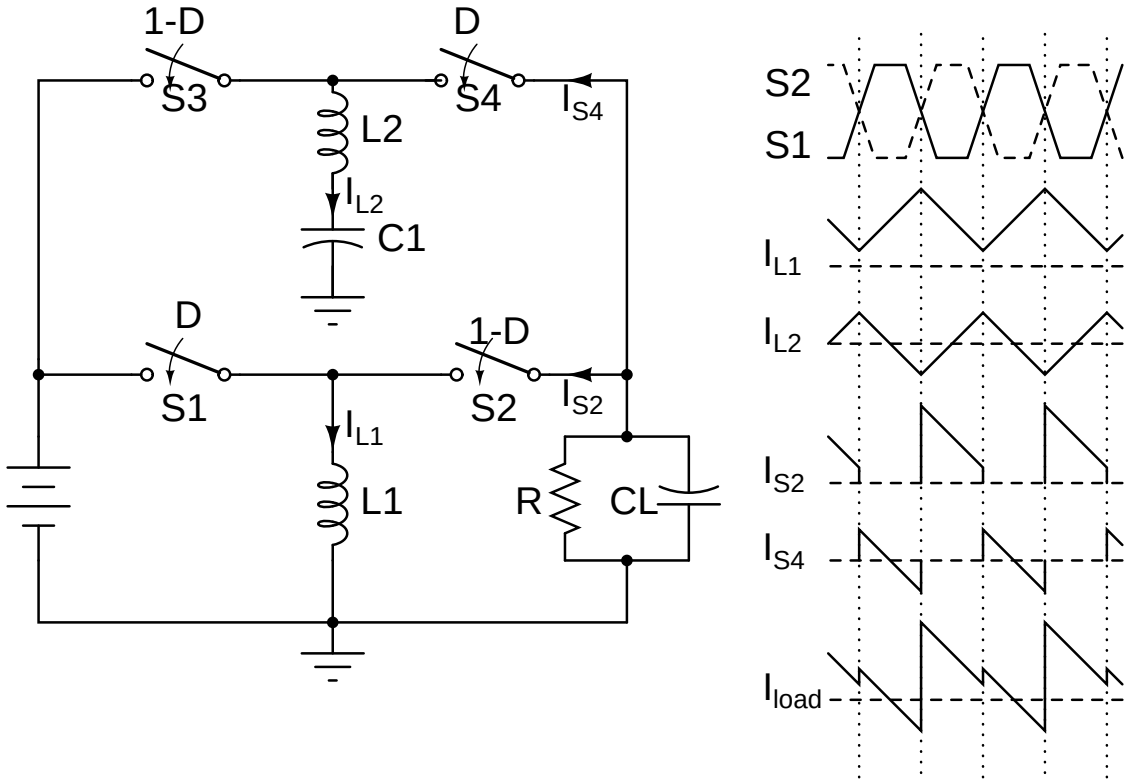


Figure 2.8: Another modified architecture of buck boost

CHAPTER 3

Charge pump based negative voltage converters

3.1 Basic operation of charge pump based negative voltage converter

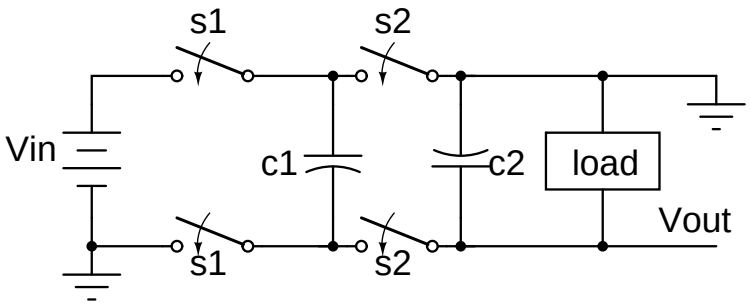


Figure 3.1: Basic operation of charge pump based negative voltage converter.

The basic operating principle of switched capacitor voltage inverter is shown in Fig. 3.1. Here S1 and S2 are complementary switches. The charge pump capacitor, C1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle - defined as the ratio of charging time for C1 to the entire switching cycle time is usually 50%, because that generally yields the optimal charge transfer efficiency. After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During

the time the pump capacitor is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz. The basic inverter circuit provides no output voltage regulation. However, techniques exist to add regulated capability and can also be implemented.

3.2 Different architectures of charge pump based negative voltage converter

There are different architectures for charge pump based negative voltage converter as mentioned below. Each one has its own advantages and drawbacks.

- Simple negative voltage converter.
- Nakagome charge pump based architecture.
- Modifications of Nakagome charge pump based architecture.

3.2.1 Simple negative voltage converter architecture

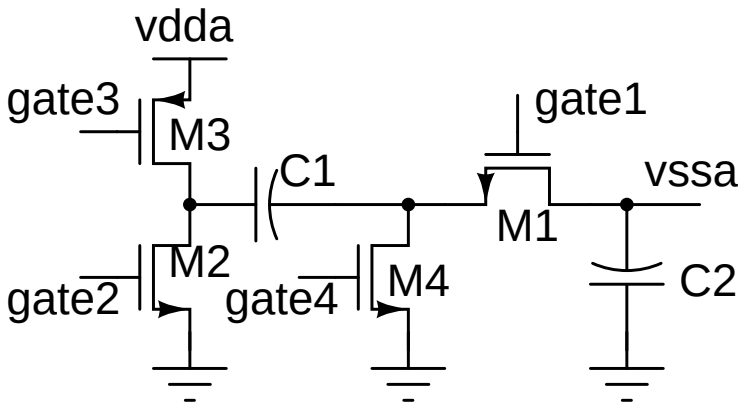


Figure 3.2: Simple negative voltage converter architecture.

The operating principle is very simple in this architecture. During one phase switches M3 and M4 are turned on and M1 and M2 are off. The capacitor C1 is charged to Vdd.In the next phase of the clock M1 and M2 are turned on and M3 and M4 are turned off. Thus C1 is connected across the load capacitor C2. To avoid any crowbar current or short circuit current during the transition, the switches must be operated in a particular sequence. While turning off M1 and M2 and turning on M3 and M4 the following order is followed.

- Turn off M1
- Turn off M2
- Turn on M4
- Turn on M3

Also, while turning on M1 and M2 and turning off M3 and M4,the reverse order is followed.

- Turn off M3
- Turn off M4
- Turn on M2
- Turn on M1

3.2.2 Nakagome charge pump based architecture

Now we discuss a voltage inverter based on the cross-coupled configuration of Fig. 3.3. Substrate connections for all devices are indicated in the figure. NMOS device share the common substrate, which is connected to Vcap, while PMOS devices are connected to Vdd. Two opposite-phase clock signals clk and clk-bar shown in Fig. 3.3 are used to drive CMOS inverters(not shown) used as buffer to drive the capacitors C0 and C1. The drive signals at nodes clock and clock-bar are shown as non-overlapping low state opposite-phase signals i.e. there are short time intervals when both clock and clock-bar are at Vdd volts. PMOS pump devices m0 and m1 have cross-coupled gates that swing between zero and -Vdd. Since the drive signals at nodes clock,clock-bar are nonoverlapping, m0 and m1

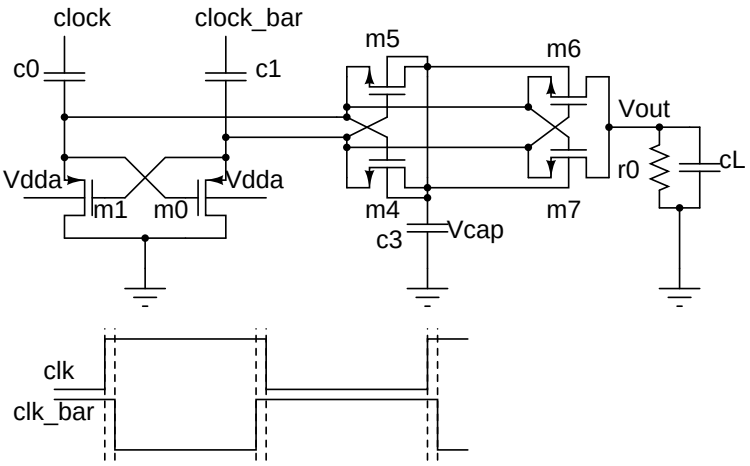


Figure 3.3: Nakagome charge pump based inverter architecture.

are never on at the same time. The energy-transfer pump capacitors C0, C1 are charged through m0, m1 to +Vdd in opposite phases of the clock signals. Series NMOS switches m6, m7 also have cross-coupled gates and are used to pass -Vdd to the output. In addition, auxiliary NMOS devices m4,m5 and capacitor C3 are used to bias the common p-substrate of the NMOS devices at voltage -Vdd. Since C3 is unloaded, Vcap is always less than or equal to Vout, which ensures that the source and drain to p-substrate junctions of the NMOS devices are always reverse biased. This is important because forward bias of these junctions may cause lossy discharge of the output or latch-up condition through the p-substrate of the chip. A problem with the circuit shown in Fig. 3.3 is that during the intervals when both clock and clock-bar are close to Vdd, both NMOS m6,m7 are turned on at the same time. As a result, undesirable lossy discharge of the output filter capacitor C_L occurs. One may attempt to reduce the time intervals when clock and clock-bar are simultaneously high, or even to slightly overlap the two drive signals. However, this contradicts the desirable timing of the drive waveforms for the PMOS pump devices m0 and m1, and may lead to the case when both m0 and m1 are turned on at the same time. This would result in lossy discharge of C0, C1 back to Gnd. The problem with exact timing of the drive signals clock and clock-bar is particularly important at high clock frequencies (in the MHz range and above), because the losses incurred due to the undesirable conduction of the cross-coupled device effectively increase the switching losses in the converter. There are some

alternative architecture for Nakagome charge pump which eliminates this problem as discussed in the next subsection.

3.2.3 Modifications of Nakagome charge pump based architecture

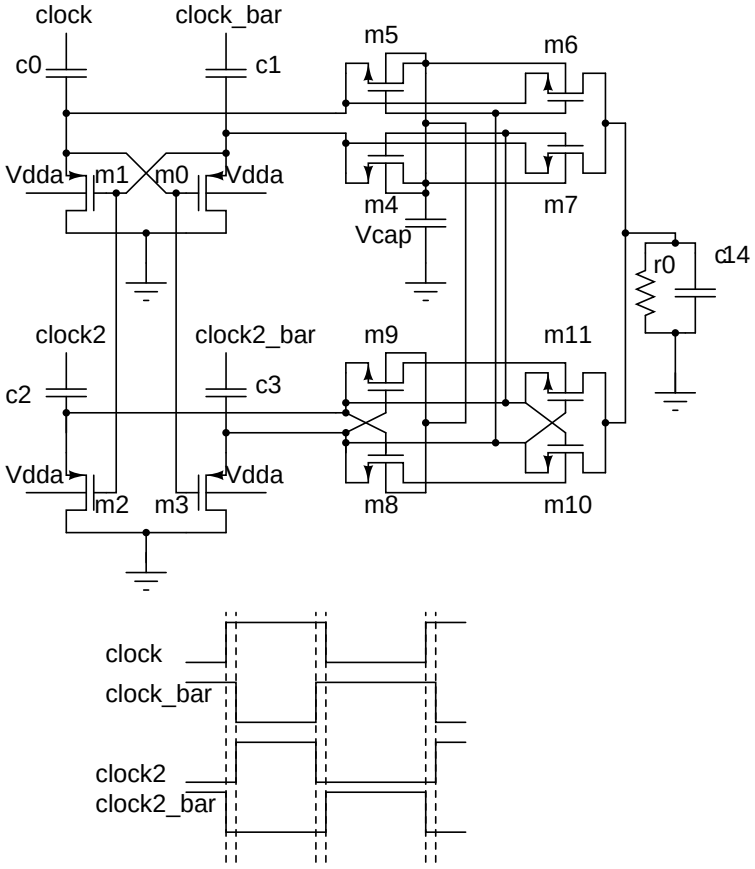


Figure 3.4: Modification 1 of Nakagome charge pump based inverter architecture.

In order to alleviate the problem observed in the circuit of Fig. 3.3 another cross-coupled pump is added as shown in the Fig. 3.4[3]. The second cross-coupled pump is driven by non-overlapping high state drive signals at nodes clock2 and clock2-bar. The two pumps are coupled so that PMOS devices(m0,m1,m2,m3), in both pumps are off during the overlap duration of signals clock and clock-bar. The NMOS devices(m6,m7,m10,m11) in both pumps are off during the overlap duration of signals clock2 and clock2-bar as shown in Fig. 3.4. As a result of this arrangement, possible lossy simultaneous conduction of the pairs (m0,m1),

(m2,m3), (m6,m7), and (m10,m11) are eliminated.The disadvantage of this architecture is the increased number of capacitors.

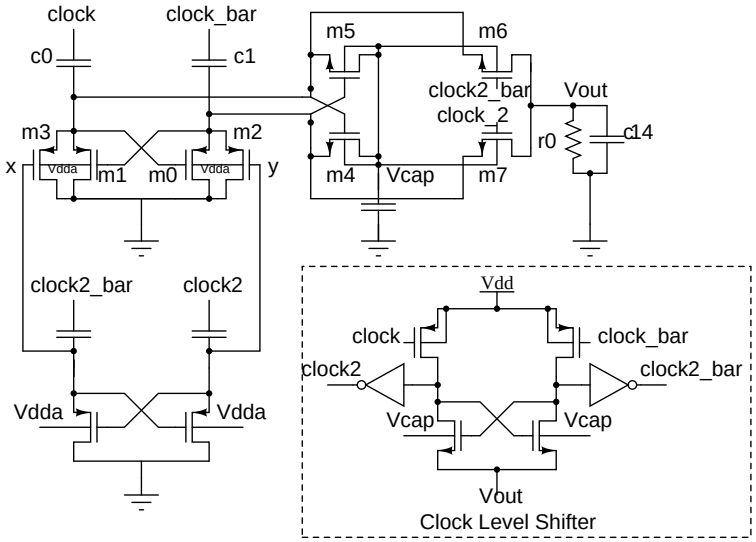


Figure 3.5: Modification 2 of Nakagome charge pump based inverter architecture.

Up to now the gate signals of the two series switches (m6,m7) were between and 0 and -Vdd (Fig. 3.3). The conductance is greatly improved if these signals can range between 0 and -2Vdd. This is very important for supply voltages under 1.8 V. Assuming a Vdd of 1.8 V and Threshold voltage V_T of 0.7 V, the overdrive voltage is 1.1 V. Driving these switches between 0 and -2Vdd boosts the overdrive voltage to 2.9V, thus the ON resistance is reduced by a significant amount.The entire charge-pump circuit is shown in Fig. 3.5[4]. The clock level shifter circuit is supplied from Vdd and the output voltage of the charge pump. The output of the level shifter is the level shifted version of the clock which varies from Vdd to -Vdd. The gates of m2 and m3 are driven between 0 and -2Vdd. This could be achieved by driving the gates of m2 and m3 from an auxiliary charge pump as shown in the Fig. 3.5 which is driven by Vdd to -Vdd clock signals. In practice, the cross coupling of m0 and m1 shown in Fig. 3.5 is necessary to start up the charge pump. The disadvantage of the circuit is increased number of capacitance. Also, since x and y nodes vary from 0 to -2Vdd, this technique must be restricted to input voltage below one third of the maximum voltage specified in the process.

3.3 Design of unregulated charge pump based negative voltage converter

The simple architecture is chosen for implementation for its simplicity which facilitates the layout process and has fewer capacitors. The relation between operating frequency, output voltage ripple and the value of the capacitors C_1 and C_2 are given below. Let ΔV be the limit on the output voltage ripple specification and f be the frequency of operation. When C_1 is connected between Vdd and ground, the output capacitor supplies the entire load current. Thus

$$C_2 \Delta V = i_{load} t_{off} \tag{3.1}$$

$$\tag{3.2}$$

assuming 50% duty cycle, $t_{on} = t_{off} = \frac{1}{2f}$ thus we have

$$C_2 = \frac{i_{load}}{2f\Delta V} \tag{3.3}$$

$$\tag{3.4}$$

In this design

- $\Delta V = 50\,\mathrm{mV}$
- $i_{out} = \frac{1.6\,V}{16\,\Omega} = 100\,\mathrm{mA}$

thus from the above equation we get

$$C_2 f = 1 \tag{3.5}$$

Thus for 200 kHz frequency of operation $C_2 = 5\,\mu F$ and for 1 MHz frequency of operation $C_2 = 1\,\mu F$.Now the value of C_1 is chosen such that it has the same voltage ripple as the output capacitor.Now during the charging period of C_1 the average current flowing through it is $2i_{load}$.So C_1 is taken to be the double of C_2.

This unregulated charge pump circuit based negative voltage converter mainly consists of two parts

- The switches.
- Switch control signal generation

3.3.1 The switches

The main switches of the charge pump are shown in Fig. 3.6 with the sizes. The sizing is done so that the output voltage is about $-1.6\,\mathrm{V}$ at full load current. The swing of gate voltages of the transistors are mentioned below.

- $gate_1$ from Vdd to Vss
- $gate_2$ from Vdd to Gnd
- $gate_3$ from Vdd to Vss
- $gate_4$ from Vdd to Vss

The gate to source voltage(v_{gs}) during the on time is 2Vdd for $gate_1$ and $gate_3$. For $gate_2$ and $gate_4$ v_{gs} is only Vdd. To decrease the On resistance for M_2 and M_4 for the same dimension the gate voltages for these two transistors can be boosted. But then the voltage range inside the chip will be 3Vdd. This will limit the maximum Vdd that can be applied in a particular technology. So, these two gate voltages are not boosted.

3.3.2 Switch control signal generation

The operating sequence for the switches is mentioned in the previous section.The gate swing of M2 is from Vdd to Gnd. All other gate voltages swing from Vdd to the most negative voltage Vss(i.e. the output voltage of the converter). External reference clock signal varies from Vdd to Gnd. We need to shift the clock voltage swing level from Vdd to Vss for proper operation.Thus a level shifter is used to change the clock signal swing from Vdd-Gnd to Vdd-Vss. The level shifter is shown in the Fig. 3.7. Before connecting to the level shifter the clock signal passes through a non-overlap generator shown in Fig. 3.8. for generating complementary non-overlapping low signal required for the level shifter.Complementary

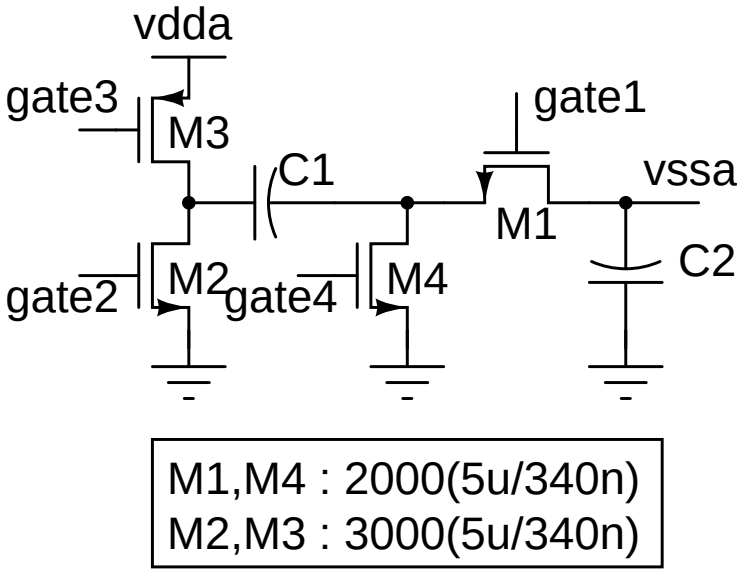


Figure 3.6: The switches of the charge pump.

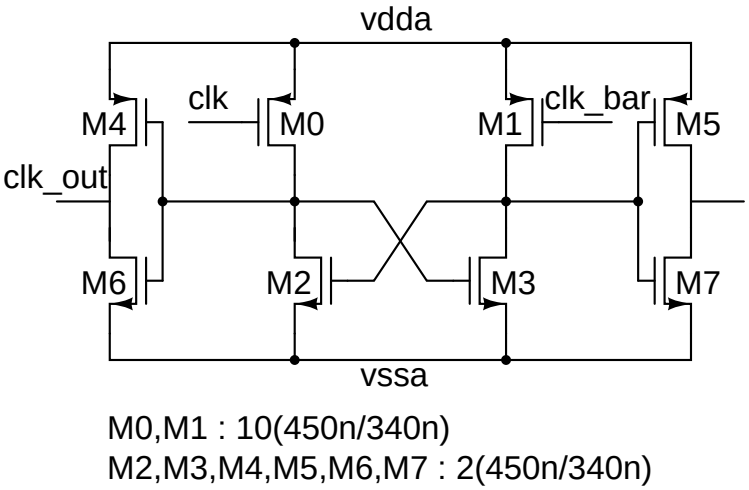


Figure 3.7: Level shifter for the clock signal.

non-overlapping low clocks applied to the level shifter eliminates the possibility of crowbar current in the level shifter.This non-overlap generator is supplied from Vdd and Gnd. Now the output from the level-shifter the clock from Vdd

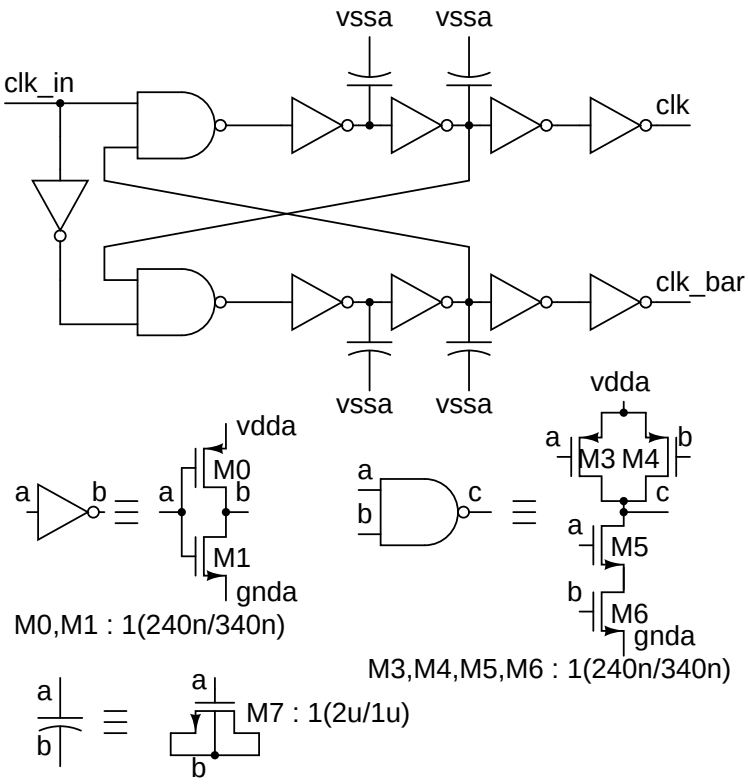


Figure 3.8: Non-overlap generator for the level shifter.

to Vss.This is fed to a chain of min sized inverters as shown in the Fig. 3.9to get the input clock with different delays.These delayed clocks are OR-ed together taking from appropriate taps to get gate2 gate3 and gate4 signals with required delays.gate1 signal is directly obtained from the middle of the chain.MOS capacitors are included in the chain to increase the delay in the chain without further increase in the number of inverters in the chain.The delays for consecutive gate signal changes are kept as 2ns.So total transition duration for the four gate signals turns out to be 6ns.When the charge pump is operated at 1MHz then the transition time is only 1.2% of the steady on or off duration.This circuit is operated between Vdd and Vss. The gate control signals generated from the delay chain is fed to the respective gats through a buffer chain for each gate control signal.Each of these buffer chain as shown in Fig. 3.10 has the same delay.The buffer chain for the gate2 should vary from Vdd to Gnd.So the source of the last inverter NMOS

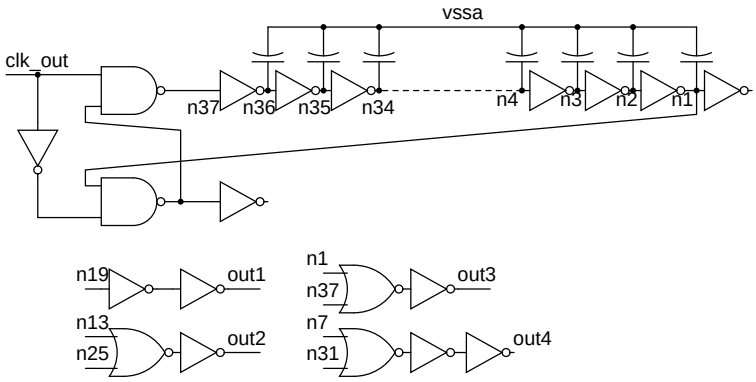


Figure 3.9: Non-overlap generator for the gate controlling signal.

is connected to Gnd and the NMOS is resized to have the same pull-down time as in the other buffer-chain.All the other inverters in the buffers are supplied from Vdd and Vss.

The output of the buffer chain is shown in the Fig. 3.11 and Fig. 3.12 .The dead-time between any two gate voltage change is about 2ns.

3.4 Performance analysis of the negative voltage converter

The variation of the output voltage for different load resistances are plotted in the Fig. 3.13. The efficiency of the negative voltage converter for different values of load resistance is plotted in the Fig. 3.14.

The efficiency of the negative voltage converter for different values of load current is plotted in the Fig. 3.15.

The external capacitor values can be decreased by operating the charge pump at higher clock frequency. But at very high frequency switching loss may increase significantly. Thus the negative voltage converter is operated at different clock frequency and the performance parameters are analyzed. The capacitors C_1 and C_2 are also varied accordingly to fix the output voltage ripple at 50 mV. The Fig. 3.16 shows the output voltage variation with frequency.As it is clear from the

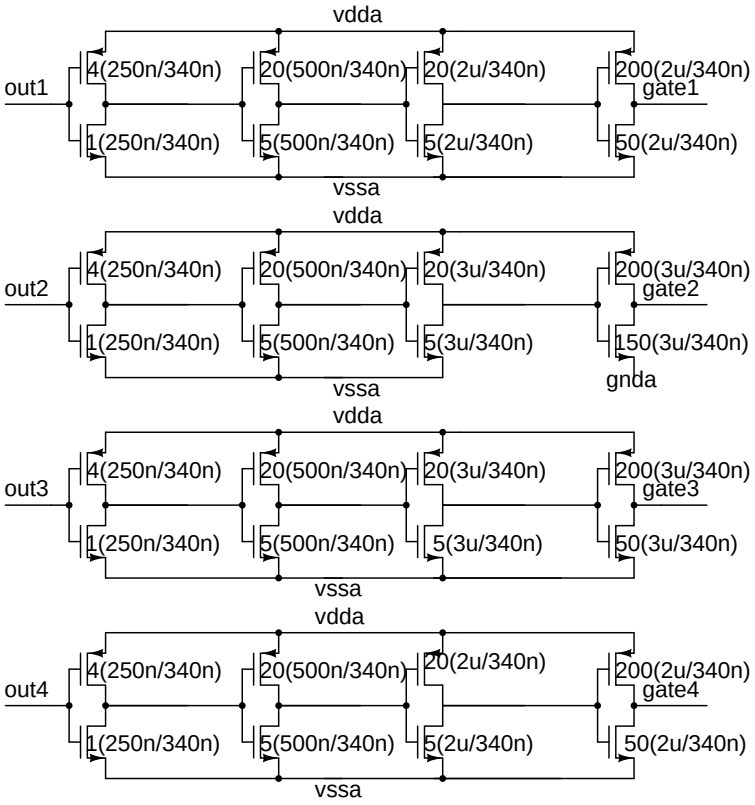


Figure 3.10: Buffer stage for the gate controlling signal.

plot, upto 2 MHz frequency of operation the output voltage does not show amy significant degradation.

The Fig. 3.16 shows the variation of efficiency with frequency. It is also clear from the plot that this charge pump can be operated over a wide frequency range without significant degradation in efficiency.

The following tables tabulates the capacitor values used at different frequencies, output voltage, efficiency, power dissipation in different sections of the circuit and total input and output power. It is observed from this analysis that power dissipation in the clock and buffer circuit increases proportionally with the frequency. Since clock and buffer circuit consume very low power compared to the main switches at rated current, the increased power dissipation in clock and buffer do not affect the overall efficiency of the converter at high frequency. We also see that the losses in the main switches do not increase with frequency. Thus it can be concluded that these switches do not have any significant switching losses. The power loss in these switches are mostly due to finite ON resistance of the switches.

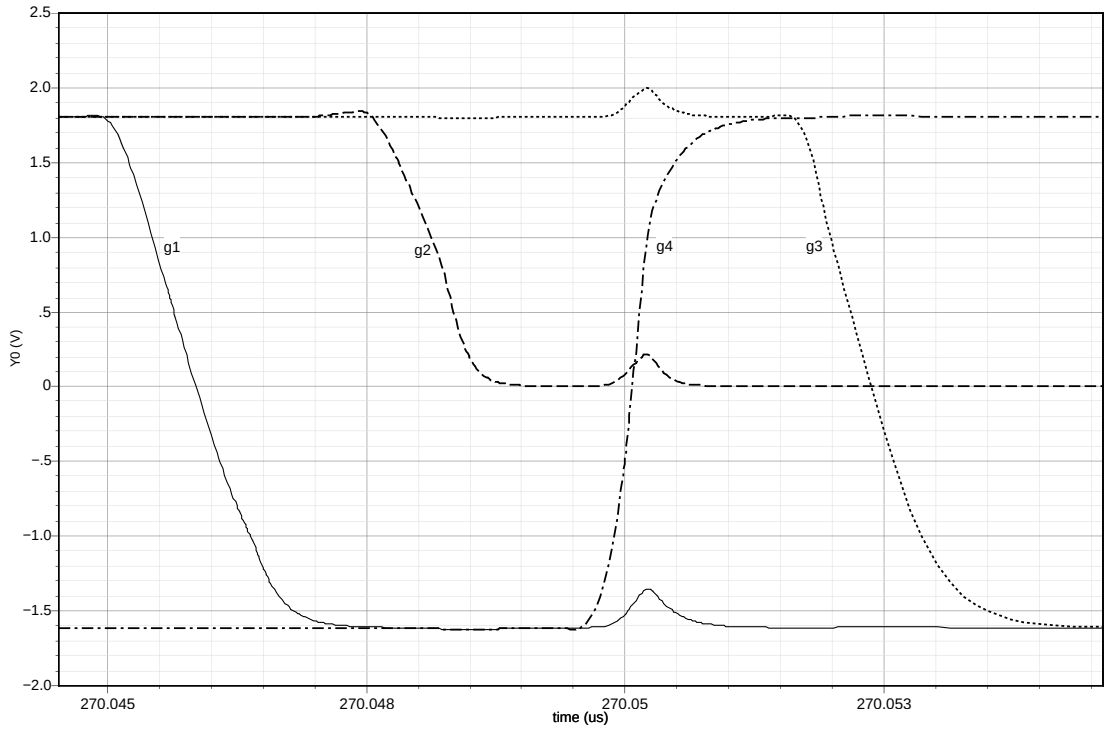


Figure 3.11: Buffer stage output during the transition when C1 gets disconnected from output and connect to Vdd.

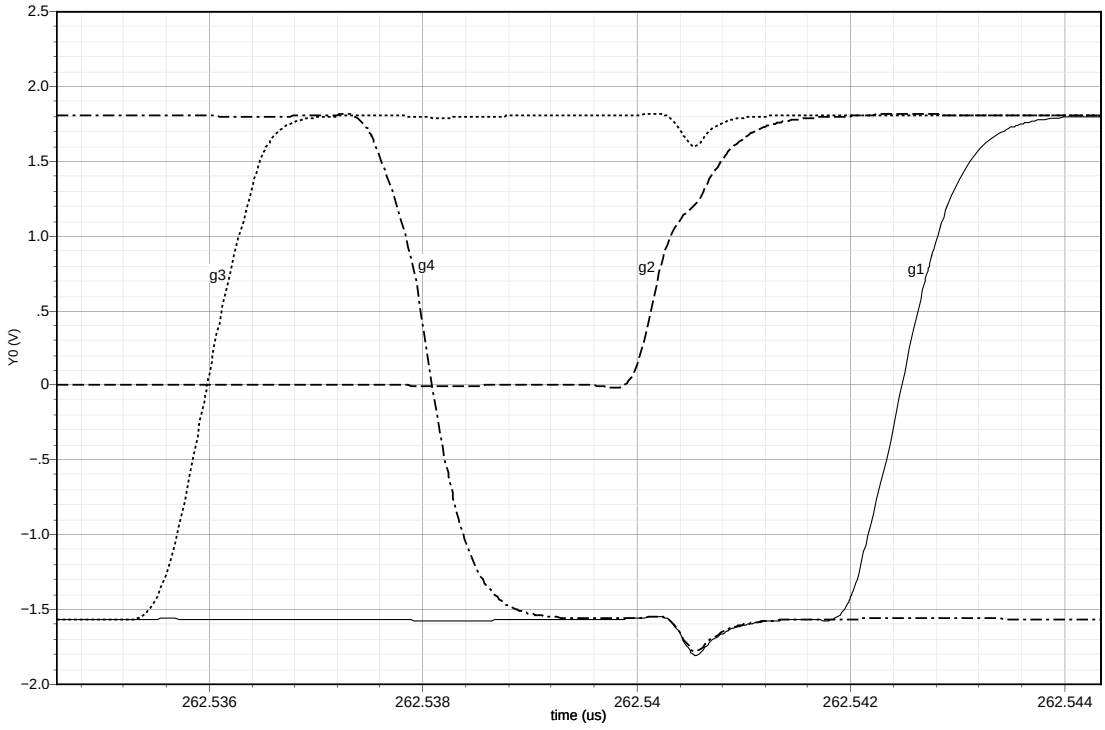


Figure 3.12: Buffer stage output during the transition when C1 gats disconnected from Vdd and connect to the output.

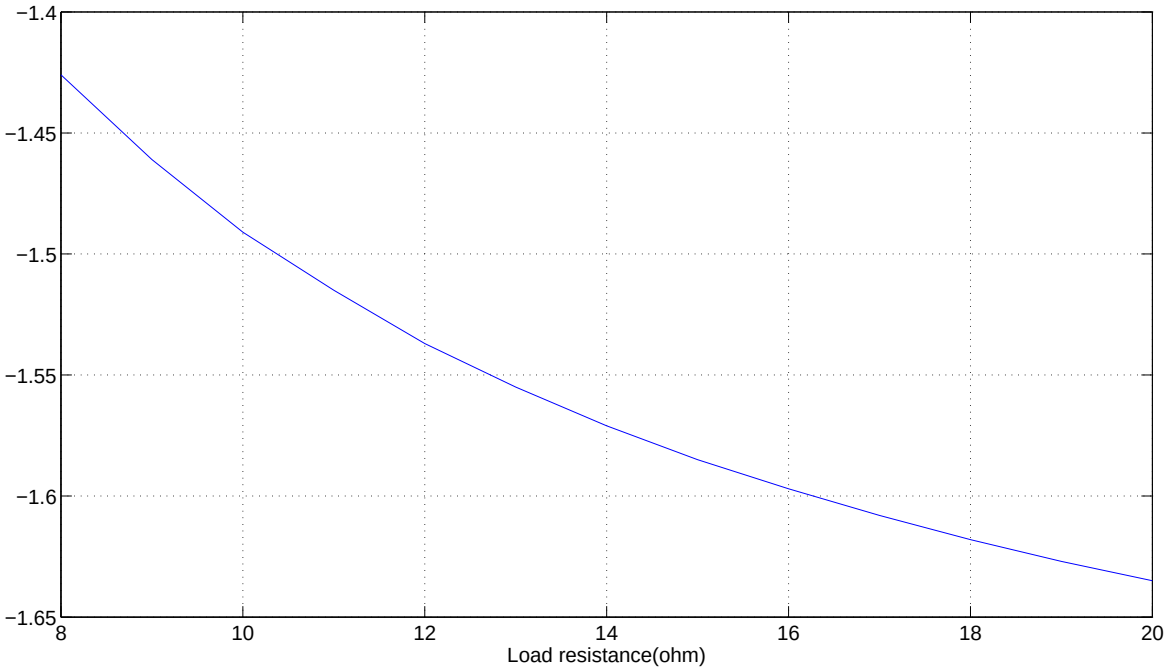


Figure 3.13: Output voltage vs load resistance plot for 16 Ω load.

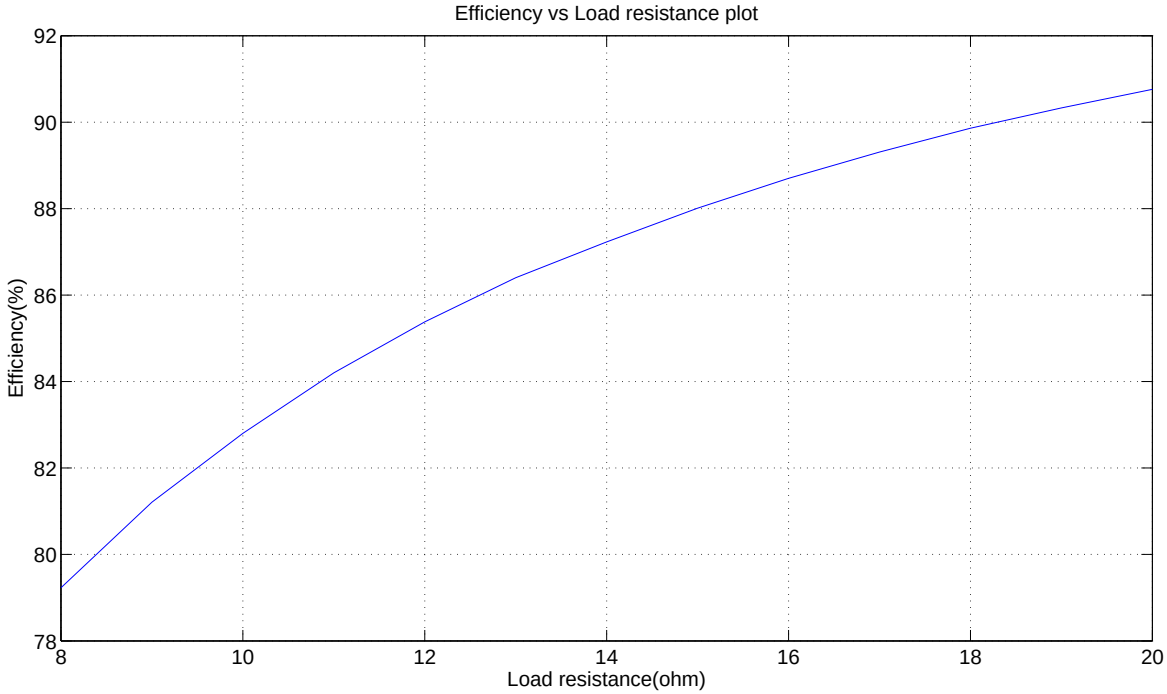


Figure 3.14: Efficiency vs load resistance plot for 16 Ω load.

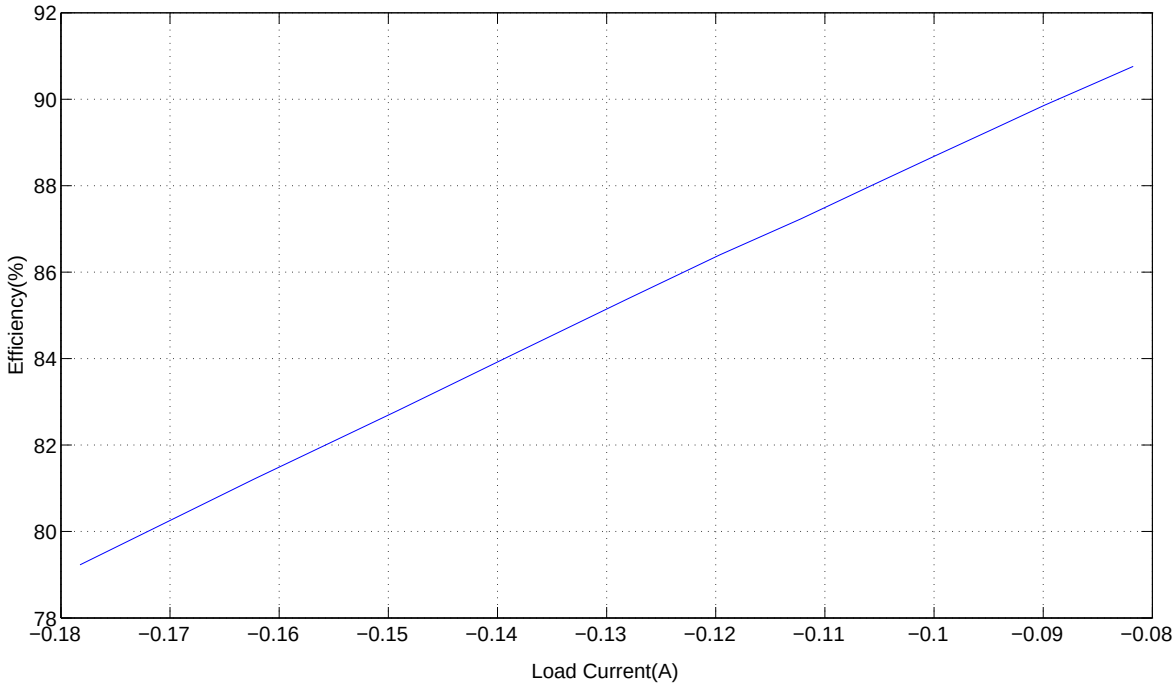


Figure 3.15: Efficiency vs load current plot for 16 Ω load.

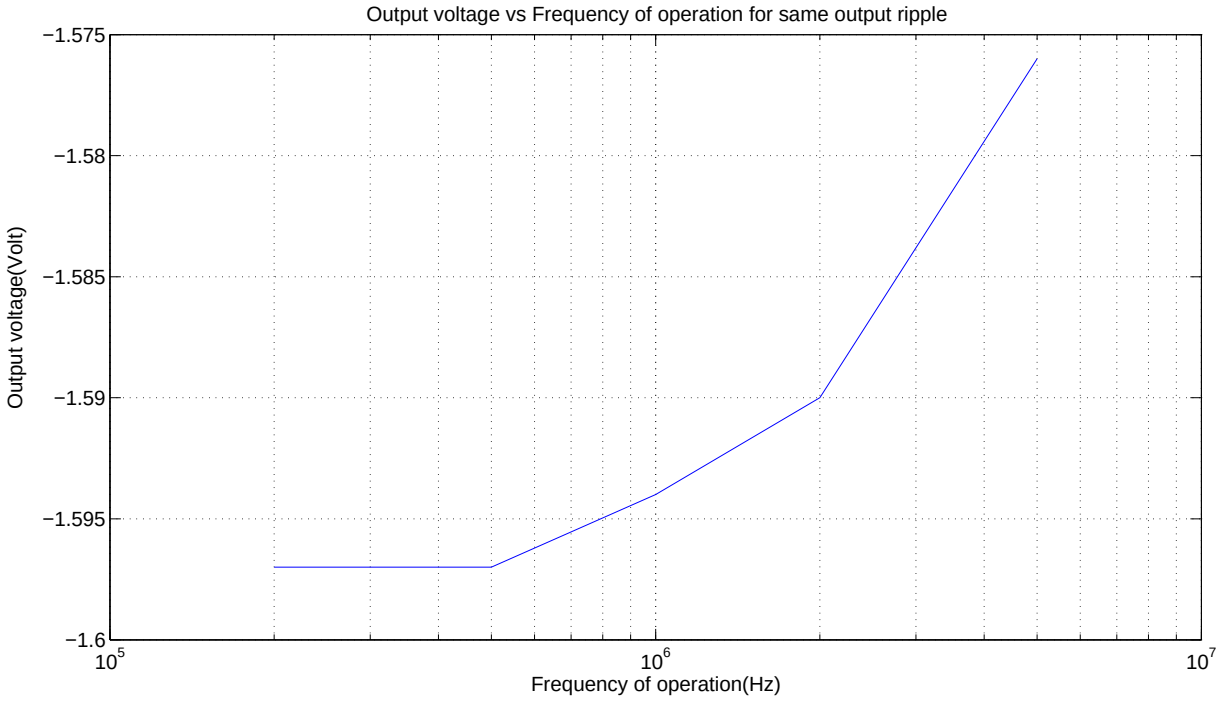


Figure 3.16: Output voltage vs operating frequency plot for 16 Ω load.

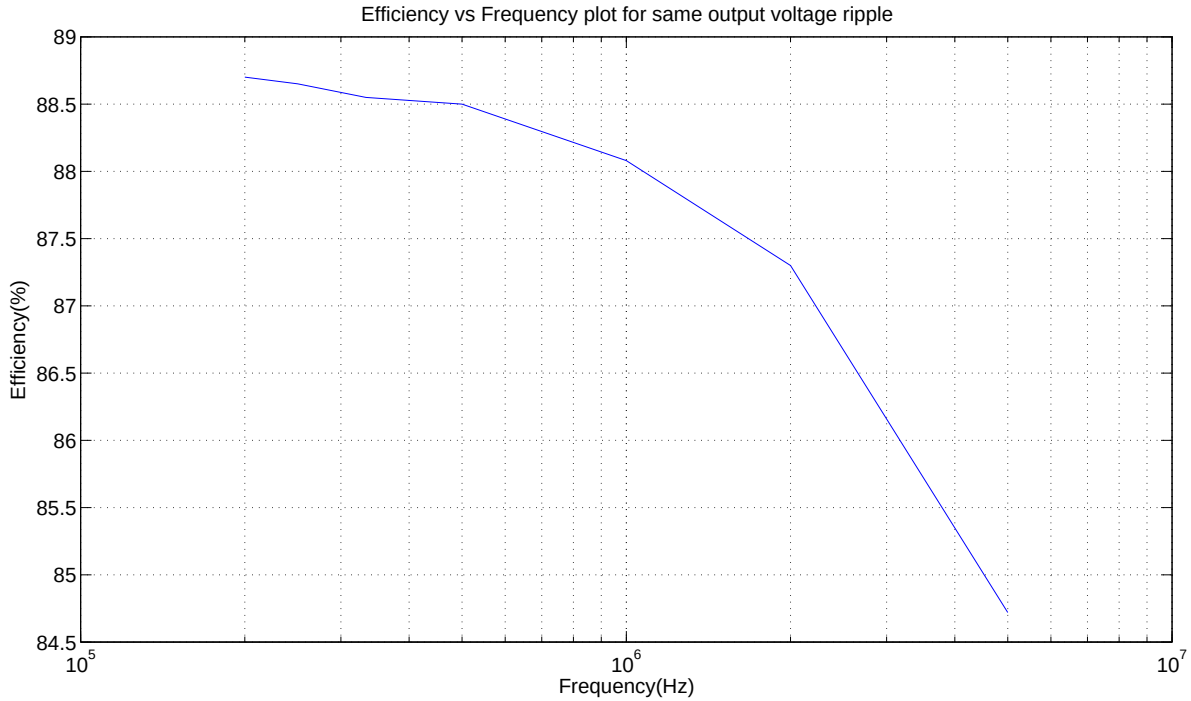


Figure 3.17: Efficiency vs operating frequency plot for 16 Ω load.

Frequency(kHz)	C2(μF)	C1(μF)	vout(V)	efficiency(%)
200	5	10	-1.597	88.7
250	4	8	-1.597	88.65
333.33	3	6	-1.597	88.55
500	2	4	-1.597	88.5
1000	1	2	-1.594	88.08
2000	0.5	1	-1.59	87.3
5000	0.2	0.4	-1.576	84.72

Table 3.1: Efficiency and output voltage at different combination of frequency and capacitor values for 16 Ω load.

Frequency (kHz)	input power (mW)	output power (mW)	switch loss (mW)	Clock circuit power (μW)
200	179.7	159.4	20	204.1
250	179.8	159.4	20.06	255.2
333.33	179.9	159.4	20.14	340.2
500	180	159.3	20.2	510.3
1000	180.4	158.9	20.5	1019
2000	181.1	158.1	21	2034
5000	183.3	155.3	23	5041

Table 3.2: Dissipation at various parts at different frequencies for 16 Ω load.

When the charge pump is operated at 200 kHz clock frequency with $C_1 = 10\,\mu F$ and $C_2 = 5\,\mu F$ with 16 Ω load resistance at the output, the output voltage waveform is shown in Fig. 3.18. It has 50 mV ripple as expected.

3.4.1 Layout considerations

The above results are obtained from schematic simulation of the voltage converter. The layout of this charge pump needed to be done very carefully as the parasitic resistance introduced after layout extraction can significantly degrade the performance. Stacked metal layers can be used to reduce the resistance between two nodes.

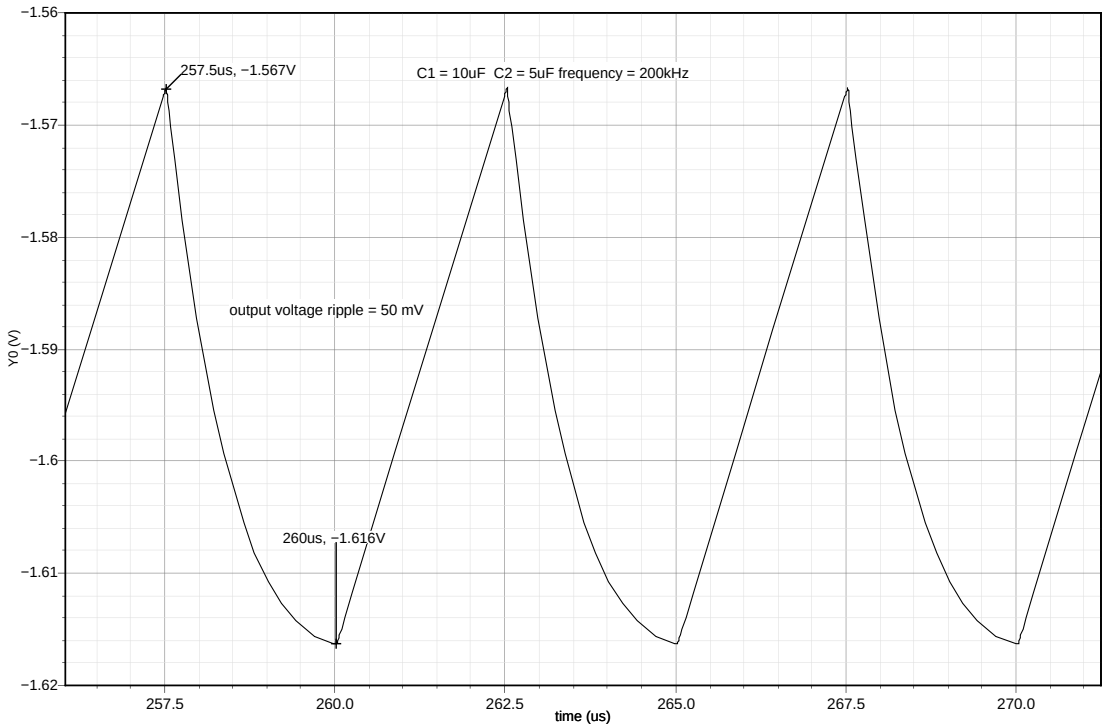


Figure 3.18: Output voltage waveform for 16 Ω load.

CHAPTER 4

Three stage opamp modeling

In this chapter three stage nested Miller compensated opamp is modeled. The parameters g_{m1}, g_{m2}, g_{m3}, g_{ds1}, g_{ds2}, C_1 and C_2 as shown in the Fig. 4.1 are obtained from spice dc analysis. From the model pole zero positions are obtained varying C_{m1}, C_{m2} and R_z. From this analysis a set of values of C_{m1}, C_{m2} and R_z are obtained for which the opamp is properly compensated.

4.0.2 Miller compensated three stage architecture with zero nulling resistance

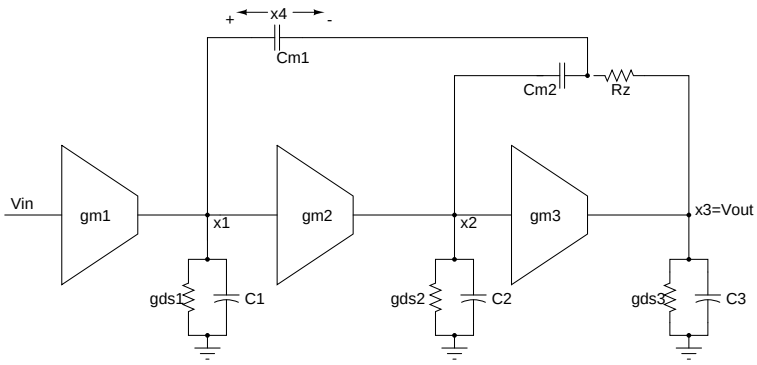


Figure 4.1: Miller compensated three stage amplifier macro-model with zero nulling resistor.

Three stage opamp can be modeled as mentioned in [5].From the macro model of Fig. 4.1 the following equations are obtained.

Here x_1,x_2,x_3,x_4 are four state variables.

$$v_{in}gm_1 = C_1x_1' + gds_1x_1 + C_{m1}x_4' \tag{4.1}$$

$$gm_2x_1 = C_2x_2' + gds_2x_2 + C_{m2}(x_2' - x_1' + x_4') \tag{4.2}$$

$$gm_3x_2 = C_3x_3' + gds_3x_3 + G_z(x_3 - x_1 + x_4) \tag{4.3}$$

$$C_{m1}x_4' + C_{m2}(x_2' - x_1' + x_4') = G_z(x_1 - x_4 - x_3) \tag{4.4}$$

From the above equation state space matrix is formed in the form shown below

$$\begin{bmatrix} x_1' \\ x_2' \\ x_3' \\ x_4' \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} v_{in} \tag{4.5}$$

$$v_{out} = \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 0 \end{bmatrix} v_{in} \tag{4.6}$$

The elements of the matrix A and B are given below.

$$a_{11} = \frac{(C_2((gm_2C_{m1})+(gds_1C_{m2}))+(gds_1C_{m1}(C_2+C_{m2}))-(C_{m1}(C_2+C_{m2})(gm_2-G_Z)))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.7}$$

$$a_{12} = \frac{(-(C_2C_{m1}gds_2)+(gds_2C_{m1}(C_2+C_{m2})))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.8}$$

$$a_{13} = \frac{-(G_ZC_{m1}(C_2+C_{m2}))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.9}$$

$$a_{14} = \frac{-(G_ZC_{m1}(C_2+C_{m2}))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.10}$$

$$\tag{4.11}$$

$$a_{21} = \frac{((gds_1C_{m2}(C_1+C_{m1}))-(C_1((gm_2C_{m1})+(gds_1C_{m2})))-(C_{m2}(C_1+C_{m1})(gm_2-G_Z)))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.12}$$

$$a_{22} = \frac{((C_1C_{m1}gds_2)+(gds_2C_{m2}(C_1+C_{m1})))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.13}$$

$$a_{23} = \frac{-(G_ZC_{m2}(C_1+C_{m1}))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.14}$$

$$a_{24} = \frac{-(G_ZC_{m2}(C_1+C_{m1}))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.15}$$

$$\tag{4.16}$$

$$a_{31} = \frac{G_Z}{C_3} \tag{4.17}$$

$$a_{32} = \frac{gm_3}{C_3} \tag{4.18}$$

$$a_{33} = \frac{-(G_Z+gds_3)}{C_3} \tag{4.19}$$

$$a_{34} = \frac{-G_Z}{C_3} \tag{4.20}$$

$$\tag{4.21}$$

$$a_{41} = \frac{(-(C_1C_{m1}(C_2+C_{m2})(gm_2-G_Z))+(C_1C_2((gm_2C_{m1})+(gds_1C_{m2})))-(C_2C_{m2}gds_1(C_1+C_{m1})))}{((C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1})))C_{m1}} \tag{4.22}$$

$$a_{42} = \frac{((C_1C_{m1}(C_2+C_{m2})gds_2)-(C_1C_2C_{m1}gds_2))}{((C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1})))C_{m1}} \tag{4.23}$$

$$a_{43} = \frac{-(G_ZC_{m1}C_1(C_2+C_{m2}))}{((C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1})))C_{m1}} \tag{4.24}$$

$$a_{44} = \frac{-(G_ZC_{m1}C_1(C_2+C_{m2}))}{((C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1})))C_{m1}} \tag{4.25}$$

$$\tag{4.26}$$

$$b_1 = \frac{(-(C_2gm_1C_{m2})-(C_{m1}gm_1(C_2+C_{m2})))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.27}$$

$$b_2 = \frac{((C_1G_{m1}C_{m2})-(C_{m2}gm_1(C_1+C_{m1})))}{-(C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1}))} \tag{4.28}$$

$$b_3 = 0 \tag{4.29}$$

$$b_4 = \frac{(-(C_1C_2gm_1C_{m2})+(C_2C_{m2}(C_1+C_{m1})gm_1))}{((C_1C_{m1}(C_2+C_{m2}))-(C_2C_{m2}(C_1+C_{m1})))C_{m1}} \tag{4.30}$$

4.1 MATLAB modeling of three stage nested Miller compensated opamp

4.1.1 Ground centered opamp modeling

The state space matrix obtained in the previous section is used to get the transfer function using MATLAB. Also the circuit parameters are extracted from the dc-analysis and input to MATLAB and the following frequency response shown in Fig. 4.2 is obtained. For the ground centered opamp the following parameters are extracted.

- $gm_1 = 586.6\,\mu\text{S}$

- $gds_1 = 170.79\,\text{nmho}$
- $C_1 = 0.103\,\text{pF}$
- $gm_2 = 16.78\,\mu\text{S}$
- $gds_2 = 112.8\,\text{nmho}$
- $C_2 = 5.63\,\text{pF}$
- $gm_3 = 22.4\,\text{mS}$
- $gds_3 = 62.9\,\text{mmho}$
- $C_3 = 100\,\text{pF}$
- $C_{m1} = 30\,\text{pF}$
- $C_{m2} = 200\,\text{fF}$
- $R_z = 10\,\mu\Omega$

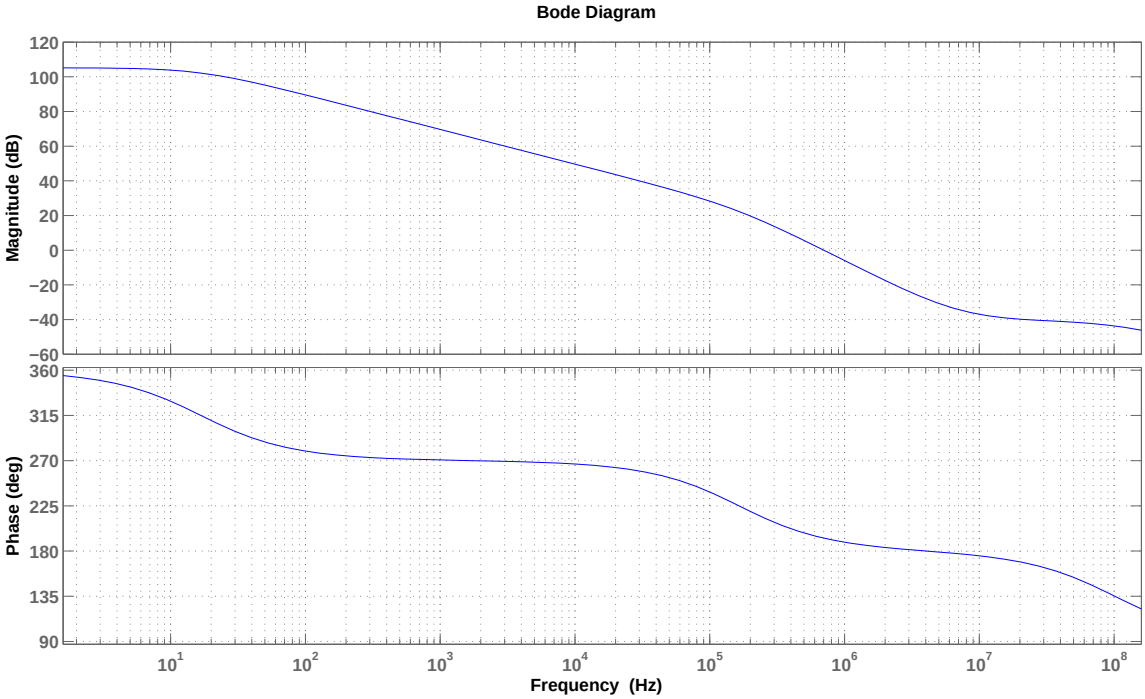


Figure 4.2: Ground centered opamp frequency response from the macro model.

The transfer function obtained from MATLAB is

$$TF = \frac{-1.976 * 10^{24}s^2 - 7.611 * 10^{28}s + 4.245 * 10^{39}}{s^4 + 3.391 * 10^{17}s^3 + 2.154 * 10^{26}s^2 + 2.227 * 10^{32}s + 2.336 * 10^{34}} \quad (4.31)$$

From the transfer function the location of poles and zeros are obtained. The zeros are at

- $Z_1 = -7.379\,\text{MHz}$
- $Z_2 = 7.373\,\text{MHz}$

poles are at

- $P_1 = -16.7\,\text{Hz}$
- $P_2 = -164.8\,\text{kHz}$
- $P_3 = -100.9\,\text{MHz}$
- $P_4 = -53965\,\text{THz}$

- dc gain = 105.2 dB
- phase margin = 12.83^0
- UGF = 700.8 kHz

From the frequency response it is clear that the system has a second pole before unity gain frequency. Now the pole positions with varying C_{m1} and C_{m2} are plotted in the Fig. 4.3, Fig. 4.4, Fig. 4.5 and Fig. 4.6. R_z is kept 1 mΩ for this analysis. While varying C_{m1}, C_{m2} is 200 fF and while varying C_{m2}, C_{m1} is 30 pF.

We see that to move the second pole outside unity gain frequency will require a very high value of Miller capacitor C_{m1} and will lead to reduced UGF. So $C_{m2} =$ 200 fF is chosen such that the second pole does not move inward. $C_{m1} = 30\,\text{pF}$ is chosen such that UGF is around 2 MHz with 20 dB/decade rolloff. UGF is kept within 2 MHz to keep the higher order poles(P_3 and P_4) beyond UGF. Now the second pole is canceled by placing a LHP zero very near to it. The value of R_z is chosen such that a LHP zero is placed near the second pole. For finding the R_z pole zero movement is plotted varying R_z.Fig. 4.7, Fig. 4.8 and Fig. 4.9 plots the location of first three poles with variation of R_z. The 4th pole is at very high frequency and its effect can be ignored.Fig. 4.10 and Fig. 4.11 plots the location of the zeros with variation of R_z.

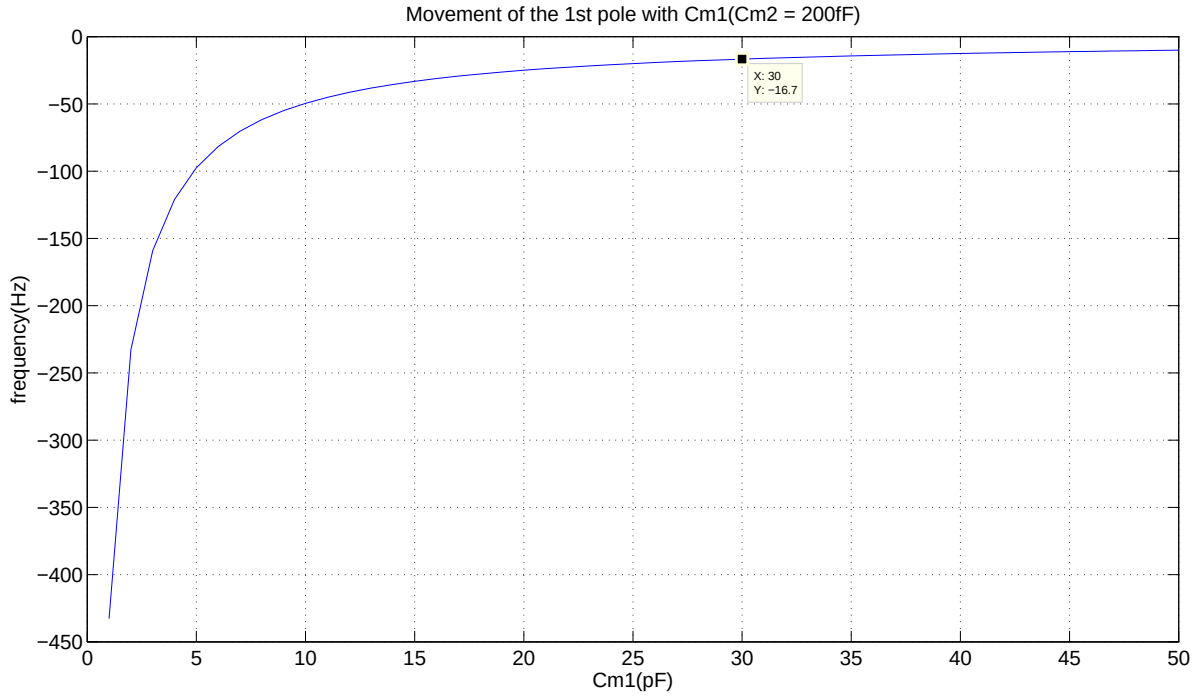


Figure 4.3: Movement of the 1st pole with variation of Cm1.

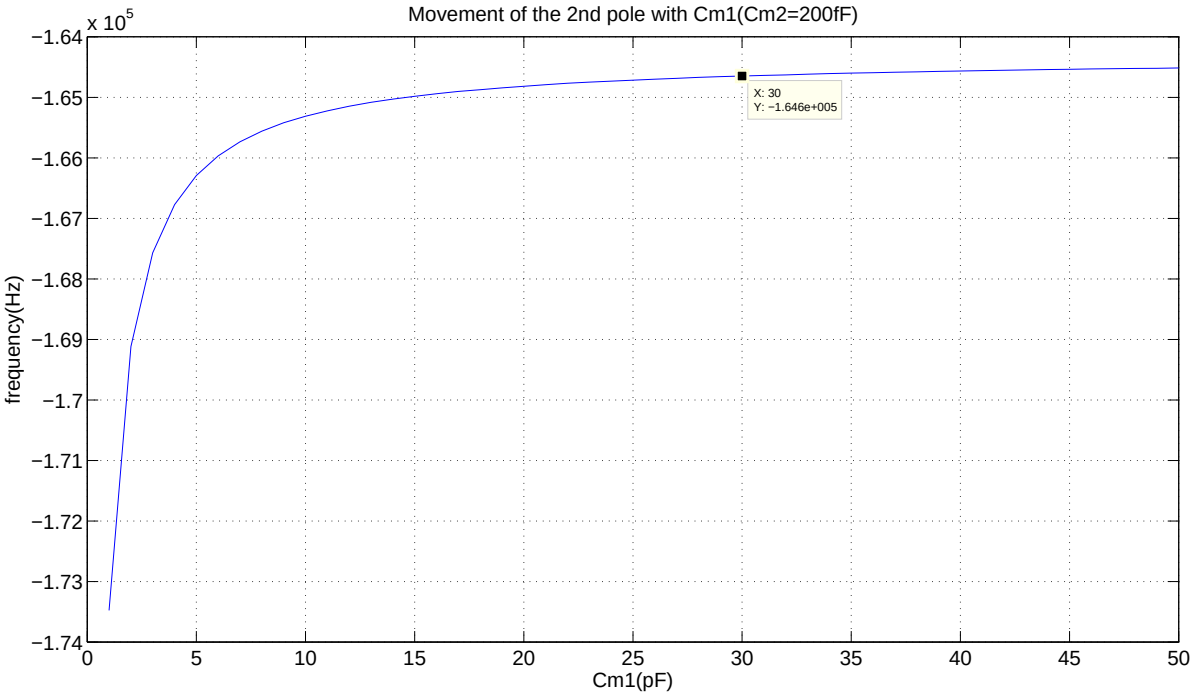


Figure 4.4: Movement of the 2nd pole with variation of Cm1.

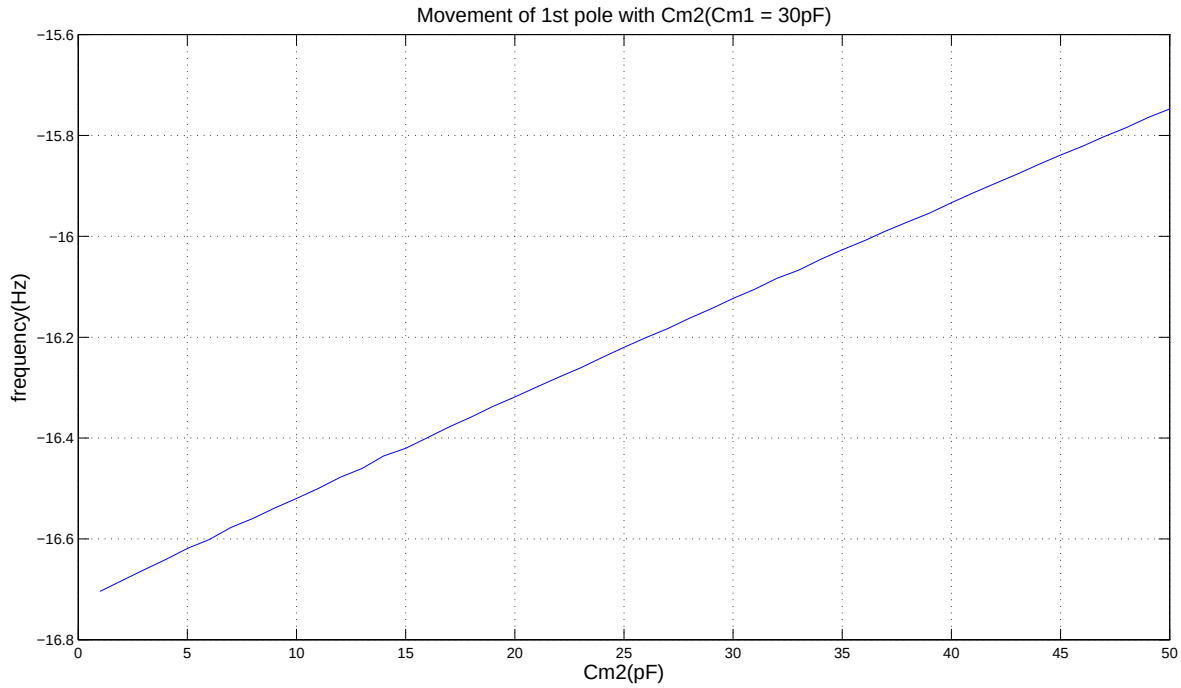


Figure 4.5: Movement of the 1st pole with variation of Cm2.

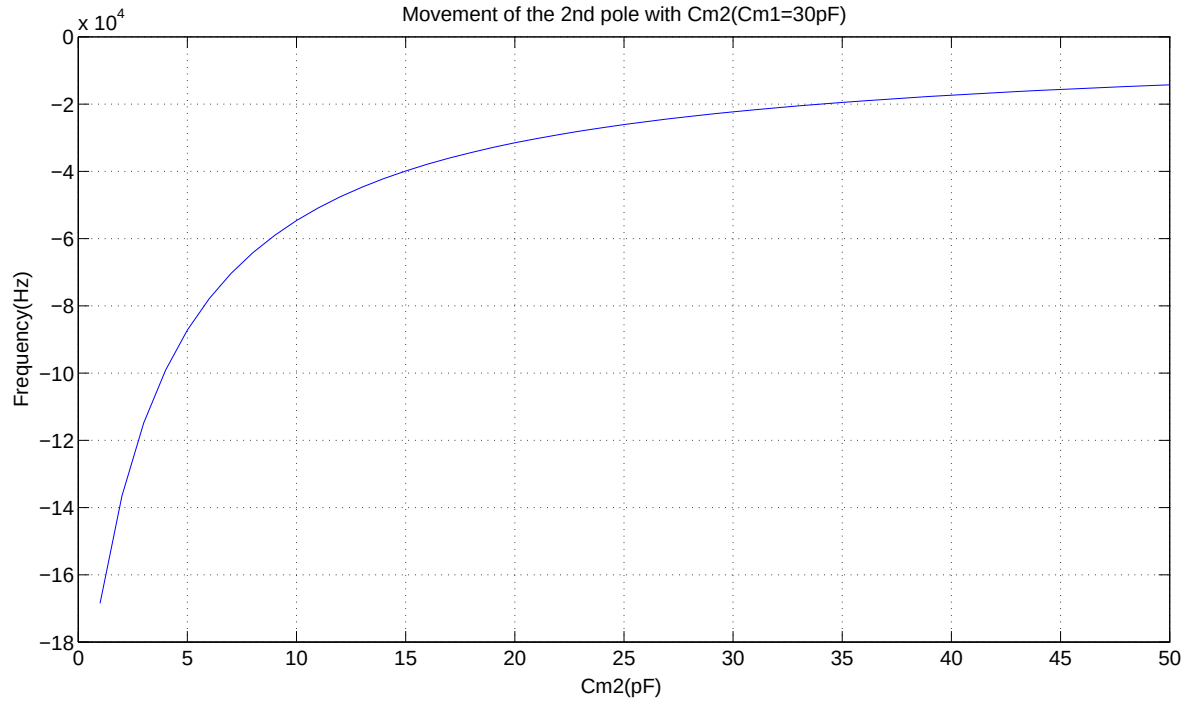


Figure 4.6: Movement of the 2nd pole with variation of Cm2.

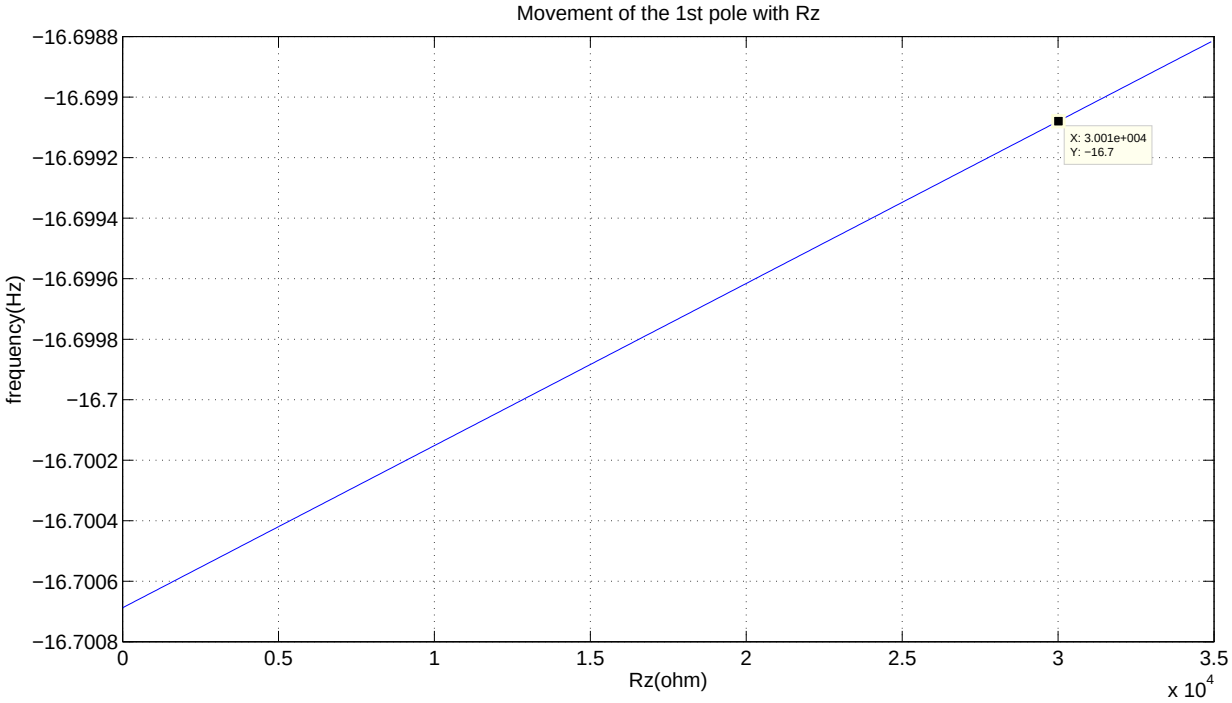


Figure 4.7: Movement of the 1st pole with variation of Rz.

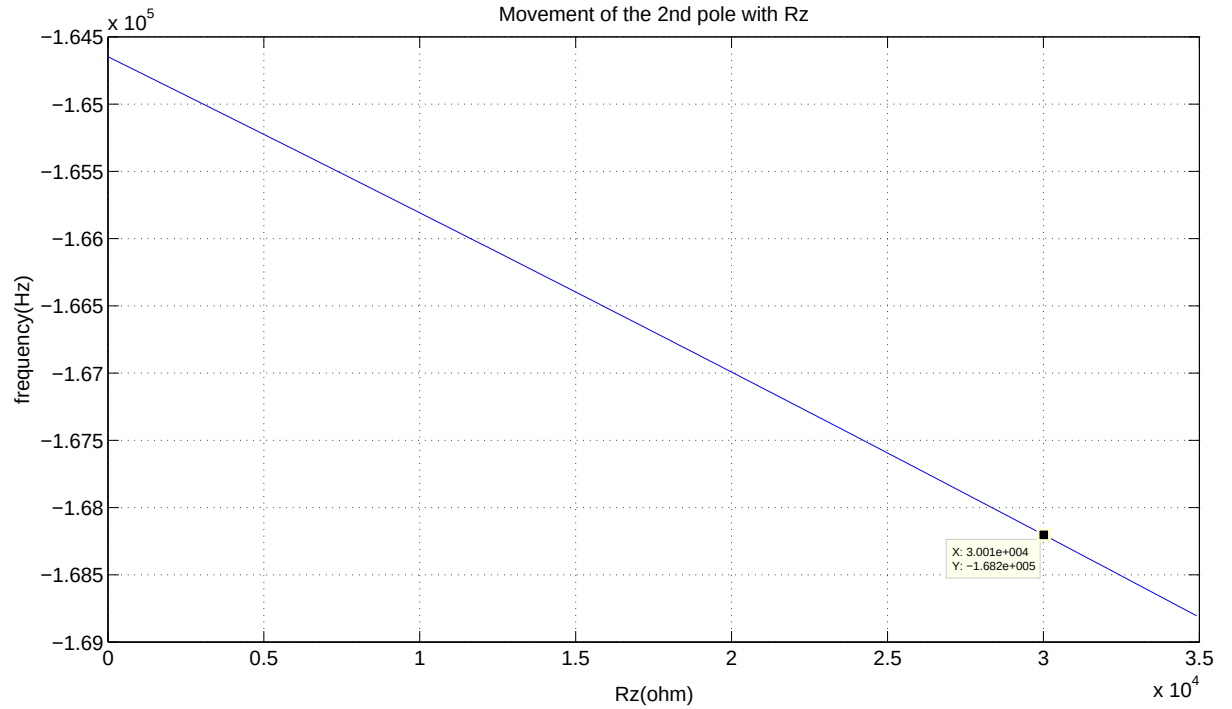


Figure 4.8: Movement of the 2nd pole with variation of Rz.

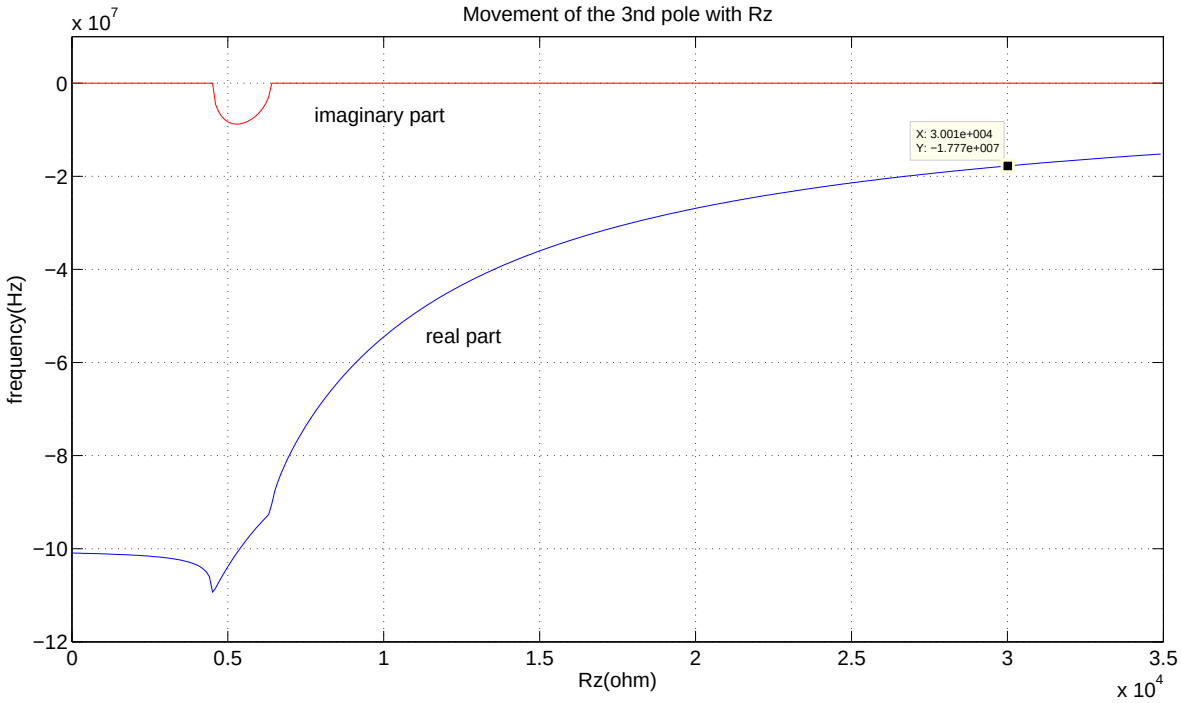


Figure 4.9: Movement of the 3rd pole with variation of Rz.

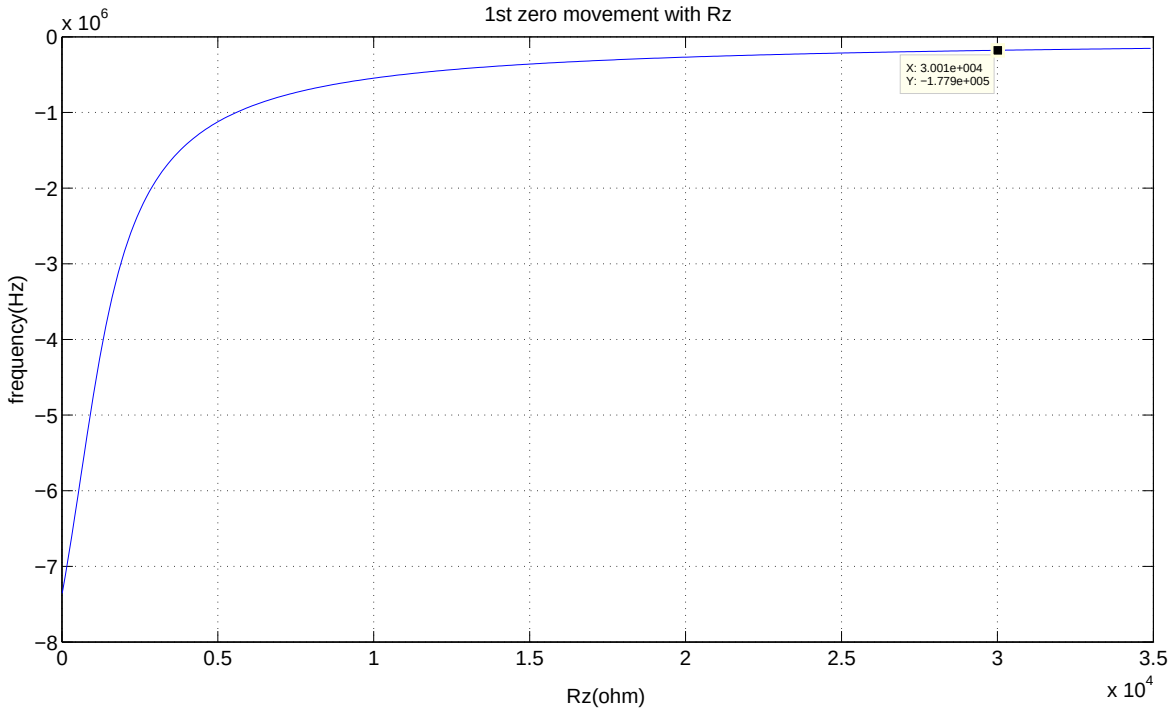


Figure 4.10: Movement of the 1st zero with variation of Rz.

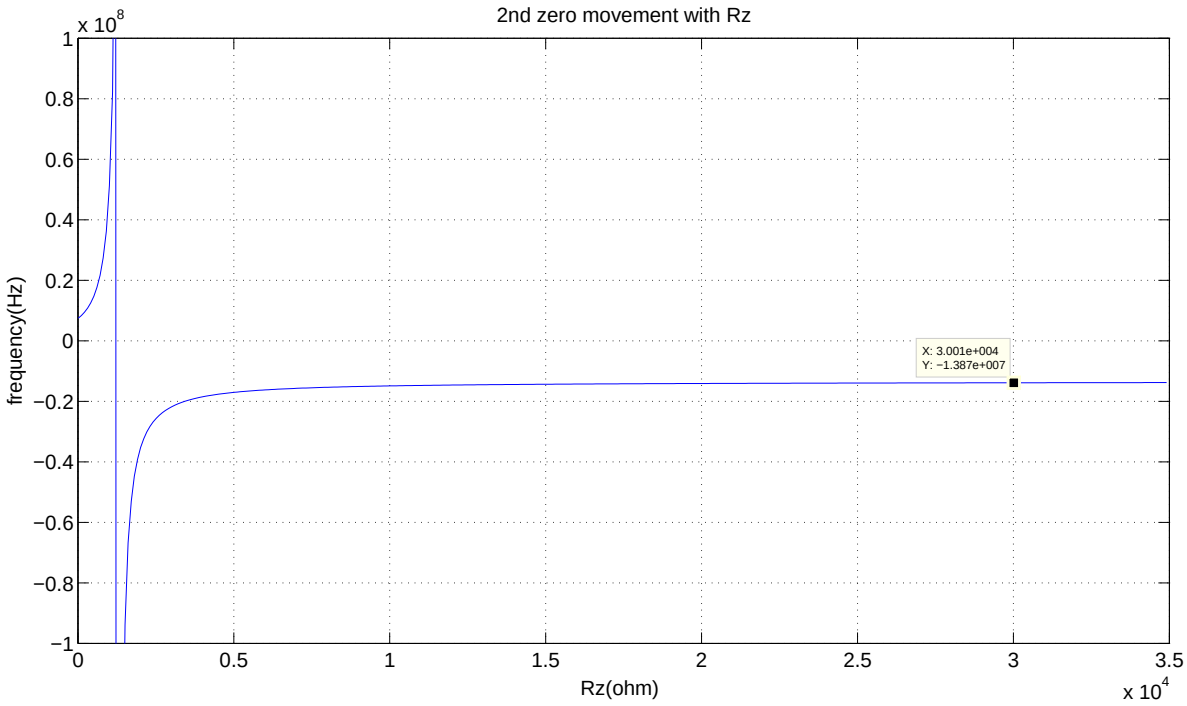


Figure 4.11: Movement of the 2nd zero with variation of Rz.

From the above plots we see that for $R_z = 30\,\mathrm{k\Omega}$ the 2nd pole is canceled by the first zero.This compensation technique has two advantages.Firstly the pole is cancelled.Also there is no RHP zero to degrade the phase response. Thus with new value of R_z is

- $R_z = 30\,\mathrm{k\Omega}$

The compensated frequency response is shown in the Fig. 4.12.This frequency response matches closely with the frequency response from actual spice simulation.

The transfer function obtained from MATLAB is

$$TF = \frac{1.452 * 10^{16}s^2 + 1.282 * 10^{24}s + 1.415 * 10^{30}}{s^4 + 7.41 * 10^8 s^3 + 7.095 * 10^{16}s^2 + 7.416 * 10^{22}s + 7.781 * 10^{24}} \quad (4.32)$$

From the transfer function the location of poles and zeros are obtained.The zeros are at

- $Z_1 = -177.9\,\mathrm{kHz}$
- $Z_2 = -13.87\,\mathrm{MHz}$

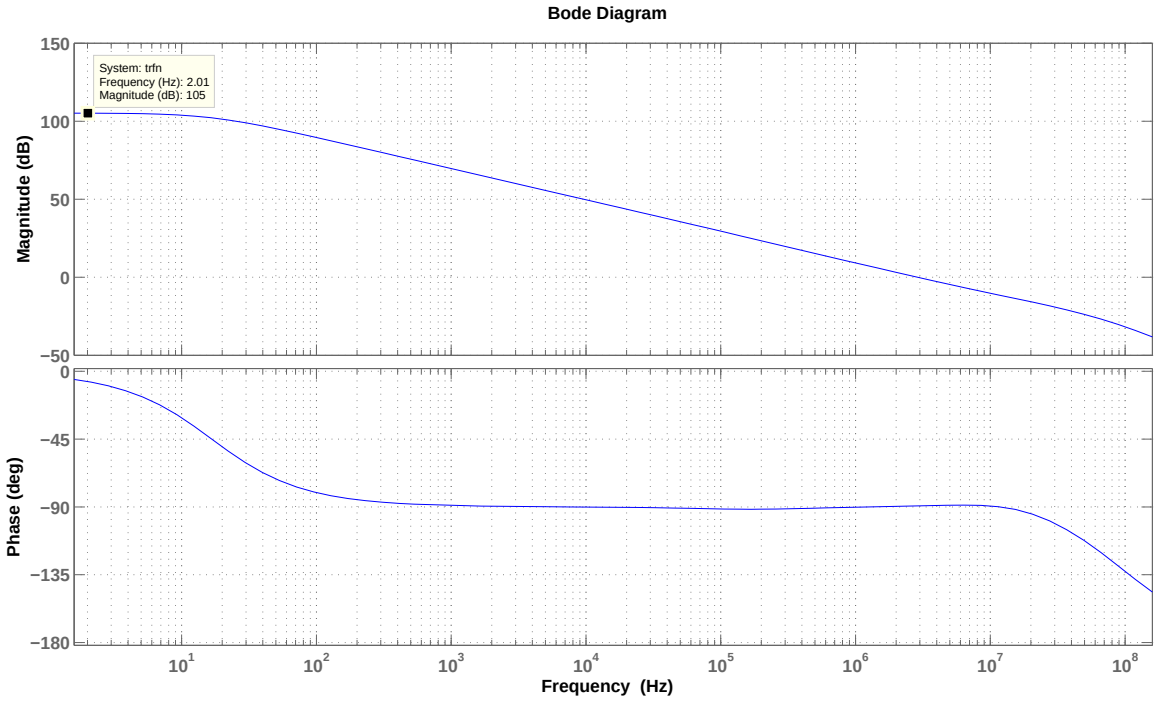


Figure 4.12: Ground centered opamp frequency response from the macro model.

poles are at

- $P_1 = -16.7\,\text{Hz}$
- $P_2 = -168.2\,\text{kHz}$
- $P_3 = -17.77\,\text{MHz}$
- $P_4 = -100\,\text{MHz}$

- dc gain $= 105.2\,\text{dB}$
- phase margin $= 90.68^0$
- UGF $= 2.89\,\text{MHz}$

4.1.2 $0.9\,\text{V}$ common mode opamp modeling

For the $0.9\,\text{V}$ common mode opamp the following parameters are extracted and Frequency response is plotted with $R_z = 10\,\mu\Omega$ (i.e basically without any series resistance with Miller capacitors).

- $gm_1 = 618.20\,\mu\text{S}$

- $gds_1 = 193.85\,\text{nmho}$
- $C_1 = 0.565\,\text{pF}$
- $gm_2 = 17.540\,\mu\text{S}$
- $gds_2 = 190.51\,\text{nmho}$
- $C_2 = 2.162\,\text{pF}$
- $gm_3 = 24\,\text{mS}$
- $gds_3 = 63.3\,\text{mmho}$
- $C_3 = 100\,\text{pF}$
- $C_{m1} = 30\,\text{pF}$
- $C_{m2} = 200\,\text{fF}$
- $R_z = 10\,\mu\Omega$

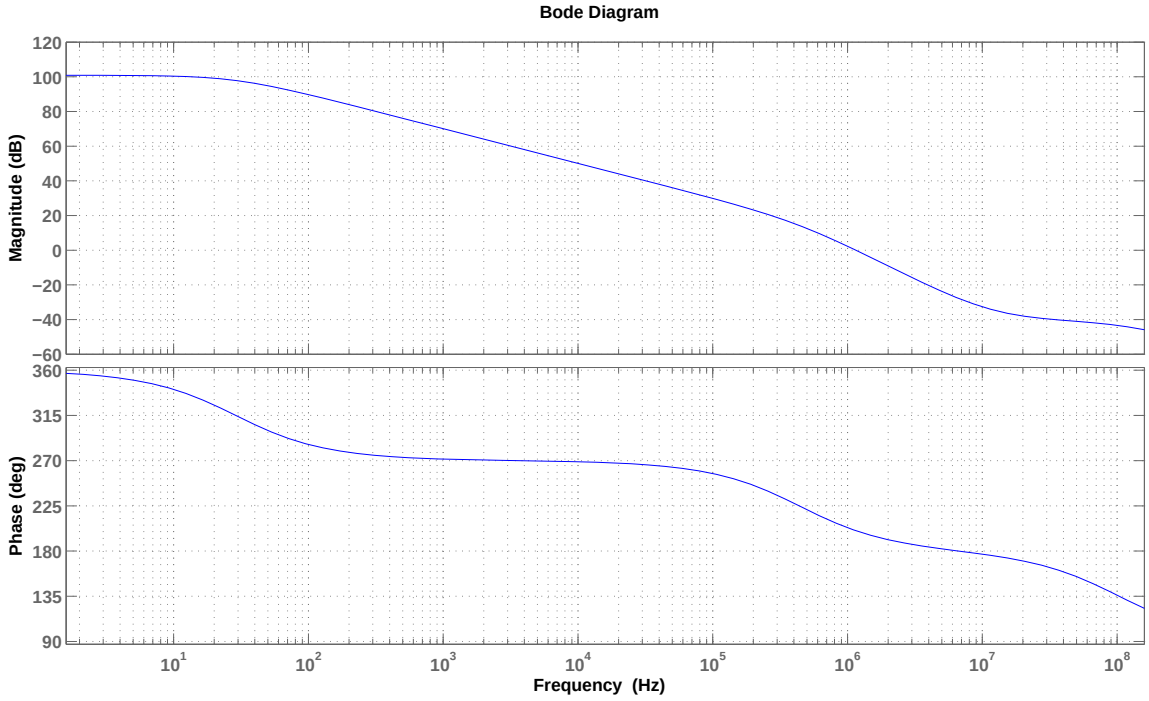


Figure 4.13: 0.9 V common mode voltage opamp frequency response from the macro model.

The transfer function obtained from MATLAB is

$$TF = \frac{-8.226 * 10^{23} s^2 - 1.071 * 10^{29} s + 4.885 * 10^{39}}{s^4 + 1.366 * 10^{17} s^3 + 8.86 * 10^{25} s^2 + 2.442 * 10^{32} s + 4.422 * 10^{34}} \quad (4.33)$$

From the transfer function the location of poles and zeros are obtained.The zeros are at

- $Z_1 = -12.27\,\text{MHz}$
- $Z_2 = 12.25\,\text{MHz}$

poles are at

- $P_1 = -28.81\,\text{Hz}$
- $P_2 = -440.55\,\text{kHz}$
- $P_3 = -102.81\,\text{MHz}$
- $P_4 = -21736\,\text{THz}$

- dc gain = $100.1\,\text{dB}$
- phase margin = 20.32^0
- UGF = $1.15\,\text{MHz}$

Now the pole positions with varying C_{m1} and C_{m2} are plotted in the Fig. 4.14,Fig. 4.15, Fig. 4.16 and Fig. 4.15.R_z is kept $1\,\text{m}\Omega$ for this analysis.While varying C_{m1}, $C_{m2} = 200\,\text{fF}$ and while varying C_{m2}, $C_{m1} = 30\,\text{pF}$.

Here also we see that to move the second pole outside unity gain frequency will require a very high value of Miller capacitor C_{m1} as before.Also $C_{m2} = 200\,\text{fF}$ is chosen such that the second pole does not move inward.$C_{m1} = 30\,\text{pF}$ is chosen such that UGF is around $2\,\text{MHz}$ with $20\,\text{dB/decade}$ rolloff. Now the second pole is canceled by placing a LHP zero very near to it.The value of R_z is chosen such that a LHP zero is placed near the second pole. Fig. 4.18,Fig. 4.19 and Fig. 4.20 plots the location of first three poles with variation of R_z.The 4th pole is at very high frequency and its effect can be ignored.Fig. 4.21 and Fig. 4.22 plots the location of the zeros with variation of R_z.

As was in the previous case,here the second pole is canceled for $R_z = 10\,\text{k}\Omega$.Thus simulation is done with new value of R_z.

- $R_z = 10\,\text{k}\Omega$

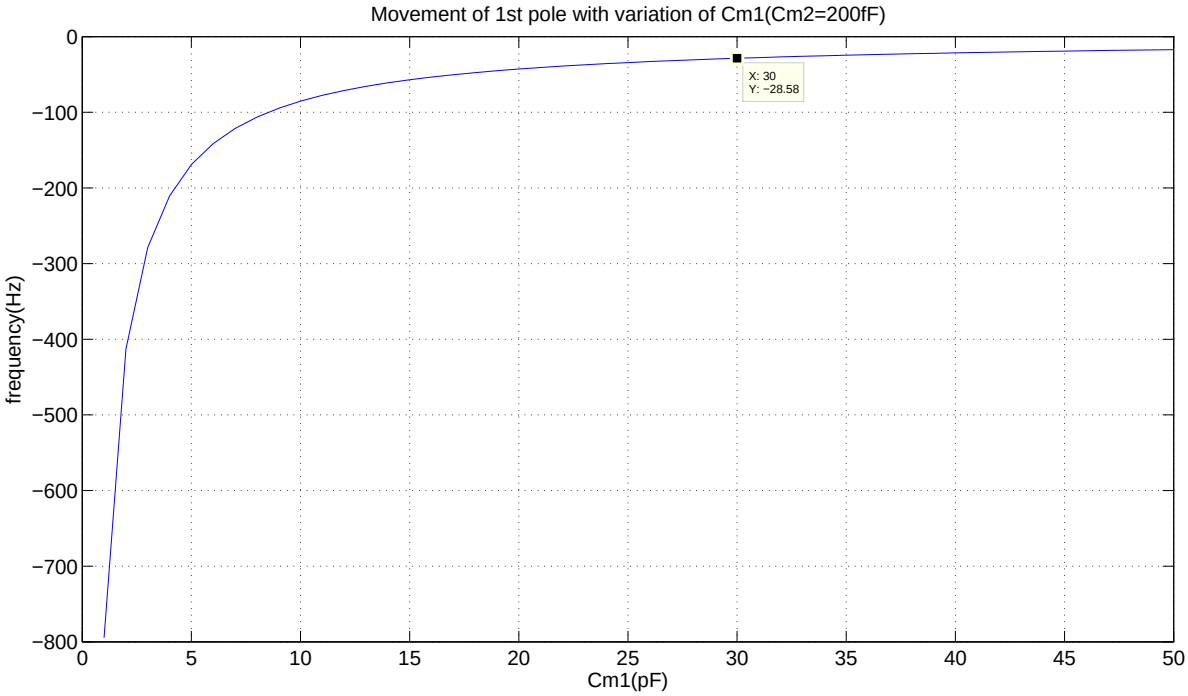


Figure 4.14: Movement of the 1st pole with variation of Cm1.

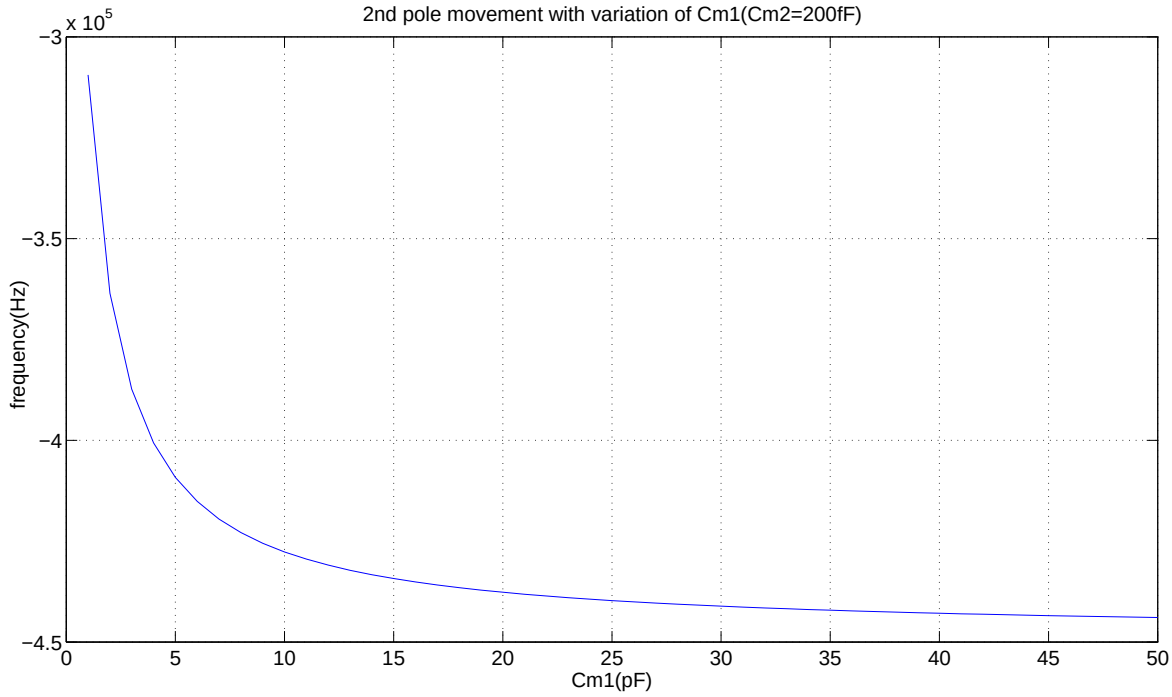


Figure 4.15: Movement of the 2nd pole with variation of Cm1.

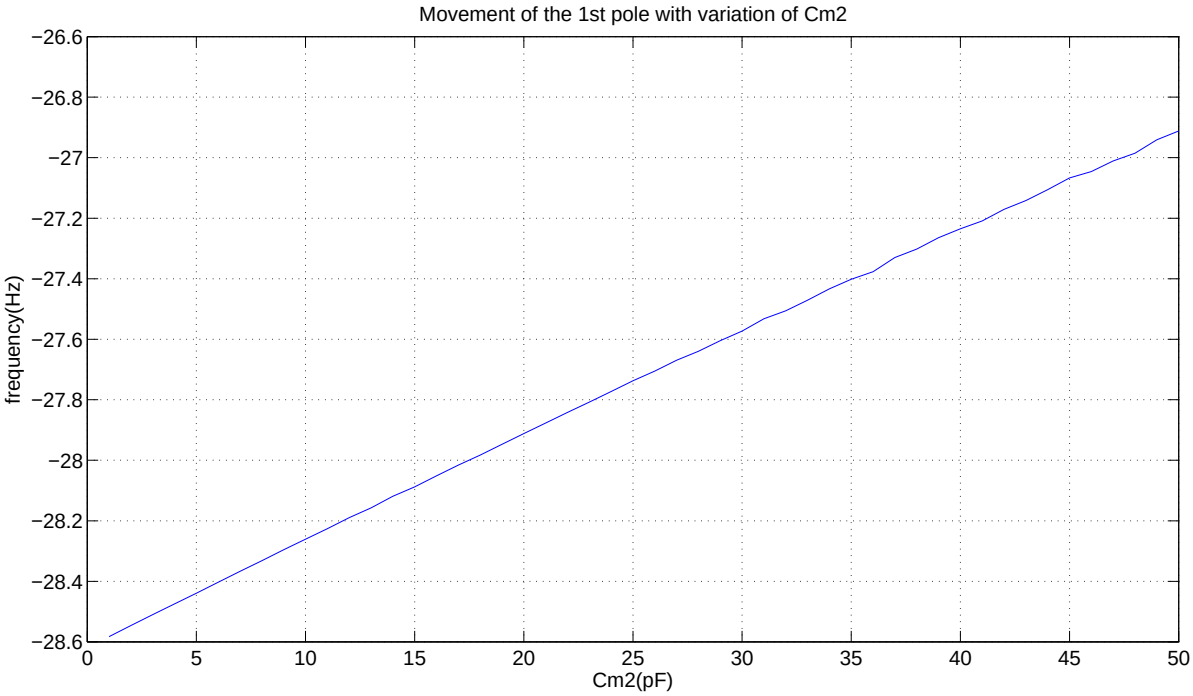


Figure 4.16: Movement of the 1st pole with variation of Cm2.

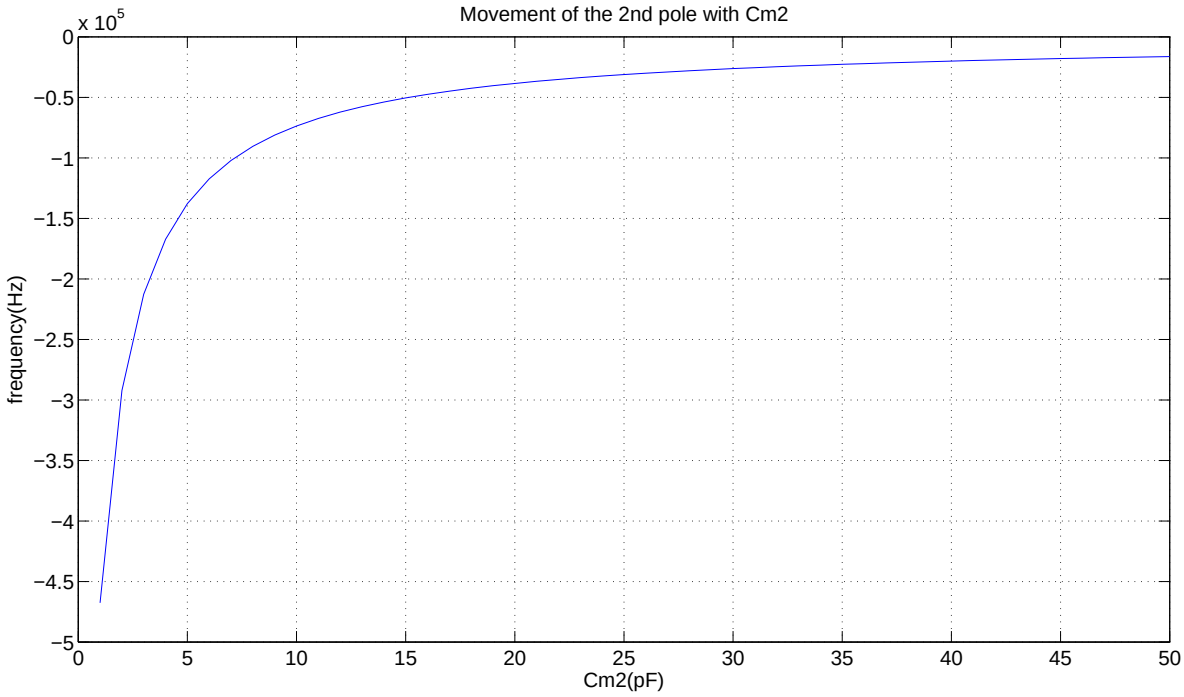


Figure 4.17: Movement of the 2nd pole with variation of Cm2.

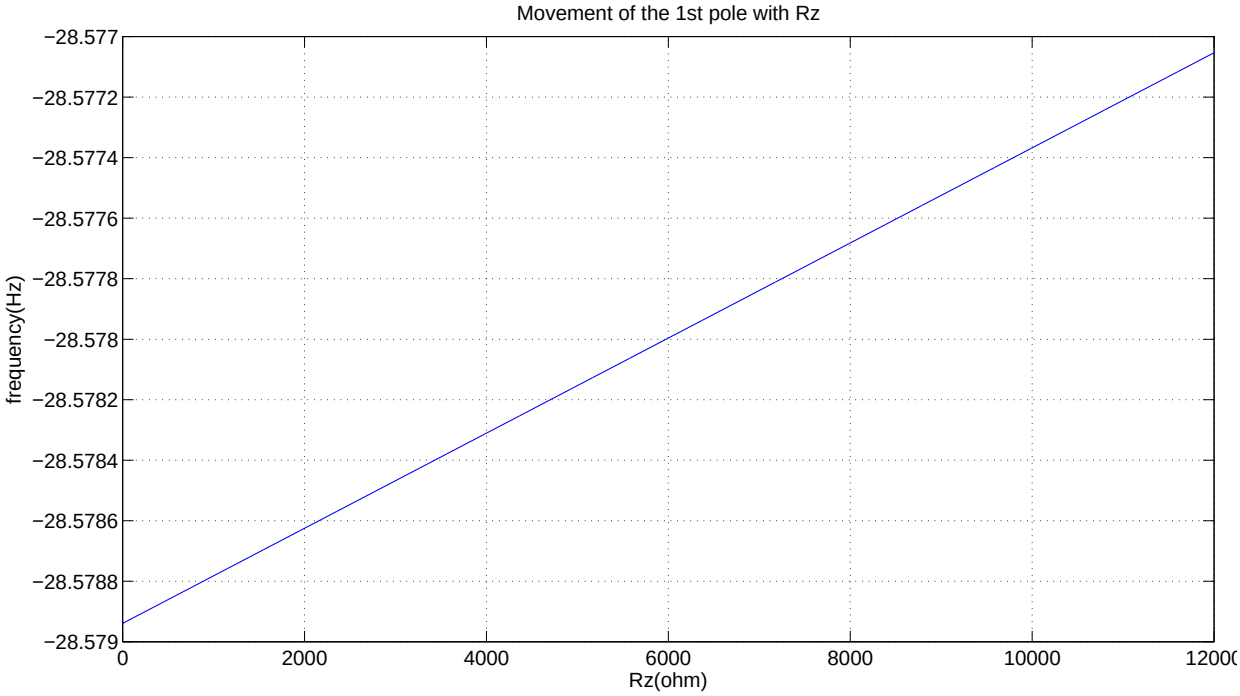


Figure 4.18: Movement of the 1st pole with variation of Rz.

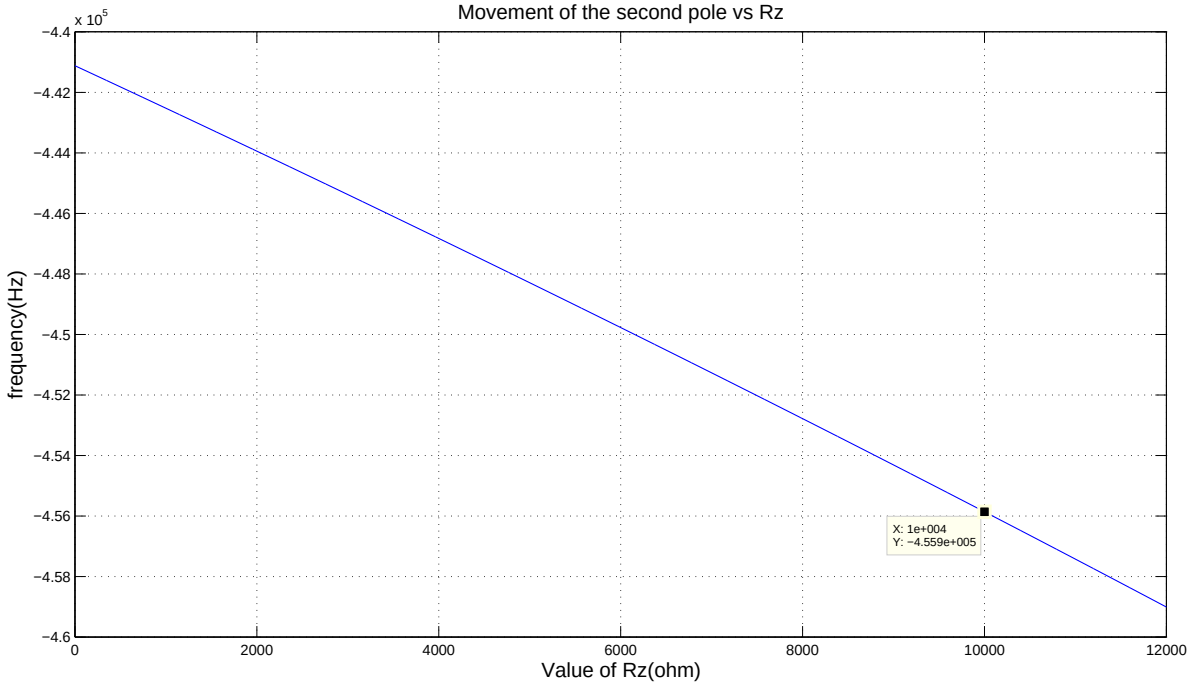


Figure 4.19: Movement of the 2nd pole with variation of Rz.

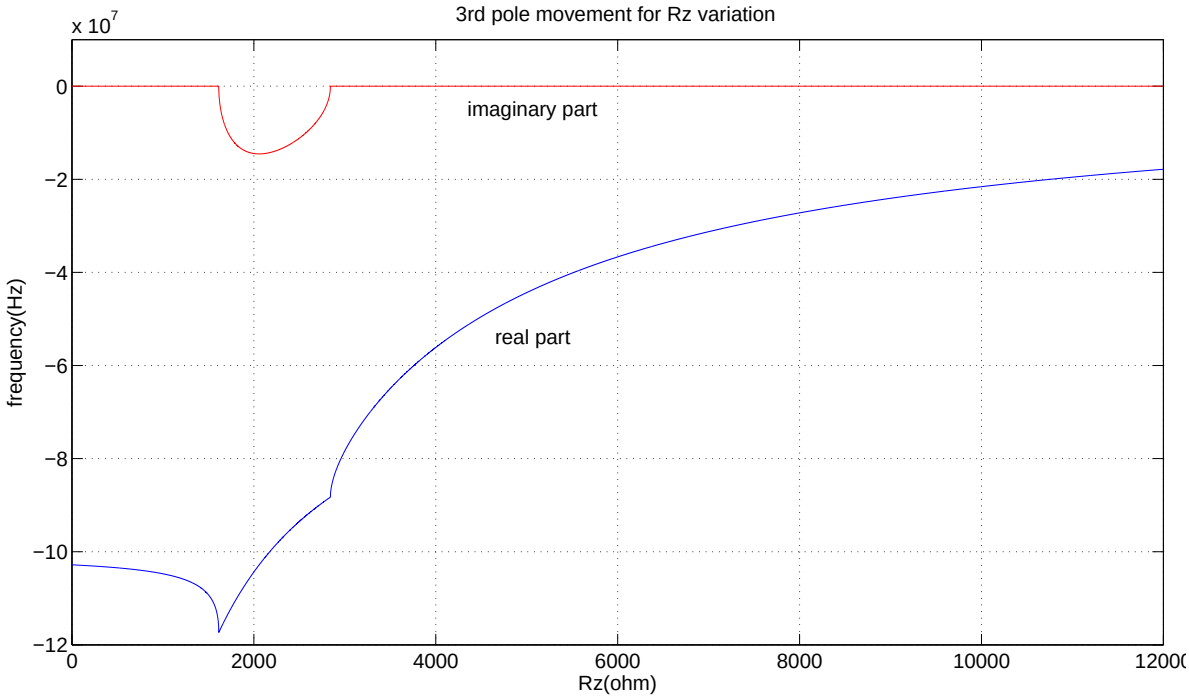


Figure 4.20: Movement of the 3rd pole with variation of Rz.

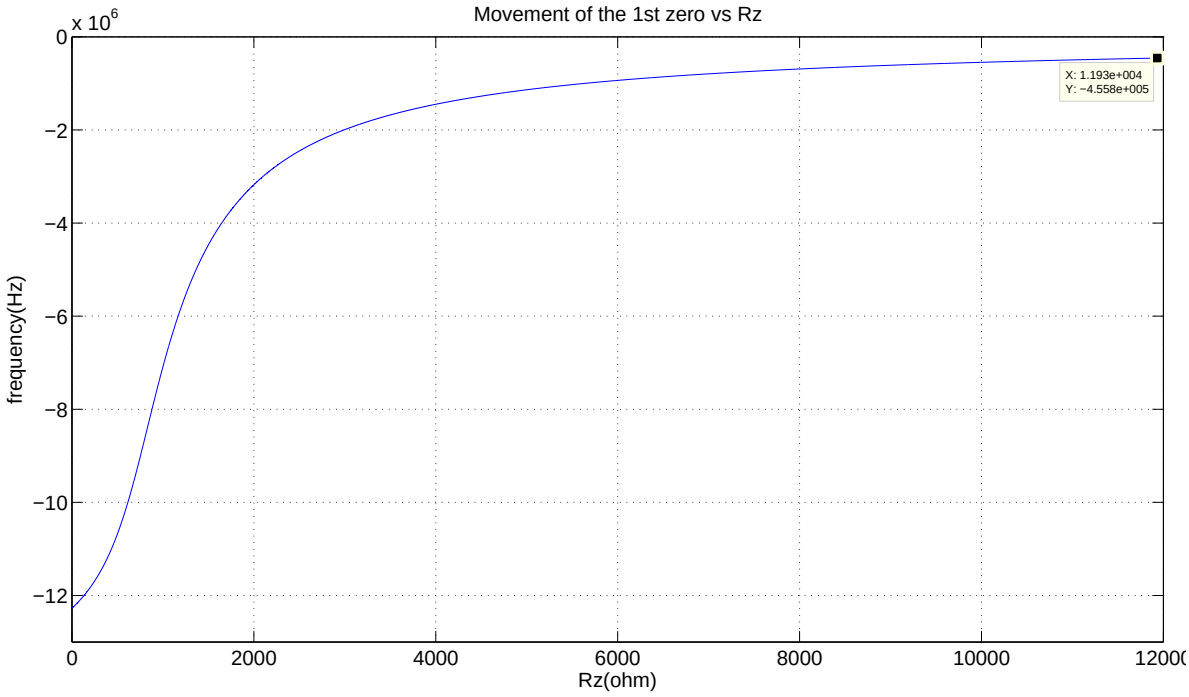


Figure 4.21: Movement of the 1st zero with variation of Rz.

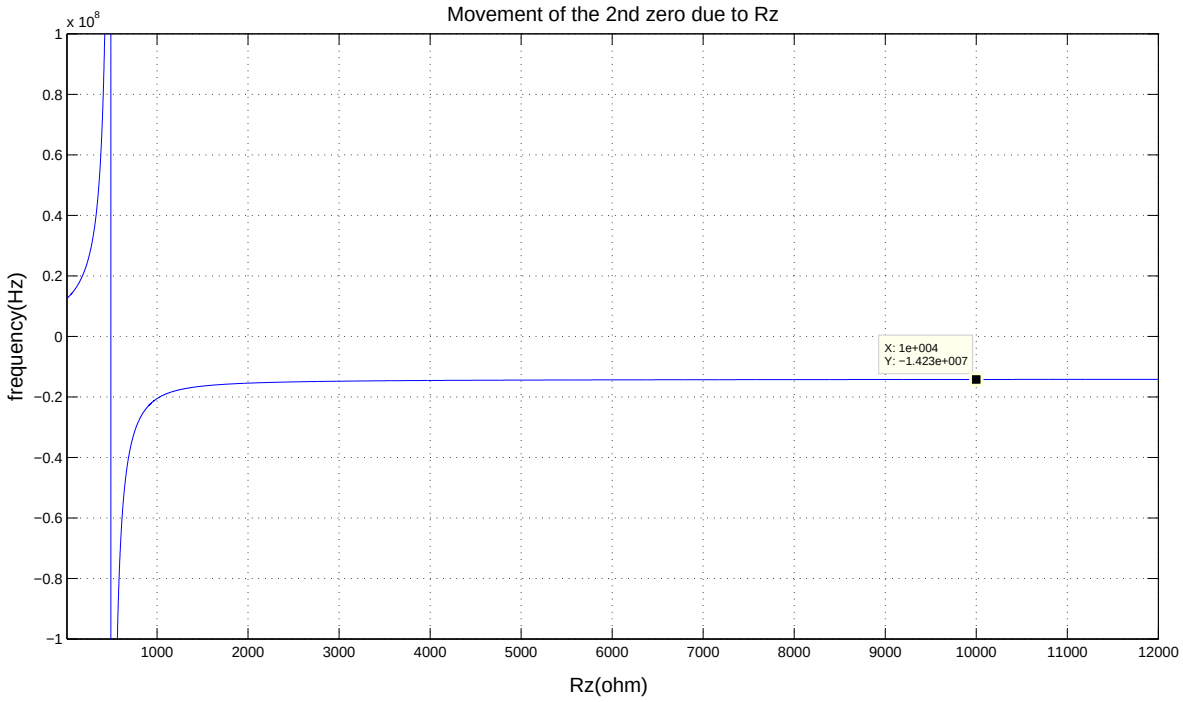


Figure 4.22: Movement of the 2nd zero with variation of Rz.

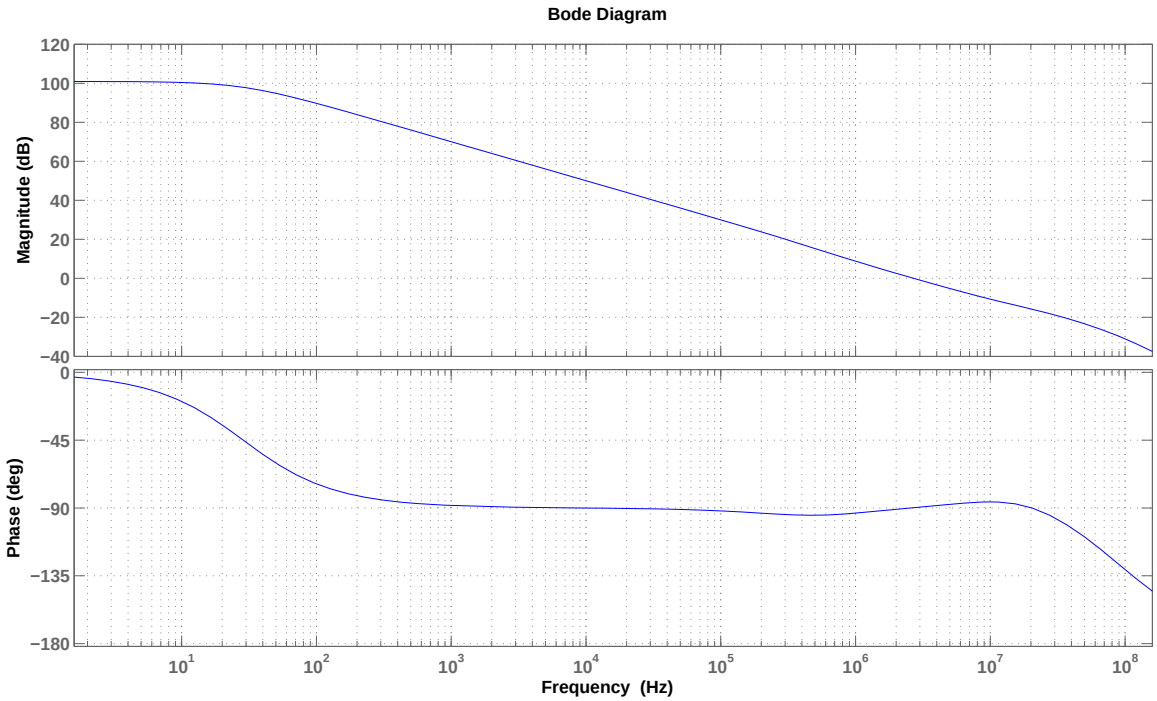


Figure 4.23: 0.9 V common mode voltage opamp frequency response from the macro model.

The frequency response is shown in the Fig. 4.23.It also matches with the frequency response obtained from spice simulation.

The transfer function obtained from MATLAB is

$$TF = \frac{1.589 * 10^{16}s^2 + 1.475 * 10^{24}s + 4.885 * 10^{30}}{s^4 + 7.681 * 10^8 s^3 + 8.757 * 10^{16}s^2 + 2.446 * 10^{23}s + 4.391 * 10^{25}} \quad (4.34)$$

From the transfer function the location of poles and zeros are obtained.The zeros are at

- $Z_1 = -547.31\,\text{kHz}$
- $Z_2 = -14.23\,\text{MHz}$

poles are at

- $P_1 = -28.57\,\text{Hz}$
- $P_2 = -455.86\,\text{kHz}$
- $P_3 = -21.58\,\text{MHz}$
- $P_4 = -100.21\,\text{MHz}$

- dc gain = 100.1 dB
- phase margin = 90.18^0
- UGF = 2.69 MHz

CHAPTER 5

$0.9\,\mathrm{V}$ common mode voltage opamp for $16\,\Omega$ load

In this chapter the design procedure of $0.9\,\mathrm{V}$ common mode voltage opamp for $16\,\Omega$ load is analyzed.

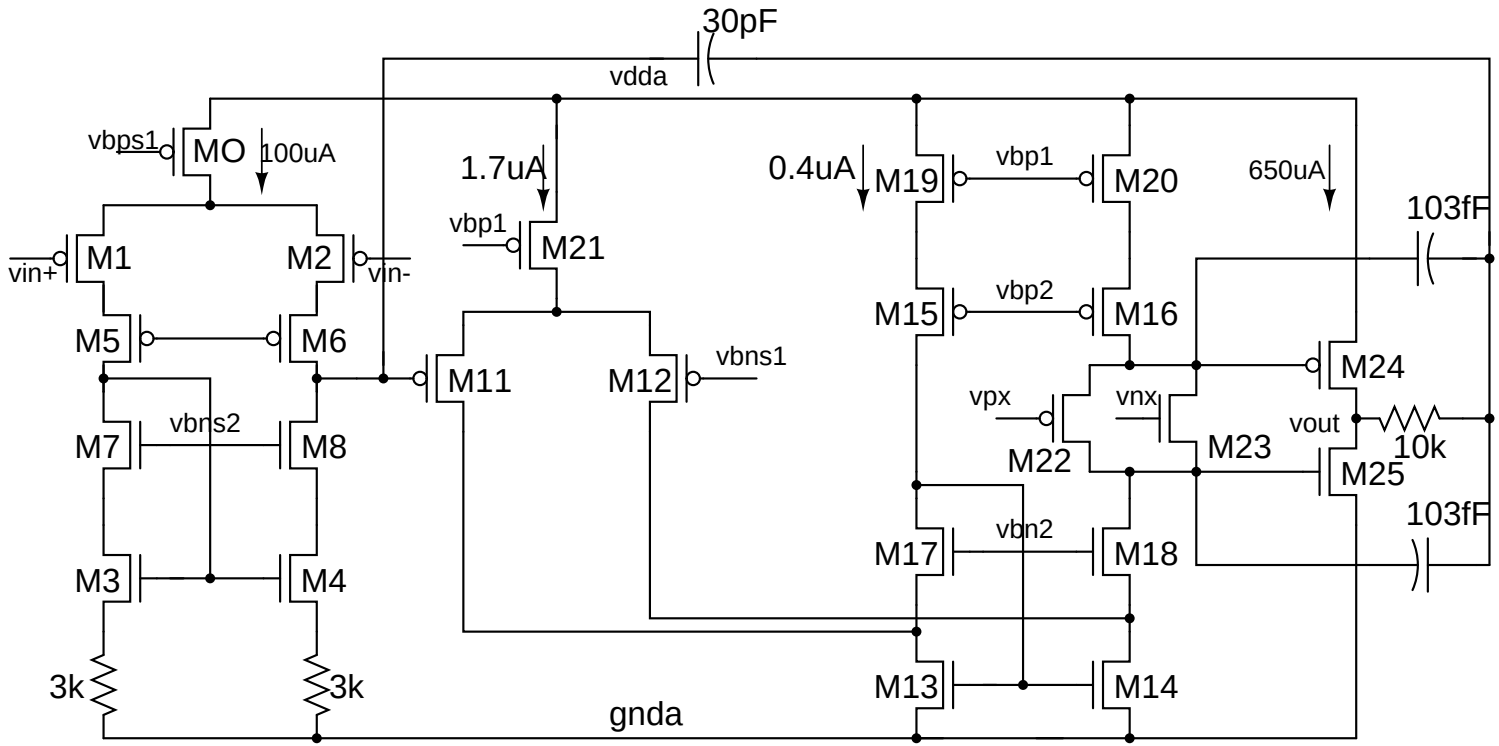
5.1 Objective

The opamp designed is supposed to be working in single-supply mode with $0.9\,\mathrm{V}$ common mode voltage for $16\,\Omega, 100\,\mathrm{pF}$ load. The first stage is telescopic cascode, the second stage is folded cascode and the third stage is class-AB stage as shown in Fig. 5.1.

5.1.1 Class-AB stage biasing

The quiescent current in the class-AB stage determines the crossover distortion. It is also necessary to minimize the class-AB stage quiescent current keeping the overall distortion within the specification limit to minimize the quiescent power consumption. Monticelli cell biasing is one of the methods of biasing class-AB stage[6].

The Fig. 5.3 is the Montecelli cell. Here the transistors M3 and M4 act as floating current mirror. Here we have



1st stage	2nd stage	3rd stage
M0 : 200(1u/500n) M1,M2 : 100(2u/2u) M3,M4 : 100(2.4u/2u) M5,M6 : 200(1u/1u) M7,M8 : 200(1.2u/1u)	M21 : 300(500n/250n) M11,M12 : 20(1u/1u) M15,M16,M19,M20 : 80(500n/250n) M22,M23 : 10(450n/180n) M17,M18 : 20(240n/180n) M13,M14 : 72(240n/180n)	M24 : 5200(240n/180n) M25 : 2600(240n/180n)

Figure 5.1: Three-stage opamp schematic.

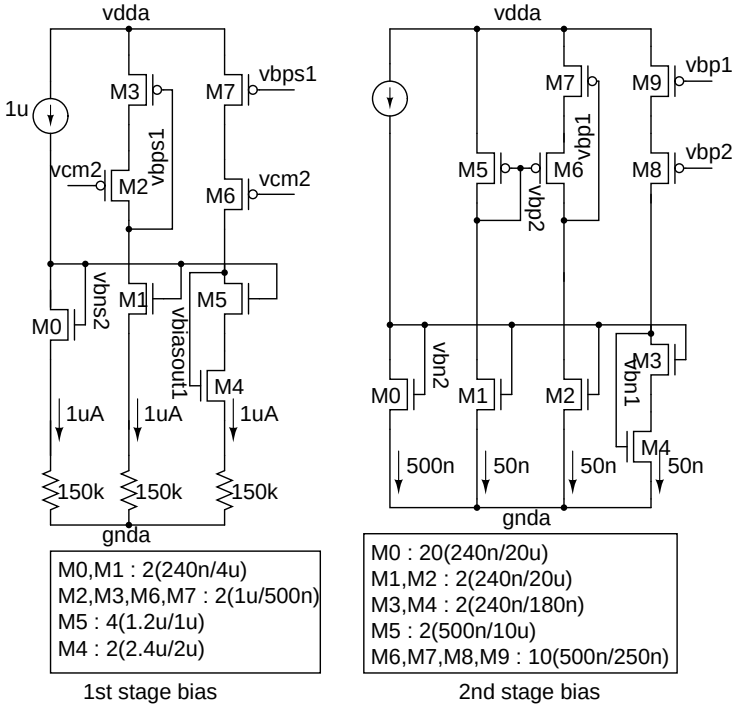


Figure 5.2: First and second stage bias schematic.

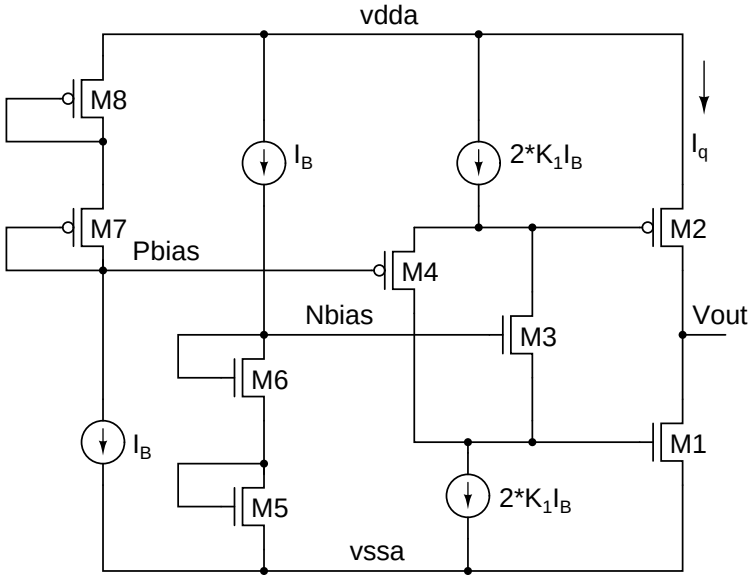


Figure 5.3: Montecelli cell for class-AB biasing.

$$(\frac{W}{L})_3 = K_1(\frac{W}{L})_6 \quad (5.1)$$

$$(\frac{W}{L})_1 = K_2(\frac{W}{L})_5 \quad (5.2)$$

$$(\frac{W}{L})_4 = K_1(\frac{W}{L})_8 \quad (5.3)$$

$$(\frac{W}{L})_2 = K_2(\frac{W}{L})_7 \quad (5.4)$$

$$(5.5)$$

. Also, from the circuit we have

$$V_{gs5} + V_{gs5} = V_{gs5} + V_{gs5} \quad (5.6)$$

$$V_{gs2} + V_{gs4} = V_{gs7} + V_{gs8} \quad (5.7)$$

. It is also assumed that the current $2K_1I_B$ is equally divided in M3 and M4. From the above criteria we get $I_q = K_2I_B$. Thus I_q can be scaled by K_2 accordingly.

5.1.2 Problems of Monticelli biasing scheme

The problem with Monticelli biasing is V_{ds} of the output transistors are different from V_{ds} of bias transistors. The assumption that the current will always be equally divided to M3 and M4 does not always hold true. At different corners the current is divided unequally between M3 and M4 and the above relation of $I_q = K_2I_B$ does not hold true. It may happen that at some corner the entire current flows through M3. In that case the quiescent current through the output NMOS will decrease and the current through the output PMOS will increase. Thus the output will saturate to Vdd. The exactly opposite situation occurs when entire current flows through M4 and the output then saturates to negative supply.

5.1.3 Modified class-AB biasing

The solution is use of replica bias to keep V_{ds} of bias transistors same as the V_{ds} of the output transistors. The Fig. 5.4 shows the modified biasing scheme. Here

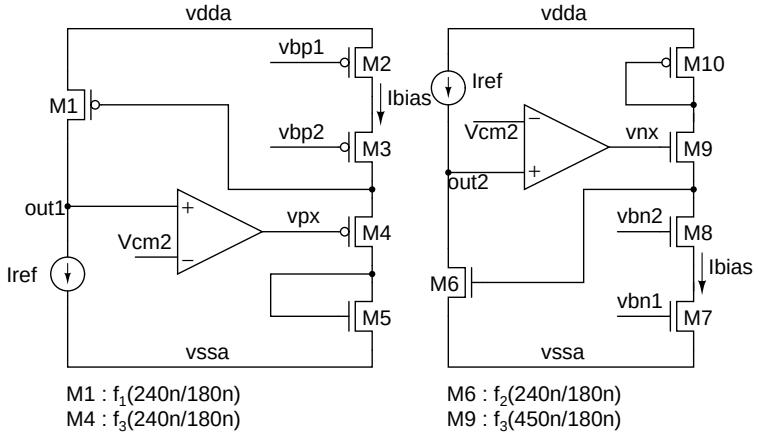


Figure 5.4: Class-AB stage modified bias.

Let f_p and f_n are the class-AB stage PMOS and NMOS finger no and let I_q be the quiescent current required. Then I_{ref} is set to be such that

$$\frac{I_{ref}}{I_q} = \frac{f_1}{f_p} = \frac{f_2}{f_n} \tag{5.8}$$

. Also, let the cascode branch of the second stage folded cascode have current of $I_{cascode}$ with M3 and M4 fingers to be f_x each. Then

$$\frac{I_{bias}}{\frac{I_{cascode}}{2}} = \frac{f_3}{f_x} = \frac{f_4}{f_x} \tag{5.9}$$

The nodes out_1 and out_2 are made to follow the output common mode voltage and the required voltages vpx and vnx are generated. These vpx and vnx vary from corner to corner and track the node out_1 and out_2 to output common mode voltage. Finally vpx and vnx are used to bias the floating current mirror transistors. This biasing circuit and the second and third stages are needed to be closely placed in layout for effective tracking.

The following Fig. 5.5 and Fig. 5.6 are the total transistor level circuit. For

NMOS bias (vnx) generation, PMOS input differential pair is used as feedback amplifier as the output of this differential pair is near positive supply. For PMOS bias (vpx) generation NMOS input differential pair is used as the output from this amplifier is near the negative supply. Miller compensation with zero nulling resistor is used to make this bias circuit stable.

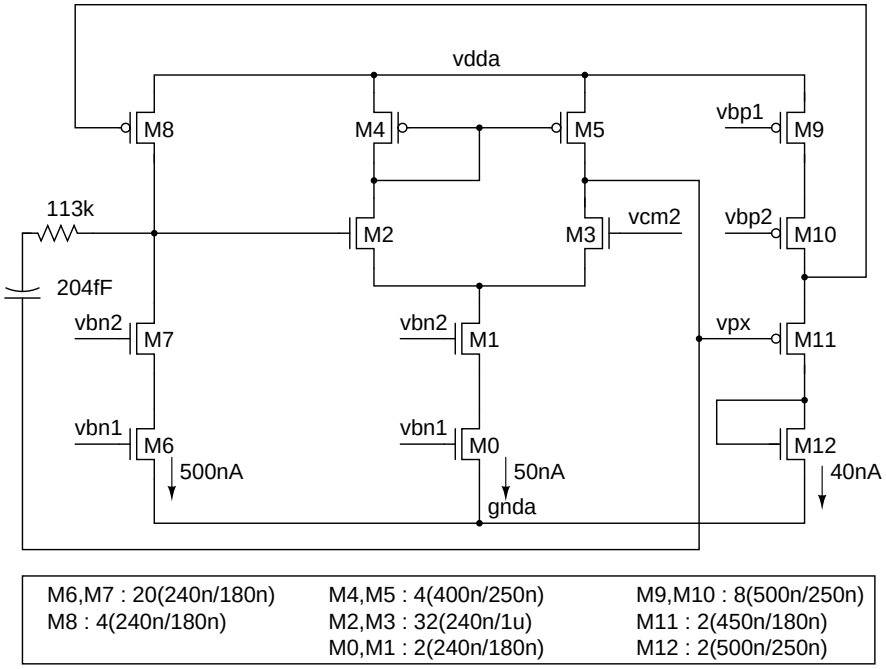


Figure 5.5: Class-AB stage PMOS bias schematic.

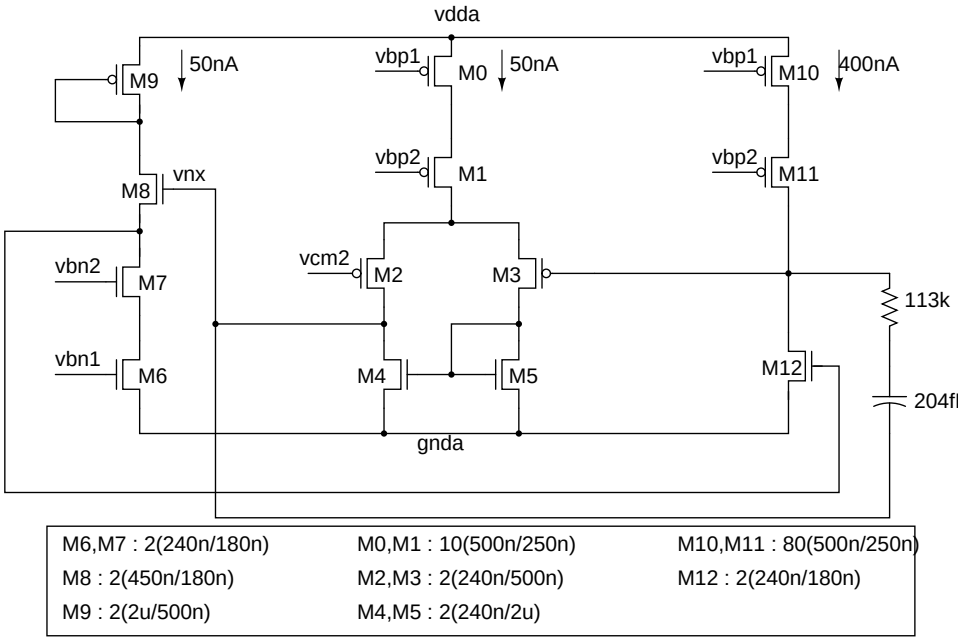


Figure 5.6: Class-AB stage NMOS bias schematic.

CHAPTER 6

Simulation and layout results for the $0.9\,\mathrm{V}$ common mode voltage 16Ω driver

6.1 Results

The three stage opamp was simulated and laid out using UMC180 μm technology. The following performance parameters are discussed consecutively.

- Open-Loop frequency response
- Transient response and Distortion
- Transfer characteristics
- Positive and Negative Slew rate
- Noise
- Area
- Power

6.1.1 Open-loop frequency response

The opamp was simulated with $16\,\Omega$ and 100 pF load at 70^0 C at corner(tt,res_typ,mimcaps_typ).

The layout is extracted after placing connection from layout to bondpad connectors to ensure that the parasitic resistance of these wires are also taken into consideration.The following are the results are obtained from simulating this extracted layout.

From the simulation the following results are obtained.

- DC-gain = 95.13dB
- Unity gain frequency = 1.752MHz
- phase margin = 81.83^0

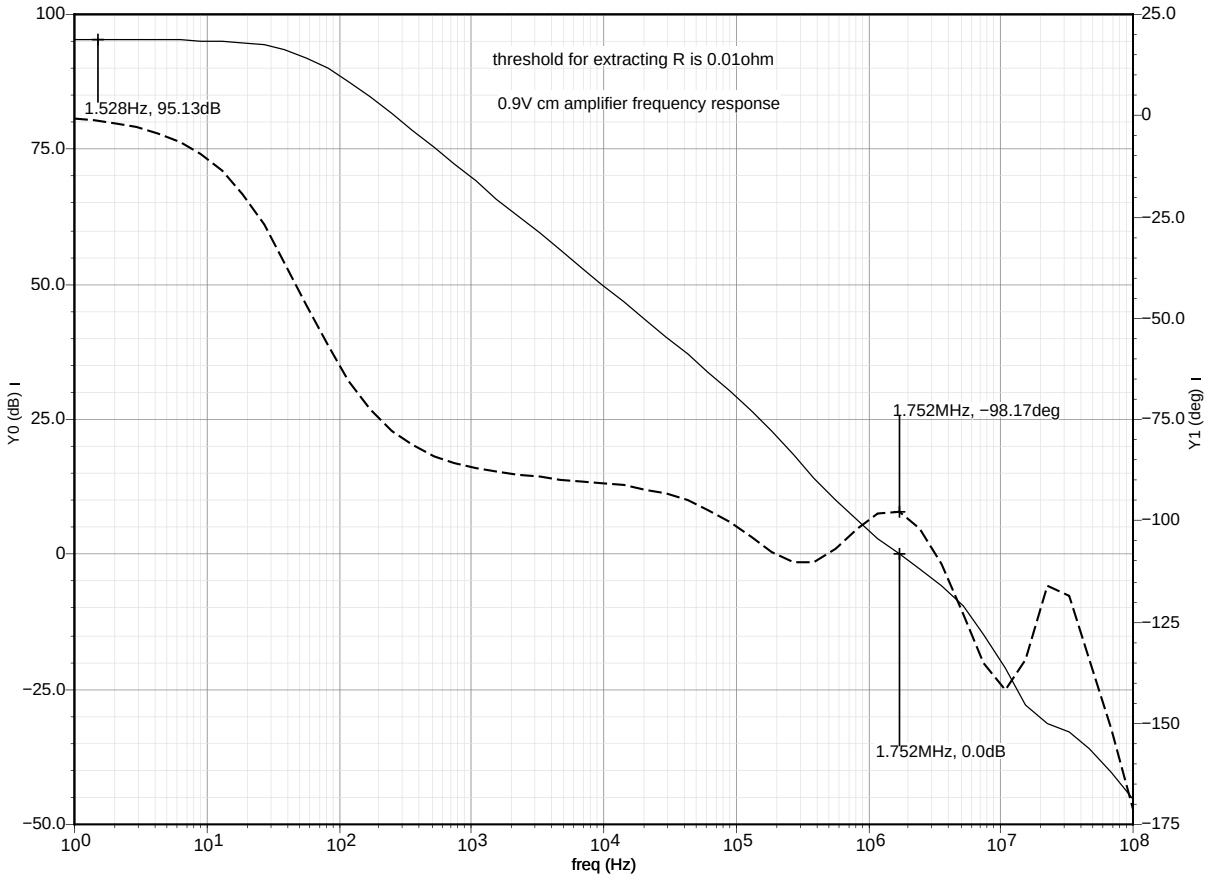


Figure 6.1: Frequency response.

6.1.2 Transient response and distortion

The opamp is connected in unity gain inverter configuration using two 20 kΩ resistors and sinusoid of frequency $\frac{7*10k}{64} = 1093.75$ Hz is applied at the input. The amplitude of the input sinusoid is gradually increased until the distortion increases due to operation of the class-AB stage transistors in deep triode region. This simulation is done with extracted layout without the extra connections to the padframe.

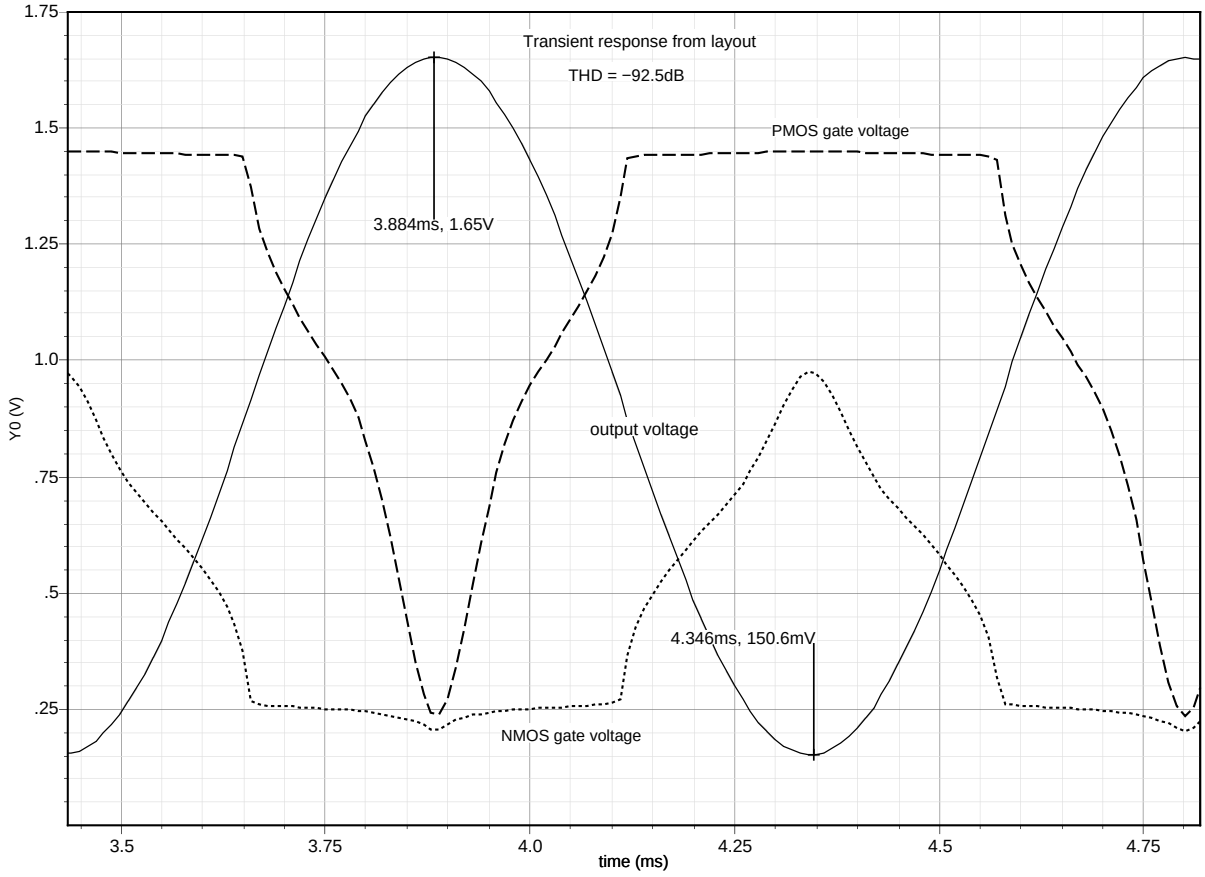


Figure 6.2: Output waveform for 1.5V peak-peak input voltage.

- THD@1093.75 Hz = -92.53 dB before connecting padframe wires.
- THD@1093.75 Hz = -89.08 dB after connecting padframe wires.

The gate voltage swing for PMOS and NMOS of class-AB stage is shown in the Fig. 6.3 with V_{in}. Also current through PMOS and NMOS are plotted in the Fig. 6.4 varying V_{in}.

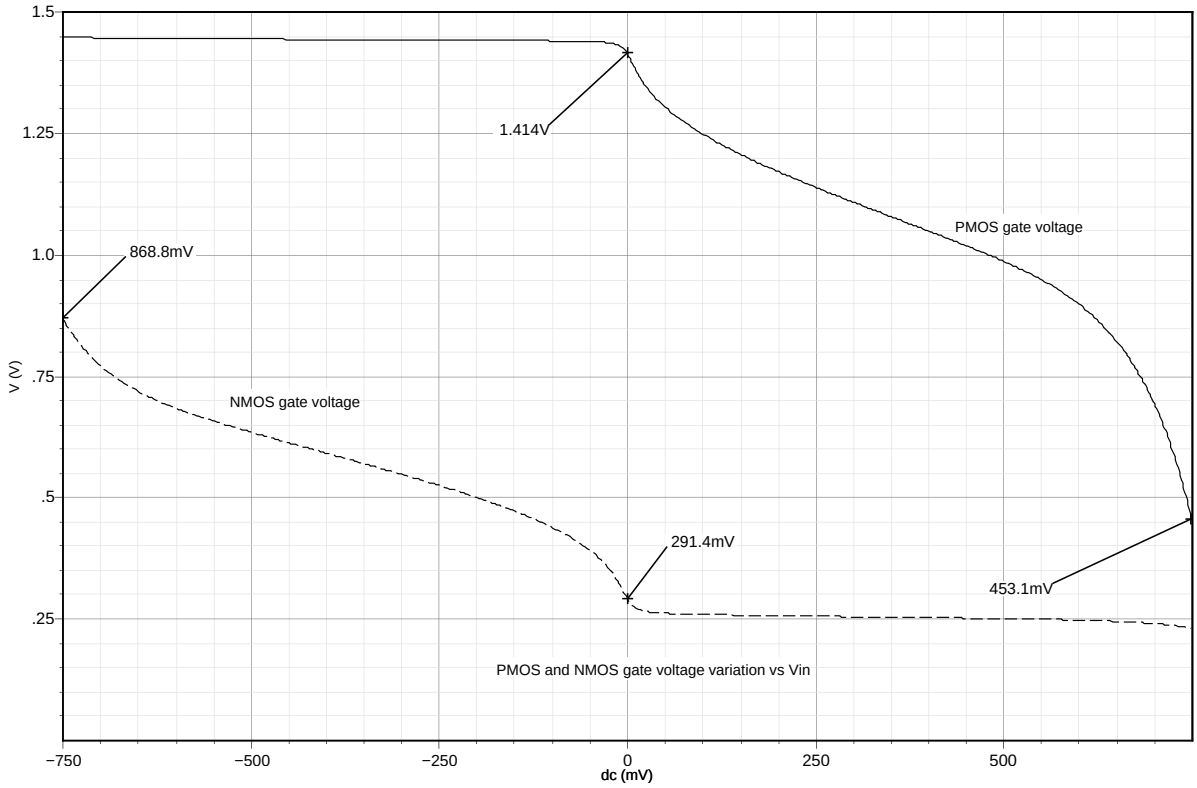


Figure 6.3: The gate voltage swing for output PMOS and NMOS vs Vin.

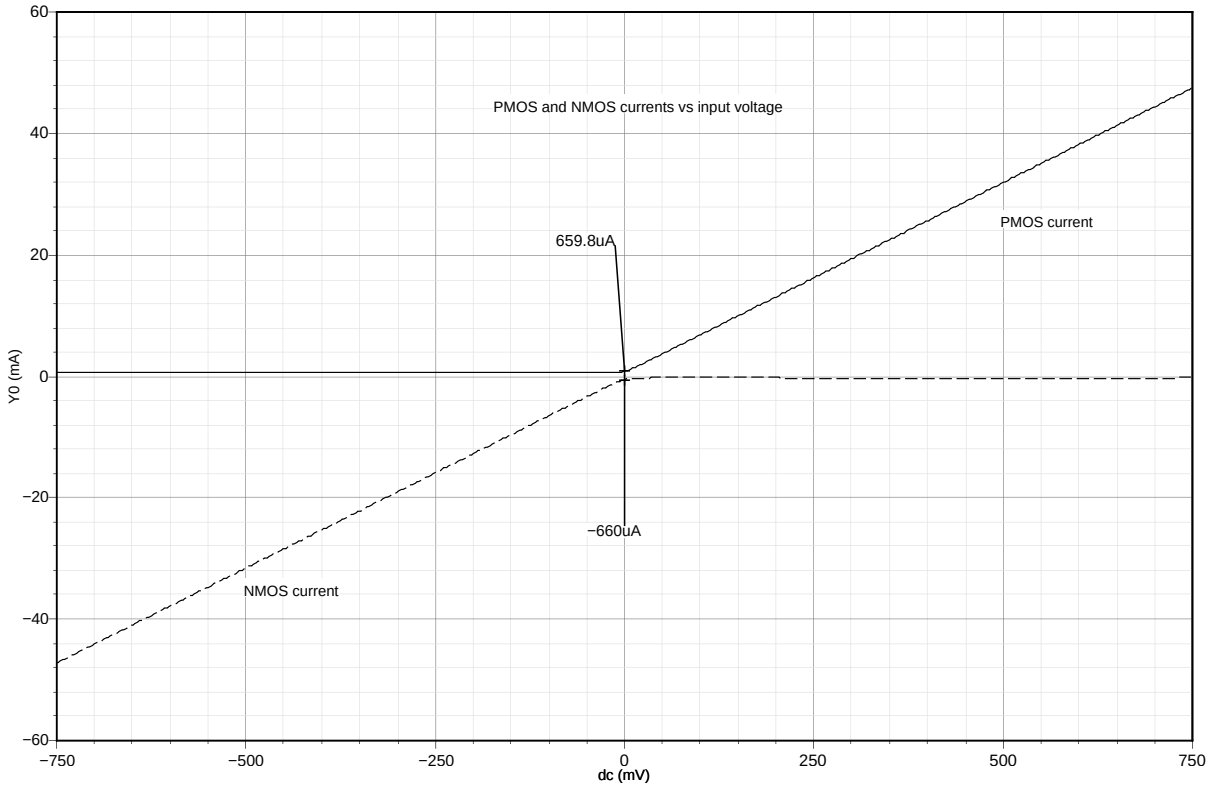


Figure 6.4: The PMOS and NMOS current vs Vin.

6.1.3 Transfer characteristics

Closed-loop transfer characteristics is shown in the Fig. 6.5.

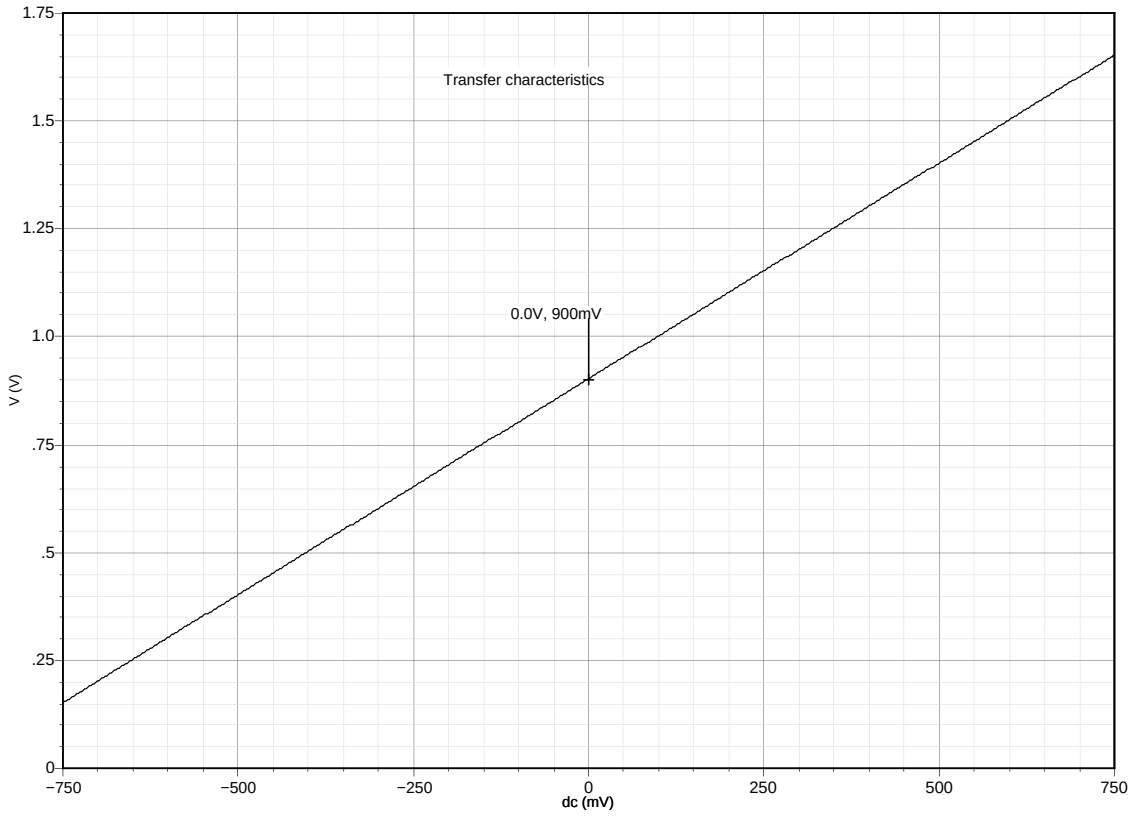


Figure 6.5: Closed loop transfer characteristics of the opamp.

6.1.4 Slew rate

The slew rate of the opamp is $100\,\mathrm{mV}/\mu\mathrm{s}$.

For an input change rate less than slew-rate, the output follows the input as shown in Fig. 8.6.

6.1.5 Noise analysis

The input referred integrated noise of the opamp at 70^0 C is $3.28\,\mu\mathrm{V}$. The $\frac{1}{f}$ corner frequency is 699 Hz.

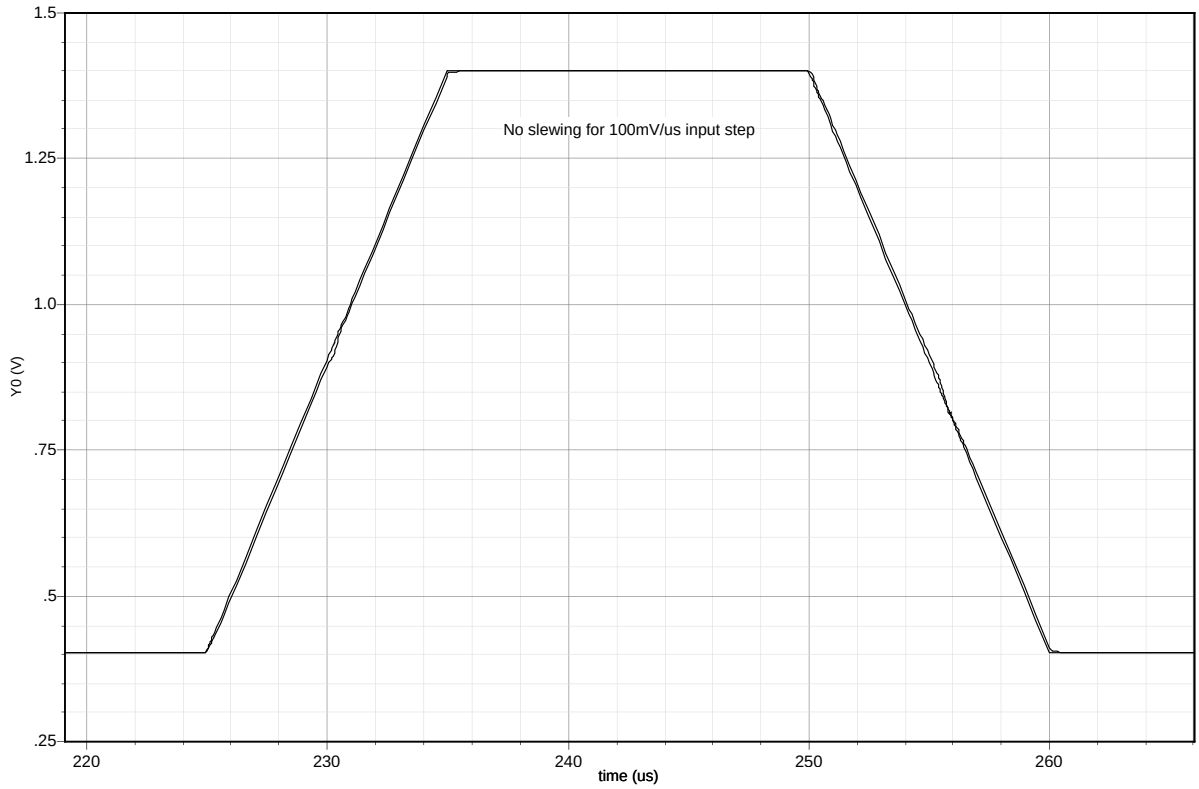


Figure 6.6: No slewing.

6.1.6 Area

- Total area = $73125\mu m^2 (195\,\mu m * 375\,\mu m)$
- Opamp area = $39000\mu m^2$
- Compensation capacitor area = $34125\,\mu m^2$

6.1.7 Power

Using supply of 1.8 V the total power consumed by the opamp is 1.394 mW with no input signal.

6.1.8 Layout

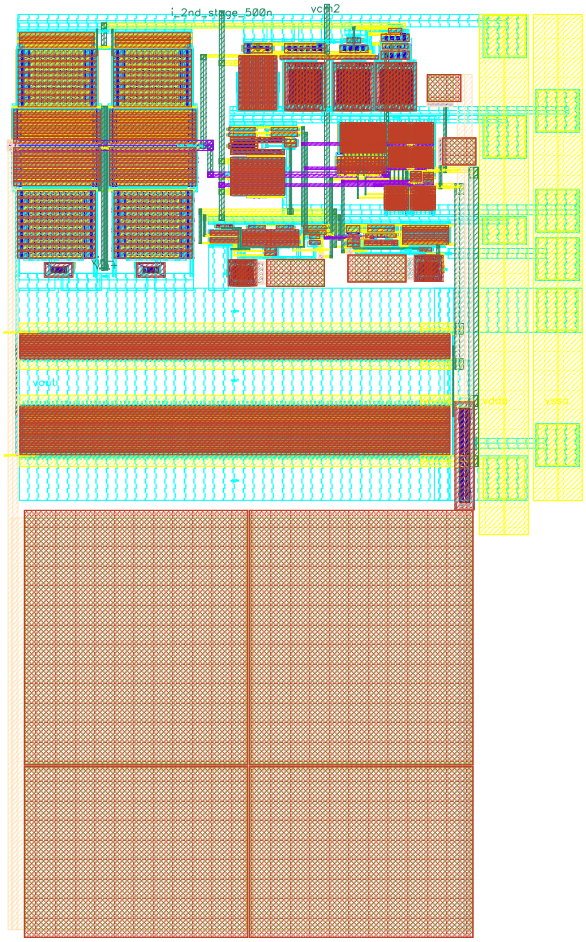


Figure 6.7: Layout of the opamp

CHAPTER 7

Ground centered opamp for $16\,\Omega$ load

In this chapter the design procedure of the ground centered opamp for 16Ω load is analyzed.

7.1 Objective

The ground centered opamp designed is supposed to be working in dual-supply mode and the negative supply is generated using the charge-pump based negative voltage converter. The ripple of the negative supply introduces distortion at the output of the opamp. This distortion can be reduced to a large extent by the following method.

Most of the gain of the three stage amplifier is provided by the first stage. Any voltage fluctuation at the ground pin of the first stage will be reflected at the output of the first stage and will increase distortion. If this stage is operated using only the positive supply and ground then this source of distortion can be avoided. Thus the first stage is operated from the positive supply and ground only.

Now, the second stage provide the biasing for the Class-AB stage. The biasing point for the output NMOS is negative. So the 2nd stage cannot be operated using positive supply and ground only.

Since the opamp is operated in dual supply configuration, if the input common mode voltage of the amplifier can be reduced to zero then it will eliminate the requirement of large DC blocking capacitor at the output. So we need to have a first stage which can have input common mode voltage to be zero while operating

between positive supply and zero and provide high gain required for this stage. Folded-cascode stage with PMOS input pair is thus a good choice for first stage. Since the major contribution of input referred noise is from the input pair, PMOS input pair is chosen for less flicker noise compared to NMOS.

7.1.1 Class-AB biasing

Here the class-AB biasing scheme is same as in the previously designed amplifier. The following Fig. 7.3 and Fig. 7.4 are the total transistor level circuit.

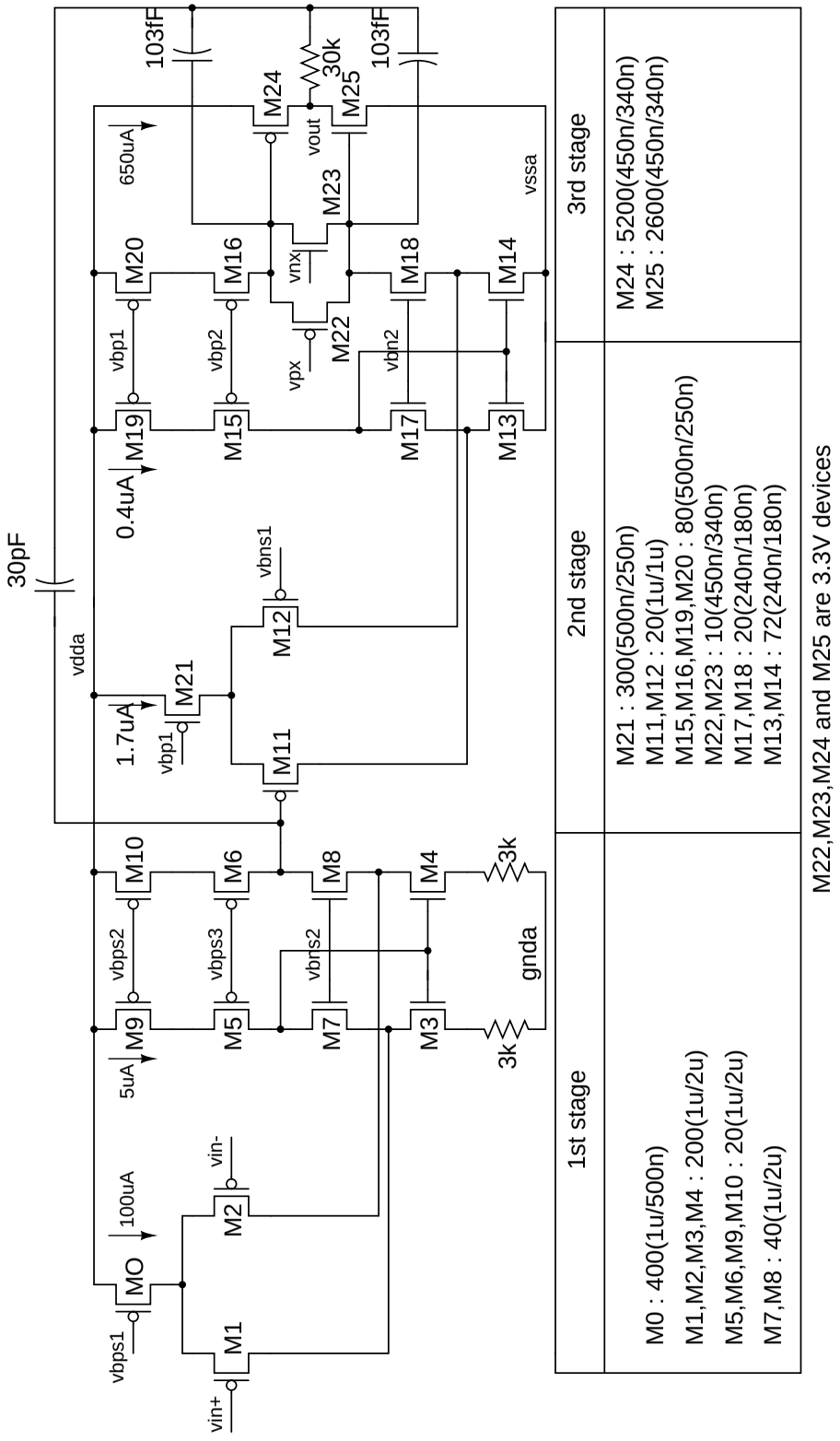


Figure 7.1: Three-stage opamp schematic.

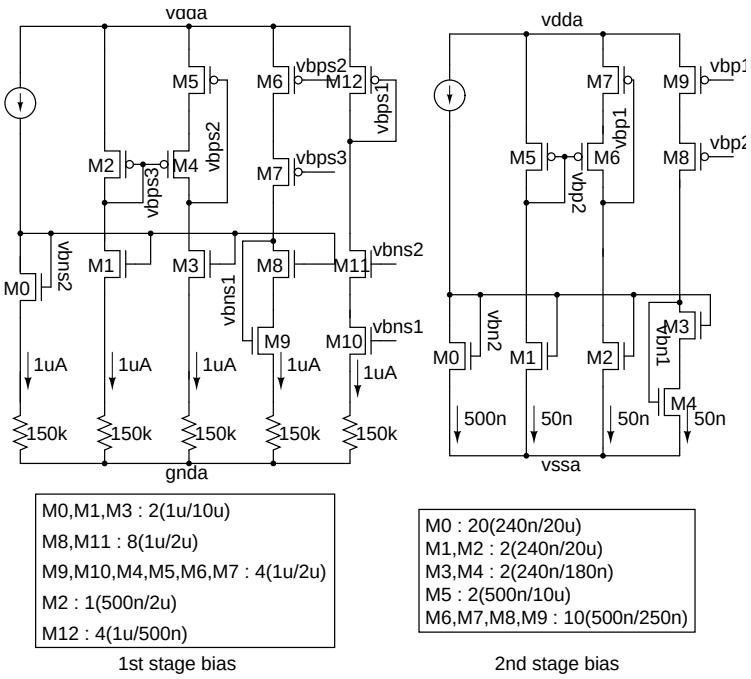


Figure 7.2: First and second stage bias schematic.

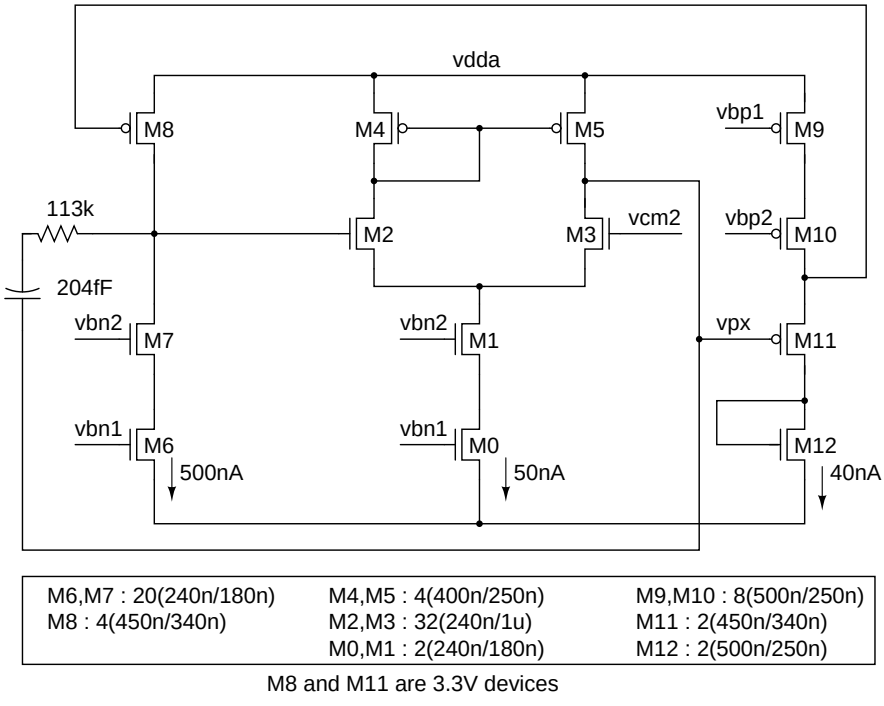


Figure 7.3: Class-AB stage PMOS bias schematic.

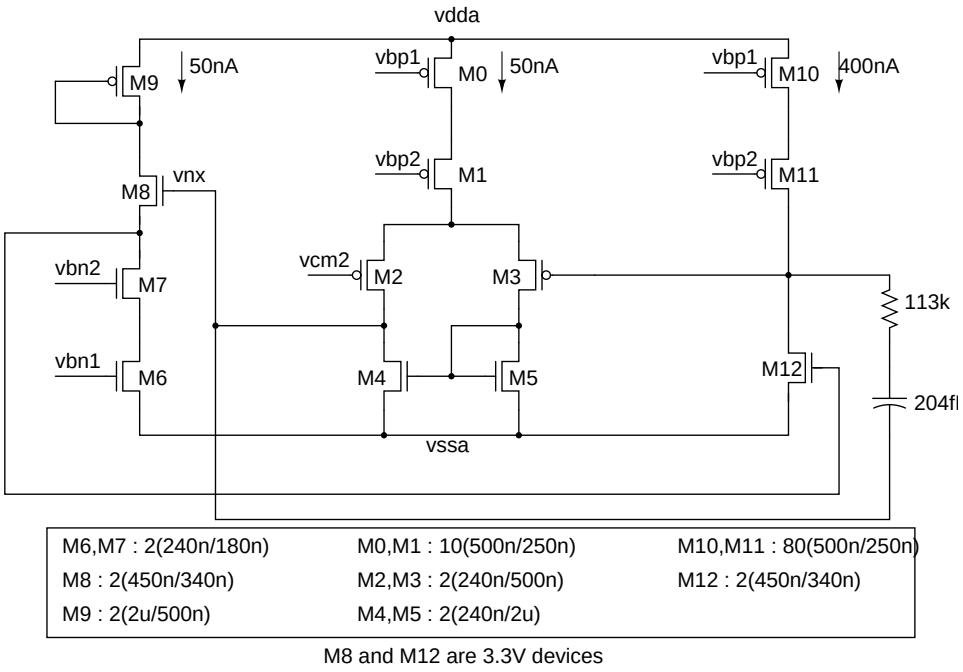


Figure 7.4: Class-AB stage NMOS bias schematic.

CHAPTER 8

Simulation and layout results for the 0 V common mode voltage 16 Ω driver

8.1 Results

The three stage opamp was also simulated and laid out using UMC180 μm technology. The following performance parameters are discussed consecutively.

- Open-Loop frequency response
- Transient response and Distortion
- Transfer characteristics
- Positive and Negative Slew rate
- Noise
- Area
- Power

8.1.1 Open-loop frequency response

The opamp was simulated with 16 Ω, 100 pF load at 70^0C at corner(tt, res_typ, mimcaps_typ).

The following are the results are obtained from simulating this extracted layout with bondpad connecting wires.

From the simulation the following results are obtained.

- DC-gain = 106.3 dB
- Unity gain frequency = 2.177 MHz
- phase margin = 71.9^0

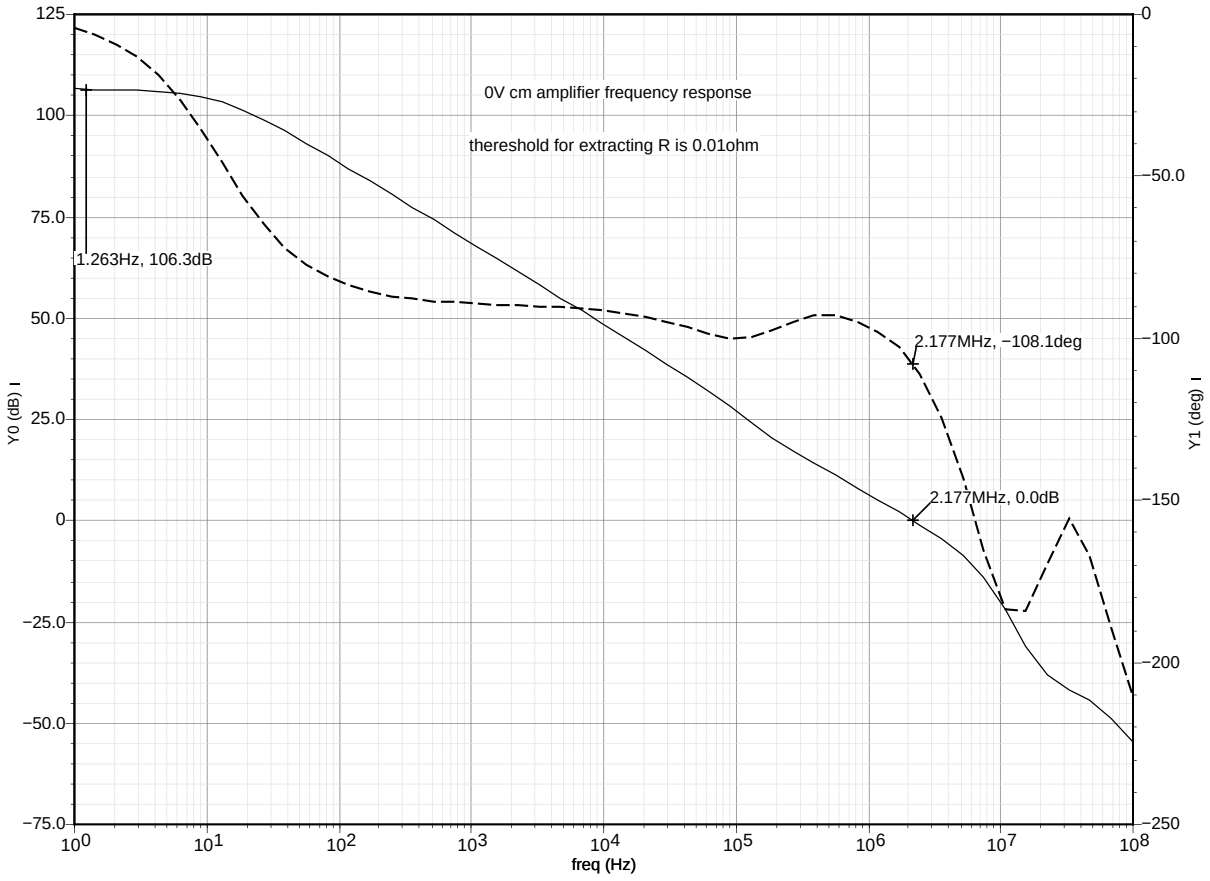


Figure 8.1: Frequency response.

8.1.2 Transient response and distortion

The opamp is connected in unity gain inverter configuration using two 20kΩ resistors and sinusoid of frequency $\frac{7*10\,\mathrm{k}}{64} = 1093.75\,\mathrm{Hz}$ is applied at the input. The amplitude of the input sinusoid is gradually increased until the distortion increases due to operation of the class-AB stage transistors in deep triode region.This simulation is done with extracted layout without the extra connections to the padframe.

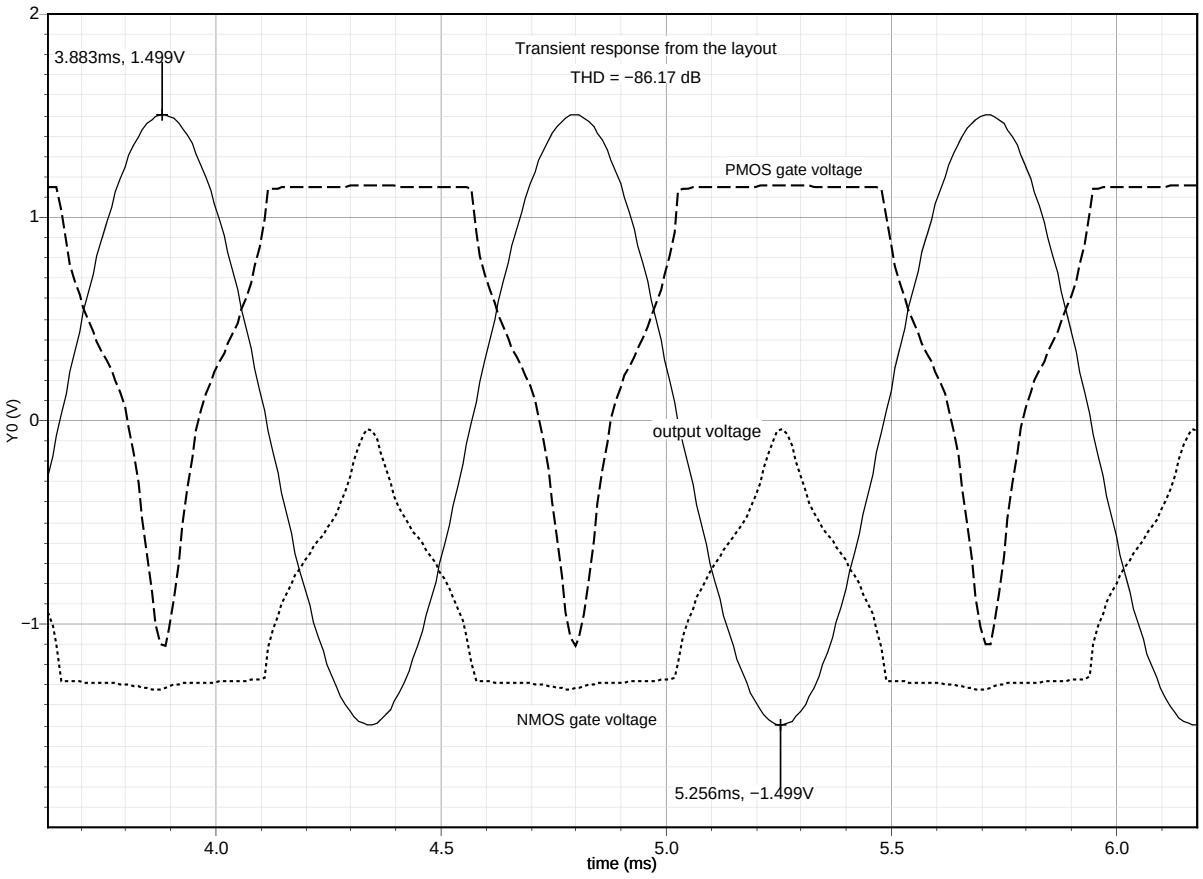


Figure 8.2: Output waveform for 3V peak-peak input voltage.

- THD1093.75 Hz = -86.17 dB before connecting padframe wires.
- THD1093.75 Hz = -85.28 dB after connecting padframe wires.

The gate voltage swing for PMOS and NMOS of class-AB stage is shown in the Fig. 8.3 with V_{in}. Also current through PMOS and NMOS are plotted in the Fig. 8.4 varying V_{in}.

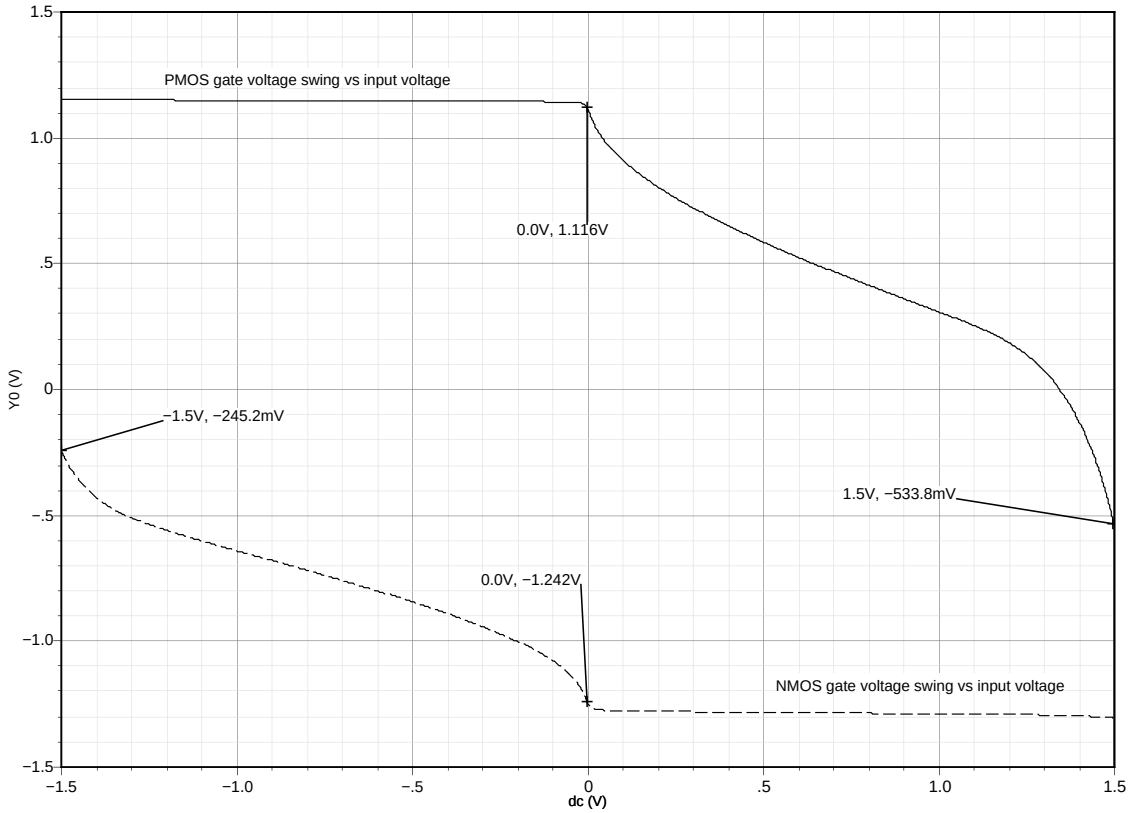


Figure 8.3: The gate voltage swing for output PMOS and NMOS vs Vin.

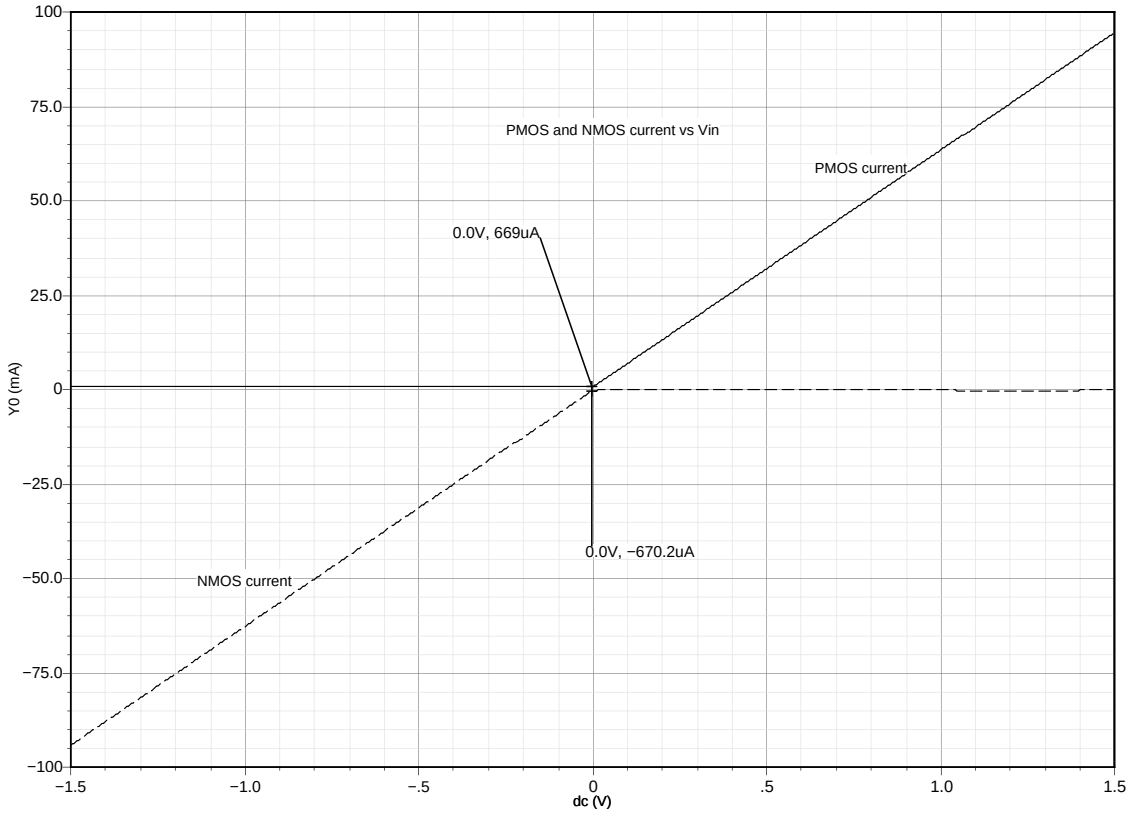


Figure 8.4: The PMOS and NMOS current vs Vin.

8.1.3 Transfer characteristics

Closed-loop transfer characteristics is shown in the Fig. 8.5.

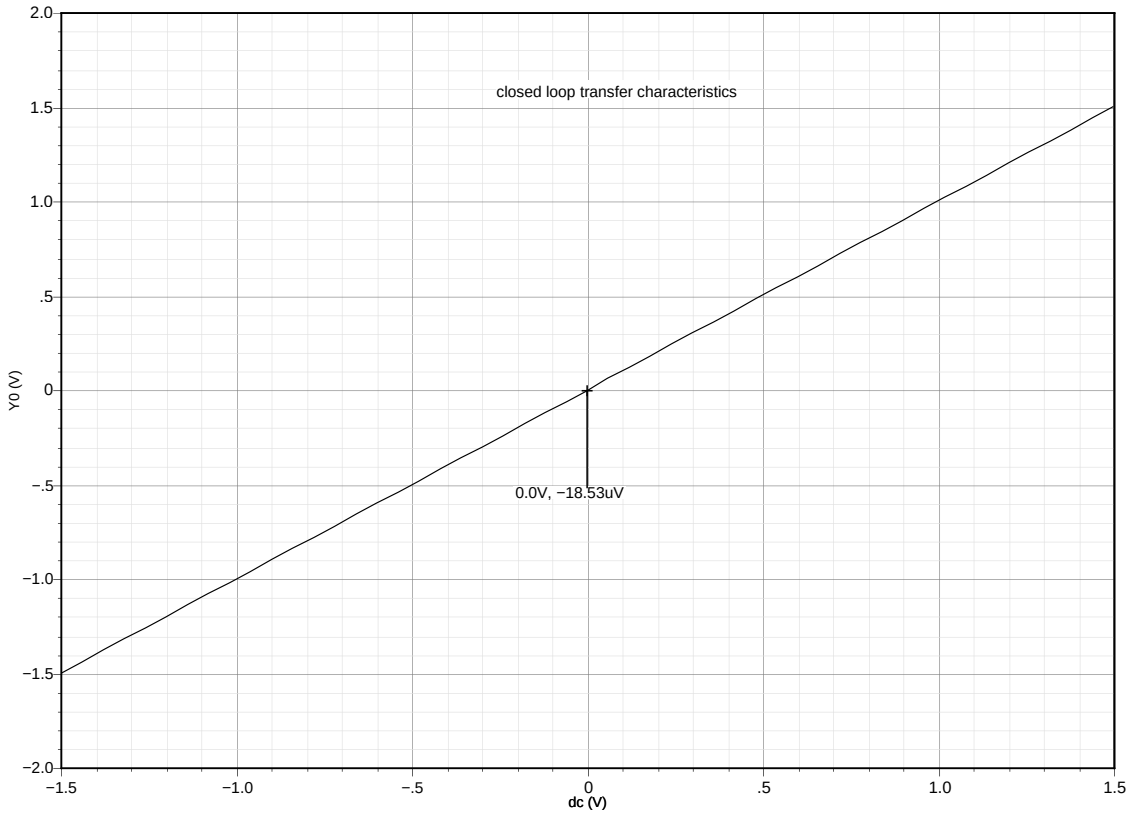


Figure 8.5: Closed loop transfer characteristics of the opamp.

8.1.4 Slew rate

The slew rate of the opamp is $150mV/\mu s$.

For an input change less than slew-rate,the output follows the input as shown in Fig. 8.6.

8.1.5 Noise analysis

The input referred integrated noise of the opamp at 70^0 C is $3.417\,\mu$V. The $\frac{1}{f}$ corner frequency is 817 Hz.

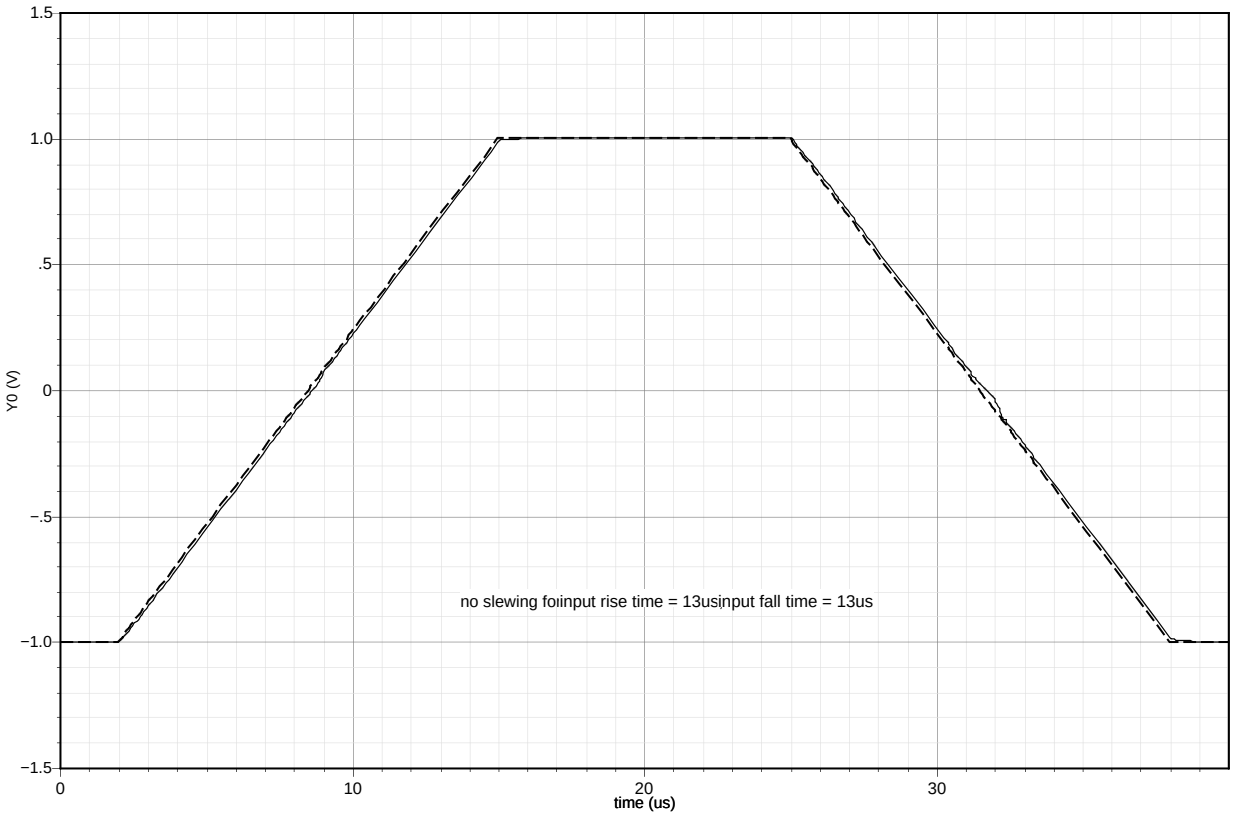


Figure 8.6: No slewing.

8.1.6 Area

- Total area = 90710 μm^2(235 μm $*$ 386μm)
- Opamp area = 55460 μm^2
- Compensation capacitor area = 34075 μm^2

8.1.7 Power

Using dual supply of 1.8 V and -1.8 V the total power consumed by the opamp is 2.65 mW.

8.1.8 Layout

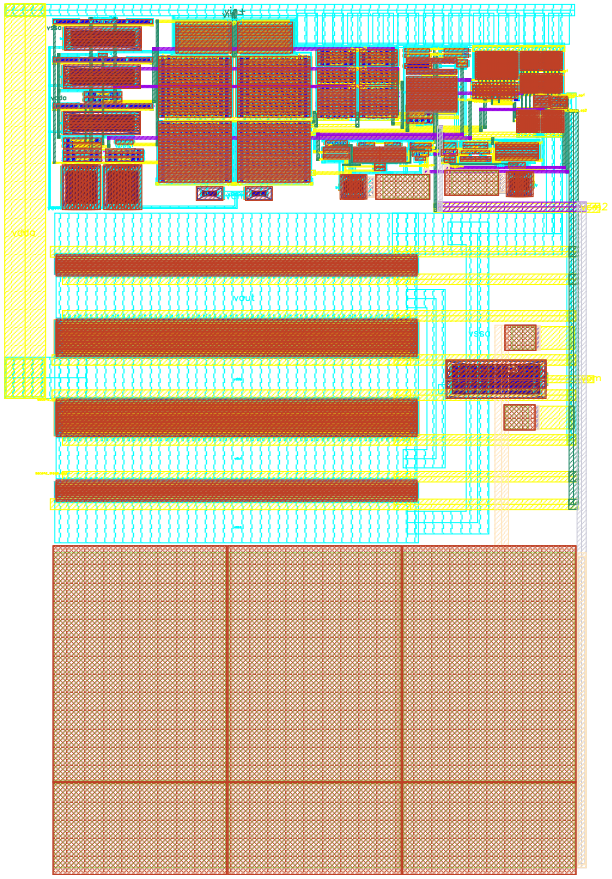


Figure 8.7: Layout of the opamp

CHAPTER 9

Simulation results of Direct-Drive amplifier

9.1 Transient response and distortion of the ground centered opamp when supplied from the negative voltage converter

The ground centered opamp is simulated for distortion along with the negative voltage converter circuit described in chapter 3 in the following two configurations. The frequency at which the negative voltage converter is operated is 227.27 kHz. At this frequency with $C_1 = 4.4\,\mu$F and $C_2 = 2.2\,\mu$F the output voltage ripple of the charge pump is 100 mV for 100 mA of load current. Input signal is $\frac{7*10k}{64}$ Hz = 1093.75 Hz with peak to peak amplitude of 2.4 V.

9.1.1 Configuration 1

All the stages of the opamp are supplied with positive supply and negative supply generated from the charge-pump circuit. Two simulations are done with varying the capacitor at the output of the inverter. Fig. 9.1 is the plot of the output voltage of the opamp and the output voltage of the negative voltage converter in this configuration. Here $C_1 = 2.2\,\mu$F is used and THD obtained is -53.56 dB. Fig. 9.2 is the same plot with $C_1 = 10\,\mu$F. THD obtained in this configuration is -66.98 dB.Less distortion is due to less ripple at the output of the negative voltage converter.

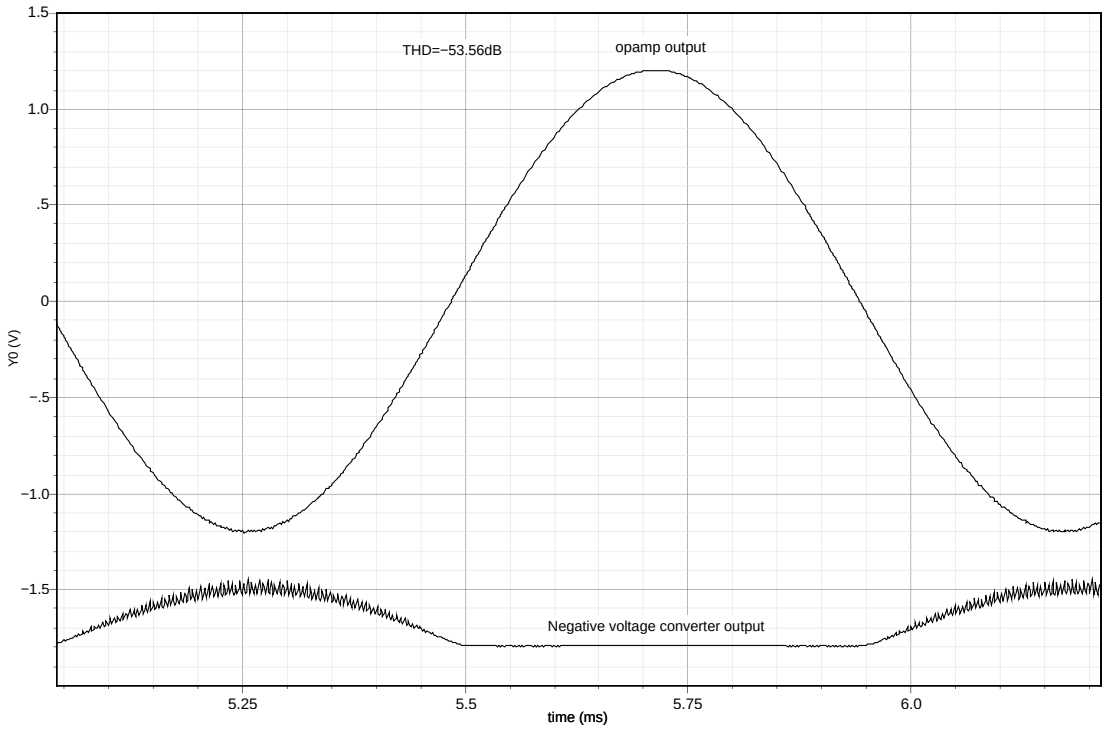


Figure 9.1: All stages are using dual supply with 2.2μF cap at the output of the inverter.This gives THD=-53.56dB

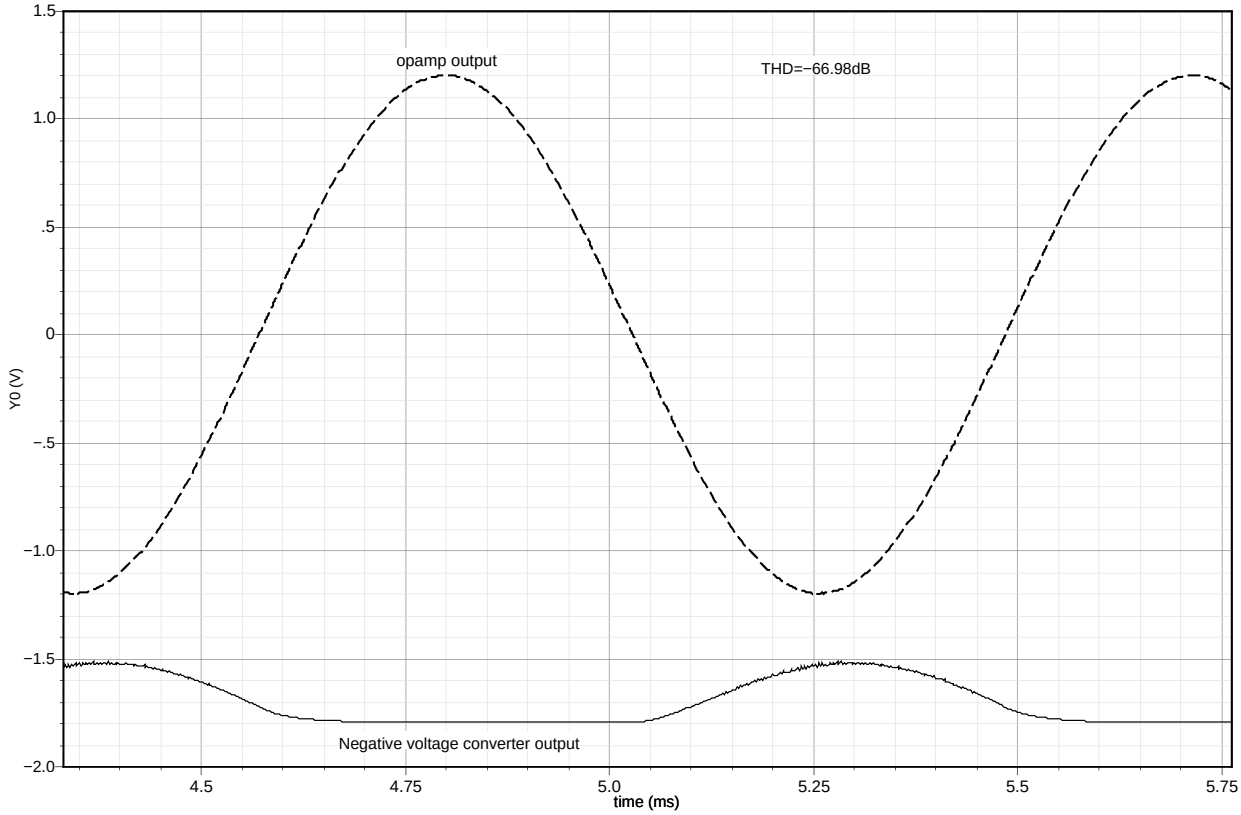


Figure 9.2: All stages dual supply with 10μF cap at the output of the inverter.This gives THD =-66.98dB

9.1.2 Configuration 2

In this configuration the first stage of the opamp uses positive supply and ground and the 2nd and 3rd stages use both the positive supply and the negative supply generated from the charge-pump circuit. Two simulations are done with varying the capacitor at the output of the inverter. Fig. 9.3 is the plot of the output voltage of the opamp and the output voltage of the negative voltage converter in this configuration. Here $C_1 = 2.2\,\mu$F and THD obtained is $-70\,$dB. Fig. 9.4 is the same plot with $C_1 = 10\,\mu$F. THD obtained in this configuration is $-84.32\,$dB. The less distortion results from less ripple in the negative supply with higher value of capacitor.

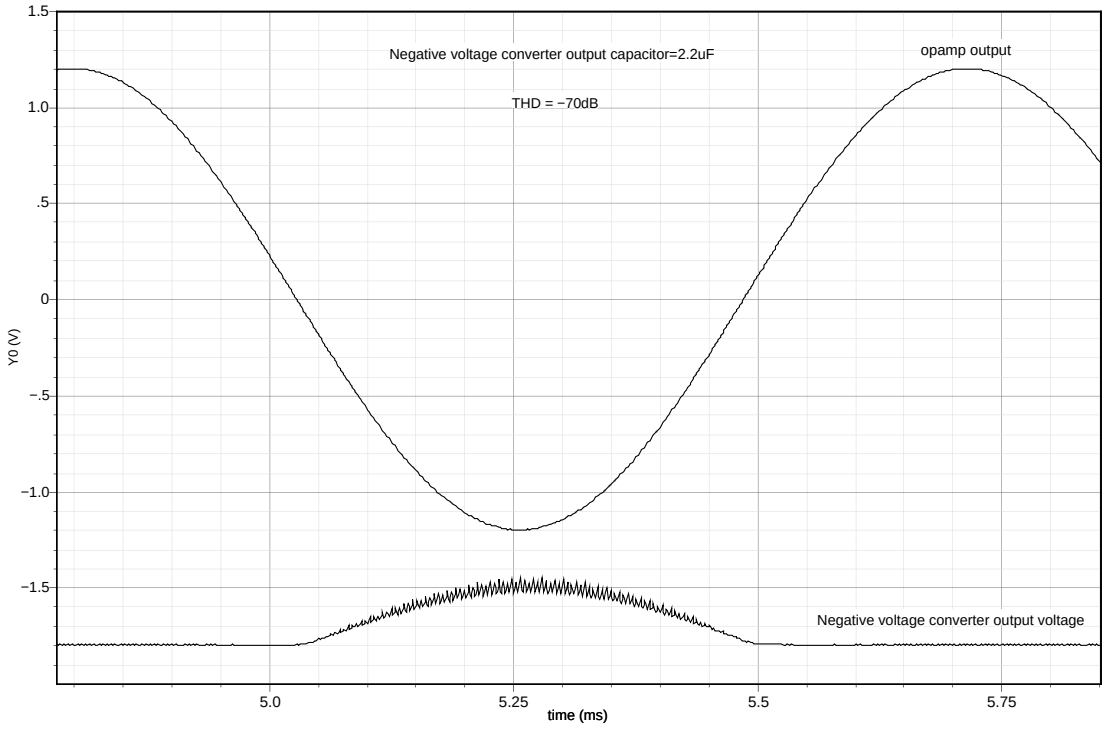


Figure 9.3: 1st stage positive supply and other stages dual supply with $2.2\,\mu F$ cap at the output of the inverter.This gives THD=$-70\,$dB

We see from the above simulation that the distortion in configuration 2 is much less than in configuration 1. Thus if the ground centered opamp is used in configuration 2 with negative voltage converter, we get distortion improvement

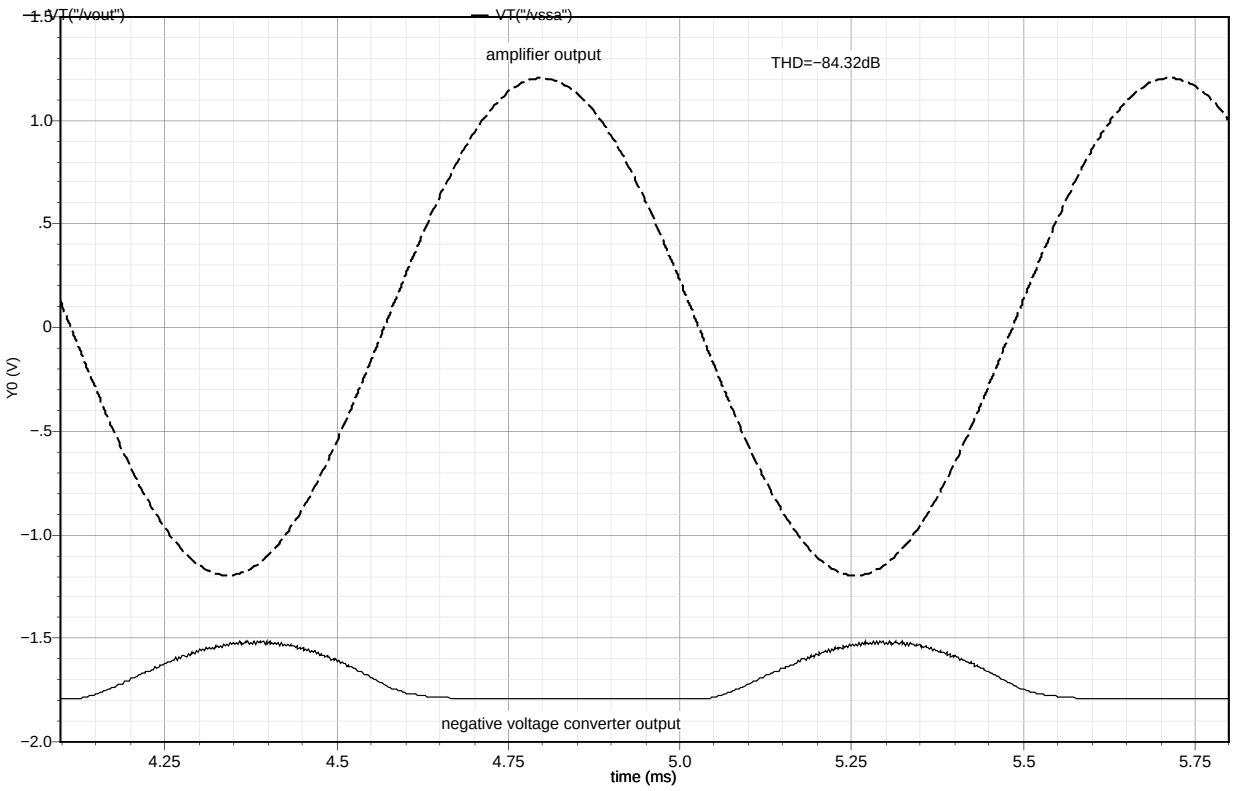


Figure 9.4: 1st stage positive supply and other stages dual supply with $10\,\mu F$ cap at the output of the inverter.This gives THD=-84.32 dB

Output Cap(μF)	THD in Configuration 1(dB)	THD in Configuration 2(dB)
2.2	-53.56	-70
10	-66.98	-84.32

Table 9.1: THD in the two configurations

compared to general configuration 1.

CHAPTER 10

Conclusion and future work

The Miller compensation with nulling resistor architecture was used to obtain high gain in the amplifiers designed. However, the compensation capacitors used are as large as 30 pF. Feedforward compensation scheme can be used to reduce the number and values of the compensation capacitors used. The peak driving capability of the ground centered opamp is around ±100 mA. The quiescent current consumption is 650 μA in the last stage(class-AB) and 100 μA in the first stage(folded cascode). The bandwdith of the opamp is 2.177 MHz. The distortion introduced by the opamp is less than −85 dB. The ratio of peak current to the quiescent current controls the distortion. The above operational amplifier was designed for a driver load of 16 Ω, 100 pF. However, the output stage can be scaled to modify the driver for other load specifications. This ground centered opamp uses single supply for the first stage which reduces distortion introduced by the charge pump output voltage fluctuations. Thus the proposed architecture is suitable Direct -Drive amplifier design. Also the 0.9 V common mode voltage opamp is suitable for single supply operation for 16 Ω, 100 pF load. The peak driving capability of the this opamp is around ±47 mA. The quiescent current consumption is 650 μA in the last stage(class-AB) and 100 μA in the first stage(telescopic cascode). The bandwdith of the opamp is 1.75 MHz. The distortion introduced by the opamp is less than −89 dB. The negative voltage converter designed for 16 Ω load can be operated over a wide range of frequencies and output capacitors can be scaled accordingly for desired ripple specification.

APPENDIX A

MATLAB code of the macro model for the three stage opamp

A.1 Code for 0.9 V common mode opamp

The following is the MATLAB code with the device parameter extracted from the dc simulation of the actual circuit.

```
clc;
% insert C1 & C2 values here from captab
C1 = 0.565e-12;
C2 = 1.5e-12 + 0.662e-12;
C3 = 100e-12;   %100pF load capacitor
CM1 = 30e-12;   %30pF miller cap to 1st stage
CM2 = 0.2e-12;  %200fF miller cap to second stage
rload = 16;     %16 ohm load resistance
RZ = 10e3;      %10k ohm series resistance with miller cap
GZ = 1/RZ;
%--------for 1st stage telescopic cascode--------------
rdz1 = 3e3;     %3k ohm degeneration resistance of the first stage
GM1 = 618.2e-6 ;  %gm of the first stage(gm of input pmos)
gds11 = 1.169e-6; %input pmos
gm15 = 751e-6 ; %cascode pmos
gds15 =5.765e-6 ; %cascode pmos
gm17 =1.131e-3 ;  %cascode nmos
gds17 =17.81e-6 ; %cascode nmos
gds13 =22.3e-6 ; %current mirror nmos
gm13 =999.5e-6 ; %current mirror nmos
GDS1 = (gds11*gds15/gm15)+
    ((gds13*gds17)/(gm13+((gm17+gds17)*(1+((gm13+gds13)/rdz1)))));%gds of stage1
disp('gm1 ');
```

```
disp(GM1);
disp('gds1 ');
disp(GDS1);
disp('C1');
disp(C1);
gain1 = 20*log10(GM1/GDS1);
disp('gain1 ');
disp(gain1);

GM1=-GM1;
%------for 2nd stage folded cascode ----------------
GM2 = 17.54e-6;      %gm of the second stage(gm of input pmos)
gds21 = 35.63e-9;  %input pmos
gm25 = 8.885e-6 ;  %cascode pmos
gds25 = 138.2e-9; %cascode pmos
gds23 = 153e-9; %current mirror pmos
gm27 = 9.26e-6;  %cascode nmos
gds27 = 733e-9; %cascode nmos
gds29 = 2.341e-6;    %current mirror nmos
GDS2 = ((gds21+gds29)*gds27/gm27)+(gds23*gds25/gm25);  %gds of the second stage
gain2 = 20*log10(GM2/GDS2);
disp('gm2 ');
disp(GM2);
disp('gds2 ');
disp(GDS2);
disp('C2');
disp(C2);
disp('gain2 ');
disp(gain2);
%----------for class AB----------------
gm3p= 11.37e-3;  %output pmos
gm3n= 12.62e-3;  %output nmos
GM3 = gm3p+gm3n; %gm of the third stage
gds3p=273.7e-6;  %output pmos
gds3n=541.7e-6;    %output nmos
GDS3 = gds3p + gds3n + (1/rload); %gds of the third stage including load
RL = 1/GDS3;
gain3 = 20*log10(GM3/GDS3);
```

```
disp('gm3 ');
disp(GM3);
disp('gL ');
disp(GDS3);
disp('C3');
disp(C3);
disp('gain3 ');
disp(gain3);

GM3=-GM3;

disp('CM1');
disp(CM1);
disp('CM2');
disp(CM2);
%------------transfer function construction-------------------------------
K = -(C1*CM1*(C2+CM2))-(C2*CM2*(C1+CM1));

A11 = (C2*((GM2*CM1)+(GDS1*CM2))+(GDS1*CM1*(C2+CM2))-(CM1*(C2+CM2)*(GM2-GZ)))/K;
A12 = (-(C2*CM1*GDS2)+(GDS2*CM1*(C2+CM2)))/K;
A13 = -(GZ*CM1*(C2+CM2))/K;
A14 = -(GZ*CM1*(C2+CM2))/K;
B1 = (-(C2*GM1*CM2)-(CM1*GM1*(C2+CM2)))/K ;

A21 = ((GDS1*CM2*(C1+CM1))-(C1*((GM2*CM1)+(GDS1*CM2)))
        -(CM2*(C1+CM1)*(GM2-GZ)))/K ;
A22 = ((C1*CM1*GDS2)+(GDS2*CM2*(C1+CM1)))/K;
A23 = -(GZ*CM2*(C1+CM1))/K;
A24 = -(GZ*CM2*(C1+CM1))/K;
B2 = ((C1*GM1*CM2)-(CM2*GM1*(C1+CM1)))/K ;

DK = -(K*CM1);
A41 = (-(C1*CM1*(C2+CM2)*(GM2-GZ))+(C1*C2*((GM2*CM1)+(GDS1*CM2)))
        -(C2*CM2*GDS1*(C1+CM1)))/DK;
A42 = ((C1*CM1*(C2+CM2)*GDS2)-(C1*C2*CM1*GDS2))/DK;
A43 = -(GZ*CM1*C1*(C2+CM2))/DK;
A44 = -(GZ*CM1*C1*(C2+CM2))/DK;
B4 = (-(C1*C2*GM1*CM2)+(C2*CM2*(C1+CM1)*GM1))/DK ;
```

```
A31 = GZ/C3;
A32 = GM3/C3;
A33 = -(GZ+GDS3)/C3;
A34 = -GZ/C3;
B3 = 0;


A = [A11 A12 A13 A14 ;A21 A22 A23 A24 ;A31 A32 A33 A34 ;A41 A42 A43 A44];
B = [B1; B2; B3; B4];
C = [0 0 1 0];
D = [0];

ABCD = ss(A,B,C,D);
trfn=tf(ABCD)%transfer function construction
[b,a]=tfdata(trfn,'v'); %b contains numerator & a contains denominator poly
h=bodeplot(trfn,{10,1e9});
setoptions(h,'FreqUnits','Hz','PhaseVisible','on');
grid on;

num = roots(b);
den = roots(a);
disp('zeros')
disp(num(1)/(2*pi))
disp(num(2)/(2*pi))
disp('poles')
disp(den(1)/(2*pi))
disp(den(2)/(2*pi))
disp(den(3)/(2*pi))
disp(den(4)/(2*pi))

[Gm,Pm,Wg,Wp] = margin(trfn);
Wp=Wp/(2*pi); %frequency in Hertz
Wg=Wg/(2*pi); %frequency in Hertz
disp('this is phase margin ');
disp(Pm);
disp('unity gain frequency');
disp(Wp);
```

A.2 Code for 0 V common mode opamp

```
clc;
% insert C1 & C2 values here from captab
C1 = 0.103e-12;
C2 = 3.72e-12 + 1.915e-12;
C3 = 100e-12;   %100pF load capacitor
CM1 = 30e-12;   %30pF miller cap to 1st stage
CM2 = 0.2e-12;  %200fF miller cap to second stage
rload = 16;     %16 ohm load resistance
RZ = 30e3;      %30k ohm resistance in series with miller cap
GZ = 1/RZ;
%-------for 1st stage folded cascode-------------
rdz1 = 3e3;     %3k ohm degeneration resistance of the first stage
GM1 = 586.6e-6 ;  %gm of the first stage(gm of input pmos)
gds11 = 1.391e-6; %input pmos
gds12 =1.1e-6 ; %current mirror pmos
gm15 = 59.41e-6 ; %cascode pmos
gds15 =106e-9 ; %cascode pmos
gm17 =107.4e-6 ;  %cascode nmos
gds17 =1.732e-6 ; %cascode nmos
gds13 =44.21e-6 ; %current mirror nmos
gm13 =1040e-6 ; %current mirror nmos
GDS1 = (gds12*gds15/gm15)  +  (gds17/(1+(((gm17+gds17)*((gm13+gds13+(1/rdz1))))
    /((gds11*(gm13+gds13))+((1/rdz1)*(gds13+gds11))))));  %gds of the first stage
disp('gm1 ');
disp(GM1);
disp('gds1 ');
disp(GDS1);
disp('C1 ');
disp(C1);
gain1 = 20*log10(GM1/GDS1);
disp('gain1 ');
disp(gain1);

GM1=-GM1;
%-------for 2nd stage folded cascode ----------------
```

```
GM2 = 16.78e-6;      %gm of the second stage(gm of input pmos)
gds21 = 33.37e-9;  %input pmos
gm25 = 9.347e-6 ;  %cascode pmos
gds25 = 94.99e-9; %cascode pmos
gds23 = 157.5e-9; %current mirror pmos
gm27 = 9.869e-6;  %cascode nmos
gds27 = 478e-9; %cascode nmos
gds29 = 2.263e-6;    %current mirror nmos
GDS2 = ((gds21+gds29)*gds27/gm27)+(gds23*gds25/gm25);  %gds of the second stage
gain2 = 20*log10(GM2/GDS2);
disp('gm2 ');
disp(GM2);
disp('gds2 ');
disp(GDS2);
disp('C2 ');
disp(C2);
disp('gain2 ');
disp(gain2);
%-------------for class AB-------------------
gm3p= 10.26e-3;  %output pmos
gm3n= 12.15e-3;  %output nmos
GM3 = gm3p+gm3n; %gm of the third stage
gds3p=159.4e-6;  %output pmos
gds3n=275.8e-6;    %output nmos
GDS3 = gds3p + gds3n + (1/rload); %gds of the third stage including load
RL = 1/GDS3;
gain3 = 20*log10(GM3/GDS3);
disp('gm3 ');
disp(GM3);
disp('gL ');
disp(GDS3);
disp('C3 ');
disp(C3);
disp('gain3 ');
disp(gain3);

GM3=-GM3;
```

```
disp('CM1 ');
disp(CM1);
disp('CM2 ');
disp(CM2);
%------------transfer function construction-----------------------------------

K = -(C1*CM1*(C2+CM2))-(C2*CM2*(C1+CM1));

A11 = (C2*((GM2*CM1)+(GDS1*CM2))+(GDS1*CM1*(C2+CM2))-(CM1*(C2+CM2)*(GM2-GZ)))/K;
A12 = (-(C2*CM1*GDS2)+(GDS2*CM1*(C2+CM2)))/K;
A13 = -(GZ*CM1*(C2+CM2))/K;
A14 = -(GZ*CM1*(C2+CM2))/K;
B1 = (-(C2*GM1*CM2)-(CM1*GM1*(C2+CM2)))/K ;

A21 = ((GDS1*CM2*(C1+CM1))-(C1*((GM2*CM1)+(GDS1*CM2)))
        -(CM2*(C1+CM1)*(GM2-GZ)))/K ;
A22 = ((C1*CM1*GDS2)+(GDS2*CM2*(C1+CM1)))/K;
A23 = -(GZ*CM2*(C1+CM1))/K;
A24 = -(GZ*CM2*(C1+CM1))/K;
B2 = ((C1*GM1*CM2)-(CM2*GM1*(C1+CM1)))/K ;

DK = -(K*CM1);
A41 = (-(C1*CM1*(C2+CM2)*(GM2-GZ))+(C1*C2*((GM2*CM1)+(GDS1*CM2)))
    -(C2*CM2*GDS1*(C1+CM1)))/DK;
A42 = ((C1*CM1*(C2+CM2)*GDS2)-(C1*C2*CM1*GDS2))/DK;
A43 = -(GZ*CM1*C1*(C2+CM2))/DK;
A44 = -(GZ*CM1*C1*(C2+CM2))/DK;
B4 = (-(C1*C2*GM1*CM2)+(C2*CM2*(C1+CM1)*GM1))/DK ;

A31 = GZ/C3;
A32 = GM3/C3;
A33 = -(GZ+GDS3)/C3;
A34 = -GZ/C3;
B3 = 0;


A = [A11 A12 A13 A14 ;A21 A22 A23 A24 ;A31 A32 A33 A34 ;A41 A42 A43 A44];
B = [B1; B2; B3; B4];
```

```
C = [0 0 1 0];
D = [0];

ABCD = ss(A,B,C,D);
trfn=tf(ABCD)%transfer function construction
[b,a]=tfdata(trfn,'v');%b contains numerator and a denominator poly
h=bodeplot(trfn,{10,1e9});
setoptions(h,'FreqUnits','Hz','PhaseVisible','on');
grid on;

num = roots(b);
den = roots(a);
disp('zeros')
disp(num(1)/(2*pi))
disp(num(2)/(2*pi))
disp('poles')
disp(den(1)/(2*pi))
disp(den(2)/(2*pi))
disp(den(3)/(2*pi))
disp(den(4)/(2*pi))

[Gm,Pm,Wg,Wp] = margin(trfn);
Wp=Wp/(2*pi); %frequency in Hertz
Wg=Wg/(2*pi); %frequency in Hertz
disp('this is phase margin ');
disp(Pm);
disp('unity gain frequency');
disp(Wp);
```

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