Design of VCO For Frequency Synthesizer in ZigBee Transceiver

A Project Report

submitted by

L. MANOJ KUMAR

in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY
Microelectronics and VLSI Design

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

JULY 2008

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of VCO For Frequency Synthesizer in ZigBee Transceiver**, submitted by **L. Manoj Kumar**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Project Advisor
Assistant Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai
Date: 6th May 2007

ACKNOWLEDGEMENTS

As with any effort this project could not have been completed without the help and support of others. First of all I wish to thank my project guide Dr. Nagendra Krishnapura. I am very grateful to Dr. Nagendra Krishnapura for his excellent support and guidance throughout this Project. It was the analog IC design course taught by Dr. Nagendra Krishnapura motivated me a lot to get into the analog IC design, the course Broadband Communication circuits taught by him helped me a lot in understanding the project well. Your guidance throughout the cource of this project is greatly appreciated.

I thank all the members of the analog group for their support throughout this project especially for Asif, Hari Prasath and Manohar. Special thanks to Abishek.G for his excellent support in resolving the problems with Cadence software.

Finally I would like to thank my family and friends for their support and encouragement. My acknowledgments would not be complete without expressing my great fullness towards GOD. so a very very special thanks to GOD.

ABSTRACT

This work presents a design of voltage controlled Ring-oscillator(VCO) which is intended to operate as a frequency synthesizer in a PLL to generate the local oscillator frequency for a Zigbee transceiver. This work proposes a new architecture for the VCO with low power consumption and better phase noise performance. The design has more emphasis on minimizing the phase noise and minimization of process and temperature variations while maintaining the low power consumption. The VCO is designed and laid out in 0.18 μm CMOS process and verified through simulations. The measured phase noise of the oscillator is -97.2 dBc/HZ at a 3.5 MHZ offset from 2.5 GHZ center frequency for a power consumption of 8.52 mW. The measured gain of the VCO is 200 MHZ/V.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

Introduction

1.1 Motivation

Voltage controlled oscillator(VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. The two mostly used VCOs are 1.) LC oscillators 2.) Ring oscillators. Although LC oscillators generally have better phase noise performance there is a motivation to design ring oscillators with comparable phase noise compared to LC oscillators. The advantages of ring oscillator include significantly less die area and generally wide tuning range. The existing PLL design has the LC based VCO which is suffering from large chip area because of on-chip spiral inductor, again accurate modeling of on-chip spiral inductor is difficult. The present work replaces the LC oscillator with Ring oscillator to achieve the less chip area with high level of integration.

1.2 Organization of the Thesis

Chapter 2 This chapter discusses the architecture of the VCO and objectives we need to achieve in this project.

Chapter 3 Discuses the basic concepts of ring oscillator,delay-cell and gain requirements of the delay cell.

Chapter 4 Discuses the design issues of delay-cell

Chapter 5 Discusses the design of Gilbert multiplier and buffer

Chapter 6 Presents the circuit layout and simulation results.

CHAPTER 2

VCO Architecture and Specifications

2.1 Architecture of the proposed VCO:

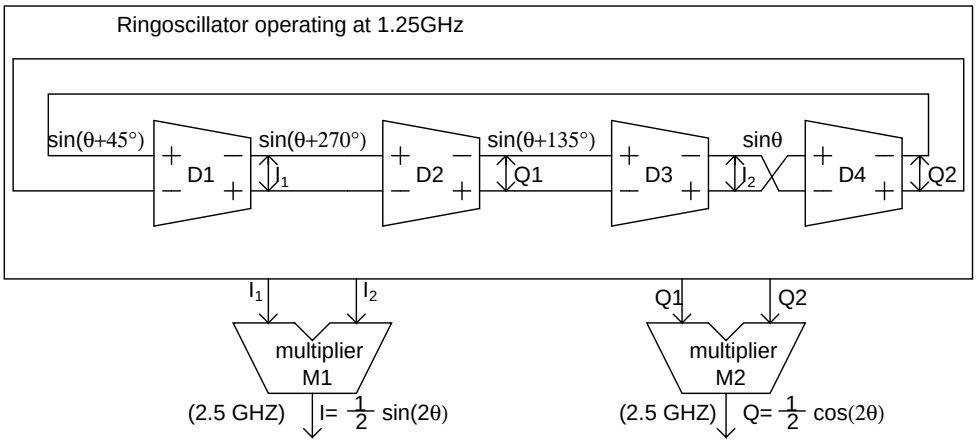


Figure 2.1: Architecture of VCO

Fig. 2.1 shows the architecture of the VCO which is implemented in this work. This contains a Ring oscillator operating at a frequency of 1.25GHZ(explained in chapter3). The Ring oscillator is followed by two multipliers to multiply quadrature signals at 1.25 GHZ and produce a signal at 2.5 GHZ. Again the signals produced by the multipliers are in quadrature(90° apart in phase).

2.2 Performance specifications of frequency synthesizer:

The two important specifications of the frequency synthesizer which are directly effected by the design of VCO are 1.)*Phase noise* 2.)*Spur*[2]. VCO phase noise and gain of the VCO are the deciding factors of the frequency synthesizer's phase noise

and spur respectively, these are explained in the following sections clearly. For the given standard(Zigbee) these two specifications are very stringent. Therefore the total design of RING VCO is centered around reduction of phase noise and minimization of gain.

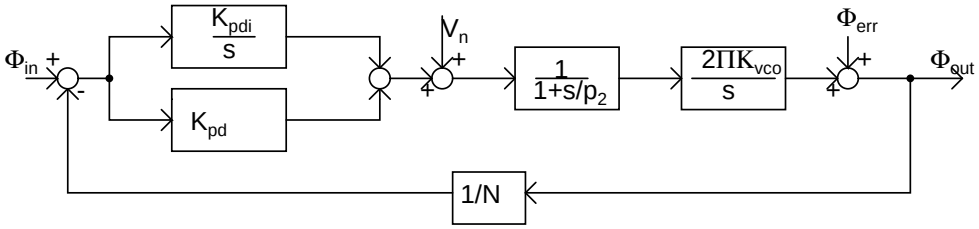


Figure 2.2: Block diagram of type2 PLL

Fig. 2.2 shows the block diagram of the type2 PLL[6]that can be used in analyzing the effect of VCO phase noise(Φ_{err}) and VCO gain(K_{vco}) on the PLL phase noise and spur respectively. The loop gain L(s) of the system is given as follows.

$$L(S) = \frac{1}{N}(K_{pd} + \frac{K_{pdi}}{s})(\frac{1}{1 + \frac{s}{p_2}})\frac{2\pi K_{vco}}{s} \tag{2.1}$$

The important parameters of the loop gain are $Z_1 = \frac{K_{pdi}}{K_{pd}}$, $f_u = \frac{K_{pdi}K_{vco}}{N}$ and p_2. To make sure the loop is stable the condition given in Equation. 2.2 must be valid.

$$Z_1 < f_u < p_2 \tag{2.2}$$

To make sure the magnitude of spurious components(spurs) is less, the condition given in equation. 2.3 must be valid.

$$p_2 < f_{ref} \tag{2.3}$$

The bode plot of the loop gain for a typical PLL design satisfying the above two constraints is shown in Fig. 2.3.

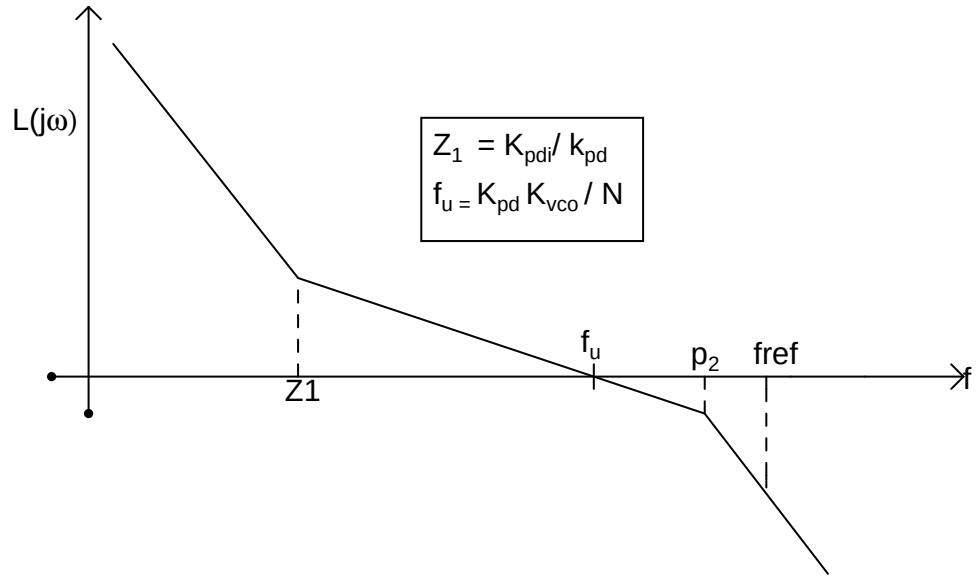


Figure 2.3: Bode plot of the Loop gain L(s)

2.2.1 Phase noise of VCO:

$$\begin{aligned} \frac{\Phi_{out}(s)}{\Phi_{err}(s)} &= \frac{L(s)}{1+L(s)} \\ &= \frac{1}{L(s)} \quad \text{for L(s)} > 1 \\ &= 1 \qquad \text{for L(s)} < 1 \end{aligned} \tag{2.4}$$

Equation 2.4 is a high pass transfer function with a cut of frequency of $fu = \frac{K_{pd}K_{vco}}{N}$ [6]. The given phase noise specification for the synthesizer is -92dBc/Hz at 3.5Mhz offset[2], this frequency falls well within the pass band of this transfer function, this means the total noise of VCO is coming out as PLL phase noise. Therefore it is needed to make a VCO with phase noise few dB lower than -92dBc/HZ specification. This discussion is just to remind the phase noise requirement of the VCO. So it is clear that making the VCO phase noise as less as possible within the power constraints is our first objective.

2.2.2 Gain of VCO:

$$\frac{\Phi_{out}(s)}{V_n(s)} = \frac{\Phi_{out}(s)}{\Phi_{err}(s)}(\frac{1}{1+\frac{s}{p_2}})\frac{2\pi K_{vco}}{s} \tag{2.5}$$

Equation. 2.5 is a transfer function between the output phase and control voltage($V_n(t)$) of the PLL. This exhibits a band pass nature[6] with a lower cut of frequency Z_1 and a higher cut of frequency f_u. The frequency f_{ref} falls under higher stop band of the transfer function, therefore it is necessary to increase the attenuation in higher stop band, this can be achieved in different ways as follows .

1.)by decreasing the value of p2: This choice reduces the phase margin of the loop and also causes more chip area[6] because of higher component values, so this is not a good way to attenuate the spurs.

2.)by decreasing the value of f_u: This trade offs with the settling time of the loop, but this is a viable option as long as the settling time is within the given requirement. Again this can be achieved in two ways

1.)by decreasing the value of K_{vco} 2.)by decreasing the value of $K_{pd} = IcpR$, where Icp is charge pump current and R is loop filter parameter[6], making Icp less is not a good choice because of difficulty in realizing smaller current sources with high degree of matching. Second option is to reduce the value of R which again causes the increase in value of p2 making the whole objective(spur attenuation) unachievable. The only best way to decrease the value of f_u is to decrease the value of K_{vco}.

From this discussion it is clear that making the gain of the VCO as less as possible is our second objective.

CHAPTER 3

Ring Oscillator

3.1 Barkhausen criteria

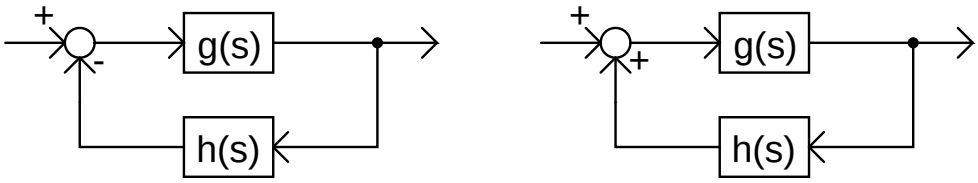


Figure 3.1: Oscillator feedback model (a)Negative feedback model (b)Positive feedback model

As a basic Requirement for producing self sustained near sinusoidal oscillation an oscillator must have a pair of complex-conjugate poles in the right half of the s-plane. As shown in Fig. 3.1 an oscillator can be modeled as a feedback system with a loop gain T(s)=g(s)h(s). Where 1-T(s) is the characteristic equation of the system from which poles are found. According to barkausen criteria for any feed back system the fulfillment of the following conditions is often used as an indication of instability.

Negative feedback model:

$$ph\{T(j\omega)\} = 180 \tag{3.1}$$

$$Mag\{T(j\omega)\} > 1 \tag{3.2}$$

Positive feedback model:

$$ph\{T(j\omega)\} = 0 \tag{3.3}$$

$$Mag\{T(j\omega)\} > 1 \tag{3.4}$$

The above conditions are necessary but not sufficient. The system may fail to oscillate even after satisfying the above conditions. As a rule of thumb the barkausen criteria is valid if it holds at only one frequency [3].

3.2 Differential Ring Oscillator

A ring oscillator consists of a number of gain stages in a loop. While single ended rings are well understood, easy to size and convenient to port over processes they are limited to an odd number of delay stages making them incapable of providing quadrature outputs. As a result differential ring oscillators are the only choice for the systems which require quadrature signals, on the other hand the differential implementations can utilize even number of stages by simply configuring one stage such that it does not invert. With four stage differential ring oscillator we can produce quadrature signals very easily.

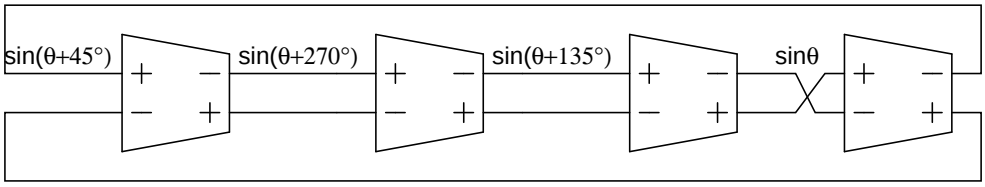


Figure 3.2: Four stage Ring Oscillator

3.3 Gain requirement of each stage:

Fig. 3.2 shows a four stage ring oscillator with one of the interconnections held non invert. The ring(loop) exhibits a Dc phase shift of 180°. From equation 3.3 we can say that an additional phase shift(frequency dependent) of 180° can make the system unstable provided the loop gain at that frequency is greater than 1, this puts a lower limit on the gain of each stage. This value can be derived by approximating each delay stage with a first order transfer function (H(s)).

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_o}}$$

Then the Loop gain of the system is given as follows.

$$T(s) = \frac{-A_o^4}{(1+\frac{s}{\omega_o})^4}$$

To get an frequency dependent phase shift of 180° each stage should introduce a phase shift of 45°. Let ω_{osc} is the frequency of oscillation. Then

$$Tan^{-1}(\frac{\omega_{osc}}{\omega_o}) = 1$$

$$\omega_{osc} = \omega_o$$

The minimum voltage gain can be obtained as follows. From equation 3.3

$$T(j\omega) > 1$$

$$\frac{A_o^4}{(\sqrt{1+(\frac{(\omega_{osc}}{\omega_o})^2)^4} > 1$$

$$\frac{A_o}{\sqrt{1+(\frac{\omega_{osc}}{\omega_o})^2}} > 1$$

$$A_o > \sqrt{(2)}$$

3.4 choice of delay-cell:

Basically differential delay-cells can be classified into two types 1.)Full swing delay cell 2.)Partial swing delay cell. The examples for these two delay cells are shown in Fig. 3.3(a) and Fig. 3.3(b) respectively. Full swing oscillators are designed as basic inverters with some positive feedback to make the rail to rail transitions sharp, in this case the output amplitude is rail to rail and it looks like a square wave. The two attributes, fast transitions and rail-to-rail swing, cause the full-swing ring oscillator to reject intrinsic noise better than a partial-swing ring oscillator. On the other hand, the partial-swing oscillator has smaller voltage swing and slow transitions leading to poor intrinsic noise rejection, but the power supply rejection capability of partial swing oscillators is more compared to full swing oscillators.

Because of higher bandwidth and higher power supply noise rejection partial-swing delay cells are more practical to implement.

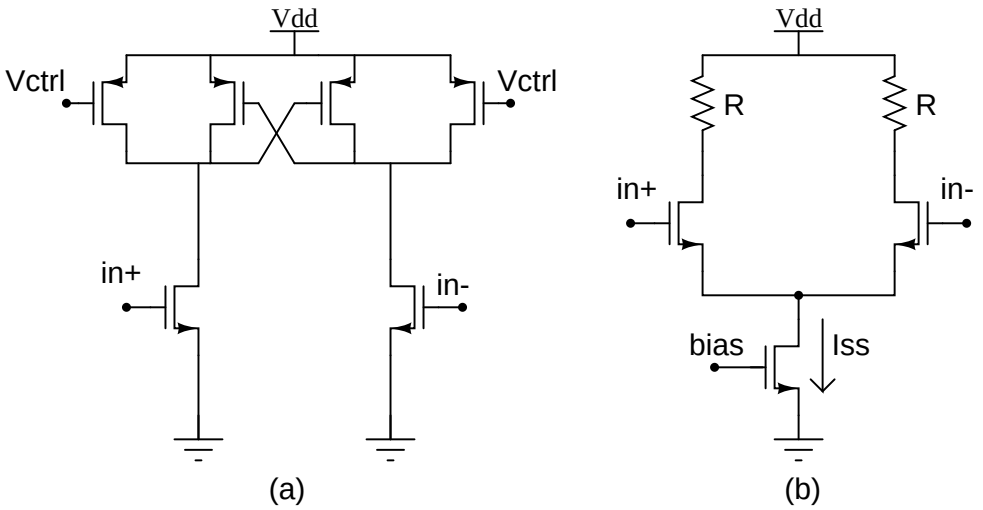


Figure 3.3: Differential delay cells (a)Full swing delaycell (b)Partial swing delay-cell

Because of lack of high quality resistors in CMOS technologies the delay cell shown in Fig. 3.3(b)is not suitable for practical implementation. Most of the practical delay-cells use PMOS transistors operating in deep triode region as the loads, examples for these type of delay-cells are shown in Fig. 3.4 . The delay-cell shown in Fig. 3.4(b) is not suitable for high frequency applications because larger load capacitance as gate of the PMOS is connected to its drain.

3.5 Tuning:

The frequency of oscillation of a N-stage Ring Oscillator is given by

$$f_{osc} = \frac{1}{(2NT_d)^{-}1}$$

Where T_d denotes the large signal delay of each stage. Therefore we can vary the frequency by varying T_d. This can be done in two ways. 1)By varying the load Resistance 2.) by varying the tail current.

We can vary the load resistance by varying the gate to source voltage of PMOS

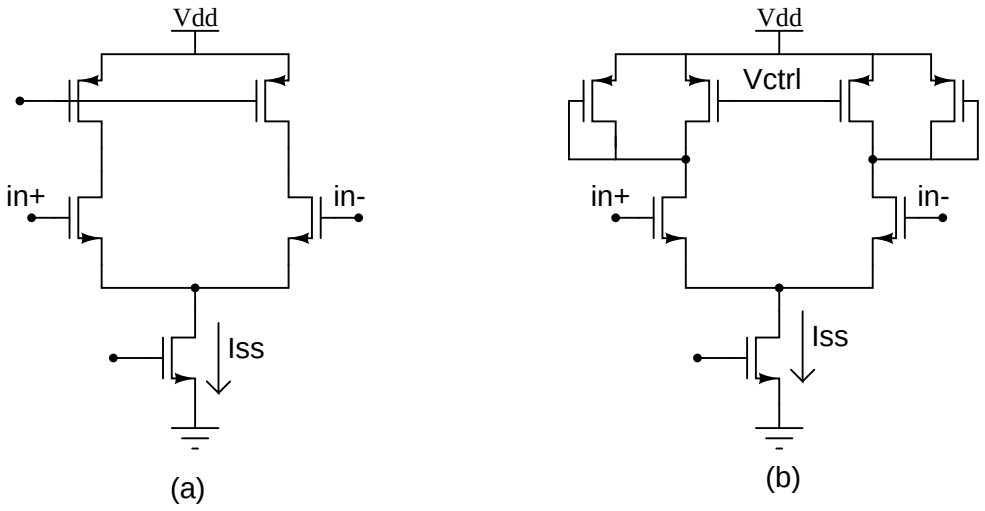


Figure 3.4: delay cells with pmosload (a)simple load (b)symmetricload

loads (by varying vctrl or Vdd)[Fig. 3.5]. But this method results in high gain of the VCO. As discussed in chapter. 2 it is always desirable to reduce the gain of the VCO as less as possible. So the better option to vary the frequency is to vary the tail current of the delay cell. Both the tuning methods mentioned here are suffering from serious drawback of amplitude variation over the given tuning range. This can be avoided to the maximum extent with the topology shown in Fig. 3.5. With complete switching each stage provides a differential output swing

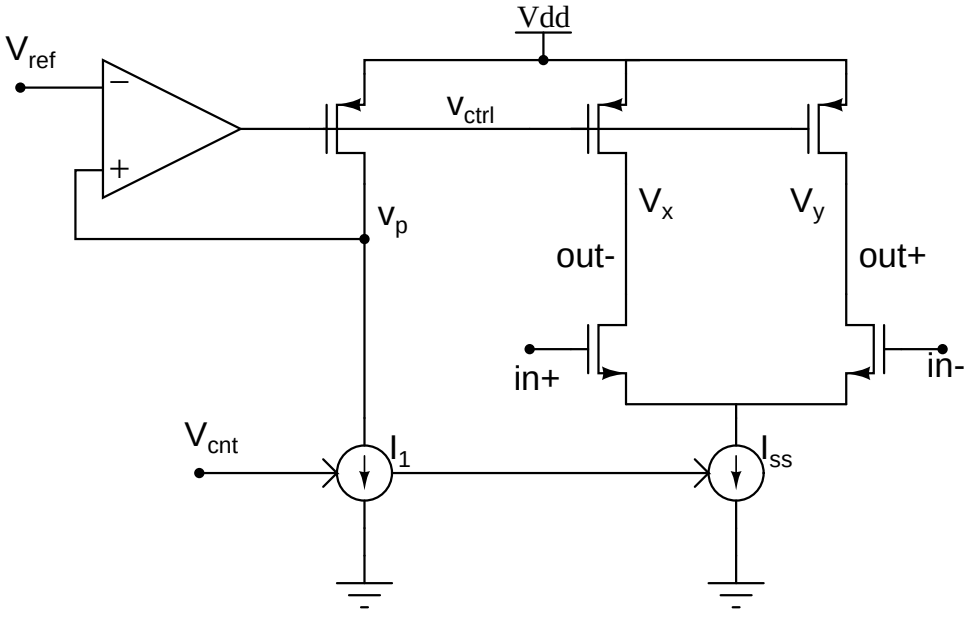


Figure 3.5: DelayCell with Replica Bias

of $2I_{ss}R_{On}$, where R_{On} is the on resistance of PMOS load. Therefore to maintain a constant output swing the circuit needs a constant $I_{ss}R_{On}$ product through out the tuning range. This can be achieved by the topology shown in Fig. 3.5 explained as follows. The negative feed back loop formed by the opamp makes the voltage at node v_p always equal to V_{ref} therefore any increase in tail current causes the gate voltage of PMOS device to decrease because of fixed drain to source voltage, this means decrease in on resistance of the PMOS device [1].

CHAPTER 4

Delay cell design

The Basic delay-cell consists of a source coupled logic inverter with PMOS loads operating in the triode region, source coupled logic is advantageous because of its higher frequency of oscillation, immunity to substrate noise and higher power supply noise rejection. As discussed in chapter. 2 meeting the given phase noise specification is very critical issue in designing of oscillator delay-cell. Before getting into design of delay-cell it is important to understand the phase noise limits for delay-cell based VCOs and how do they depend on delay-cell design parameters.

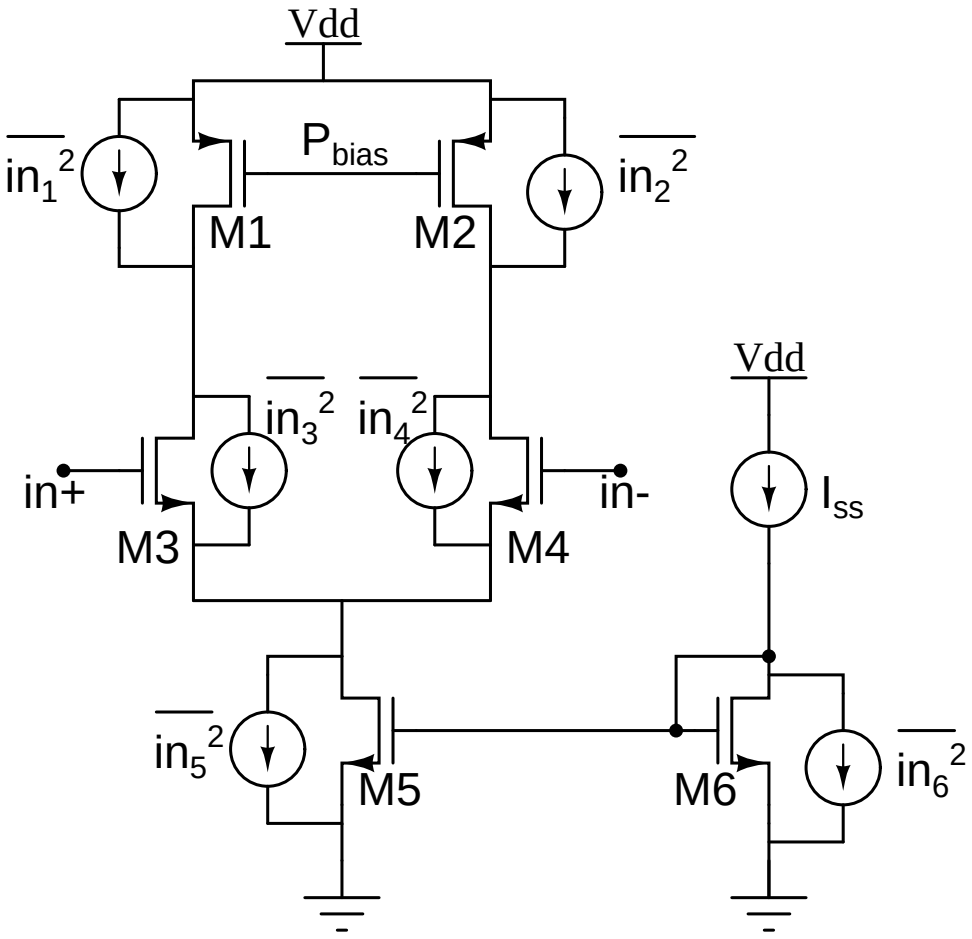


Figure 4.1: Delay-cell With Thermal noise sources.

4.1 Phase noise analysis:

The noise sources shown in Fig. 4.1 introduce timing jitter by corrupting the rising and falling edges of transitions that propagate through chain of delay-cells. There are mainly two types of approaches to deal with the phase noise of ring oscillator namely time domain approach and frequency domain approach. In this project I made use of the both the approaches to arrive at the given delay-cell design. In time domain approach first a relationship is derived between the design parameters of the delay-cell and timing jitter(A time domain specification of the oscillator), then a link is established between timing jitter and phase noise[4]. Whereas the frequency domain approach uses the linear feed back model of the oscillator to arrive at the given phase noise relation [5].

In the following discussion of this chapter both the approaches are explained briefly, so that one can appreciate the sizes of the transistor and swing chosen for the given delay-cell design, on the way a small comparison is made between the two approaches so that one can get more insight into the phase noise analysis of VCO.

4.1.1 Frequency domain approach:

In this approach the total phase noise is classified into three categories.

1.)Additive noise.

2.)High frequency multiplicative noise.

3.)Low frequency multiplicative noise.

Additive noise:

Additive noise consists of components that are directly added to the output and can be calculated with the linearized model. It is shown in [5] that the additive noise goes down as square of the offset. And the relation is given as follows.

$$A_n(\omega) \propto K \left(\frac{\omega_0}{\omega}\right)^2 \widetilde{I}_n^2 \tag{4.1}$$

- K is a constant decided by the gain of the delay-cell and number of stages in the Ring.
- $\widetilde{I_n^2} = \frac{8KT}{3}(gm_1 + gm_3)$
- ω_0 is the oscillation frequency.
- ω is the offset frequency.

Additive noise can be predicted by the linearized model with high accuracy if the stages in the ring operate linearly for most of the time. Since additive noise is shaped by equation4.1 its effect is significant for components close to the oscillation frequency, i.e The thermal noise of the devices(M1, M2, M3, M4)4.1 play important role here.

High Frequency multiplicative noise:

The nonlinearity in delay-cells especially when they turnoff and turn on cause noise components to be multiplied by the carrier and by each other.
Let say the input output characteristics of the delay-cell is given by

$$V_{out} = \alpha_1 v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 \tag{4.2}$$

Let say the input consisting of carrier and noise is given by

$$V_{in}(t) = A_0 cos\omega_0 t + A_n cos\omega_n t. \tag{4.3}$$

Then the output exhibits the following components.

$$V_{out1}(t) \propto \alpha_2 A_0 A_n Cos(\omega_0 \pm \omega_n)t \tag{4.4}$$

$$V_{out2}(t) \propto \alpha_3 A_0 A_n^2 Cos(\omega_0 - 2\omega_n)t \tag{4.5}$$

$$V_{out3}(t) \propto \alpha_3 A_0^2 A_n Cos(2\omega_0 - \omega_n)t \tag{4.6}$$

$$\tag{4.7}$$

Note that $V_{out1}(t)$ appears in the vicinity of the carrier if ω_n is small, i.e., if it is a low-frequency component, but in a fully differential configuration, $V_{outl}(t) = 0$ because $\alpha_2 = 0$. Also, $V_{out2}(t)$ is negligible because $A_n \ll A_0$ leaving $V_{out3}(t)$ as the only significant product. It is shown in [5] that the magnitude of this cross product is significant for the noise components close to ω_0. Therefore in this case also the thermal noise of the devices(M1, M2, M3, M4) dominates the situation.

Low Frequency multiplicative noise:

Since the frequency of oscillation is a function of the tail current in each delay-cell, noise components in this current modulate the frequency. This effect is quiet different from above two approaches where the noise components cause uncertainty in rising and falling edges. But in this case noise current directly modulates the frequency thereby contributing to phase noise, this will be cleared with the following analysis.

Let say K_{vco} is the gain of the VCO, and is defined as

$$K_{vco} = \frac{d\omega_{out}}{dI_{ss}} \tag{4.8}$$

Let say $I_n cos\omega_n t$ is noise component present in the tail current. Then the output of the Oscillator can be written as

$$\begin{aligned} V_{out}(t) &= A_0 cos(\omega_0 t + K_{vco} \int I_n cos\omega_n t dt) && (4.9) \\ &= A_0 cos(\omega_o t + \frac{K_{vco}}{\omega_n} I_n sin\omega_n t) && (4.10) \end{aligned}$$

for $\frac{K_{vc0} I_n}{\omega_n} \ll 1$ the output can be approximated as follows(narrow band F.M).

$$V_{out}(t) \approx A_0 cos\omega_0 t + \frac{A_0 I_n K_{vco}}{2\omega_n}[cos(\omega_0 + \omega_n)t - cos(\omega_0 - \omega_n)t] \tag{4.11}$$

from the above equation we can express the noise power relative to carrier as follows.

$$\widetilde{v_n^2}\text{with respect to carrier} = \frac{1}{4}\left(\frac{k_{vco}}{\omega_n}\right)^2 I_n^2 \tag{4.12}$$

From equation 4.12 we can say that the magnitude of the output noise component is more for lower values of ω_n i.e low frequency noise present in the tail current source. Therefore the flicker noise of the tail current is more of interest than its thermal noise. In the discussion of time domain approach that follows we come to know the thermal noise of tail current also plays a significant role in contributing phase noise.

4.1.2 Time domain approach:

A detailed derivation of phase noise in time domain approach is given in[4]. In this section i am going to present the final phase noise result given in[4] and explain significance of each term present in that result so that one can understand trade offs involved in delay-cell design which follows in further sections of this chapter. The Relation between phase noise of the oscillator and design parameters of the delay cell is given as follows.

$$S_\phi(fm) = \left(\frac{f_0}{f_m}\right)^2 \left[\frac{F_1 KT}{I_{ss}(V_{Gs} - V_T)}\right] \tag{4.13}$$

- f_0 is the frequency of oscillator.
- f_m is the offset frequency of interest in phase noise calculation.
- I_{ss} is the tail current of the delay cell.
- $V_{Gs}-V_t$ is the gate overdrive of the differential pair transistors(M3, M4)(Fig. 4.1)

$$F_1 = \frac{a_v \zeta^2}{2}$$

- a_v is the gain of the delay-cell.

$$\zeta^2 = 2\gamma_1 + 2\gamma_3 a_v \lambda_{a2}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta)\lambda_{b2}(2t_d) \tag{4.14}$$

- γ_1:This is due to triode region PMOS transistors(M1, M2). The thermal noise power spectral density of these transistors is given by $i_n^2(f) = 4KT\gamma g_{dso}$. Where g_{dso} is the zero bias drain to source conductance. γ varies from 1 for $V_{ds} = 0$ to $\frac{2}{3}$ at the onset of saturation. γ_1 is the average value of γ over the transient its value is close to 1.

- γ_3:This is due to NMOS differential pair transistors(M3, M4). These transistors are operating in saturation or cutoff, in saturation the thermal noise power spectral density of these transistors is given by $i_n^2(f) = 4KT\gamma_3 g_m$, where g_m is the transconductance of these devices. γ_3 value varies from $\frac{2}{3}$ for long channel devices to as high as 2 or 3 for devices exhibiting short channel effects.

- γ_5:This is due to tail current device which is operating in saturation for all the time and is similar to γ_3, generally length of this transistor is high, and its value is almost equal to $\frac{2}{3}$

- $\alpha = \frac{sizeofM5}{sizeofM3}$
- $\beta = \frac{sizeofM5}{sizeofM6}$
- $\lambda_{a2}(t)$, $\lambda_{b2}(t)$ are the noise evaluation factors.

- $\lambda_{b2}(t) = [1 + 2at + 2a^2t^2]e^{-2at}$
- $\lambda_{a2}(t)$ =1-$\lambda_{b2}(t)$
- a = $\frac{1}{R_L C_L}$
- R_L is the load resistance.
- C_L is the load capacitance.

Significance of Noise Evaluation factors$\lambda_{a2}(t)$, $\lambda_{b2}(t)$:

The main advantage of time domain analysis over frequency domain analysis is its consideration of time varying nature of noise sources and interstage amplification in deriving the given phase noise relation (equation. 4.13). And these two effects are taken into consideration by introducing the noise evaluation factors.

Time varying nature of noise sources: The assumption of constant noise spectral density for input differential pair transistors(M3, M4)(Fig. 4.1) is not fully valid. Since each stage switches from fully off to fully on, during which the

transconductance and hence the noise contribution changes dramatically. Further as discussed in previous section only low frequency noise of tail current is significant contributor of phase noise, this is true when the differential pair is in balanced mode. But high frequency noise also contributes to the output noise during other parts of the switching transient.

Interstage amplification: The second effect which is not taken into consideration in frequency domain analysis is this. The switching times of adjacent stages in a CMOS inverter chain overlap and there are times when more than one stage is in active region of amplification, in this case it is not sufficient to consider the noise contribution of the single inverter alone, because noise from one inverter may be amplified and filtered by next stage.

4.2 Implementation details

In this section i am going to discuss about the key design parameters one should be familiar with before designing of the delay-cell, these parameters includes output swing, gain, and biasing conditions for the delay-cell.

4.2.1 Swing considerations

Choosing the proper value for output swing, V_{SW}, depends on several competing factors like speed of operation, gain of the inverter stage, biasing conditions of PMOS devices(M1, M2)and biasing conditions of NMOS devices and noise margins etc, will be explained as follows.

Speed: The large signal delay of the delay-cell is given by $\frac{C_L V SW}{I_{ss}}$, where C_L is the load capacitance, V_{SW} is the output swing and I_{ss} is the tail current. Higher speed requires smaller delays that means smaller swings favors higher speeds and larger swings favors lower speeds.

Gain: The gain of the delay-cell is given by

$$a_v = g_m R_L \tag{4.15}$$

where g_m is the transconductance of the input pair(M3, M4). And R_L is the load resistance offered by the PMOS load.
The expression for g_m is given by

$$g_m = \frac{2(\frac{I_{ss}}{2})}{V_{GS} - V_T}$$

Where $V_{GS} - V_T$ is the gate overdrive of the differential pair transistors(M3, M4). The voltage drop across the PMOS devices is V_{SW} when the complete current I_{ss} flows through it. Therefore the load resistance R_L is given by

$$R_L = \frac{V_{sw}}{I_{ss}}$$

By substituting the expressions for R_L and g_m in equation. 4.15 we can express the gain as follows.

$$gain = a_v = \frac{V_{sw}}{V_{GS} - V_T} \tag{4.16}$$

As discussed in the chpter. 3 gain of the delay-cell should be greater than or equal to $\sqrt{2}$, this means lower swing requires lower values of $V_{GS} - V_T$. But lower values of $V_{GS} - V_T$ will result in higher phase noise, this is evident from equation 4.13.
PMOS biasing(M1, M2): For better linearity it is needed to bias the PMOS transistors in deep triode region. For this transistors to be in triode region, the following condition must be satisfied through out all the process corners and temperatures.

$$V_{SW} < V_{GS} - V_{TP} \tag{4.17}$$

If we go for higher values of V_{SW} we need to bias these PMOS devices at higher values of V_{GS}. But maximum value of V_{GS} is limited to V_{DD}. Therefore an upper

limit is set on the V_{SW} by the triode region condition of PMOS devices(M1, M2). **NMOS biasing(M3, M4):**Another important issue in choosing the value for swing is making sure that these NMOS devices always operate in saturation or cutoff regions. Let say VCM is the output common mode level. An output swing V_{SW} means we will get $\pm\frac{V_{SW}}{2}$ variations around this common mode value. If gate of this NMOS device is at $VCM + \frac{V_{SW}}{2}$ its drain voltage will come down to$VCM - \frac{V_{SW}}{2}$, under this condition to maintain the device in saturation the following condition must be satisfied.

$$V_{CM} + \frac{V_{SW}}{2} - V_T < V_{CM} - \frac{V_{SW}}{2} \tag{4.18}$$

$$V_{SW} < V_T \tag{4.19}$$

$$\tag{4.20}$$

For the Design implemented here V_{SW}=0.5V.

4.2.2 gain(a_v) considerations:

The immediate step after selecting a value for swing V_{SW} is the selection of proper gain for the delay cell. From the discussion in chapter. 3 it was clear that gain should be grater than $\sqrt{2}$. The first question is that a gain exactly equivalent to $\sqrt{2}$ is sufficient or do we need higher gain. The second question is if we need larger gain how large this should be when compared to the minimum gain($\sqrt{2}$).

$$a_V = \frac{V_{SW}}{V_{GS} - V_T}$$

- The answer to the first question is exactly not, because of process and temperature variations. The gain of the delay cell varies by significant amount with process and temperature variations. One should choose a gain such that it is always above the minimum gain for all the process corners and temperatures.
- The answer to the second question is clear from the phase noise relation given in equation. 4.13. If we go for higher gains we need smaller values of $V_{GS} - V_T$, which in turn results in larger phase noise.

- Another important issue I observed during simulations is smaller gains results in lower output amplitudes at slow process corners and higher temperatures.

Therefore practical delay-cell gains are in the range of 1.5 to 3.

In my case I have chosen a value of 1.8 for gain, the worst case gain for this design is 1.42(ss, 80°).

4.2.3 design procedure:

I followed the same design procedure given in [4]. Just for convenience I listed the design steps here.

- Choose output swing, V_{SW}
- Set the target current, I_{ss}
- Set target $V_{GS} - V_T$ bias point for PMOS loads including the margin for process variations.
- Determine the PMOS load device sizes $(\frac{W}{L})_1$.
- Determine the NMOS Differential pair device sizes $(\frac{W}{L})_3$ to meet the target gain while maximizing $(V_{GS} - V_T)$.
- Set a load capacitance of C_L at the output.
- Scale the sizes of transistors(M1, M2, M3, M4) to achieve the desired frequency for the given load C_L. Maximum achievable frequency is set by the technology.
- Determine the current source device sizes(M5, M6) and configuration.

Scaling:

Let say we followed the designed steps mentioned above and arrived at the proper design for delay cell. Typically there are two cases where one should need scaling 1.)unacceptable phase noise 2.)wrong estimation of the load capacitance(wiring, mixer). I will explain the scaling procedure in each case separately.

scaling for phase noise: From the equation 4.13, it is clear that to improve the phase noise one should increase the tail current I_{ss}. Scaling the tail current alone

will change all the bias conditions(PMOS load resistance, Gate overdrive of NMOS devices). Therefore to maintain the same bias conditions we have to scale the devices(M1, M2, M3, M4) by the same factor as that of tail current.

$$t_d = \frac{C_L V_{SW}}{I_{SS}} \tag{4.21}$$

$$C_L = C_{int} + C_W \tag{4.22}$$

C_{int} is the intrinsic capacitance of the delay-cell, C_W includes the wiring capacitance and load capacitance(mixer). If we scale the I_{ss} by K times, C_L also should be scaled by the same factor to maintain the delay t_d as constant. i.e scaling C_{int} alone by Scaling the devices[M1, M2, M3, M4] is not sufficient, we need scale the C_W also in the same way i.e we need to scale the mixer also in the same way or we need to put some load capacitance to compensate this effect.

scaling for load capacitance:

This is the case where our load capacitance C_W is scaled by some factor because of wiring capacitance. Let say C_W is scaled by K, Then to maintain the same delay we need scale I_{SS} and C_{int} also by the same factor. Scaling C_{int} is nothing but scaling the devices(M1, M2, M3, M4).

Design

Initially I assumed $\alpha = 0$, and $\beta = 0$, and $Swing = V_{SW} = 0.5$[refer section 4.2.1] and calculated the tail current for a phase noise of -100dBc/Hz using the formula of phase noise given in equation. 4.13. And I found a tail current of 250μA satisfies this phase noise requirement. After that i implemented the delay-cell with the design procedure mentioned above(section 4.2.3) and I found significant deviations in phase noise because of non zero values of α and β i got through circuit implementation, again using these values of α and β i repeated the same procedure. After few iterations i was arrived at the following design parameters(table. 4.1).

The β value given in this table assumes a reference tail current of $10\mu A$. And the circuit implementation of delay-cell is shown in Fig. 4.2. The theoretical value of phase noise for these parameters is -95dBc/HZ. The circuit shown in Fig. 4.2 includes replica bias and biasing circuitry also, these will be explained in future sections. The biasing circuit has some capacitances(C1, C2, C3), the significance of these capacitances is explained in section 4.4. The gain of the delay-cell varies over temperature and process, as shown in Fig.4.3 gain of the delay cell varies from 1.42 to 2.2. Fig.4.4 shows the output of the ring oscillator whose amplitude is just 348mV significantly different from 500mV(Swing) as for the design, this is due to incomplete settling of the signals.

Table 4.1: Design parameters of the delaycell

Design parameter	Value
Swing	0.5 V
I_{SS}	360 μA
gain	1.9
$(V_{GS} - V_T)_{PMOS}$	1.4 V
α	0.548
β	36

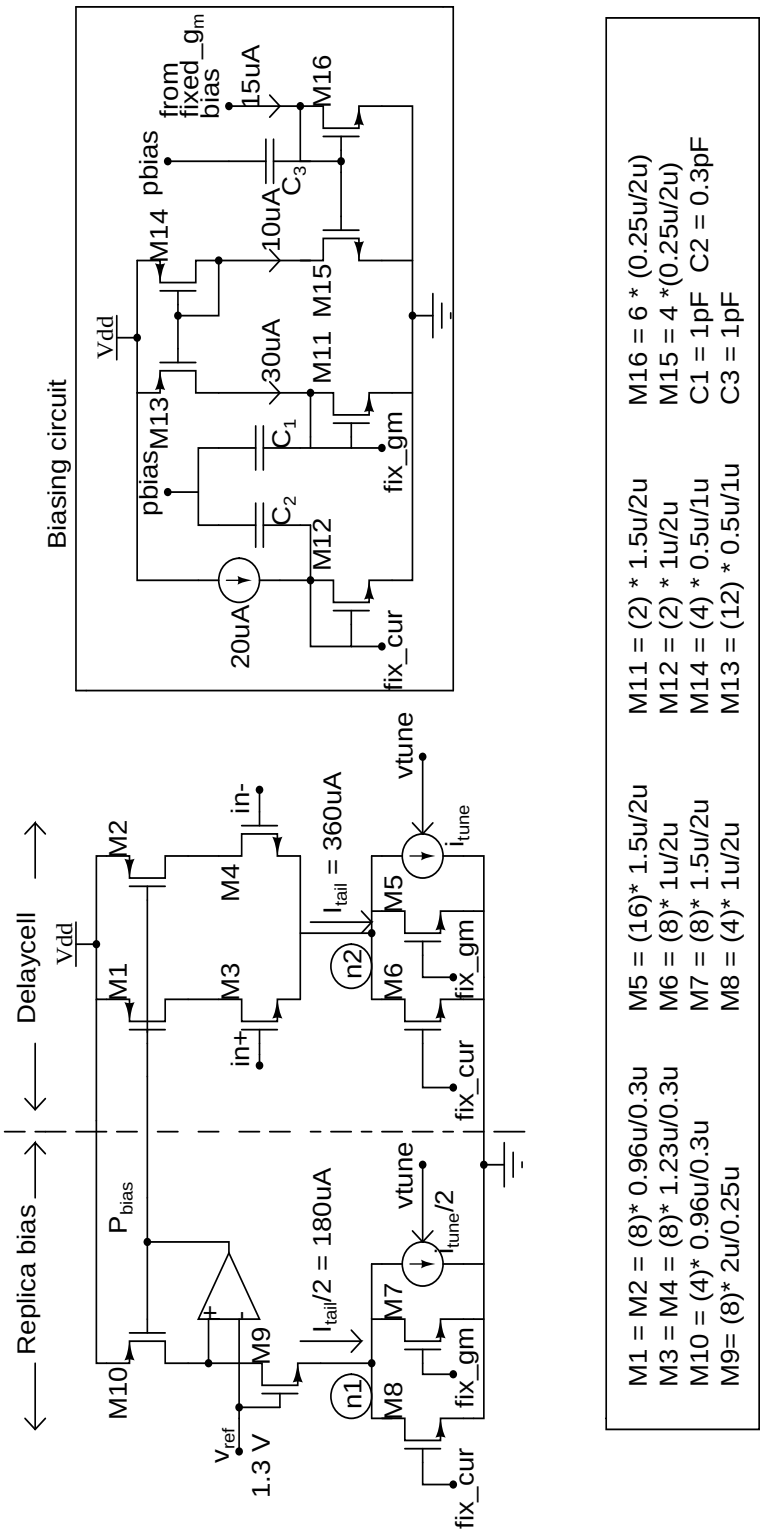


Figure 4.2: schematic of Delaycell with replica bias

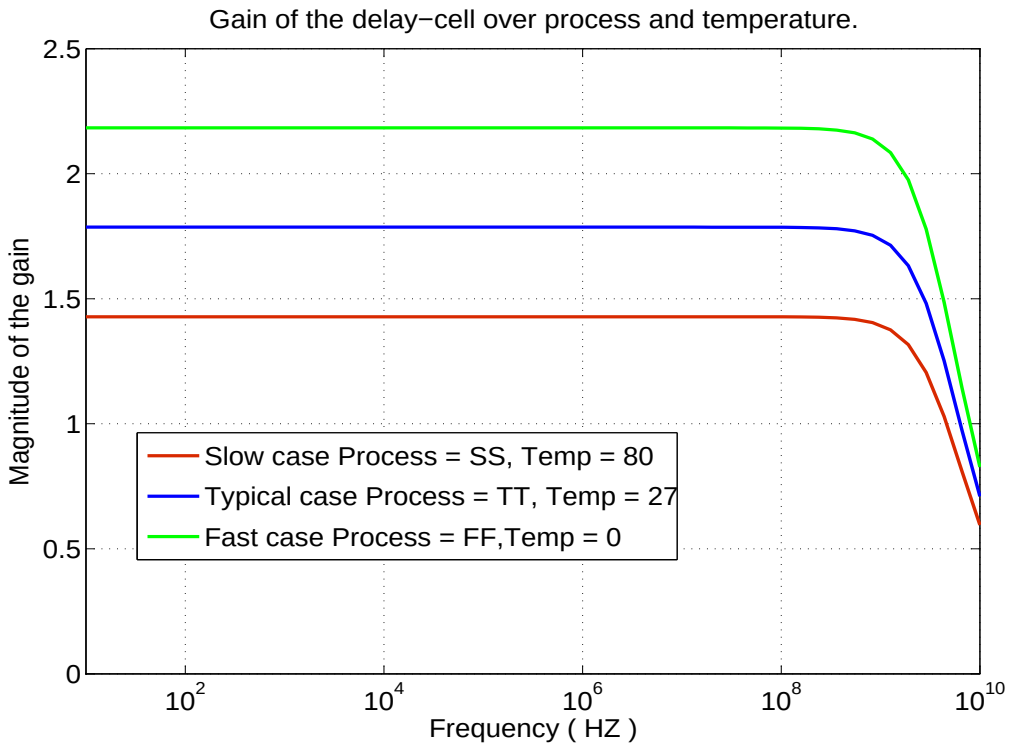


Figure 4.3: Gain of the delaycell over process and temperature

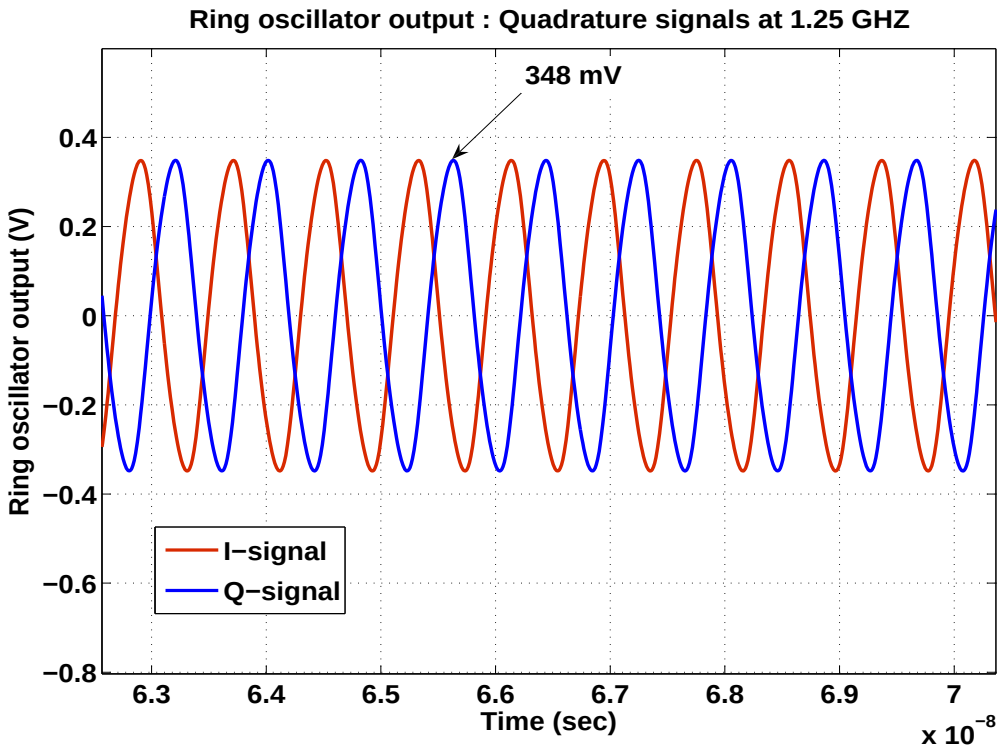


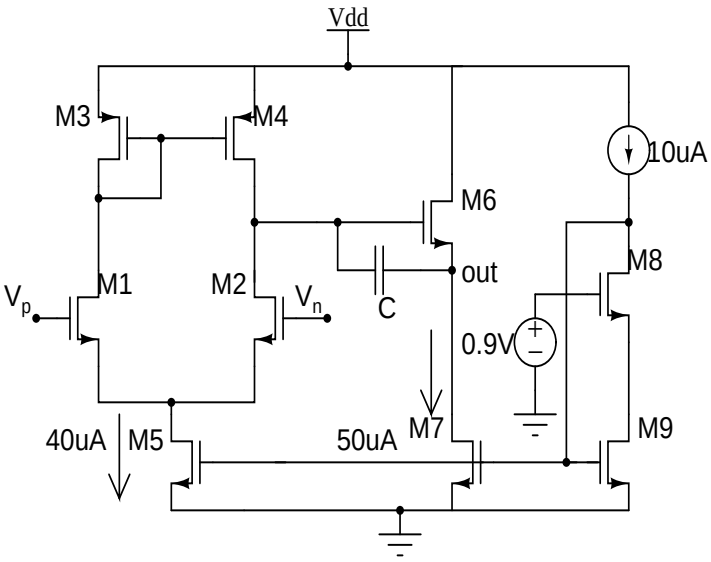
Figure 4.4: Ring Oscillator output:Quadrature signals

4.3 Replica bias:

As discussed in chapter. 3 replica bias is used to maintain constant voltage swing for varying currents. The implementation is shown in Fig: 4.2. When the total tail current in the delay cell switches to one side the voltage drop across the PMOS load is equal to V_{ref}(.5V). In our case the current in the replica bias is half of the tail current of the delay-cell, this particular value of current is chosen based on the noise coming from the Replica bias. We can observe from Fig: 4.2 that M10, M8, M7 are the scaled versions of M1, M6, M5 by a factor of $\frac{1}{2}$, but M9 is not exactly scaled version of M3, this is because of difference in input common mode voltages of M3, M9. So M9 is sized to get same voltages at nodes n1 and n2 Fig: 4.2.

opamp

The opamp in replica bias forms a negative feedback and modulates the gate voltage of PMOS to get a drain voltage of $V_{DD} - V_{ref}$. The only constraint on opamp is its band width should be larger than the PLL loop bandwidth, in the existing PLL the loop bandwidth is just 35.48KHZ[2]. So this is not a big constraint. The schematic of the opamp is shown in Fig: 4.5. Here the currents are chosen based on bandwidth and noise requirements. Sizing of the devices is done in such a way that gain of the opamp should be large enough even for the worst case output, in our case the worst case output is 50mV. The capacitor C is used to stabilize the loop formed by opamp and PMOS device (M10). Fig: 4.6 shows the magnitude plot of the gain of opamp for the given load, load includes C1, C2, C3(shown in Fig: 4.2), and 4 delay-cells. The 3dB bandwidth of the opamp is 6.8MHZ.



M1 = M2 = (4) * 1.2u/0.9u	M5 = (16) * 1.25u/0.3u
M3 = M4 = (8) * 1u/0.3u	M7 = (20) * 1.25u/0.3u
M6 = (2) * 2u/1.8u	M9 = (4) * 1.25u/0.3u
M8 = (2) * 1.5u/0.6u	C=500fF

M8

Figure 4.5: Schmatic of the OPAMP

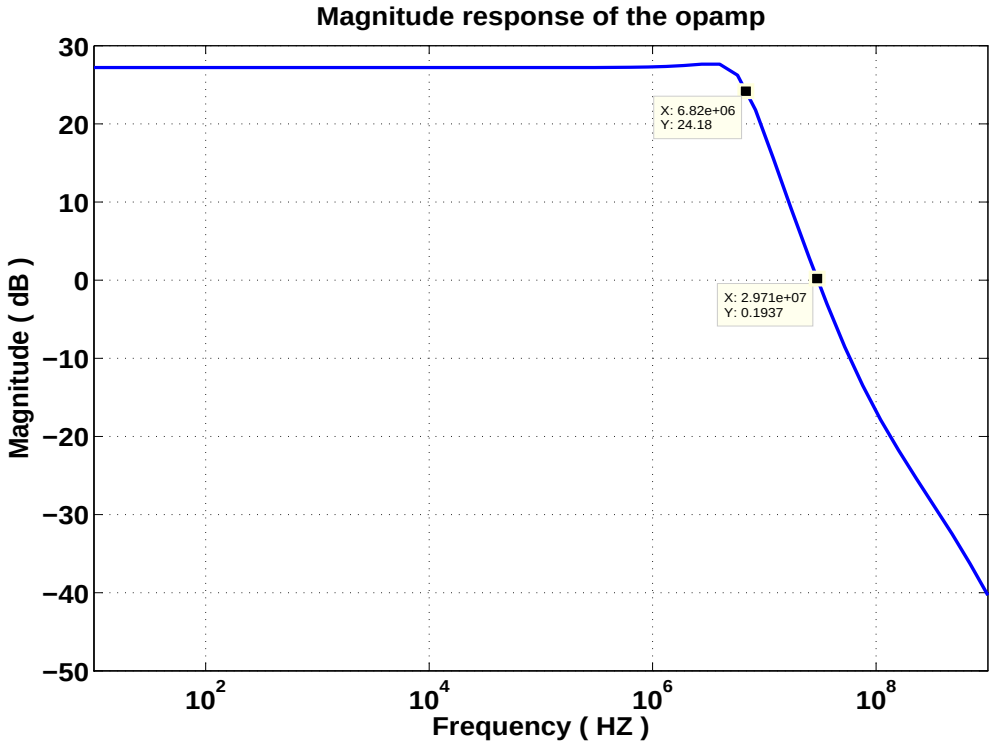


Figure 4.6: Gain of the Opamp

4.4 Noise reduction capacitance:

Contribution of tail current white noise to the phase noise:

As mentioned in section 4.2.1 there are times during which the white noise of the tail current source comes to the output and significantly contributes to the output phase noise. These are the times at which one branch of the delay-cell completely off and the other branch is completely off. The capacitances (C1, C2, C3) are used to reduce this contribution. At the time of writing this thesis we did not derive analytical reason behind this noise reduction phenomenon. But we have simulation results in well agreement with this phase noise reduction.

Circuit used for simulation:

The circuit shown in Figure. 4.7 resembles the condition mentioned above where one branch of the delay-cell is completely on and the other branch is completely off. Using this circuit transfer function is evaluated between output noise voltage(V_{nout}) and tail current noise source(i_{n6}) using Ac analysis in spice for different values of capacitance. And the simulation results are shown in Fig. 4.8. From this simulations we can easily observe that there is a significant attenuation in the output noise voltage in the frequency range of 100KHZ to 60 MHZ. And this attenuation getting increased as we increase the capacitance. From this observation it is evident that this capacitance reduces the effect of tail current noise significantly. Fig. 4.9 shows the phase noise plots of oscillator with delay cell shown in Fig. 4.2 with and without the capacitances C1, C2, C3, and this result shows a 5.6dB improvement in phase noise with the capacitances.

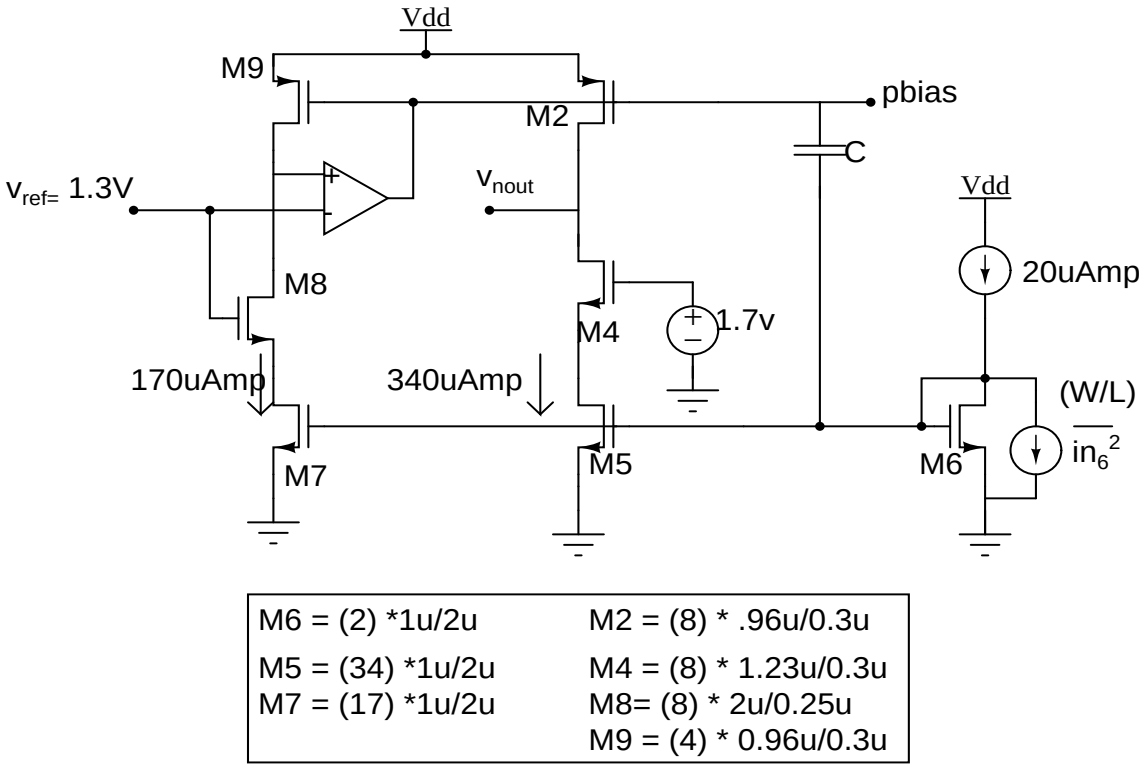


Figure 4.7: Circuit used to simulate the capacitance effect

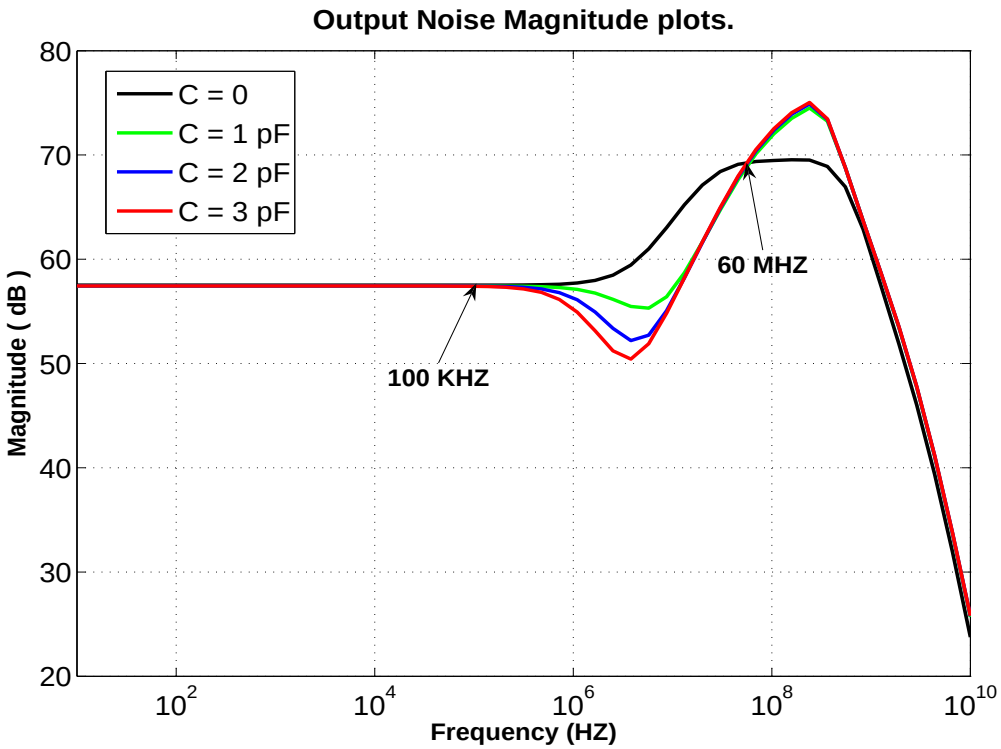


Figure 4.8: Output noise Magnitude plots

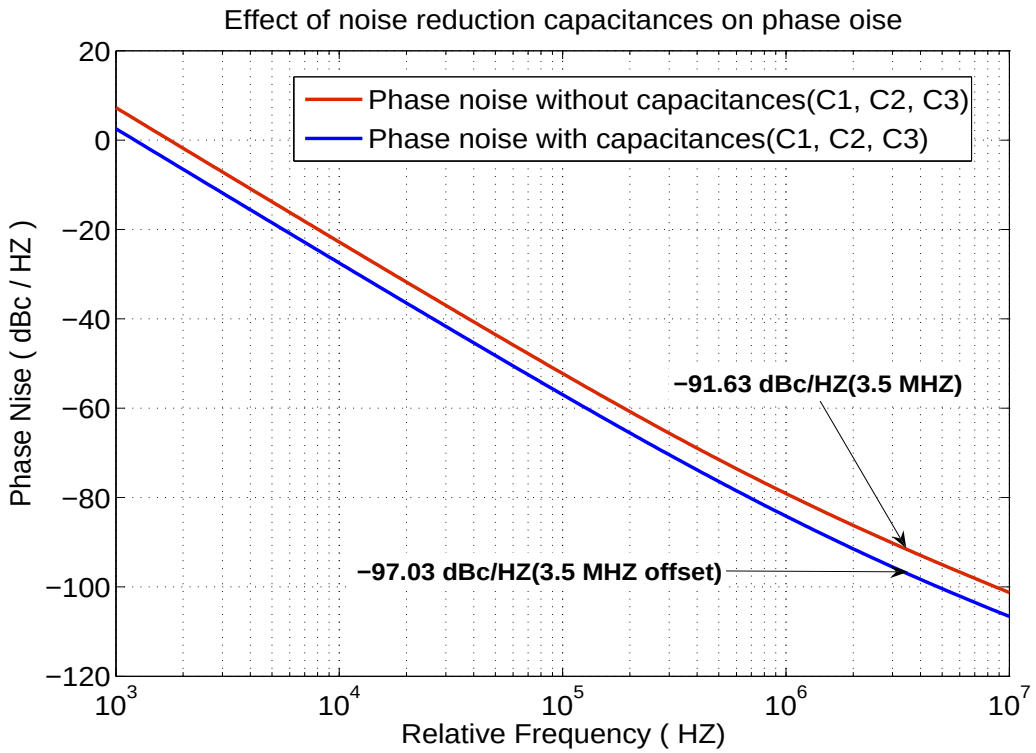


Figure 4.9: Phase noise plots with and without the capacitors

4.5 Process variations:

Oscillator frequency:

The delay per stage is given by

$$t_d = \frac{C_L V_{SW}}{I_{SS}}$$

The period of N-stage Ring oscillator is approximately 2N times the delay per stage. Therefore frequency of oscillation is given by

$$\begin{aligned} f_{osc} &= \frac{1}{2Nt_d} \\ &= \frac{I_{SS}}{2NC_L V_{SW}} \end{aligned} \tag{4.23}$$

$\frac{V_{SW}}{I_{SS}}$ is the effective resistance of the PMOS triode load and is given by

$$\begin{aligned} R_L &= \left(\frac{dV_{ds}}{dI_D}\right) \\ &= \frac{1}{\mu_p C_{ox} \frac{W}{L}_p [V_{GS} - V_{Tp} - V_{DS}]} \end{aligned} \tag{4.24}$$

If the load is well into the triode Region so that the output resistance is not too nonlinear then the average resistance of the load can be approximated by its resistance seen at $V_{DS} = \frac{V_{SW}}{2}$. Therefore R_L can be approximated as follows.

$$R_L = \frac{1}{\mu_p C_{ox} \frac{W}{L}_p [V_{GS} - V_T p - \frac{V_{SW}}{2}]} = \frac{V_{SW}}{I_{SS}}. \tag{4.25}$$

Substituting equation 4.25 into equation 4.23 we will get the following relation.

$$f_{osc} = \frac{\mu_p}{2N} \frac{C_{ox}}{C_L} \frac{W}{L}_p [V_{GS} - V_T p - \frac{V_{SW}}{2}]. \tag{4.26}$$

The load capacitance C_L seen at the output consists of gate to source capacitance of next stage and drain capacitances of triode load and differential pair transistors. The input capacitance of next stage is either $\frac{2}{3} C_{OX} W_n L_n$ or $W_n L_n C_{OX}$ depending on whether the device is in saturation or cutoff. The triode load capacitance is $\frac{1}{2} W_p L_p C_{OX}$, like wise all the parasitics are directly proportional to the area of the corresponding device, approximately we can express every parasitic capacitance in terms of the gate capacitance of triode load with the help of some multiplication constant. In that case the load capacitance can become.

$$C_L = K_L W_P L_P COX \tag{4.27}$$

where K_L is the, multiplication factor depends on the technology and relative device sizes of the transistors. By substituting value of C_L into eq. 4.26we will get,

$$f_{osc} = \frac{1}{2N} \frac{\mu_p}{K_L L_P^2} [V_{GS} - V_T p - \frac{V_{SW}}{2}]. \tag{4.28}$$

From the above eqaution(eq. 4.28) for frequency of oscillation, the following observations are very clear.

- The Frequency of oscillation depends on the number of stages, in our case it is fixed to four stages.
- The capacitance factor K_L effects the frequency of oscillation, one can fix the K_L value for the desired frequency of oscillation.
- The most important factor is $\frac{\mu_p}{L_p^2}$, this is sensitive to temperature, process variations. And becomes the main reason for variation of frequency of oscillator over temperature and process variations.

Gain of VCO

As discussed in the chapter1 gain of the VCO is the second major issue in designing the VCO, it is desirable to reduce the gain of the VCO as much as possible. The process and temperature variations have direct impact on the gain of the VCO. This will be clear from the following discussion. The oscillator should be designed in such a way that it can be tuned over the desired tuning range for all the process corners and temperatures.

Let say the difference between the worst case fast and worst case slow frequencies is f_{var}. If we want to tune the worst case fast condition over a tuning range f_{tune} the slow condition must be tuned over $f_{tune} + f_{var}$ to achieve the higher limit of the tuning range. Therefore the gain of the VCO is given by

$$K_{VCO} = \frac{f_{var} + f_{tune}}{V_{hT} - V_{lT}} Hz/V \tag{4.29}$$

Where V_{hT}, V_{lT} are the lower limit and upper limit of the tuning voltage respectively. Fig. 4.10 shows the frequency variations of the oscillator for fixed current biasing of the delay-cell, this has a frequency variations of f_{var}=550MHZ. From this figure we can make some important observations as follows.

- Frequency increase for fast corner(FF) and decrease for slow corner(SS).
- In every corner(FF, SS, TT) the frequency decreases for increase in temperature.

The above two problems can be solved by fixedgm current bias. This biasing supplies more current at slow corners and higher temperatures. Fig. 4.11 shows the frequency variations for fixedgm biasing and this has a frequency variations of 220 MHZ, a considerable improvement when compared with the fixed current biasing. From figures (Fig. 4.10 and Fig. 4.11) we can make some important observations as follows.

- For fixed current biasing Fig. 4.10 the frequency decreases with increase in temperature.
- For fixed gm biasing Fig. 4.10 the frequency increases with increase in temperature.

Therefore there is a chance for maintaining the frequency as constant over temperature if we divide the total tail current into two parts one is biased by fixedgm and the other is biased by fixed current mechanisms. The same idea was implemented for biasing delay cell and found improvement in frequency variations as shown in Fig. 4.12. In this case the frequency variations are only 160MHZ. All these three simulations are done with a tail current of 360uAmps. In my case for mixed biasing(combination of fixed current, fixedgm) the best value for fixedgm current is 240uAmps out of 360uAmps, and this value is found through simulations only.

4.6 Tuning circuit:

Tuning circuit is a linear Voltage to Current converter. From the simulations i found that the minimum tail current i need is 10uAmps for the worst case fast condition(FF, 80) to make oscillating at 2.40GHz, and maximum tail current i need for the worst case slow condition(SS, 80) to make oscillating at 2.48GHZ is 70uAmps. From the charge pump characteristics[2], i have a voltage tuning range

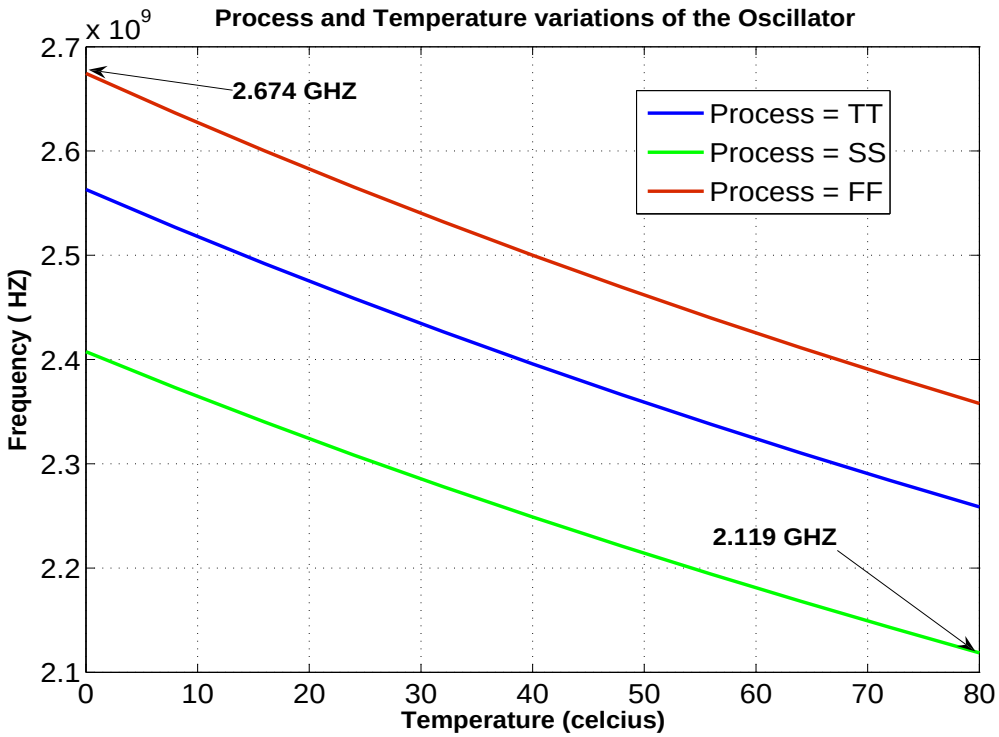


Figure 4.10: Process and Temperature variations For fixed current biasing

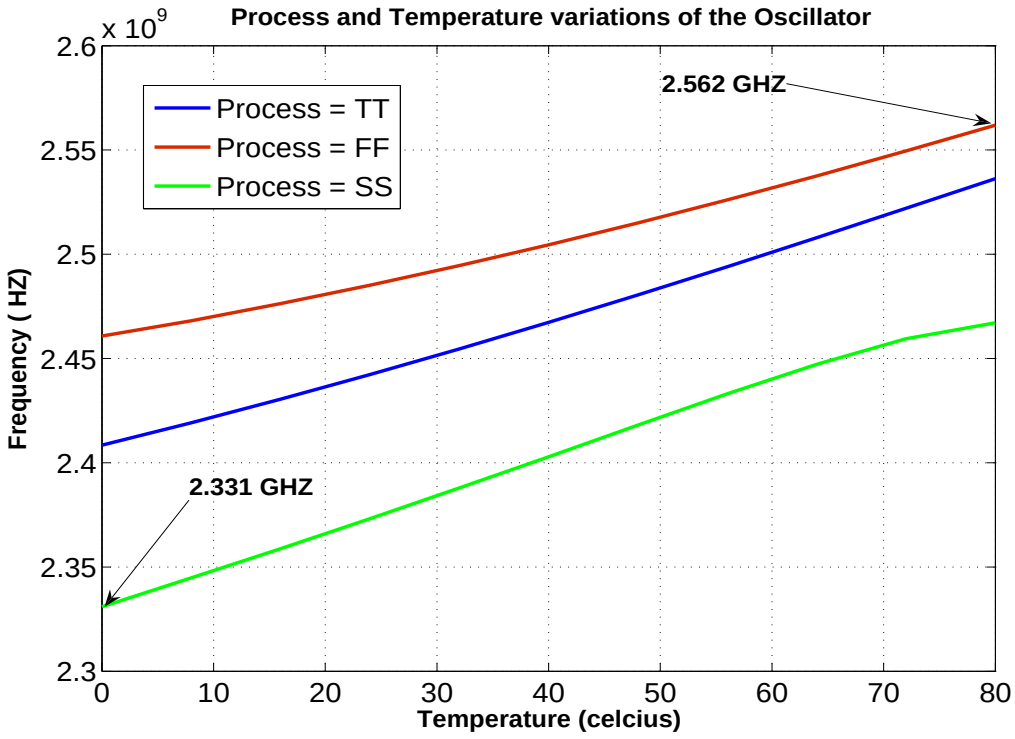


Figure 4.11: Process and Temperature variations For fixedgm biasing

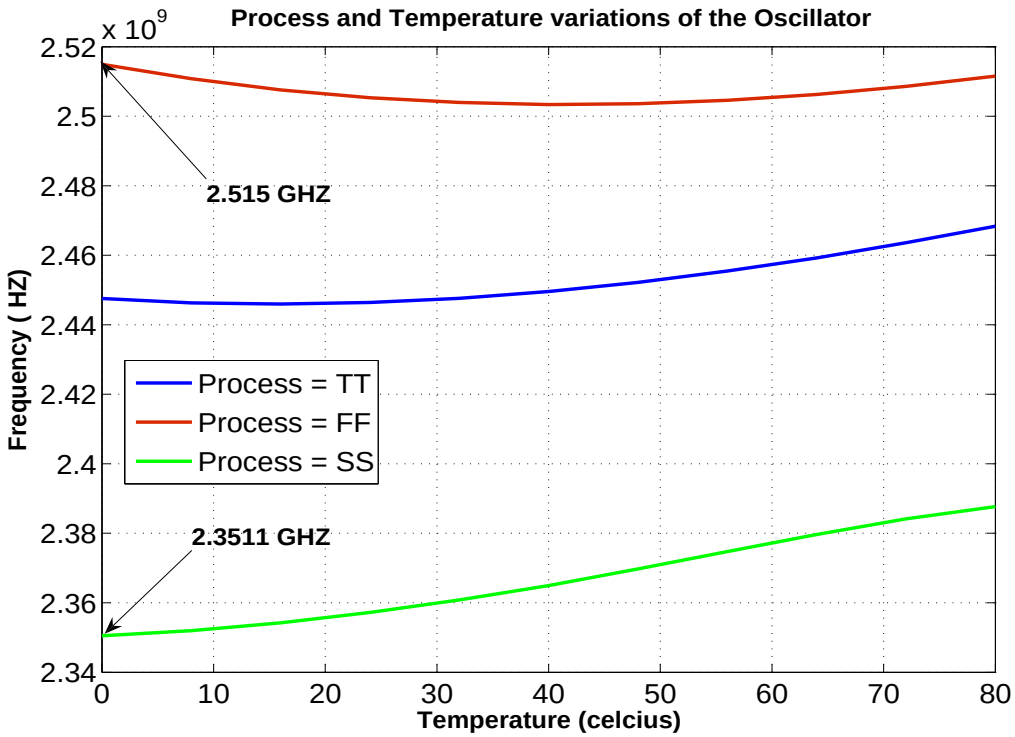


Figure 4.12: Process and Temperature variations For mixed biasing

of 0.3V to 1.2V. So the slope(S) of my Voltage to current converter is given by.

$$\begin{aligned} S &= \frac{I_2 - I_1}{V_2 - V_1} \\ &= \frac{70\mu - 10\mu}{1.5 - 0.3} \\ &= 50\mu A/V \end{aligned} \tag{4.30}$$

$$\tag{4.31}$$

So i need to design a voltage to current converter with this slope. The design is shown in Fig. 4.13

circuit operation

Fig. 4.13(b) shows the model of the voltage to current converter implemented in Fig. 4.13(a). As shown in Fig. 4.13(b) I_1 varies linearly with respect to tuning voltage(v_{tune}) in the range of 0 to 0.9V, this is realized by PMOS differential pair(M1, M2). AndI_2 varies linearly with respect to tuning voltage(v_{tune}) in the

range of 0.9V to 1.8V, this is realized by NMOS differential pair(M1, M2). Therefore the total current $I_1 + I_2$ flows through M11 varies linearly with respect to tuning voltage in the range of 0V to 1.8V, this current is replicated to the tail current of the delay-cell. The transistors M9, M10 provides sufficient voltage at the drain of M8 to make it operating in saturation region for given value of V_{cm}. Here V_{cm} value is chosen based on the common mode value of the delay-cell. The I-V characteristics of this voltage to current converter for different corners are shown in Fig. 4.14.

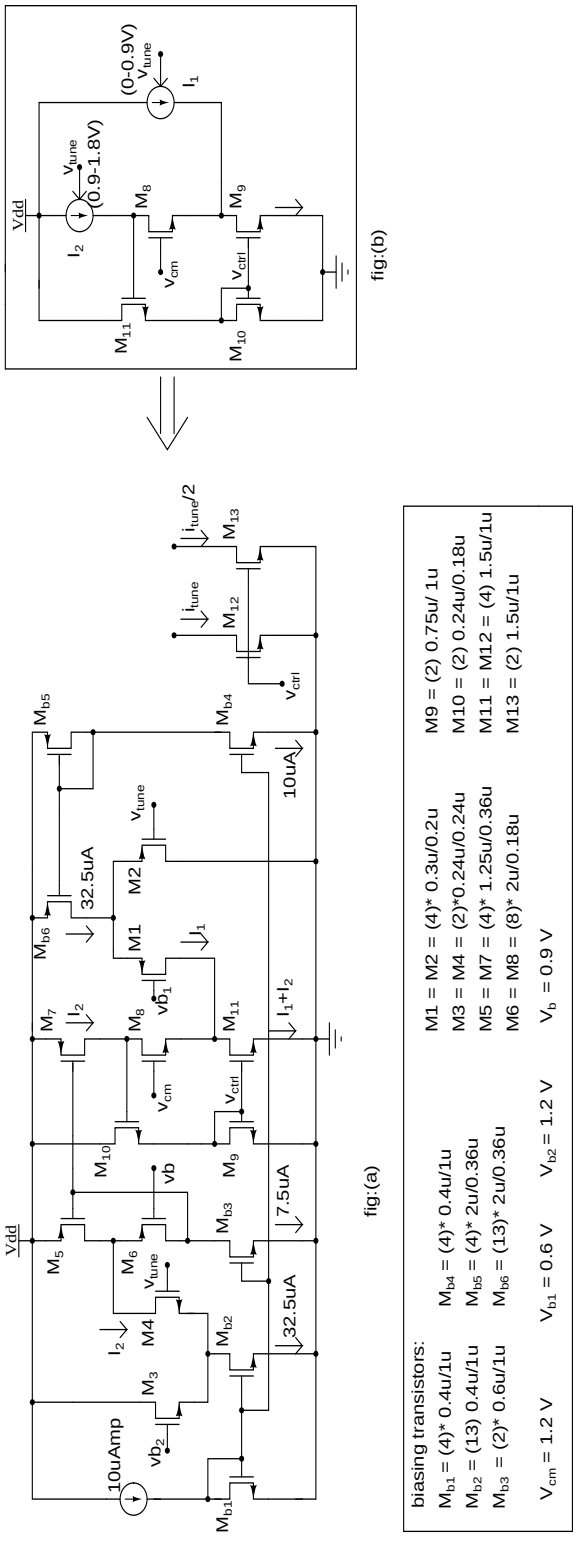


Figure 4.13: Voltage to Current converter

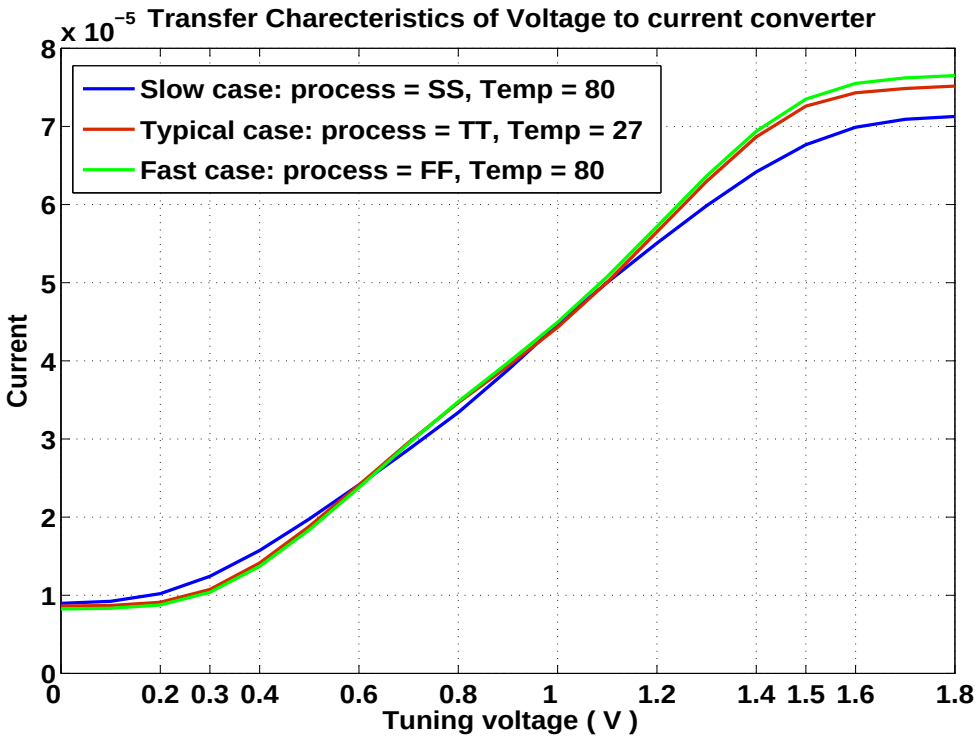


Figure 4.14: Transfer characteristics of voltage to current converter

CHAPTER 5

Gilbert Multiplier and Buffer

5.1 Basic gilbert-cell

For the multiplier in our case we don't need much linearity we just need a switching multiplier. This is equivalent to simple XOR gate in digital terminology. A simple gilbert-cell used for this multiplication is shown in Fig. 5.1, this is just equivalent to CML XOR gate. For an XOR gate if we apply two signals with the same frequency and one signal is delayed by quarter cycle with respect to another signal it produces an output with a frequency twice that of input signal. The simple implementation of XOR gate shown in Fig. 5.1 is mainly suffering from two problems.

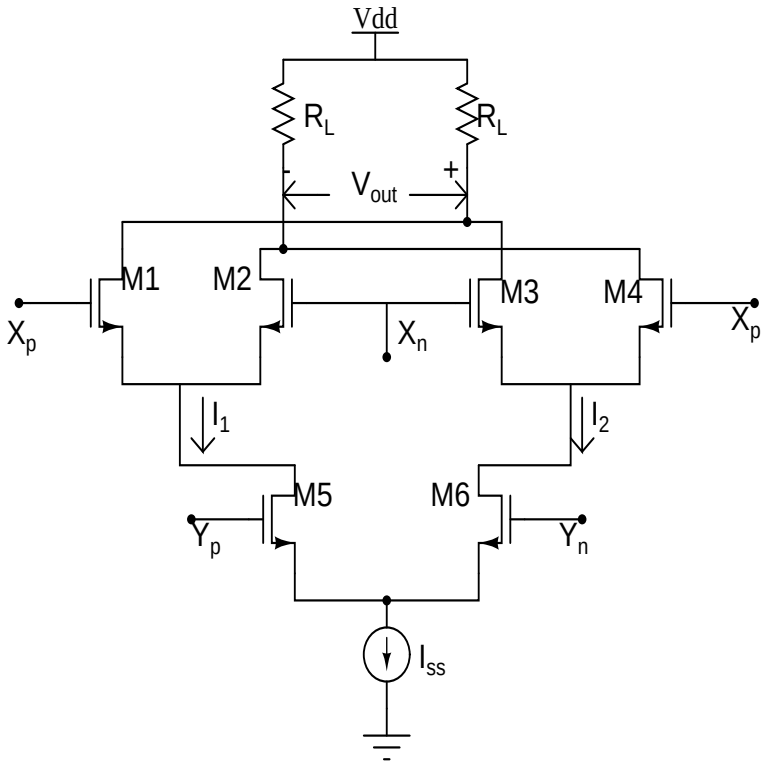


Figure 5.1: Basic gilbertcell

1.)Unequal rise and fall delays at the output, which in turn results in unsymmetrical out put with respect to output common mode.
2.)Unequal load seen by the input signals of the multiplier makes the ring oscillator to see different loads for different delay cells, which in turn leads to unequal phase shifts across different delay-cells. This will cause error in quadrature relation among I and Q signals of the oscillator (Fig. 2.1).

Unequal rise and fall delays:

Fig. 5.2 shows the output of the XOR gate for one cycle of the input. One important observation here is that output high to low transitions are taking place when the input X is stable and low to high transitions are taking place when Y is satbel. Let us take the time instant T1(*output high* $\longrightarrow$ *low transition*) where Y switches from low to high and X is stable, in this case the transition in the output takes place by switching the current through the transistors M5, M1(Fig. 5.1). Let us take the time instant T2(*output low* $\longrightarrow$ *high transition*) where X switches from high to low and Y is stable, in this case the the output transition takes place by switching the current through the transistors M2 only. Therefore it is clear that these two transitions does not have equal transition delays because of unequal signal paths.

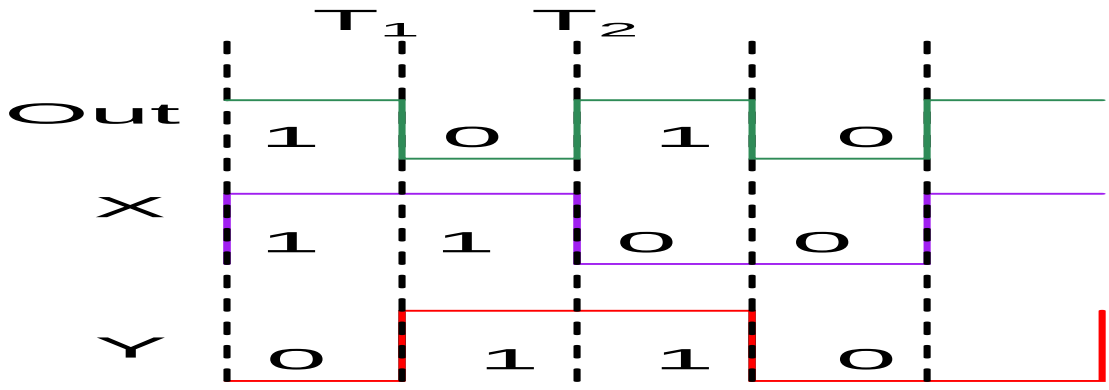


Figure 5.2: Output of the XOR gate

5.2 Symmetric gilbert Multiplier:

The two problems mentioned in previous section are eliminated with the architecture proposed in Fig. 5.3 where G1, G2 are two basic gilbert-cells with inputs interchanged from each other, A is an adder that adds the outputs from G1 and G2 and produces an output proportional to the product of two inputs. The circuit implementation is shown in Fig. 5.4 this circuit uses active inductors as load elements to enhance the bandwidth of the circuit. The explanation of active inductor is given in [2]

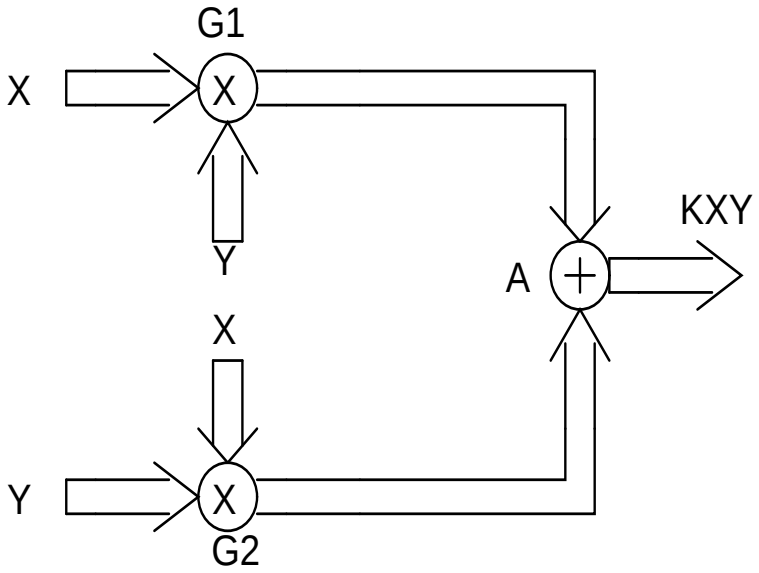


Figure 5.3: Block Diagram of symmetric multiplier

5.3 Buffer:

Buffer is a simple differential pair with active inductor loads, here the buffer is designed to drive a capacitive load of 180fF which is equal to load given by Up conversion Mixer, Down conversion mixer and divider chain in the PLL loop. Approximately the gain of the buffer is 1.

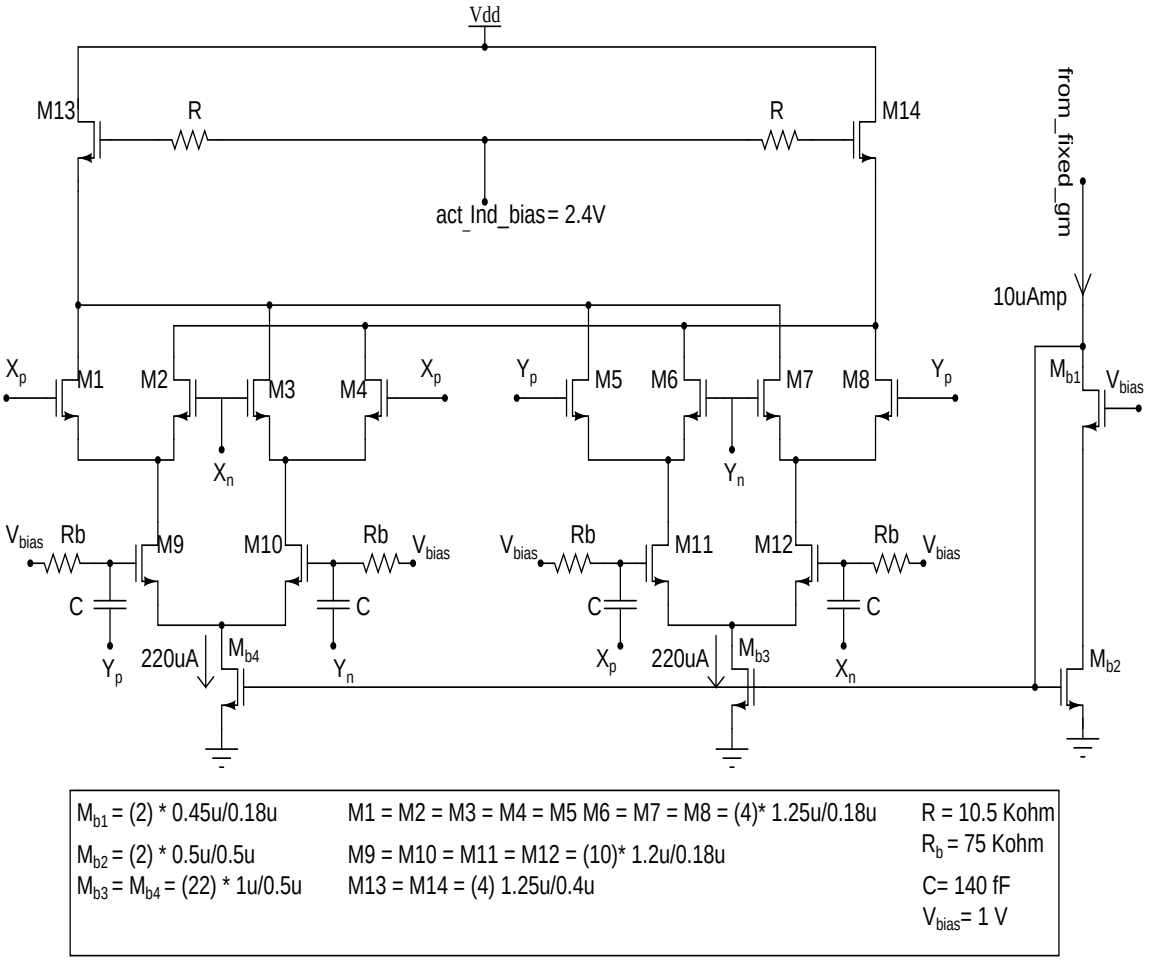


Figure 5.4: Circuit implementation of Symmetric Multiplier

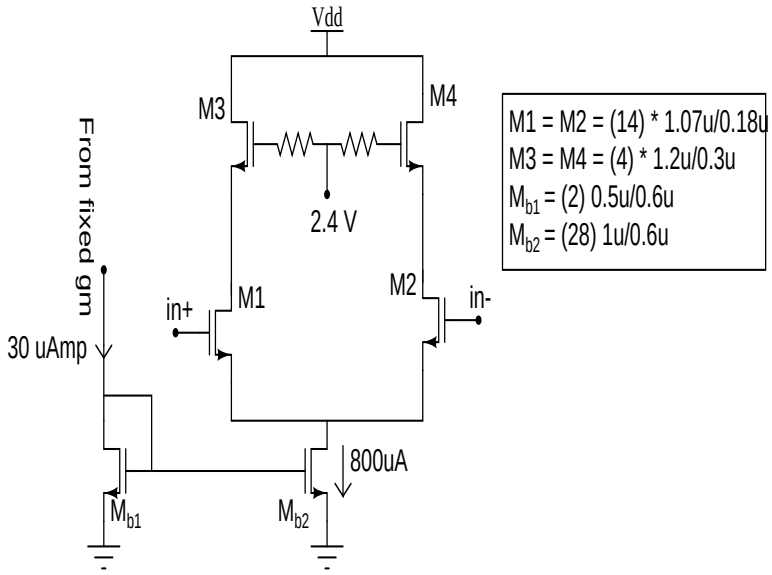


Figure 5.5: Schematic of the output buffer

CHAPTER 6

Layout and simulation results

6.1 Layout

Fig. 6.1 Shows the layout of RING VCO, Gilbert Multiplier and output Buffer,The remaining components are not laid out by the time of writing this thesis.

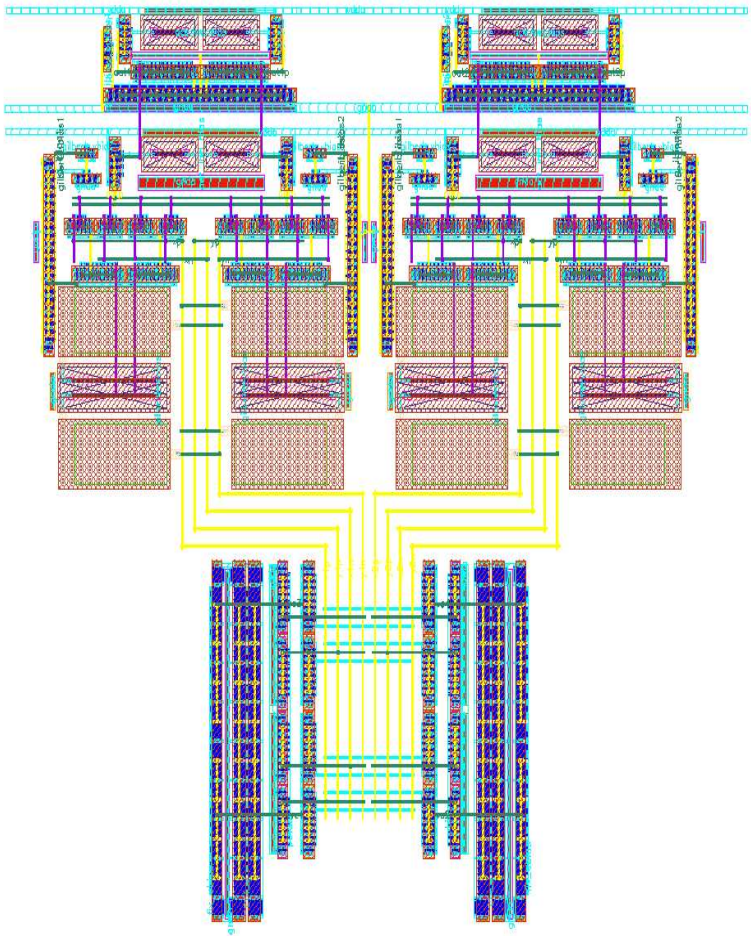


Figure 6.1: LAYOUT of the VCO:[Ring oscillator,Multiplier,Buffer]

6.2 Simulations

All the simulations shown here are done on the extracted view of the layout shown in Fig. 6.1. Table. 6.1 shows simulation results of The VCO across different corners and temperatures. Table. 6.2 shows the comparison between LC Oscillator and Ring Oscillator all these comparisons are made for typical process(TT) at $55°C$. Fig. 6.4 shows the I and Q signals at the output of the buffer. Fig. 6.2 shows the tuning of the VCO for different corners. Fig. 6.3shows the phase noise plots of the VCO over different corners.

Table 6.1: Simulation results for the VCO

MOS corners	T, °C	V_{out}, mV	Phasenoise, dBc/HZ	Power,mW
TT	27	308.42	-97.2	8.52
SS	0	325.26	-97.97	8.72
SS	80	240	-97.11	10.86
FF	0	263.68	-96.63	7.2
FF	80	288.95	-96.45	9.14

Table 6.2: Comparison of LC OScillator and RING Oscillator

Parameter	RING VCO	LC VCO
Power	9 mW	7.46mw
Phasenoise	-97.08 dBc/HZ	-117 dBc/HZ
Area	140 X 140 μm^2	370 X 140 μm^2
Gain	200 to 220 MHZ/V	140 to 165 MHZ/V

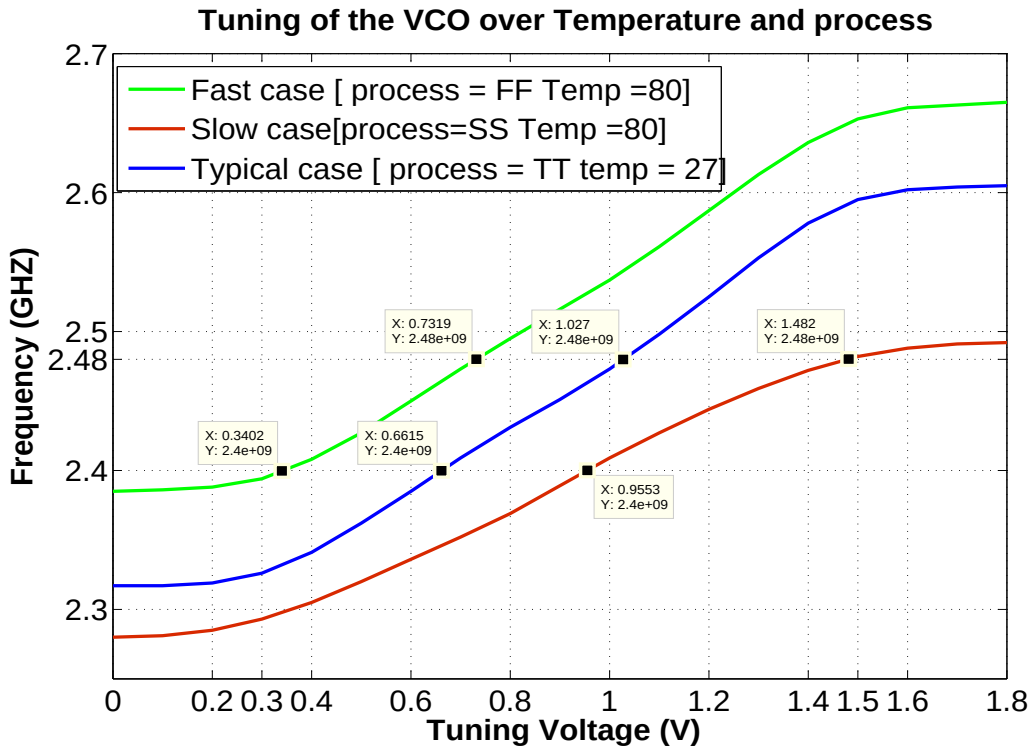


Figure 6.2: Tuning of the VCO over process and temperature

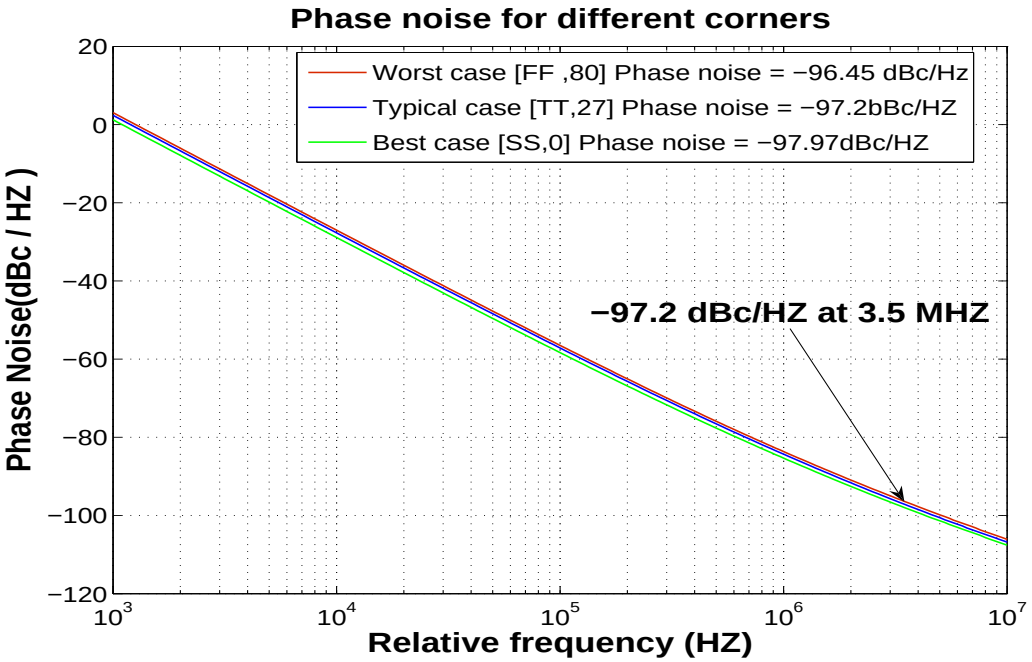


Figure 6.3: Variation of phase noise over process and Temperature

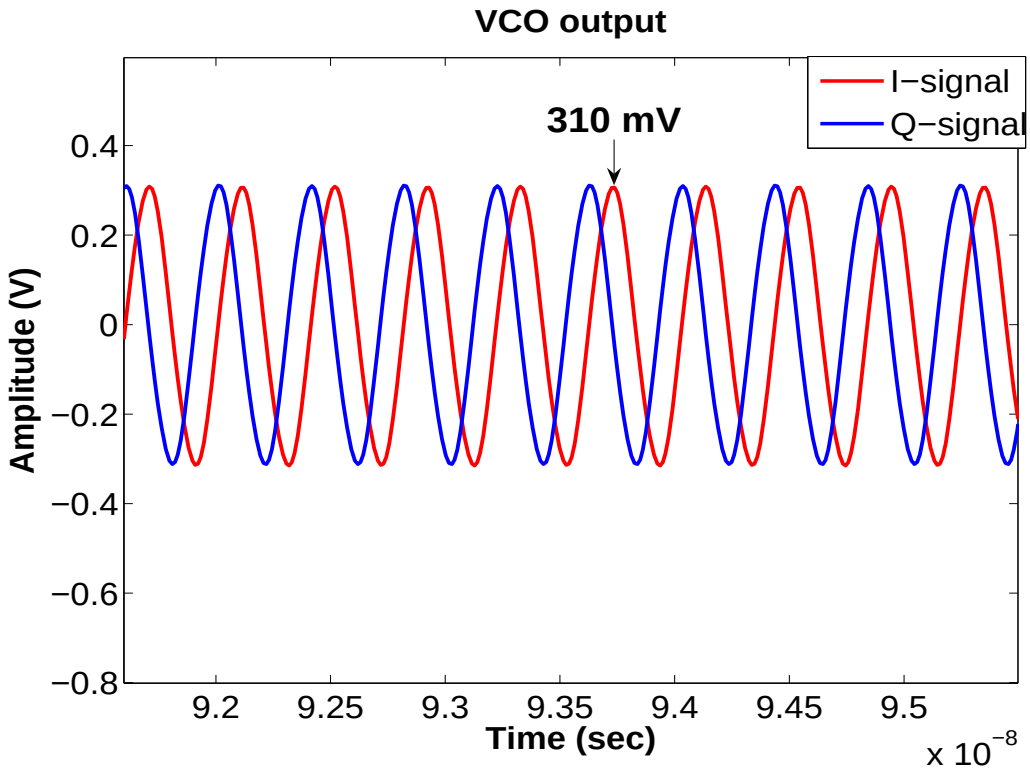


Figure 6.4: Output of the VCO

6.3 Conclusion and future work:

A low gain Ring VCO is designed with a phase noise suitable for zigbee standard. The power consumption of the Ring oscillator is gone up by 1.5 mW when compared to LC oscillator but there is a significant improvement in terms of area. The area of the Ring VCO has gone down by a factor of 2.6 when compared to the area of the LC oscillator(Tabel. 6.2).

Here we used a mixed biasing scheme(fixedgm, fixedcurrent) to reduce the gain of the VCO,One can go for current steering DAC method[4],where the tail current of the delay-cell is adjusted with a digital control by sensing the output frequency.

REFERENCES

[1] Behzad Razavi, *Design of analog CMOS Integrated circuits*. McGRAW-HILL INTERNATIONAL Edition ,2001.

[2] Arun.M "Design of frequency synthesizer for zigbee transciver," M.tech thesis ,Department of electrical energy,IIT MADRAS ,july,2007.

[3] Nhat M. Nguyen and G. Meyer, "Start-up and Frequency Stability in High-Frequency Oscillators ", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 27, no. 5, 1992.

[4] Todd Charles Weigandt "Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Synthesizers" ,Phd thesis ,Engineering-Electrical Engineering and Computer Sciences,UNIVERSITY OF CALIFORNIA, BERKELEY ,spring,1998.

[5] Nhat M. Nguyen and G. Meyer, "A Study of Phase Noise in CMOS Oscillators ", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, vol. 31, no. 3, 1996.

[6] "Broad band Communication circuits :http://www.ee.iitm.ac.in/ nagendra/videolectures/doku.php."