Design of a 12-Bit 40 MSPS Pipelined Analog to Digital Converter

A Project Report

submitted by

SHRAVAN SIDDARTHA N

in partial fulfilment of the requirements
for the award of the dual degree of

BACHELOR OF TECHNOLOGY

and

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

May 2011

This thesis is dedicated to my parents

Geetha and **Srinivas Reddy**.

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a 12-Bit 40 MSPS Pipelined Analog to Digital Converter**, submitted by **Shravan Siddartha N**, to the Indian Institute of Technology Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Advisor,
Associate Professor,
Dept. of Electrical Engineering,
IIT-Madras, 600 036

Place: Chennai
Date: 27 May 2011

ACKNOWLEDGEMENTS

At the onset I would like to thank my guide Dr. Nagendra Krishnapura for his support and motivation during this project. I thank Dr. Dilip Veeraraghavan for his valuable advice and thought provoking discussions during my initial years at IIT. I sincerely thank Dr. Shanthi Pavan for his awesome lectures on analog circuit design and Dr. Krishna Vasudevan for his power electronics courses.

I would like to take this opportunity to thank my friends Rahul, Kitty, Dhiraj, Amar, Rakesh, Sadu, Manmohan and Shashank for their company and support during my stay at IITM. I thank my labmates Srinu, Santosh, Nimit, Harshit, Ravi, Kamlesh, Anil, Sandeep, Lokesh, Naga, Timir, Ankesh, Karthik, Anirudh, Radha, Shankar, Amrith, Kunal and Pradeep for their advice and help during this project.

I don't find words to express my gratitude and thanks to my parents for all the sacrifices they have made for my upbringing and education. As a token of my undying love and gratitude I dedicate this thesis to my parents.

ABSTRACT

This project involves the design of a 12-bit pipelined ADC with sampling rate of 40 MSPS. The ADC has been designed, laid out and verified in UMC 0.18 μm CMOS technology with a 1.8 V supply. It is designed in 6 stages with each stage contributing 2 bits (effectively). The ADC occupies an active area of 1.25 mm $\times$ 1 mm and consumes a total power of 50 mW from 1.8 V supply.

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ABBREVIATIONS

MSPS	Mega samples per second
ADC	Analog to Digital converter
DAC	Digital to Analog converter
SC	Switched sapacitor
DEM	Dynamic element matching
UGB	Unity gain bandwidth
S/H	Sample and hold
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET
GBA	Gain boosting amplifier
NGBA	NMOS gain boosting amplifier
PGBA	PMOS gain boosting amplifier
CMFB	Common mode feedback
MSB	Most significant bit
LSB	Least bignificant bit
DEC	Digital error correction
PSD	Power spectral density

NOTATIONS

A_{dc}	DC gain
ω_u	Unity gain bandwidth
ϕ_m	Phase margin
ϕ_s	Sampling phase
ϕ_h	Hold phase
ϕ_{sA}	Advanced sampling phase
ϕ_{hA}	Advanced hold phase
V_{FS}	Full scale voltage

CHAPTER 1

Introduction

Over the past years, advancements in the field of Digital signal processing (DSP) and availability of robust and cheap digital circuits has made DSP more preferable to analog processing. However the inability of human beings to process digital signals calls for interfacing devices between the DSP and the natural world as shown in Fig. 1.1. The interface devices primarily consist of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The ADC converts a continuous time continuous amplitude signal into a digital signal while the DAC perform the reverse operation of converting a digital signal into a continuous time discrete amplitude signal. This chapter aims at providing the basic principles of analog to digital conversion and details of some popular ADC architectures.
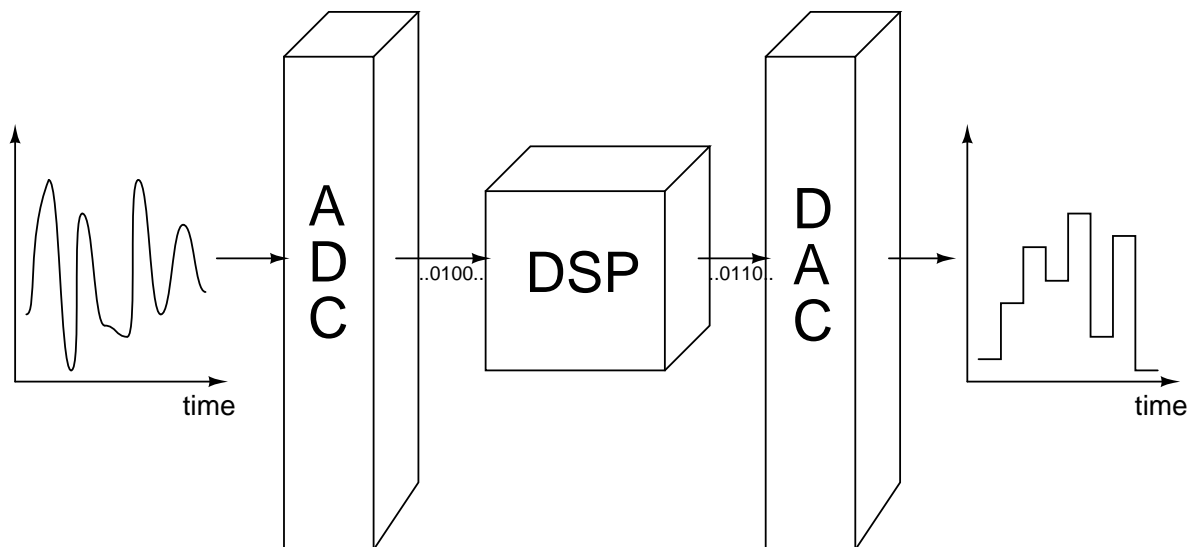
Figure 1.1: Functional view of interface devices.

1.1 Fundamentals of ADC

1.1.1 Sampling

Sampling is the first step of analog to digital conversion. Sampling is the process of converting a continuous time signal into a discrete time signal. During sampling the input signal is sampled at continuous intervals to produce a discrete time signal as shown in Fig. 1.2. The information in the original signal is not lost during sampling if the sampling rate f_s is greater than $2f_b$, where f_b is the bandwidth of the signal which is being sampled.
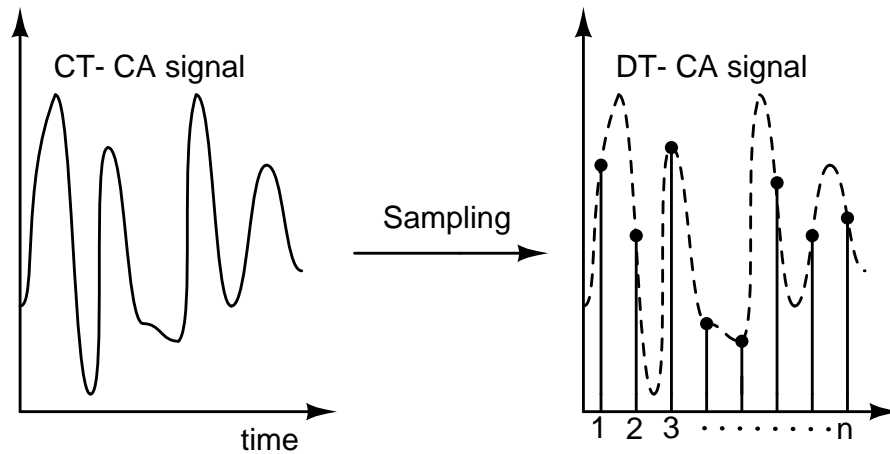
Figure 1.2: Illustration of sampling occurring in an ADC.

1.1.2 Quantization

Quantization is the second step of analog to digital conversion. The block that performs quantization is called a quantizer. Quantization is the process of coverting a continuous amplitude signal into a discrete amplitude signal. It basically rounds off the given value to the nearest predefined level as shown in Fig. 1.3. The predefined levels are equi-spaced with a separation of LSB (Δ).

Quantization results in loss of information as the values are rounded off. This loss of information is modelled as quantization error (e_q) as shown in Fig. 1.4.
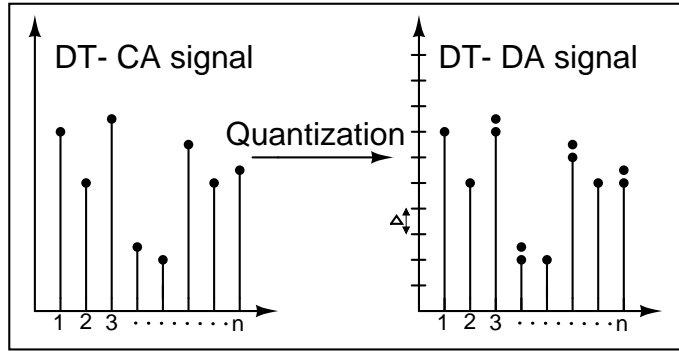
Figure 1.3: Illustration of quantization occurring in an ADC
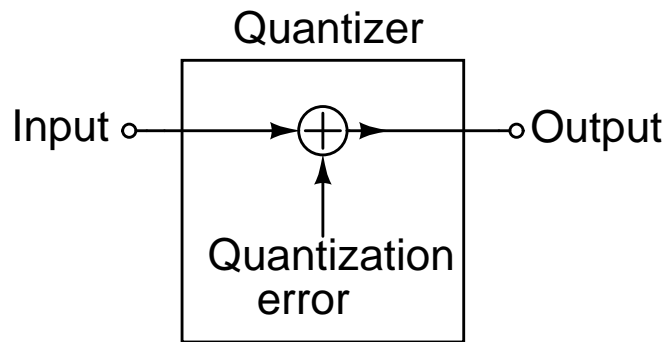
Figure 1.4: Quantizer model.

The input output characteristics for a 2-bit quantizer are shown in Fig. 1.5.

(a)

(b)
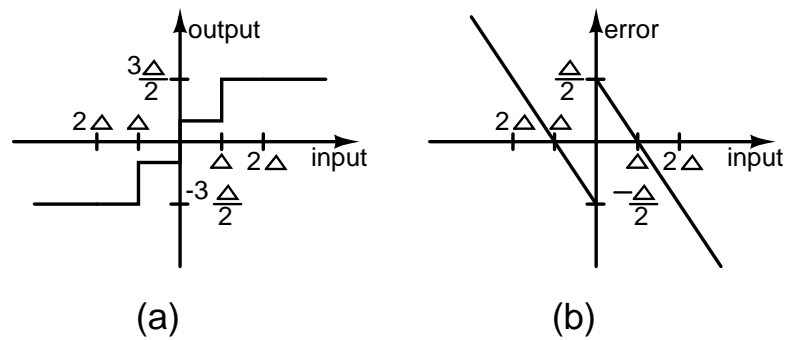
Figure 1.5: (a)Input versus output (b)Input versus quantization error.

The quantizaion error is dependent on input. This makes it very difficult to model this error. For this reason it is modelled as additive white gaussian noise. This assumption agrees with statistical data. The value of e_q is dependent on Δ

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which is in turn dependent on the resolution (N) and full scale voltage (V_{FS}) of the ADC as shown below.

$$e_q = \frac{\Delta^2}{12} \tag{1.1}$$

$$= \frac{1}{12} \times \left(\frac{V_{FS}}{2^N}\right)^2 \tag{1.2}$$

The Signal-to-Noise Ratio (SNR) for a full-scale sinusoidal input is given by Eq. (1.3)

$$SNR = (6.02N + 1.76)dB \tag{1.3}$$

1.2 ADC architectures

The type of ADC to be used for a application varies widely depending upon input bandwidth, resolution, power consumption, etc. Depending on this factors various architectures are chosen. Some of the popular architectures are

- Flash ADC
- Successive approximation register (SAR) ADC
- Pipelined ADC

A brief introduction to the topologies and working principles of the above mention ADCs is given in the following sections.

1.2.1 Flash ADC

As the name suggests, the flash ADC can process inputs at a very high rate. It consists of a resistive ladder which produces the required reference voltages. The input is then compared with this reference voltages and output is determined. The comparison is done by using an array of comparators as shown in Fig. 1.6.
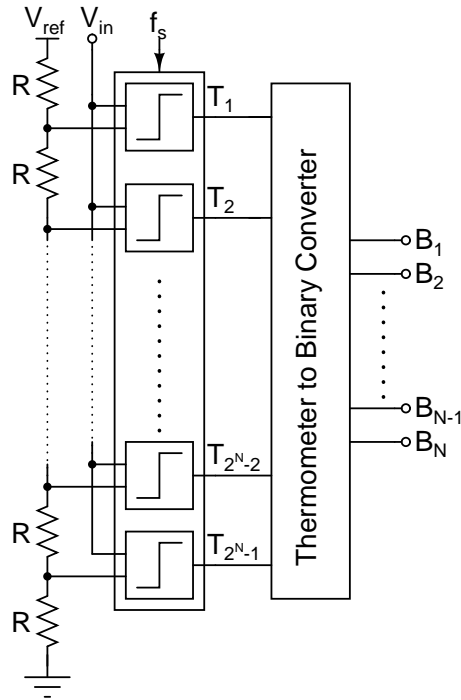
Figure 1.6: Block diagram of a N-bit flash ADC.

The outputs of the comparator array are thermometer coded. This thermometer code $(T_1 - T_{2^N-1})$ is converted into a binary code $(B_1 - B_N)$ by using a thermometer to binary converter. The disadvantage of Flash ADC is that the number of resistors and comparators increase exponentially with N. For this reason, flash ADC is recommended for high speed low resolution applications.

1.2.2 Successive approximation register (SAR) ADC

The SAR ADC works on the principle of binary search. It consists of a single comparator in contrast to the flash ADC. This comparator takes the reference voltage from a N-bit DAC. The input for DAC is produced by a control circuit as shown in Fig. 1.7.
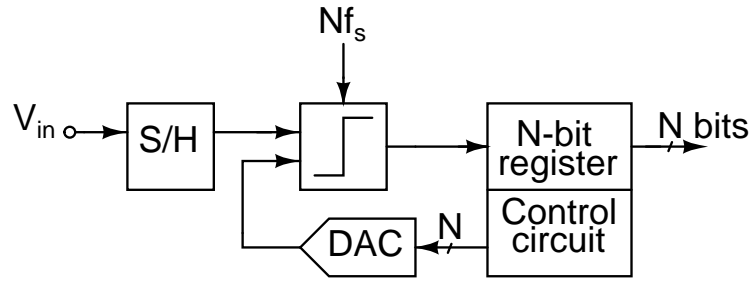
Figure 1.7: Block diagram of a N-bit SAR ADC.

The cost paid for reduced number of components is the speed. To produce a N-bit output, the comparator has to operate at a speed $N.f_s$. Thus SAR ADC is recommended for low speed high resolution applications.

1.2.3 Pipelined ADC

This architecture is a compromise between the flash ADC and SAR ADC. It eliminates the sampling rate problems associated with SAR by processing the data in multiple stages parallelly [1]. The number of comparators needed is more than that of a SAR ADC but much lower than that of a flash ADC.

A N-bit, two stage pipeline ADC is discussed here. The block diagram for this converter is shown in Fig. 1.8.
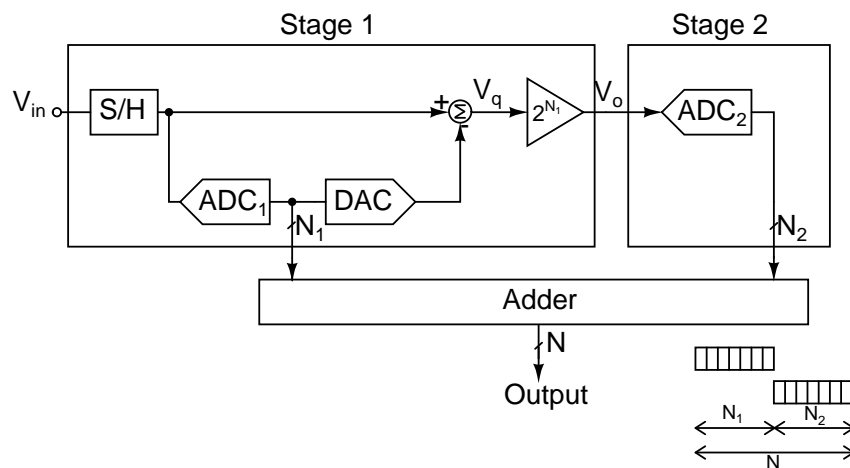
Figure 1.8: Block diagram of a N-bit pipelined ADC.

The input is sampled by the sample and hold circuit in stage 1. This sampled value is now processed by ADC_1 (N_1-bit ADC) to determine the nearest reference voltage. Depending on the output of ADC_1, the DAC generates the reference value. This voltage is then subtracted from the sampled value to get the error V_q. This error V_q is now amplified to the full scale (V_o) using an amplifier of gain 2^{N_1} as shown in Fig. 1.8. Generally the DAC, subtractor and multiplier are realized as a single block called MDAC. The output V_o is sampled by the second stage. The second stage consists of ADC_2 which extracts the remaining N_2 bits. The outputs of the two stages are added in a non-overlapping fashion in the adder block as shown in Fig. 1.8. The V_q and V_o characteristics are shown in Fig. 1.9.
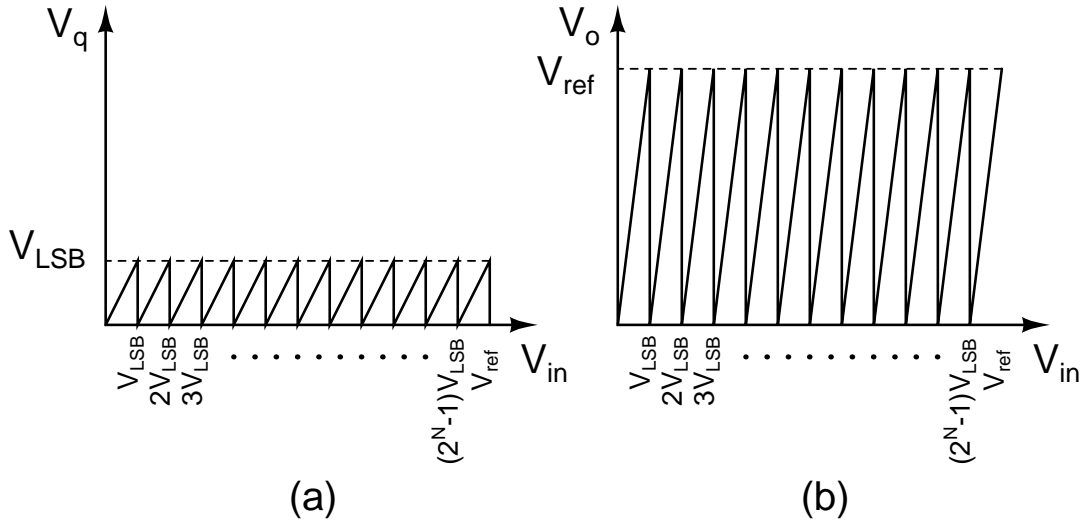
Figure 1.9: Two stage pipelined ADC (a) V_q versus V_{in} (b) V_o versus V_{in}.

Digital error correction

The drawback with the above architecture is that it is very sensitive to errors in the transition points of ADC_1. An error in the transition points of ADC_1 results in the overloading of ADC_2. This problem can be mitigated by

- Reduce interstage gain to 2^{N_1-1}.
- Shifting all the transition points of ADC_1 to the right by 0.5LSB.
- Reduce the number of comparators of ADC_1 to $2^{N_1} - 1$ by removing the last comparator.

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The block diagram of the modified architecture is shown in Fig. 1.10. The V_q and V_o characteristics are shown in Fig. 1.11. As the gain is reduced by a factor of two, the bits from both the stages should be added with 1-bit overlap as shown in Fig. 1.10. This reduces the resolution to N-1.
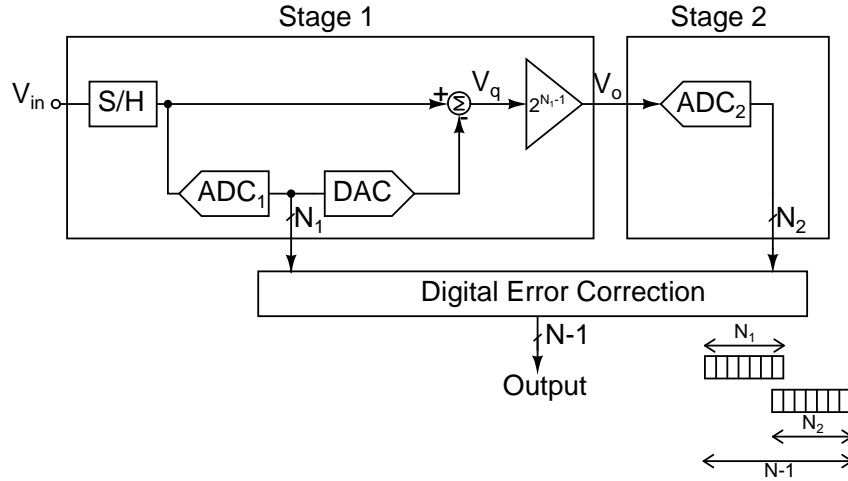
Figure 1.10: Block diagram of modified pipelined ADC.
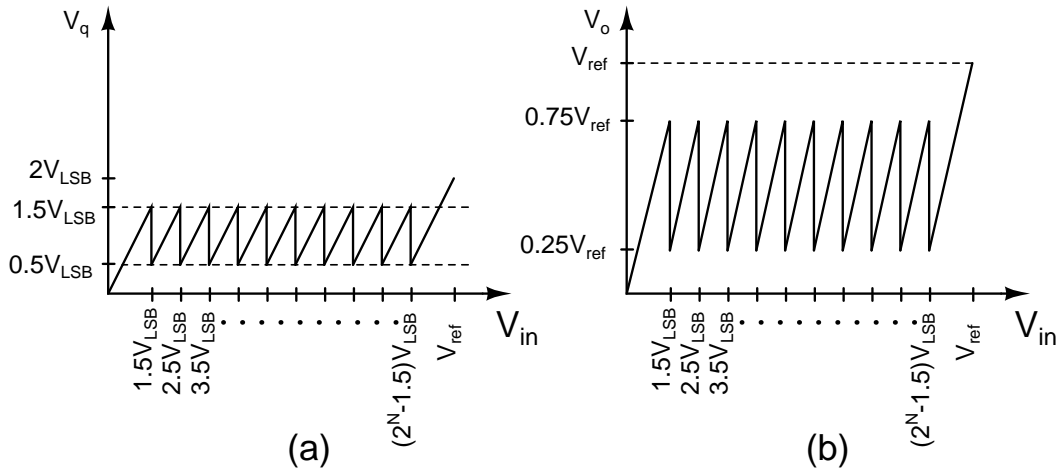
Figure 1.11: Modified pipelined ADC architecture (a) V_q versus V_{in} (b) V_o versus V_{in}.

1.3 12-bit pipelined ADC architecture

The pipelined ADC has been designed with the following specifications.

- Sampling rate - 40 MSPS.

- Reference voltage - 2V peak-to-peak differential.

- Number of stages - 6.

- Effective number of bits per stage - 2.

- Technology - 0.18 μm CMOS.

- Supply - 1.8 V.

The block diagram for the ADC is shown in Fig. 1.12.
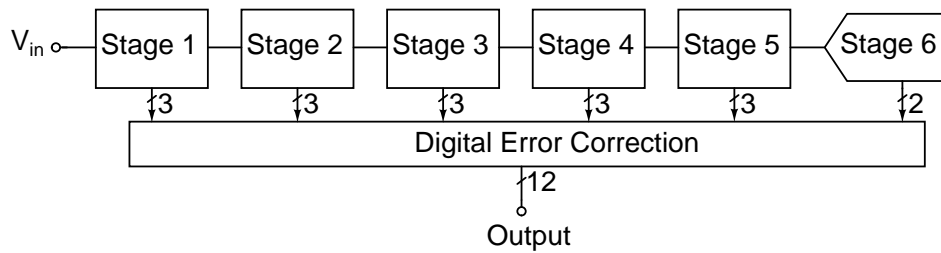
Figure 1.12: Block Diagram of 12bit ADC.

1.4   Organisation of the thesis

Chapter 2 presents the basics of switched capacitor (SC) techniques. It is followed by realization of MDAC with this techniques. Various problems associated with this circuits and their solutions are discussed. Various aspects like capacitor sizes, opamp specs., etc are determined.

Chapter 3 presents the design details of opamps to be used in the MDACs. The concept of gain boosting is introduced. Based on this concept, high speed, high gain opamps have been designed.

Chapter 4 presents the control circuit for the MDAC. It presents the design details of 2.5-bit flash ADC, bubble correction circuit and thermometer to binary converter. The concept of dynamic element matching (DEM) is discussed.

Chapter 5 presents the design details of the digital error correction and the timing analysis for all the stages.

Chapter 6 presents the layout details and the simulation results for the entire ADC.

CHAPTER 2

MDAC Architecture

The MDAC is realized using switches capacitor (SC) techniques. The working of a basic SC amplifier is discussed below.

2.1 Switched capacitor amplifier

The working principle of a SC amplifier is, the voltage across a capacitor is inversely proportional to the capacitance (for constant amount of charge). The circuit diagram for a SC amplifier is shown in Fig. 2.1.
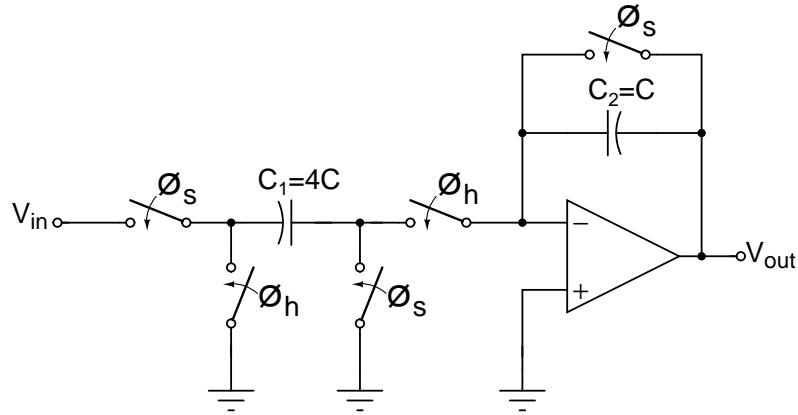
Figure 2.1: Circuit diagram of a SC amplifier with gain of 4.

The cloocks ϕ_s and ϕ_h are non overlapping. During ϕ_s, V_{in} is sampled onto capacitor C_1 and capacitor C_2 is reset. A charge of $V_{in} \times C_1$ is stored on C_1. During ϕ_h all this charge is transferred from C_1 to C_2 by the opamp. The output voltage V_{out} is given by

$$V_{out} = \frac{C_1}{C_2} \times V_{in} \tag{2.1}$$

The gain of 4 required in the MDAC is achieved by choosing $C_1 = 4 \times C_2$.

2.1.1 Charge Injection

The circuit in the previous section (Fig. 2.1) suffers from the problem of charge injection onto the capacitor C_1 when the switches are opened. This charge, which is input dependent, results in harmonic distortion of the output. This problem can be mitigated by advancing the falling edge of clocks controlling the switches connecting the top plate of C_1 to ground and virtual ground as shown in Fig. 2.2.
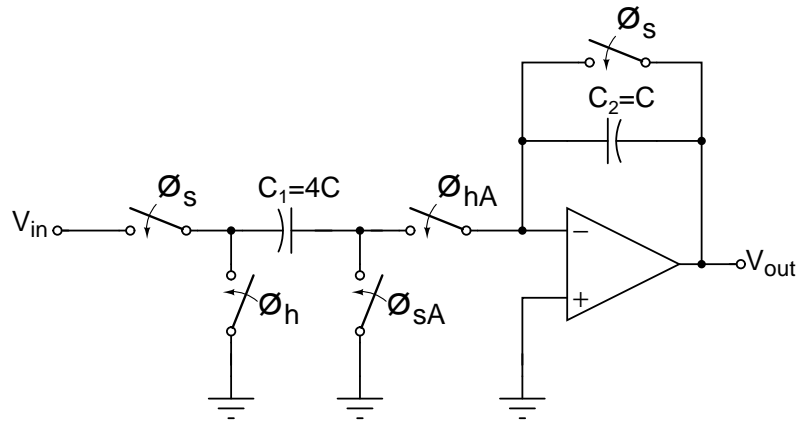
Figure 2.2: Circuit diagram of a SC amplifier with ϕ_{sA} and ϕ_{hA}.

Now the charge is injected onto C_1 only by the switches controlled by ϕ_{sA} and ϕ_{hA}. This charge is signal independent and hence doesn't cause harmonic distortion. This charge however results in an offset which is cancelled by using a fully differential circuit.

2.1.2 Nonlinear switch resistance

The switches in the above circuit (Fig. 2.2) are realized using MOS transistors. The ON resistance (R_{on}) is given by

$$R_{on} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_T)} \tag{2.2}$$

$V_{GS} = V_{dd} - V_{in}$. This dependence of R_{on} on V_{in} results in harmonic distortion. This issue is resolved by bootstrapping the input switch. The concept of bootstrapping is discussed in detail later.

2.2 MDAC

The SC amplifier discussed above, with necessary changes, can be modified as a MDAC. The circuit diagram for a fully differential MDAC is shown in Fig. 2.3.
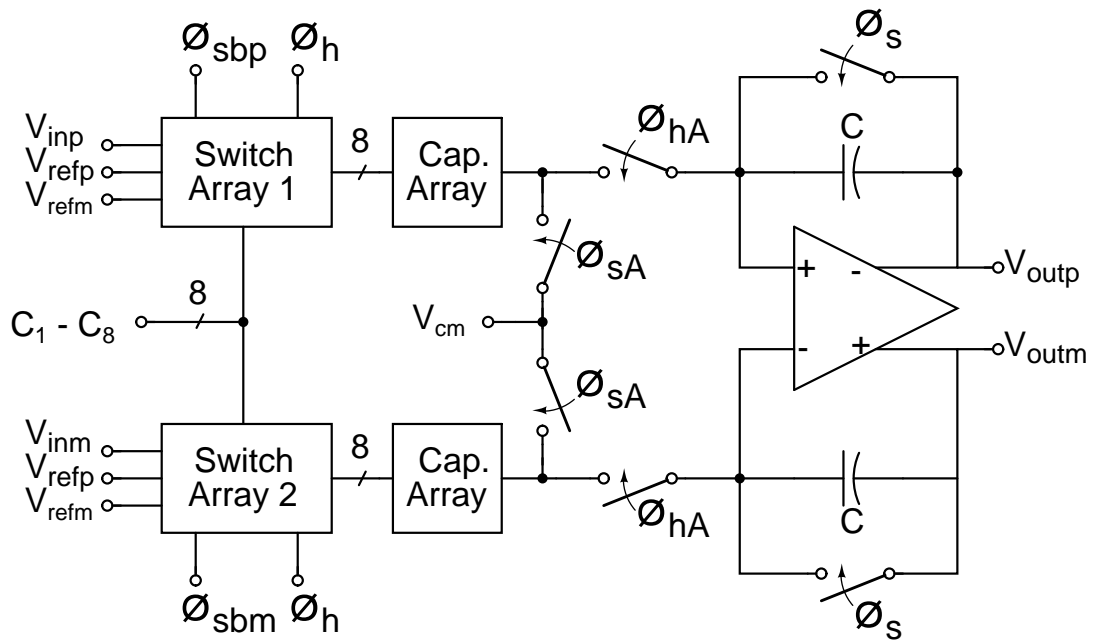
Figure 2.3: Circuit diagram of MDAC.

The capacitor C_1, used in the SC amplifier, is split into 8 capacitors of value $\frac{C}{2}$ each as shown in Fig. 2.4.
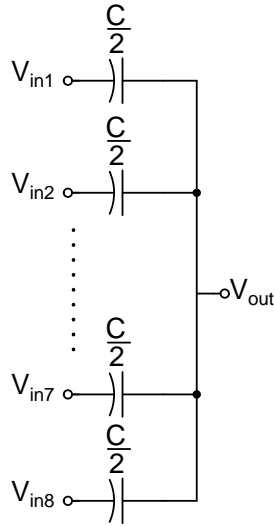
Figure 2.4: Circuit diagram of the capacitor array used in the MDAC.

V_{in1} to V_{in8} are generated by a array of switches. The circuit diagrams for both the switch arrays, switch array 1 and switch array 2, are shown in Fig. 2.5 and Fig. 2.6.
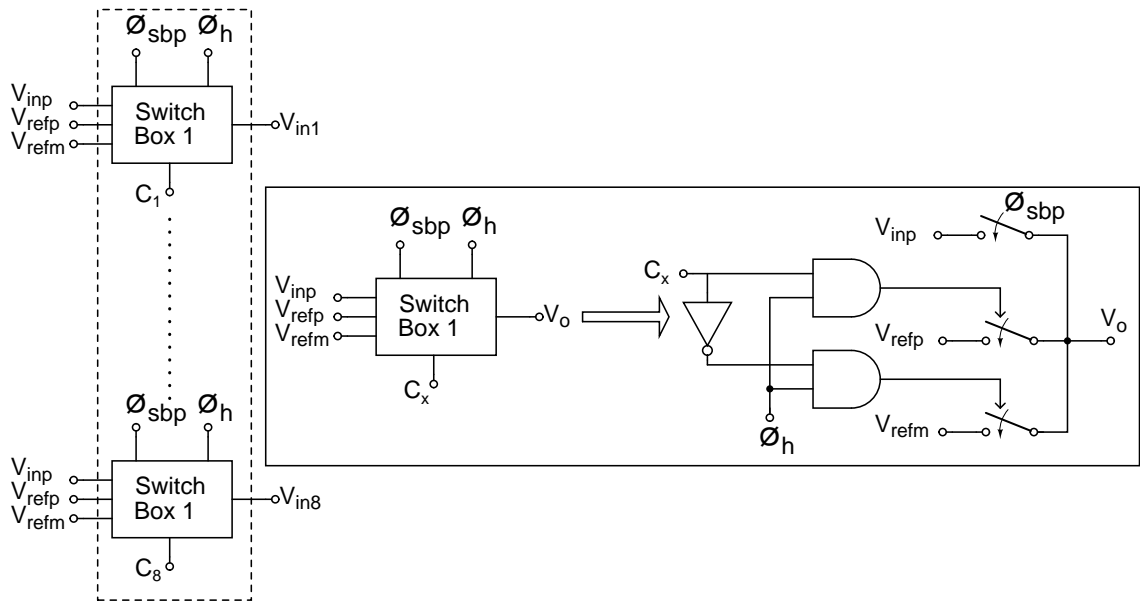
Figure 2.5: Circuit diagram of the switch array 1 used in MDAC. ϕ_{sbp} is the Bootstrapped version of ϕ_s with respect to V_{inp}.

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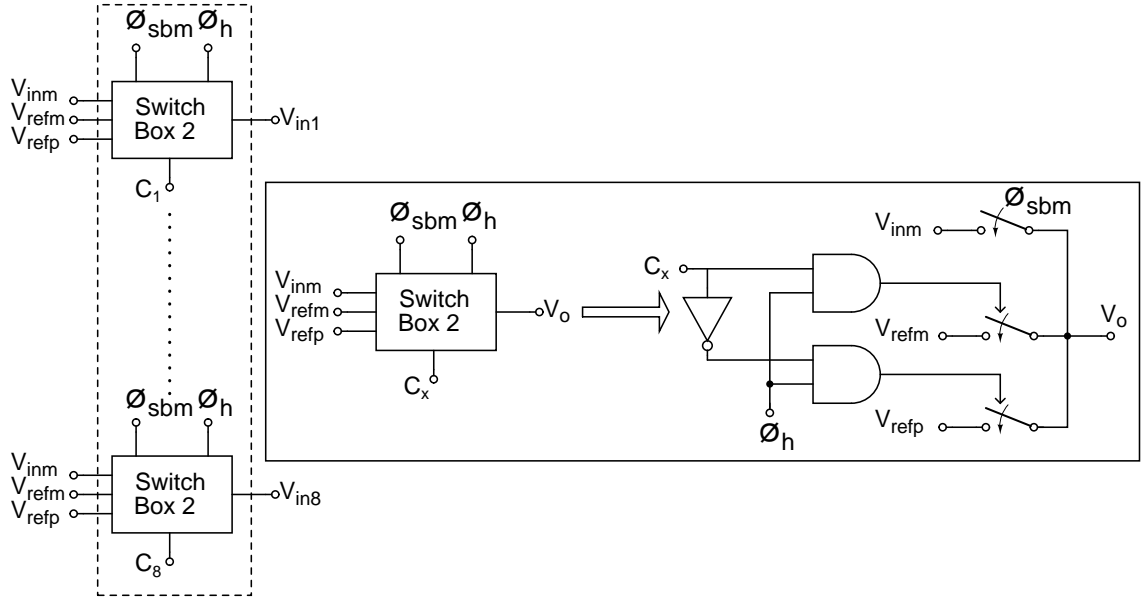
Figure 2.6: Circuit diagram of the switch array 2 used in MDAC. ϕ_{sbm} is the Bootstrapped version of ϕ_s with respect to V_{inm}.

During ϕ_s, V_{in} is given to the bottom plate of these capacitors through a bootstrapped switch. During ϕ_h, the bottom plate of the capacitors are tied to either V_{refp} or V_{refm} depending on the output of the sub ADC. Out of the eight control signals (C_1-C_8) to the MDAC, C_1 to C_6 are the outputs of sub-ADC. The control signal C_7 is logic 1 and C_8 is logic 0. The relationship between the DAC output and control signals is shown in Table 2.1.

Table 2.1: DAC output (verses) Control Signals.

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	DAC output
1	1	1	1	1	1	1	0	$0.75V_{ref}$
0	1	1	1	1	1	1	0	$0.50V_{ref}$
0	0	1	1	1	1	1	0	$0.25V_{ref}$
0	0	0	1	1	1	1	0	0
0	0	0	0	1	1	1	0	$-0.25V_{ref}$
0	0	0	0	0	1	1	0	$-0.50V_{ref}$
0	0	0	0	0	0	1	0	$-0.75V_{ref}$

2.3   Determining C and Opamp Specifications

2.3.1   Value of C

The value of the feedback capacitor (C) depends on two factors.

- Thermal Noise
- Capacitor Matching

Thermal Noise

Thermal noise is produced from a variety of sources like resistors, MOS transistors. The thermal noise (rms) on a capacitor of value C with a series resistance R is given by $\sqrt{\frac{kT}{C}}$ where k is the Boltzmann's constant and T is the absolute tempetarure. As value of thermal noise is inversely proportional C, increasing the the value of C decreases the thermal noise. For the proper functioning of the ADC, thermal noise is restricted to $0.1V_{LSB}$. This gives

$$\sqrt{\frac{KT}{C_{sample}}} < 0.1V_{LSB} \tag{2.3}$$

The input is sampled onto eight capacitors of value $\frac{C}{2}$ in the capacitor array. Hence $C_{sample} = 8 \times \frac{C}{2}$. The minimum capacitance (C) to be used in each stage to mitigate thermal noise is shown in Table 2.2

Table 2.2: Minimum capacitance to restrict the thermal noise to 0.1LSB.

Stage	LSB(mV)	C	C_{sample}
1	0.5	414 fF	1.66 pF
2	2	26 fF	0.10 pF
3	8	1.6 fF	6.4 fF
4	32	0.10 fF	0.4 fF
5	128	6 aF	24 aF

Capacitor Matching

The amplification obtained in the MDAC is given by the ratio of capacitors. The values of capacitors however vary from the nominal value (C_N) due to various reasons like imperfect edges of devices and chip gradients. This causes mismatch between capacitors. For MIM capacitors, the random mismatch, due to imperfect edges, is inversely proportional to $\sqrt{WL}$ where W and L are the widths and lengths of the capacitor. The matching between two capacitors of nominal value(C_{nom}), as provided by the process vendor (UMC) is shown in Table 2.3

Table 2.3: Matching report of two capacitors. σ - standard deviation.

C_{nom} (fF)	3σ (%)
5000	0.048
3000	0.081
1000	0.100
600	0.120
300	0.132
100	0.156

The matching between capacitors for stage 1 should be 10-bit accurate. From Table 2.3 it can be observed that to get such high accuracy, very larger capacitances are required. This however increases the load on the opamp and hence increases the power consumption. To counter this problem Dynamic Element Matching(DEM) is introduced. The usage of DEM gives improved SFDR by converting the undesirable harmonic distortion (due to mismatch) into white noise.

The the value of capacitance (C) is chosen only taking thermal noise into consideration and it is assumed that mismatch can be countered by DEM. The value of C chosen for each stage is shown in Table 2.4.

Table 2.4: Values of C used in each stage.

Stage	C (fF)
1	1000
2	200
3	150
4	150
5	150

2.3.2 Opamp specifications

The finite dc gain (A_{dc}) and unity gain bandwidth(UGB) of the opamp result in static and dynamic errors at the output of the MDAC.

Finite DC gain(A_{dc})

For a inverting amplifier of gain $= 4$, finite DC gain of opamp results in a static error given by Eq.(2.5).

$$V_{out} = \frac{4}{\left(1 + \frac{5}{A_{dc}}\right)} \times V_{FS} \tag{2.4}$$

$$Error = \frac{4}{\left(1 + \frac{A_{dc}}{5}\right)} \times V_{FS} \tag{2.5}$$

Finite unity gain bandwidth(UGB)

The finite UGB results in dynamic error. The output voltage when the opamp's UGB $= \omega_u$ rad/s and max. output $= V_{FS}$ is

$$V_{out} = \left(1 - e^{-t\beta\omega_u}\right) \times V_{FS} \tag{2.6}$$

β is the feedback factor and is equal to 0.2 in this case. By taking settling time $t = \frac{1}{2f_s}$ where f_s is the sampling frequency, the error can be calculated as in Eq.(2.7)

$$Error = e^{-\frac{\beta\omega_u}{2f_s}} \times V_{FS} \tag{2.7}$$

The maximum tolerable error is $V_{LSB}/2$, where V_{LSB} is given by Eq.(2.8)

$$V_{LSB} = 2 \times \left(\frac{V_{FS}}{2^N}\right) \tag{2.8}$$

N is the number of bits to be extracted by the stages following this stage. The opamp specs obtained from the above analysis are summarised in Table 2.5

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Table 2.5: Opamp specifications.

Stage	A_{dc} (dB)	ω_u (MHz)
1	74	487
2	62	400
3	50	310
4	38	222
5	26	133

The UGB obtained from the above calculations are applicable only for small signal variations. However in the case of MDAC the output varies from V_{refp} to V_{refm}. Hence the slew rate of opamp and the initial charge on the load must also be considered. However small signal analysis is very useful in estimating the stability of opamp in closed loop. The design of opamps for each stage is discussed in the next chapter.

2.4   Bootstrap switch

As mentioned in earlier section, all input switches are bootstrapped. By boot-strapping the switches, there ON resistance is made independent of the input signal. One way to achieve this is by connecting a voltage source V_{dc} between the input and gate of the switch whenever ϕ_s is high. This would make the ON resistance as

$$R_{on} = \frac{1}{\mu_n C_{ox}(\frac{W}{L}).V_{dc}} \tag{2.9}$$

In practice a large capacitor (C_B) is used instead of the voltage source. The capacitor however needs to be charged frequently to compensate for leakages. This is done by charging the capacitor to V_{dd} when ϕ_s is low. The circuit diagram for the bootstrap signal generator is shown in Fig. 2.7
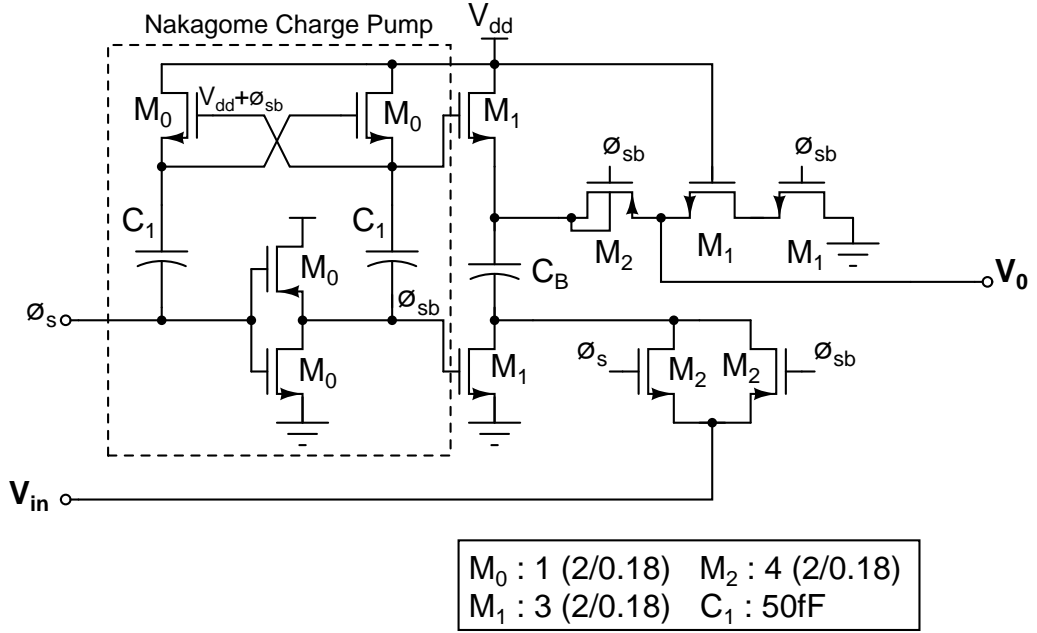
Figure 2.7: Circuit diagram of Bootstrap Signal Generator.

In this signal generator one clock $\phi_{sb} + V_{dd}$ is needed. To generate this signal, a Nakagome charge pump [2] is employed. The bulk of transistor M_2 is shorted to its source(instead of V_{dd}) as the source voltage exceeds V_{dd} and can reach a maximum of $V_{dd} + V_{refp}$. The output of this generator V_o is given to all the eight input switches in the capacitor array.

2.4.1 Charge Redistribution

The signal V_o-V_{in} is expected to alternate between 0 and V_{dd} (for zero input). The transient analysis plot (Fig. 2.8) shows that the signal alternates between 0 and 1.47 V. This is because of the gate capacitance of the switches. The charge from C_B is used up in charging the gate capacitance of the switch during ON phase of ϕ_s. The value of C_B is thus determined by the gate capacitance which is in turn dependent on the switch sizes. C_B is chosen as 1pF for stage 1 (large input switches) and 0.5pF for all subsequent stages.
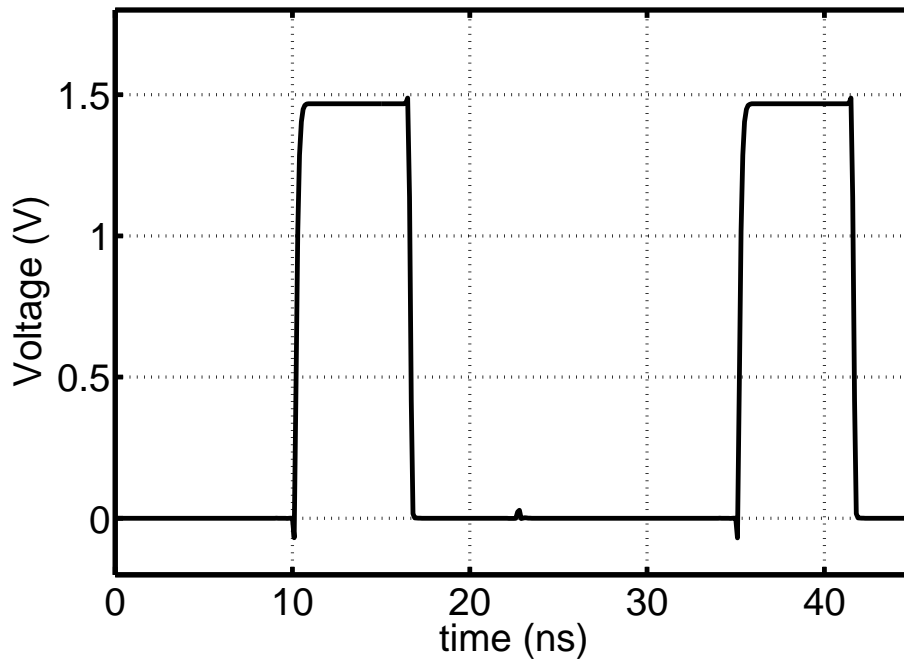
Figure 2.8: V$_o$-V$_{in}$ for the Stage 1 bootstrap signal Generator.

2.4.2 Harmonic Distortion

The sampling switch introduces harmonic distortion. It has to be carefully designed such that this THD introduced by the input switch is well below the quantization noise (73.6 dB below FS). The input is sampled by Stage 1 using a clock LC (LC is also the sampling clock for the sub ADC) with duty cycle 0.25. The THD at the output of the S/H for a full scale input at 19 MHz is -92 dB. The output PSD is shown in Fig. 2.9.

Figure 2.9: Output PSD for the S/H in MDAC. THD = -92 dB.

CHAPTER 3

Opamp Topology

A gain boosted folded cascode opamp is used in the MDAC stage. The gain boosted opamp consists of one main opamp (NMOS folded cascode) and four auxiliary opamps (two NMOS folded cascode and two PMOS folded cascode opamps). The main opamp along with auxiliary opamps gives very high dc gain. Hence the name gain boosted opamp.
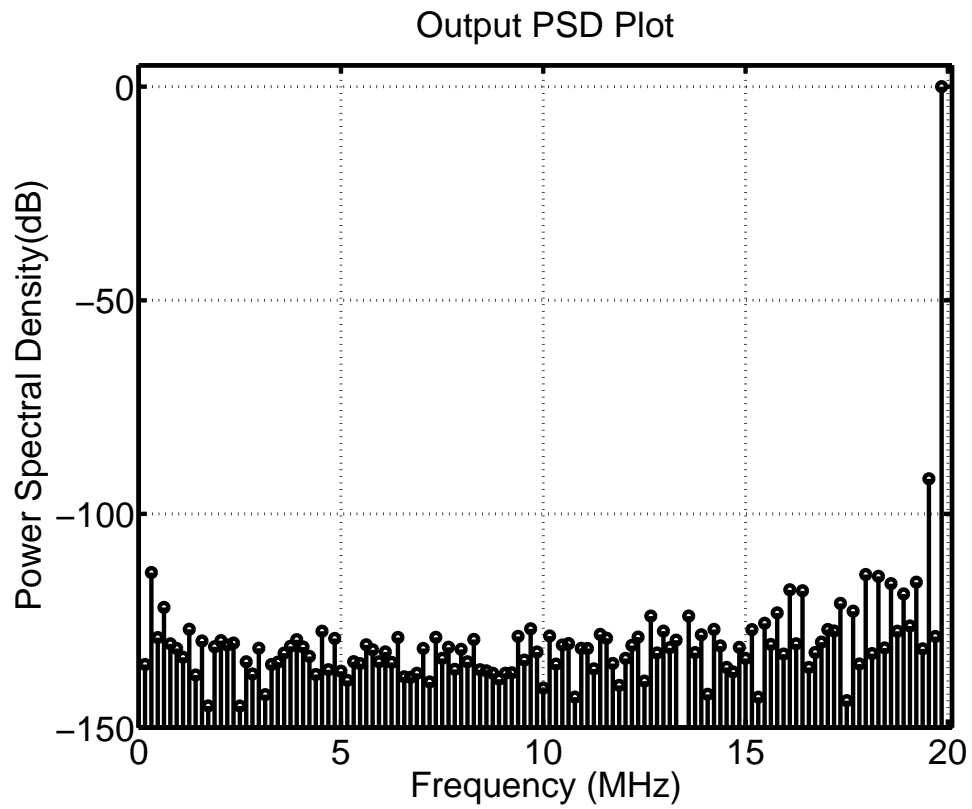
3.1 Gain Boosting

The principle of gain boosting has been explored in [3] . It is based on boosting the performance of the cascode used in the main opamp by using an amplifier (GBA). The effective looking in resistance (R_{cas}) of cascode is increased by a factor A_0, where A_0 is the gain of the GBA. The effective gain of the cascode shown in Fig. 3.1 given by Eq.(3.1).

$$Gain = (g_{m1}.r_{o1}).A_0.(g_{m2}.r_{o2}) \tag{3.1}$$
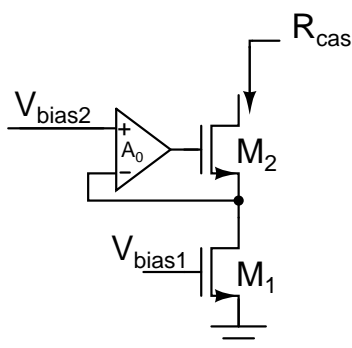

Figure 3.1: Principle of gain boosting.

3.2   Main opamp

For the main opamp, a folded cascode architecture has been used to increase the output swing. The load seen by each opamp is different as different values of capacitors are used for sampling in different stages. The load seen by the opamp in stage N is given by Eq.(3.2).

$$C_L = 0.8C_N + 4C_{N+1} \tag{3.2}$$

where C_N is the value of the feedback capacitor of Stage N.

As the load and accuracy requirements decrease for later stages, two different opamps have been designed. The first one, Opamp1, is for stage 1 and the second one, Opamp2, is for stages 2,3,4 and 5 . The opamps in later stages have been biased at lower currents to reduce power consumption. The circuit diagram for the main opamp is shown in Fig. 3.2. The biasing current details for different stages are provided in Table 3.1.

Table 3.1: Bias current details for Main Opamps.

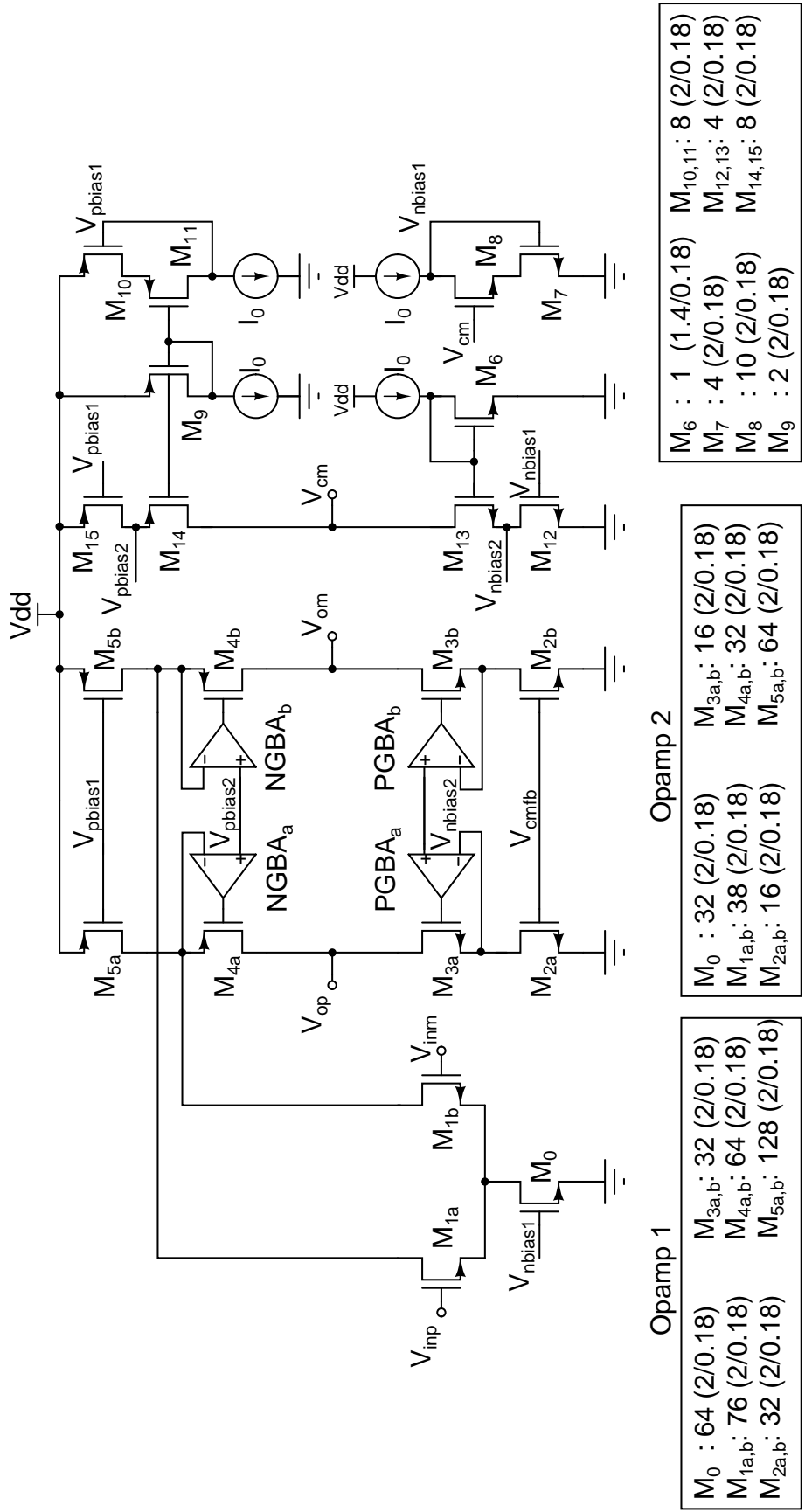| Stage	$I_0(\mu A)$
1	160
2	160
3	160
4	160
5	50

Figure 3.2: Circuit diagram for Main opamp.

3.3 Gain boosting amplifiers

3.3.1 NGBA

This opamp is a NMOS input folded cascode. This architecture is chosen because the input common mode for this opamp is close to V_{dd} i.e., $V_{dd} - 2\Delta V$. Similar to main opamp, two NGBAs (NGBA$_1$ and NGBA$_2$) have been designed. NGBA$_1$ is used in stage 1 and NGBA$_2$ is used in stages 2,3,4 and 5. The circuit diagram for the NGBA is shown in Fig. 3.3.
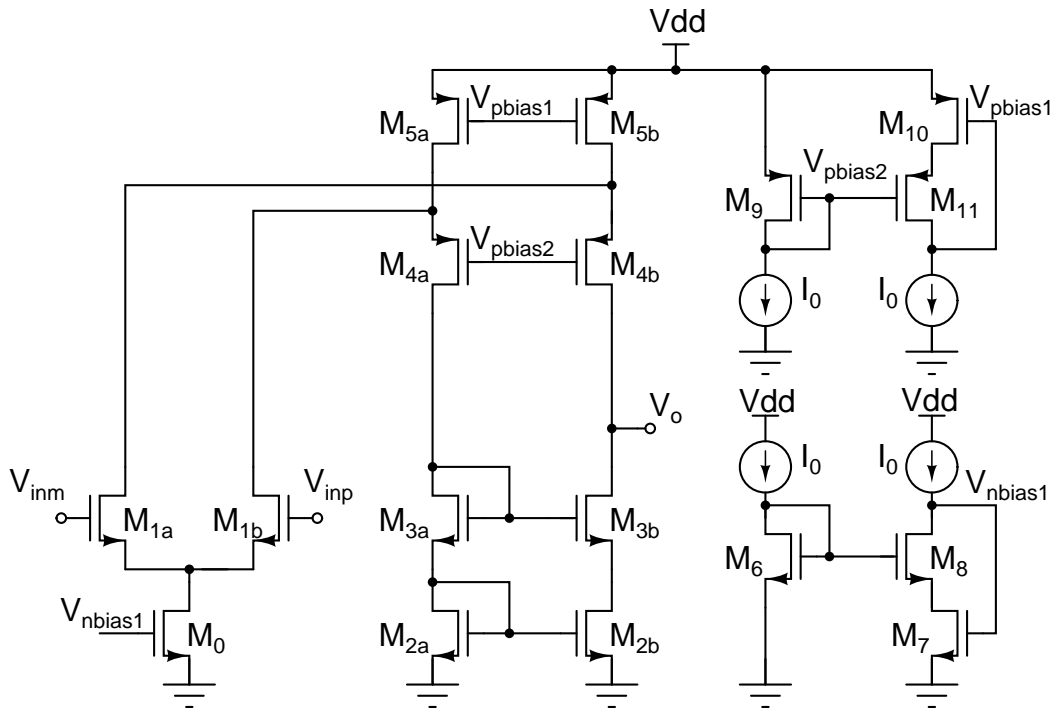
Details for NGBA$_1$

M_0 : 16 (2/1.08)	$M_{4a,b}$: 16 (2/0.54)	M_9 : 1 (1.5/0.54)
$M_{1a,b}$: 16 (2/0.36)	$M_{5a,b}$: 12 (2/0.54)	$M_{10,11}$: 4 (2/0.54)
$M_{2a,b}$: 8 (2/1.08)	M_6 : 1 (1/1.08)	I_0 = 40 uA
$M_{3a,b}$: 12 (2/0.54)	$M_{7,8}$: 4 (2/1.08)	

Details for NGBA$_2$

|		
M_0 : 8 (2/1.08)	$M_{4a,b}$: 8 (2/0.54)	M_9 : 1 (1.5/0.54)
$M_{1a,b}$: 8 (2/0.36)	$M_{5a,b}$: 6 (2/0.54)	$M_{10,11}$: 2 (2/0.54)
$M_{2a,b}$: 4 (2/1.08)	M_6 : 1 (1/1.08)	I_0 = 40 uA
$M_{3a,b}$: 6 (2/0.54)	$M_{7,8}$: 2 (2/1.08)	

Figure 3.3: Circuit diagram for NMOS Gain Boosting Amplifier (NGBA).

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3.3.2 PGBA

This opamp is a PMOS input folded cascode. This architecture is chosen because the input common mode for this opamp is close to ground i.e.,$2\Delta V$. Similar to NGBA, two PGBAs (PGBA$_1$ and PGBA$_2$) have been designed. PGBA$_1$ is used in stage 1 and PGBA$_2$ is used in stages 2,3,4 and 5. The circuit diagram for PGBA are shown in Fig. 3.4.
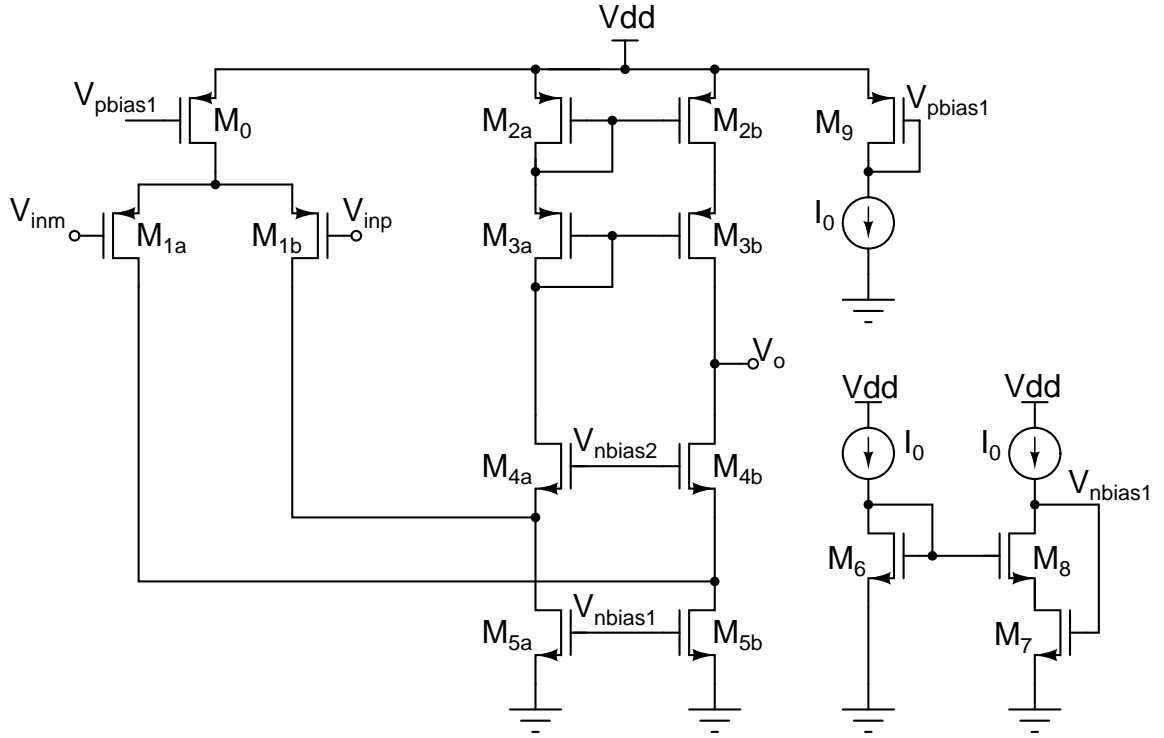
Details for PGBA$_1$

M$_0$: 16 (2/1.08)	M$_{4a,b}$: 8 (2/0.72)	M$_9$: 8 (2/1.44)
M$_{1a,b}$: 12 (2/0.36)	M$_{5a,b}$: 12 (2/1.44)	I$_0$ = 40 uA
M$_{2a,b}$: 12 (2/0.25)	M$_6$: 2 (1.5/0.75)	
M$_{3a,b}$: 12 (2/0.25)	M$_{7,8}$: 8 (2/1.44)	

Details for PGBA$_2$

M$_0$: 8 (2/1.08)	M$_{4a,b}$: 4 (2/0.72)	M$_9$: 8 (2/1.44)
M$_{1a,b}$: 6 (2/0.36)	M$_{5a,b}$: 6 (2/1.44)	I$_0$ = 40 uA
M$_{2a,b}$: 6 (2/0.25)	M$_6$: 2 (1.5/0.75)	
M$_{3a,b}$: 6 (2/0.25)	M$_{7,8}$: 4 (2/1.44)	

Figure 3.4: Circuit diagram for PMOS Gain Boosting Amplifier(PGBA).

3.4   Common mode feedback (CMFB) Circuit

A switched capacitor CMFB is used for the main opamp. This architecture is chosen to preserve the high DC gain of the opamp (If a resistive CMFB is used, the value of resistance needs to be very high). The value of the capacitance should be chosen appropriately as this capacitance loads the differential output. The circuit diagram for the CMFB circuit are shown in Fig. 3.5
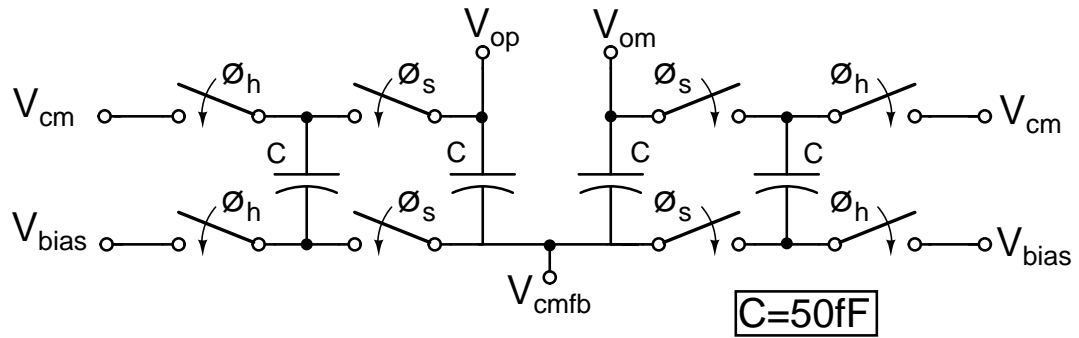

Figure 3.5: Switched Capacitor CMFB Circuit

3.5   Frequency response

The frequency response of the opamps can be seen in Table 3.2. The bode plot of loop gain for stage 1 amplifier is shown in Fig. 3.6. The disturbance in the phase plot near UGB is due to the improper pole zero cancellation.

Table 3.2: Open loop response of opamps

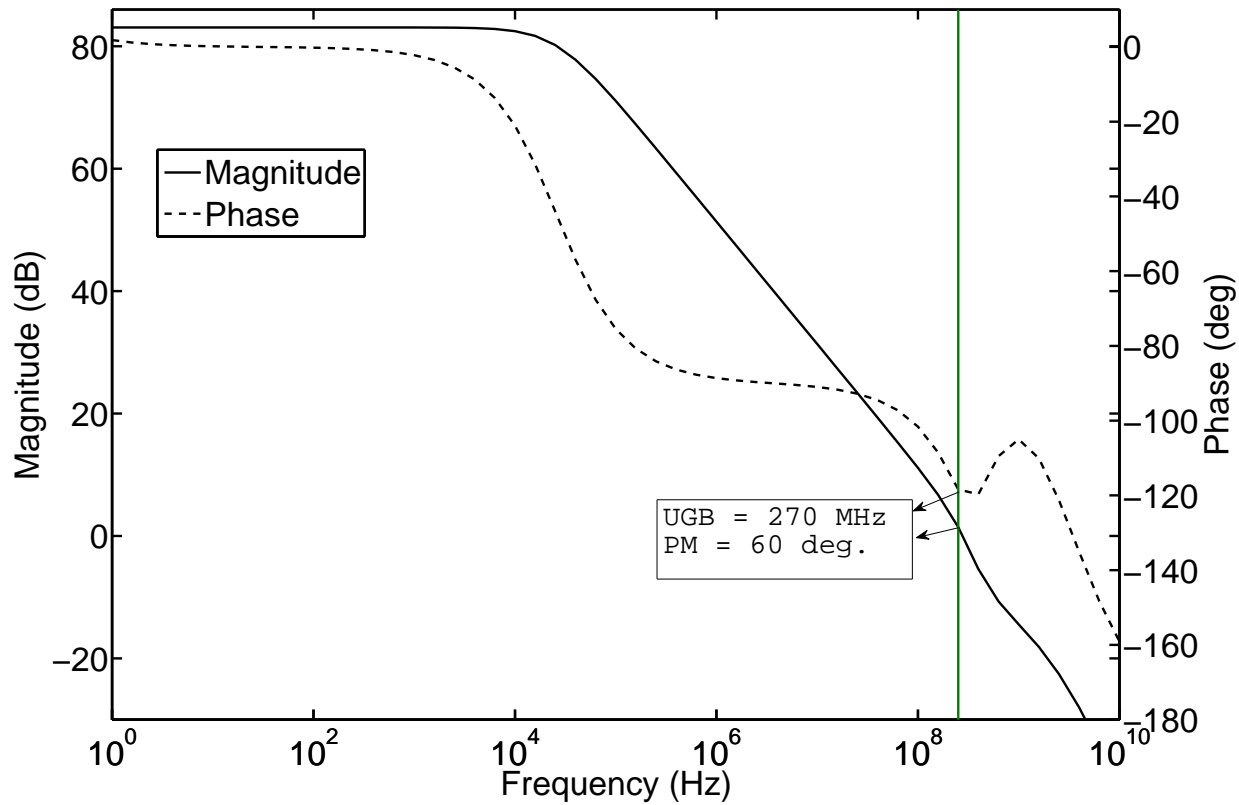| Stage	C_L (pF)	A_{dc}(dB)	ω_u(MHz)	ϕ_m(deg)
1	1.60	98	717	68
2	1.24	88	708	53
3	1.08	88	655	50
4	1.08	88	655	50
5	0.48	78	613	42

Figure 3.6: Bode plot - loop gain of stage 1 amplifier

3.6 Noise analysis

Opamp is a major contributor to noise in the amplifier. The noise calculations (PSS and PNOISE analysis in cadence) give the equivalent input referred noise (rms) for stage 1 = 75 μV. This gives an SNR of 86 dB for an input of 2 V peak-to-peak. This SNR is much higher than the SQNR (73.6 dB). Hence thermal noise will not result in the performance degradation of the ADC.

CHAPTER 4

MDAC Control Circuit

The MDAC control circuit generates the control signals to the MDAC depending on the input. It consists of a 2.5-bit flash ADC, a thermometer to binary converter and a DEM (for stage 1).

4.1 2.5-bit flash ADC

4.1.1 Resistive ladder

The 2.5-bit flash ADC studied in [4] consists of two resistive ladders and 6 comparators as shown in Fig. 4.1.
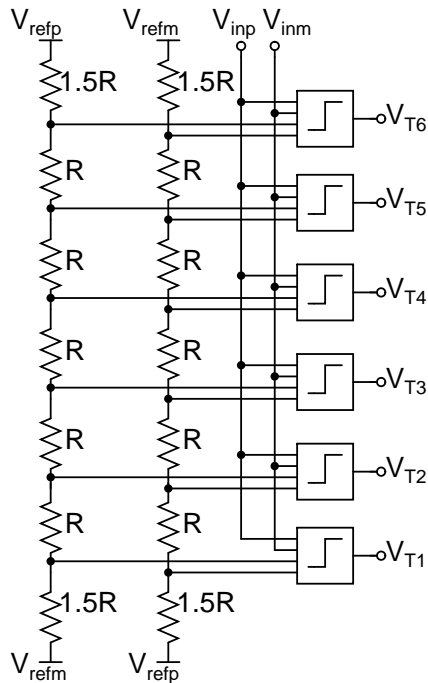
Figure 4.1: Circuit diagram of the resistive ladder used 2.5-bit flash ADC.

This ladder generates the required reference voltages for the comparators. All the nodes in the ladder have been provided with bypass capacitors (MOS capacitors) of value 2.5 pF.

4.1.2 Comparator

The comparator compares the input with the reference voltage and gives an output of logic 1 if input is greater than the reference and a logic 0 if input is smaller than the reference. The circuit diagram for comparator is shown in Fig. 4.2.
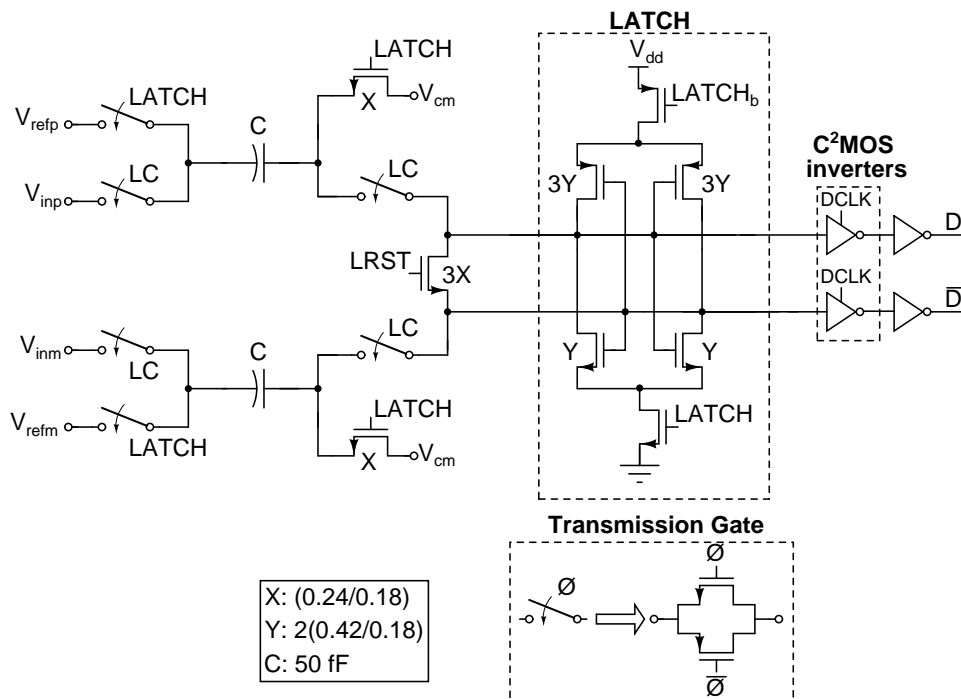
Figure 4.2: Comparator for flash ADC.

The comparator takes two reference voltages (V_{refp} and V_{refm}) from the resistive ladder and compares it with V_{inp} - V_{inm}. It has a back to back connected inverters which perform the function of a latch. The timing diagram for the multiple clocks used for the latch is shown in Fig. 4.3.
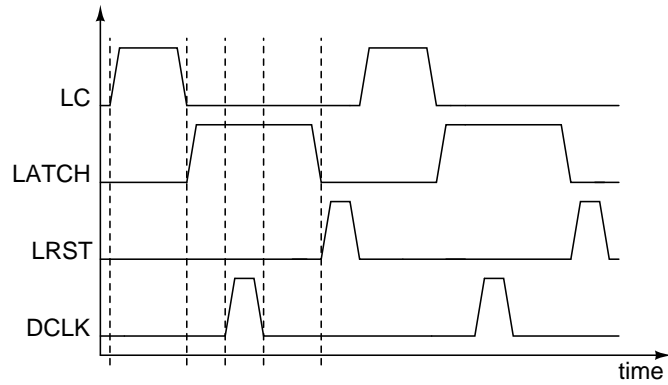
Figure 4.3: Timing diagram for the comparator.

LC phase

The coupling capacitor (C) is charged to the reference voltage during LATCH phase. During LC phase, the inputs are tracked by the comparator. The latch is disabled during this phase (by disconnecting supply and ground) making its input nodes float. As these nodes are floating, the voltage across the capacitors does not change and remains equal to V_{ref}. During the falling edge of LC, the input is sampled onto C. The inputs to latch is V_{in}-V_{ref}.

LATCH phase

During the rising edge of LATCH, the inputs to the latch is V_{in}-V_{ref}. Depending upon this value, the latch regenerates to the appropriate digital levels. The capacitor C is also charged to V_{ref} during this phase.

DCLK phase

The rising edge of DCLK comes after an appropriate time is given for the latch to regenerate. At the rising edge of DCLK, the output of latch is sampled by C^2MOS inverters. This output is to be buffered appropriately depending on the load.

LRST phase

During LRST, the outputs of latch are reset by shorting them. This improves regeneration time.

The comparator array generates six thermometer coded outputs (T_1-T_6). This are feed to a bubble correction circuit to remove any bubbles (errors).

4.1.3   Bubble correction circuit

The correction logic employed is majority three logic. The truth table for this logic is shown in Table 4.1. The circuit diagram for the bubble corrector is shown in Fig. 4.4.

Table 4.1: Truth table for majority three logic.

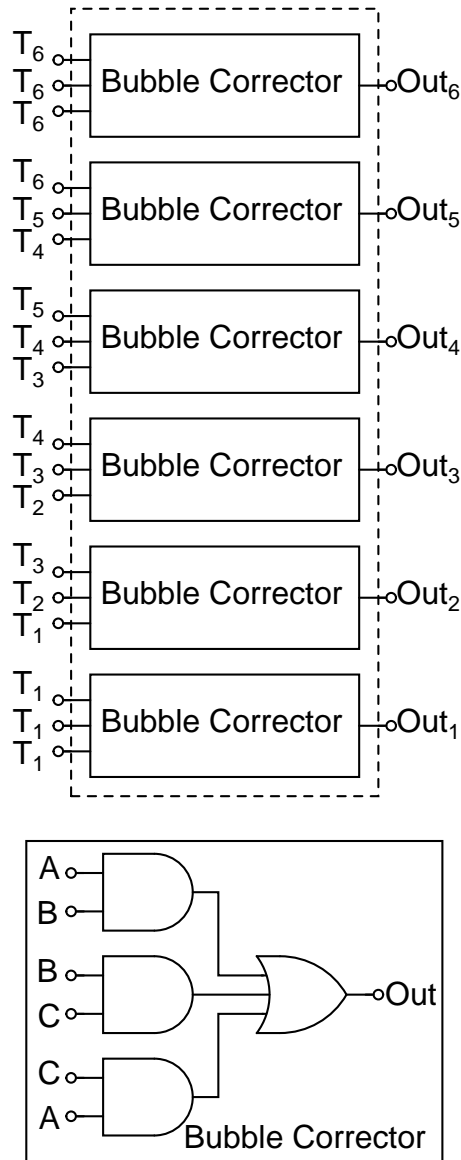| A	B	C	Output
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 4.4: Circuit Diagram for bubble correction circuit.

4.2 Thermometer to binary converter

Thermometer to binary conversion is achieved by the addition of the six thermometer code bits. This method doesn't rely on the $1 \rightarrow 0$ transition. The converter can be realized as shown in Fig. 4.5.
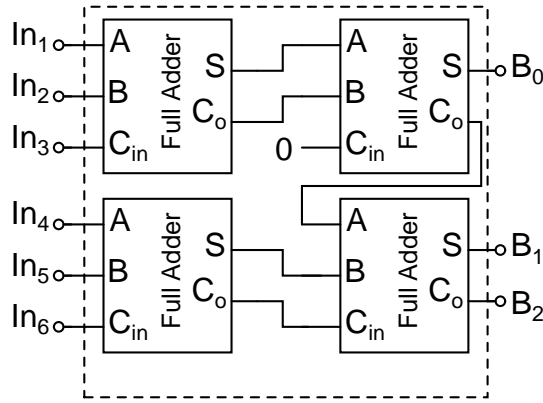
Figure 4.5: Implemention of thermometer to binary converter. Where B_0 is LSB and B_2 is the MSB.

4.3 Dynamic element matching

The Capacitor mismatch in stage 1 is a major limiting factor in the proper functioning of MDAC. To address this issue, DAC elements are randomised. In this case the DAC elements are capacitors. In order to randomise the mapping of a particular input to DAC elements, a DEM circuit is employed. As explained in [5] DEM improves SFDR. The DEM circuit takes inputs from the Flash ADC and gives output to the MDAC as shown in Fig. 4.6.
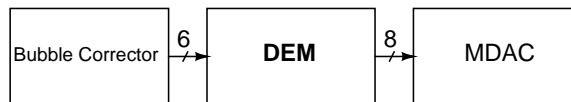

Figure 4.6: Placement of DEM circuit.

4.3.1 Butterfly scrambler

To perform shuffling of the lines, a 8 line butterfly scrambler is used. The butterfly scramblers consists of an array of switches which shuffle the input based on the control signals they receive from the random sequence generator. The circuit diagram for the butterfly scrambler is as shown in Fig. 4.7. The control signals
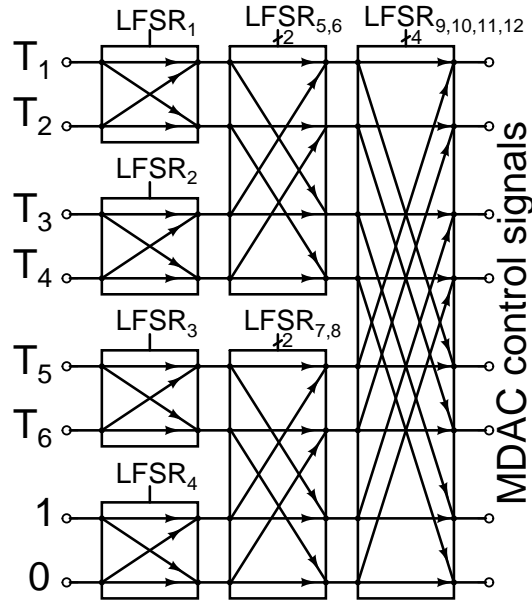
Figure 4.7: Circuit diagram of 8 line butterfly scrambler. $LFSR_{1-12}$ are the control signals.
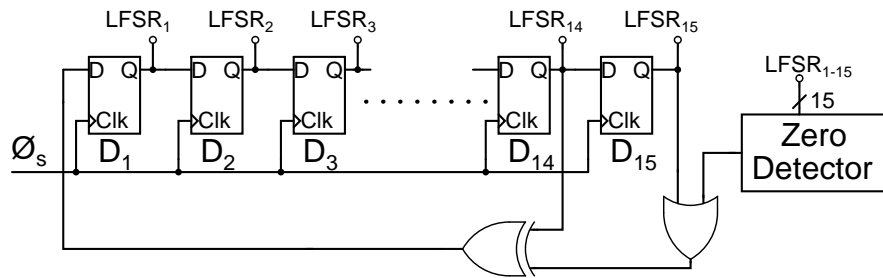

Figure 4.8: Circuit diagram for 15 bits LFSR, ϕ_s is the sampling clock of the MDAC.

for the scrambler are generates by a Linear feedback shift register (LFSR).

4.3.2 Linear feedback shift register (LFSR)

The LFSR [6] is designed with a period of $2^{15} - 1$. It consists of 15 registers(D flip flops) connected in a feedback with XOR gate as shown in Fig. 4.8. The LFSR goes into a locked state if all the bits $LFSR_{1-15}$ are logic 0. To avoid such a state, an all zero detector is used load a logic 1 if the LFSR goes into the locked state.

CHAPTER 5

Digital Error Correction and Timing Analysis

5.1 Digital error correction

The bits corresponding to an input are processed at different time instants by different stages. This bits must now be delayed appropriately before addition. To perform the task of delaying, a flip flop array is used. The delay and number of flip flops used for each stage are given in Table 5.1. Data is synchronised to ϕ_s of stage 1.

Table 5.1: Details of number of clock cycle delay and number of flip flops used (to achieve this delay) in each stage.

Stage	Delay	Flip Flops
1	3	3
2	3	3
3	2	2
4	2	2
5	1	1
6	1	1

The delayed data should be appropriately added from the right side as shown in Fig. 5.1.
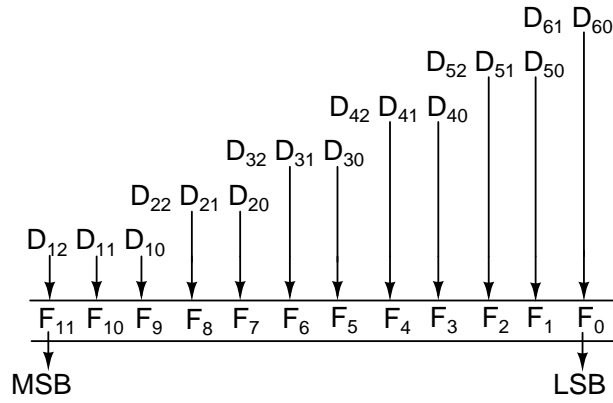
Figure 5.1: DEC algorithm, D_{xy} is the output of stage x. y=0 is the LSB.

5.2 Timing Analysis

For the proper functioning of MDAC, the DAC output should be available before the amplification phase starts i.e., the voltage to be subtracted from input should be available before performing subtraction. The DAC output depends on the input it gets from the sub-ADC. As seen in earlier chapter, the latch used in the flash ADC takes some time to regenerate. For this reason the rising edge of LATCH clock is placed $0.25T_s$ (Fig. 5.3) before the amplification phase starts, thus giving the latch enough time to regenerate.

5.2.1 Timing - Stage 1

To avoid any errors in the DAC output, the value sampled by the flash ADC should be same as the value sampled by the MDAC. To achieve this the sampling phase (ϕ_s) of stage 1 is made identical to the LC phase as shown in Fig. 5.2
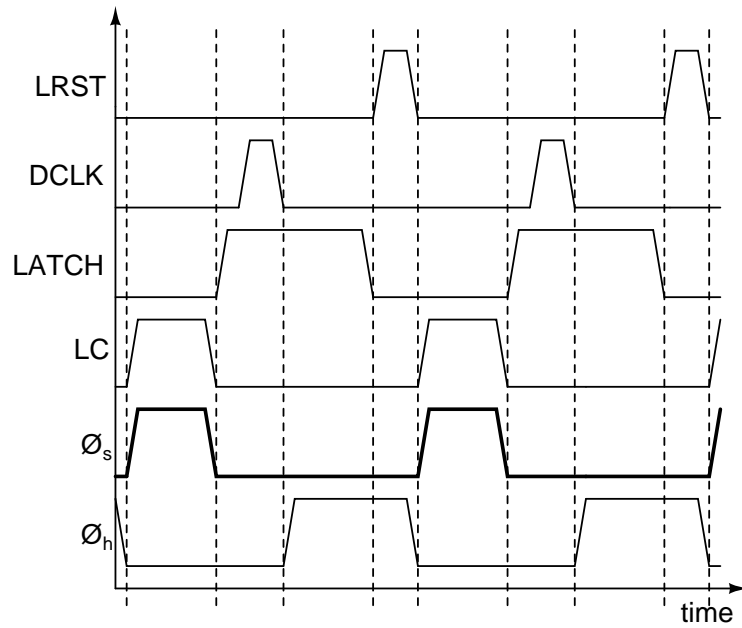
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Figure 5.2: Synchronisation of flash ADC clocks and MDAC clocks for stage 1.

5.2.2 Timing - Stages 2, 3, 4, 5

In this stages ϕ_s is the ϕ_h of previous stage. To maximise the time available for amplification (reduces the bandwidth requirements of the opamps), ϕ_s is stretched in time as shown in Fig. 5.3
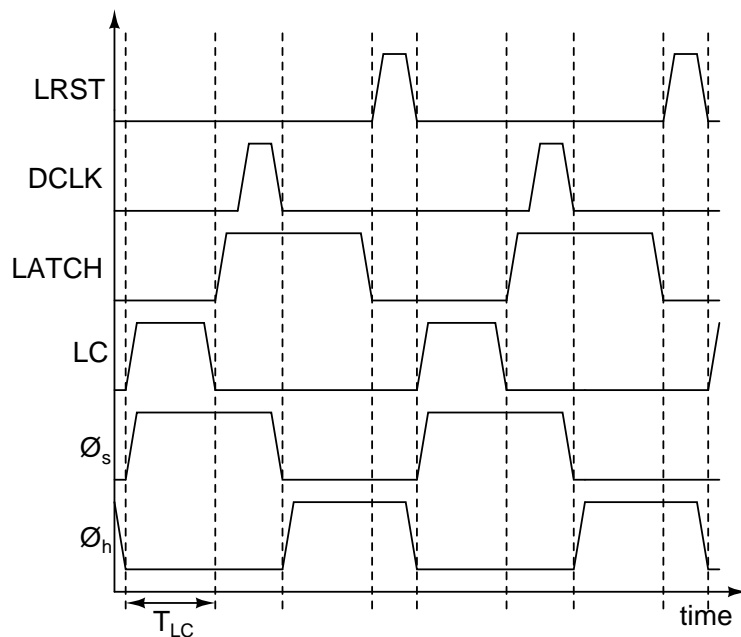
Figure 5.3: Synchronisation of flash ADC clocks and MDAC clocks for stages 2, 3, 4, 5.

This stretching of ϕ_s results in a mismatch between the value sampled by flash ADC (falling edge of LC) and MDAC (falling edge of ϕ_s). This mismatch error is shown in Fig. 5.4. This error translates into a transition point error in the flash ADC. As discussed in previous section, an error of 0.5 LSB in the transition points of sub-ADC is acceptable. For this reason the MDAC output should reach at least $V_f - 0.5LSB$ in time T_{LC}.
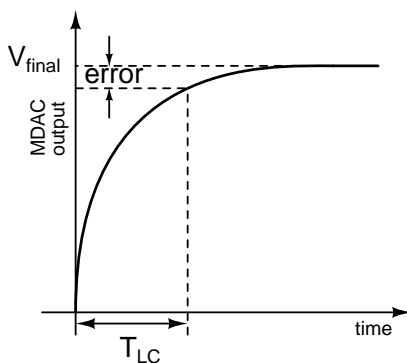

Figure 5.4: Mismatch between values sampled by flash ADC clocks and MDAC clocks for stage 2, 3, 4, 5.

The residue generated by stage N is the input for stage N+1. In order to achieve this successive stages should be out of phase by 180 deg. The clock details for all the stages are shown in Table 5.2. The stage 6 is only a flash ADC and it doesn't have an amplification phase.

Table 5.2: MDAC Clock details for all stages.

Stage	ϕ_h	ϕ_s
1	LC	ϕ_2
2	ϕ_2	ϕ_1
3	ϕ_1	ϕ_2
4	ϕ_2	ϕ_1
5	ϕ_1	ϕ_2
6	-	ϕ_1

5.3   Clock generation

5.3.1   MDAC clocks

The sampling clock and amplification clock should be non overlapping. This is achieved by a non-overlapping clock generator shown in Fig. 5.5. The NAND gate delay (t_d) is adjusted by appropriate (even) number of inverters. The clocks should be appropriately buffered before giving to MDACs.
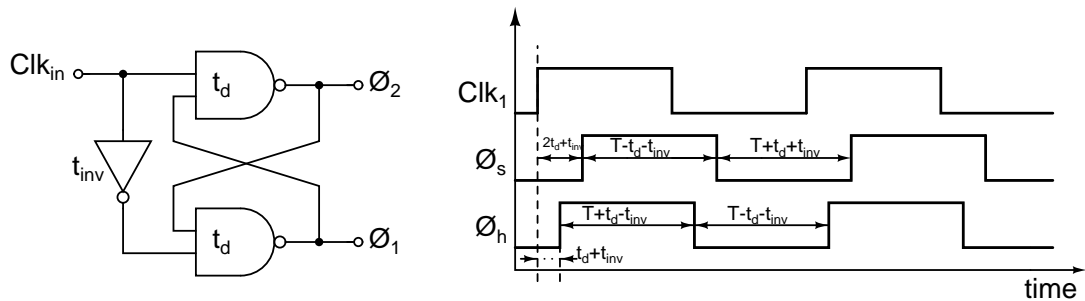

Figure 5.5: Circuit diagram for non-overlapping clock generator for MDAC clocks.

5.3.2 Latch clocks

The latch clocks are also generated in a fashion similar to that of MDAC clocks as shown in Fig. 5.6. Two such generators are needed as we need two sets of latch clocks (one set for odd numbered stages other set for even numbered Stages).
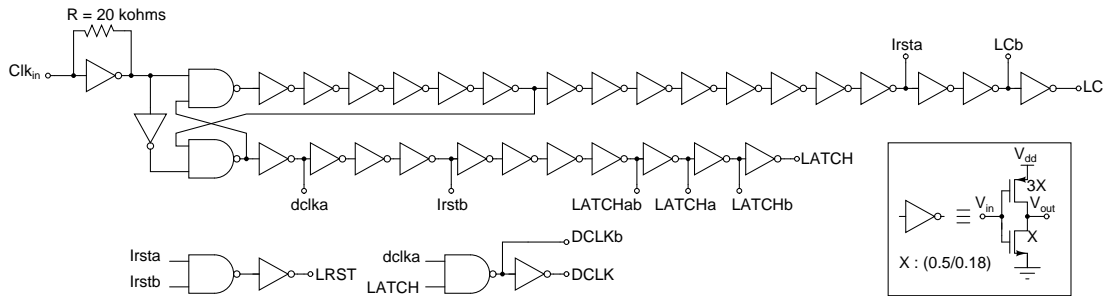

Figure 5.6: Circuit diagram for non-overlapping clock generator for latch clocks.

5.3.3 Clock divider

The input clocks for the above generators are generated from a master clock at 80 MHz using a clock divider as shown in Fig. 5.7. Clk_1 is MDAC clock generator input, Clk_2 is odd latch clock generator input and Clk_3 is even latch clock generator input. The clocks should be buffered by the same buffer used for MDAC clocks.
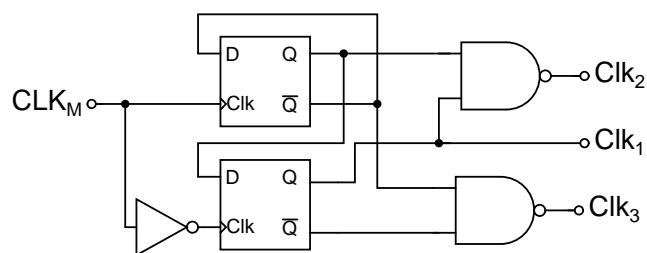

Figure 5.7: Circuit diagram for master clock divider.

5.3.4 Clock buffer

The effective widths of switches to be driven by the clocks is in the order of hundreds of microns. To provide this driving capability, all clocks are buffered by using a clock buffer as shown in Fig. 5.8.
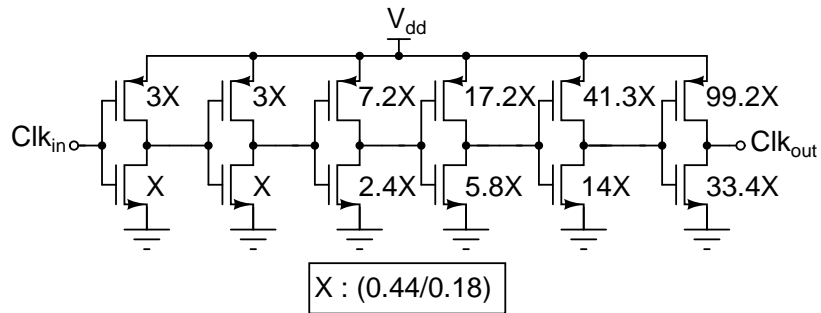

Figure 5.8: Circuit diagram for clock buffer.

CHAPTER 6

Layout and simulation results

6.1 Layout

The designed pipelined ADC was laid out using CADENCE virtuoso tool. The chip has been designed using a 33 pin QFN package. The converter occupies an active area of 1.25 mm × 1 mm.

The layout of capacitors is very critical. The capacitors are laid out in a common centroid fashion as shown in Fig. 6.1. This arrangement nullifies the mismatches due to first order chip gradients and reduces the mismatches due to higher order gradients.
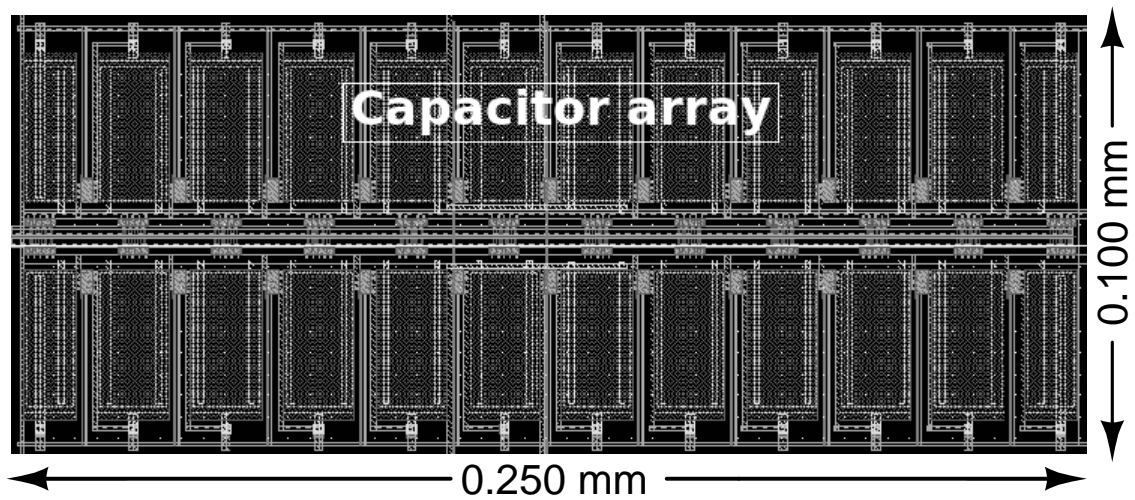

Figure 6.1: Layout of stage 1 capacitor array.

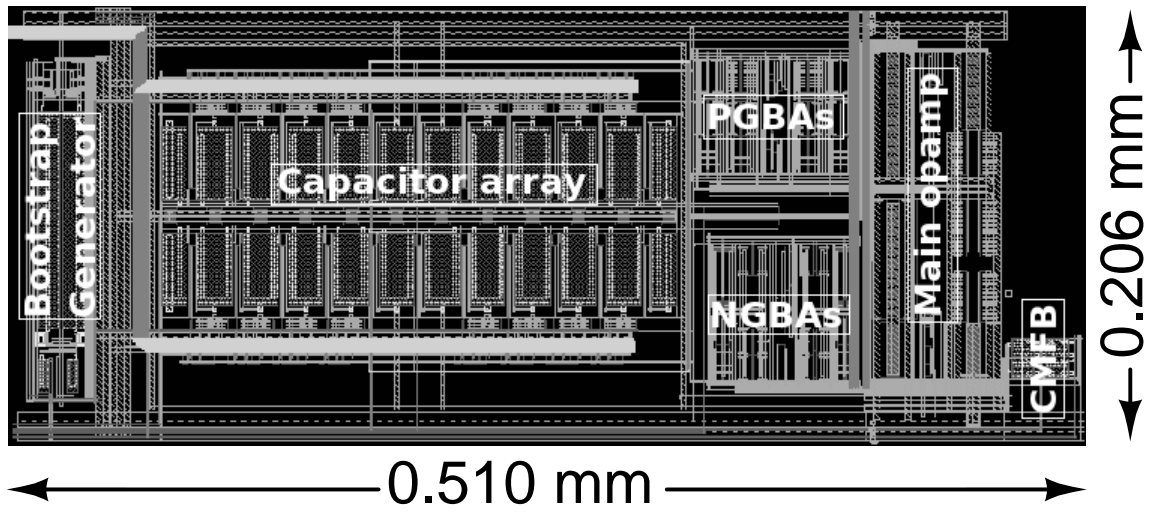The layout of MDAC and flash ADC are shown in Fig. 6.2 and Fig. 6.3 respectively.

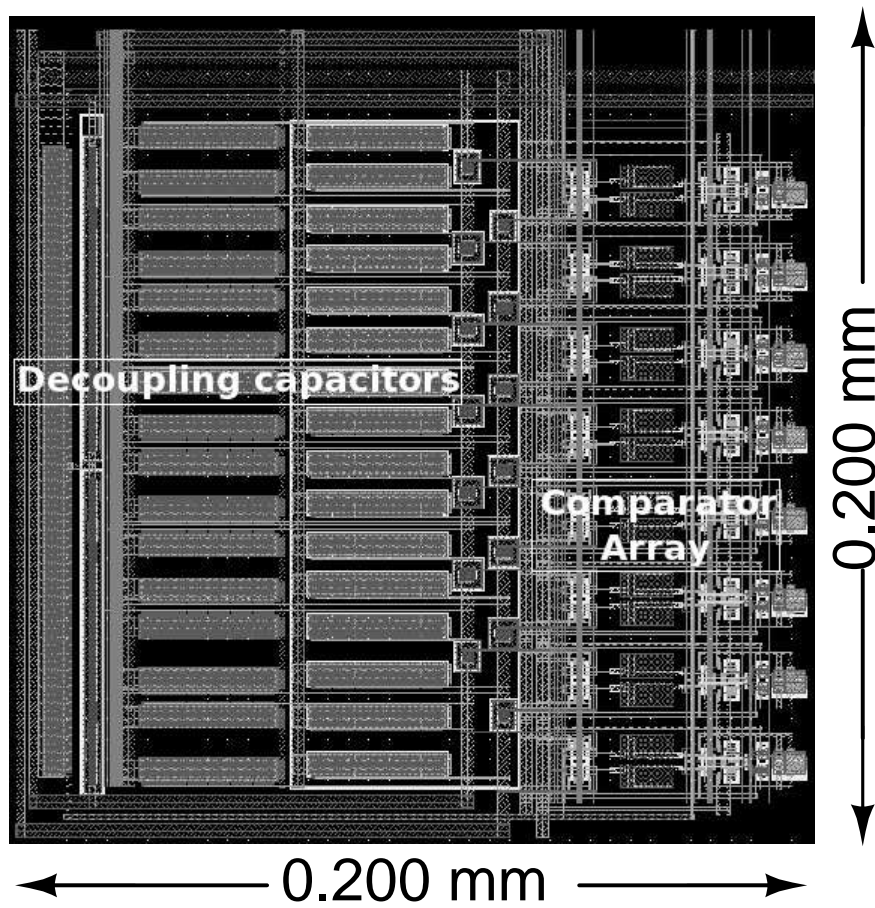Figure 6.2: Layout of stage 1 MDAC.

Figure 6.3: Layout of flash ADC.

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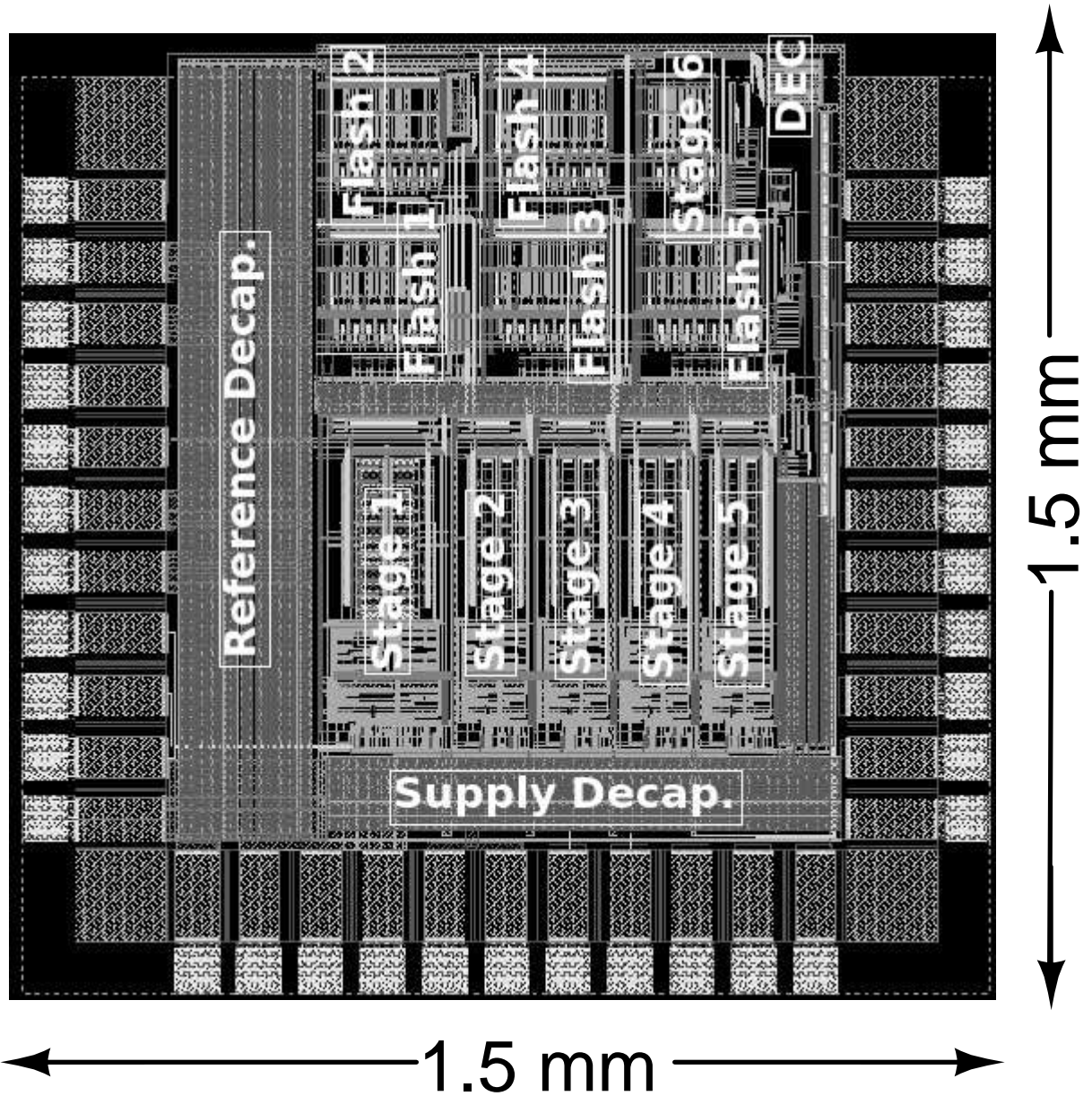The layout for the entire ADC is shown in Fig. 6.4.

Figure 6.4: Layout of 12-bit ADC along with I/O pads.

6.2   Simulation results

The entire pipelined converter was simulated with the extracted view after layout. An input of full scale amplitude at 19 MHz was used for simulations. The

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simulation results for various process corners are shown in Table 6.1. The output power spectral density plot is shown in Fig. 6.5. This results show that the ADC has a resolution of 12-bit at sampling rate of 40 MSPS.

Table 6.1: Simulation results for various process corners.

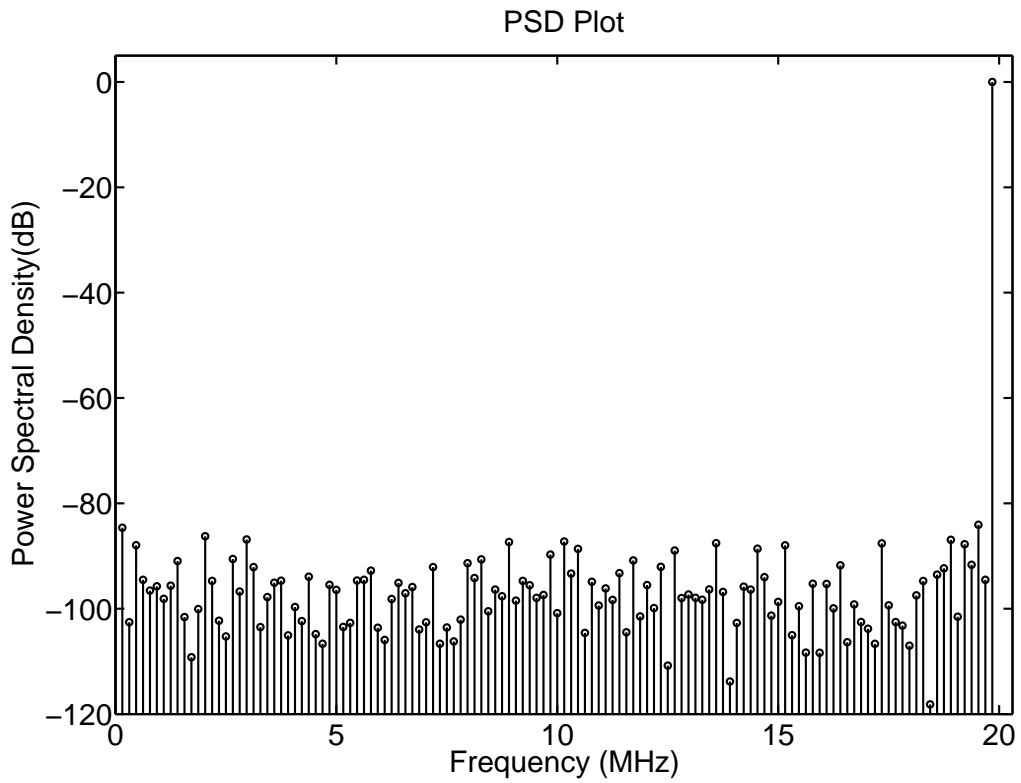| Corner	Temp.(C)	SNDR (dB)
ss	0	73.6
ss	70	72.9
tt	27	73.2
ff	0	74.0
ff	70	73.4

Figure 6.5: ADC output power spectral density plot for input at $127/256$ F_s. SNDR = 73.2 dB.

6.3 Conclusion

A 6 stage 12-bit pipelined ADC with 40 MSPS sampling rate has been designed in 180 nm technology. The techniques of gain boosting and DEM have been used to reduce gain error and harmonic distortion. The total power consumption in the ADC is 50 mW.

6.4 Future work

The power consumption can be reduced by employing opamp sharing [7]. By employing digital calibration techniques, the precision gain requirements in the starting stages can be reduced.

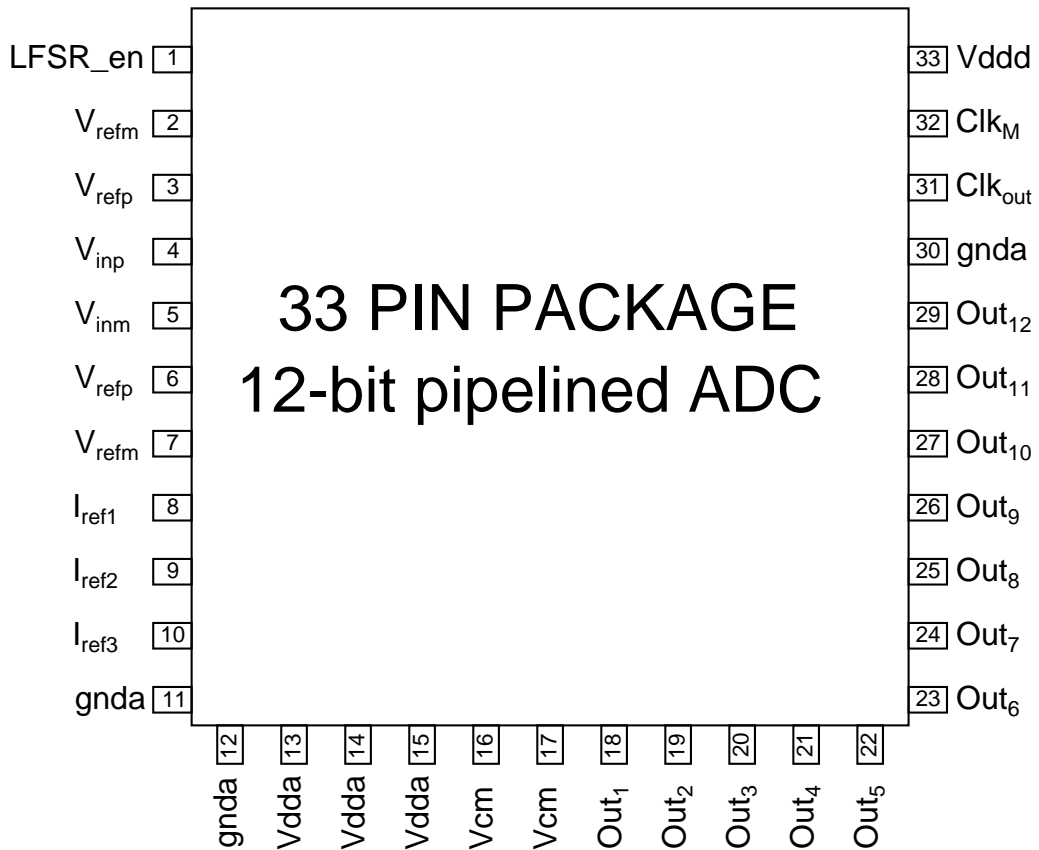# APPENDIX A

Pin details of the pipelined ADC

Figure A.1: Pin diagram of the pipelined ADC.

Table A.1: Functionality of each pin

Pin	Name	Functionality)
1	$LFSR\_en$	Enable bit for the LFSR
2, 7	V_{refm}	Low reference voltage (0.4 V)
3, 6	V_{refp}	High reference voltage (1.4 V)
4, 5	V_{inp}, V_{inm}	Differential inputs
5	V_{inm}	Negative differential input
8	I_{ref1}	Biasing current for Stage 1 main opamp
9	I_{ref2}	Biasing current for Stage 2, 3, 4, 5 main opamps
10	I_{ref3}	Biasing current for gain boosting amplifiers
11, 12, 30	$gnda$	Ground
13, 14, 15	$Vdda$	Analog supply
16, 17	Vcm	Common mode voltage (0.9 V)
18 - 29	Out_1 - Out_{12}	Final output bits. MSB - Out_{12}, LSB - Out_1
31	Clk_{out}	Output synchronizing clock. Data to be sampled at the falling edge of clock
32	Clk_M	Input clock at 80 MHz
33	$Vddd$	Digital supply

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