Continuous-Time $\Delta\Sigma$ Modulated ADCs with a VCO based quantizer

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **Continuous-Time $\Delta\Sigma$ Modulated ADCs with a VCO based quantizer**, submitted by **Chinmoy Venkatesh Mandayam Nayaka**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Analog-to-Digital Conversion; CT-DSM; VCO quantizer.

We will study the design of an analog-to-digital converter (ADC) which uses a voltage controlled oscillator (VCO) to discretize the input signal, instead of a set of comparators, to reduce power consumption. We shall also study non-idealities in such a quantizer, such as distortion and delay.

We shall study Continuous-Time $\Delta\Sigma$ modulator (CT-DSM) loops which use such a quantizer, to increase the resolution of this converter. We shall also see some other aspects of CT-DSM design, such as DAC design. Simulation outputs are provided to illustrate these results.

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ABBREVIATIONS

ADC	Analog-to-Digital Converter
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
SQNR	Signal to Quantization Noise Ratio
DAC	Digital-to-Analog Converter
DT	Discrete-Time
CT	Continuous-Time
DSM	$\Delta\Sigma$ Modulator
CT-DSM	Continuous-Time $\Delta\Sigma$ Modulator
DT-DSM	Discrete-Time $\Delta\Sigma$ Modulator
NTF	Noise Transfer Function
STF	Signal Transfer Function
LTF	Loop Transfer Function
QTF	Quantizer Transfer Function
OSR	Oversampling Ratio
OBG	Out-of-Band Gain
VCO	Voltage-Controlled Oscillator
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
HPF	High-pass Filter
BHPF	Butterworth High-pass Filter
UMC	United Microelectronics Corporation
RZ	Return-to Zero
NRZ	Non-Return-to Zero

NOTATION

α	Delay between the register clock and the sampler clock
ζ	Ratio of tuning transistor width to inverter transistor width
$L(z)$	External DT loop transfer function
$L_{eff}(z)$	Effective DT loop transfer function
$L_c(s)$	External CT loop transfer function
ξ	Location of negatice real zero

CHAPTER 1

Introduction and Motivation

Many applications where electronic systems are used can be categorized as information processing systems. They take some real world data as input in some and return an output again to the real world, possibly in some other form. Usually the the input data is processed in some manner to extract some meaning or use. Often, this processing is highly abstract or mathematical and is most easily performed by some form of digital logic based computation. Thus, there arises a need to convert the real world data in to a suitable form. Since real world data is almost always analog, this creates a need for analog-to-digital (A/D) conversion.

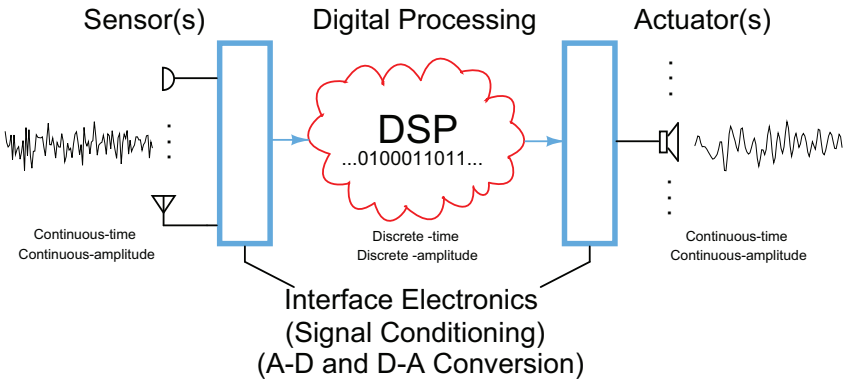

Figure 1.1: A generic electronic system (Pavan and Krishnapura, 2008)

Current digital processor technologies have advanced to the point that some applications which earlier required specialized circuitry, such as wireless receivers, can now be performed easily and quickly by just running the appropriate software. This approach is also much more flexible and updating such a system to meet newer specifications is much more economical. However, to support the high data rates that modern systems have with a low error rate, we require A/ D converters (ADCs) with both high bandwidth and high resolution. At the same time, since mobility is a desirable feature for many devices, we would like our ADCs to have low power consumption to increase battery life.

Unfortunately, due to thermodynamics, achieving all three simultaneously is not possible, so we have to do the best we can to come close to this ideal. Using clever circuit design and signal processing techniques, we can improve the trade-offs between these design goals to suit our requirements.

1.1 $\Delta\Sigma$ -Modulators

One popular way of creating high resolution, low power ADCs, which have a reasonably high bandwidth is to use $\Delta\Sigma$ -modulated ADCs. According to the sampling theorem, if we sample a band-limited signal at a frequency which is twice the bandwidth, it is sufficient to ensure that we can reconstruct the signal without any aliasing. If we sample at a higher frequency we have redundancy from the perspective of the frequency domain, which we can try to exploit to improve the resolution. This becomes more apparent if we approximate the quantization error to be a signal-independent white noise source. The quantization noise power σ_q^2 in every sample is independent of the sampling frequency and only dependent on the resolution of the quantizer as it is given by the expression $\frac{V_{lsb}^2}{12}$, where V_{lsb} is the voltage corresponding to one quantization level. By just oversampling, filtering the digital output data, and then decimating, we can obtain an improvement in the SQNR, to better level than the quantizer's initial level. Increasing the sampling frequency directly improves the SQNR, since the power of the quantization noise is spread over a wider frequency range, so that the total noise power in the desired signal band is reduced correspondingly. This is illustrated in Figure 1.2 (Singh, 2010).

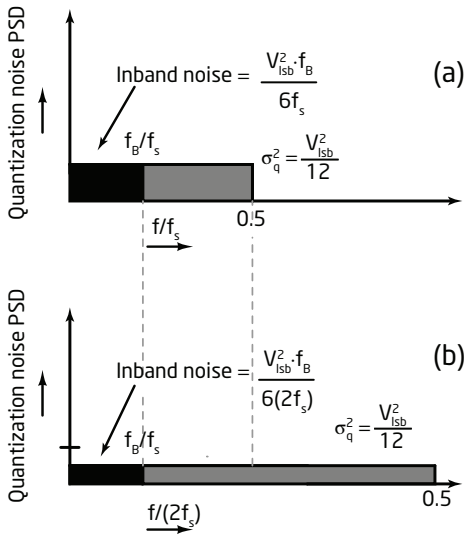

Figure 1.2: Oversampling to reduce inband quantization noise (Singh, 2010)

This method gives a gain of only 3 dB in the SQNR for doubling the *oversampling ratio* (OSR), which is the ratio of the actual sampling frequency to the minimum required sampling frequency for the input as obtained from the sampling theorem. Using the quantizer with analog feedback, we can shape the quantization noise spectrum so that at low frequencies, the noise power is reduced, but

is increased at higher frequencies. Since we will digitally filter away the higher frequencies, the reduction of low frequency noise is quite desirable. Hence we can obtain much higher improvements in SQNR by combining oversampling and analog feedback. This is the method of $\Delta\Sigma$ modulation. Figure 1.3 shows the model of a general $\Delta\Sigma$ modulator and Figure 1.4 shows how noise shaping reduces the inband noise.

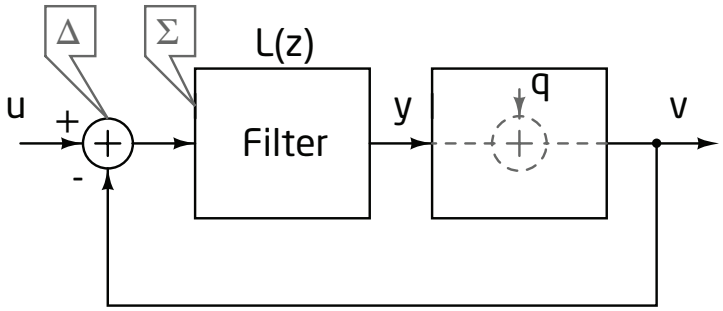

Figure 1.3: A general$\Delta\Sigma$ modulator schematic (Singh, 2010)

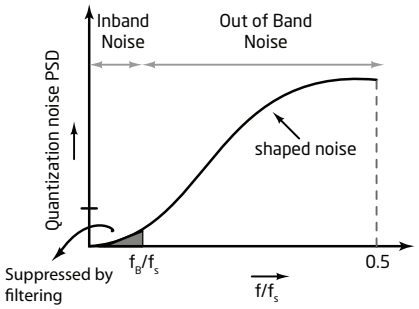

Figure 1.4: Noise-shaping to further reduce inband quantization noise (Singh, 2010)

Since the digital output of the quantizer is sampled data, The feedback and noise shaping is nominally done by a discrete-time filter. The filter in the feedback path is called the loop-filter and its transfer function, called the *loop transfer function* (LTF) is denoted by $L(z)$. The transfer function from the imaginary source for the quantization error, q to the output is called the *noise transfer function* (NTF) and the transfer function from the input u to the ADC to the output is called the *signal transfer function* (STF). We have the following relations among these transfer functions:

$$STF(z) = \frac{V(z)}{U(z)} = \frac{L(z)}{1 + L(z)} \tag{1.1}$$

and

$$NTF\left(z\right)=\frac{V(z)}{Q(z)}=\frac{1}{1+L(z)} \tag{1.2}$$

For good quantization noise shaping, $L\left(z\right)$ should be a low-pass transfer function with a very high low frequency gain. This will also ensure that the STF is close to unity in the desired frequency band.

Discrete-time filters usually involve switched-capacitor circuit based implementations. However, these tend to consume a lot of power. Instead, a continuous-time filter $L_c\left(s\right)$, whose output has the same value at the sampling instant as the discrete-time filter $L\left(z\right)$, can be used. Such an architecture is called a CT-$\Delta\Sigma$ modulator (CT-DSM). These circuits have very low power consumption. To make a CT-DSM, we also have to move the sampling from before the modulator loop input to just before the quantizer. The feedback path also has a DAC, which is also needed in case of the discrete-time $\Delta\Sigma$ modulator (DT-DSM). However, the DAC waveform characteristics over the entire sample period now have an important effect, rather than just at the sampling instant. Thus, a block diagram of a CT-DSM would be as in Figure 1.5. This gives an additional advantage because $L_c\left(s\right)$ which would also be a low-pass filter, would act like an anti-aliasing filter itself, further saving area and power.

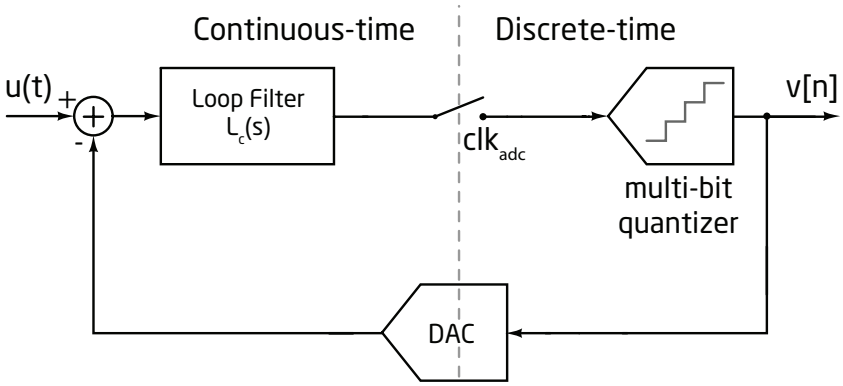

Figure 1.5: Schematic of a continuous-time $\Delta\Sigma$ modulator

Normally, we would like the noise performance of any system to be limited by thermal noise, so that we are consuming the minimum possible power. Because of the high gain of the loop-filter, we would expect the noise at its input to be the most significant contributor to the noise performance.Therefore, we would also like the power of the signal sources that feed to this point to make up the bulk of the power consumption, so that we are having the best performance for the power consumed.

However, it was found that for a high speed CT-DSM (Singh, 2010), the quantizer was consuming most of the power , even though the corresponding noise contributions were not so important. Thus there is a need to reduce the quantizer power.

The use of voltage-controlled oscillators as quantizers in CT-DSMs has been proposed as a way to achieve this. Thus, we will explore these quantizers in the following chapters

1.2 Overview of the thesis

The rest of the thesis is organized as follows.

Chapter 2 provides an analysis of the VCO quantizer and some methods to ease its simulation.

Chapter 3 includes a rigorous analysis of the integration of a feedback loop with the VCO quantizer to create the $\Delta\Sigma$ modulator.

Chapter 4 includes simulation results for various blocks in the VCO quantizer based CT-$\Delta\Sigma$ modulator.

Chapter 5 concludes the thesis and discusses some future extensions of this work.

CHAPTER 2

VCO-based quantizers

2.1 Introduction

The ultimate aim of any A/D converter is the conversion from a real-valued physical input quantity, such as voltage, current, temperature, etc., to a representation by a rational number. Internally, the conversion from such a dimensional quantity to a dimensionless number is the fundamental step. Most current A/D converters, which measure voltages, are based on directly measuring the input voltages by means of comparison with a fixed reference value. The data obtained from this measurement may be directly used (as in a *flash* ADCs), or may be reused to improve further measurements (as in *pipelined, successive approximation* and *oversampled* ADCs). But fundamentally they are all based on directly comparing voltages or currents directly dependent on these voltages.

There are other types of A/D converters which are more indirect, comparing quantities other than the traditional electrical variables. Some of these convert an input to a *time* quantity which can then be measured by a clock (which is an oscillator). Examples of such A/D converters are *single-slope* and *dual-slope* converters, still used in some low speed applications. However one major disadvantage of such converters is that they are not suited for uniform sampling, as the time required for each conversion is itself dependent on the input.

We can, however turn the time-to-digital based converter on it head so that while we keep the conversion time period constant, we instead change the frequency of the clock based on the input. Such a clock, whose time-period (and hence frequency) is dependent on some voltage are called *voltage-controlled oscillators* (VCOs). A/D converters based on substituting VCOs in place of comparator based quantizers have certain advantages which we shall elucidate in the following sections.

2.2 Operation of VCO-based quantizers

VCO-based quantizers use the idea of counting the number of cycles of oscillation that take place in a sampling period of an A/D converter. Since the number of

full cycles is just the greatest integer multiple of 2πin the total phase traversed by the oscillator in one cycle, we can say that a VCO quantizer is a phase-to digital converter. To do this, we need is a fast counter, whose clock pulse is given by the VCO and whose count value is reset every sampling period. Figure 2.1 from Straayer and Perrott (2008) illustrates this technique.

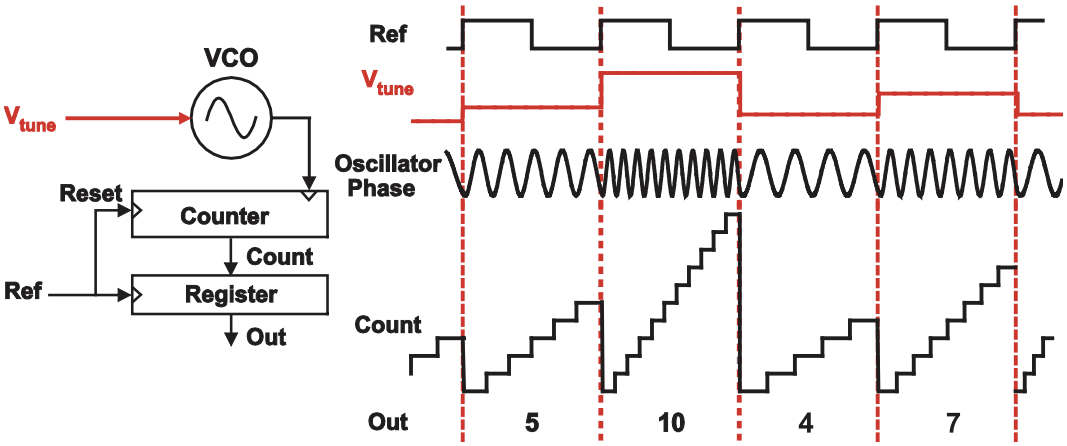

Figure 2.1: A VCO based A/D converter implementation (Straayer and Perrott, 2008)

A major benefit of using VCOs as quantizer is because of the inherent quantization noise shaping they offer. At the end of each sampling period, while the output only counts the number of full cycles completed. However, for the incomplete cycles, the additional phase generated is not lost since the oscillator waveform in the next period continues from where it was when the sampling period ended. Thus, the phase that has to be accumulated to cross a multiple of 2π in the next sample period is reduced by this quantity. Therefore, if the intrinsic value of the quantization error of in the n^{th} sample is q[n], which is just the fractional part of a cycles unaccounted for at the end of that sample period, then, the actual value of quantization error in the n^{th} sample, e[n], is given by,

$$e[n] = q[n] - q[n-1] \tag{2.1}$$

This shows that quantization noise spectrum is being shaped by a first order transfer function. This is illustrated in Figure 2.2 . Thus, if were to use the VCO quantizer as an oversampling converter, we could get the benefits of similar to a first-order $\Delta\Sigma$ system without even having to construct a feedback loop.

Such a behaviour is possible because in the VCO the output, phase, is not an instantaneous function of the input voltage. Rather, the frequency is instantaneously related to the input. Since the phase is the time integral of the frequency,

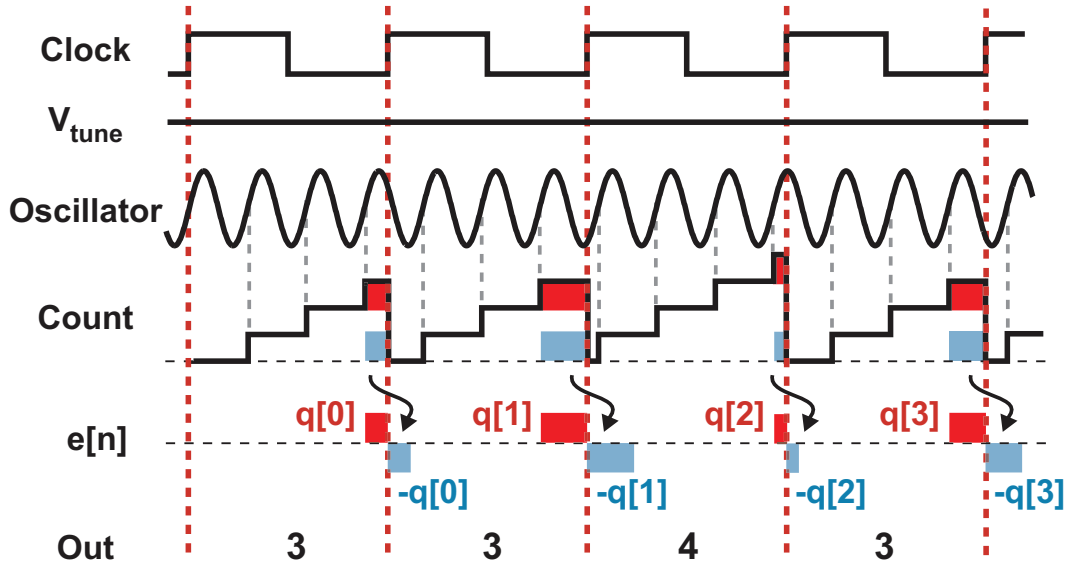

Figure 2.2: Inherent noise shaping in VCO based A/D converter implementation (Straayer, 2008)

to get the instantaneous voltage value, it has to be differentiated, which is done here in the discrete-time domain when we effectively calculate the phase *difference* over one sampling period. When the input signal is sampled data, the virtual integrator effectively acts like an accumulator. Thus the accumulator and the differencing cancel out. The quantization noise however is directly in the form of phase, so there is no accumulation involved. It still undergoes the discrete-time differentiation however, which leads the first order quantization noise shaping property.

This is shown in Figure

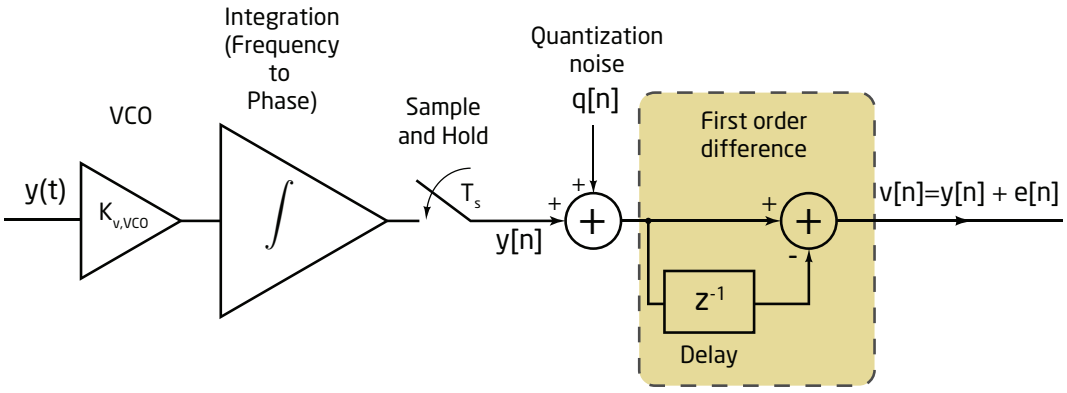

Figure 2.3: A block diagram representation of the signal flow

It is obvious that the maximum number of quantization levels (which is just the maximum number of cycles in a sampling period) is limited by the speeds of the oscillator as well as those of the counter. Since the precise shape of the

oscillator does not really matter, we can create very fast VCOs indeed with current technologies. however interfacing to another counter which has to run at the same speed may be cumbersome, considering the addition control circuitry required to quickly reset the counter. If we use a binary counter, to use the VCO in a $\Delta\Sigma$ loop, we would likely require an additional binary-to-thermometer conversion, which would mean that there is further excess loop delay in the quantizer stage itself

2.3 Voltage-Controlled Ring-Oscillators

A work-around for this would be to integrate the VCO and the counter into a single step if possible. Fortunately a voltage-controlled ring oscillator would achieve our requirement easily. In such an arrangements, as the input varies, the number of bits that flip will vary according to the VCO frequency. The change from a single oscillator to a ring oscillator can be viewed in two ways: either as slowing down the oscillator by a factor corresponding to the number of elements in the ring and reducing the phase quantization step size by the same quantity; or as mapping every half cycle of the phase difference to successive ring oscillator elements. Either way, we no longer need a special counter or a binary to thermometer conversion, since the ring oscillator outputs themselves are logic levels and to "count" the changes, we only need a transition detector, which can be easily implemented with just two registers and a exclusive-OR gate, working at the sampling frequency. One constraint for such a system is that the sampling frequency is fast enough so that there is no chance of any VCO element transitioning twice within one cycle, which would cause such a double transition to be counted as no transition. Thus, sampling period has to be less than half the time period of the overall ring oscillator, i.e.,

$$F_s > 2F_{ring,VCO}$$

Such a system is shown in Figure 2.4 (Straayer, 2008).

2.3.1 DAC mismatch control with Dynamic Element Matching.

For multi-bit quantizer based $\Delta\Sigma$ architectures, we require a full D/A converter to complete the feedback path. This is usually implemented as an array of identical sources which can be switched based on a logical input. Due to area and power

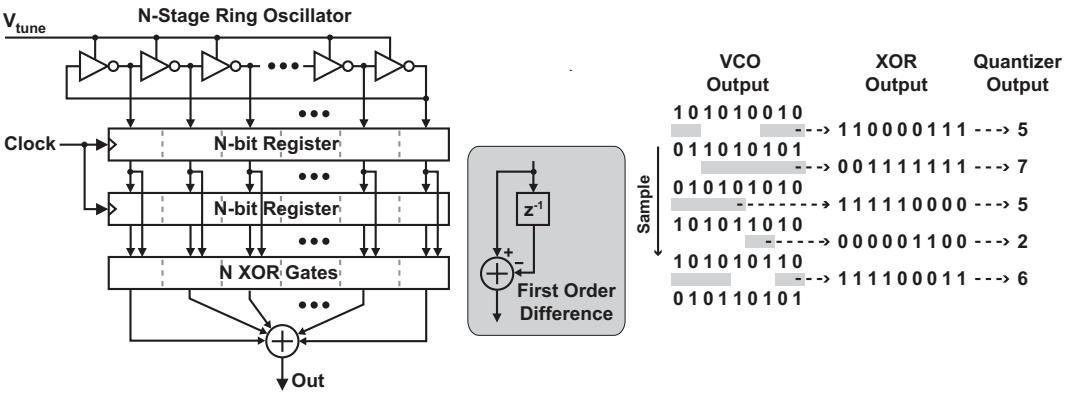

Figure 2.4: A voltage-controlled ring oscillator based quantizer

constraints, we cannot make them large enough to make mismatches between such devices to be negligible. This is crucial in $\Delta\Sigma$ converters, since any errors due to mismatch in the quantizer appear in the signal path at the output and are attenuated due to noise shaping. However, the DAC mismatch errors are in the same place as the input on the signal path, and hence are not naturally shaped away. Also, these mismatches appear as non-linearities, which can create unwanted harmonic tones in the desired signal band.

Dynamic element matching (DEM) is based on the idea that such non-linearities are created because normally the mismatch error corresponding to any digital input level to the DAC is a constant.This is because it the same set of DAC elements being switched on for each particular level. Thus, the error itself is directly dependent on the signal, creating tones. DEM involves randomly or pseudo-randomly changing the combination of DAC elements being switched on for a given digital DAC input. Thus, the DAC mismatch error becomes independent of the output signal, and therefore, of the input signal as well, eliminating tones.

Among the various DEM techniques, *data weighted averaging* (DWA) is quite attractive, because it also has the property of first order shaping of the mismatch error spectrum. However, because it is not truly random, the potential for tones, though greatly diminished, is still present. Nonetheless, it is a popular method used in several converters, despite the need for switching circuitry. An illustration is shown in Figure 2.5(Pavan and Krishnapura, 2008)

Implicit DWA in ring-VCO implementation

The similarity of the switching pattern of DAC in DWA and the outputs of a ring-VCO based quantizer are obvious. Thus, the VCO based quantizer also has the advantage of naturally giving DWA thermometer code outputs to the feedback

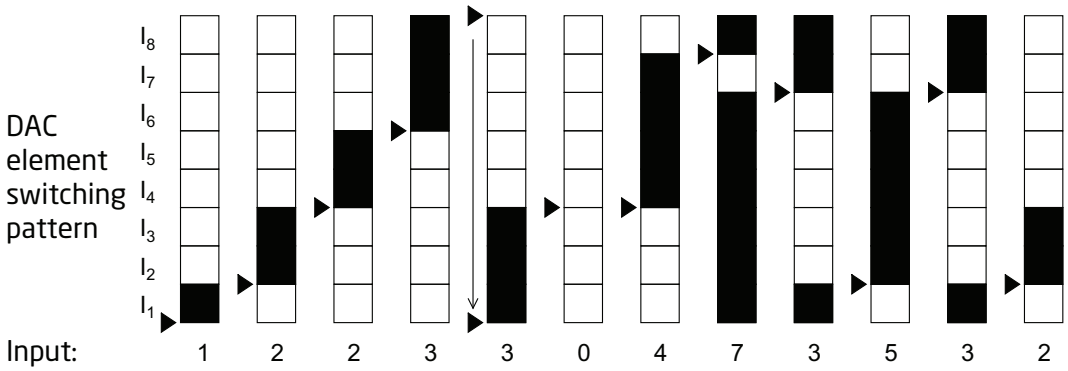

Figure 2.5: An illustration of the data weighted averaging (DWA) technique

DACs, eliminating the need for switching circuitry which could have further added to the excess loop delay.

Another feature of the VCO quantizer is that for a given input value, since the output depends on the initial phase, one instance is not sufficient to determine the true input-output relation. Instead, average number of transitions for a given input is what defines the VCO quantizer's transfer characteristic.This is a continuous curve rather than the stepped curves that curves

2.3.2 Non-linearity of VCO transfer characteristics

Most VCO's have highly non-linear tuning characteristics. Thus, the instantaneous frequency is a non-linear function of the input voltage. We have already seen that for the quantization noise, VCO quantizer has the performance benefits of first-order $\Delta\Sigma$ loop. However, the voltage-to-frequency transformation appears before the frequency to phase integration step in the signal flow shown in Figure 2.3. Thus, the benefit of the first-order difference is nullified by the accumulator effect of the integration. So, the non-linearity of the VCO remains a major issue.

2.3.3 Transistor implementation of voltage-controlled ring oscillators

To implement the voltage-controlled ring-oscillator, we used the simplest circuit, consisting of a chain of inverters with tail current sources which were controlled by the input voltage. We shall call the tail current sources as tuning transistors and the transistors in the middle, which behave like inverters would in a simple ring oscillator as the inverter transistors. By using minimum length (180 nm) transistors, we have the benefit of obtaining a small stage delay in the ring, increasing the

potential number of quantization levels. While we tested the the system by using the smallest allowed width, 240 nm for the NMOS inverter transistor, we used twice this width for the PMOS inverter transistor, to compensate for its lower conductivity. The ratio of the widths of the NMOS and PMOS tuning transistors to those of their respective inverter transistors was kept as a design variable, which we shall call ζ. The inputs to the tuning transistor are just the differential input voltages, with the positive input going to the gate of the NMOS transistor and the negative input going to the gate of the PMOS transistor. This is to make sure that the output increases on increasing the differential input voltage. Figure 2.6shows the schematic of one element cell of the ring oscillator.

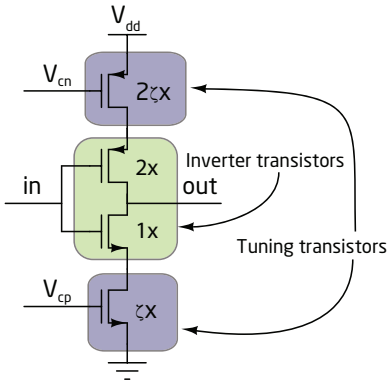

Figure 2.6: Schematic of the ring-oscillator cell

We also see that since every ring-oscillator cell is connected to an input of a register, there as an additional capacitive loading that has to be considered as well. This could also vary based on the sizing of the flip-flops.

2.3.4 Extraction of the transfer characteristics of the VCO from simulation

The transfer characteristic can be extracted easily by feeding a ramp input and taking the average number of transitions per clock cycle for a small interval around every desired input voltage data point. For the differential input range of -1.8 V to 1.8 V, we used 73 data points, and took the data from 50 clock periods for each data point.

Figures 2.7 and 2.8 shows the variation of transfer characteristics with the load capacitance as well as with as with ζ.

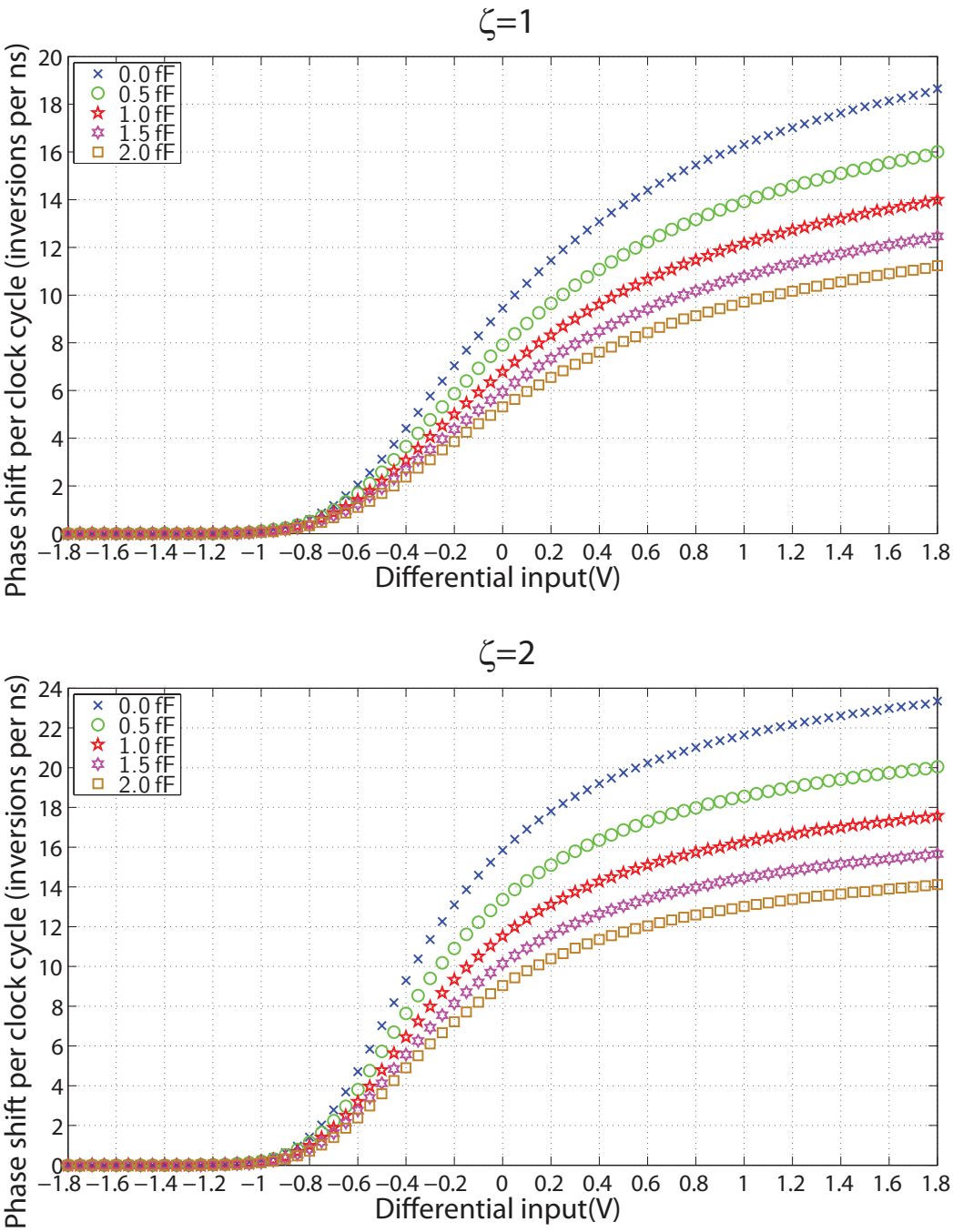

Figure 2.7: Variation of VCO transfer characteristics with capacitive load and ζ

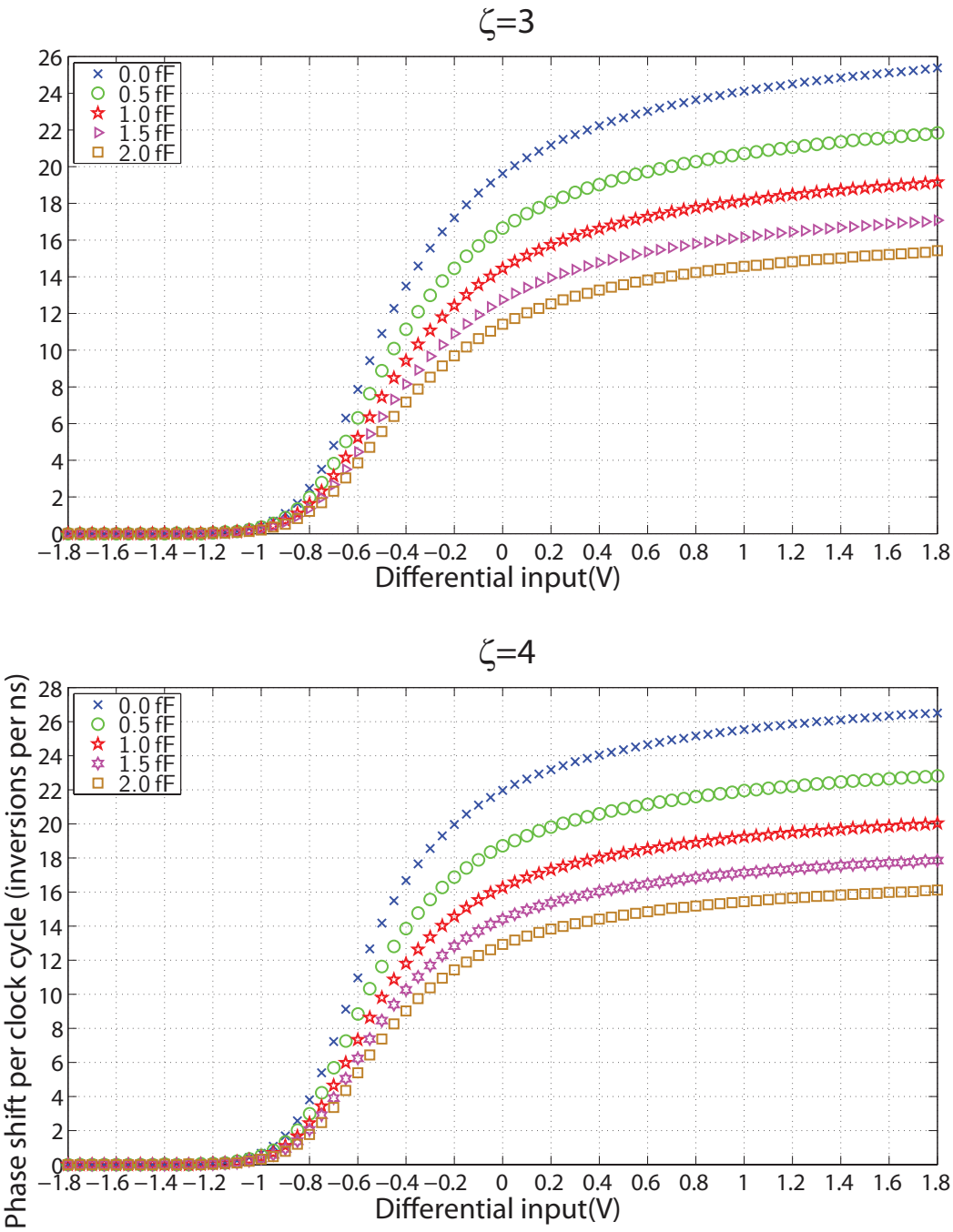

Figure 2.8: Variation of VCO transfer characteristics with capacitive load and ζ

2.3.5 Observations about the VCO transfer characteristics

It can be seen in the figure that these characteristics are not even close to linear over the entire input range. However some observations can be made regarding the nature of the curve.

Monotonicity

The transfer characteristic is monotonically increasing (within the resolution of the measurement). This is because as the input voltage increases, the gate overdrive for the tuning transistors increases, reducing the effective resistance offered by them.

Flat initial region

At lower input voltages the output is identically equal to zero. This is because at these values, the gate-source potentials is below the threshold, so that only tiny leakage currents drive the inverter. Thus, transitions, if any, are over timescales far exceeding the sample period.

Fast-rising section

After a certain knee-voltage the output rises rapidly, which is just a reflection of the rapid rise in the current driving capacity of the tuning transistors. The transfer characteristics are much more linear in this region however, and this is the part of the characteristics where the VCO works best as an A/D converter.

Saturating section

The output then flattens out, with the incremental gain continually falling in spite of the current driving capacity of the tuning transistors increasing. This is because the inverter transition rate is now limited by the current carrying capacity of the inverter transistors themselves. However, the output doesn't completely saturate within the input range. This is because the tuning current sources now effectively appear as small degenerating resistors to the inverter transistors. Their effective resistance reduces with increasing inputs, thus improving the speed of the inverter, but naturally, the increases are diminishing.

2.4 Fast Modeling of the VCO for MATLAB or Verilog-A

For initial tests of performance estimates for ADCs using VCO based quantizer, we can perform simulations by keeping only the the VCO block as transistor level circuitry but replacing the other with ideal blocks. However it was observed that even such simulations take extremely large amounts of time, since the transistor model of the VCO has several hundred nodes in SPICE simulations. Therefore, simpler macro-models which are computationally efficient but still manage to retain the characteristics of the VCO based quantizer, such as its inherent noise-shaping and an accurate modeling of the non-linearities in the transfer characteristic become necessary. In this section we shall take the example of the case of a VCO ring in which the ζ factor is 2 along with a parasitic load of 1 fF per cell, whose characteristics are shown in Figure 2.9.

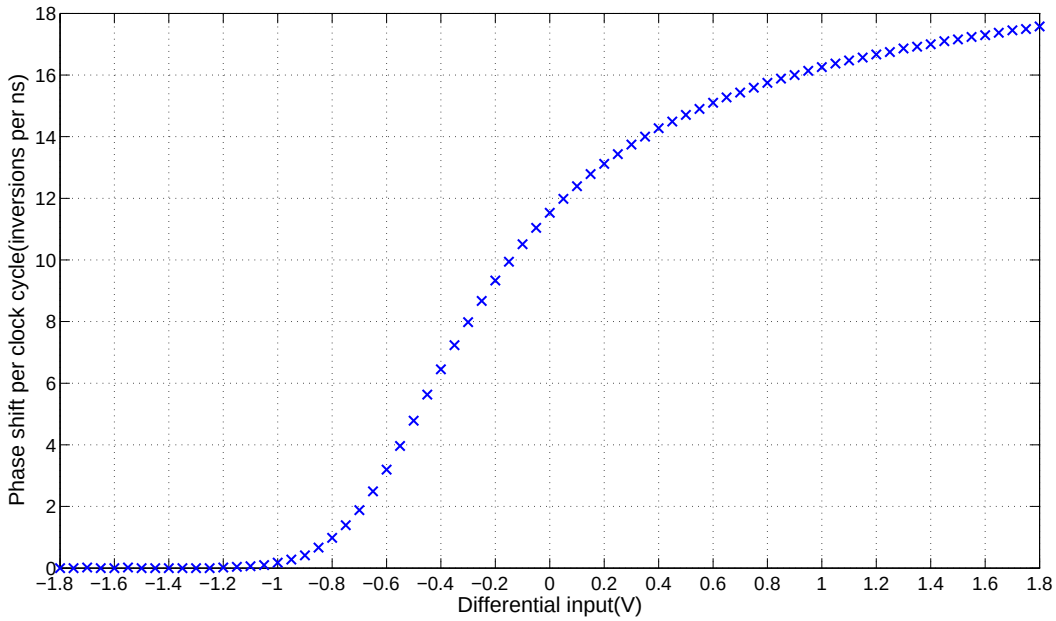

Figure 2.9: VCO transfer characteristics

2.4.1 Polynomial-fit based models

Since the characteristics are non-linear, the easiest models to describe a general non-linear curve are polynomials. These are especially well suited for systems which are nearly linear, i.e. those in which the linear term is much larger than the other terms, over the region of interest (since if we extend our analysis towards infinity, the highest order terms will always dominate the curves.). Preferably a

low order polynomial should provide a good fit, so that the number of parameters which have to be solved for are minimized.

When attempts were made to fit such models to the generated VCO characteristics, it was found that lower degree polynomials were very poor choices to fit to the curves. The best fit polynomials always had to dip below zero initially, to be able to come close to the characteristics, and for polynomials below the 9^{th} degree this dip was very severe indeed. Figure 2.10 shows this phenomenon in a sixth order polynomial. This is a very serious drawback; the incremental gain changes sign if the curve is non-monotonic, which can turn a negative feedback loop into an unstable positive feedback loop. The co-efficients of the higher order polynomials, which came reasonably close to the actual characteristics, were devoid of any intuition whatsoever, making any attempt at manually fitting characteristics, impossible.

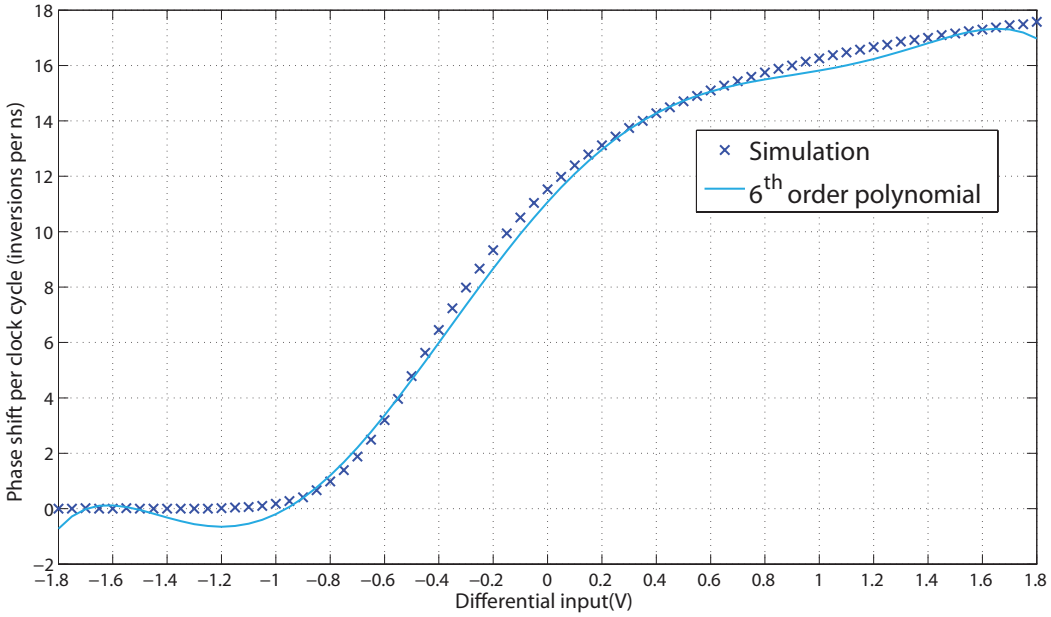

Figure 2.10: VCO transfer characteristics with a polynomial fit

2.4.2 Better models for VCO characteristics

Since polynomials were shown to be unsuited for modeling the VCO transfer curves, we shall have to develop other classes of functions which might be better at fitting these curves. One of the main "problem regions" for the polynomial based models was the near constant region at the beginning of the curve. The near saturation at the end of the curve was also a problem since polynomials never saturate. However, there are other curves which have a flat region near an origin and

then rise up quickly and saturate, namely, high-pass filter (HPF) transfer functions. Among such functions, are Butterworth high-pass filter (BHPF) transfer function curves, which are of the form

$$f_{BHPF}(\omega) = \frac{\omega^n}{\omega_0^n + \omega^n}$$

which can be generalized to the form

$$f(x) = \frac{a(x-b)^n}{c + (x-b)^n}$$

Here, the coefficient a is the final saturation value,b represents a shift in the origin, n is related to how quickly the function rises and c is related to where the function starts rising.

When we try to fit BHPF-like functions of various orders to these VCO characteristics, we find that there a very good fit in the initial flat region as well as in the fast rising portions of these curves. However, there are deviations in the end of the characteristics, since the VCO characteristics do not actually saturate and only approach saturation.

Thus a slight modification is required, for which we add an additional term in the numerator.

$$f(x) = \frac{a\left((x-b)^n - d(x-b)^{n-1}\right)}{c + (x-b)^n} \tag{2.2}$$

If we use the single ended voltage driving the NMOS tuning transistor, we can simplify this by eliminating b

$$f(x) = \frac{a(x^n - dx^n)}{c + x^n} \tag{2.3}$$

In such a curve, the new term has a gradually diminishing effect, which slows down the saturation, so that these models can match the slowly saturating regions of the VCO transfer curve as well. Indeed, an excellent fit can be obtained by manually putting in the model co-efficients just by observation and trial and error. For instance for the characteristics shown in Figure 2.9, the values of the coefficients in Eq. 2.3 which were manually fixed are

$$a = 22$$
$$n = 6$$
$$d = 0.35$$
$$c = 0.08$$

The results are shown in Figure 2.11, which is seen to be much better than a 6^{th} order polynomial fit even though it has only four degrees of freedom compared to the seven that the polynomial has.

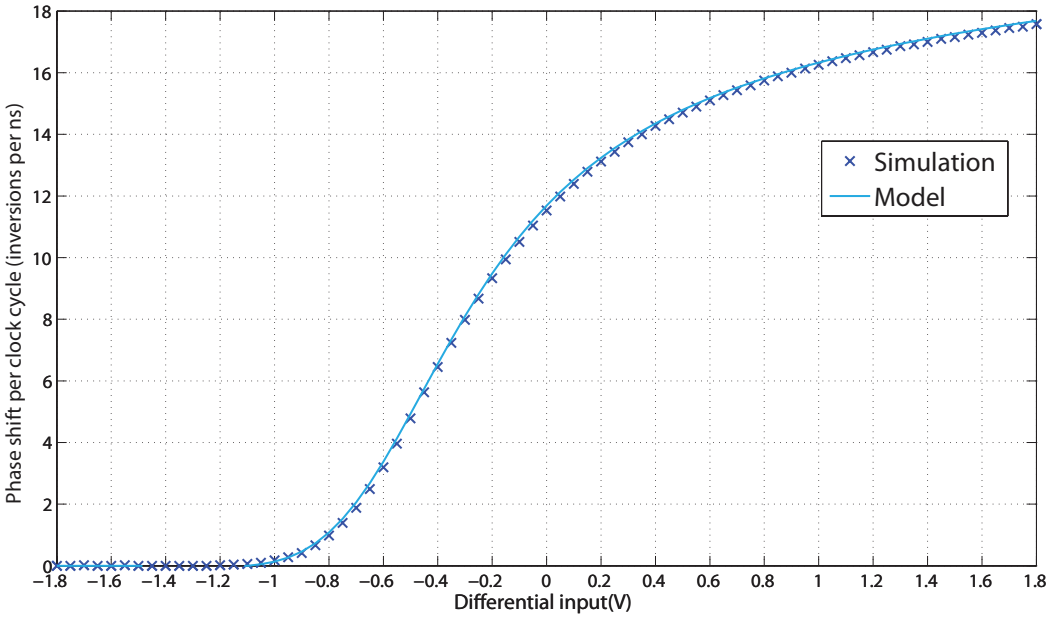

Figure 2.11: Manually fit VCO transfer characteristics

While the additional term now causes the the characteristics to dip below zero in the the beginning, this effect is so small (the maximum negative slope is about 100 times smaller than the maximum positive slope), that we can avoid such instabilities. If necessary, another term can be added in the denominator to suppress this further

In Figure 2.12 we have the results of fitting the coefficients using MATLAB's non-linear least squares fitting tools.

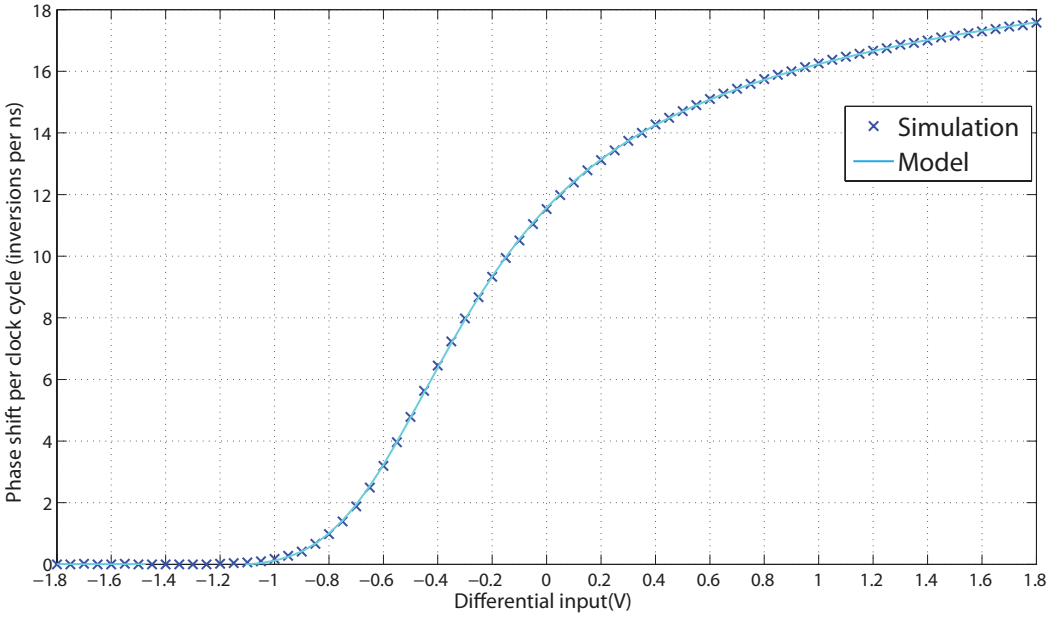

Figure 2.12: VCO transfer characteristics along with the best-fit curve of the form defined by Eq. 2.3

2.4.3 Utilization of the model

Thus we have a simple empirical model to calculate the VCO quantizer's output for a given analog input. These models also give continuous and differentiable curves which can help in determining loop gain easily as well. Also, these models are ideal for creating discrete-time equivalent $\Delta\Sigma$ structures which can be analyzed very quickly in MATLAB. Verilog-A blocks can also be designed, to simulate the VCO quantizers without idealizing the rest of the $\Delta\Sigma$ loop components.

CHAPTER 3

$\Delta\Sigma$ A/D Converters with VCO-based quantizers

3.1 Introduction

In this chapter, we shall describe how we shall integrate the VCO into a $\Delta\Sigma$ loop to leverage the high sampling speed that it enables to improve resolution. As we have observed earlier, the VCO quantizer has advantages like inherent DWA'ed thermometer outputs which aren't particularly good for use as a stand-alone quantizer but very good for use in with feedback DACs in $\Delta\Sigma$ ADCs. They also naturally have some quantization noise shaping, which would only improve the performance of a $\Delta\Sigma$ loop. However, it also suffers from significant non-linearities, which $\Delta\Sigma$ loops are very good at eliminating. Thus, it would seem that VCO quantizers would fit in quite well within the framework of $\Delta\Sigma$ ADCs. However, there are some issues which have to be handled before we can use them in this manner.

3.2 Offset and distortion

As seen earlier the transfer characteristics of the VCO are non-linear. We will now make some observations about the specific nature of the non-linearities and the challenges they pose.

3.2.1 Offset

When we observe the characteristics in Figures 2.7 and 2.8, we observe that the characteristics are not symmetric about zero. The fast rising sections, which are also the most linear sections of the characteristics of all these graphs are off to one side. If we give a full scale sine-wave input, the mean output value would also be off from the mean value of the maximum and minimum output values. In a normal quantizer, this would not be too much of a problem, as the high feedback gain at DC ensures that that any offset is minimized. However, because the VCO quantizer characteristics are highly non-linear, this offset can cause the

$\Delta\Sigma$ modulator to become unstable. Thus, this would require careful design of the parameters of the modulator so that correct operation is assured.

3.2.2 Distortion

Since the tuning characteristics of the VCO quantizer are highly non-linear, we observe high harmonic distortion when the system is used in open loop. When the VCO quantizer is used in a $\Delta\Sigma$ modulator, the non-linearities are suppressed by the large loop gain at low frequencies, but not eliminated. The frequency spectrum also shows that the second-order (quadratic) distortion is the most significant term in the non-linearity.

3.2.3 A differential method for reduction of distortion

In other types of quantizers, any distortion or offset is usually the result of random mismatch. In the VCO quantizer, the tuning characteristic has these problems even without such variations. Essentially the non-linearity is a systematic defect. Thus, we can try to ameliorate it.

Let the VCO tuning characteristic be $f(V_{in})$. Then, we can expand it in a power series (the Taylor series) about the origin as

$$f(V_{in}) = c_0 + c_1 V_{in} + c_2 V_{in}^2 + c_3 V_{in}^3 + \dots \tag{3.1}$$

This is the function with all its non-linearities (terms with coefficients c_2, c_3, c_4 ...) and the offset (the constant term c_0).

Now, let us consider the expression

$$f_{lin}(V_{in}) = f(V_{in}) - f(-V_{in}) \tag{3.2}$$

If we expand the right hand side of the above expression, we get

$$\begin{aligned} f_{lin}(V_{in}) = {} & c_0 + c_1 V_{in} + c_2 V_{in}^2 + c_3 V_{in}^3 + \dots \\ & - \left(c_0 - c_1 V_{in} + c_2 V_{in}^2 - c_3 V_{in}^3 + \dots\right) \end{aligned} \tag{3.3}$$

This simplifies to

$$f_{lin}\left(V_{in}\right) = 2c_1V_{in} + 2c_3V_{in}^3 + 2c_5V_{in}^5 + \ldots \tag{3.4}$$

We see that the offset and all even order non-linearities have been eliminated. While odd-order non-linearities still remain with double the coefficient as before, they have the same value as before relative to the linear term, which is the desired term. Therefore, this is a feasible way to reduce the non-linearity of the VCO transfer characteristics.

To implement this expression with the VCO quantizer is quite simple. We now use two quantizers, one to obtain $f\left(V_{in}\right)$, and the other to obtain $f\left(-V_{in}\right)$. Since we have differential inputs, to get $f\left(-V_{in}\right)$, all we have to do is interchange the positive and negative inputs.

The subtraction of the outputs of the two quantizers could create a large delay in the $\Delta\Sigma$ loop if implemented with digital logic. However, this is not necessary since we have thermometer outputs. If we are using current steering DACs, to implement the subtraction we once again interchange the outputs of the DAC. This method of obtaining $f_{lin}\left(V_{in}\right)$ is illustrated in Figure 3.1.

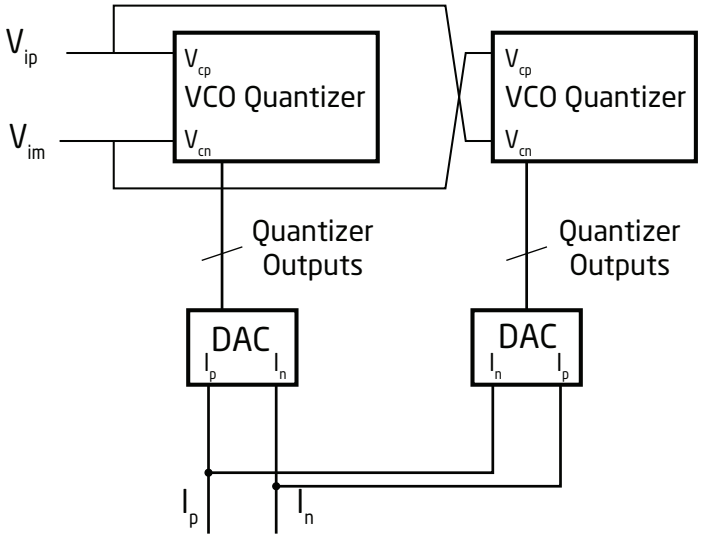

Figure 3.1: Differential quantizer to reduce non-linearity and eliminate offset.

This method of canceling the offset is a kind of differential operation, because of which we shall call this a *differential VCO quantizer*. Figure 3.2 shows one example of how the characteristic has been linearized and the offset eliminated, when we crate a differential VCO quantizer from the VCO quantizer whose characteristics are shown in Figure 2.9.

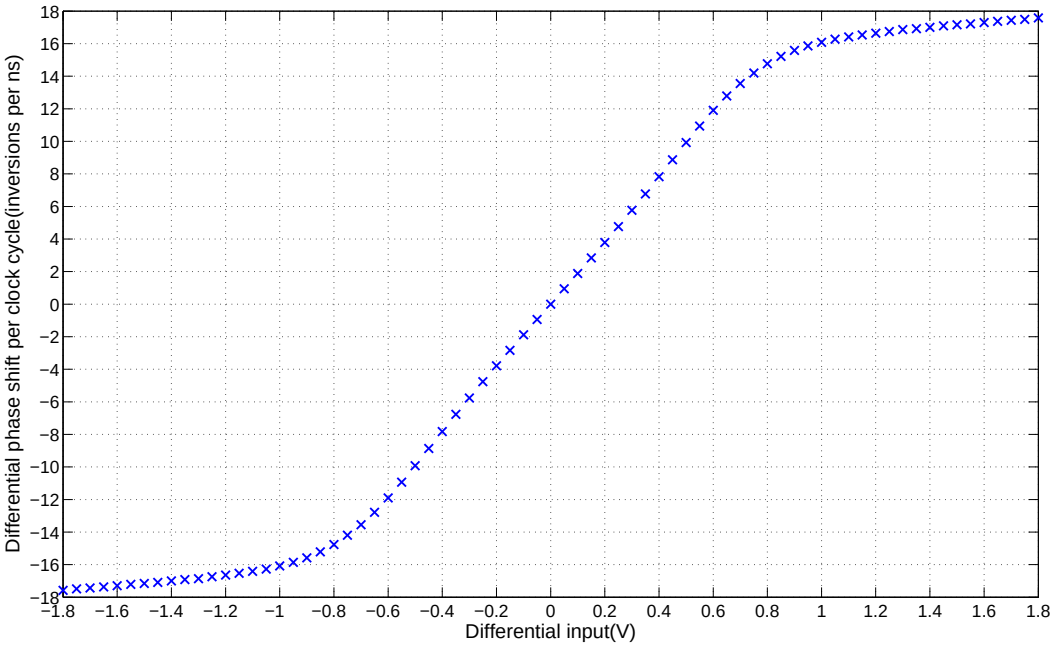

Figure 3.2: Differential VCO quantizer transfer characteristics

In addition to the improvement in distortion, there is also an improvement in the SQNR. If we consider the quantization noise in each quantizer, we can assume them to be uncorrelated. This assumption is further strengthened because of the inherent first-order noise shaping of the VCO quantizer. Thus, the quantization noise power in the differential VCO quantizer is just double that of a single VCO quantizer. The signal amplitude doubles, quadrupling the signal power. Thus, the SQNR increases by 3 dB, increasing the ENOB by 0.5 bits . In a classical quantizers, by doubling the number of comparators and staggering the quantization levels correctly, we can increase the SQNR by 6 dB and thus increase the ENOB by 1 bit. So, it might seem that this is wasteful. However, the main objective of the differential quantizer was to reduce distortion, and if the second order distortion is the dominant cause of harmonics, then the benefit in SNDR could be much more than 6 dB, making this method quite viable. The differential quantizer also has another benefit. In a simple $\Delta\Sigma$ modulator, the number of DAC elements switching is usually a small number, which is more or less independent of the input., thanks to the relative slowness of the input signal. However, with DWA, the number of DAC elements switching would become almost proportional to the input, which could lead to large dynamic non-linearities. In the differential VCO quantizer, the total number of DAC elements switching would be the sum of the two quantizers, which consist of the offset and the even order non-linearities. This would vary much less, and the dynamic non-linearity from switching would be mostly converted to a DC offset.

Finally, even if the power consumption of the quantizer doubles, the overall power consumption of a $\Delta\Sigma$ ADC with this quantizer is relatively unaffected, since the VCO quantizer consumes so less power compared to rest of the loop.

3.3 Sampling and the VCO quantizer

In the voltage-controlled ring oscillator architecture that we have chosen, there is a sampling action which occurs when there is a clock edge at the registers. However these is a virtual integrator between the input to the oscillator and this sampler. This has to be taken care of in a continuous-time framework rather than in a discrete-time one. However, if we add a sample-and-hold before the VCO input , then, this integrator behaves exactly like a discrete-time accumulator, and so, the entire loop transfer function can be handled in the discrete-time domain. Thus, this architecture can be used with either CT-$\Delta\Sigma$ modulators or with DT-$\Delta\Sigma$ modulators. There are some other crucial differences, which we shall explore in later sections. However we shall first consider the VCO quantizer with a sampler at its input.

3.4 Latency and excess loop delay in sampled-input VCO quantizers

The output of the quantizer, which reflects the phase of the oscillator, is dependent on the integral of the input voltage. Thus, it can never give instantaneous outputs. We have to take the phase change over a finite time period to get the correct output. In the current technique for extracting the output of the VCO quantizer, there is latency of one sampling period before we obtain the output corresponding to a given input, even ignoring any delays in the digital logic. In a CT-$\Delta\Sigma$ loop, this would mean that the excess loop delay is at least one clock cycle, which cannot be be compensated for exactly by any known method. Even DT-$\Delta\Sigma$ loops would be unable to work properly. One work around for this would be to measure the phase change over a fraction of the sampling period, instead of the whole sampling period. Then, the loop delay could be lower than one clock cycle, which can be compensated for by changing the integrator coefficients in the loop-filter. However, there are major problems with such a plan. Firstly, our current method for obtaining the correct outputs would no longer work. Since the phase accumulation takes place over a shorter time, the resolution of the quantizer would

also be reduced. Most importantly, the first order noise shaping property would be lost. In fact, there would now be two sources of quantization noise, one at the beginning of the quantization period and one at the end, neither of which is correlated amongst successive samples. Thus, we can not try to take the results from the phase change over a part of the cycle alone. This is shown in Figure 3.3.

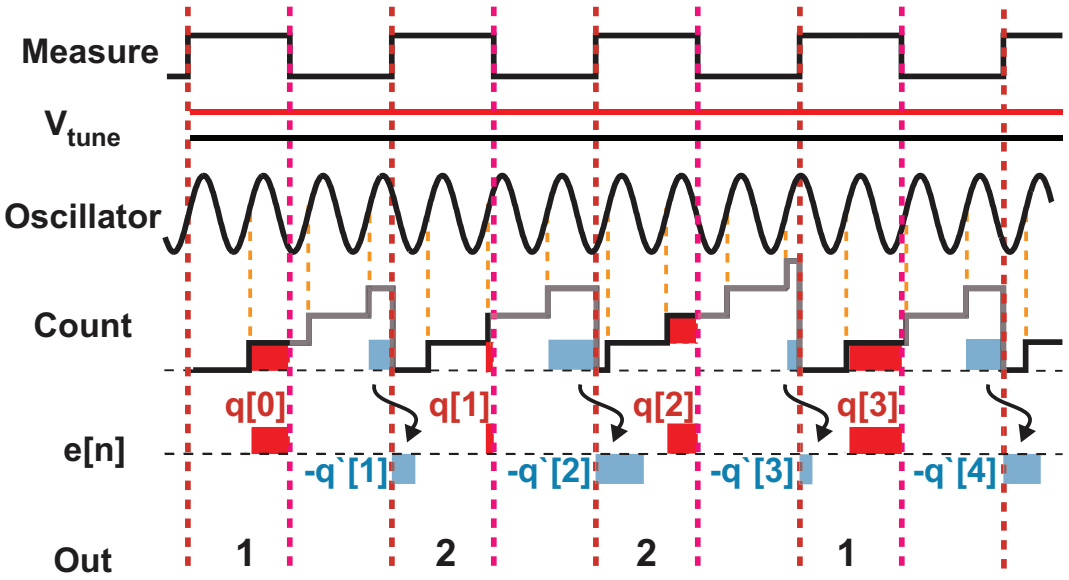

Figure 3.3: Increased noise with fractional cycle measurements

If we take the phase change over one complete sample period, the first order noise-shaping must also be considered while computing the NTF and the LTF. Otherwise, coupled with the latency, this might affect the stability of the system when blindly coupled with a normal loop filter. In the following section, we shall analyze these in detail, so that we can properly derive stable loop filters.

3.5 A reorganized model for feedback in sampled-input VCO quantizers

To simplify our analysis, we will ignore the non-linearity in the VCO characteristic. We already know that for sampled input, the STF is just a delay of one sample and that the NTF is the first order difference function, as shown in the the following figure.

The same STF can be obtained by have an accumulator with a delay, followed by a first order difference block, which is shared with the quantization noise, as seen in Figure 3.4. Since we will be operating in the discrete-domain, we can now

ignore the sample-and hold blocks for simplicity. We will also normalize the "gain" of the block, so that the nominal gain is unity.

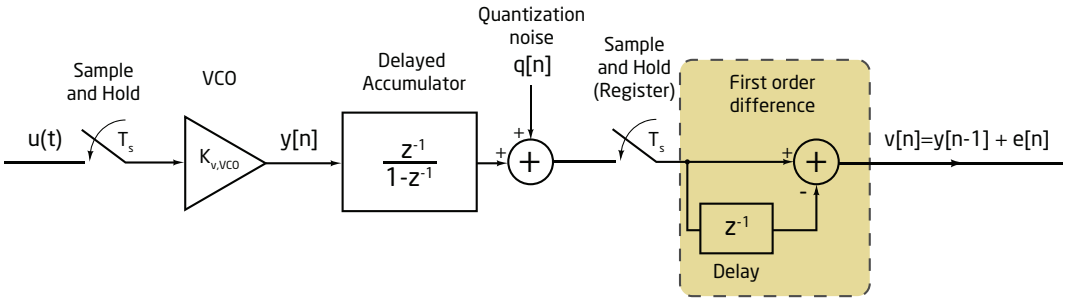

Figure 3.4: A block diagram for the sampled input VCO quantizer

The first order difference can also be modeled as the result of a feedback loop, using an accumulator with a delay in the feedback path as shown in Figure 3.5.

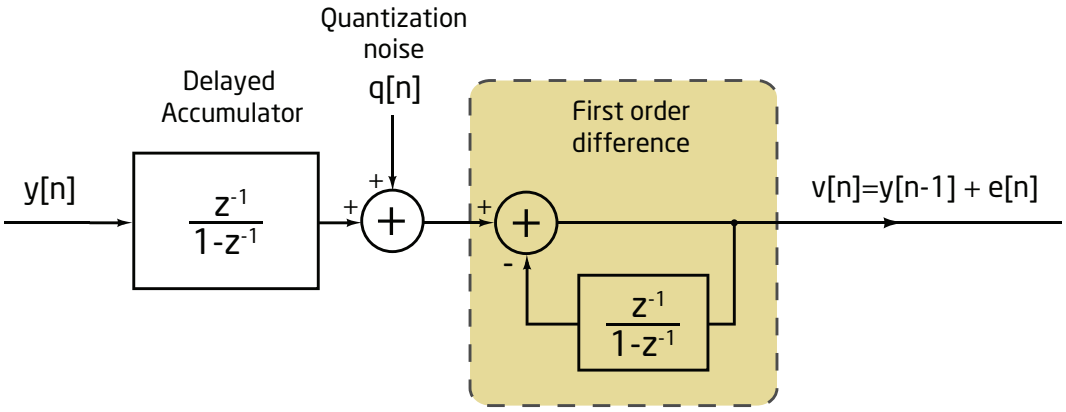

Figure 3.5: A feedback-based model for the first order difference

With a little rearrangement of the block diagram, we obtain the following model shown in Figure 3.6 for the VCO quantizer. The non-linearity can just be added to the beginning of this model as another block if necessary.

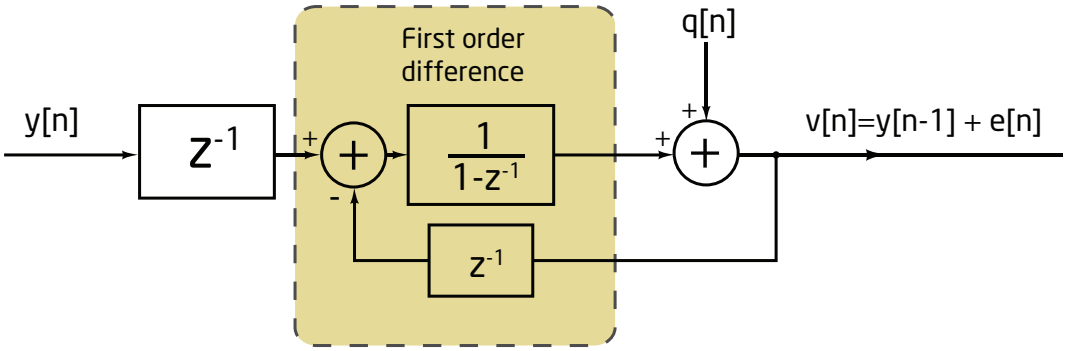

Figure 3.6: A feedback model for the VCO quantizer

Now if we add any additional feedback $L(z)$, then, it would change the modulator to Figure **??**. Note that for the loop filter, the the zeroth sample must be zero, since no feedback can be instantaneous in discrete-time. A CT- $\Delta\Sigma$ modulator with this model is shown in 3.8 Note that for the loop filter, the the zeroth sample must be zero, since no feedback should be instantaneous in discrete-time.

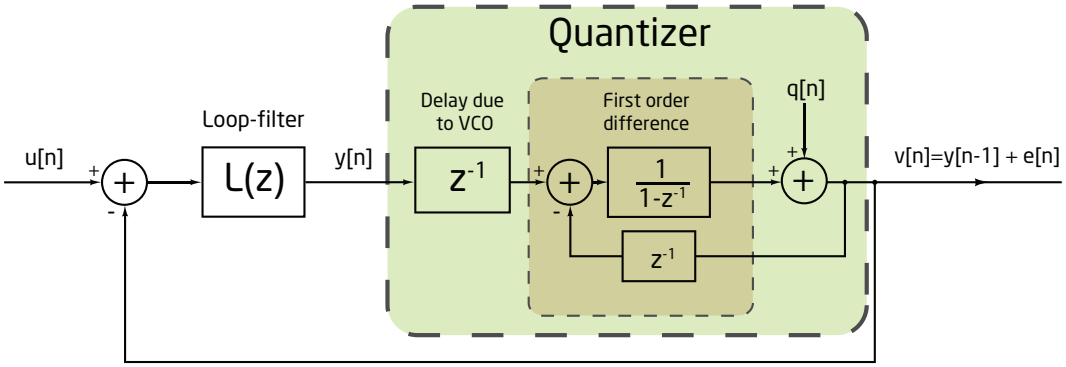

Figure 3.7: A Block diagram model with additional loop-filter

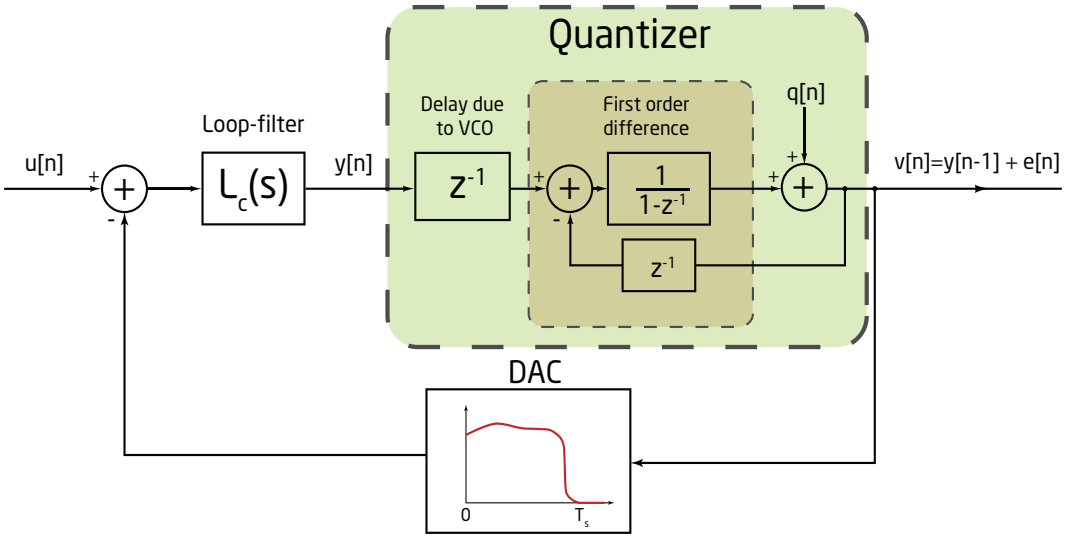

Figure 3.8: A model for a CT- $\Delta\Sigma$ modulator with the sampled VCO quantizer

This would would mean that the effective loop transfer function is now

$$L_{eff}(z) = \frac{L(z)\,z^{-1} + z^{-1}}{1 - z^{-1}} = \frac{(L(z) + 1)\,z^{-1}}{1 - z^{-1}} \tag{3.5}$$

3.5.1 Loop-filter transfer functions for sampled-input VCO quantizers

Now, since, the value of zeroth sample of $L(z)$is always zero, this means that the first sample (corresponding to the co-efficient of z^{-1} in the Laurent series

expansion of $L_{eff}(z)$ must be the same as that of $\frac{z^{-1}}{1-z^{-1}}$, which is unity.

Thus, we have condition that the the loop transfer-function is always of the form

$$z^{-1} + az^{-2} + bz^{-2} \ldots$$

In zero-pole-gain form, this would mean that LTF is always of the form

$$L_{eff}(z) = \frac{z^{-1}(1 - a_1 z^{-1})(1 - a_2 z^{-1}) \ldots (1 - a_m z^{-1})}{(1 - p_0 z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} \tag{3.6}$$

Thus, the gain factor would always have to be unity.

Now, while it is obvious from (3.21) that any transfer function obtained with a realizable transfer function will always be of the form shown in (3.7), we shall now show that such transfer functions always result in realizable loops.

For a $L(z)$ to be realizable, it must be of the form

$$L(z) = \frac{k\, z^{-1}(1 - a_1 z^{-1})(1 - a_2 z^{-1}) \ldots (1 - a_m z^{-1})}{(1 - p_0 z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} \tag{3.7}$$

If $L_{eff}(z)$ has a pole at $z = 1$, then it is of the form

$$L_{eff}(z) = \frac{z^{-1}(1 - a_1 z^{-1})(1 - a_2 z^{-1}) \ldots (1 - a_m z^{-1})}{(1 - z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_m z^{-1})} \tag{3.8}$$

for this effective transfer function, the required $L(z)$ would be

$$\frac{L(z)\, z^{-1}}{(1 - z^{-1})} = \frac{z^{-1}(1 - a_1 z^{-1})(1 - a_2 z^{-1}) \ldots (1 - a_n z^{-1})}{(1 - z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} - \frac{z^{-1}}{(1 - z^{-1})} \tag{3.9}$$

$$\implies \frac{L(z)\, z^{-1}}{(1 - z^{-1})} = \frac{z^{-1}\{(1 - a_1 z^{-1}) \ldots (1 - a_m z^{-1}) - (1 - p_1 z^{-1}) \ldots (1 - p_n z^{-1})\}}{(1 - z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} \tag{3.10}$$

$$\implies \frac{L(z)\, z^{-1}}{(1 - z^{-1})} = \frac{z^{-2}\left(b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_{n-1} z^{-(n-1)}\right)}{(1 - z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \ldots (1 - p_n z^{-1})} \tag{3.11}$$

$$\implies L(z) = \frac{b_0 z^{-1}(1 - c_1 z^{-1})(1 - c_2 z^{-1}) \dots (1 - c_{n-1} z^{-1})}{(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \dots (1 - p_n z^{-1})} \tag{3.12}$$

This shows that whenever the desired LTF has a pole at $z = 1$, the additional loop-filter transfer function is not only realizable, but can also be implemented with one fewer order than the actual LTF.

Now we consider the case when there is no pole at $z = 1$. Here, we have

$$\frac{L(z) z^{-1}}{(1 - z^{-1})} = \frac{z^{-1}(1 - a_1 z^{-1})(1 - a_2 z^{-1}) \dots (1 - a_n z^{-1})}{(1 - p_0 z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \dots (1 - p_n z^{-1})} - \frac{z^{-1}}{(1 - z^{-1})} \tag{3.13}$$

$$\implies \frac{L(z) z^{-1}}{(1 - z^{-1})} = \frac{z^{-1}\left\{(1 - z^{-1})(1 - a_1 z^{-1}) \dots (1 - a_n z^{-1}) - (1 - p_0 z^{-1}) \dots (1 - p_n z^{-1})\right\}}{(1 - z^{-1})(1 - p_1 z^{-1})(1 - p_2 z^{-1}) \dots (1 - p_n z^{-1})} \tag{3.14}$$

In this case, these calculations are equivalent to multiplying both the numerator and denominator of the original desired LTF by $(1 - z^{-1})$. After that, it is similar to the case with a pole at $z = 1$. However, we no longer have the benefit of the extra order we had in case of the transfer functions with poles at $z = 1$, because the pole we gain is lost when we increase the order of the numerator and denominator.

3.5.2 Usable loop-filter transfer functions

Now that we have seen what are the requirements of the loop transfer functions which can be used with a sampled-input VCO quantizer, we shall now try to obtain NTFs and their corresponding LTFs satisfying these requirements for implementing $\Delta\Sigma$ modulators.

Most of the characteristics of the LTF are determined by the poles of the NTF, with the position of the zeros providing a small additional boost to the SQNR. To simplify or analysis and gain insight, we shall first consider NTFs with all their zeros at $z = 1$.

The simplest such NTFs are of the form $(1 - z^{-1})^M$, where M is the the order of the modulator. Consider a 3rd order modulator of this kind, i.e., with an NTF $(1 - z^{-1})^3$. The corresponding loop transfer function for this would be

$$\frac{3z^{-1} - 3z^{-2} + z^{-3}}{(1 - z^{-1})^3}$$

Clearly, this does not satisfy the requirements given earlier. We would therefore have to modify this transfer function to be of the correct form. A simple way of doing this is to either scale the whole LTF down by a constant factor, so that the coefficient of the z^{-1} term in the numerator is unity; another way is to scale down only the coefficient of z^{-1} term in the numerator to unity. However, if we check the resultant NTF, in both cases, the NTFs had poles outside the unit circle, making the system unstable. We can try these methods with other NTFs as well, but usually either the new NTF is unstable or has excessive peaking in the frequency response, making it unsuitable for use with $\Delta\Sigma$ modulators. Thus, there is no simple way to modify a general NTF to be suitable for our use.

We can try other methods to find suitable NTFs. We usually use NTFs which are are maximally-flat high-pass filters, characterized by their high frequency gain, also called the out-of-band gain (OBG). Higher order $\Delta\Sigma$ modulators use an OBG of about 1.5 with single-bit quantizers and OBGs used with multi-bit quantizers range from 2-3. This is for reasons to do with stability. By using numerical methods, we find that for a third order maximally-flat transfer function, the loop-filter gain is unity when the OBG is about 1.66. For fourth and fifth order NTFs , the same requirement is again met at very similar OBGs. These are tabulated in Table 3.1 on page 31.

Table 3.1: Maximally-flat NTFs without optimized zeros

Order	OBG	NTF
3	1.6656	$\frac{(1 - z^{-1})^3}{(1 - 0.5901z^{-1})(1 - 1.41z^{-1} + 0.6107z^{-2})}$
4	1.6571	$\frac{(1 - z^{-1})^4}{(1 - 1.378z^{-1} + 0.486z^{-2})(1 - 1.622z^{-1} + 0.7494z^{-2})}$
5	1.6538	$\frac{(1 - z^{-1})^5}{(1 - 0.73z^{-1})(1 - 1.53z^{-1} + 0.605z^{-2})(1 - 1.74z^{-1} + 0.828z^{-2})}$

After obtaining suitable NTFs, we have have to obtain the transfer function for the continuous-time filter to be placed in the loop. From the NTF, we can easily obtain the desired effective loop transfer functions shown in Table 3.2 on page 32 . Using (3.21), we can obtain the external LTF to be added, which is given by

$$L(z) = \frac{L_{eff}(z)(1 - z^{-1})}{z^{-1}} - 1 \tag{3.15}$$

Table 3.2: LTFs for maximally-flat NTFs without optimized zeros

Order	LTF
3	$\frac{z^{-1}\left(1-1.557z^{-1}+0.6397z^{-2}\right)}{\left(1-z^{-1}\right)^3}$
4	$\frac{z^{-1}\left(1-0.7893z^{-1}\right)\left(1-1.74z^{-1}+0.8055z^{-2}\right)}{\left(1-z^{-1}\right)^4}$
5	$\frac{z^{-1}\left(1-1.671z^{-1}+0.703z^{-2}\right)\left(1-1.848z^{-1}+0.9021z^{-2}\right)}{\left(1-z^{-1}\right)^5}$

If we assume a non-return-to-zero (NRZ) DAC for the feedback path in the loop-filter, then, to obtain the continuous-time loop filter, we can just use the `d2c` function in MATLAB. Table 3.3 on page 32 shows the CT transfer functions assuming a sampling frequency of 1 Hz. For any other sampling frequency F_s Hz, this can be scaled appropriately using the substitution

$$s \rightarrow \frac{s}{F_s} \tag{3.16}$$

Table 3.3: LTF implementation for maximally-flat NTFs without optimized zeros

Order	External LTF	CT External LTF
3	$\frac{0.4426z^{-1}\left(1-0.8141z^{-1}\right)}{\left(1-z^{-1}\right)^2}$	$\frac{0.4015}{s}+\frac{0.0.0823}{s^2}$
4	$\frac{0.47042z^{-1}\left(1-1.745z^{-1}+0.7741z^{-2}\right)}{\left(1-z^{-1}\right)^3}$	$\frac{0.415}{s}+\frac{0.1062}{s^2}+\frac{0.01375}{s^3}$
5	$\frac{0.4820z^{-1}\left(1-0.865z^{-1}\right)\left(1-1.85z^{-1}+0.877z^{-2}\right)}{\left(1-z^{-1}\right)^4}$	$\frac{0.4204}{s}+\frac{0.1162}{s^2}+\frac{0.02029}{s^3}+\frac{0.001784}{s^4}$

The frequency response for these NTFs is given in Figure 3.9. We can see that for the transfer functions without optimized zeros, there is not too much improvement in the response for various orders except at very low frequencies. Indeed, for frequencies with an OSR below 20, increasing the order actually worsens the SQNR. The theoretical improvement in SQNR of $\Delta\Sigma$ ADCs with an OSR of 25 compared to that of a Nyquist rate ADC using the same quantizer is shown in Table 3.4 on page 33. As we can see, there is very little benefit from increasing the order in this class of transfer functions

Therefore, we can try to add optimized zeros, for these transfer functions. Using the Schreier toolbox for MATLAB, we can find easily NTFs with optimized zeros for a given OBG specification. We can then choose the OBG as we can

Table 3.4: Theoretical improvement in SQNR for $\Delta\Sigma$ modulators without optimized zeros

Order	SQNR Improvement (dB)
3	54.83
4	58.41
5	59.57

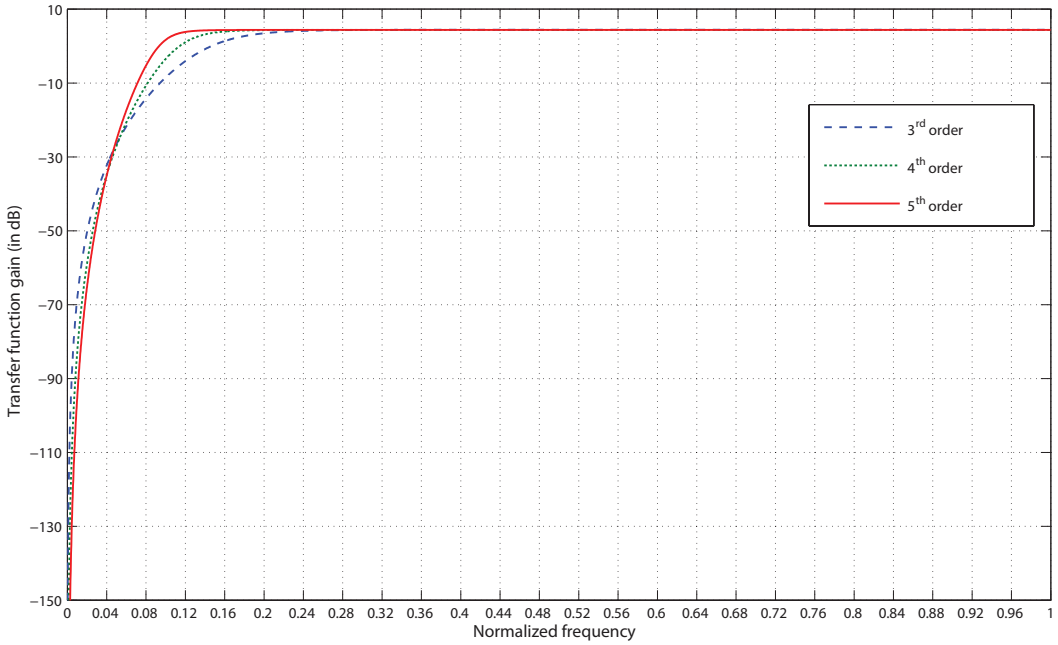

Figure 3.9: NTF frequency response without optimized zeros

iteratively search for noise transfer functions whose LTFs have a gain of unity. There is no difficulty in doing this for odd-order modulators. However, for even-order modulators with optimized zeros, there is no zero at $z = 1$. Thus, to implement these transfer functions, the required external feedback loop would have to be of the same complexity as it would be for the next higher odd-order modulator,which would give a better performance than the even order modulator. If we are forced to build even-order modulators, then we should keep two zeros at $z = 1$ and optimize the other zeros.

Once again in all three cases, the OBG was found to be close to 1.66. The properties of the NTFs and their loop-filter implementations are shown in Table 3.5 on page 34, Table 3.6 on page 34 and Table 3.7 on page 34.

Table 3.5: Maximally-flat NTFs with optimized zeros

Order	OBG	NTF
3	1.6719	$\frac{(1-z^{-1})(1-1.99z^{-1}+z^{-2})}{(1-0.6017z^{-1})(1-1.389z^{-1}+0.5916z^{-2})}$
4	1.6680	$\frac{(1-z^{-1})^2(1-1.989z^{-1}+z^{-2})}{(1-1.353z^{-1}+0.4656z^{-2})(1-1.636z^{-1}+0.758z^{-2})}$
5	1.6614	$\frac{(1-z^{-1})(1-1.995z^{-1}+z^{-2})(1-1.987z^{-1}+z^{-2})}{(1-0.73z^{-1})(1-1.522z^{-1}+0.599z^{-2})(1-1.73z^{-1}+0.821z^{-2})}$

Table 3.6: LTFs for maximally-flat NTFs with optimized zeros

Order	LTF
3	$\frac{z^{-1}(1-1.563z^{-1}+0.6441z^{-2})}{(1-z^{-1})(1-1.99z^{-1}+z^{-2})}$
4	$\frac{z^{-1}(1-0.7982z^{-1})(1-1.743z^{-1}+0.8107z^{-2})}{(1-z^{-1})^2(1-1.989z^{-1}+z^{-2})}$
5	$\frac{z^{-1}(1-1.686z^{-1}+0.7168z^{-2})(1-1.834z^{-1}+0.8942z^{-2})}{(1-z^{-1})(1-1.995z^{-1}+z^{-2})(1-1.987z^{-1}+z^{-2})}$

Table 3.7: LTF implementation for maximally-flat NTFs with optimized zeros

Order	External LTF	CT External LTF
3	$\frac{0.4272z^{-1}\left(1-0.8333z^{-1}\right)}{\left(1-1.99z^{-1}+z^{-2}\right)}$	$\frac{0.3922s+0.07128}{\left(s^2+0.009567\right)}$
4	$\frac{0.448z^{-1}\left(1-1.757z^{-1}+0.7877z^{-2}\right)}{\left(1-z^{-1}\right)\left(1-1.989z^{-1}+z^{-2}\right)}$	$\frac{0.3989}{s}+\frac{0.0952s+0.00927}{\left(s^2+0.01128\right)s}$
5	$\frac{0.463z^{-1}\left(1-0.884z^{-1}\right)\left(1-1.844z^{-1}+0.878z^{-2}\right)}{\left(1-1.995z^{-1}+z^{-2}\right)\left(1-1.987z^{-1}+z^{-2}\right)}$	$\frac{0.4087s+0.104}{\left(s^2+0.01309\right)}+\frac{0.01952s+0.001349}{\left(s^2+0.01309\right)\left(s^2+0.00462\right)}$

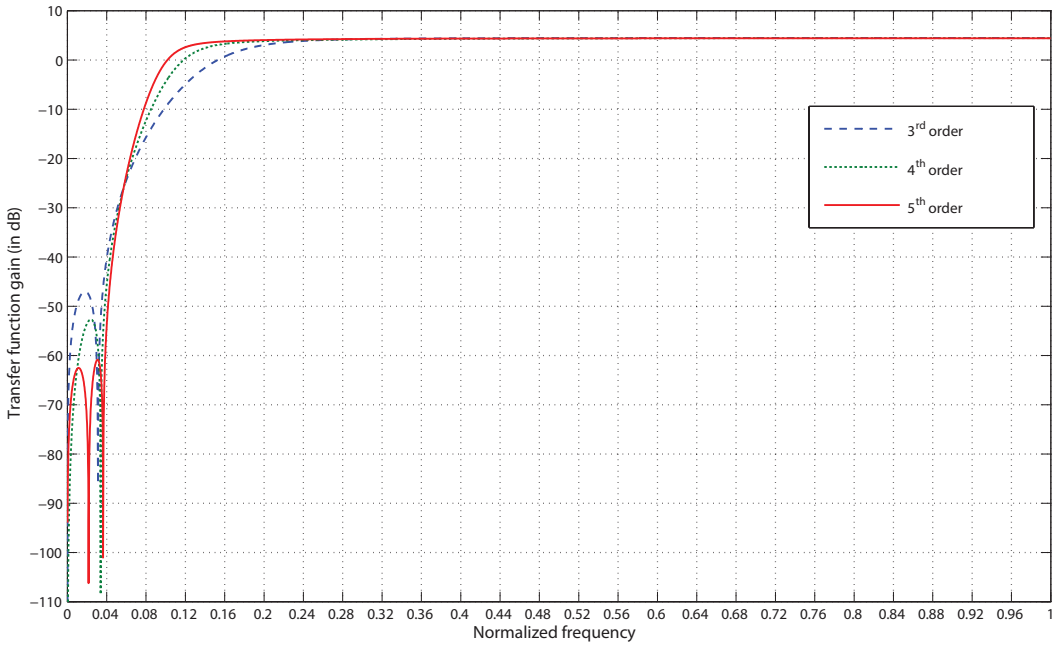

Figure 3.10: NTF frequency response with optimized zeros

The frequency response of the NTF is shown in Figure 3.10. The relative improvement in SQNR is shown in Table 3.8 on page 35. It is observed that not only are these improvements more than in the case without optimized zeros, there is also a significant benefit obtained from increasing the order of the filter.

Table 3.8: Theoretical improvement in SQNR for $\Delta\Sigma$ modulators without optimized zeros

Order	SQNR Improvement (dB)
3	62.67
4	69.32
5	78.04

3.6 Asynchronous sampling

While we can get good results using the methodology described previously, we are still limited to an OBG of about 1.65. However, with a multi-bit quantizer, we can have NTFs with an OBG of up to 3, which can shape the quantization noise much better. Indeed, we for a fifth order transfer function, an NTF with OBG of 3 gives an improvement of about 30dB compared to an NTF with an OBG of 1.65. Thus, this a limitation we would like to eliminate.

Normally the external added loop filter always have a delay of at least one cycle, as we have assumed in the preceding section. This is to satisfy the requirement that there should not be any delay-free loops. However, in this case, since the quantizer has an internal delay, this is not a necessary requirement in our case, since we will still not have a delay-free loop. However, this would mean that there would have to be at least a small delay between the clock edge controlling the sampling by the register and the clock edge for the sample and hold. Since these clocks are no longer synchronized, we shall call this *asynchronous sampling*.

3.6.1 Effect of asynchronous sampling on the VCO transfer function

The VCO quantizer quantizes the phase accumulated in the time-interval between two rising edges of the clock controlling the register. When the sample-and hold runs off a delayed clock, for one part of the register cycle , the rate of phase accumulation, which is the frequency, is controlled by the data from one sample value of the controlling voltage, whereas for the rest of the register cycle, the frequency is controlled by another sample value. This is illustrated in Figure 3.11 , where we show this effect taking place on a generic VCO quantizer.

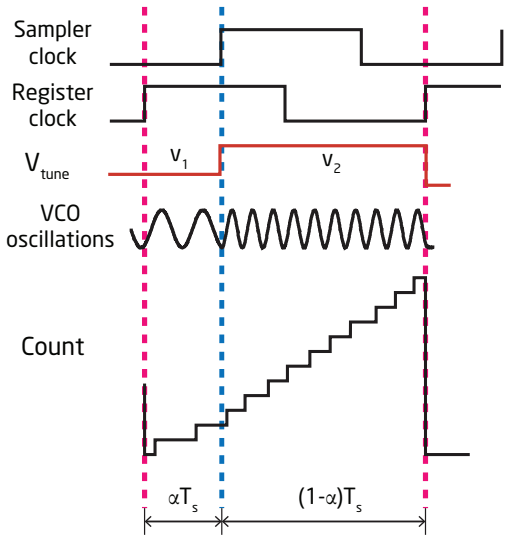

Figure 3.11: Asynchronous sampling in sampled-input VCO quantizers

If we assume that we have a reasonably linear VCO, so that we can neglect non-linearity, then, the final phase difference wold be related to a weighted sum of the two sample values. The weights would naturally be the fraction of the Sample period for which the corresponding input value controls the VCO frequency. Let α

be the delay between the register clock edge and the sample-and-hold clock edge, as a fraction of the sampling period. Then , if the input voltage values are v_1 and v_2, then the effective tuning voltage is

$$v_{eff} = \alpha v_1 + (1 - \alpha) v_2 \tag{3.17}$$

Now, since there are two clocks, we have a choice as to which of the two clock edges begins a new sample period. If we choose the register clock as determining the start of the sample period, then, when the output gets updated at one such edge, $v_2$would have been from the previous cycle and v_1 would correspond to the cycle before that, which would mean that the transfer function of the quantizer itself would be

$$QTF\,(z) = (1 - \alpha) z^{-1} + \alpha z^{-2} \tag{3.18}$$

As mentioned earlier however, any external loop filter would no longer need to have a delay.

If we consider the sample and hold clock as marking the sample periods, then, $v_2$would have been from the current cycle and v_1 would correspond to the cycle before that, which would mean that the transfer function of the quantizer itself would be

$$QTF\,(z) = (1 - \alpha) + \alpha z^{-1} \tag{3.19}$$

However, any external loop filter would now necessarily have a delay of a at least one cycle. Essentially we have just shifted the delay from the sample-and-hold to the feedback loop. Thus, this does not affect the loop gain .

In the case of synchronous sampling, we have

$$QTF\,(z) = z^{-1} \tag{3.20}$$

In the case of the register clock based analysis, this would correspond to $\alpha = 0$. Essentially, in this case α always takes values in the open interval from zero to unity, along with zero, i.e.,

$$\alpha \in [0, 1)$$

This is because the delay to the next edge of the other clock can never exceed one cycle.

In the other case, when we analyze with respect to the sample and hold clock, synchronous sampling corresponds to $\alpha = 0$. In this case ,

$$\alpha \in (0, 1]$$

We shall use the latter convention henceforth. Then a more accurate definition of α would be the delay between the register clock edge and the next sampler clock edge at which information from the quantizer can be fed to the sampler. The inherent noise shaping does not change because of this sampling, and hence does not need to be accounted for. Thus, a suitable model for the asynchronous quantizer, similar to the one for the synchronously sampled quantizer is given in Figure 3.12.

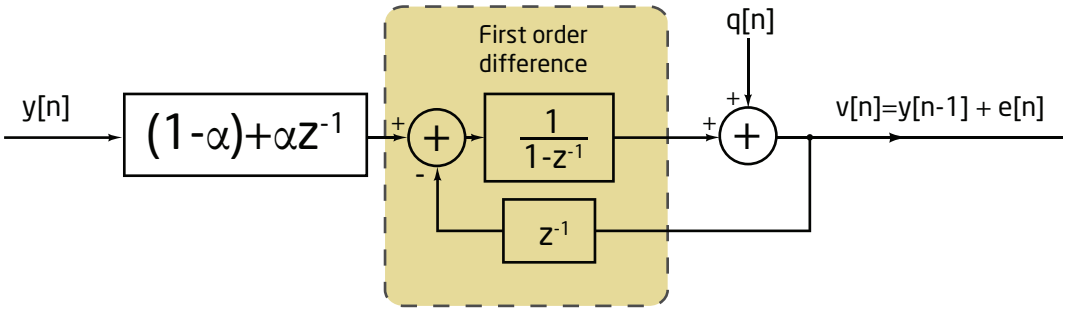

Figure 3.12: A model for the asynchronously sampled VCO quantizer

Therefore, the model for a $\Delta\Sigma$ modulator, using such a quantizer is as given in Figure 3.13. A model for a CT- $\Delta\Sigma$ modulator with the asynchronously sampled VCO quantizer is shown in 3.14.

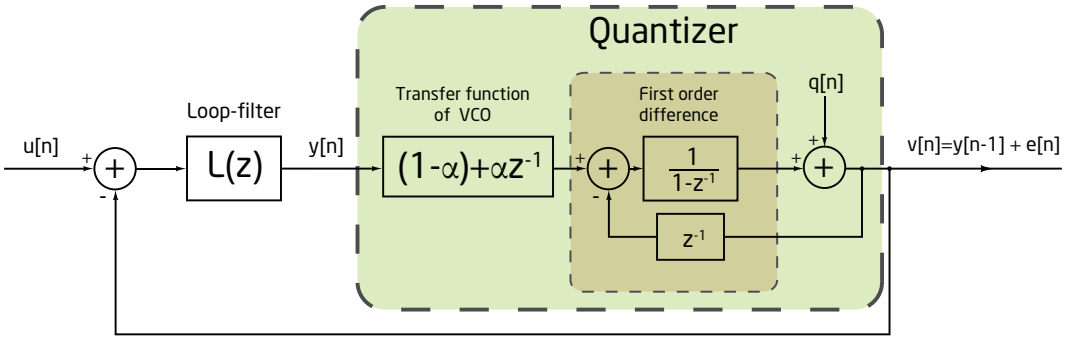

Figure 3.13: A feedback model for the asynchronously sampled VCO quantizer

Thus we can derive the expression for the effective LTF , similar to the case of

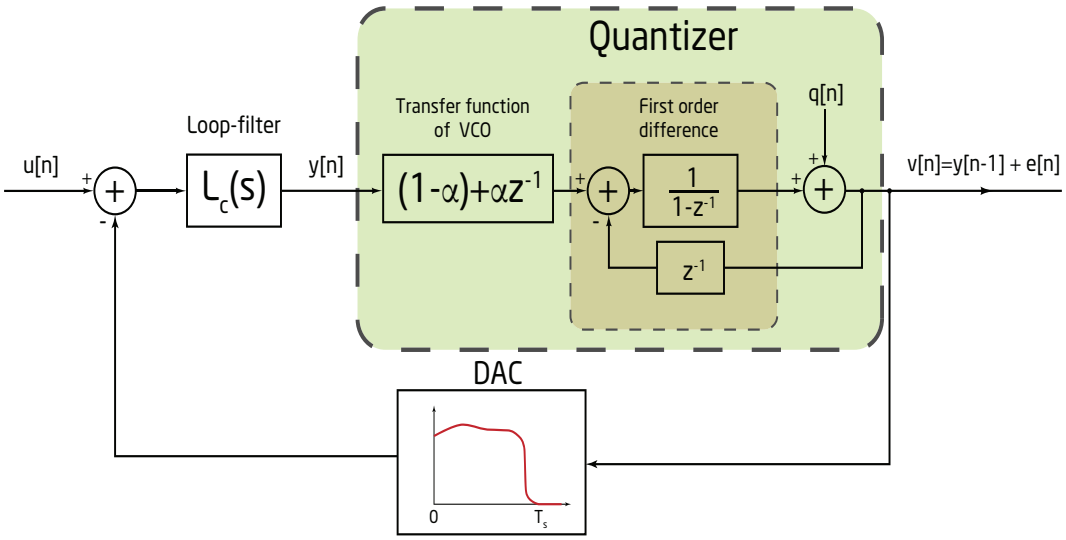

Figure 3.14: A model for a CT- $\Delta\Sigma$ modulator with the asynchronously sampled VCO quantizer

the synchronous sampler

$$L_{eff}(z) = \frac{L(z)\,QTF(z) + z^{-1}}{1 - z^{-1}} = \frac{L(z)\left((1-\alpha) + \alpha z^{-1}\right) + z^{-1}}{1 - z^{-1}} \tag{3.21}$$

3.6.2 Usable loop-transfer function for use with asynchronous sampling

We can first consider the transfer functions in the limit of low α, i.e., $\alpha \ll 1$. then

$$L_{eff}(z) = \frac{L(z)\left((1-\alpha) + \alpha z^{-1}\right) + z^{-1}}{1 - z^{-1}} \approx \frac{L(z) + z^{-1}}{1 - z^{-1}} \tag{3.22}$$

Thus it is easy to obtain the external loop transfer function with this assumption, which we shall call $L'(z)$

$$L'(z) = L_{eff}(z)\left(1 - z^{-1}\right) - z^{-1} \tag{3.23}$$

Now, we can ignore the delay and the zero and implement the loop filter. If we then add the effect of the delay so that the final effective LTF is

$$L'_{eff}(z) = \frac{L'(z)\left((1-\alpha) + \alpha z^{-1}\right) + z^{-1}}{1 - z^{-1}} \tag{3.24}$$

Now, when we consider the variation of the transfer function response, we see

that as α increases, there is increasing peaking in the transfer function response, and beyond a certain value, the NTF will have poles outside the unit circle. We can reduce the peaking by scaling $L'(z)$ appropriately to $kL'(z)$. However, even this doesn't help for higher delays. For example, with a fifth order NTF with an OBG of 3, this method leads to the poles crossing the unit circle at an $\alpha$of about 0.35, and the peaking already becomes intolerable well before this limit.

We need to find another way to make up for the quantizer transfer function. One way would be to add a pole to counter this zero. This would of course increase the order of the modulator. Moreover, the QTF has a negative real zero, which means that its impulse response has terms of alternating signs. To counter this with a continuous-time loop filter, we would need an additional resonator. This would mean that the loop-filter order would increase by two, which is quite unacceptable. Some other way of achieving good NTFs must be found.

While we have now seen the limit of low α, recall that synchronous sampling is equivalent to having $\alpha = 1$. We were able to get stable NTFs even at this extreme limit previously. So, we shall try to see how we managed this, and if we can learn from that case to other values of α as well.

In this case the LTF was always of the form

$$L_{eff}(z) = \frac{L(z)\,z^{-1} + z^{-1}}{1 - z^{-1}} = \left.\frac{L(z)\left((1-\alpha) + \alpha z^{-1}\right) + z^{-1}}{1 - z^{-1}}\right|_{\alpha=1} \tag{3.25}$$

If we define another transfer function $L_0(z)$, such that

$$L_{eff}(z) = \frac{L_0(z) + z^{-1}}{1 - z^{-1}} \tag{3.26}$$

i.e.

$$L_0(z) = L(z)\left((1-\alpha) + \alpha z^{-1}\right)$$

In effect, we have included the zero of the QTF while choosing the desired LTF itself when $\alpha = 1$. Thus, perhaps we can do the same for other values of α as well. For this to happen $((1-\alpha) + \alpha z^{-1})$has to be a factor of $L_0(z)$, which is given by

$$L_0(z) = L_{eff}(z)\left(1 - z^{-1}\right) - z^{-1} \tag{3.27}$$

We would like $L_{eff}(z)$ to be such that the NTF is still be a maximally-flat

high-pass transfer function. For this , we shall check for various values of OBG, if the corresponding $L_0(z)$ has a negative real zero and if it does, what values of αit would be suitable .

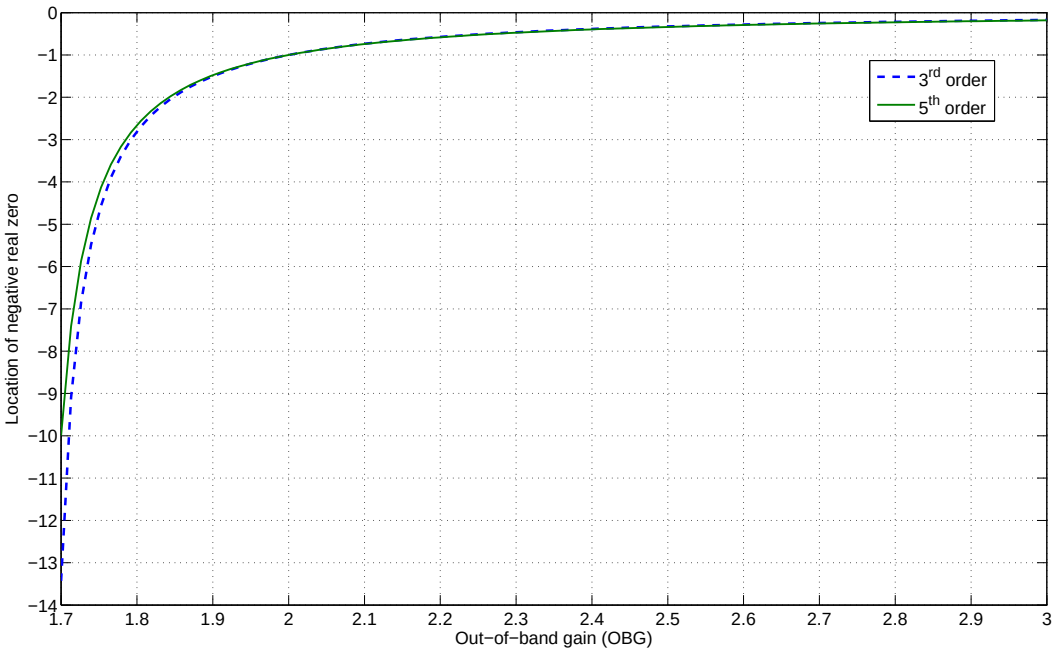

Figure 3.15: Variation of the position of the negative real zero in $L_0(z)$ with OBG

Figure 3.15 shows the variation of the negative real zero in $L_0(z)$ as the OBG varies from 1.7 to 3, in both 3^{rd} and 5^{th} order modulators. From this, we can also find the value of α corresponding to the zero. If the negative real zero is at ξ, then, we have

$$\alpha = \frac{\xi}{\xi - 1} \tag{3.28}$$

Thus, we have a relation between the OBG for which $L_0(z)$ has a negative real zero and the value of α for which the asynchronously sampled VCO quantizer itself has this zero as its transfer function. This is shown in Figure 3.16The extreme case of $\alpha = 1$ corresponds to synchronous sampling, which works with an OBG of about 1.66.

Once we have calculated the appropriate $L_0(z)$, the new loop filter will have a lower number of zeros but the same number of poles. We can easily find the continuous-time equivalent using MATLAB again. However, while the quantizer and DAC output appears notionally within the same DT sample, the DAC output is updated just before the onset of the next clock edge of the sample-and-hold. Thus, the quantizer and DAC add an excess-loop delay of one clock cycle, which needs to compensated for. But this is exactly the same as advancing $L(z)$ by a

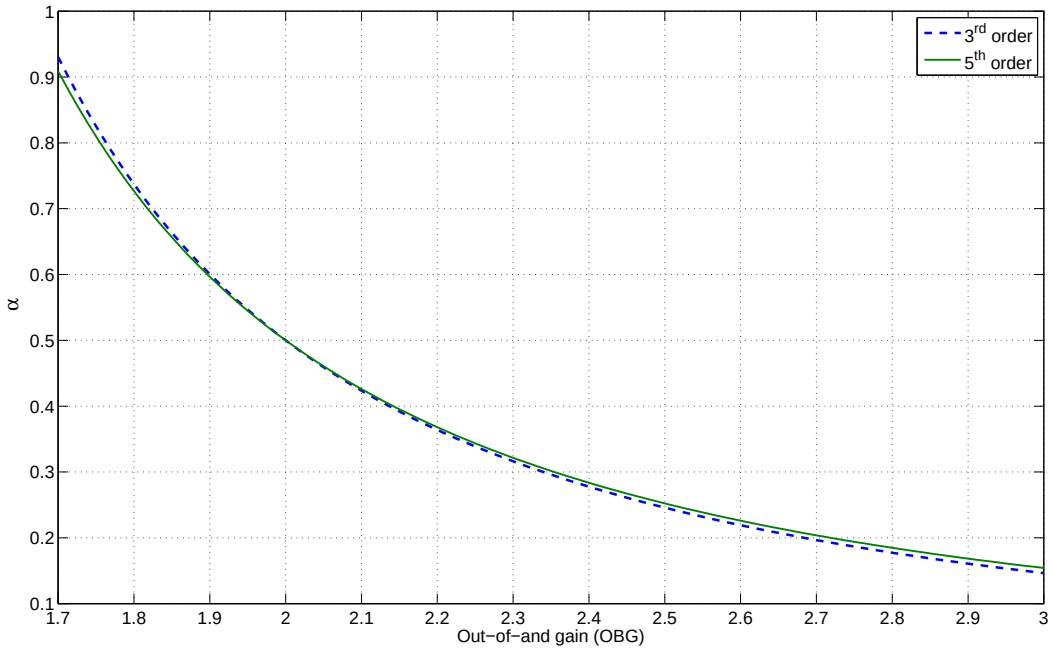

Figure 3.16: Variation of α corresponding to the negative real zero in $L_0(z)$ with OBG

cycle. Thus, the discrete-time transfer function that will have to be implemented in continuous time is actually given by

$$L(z) = \frac{L_0(z)\,z}{((1-\alpha)+\alpha z^{-1})} \tag{3.29}$$

It must be noted that there will now be a direct path in the feedback loop. It was observed that even if α was varied within ± 0.1 of the value we assume while choosing our NTF, while maintaining the external feedback transfer function, there was no excessive peaking or instability. This could be very helpful if the sample-and-hold delay is hard to characterize.

This insensitivity can also enable us achieve performance better than that predicted by Figure 3.16 for a given delay.

Thus, we have a method for obtaining higher performance than the low OBG transfer functions of the synchronously-sampled VCO quantizer ADCs.

3.7 Excess loop delay compensation with sampled-input VCO quantizers

We have assumed no delay for the digital logic or the sample-and-hold. We will now describe what steps have to be taken to compensate for these delays. We will assume that the total non-ideal delay is less than one clock cycle.

3.7.1 Sample-and-hold delay

Any real sample-and-hold circuit never changes its output to the the new input value instantly. Usually there is some sort of settling behaviour which can be crudely characterized by a delay, which we shall denote by $T_{d,SH}$. Since the input to the VCO is from the output of the sample-and hold, this needs to be accounted for, especially in the case of synchronous sampling. Otherwise, the input data from the previous cycle would still affect the input to VCO in the current cycle, changing the system to the asynchronous sampling model. The sample and hold clock needs to be advanced by $T_{d,SH}$. This would mean that CT-loop-filter outputs would have to reach their correct values earlier by the same amount of time. This is just as if there was a delay of $T_{d,SH}$ in the CT-loop-filter. This delay can be compensated for exactly as it would be in a $\Delta\Sigma$ modulator with a classical quantizer, using methods such as those described in Pavan (2008).

For asynchronously-sampled $\Delta\Sigma$ modulators, there is no sample-and-hold delay compensation, as this delay would have to be accounted for while designing the loop filter, as a part of the αcycles of delay. However, it does not affect the lag between the sample-and-hold clock and the register clock. While there is no compensation to be computed, this delay not only influences the CT transfer function, it also affects the SQNR performance of the modulator.

3.7.2 Digital logic and DAC delay

These delays are different from the sample-and-hold in that they come after the quantization. We can club then together as $T_{d,DAC}$. These delays do not affect the timing of the clock edges, however, they modify the CT transfer function, which needs to be compensated. These delays would have to be added to can again be compensated using the methods described in Pavan (2008).

Once again, for asynchronously-sampled $\Delta\Sigma$ modulators, there is no delay

compensation, as this delay would have been accounted for while designing the loop filter itself. Unlike in the case of the synchronously-sampled $\Delta\Sigma$ modulators, these delays affect the timing lag between the sampler clock and the register clock. Neglecting any delays we have not considered so far, the delay of the sampler clock with respect to the register clock would have to be very slightly more than $T_{d,DAC}$. However the value of α to be used for computation of the NTF would be

$$\alpha = \frac{T_{d,DAC} + T_{d,SH}}{T_s}$$

3.8 Quantizers without additional sampling

As we have remarked earlier, we can also eliminate the sample and hold that we had placed before the quantizer. This would eliminate the inherent one-sample delay that we had in the previous case. However there is now a virtual continuous-time integrator between the input to the quantizer and the nominal sampling quantization process we have in our model. Therefore, our external loop-filters will have to account for this as well. We will now develop a model for the external feedback as well as the intrinsic feedback in such a quantizer. For this , we will assume that there is no delay in the digital logic , the DAC or in the loop-filter.

We already have a model for the VCO quantizer as an integrator followed by a first order difference. This is shown in Figure 3.17.

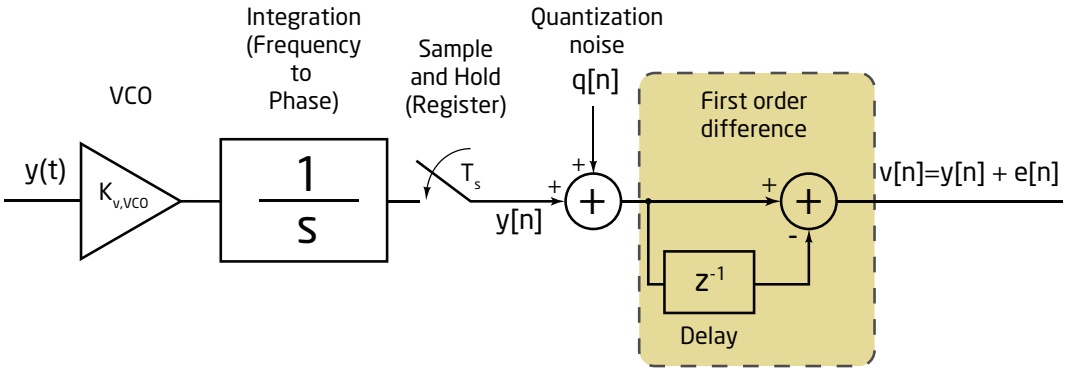

Figure 3.17: A model for the VCO quantizer without an additional sampler

Again, we can normalize the model with respect to the VCO tuning gain. We can then implement the first order difference as the result of a feedback loop. This is shown in Figure 3.18

We can then do some block diagram manipulation to send the quantization noise source within the feedback loop. Thus, the quantization noise behaviour can

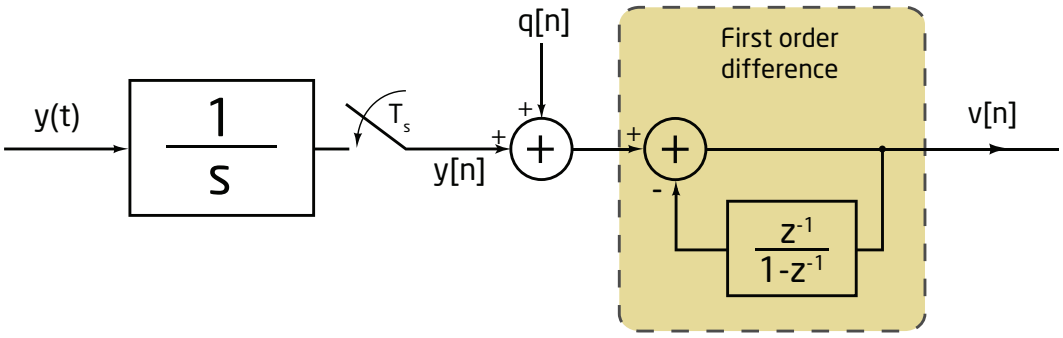

Figure 3.18: A feedback-based model for the unsampled VCO quantizer

now be studied in the $\Delta\Sigma$ framework. This model for the VCO quantizer is shown in Figure 3.19

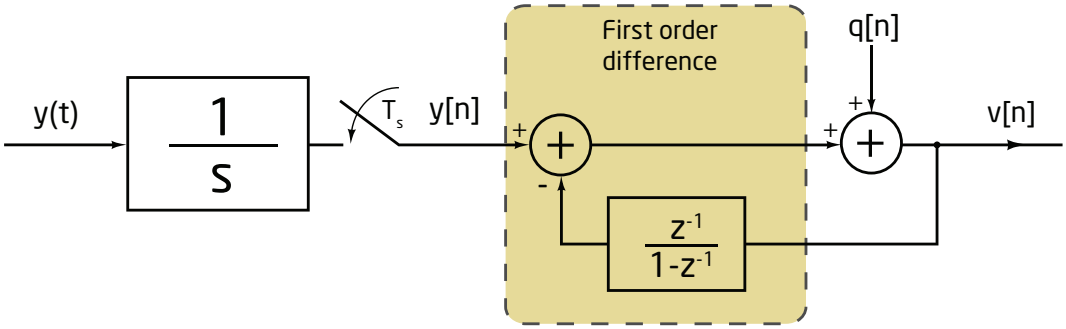

Figure 3.19: A better feedback-based model for the unsampled VCO quantizer

We then add the external feedback to the loop. The resultant model is shown in Figure 3.20. The external feedback DAC can be of any kind, either non-return-to-zero (NRZ) or return-to-zero (RZ).

We now have the the external feedback completely in the CT- domain. To combine the external feedback with the intrinsic feedback, we can then convert the transfer function to discrete-time for analysis. Thus, the effective loop transfer function will be

$$L_{eff}(z) = \mathcal{D}\left(\frac{L_c(s)}{s}\right) + \frac{z^{-1}}{1-z^{-1}} \tag{3.30}$$

where $\mathcal{D}$ denotes the transformation from continuous-time to discrete-time.

If desired, we can also convert the intrinsic feedback into continuous time feedback. We can assume a virtual NRZ-DAC inside the quantizer. For such a DAC, the feedback transfer function of $\frac{z^{-1}}{1-z^{-1}}$, which is a delayed accumulator, would correspond to the continuous-time integrator, whose transfer function is $\frac{1}{s}$. Thus, with further manipulation of the model, we can get the fully continuous-time

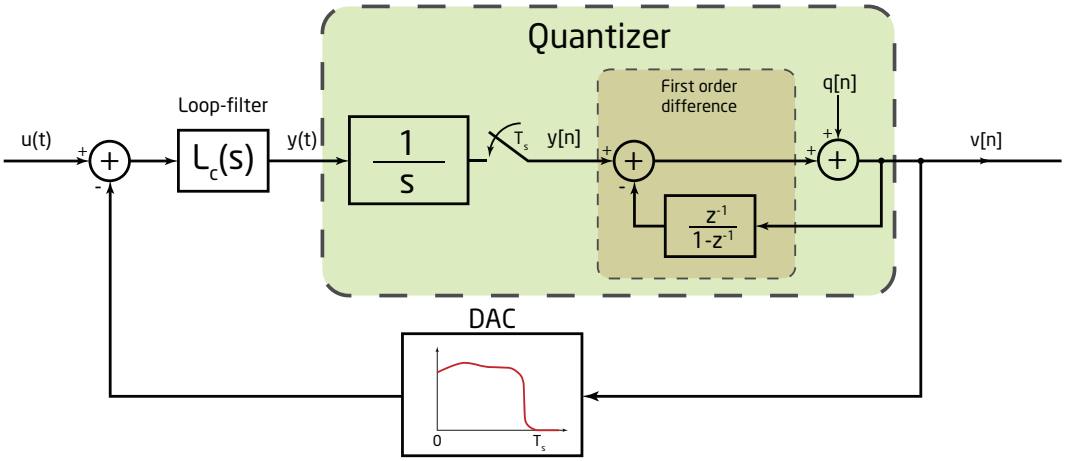

Figure 3.20: A model for a CT- $\Delta\Sigma$ modulator with the unsampled VCO quantizer

feedback model of Figure 3.21.

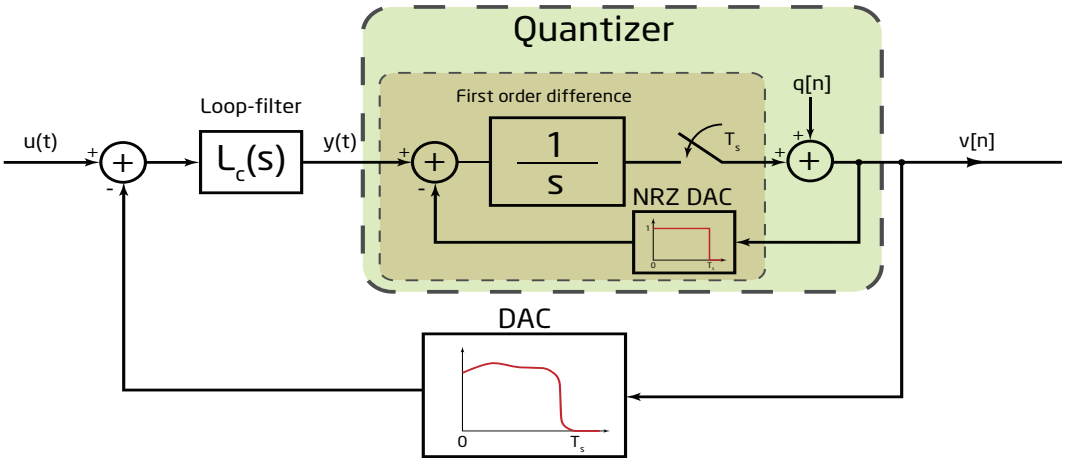

Figure 3.21: A model for a CT- $\Delta\Sigma$ modulator with the unsampled VCO quantizer, with CT internal feedback

If we are using an NRZ-DAC ourselves, then, it becomes quite simple to analyze the loop transfer function as we will then have

$$L_{eff}(z) = \mathcal{D}\left(L_{c,eff}(s)\right) = \mathcal{D}\left(\frac{L_c(s)+1}{s}\right) \tag{3.31}$$

The effective continuous-time LTF has a additional pole at $s = 0$, unless we deliberately introduce a zero at the same value to cancel it. Thus, similar to the case of sampled-input quantizer, if our desired NTF has a zero at $z = 1$, then we can achieve it with one less integrator than with a conventional quantizer.

For any desired LTF response $L_{eff}(z)$, the required continuous-time loop-filter

to be added, $L_c(s)$, is given by

$$L_c(s) = s\,\mathcal{C}\left(L_{c,eff}(s)\right) - 1 \tag{3.32}$$

where $\mathcal{C}$ denotes the transformation from continuous-time to discrete-time.

3.8.1 Advantages of the VCO quantizer without a sampled input.

This type of quantizer has some advantages over the sampled-input quantizers. Most notably, the removal of the sampler can reduce a major source of the excess loop delay. Another advantage is that the integration from frequency to phase further adds to the anti-aliasing property of the CT-$\Delta\Sigma$ modulator. For the sampled-input VCO quantizer based modulators, only the external loop-filter has the anti-aliasing property, whereas the the virtual integrator is converted into an accumulator.

3.8.2 Excess loop delay compensation.

Even without the sample-and-hold, we will have some delay due to the digital logic and the DAC. If we use an NRZ-DAC, we could once again use the technique from Pavan (2008) to calculate the new LTF. This compensation would have to be calculated not on $L_c(s)$ alone, but on $\frac{L_c(s)}{s}$, since that is the actual transfer function for the external feedback. The intrinsic feedback has no problems with excess loop-delay, since it doesn't actually have any loop.

Unfortunately, there is a problem with this method. Without the delay, $\frac{L_c(s)}{s}$ would have terms with at least s in the denominator. The compensated transfer functions would have constant terms, corresponding to a direct path to where the phase gets quantized. However, when we give any input to the VCO quantizer, we only give an input to the virtual integrator. The phase quantizer block is inaccessible to the outside. To make up for this, $L_c(s)$ would have to have terms of the form $k_0 s$. This would mean that the output of the external loop filter would have spikes. However, the high non-linearity of the VCO quantizer makes this unfeasible. The VCO tuning characteristic would just saturate for the duration of the spike, preventing the jump in the phase that we desired.

Thus, we can not use NRZ-DACs easily with such $\Delta\Sigma$ modulators. If the delay

is small enough, we can use RZ-DACs, but even they cannot do very well if the delay exceeds the off-time of the RZ-DAC. Also, to compensate for the smaller on-time, the voltage corresponding to RZ-DAC being on would have to have to be higher which would again increase the problem of non-linearity.

CHAPTER 4

Implementation and Simulation

To implement a complete CT-DSM system, we also need to implement the DAC and the loop-filter. The output of the DAC feeds directly to the input of the loop-filter, and there is no amplification from the input to the CT-DSM to the loop-filter input. Thus, any noise and distortion added by these components is equivalent to adding noise and distortion to the input. This means that the performance of these blocks is what eventually limits the ADC performance, if the CT-DSM has been designed properly. For these circuits, we shall chiefly use the designs from Singh (2010).

4.1 The feedback DAC

The usual topology for the feedback DAC in a fully differential CT-DSM is the current steering DAC. Here, the current drawn or pushed by a current source is steered to either the positive or the negative node by controlling switches based on the digital input. Because of the faster speed of the NMOS, we would usually like to switch a current that is pulled by an NMOS source by changing the state of an NMOS switch. This is shown in Figure 4.1

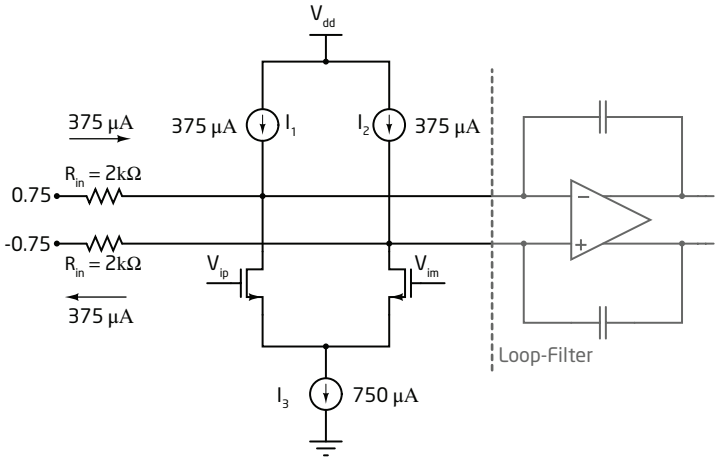

Figure 4.1: An NMOS-switched DAC (Singh, 2010)

An alternate method would be to switch both the current that is pushed into a node, as well as the current that is drawn from the node. For this we have to use

switch both the PMOS as well as NMOS current sources . Such a complementary current steering DAC, would supply the same differential current while using half as much power as the NMOS-switched DAC.This is shown in The noise contributed by the DAC would also reduce, since the major noise sources which are again the transistors of $I_1$and I_2 are themselves half as large as before.

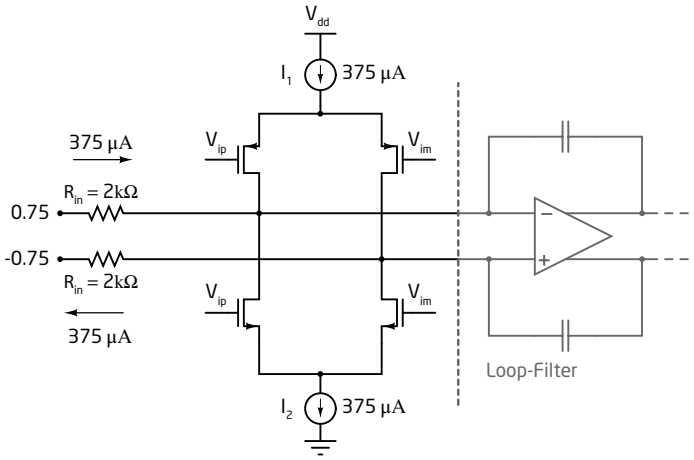

Figure 4.2: A complementary-switched DAC (Singh, 2010)

We tested the quantization noise performance of both these DACs, when they were designed to supply the same current. For this we used the modulator design from Singh (2010), which used a novel method to handle excess-loop delays of greater than one clock cycle. It was designed for a sampling frequency of 800 MHz, an excess loop delay of 1.5 clock cycles, and an OSR of 25. Since this was known to be a working modulator design, we decided to test the DACs within this $\Delta\Sigma$ loop. The output spectrum of this design with ideal loop-filter, quantizer and DAC is shown in Figure 4.3. The input signal was a sinusoid with differential amplitude 1 V.

The output power spectrum is provided in Figure4.4. In this figure and other following figures, we shall use a logarithmic frequency axis to better show the differences in inband performance. The output when we use an ideal loop-filter and DAC is also included for comparison. We see that the inband performance of the NMOS DAC is much better than that of the complementary current steering DAC. The inband SQNR for the complementary switching DAC is 88.9 dB while that of the NMOS switching DAC is 93.4 dB. This compares favourably with the ideal CT-DSM, which had a SQNR of 96.7 dB.

There are many plausible mechanisms through which the performance of the complementary switching DAC could have this performance degradation.One possible reason could be that while the DAC switches from high to low, the potential

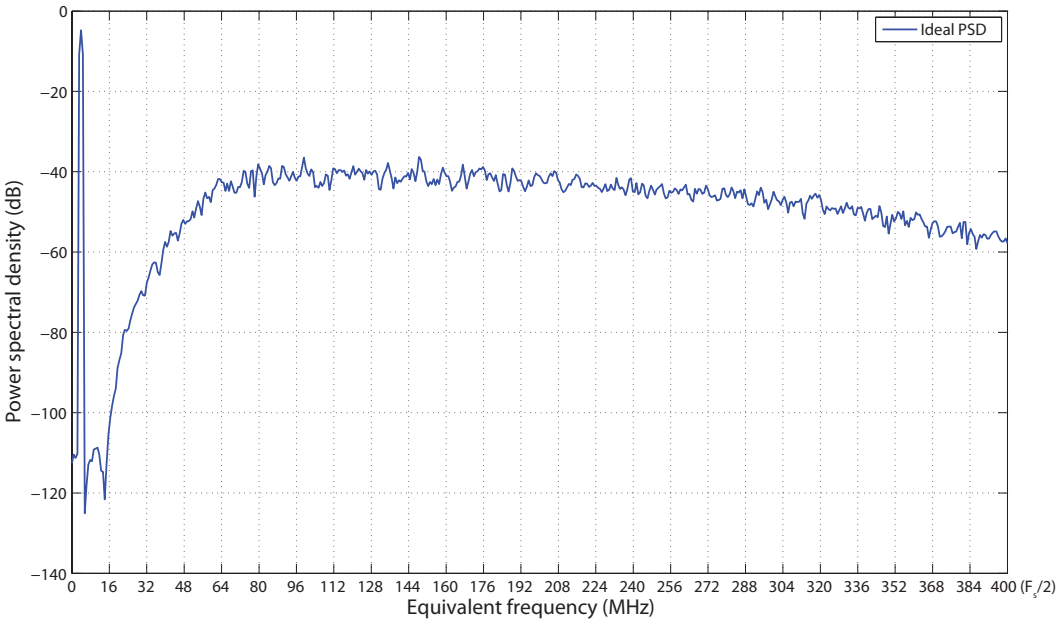

Figure 4.3: Ideal output spectrum

at the drain of tail current source varies. This could reduce the DAC current for a short time. This unwanted variation, which could also give rise to signal dependent distortion, might be reducing the SQNR. To combat this we devised a scheme which would count the number of transitions and try to keep the number of transitions constant by switching additional DAC elements added especially for this purpose. Since we did not want these dummy elements to add to the differential signal current, they have to be used in pairs, whose nominal currents cancel leaving only the switching current. Because we have to use this method in pairs, the number of extra transition we introduce will always be an even number. So, we will have k total transitions if the number of transitions in the actual DAC is even and $k + 1$ total transitions if the number of transttions in the actual DAC is odd.Thus the variation in the number of switching current would be reduced to one. This method would make a majority of the switching current variation seem like a simple DC offset. In the $\Delta\Sigma$ modulator, since the number of elements switching very rarely exceeds four, we would need only four dummy elements. We simulated such a system, but inexplicably, the performance actually significantly deteriorated as seen in Figure 4.5. The SNDR had degraded to 80.8 dB, so we abandoned this method. Perhaps it could be tested by using pairs of current sources of half the size, so that the effective number of transitions is kept exactly constant.

To test another mechanism of degradation, instead of directly feeding the DAC current to the loop-filter op-amp, we split the two apart. The DAC outputs were

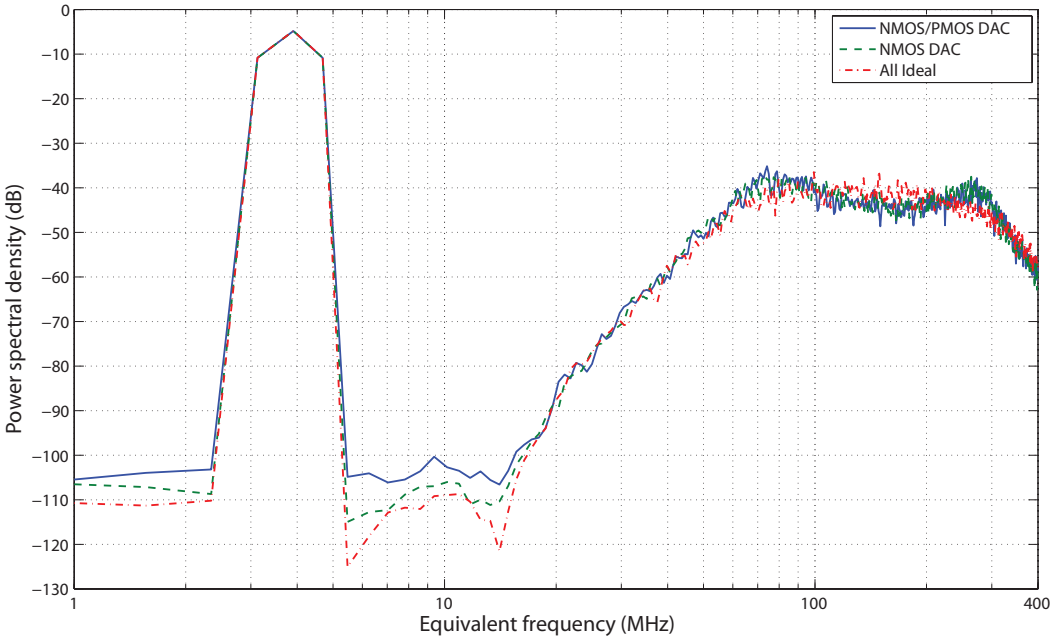

Figure 4.4: Comparison of DAC performance

connected to ideal voltage sources maintained at the common -mode voltage. The op-amps were then fed the current passing through the voltage sources by means of a current controlled current source. The result of this simulation is shown in Figure 4.6 along with prior results for comparison. We see that the performance is very close to the ideal CT-DSM, with an SQNR of 94.2 dB. This means that the degradation was primarily due to the effect voltage variation at the virtual ground of the op-amp on the DAC current sources.

Thus, to improve the performance, we can also try other means to reduce the voltage variation at the op-amp inputs. A simple method for this would be to increase the gain of the first op-amp in the loop filter. So, instead of scaling up the DAC current to make an NMOS switching DAC, we can scale up the op-amp current consumption instead. The result of scaling up the op-amp by a factor of two is given in Figure 4.7. This was found to have an SQNR of 90.6 dB

We have also considered the effect of additional parasitic capacitances which will be added when we layout the circuit on the NMOS DAC. We see that the SQNR has decreased. scaling up the op-amp only slightly reduces the damage. The SQNR without the scaled-up op-amp was 91.7 dB, whereas with the doubled up op-amp, it was 92.0 dB

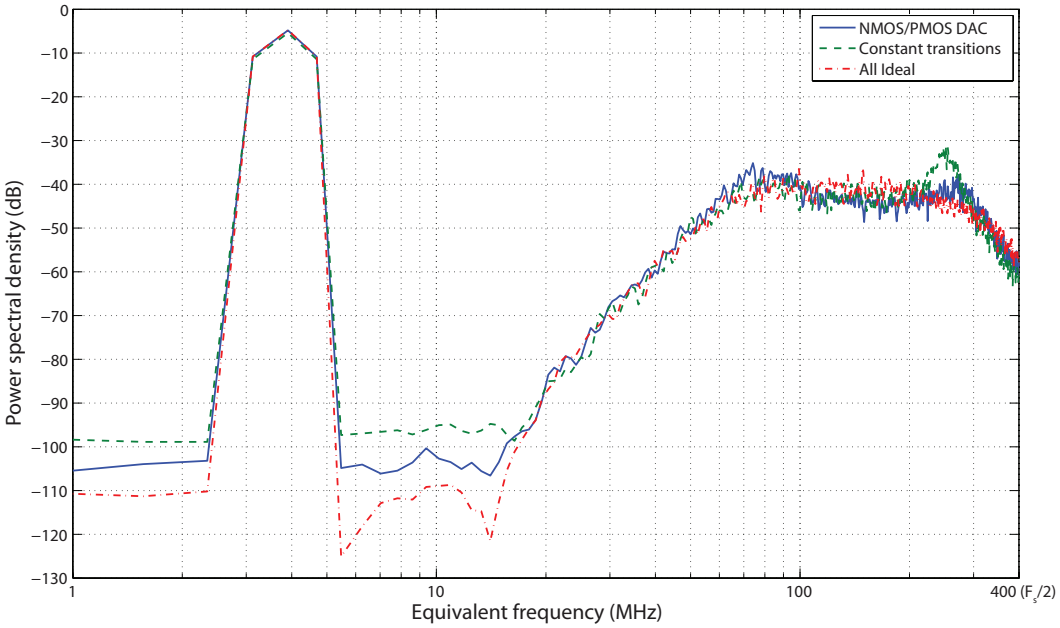

Figure 4.5: DAC performance with forced near-constant transitions

4.1.1 Noise performance

When we consider the noise performance, however, the tables are turned. The input-referred inband noise PSD of the two DACs is given in Figure4.9 while the noise of the first op-amp of the loop-filter is given in Figure 4.10. Because of the high gain of the first op-amp in the inband frequencies, we can ignore the noise contributions of the other op-amps in the loop-filter. We see that the noise performance of the NMOS-switched DAC is about 3 dB more the the complementary-switched DAC. The noise power inband for the complementary-switched DAC was -86.5 dB, whereas that of the NMOS-switched DAC was -83.0 dB. The noise of the original op-amp was -87.1 dB and that of the scaled-up op-amp was 87.0 dB. So, the SNR due to thermal noise, for the input signal of strength -3 dB for the complementary-switched DAC with a scaled-up op-amp was 80.7 dB whereas that of the NMOS-switched DAC, without op-amp scaling was only 78.6 dB.

49% of the noise in the NMOS-switched DAC is from the PMOS current sources, which had been sized the same as in the complementary-switched DAC. Since there is no switching of the PMOS current, we can significantly increase the gate overdrive of the PMOS current source transistors, reducing this noise contribution considerably. Even so, the total noise of the NMOS-switched DAC will still exceed that of the complementary-switched DAC.

To compensate for this, we would have to increase DAC current, and reduce the loop-filter input resistance. To negate the 2.1 dB difference, we would have

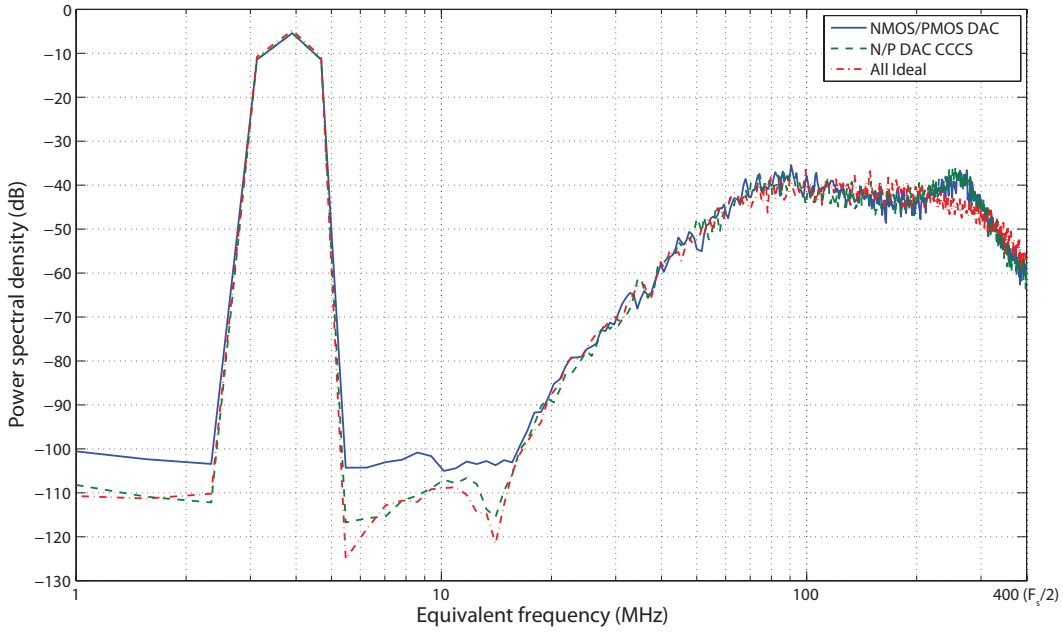

Figure 4.6: DAC performance with CCCS in loop

to increase the DAC current by 1.6 and reduce the input resistance by the same factor. This would lead to increased load on the loop filter op-amp, the effect of which on the SQNR performance should also be studied. This may need the op-amp to scaled up again, which would further increase the power consumed. Thus, the complementary switched DAC, with a more powerful op-amp would be a better option to reduce any dynamic non-linearities.

4.2 VCO quantizer based CT-DSM

We simulated the VCO based quantizer in the 180 nm UMC process. We used ideal blocks for the digital data extraction, DAC and the loop filter.

4.2.1 Normalization of loop gain.

To make sure that the loop gain had the correct values we need to account for the VCO tuning gain as well. By taking the first derivative of the VCO transfer characteristics, we identify the most linear region of the characteristics. We then take the difference between the expected VCO quantizer output values on the boundaries of this region. Rounding up this number gives us the effective number of quantization levels. Considering the maximum input range to the loop filter, we can now find the DAC element size as an input referred voltage. The average value

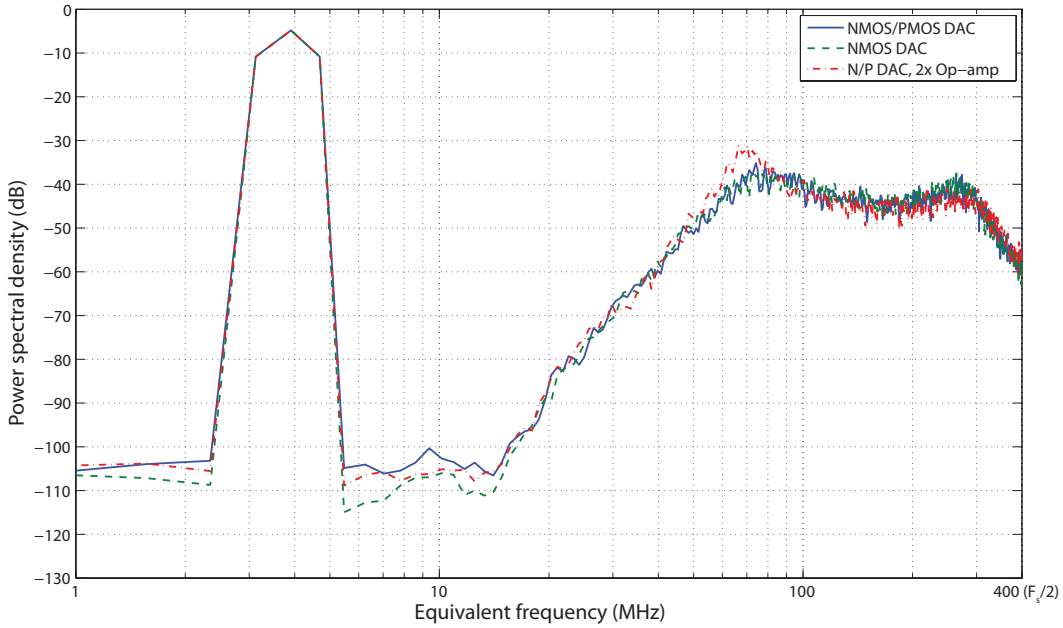

Figure 4.7: DAC performance with scaled up op-amp

of the first derivative VCO transfer characteristics gives the number of quantization levels per volt of input to the quantizer. Using this value and the DAC element size, we can now find the correct node-scaling to be applied at the output of the loop-filter, just before the VCO. Since we are using ideal DACs and loop-filters, we are free to scale the maximum input signal as we please. Therefore, we chose an input range of $\pm 1\,\mathrm{V}$. We gave an input of amplitude $900\,\mathrm{mV}$. Because of low OBG, the linear range was exceeded only rarely.

4.2.2 Fast modeling coefficients.

The values of the co-efficients in the models presented in 2.4 for a some sets of parameters of the VCOs is given in Table 4.1

Table 4.1: Coefficients for fast modeling of VCO quantizers

VCO parameters	a	n	d	c
$\zeta = 1$,load=0 fF	24.32	4.58	0.4067	0.2583
$\zeta = 1$,load=1 fF	18.31	4.435	0.4023	0.3136
$\zeta = 2$,load=1.5 fF	19.55	6.014	0.3538	0.08835

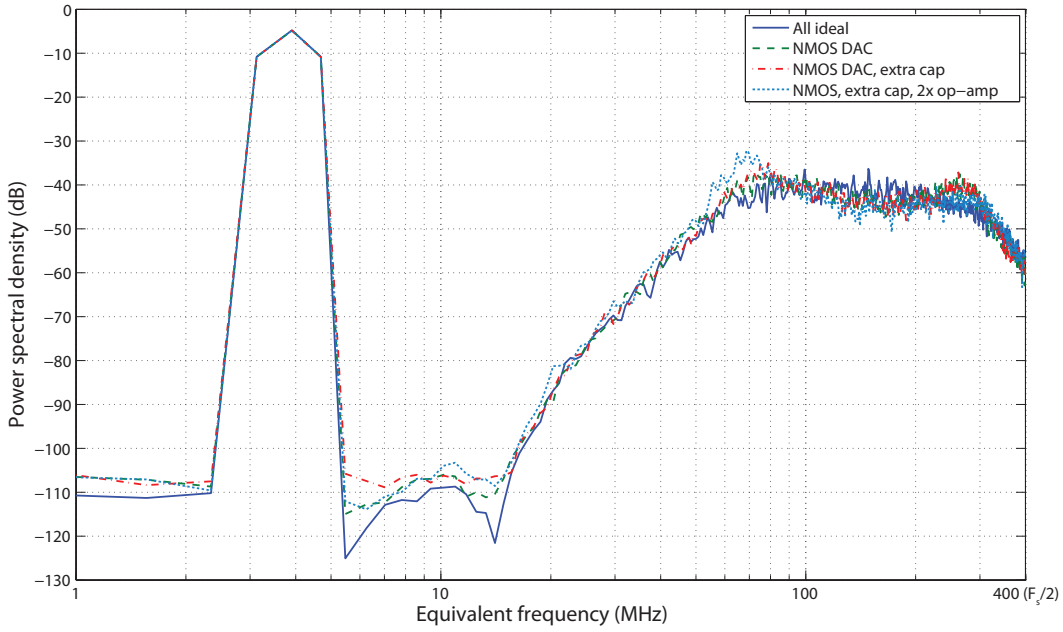

Figure 4.8: NMOS DAC performance with extra parasitic capacitance

4.2.3 4^{th}order $\Delta\Sigma$ modulator

We first designed a fourth order $\Delta\Sigma$ modulator using the synchronously sampled differential VCO quantizer without optimized zeros. We tried two sets of parameters for the quantizers. These were chosen to minimize the non-linearity over as large a range as possible. We used a quantizer with $\zeta = 1$ and no loading, and another with $\zeta = 2$ and a load of 1.5 fF. The actual effective total number of quantization levels is hard to define for a VCO quantizer, since on rare occasions, an additional inversion could take place if the initial phase is right. We shall therefore ignore these rare occurrences to decide a rough number to call the number of quantization levels. In this case the number of quantization levels was effectively 18 and 20 respectively for the two sets of parameters. The loop filter coefficients after normalization were determined from Table 3.3 on page 32. We used the model described in Section 2.4 for simulation. The output PSD is given in Figure 4.11. The SNDR and SNR are tabulated in Table 4.2.

If we optimize the zeros, considering the fact that there must be zeros at DC, then we get the result that the other two zeros must be at $\sqrt{\frac{5}{7}}$ of the upper cut-off frequency of the desired signal band. Using these zeros, the new loop filter co-efficients were determined from Table 3.7 on page 34. The output The output PSD is given in Figure 4.12. The SNDR and SNR are again tabulated in Table 4.2.

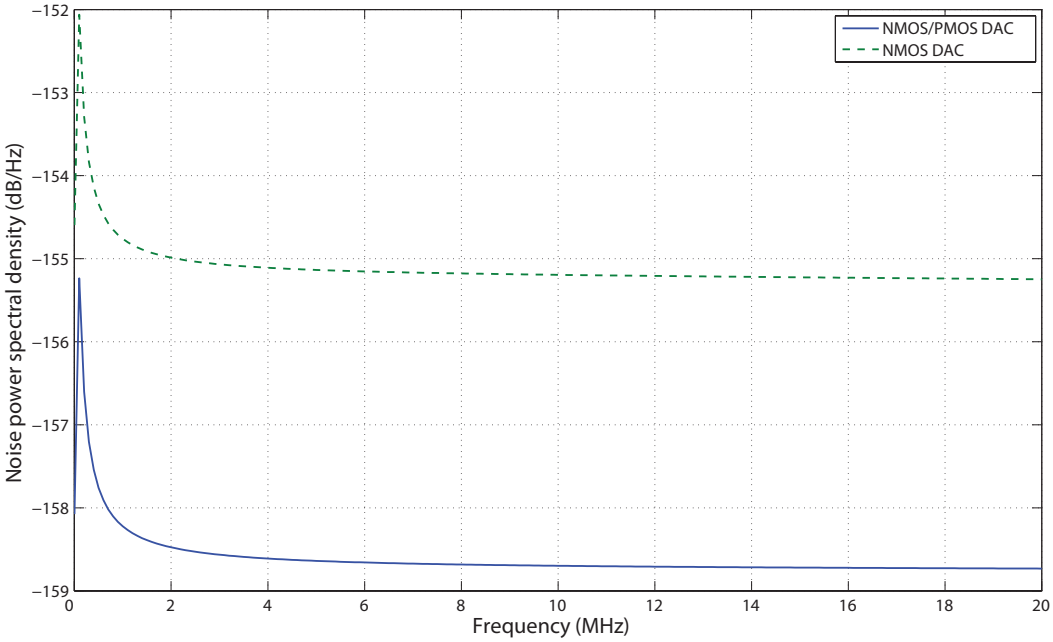

Figure 4.9: DAC noise power spectral density

Table 4.2: 4^{th}order $\Delta\Sigma$ modulator performance with VCO quantizer

Loop Filter	$\zeta = 1$,0 fF		$\zeta = 2$,1.5 fF	
	SNR (dB)	SNDR(dB)	SNR(dB)	SNDR(dB)
4^{th}order, zeros at DC	84.0	79.1	82.0	73.9
4^{th}order, optimized zeros	94.7	71.8	93.8	70.8

4.2.4 5^{th}order $\Delta\Sigma$ modulator

We also designed fifth order $\Delta\Sigma$ modulators using the synchronously sampled differential VCO quantizer. We again used the same two sets of parameters for the quantizers. We only used the NTF with optimized zeros. The loop filter coefficients after normalization were determined from Table 3.3 on page 32. We simulated using both the models from Section 2.4 as well as using the transistor level schematic of the VCO. The output PSD from the fast models is given in 4.13 and from the transistor level simulations is shown in . The SNDR and SNR are tabulated in Table 4.3.

We see that the transistor model does not seem to have inband noise shaping at all. It has been suggested that this might be because of the value of `reltol` used for the simulation might have been too high.

Finally, we also simulated $\Delta\Sigma$ modulators using single VCO quantizers. We

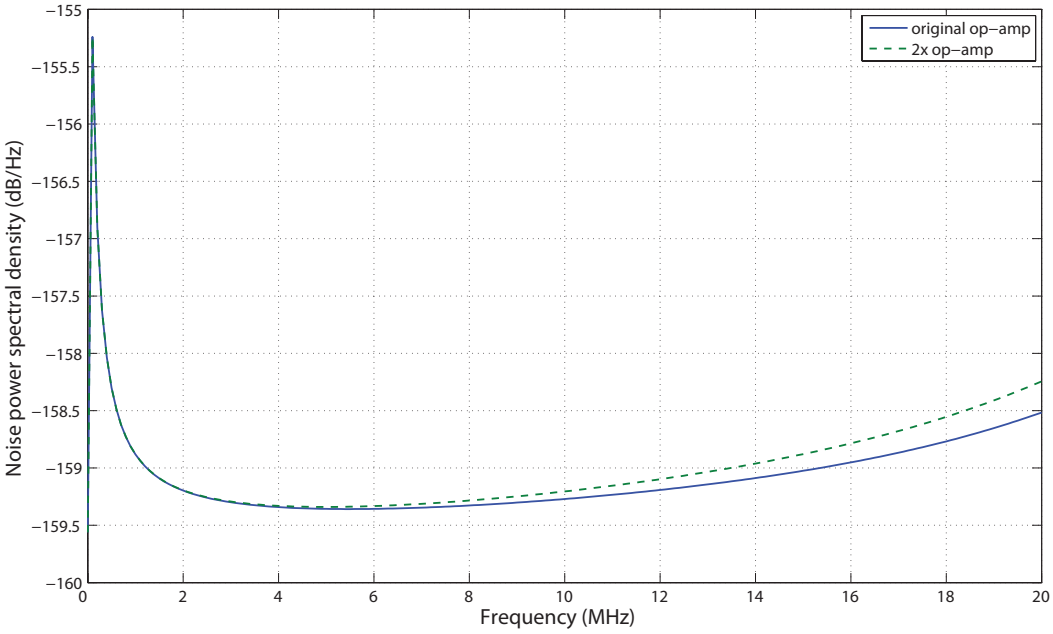

Figure 4.10: Op-amp noise power spectral density

Table 4.3: 5^{th}order $\Delta\Sigma$ modulator performance with differential VCO quantizer

Simulation	$\zeta = 1$,0 fF		$\zeta = 2$,1.5 fF	
	SNR (dB)	SNDR(dB)	SNR(dB)	SNDR(dB)
Model	106.4	84.5	105.8	82.5
Transistor	99.0	93.7	99.1	80.9

chose new sets of parameters for the quantizers, since the VCO with $\zeta = 2$ and a load of 1.5 fF was not well suited for single quantizer operation. We also artificially reduced the offset to simplify the design. The output PSD is in Figure 4.15 and the results are presented in Table 4.4. We have neglected the significant DC power while computing SNR and SNDR. A significant second order harmonic is also seen.

Table 4.4: 5^{th}order $\Delta\Sigma$ modulator performance with single VCO quantizer

Simulation	$\zeta = 1$,0 fF		$\zeta = 1$,1.0 fF	
	SNR (dB)	SNDR(dB)	SNR(dB)	SNDR(dB)
Model	99.1	74.6	99.9	77.5

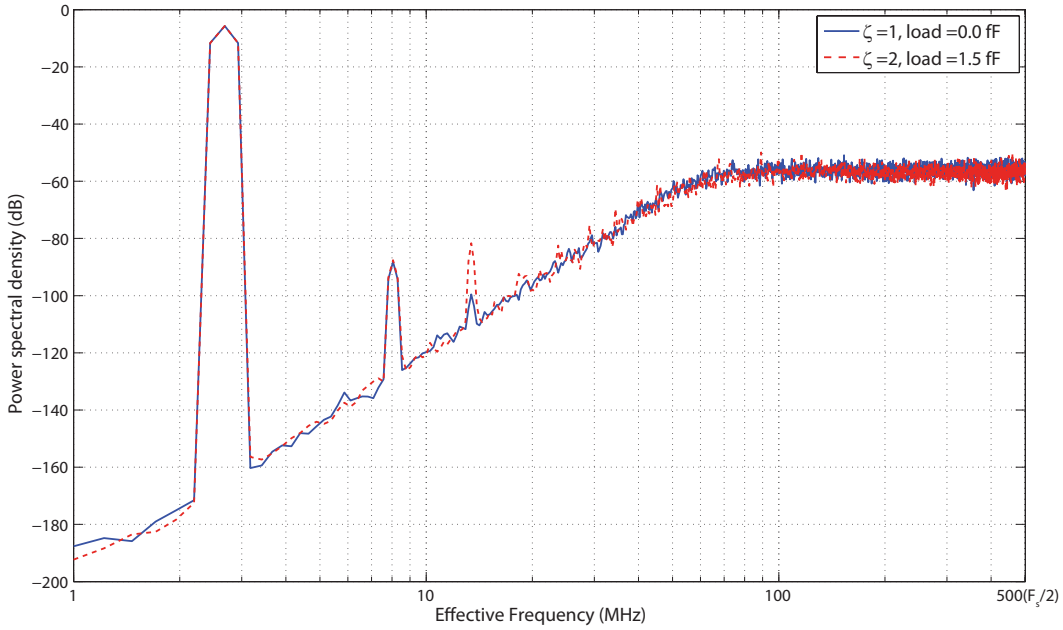

Figure 4.11: Differential VCO quantizer CT-DSM output PSD for 4^{th}order modulator without optimized zeros

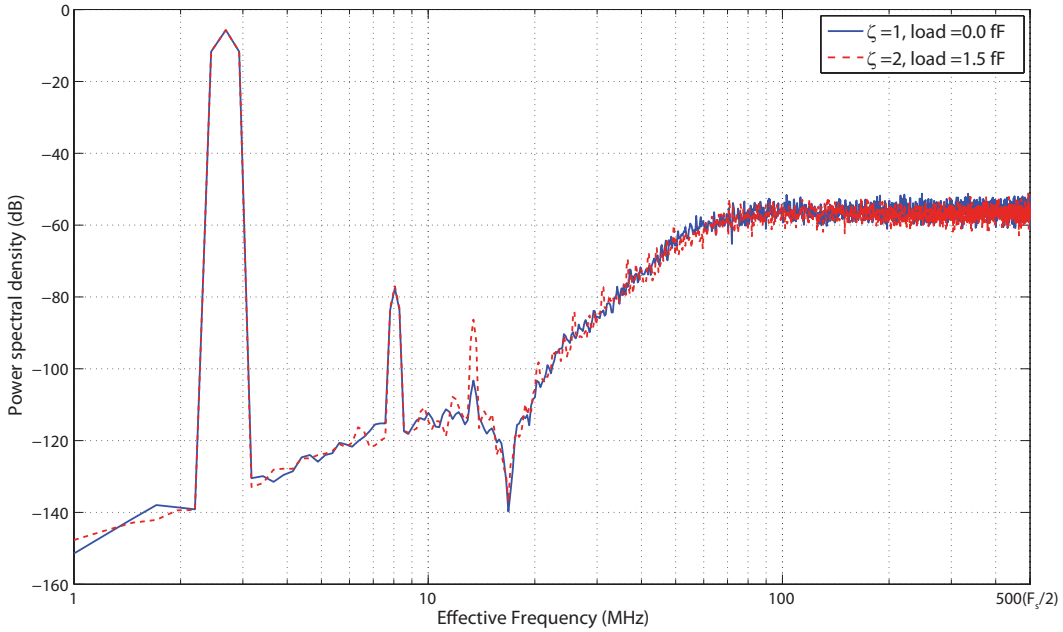

Figure 4.12: Differential VCO quantizer CT-DSM output PSD for 4^{th}order modulator with optimized zeros

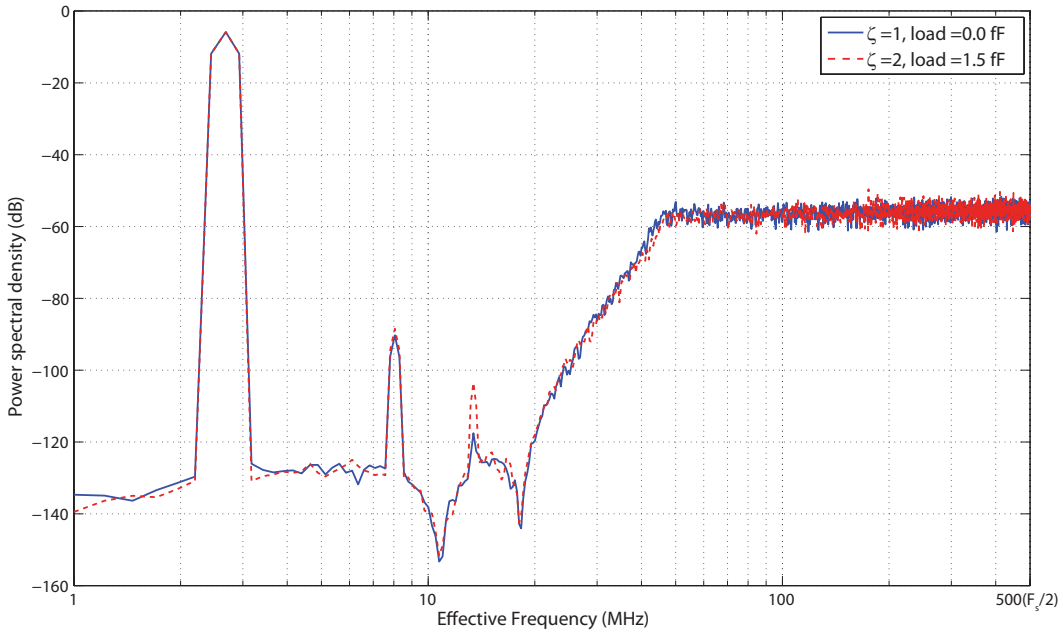

Figure 4.13: Differential VCO quantizer CT-DSM output PSD for 5^{th}order modulator with optimized zeros (model)

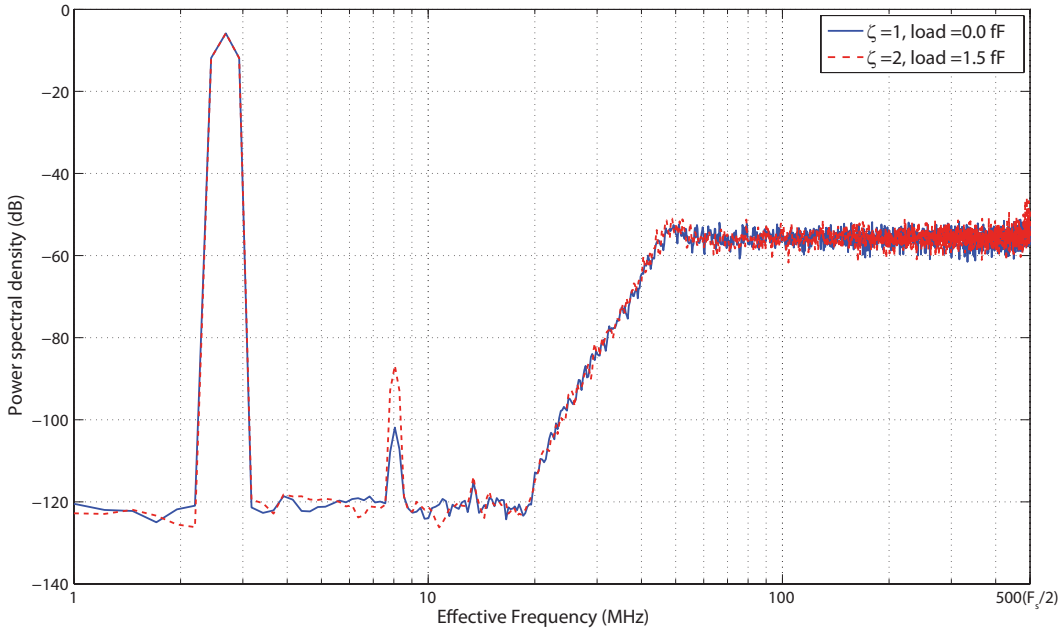

Figure 4.14: Differential VCO quantizer CT-DSM output PSD for 5^{th}order modulator with optimized zeros (schematic)

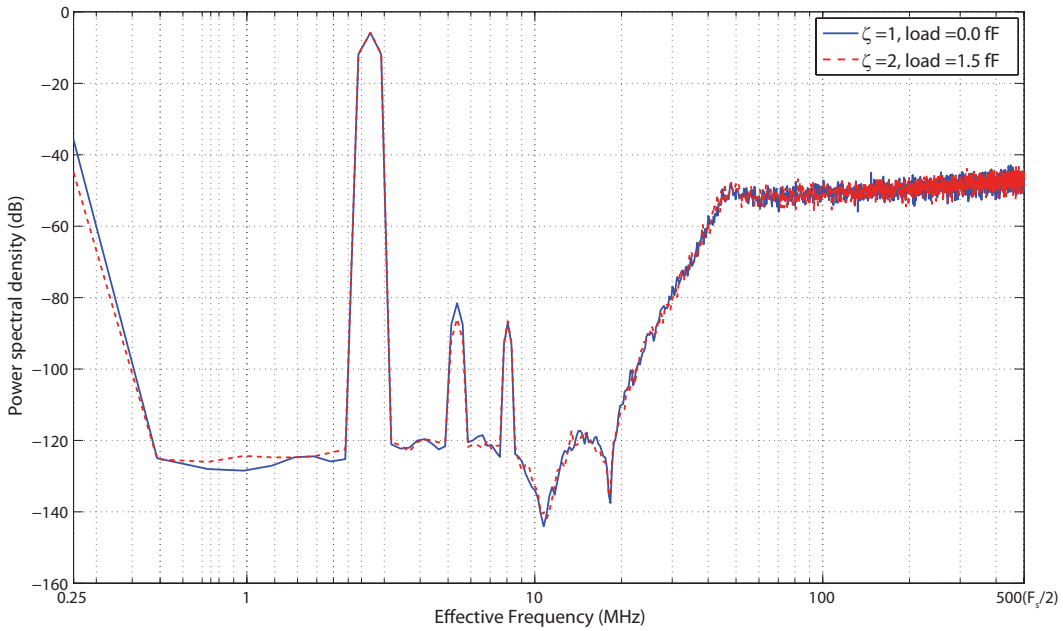

Figure 4.15: Single VCO quantizer CT-DSM output PSD for 5^{th}order modulator with optimized zeros

CHAPTER 5

Conclusions and future work

We have developed techniques to design a high resolution, low power continuous-time $\Delta\Sigma$ modulator type ADC using voltage-controlled oscillators. By studying the intrinsic noise shaping properties of VCO based quantizers, we have developed three methods of implementing CT-DSMs using these devices. We have also developed a method for fast behavioral simulation for systems using such quantizers. We have also developed a method of reducing the non-linearity and offset present in VCO quantizers, so as to simplify the design of $\Delta\Sigma$ modulators. Using these techniques, a $\Delta\Sigma$ modulators with 5^{th} order noise shaping using only four integrators was simulated

We have also studied some existing DACs and loop-filters for CT-DSMs. From simulation results we have deduced the optimal way to trade-off thermal noise, quantization noise and power consumption in these critical blocks.

5.1 Future work

While the VCO has been simulated at a transistor level and the DAC and loop-filter have also been studied in detail, the rest of the modulator has to be synthesized since they have been replaced with ideal components. Fast latches have to be developed to implement the digital logic section of the VCO quantizer. Also, a fast sample-and-hold circuit has to be designed to implement either of the the two-sampled input VCO quantizer based topologies. Most importantly, a layout has to be developed for the whole system, without which we cannot fabricate and test the performance in silicon. There are some other improvements that can be made as well.

5.1.1 Linearity enhancement

In order to minimize harmonic distortion, we are forced to reduce the input range to the VCO quantizer. However, this leads to inefficiencies in the power consumption. When we reduce the input range, the quantizer output no longer has all

outputs off for the lowest input. Thus, effectively, some DAC elements act like dummies, not contributing to the actual signal but still drawing power. What is worse, these dummy elements also contribute noise currents so that there is a considerable power wastage.

Therefore, there is lot to be gained from increasing the linearity of the quantizer. The present architecture of the VCO is also not really suitable for linear transfer characteristics. This is because the VCO frequency is roughly proportional to the current in the inverter transistors. In this topology, the VCO input voltage to tuning current relation is closer to the MOSFET square law than the linear relation we would desire. one possible way to remedy this would be to pre-distort the voltage input to the quantizer before feeding it to the quantizer. One way to do this would be to use resistors in series with a diode connected MOSFETs whose gate voltages are then taken as the VCO tuning inputs. This way the current could be made more linear, hopefully improving the quantizer characteristics.

5.1.2 Choice of switching methodology for the DAC

While we have seen that the complementary-switching DAC gives the best noise-power trade-off, because we are using the differential quantizer technique, we have some flexibility how we use the switches. Instead of using a pair of current sources for each DAC elements, we could perhaps use NMOS for the outputs of one quantizer and PMOS for the outputs of another. We could also interleave this pattern, so that consecutive elements of each ring oscillator are alternately connected to PMOS and NMOS. This would simplify the switching somewhat, since each quantizer element corresponds to one switching element rather than two .

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