Design of Low Power RF Front-End Blocks for a 2.4 GHz IEEE 802.15.4 Compliant ZigBee Transceiver

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of Low Power RF Front-End Blocks for a 2.4 GHz IEEE 802.15.4 Compliant ZigBee Transceiver**, submitted by **J. Raja Prabhu**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

This project is part of a design effort to build a direct conversion transceiver complying with the IEEE 802.15.4 (ZigBee) standard. This thesis reports the design of some low power radio frequency (RF) front-end blocks to be used in the transceiver. The designed blocks are a low noise amplifier (LNA) and quadrature downconversion mixers to be used in the direct conversion receiver and a quadrature up-converter to be used in the direct conversion transmitter. The front-end blocks were designed, laid out and verified through simulations, in UMC 0.18 μm CMOS process, and found to satisfy the system requirements with sufficient margin.

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CHAPTER 1

Introduction

The work reported here is part of a project to design a low power IEEE 802.15.4 (ZigBee) compliant transceiver to be used in battery powered wireless sensor applications. So low power design is of utmost importance. This work deals with the design of low power RF front-end blocks, namely, the low noise amplifier, downconversion mixer for the direct conversion receiver and quadrature up-converter for the direct conversion transmitter. The RF front-end will be integrated with the other blocks and will be sent for fabrication. The technology used for the design is UMC 0.18 μm CMOS process.

1.1 Organization of the Thesis

Chapter 2 introduces the problems encountered in RF reception, provides a brief introduction to the terminologies used to characterize a RF system, shows the derivation of design specifications related to the RF front-end. It concludes with an introduction to the direct conversion receiver architecture, adopted in the design.

Chapter 3 discusses the LNA requirements, topology comparison, design issues, procedure and simulation results.

Chapter 4 discusses the downconversion mixer requirements, topology comparison, design issues, procedure. Simulation results for the front-end (LNA + downconversion mixer) is given.

Chapter 5 discusses the quadrature up-converter requirements, design issues, procedure and simulation results.

Chapter 6 introduces to the use of differential inductors in RF circuits. A

method used to model the mutual magnetic coupling and parasitic capacitances is presented, along with its implication to circuit design.

Chapter 7 summarizes the work done and lists the future work to be done.

CHAPTER 2

RF Front-End Specifications and Architecture

2.1 RF wireless communication system characteristics

A unique property of any mobile wireless communication system is its large dynamic range requirement. This directly results from the desired coverage range for a given transmitted power. For the ZigBee standard, for example, the received signal power levels can vary from -85 dBm to as high as -20 dBm. It should be noted that, at a time, there will many active channels near the desired channel, transmitting at large power levels. So, the typical problem faced in the design of RF receivers is to detect weak signals in the presence of a large blocking signal nearby as shown in Fig. 2.1(a) and in the presence of two adjacent large interferers as shown in Fig. 2.1(b). This demands signal reception using highly linear and low noise amplifiers and downconverters. Nonlinearity in the signal path results in intermodulation distortion, harmonic distortion, gain compression, gain desensitization [1]. All the above effects degrade the received signal quality. For very weak signals the receiver should add little noise, so that the signal at the final detector input has sufficient signal to noise ratio (SNR).

2.2 RF system specifications

The dynamic range of a RF receiver is limited on the lower side by the noise requirements, specified using Noise Figure (NF), and on the upper side by the large signal non-linear effects, specified using HD3, IM3, IIP3, P_1dB.

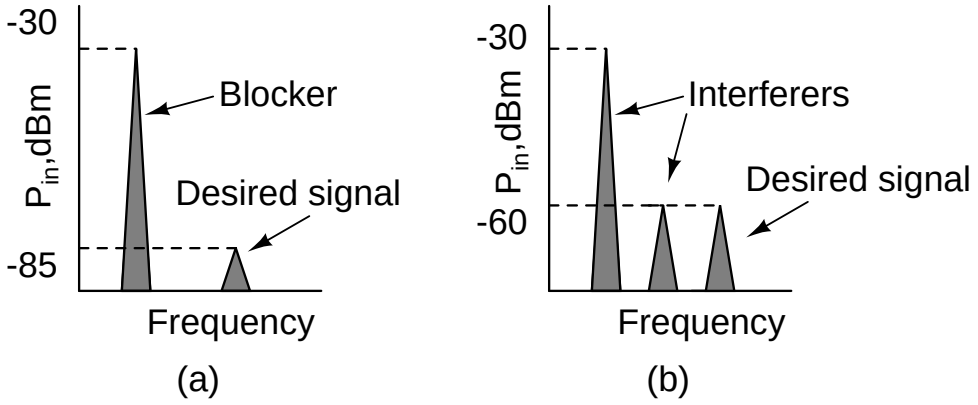

Figure 2.1: RF signal reception problem.

2.2.1 Noise Factor and Noise Figure (NF)

Noise Factor is defined as the ratio of the output noise power of the device under consideration to the noise power contributed by the thermal noise in the input termination at standard noise temperature (typically 300 K). It can also be defined as,

$$\text{Noise Factor} = \frac{\text{SNR}_{\text{input}}}{\text{SNR}_{\text{output}}} \tag{2.1}$$

$$\text{Noise Figure} = 10 \log (\text{ Noise Factor}) \tag{2.2}$$

In the case of frequency translating systems like mixers, where noise from the the image bands can fold back into the desired band two versions namely Single Side Band (SSB) and Double Side Band (DSB) noise figures are used.

For a given frequency translating system the output noise power over any desired bandwidth will be the same in both the NF calculations. The difference arises in the input termination's contribution used to divide the total output noise power. In DSB NF calculation the input termination's contribution from both the desired band and the image band are used, while in SSB NF calculation only one side band's contribution is used. As a result DSB NF will be 3 dB lower than the SSB NF.

DSB noise figure is applicable for direct conversion receivers, while SSB noise

figure is applicable for heterodyne receivers.

2.2.2 HD3, IM3, IIP3, P_{1dB}

A nonlinear amplifier is usually modelled with a power series shown below,

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + ... \quad (2.3)$$

a_0 represents the dc bias point, a_1 represents the small signal gain. All the other terms cause distortion.

If a tone at frequency f_1 is input to a such a nonlinear amplifier all the harmonics of f_1 are generated at the output as shown in Fig. 2.2(a). Such a distortion known as harmonic distortion is characterized by HDn, the ratio of the component at frequency nf_1 to the fundamental component. Harmonic distortion in some applications is tolerated if the unwanted harmonics are finally filtered out at the output.

If two tones f_1 and f_2 are input to the nonlinear amplifier all the possible frequency components given by $\pm mf_1 \pm nf_2$ are generated. Since typically fully differential circuits are used everywhere, the dominant distortion is always the third order distortion. In this case the IM3 products given by $2f_1 - f_2$ or $2f_2 - f_1$ is troublesome since it can fall in the desired signal band, as shown in Fig. 2.2(b) and cannot be removed by filtering. Intermodulation distortion is characterized by IMn, the ratio of the component due to n^{th} order intermodulation to the fundamental component.

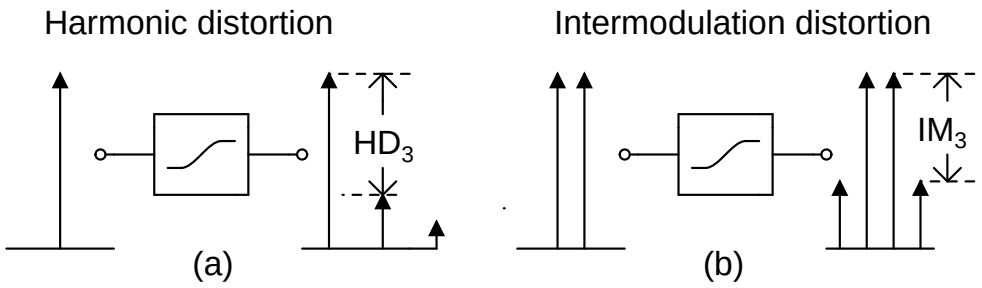

Figure 2.2: Harmonic and intermodulation distortion.

Another measure related to IMn is the input referred n^{th} order intercept point, IIPn. It is the value of the input power at which the extrapolated curves of the fundamental and n^{th} order intermodulation component meet when two closely spaced tones of equal amplitude are input to the nonlinear amplifier. It can be shown that [2], $\text{IIPn} = \text{P}_{\text{in}} + \frac{\text{IMn}}{\text{n}-1}$. Fig. 2.3 illustrates the the third order intercept point.

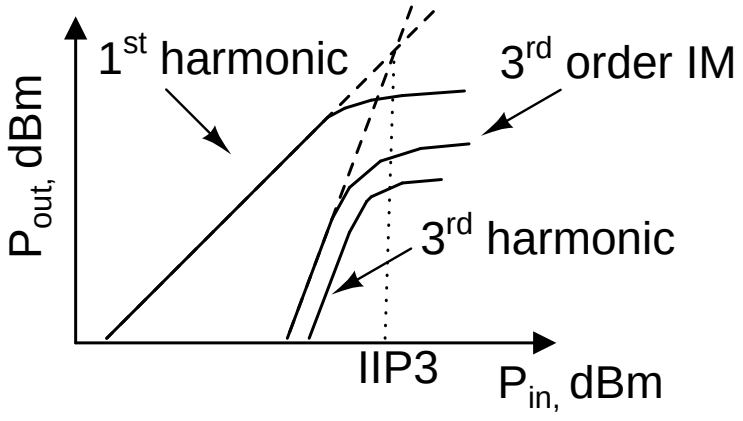

Figure 2.3: Illustration of IIP3.

Another approximate measure to characterize the compression effects is to specify a -1dB gain compression point. It is the input power level at which the fundamental component's amplitude gets compressed by 1dB.

2.3 ZigBee receiver specifications

Summary of the ZigBee RF front-end specifications, inferred from the IEEE 802.15.4 standard [3], are given in Table. 2.1.

Table 2.1: ZigBee receiver specifications

Parameter	Value
Data rate	250 kbps
System	DS-spread spectrum/TDD
Chip rate	2 Mcps
Modulation	MSK
$SNR_{detector}$	0 dB
Spectrum	2.405 to 2.485 GHz
Channels	16
Channel spacing	5 MHz
Sensitivity	$>$ -85 dBm
Maximum power level	-20 dBm
Adjacent channel rejection	0 dB
Alternate channel rejection	30 dB
Inband blocker level	-30 dBm

2.4 Derivation of the receiver design specifications

2.4.1 Noise Figure (NF) for the receiver

From Table. 2.1

Ideally 0 dB SNR at the detector input is sufficient to get the desired PER $<$ 1% [4]. So assuming 6 dB as the required SNR and 1.5 MHz as the bandwidth (BW).

$$\begin{aligned} \text{NF} &= (\,\text{Sensitivity} + 174 - 10\log(\text{BW})) - \text{SNR}_{\text{detector}} \\ &= -85 + 174 - 10\log(1.5 \times 10^6) - 6 \\ &= 21\,\text{dB} \end{aligned} \tag{2.4}$$

Leaving 5 dB margin for implementation losses, the final receiver NF is found to be 16 dB.

2.4.2 Linearity requirements for the receiver

Designing a RF front-end to handle power levels ranging from -85 dBm to -20 dBm without any gain switching leads to implementation difficulties. So it was decided to switch down the gain of the LNA at some large input power. Since the maximum power level is -20 dBm and considering the alternate channel rejection of 30 dB, the gain should be switched down at a power level greater than -50 dBm. Considering the the inband blocker level of -30 dBm, the gain was decided to be switched down by 14 dB at the input power level of -60 dBm.

With this gain switching arrangement, the front-end should be designed to handle -30 dBm (including blocker) in the high gain mode and -20 dBm in the low gain mode.

Derivation of the IIP3 requirements

For each gain setting the IIP3 requirement has to be obtained from the adjacent and alternate channel rejection specifications shown in Fig. 2.4.

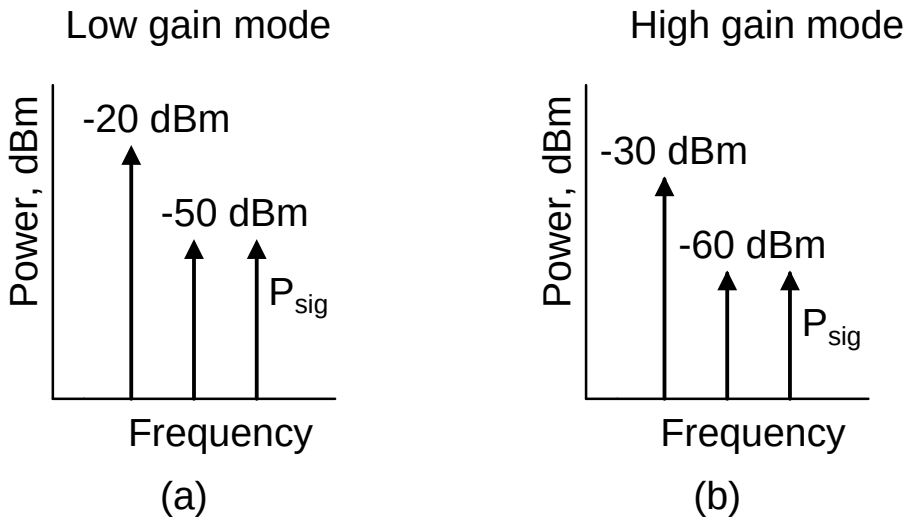

Figure 2.4: Adjacent and alternate channel interferers.

IIP3 is usually defined with two equal tones as input to a nonlinear amplifier. Consider two tones with unequal powers P_1 and P_2 input to a weakly nonlinear amplifier and let P_{IM} be the power of the intermodulation component, referred to

the input, as shown in Fig. 2.5(a). It can be shown that two tones with equal power given by $P_{eq} = P_1^{\frac{1}{3}} P_2^{\frac{2}{3}}$ will result in the generation of the same intermodulation power P_{IM} as in the previous case, as shown in Fig. 2.5(b). This property will be used to determine the IIP3 requirements.

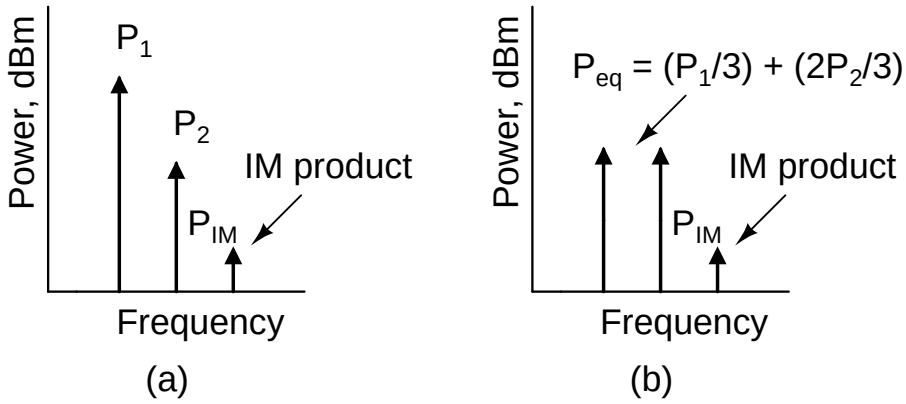

Figure 2.5: Property used to find IIP3 requirements.

In the relation $IIP3 = P_{eq} + \frac{IM3}{2}$, IM3 products generated are equated to the thermal noise level at the particular gain setting to find the IIP3 requirement.

$$\begin{aligned} IIP3 &= P_{eq} + \frac{IM3}{2} \\ &= P_{eq} + \frac{P_{eq} - P_{IM3}}{2} \\ &= P_{eq} + \frac{P_{eq} - (P_{sig} - \text{SNR}_{\text{out}})}{2} \\ &= \frac{3P_{eq} - P_{sig} + \text{SNR}_{\text{out}}}{2} \end{aligned} \tag{2.5}$$

The IIP3 values obtained using the above relations are listed in Table 2.2. NF was taken to be 21 dB in both the cases which will result in a pessimistic IIP3 value for the low gain mode. A margin of 5 dB is provided to get the IIP3 values for the design.

Also it should be noted that the front-end has to handle -20 dBm signal level in the low gain mode. So the $\text{P}_{1\text{dB}}$ should be around -20 dBm for the low gain mode. This implies, for the system with weak third order nonlinearity, that IIP3

should be around -10 dBm for the low gain mode [2].

Table 2.2: IIP3 values for the receiver in the two gain settings

Gain setting	P_{eq}	P_{sig}	$\mathrm{SNR_{out}}$	IIP3	$\mathrm{IIP3_{design}}$
Low gain	-40 dBm	-50 dBm	41 dB	-14.5 dBm	-9.5 dBm
High gain	-50 dBm	-60 dBm	31 dB	-29.5 dBm	-24.5 dBm

The gain step will be implemented at the output of the LNA. Nonlinearity in the LNA typically arises primarily due to the LNA transconductor if tuned output loads are used. There will be attenuation from the LNA transconductor input to the mixer input in the low gain mode. So IIP3 of the LNA dominates the low gain mode IIP3 of the receiver if the mixer is designed to be more linear than the LNA transconductor. So it is sufficient if the IIP3 of the LNA is slightly better than -9.5 dBm. In the high gain mode, mixer will be dominating the receiver IIP3 due to the LNA gain preceding it.

2.5 Receiver architecture

The direct conversion or zero IF architecture shown in Fig. 2.6 was selected since it can be highly integrated and can be implemented at reduced power consumption compared to other architectures [5].

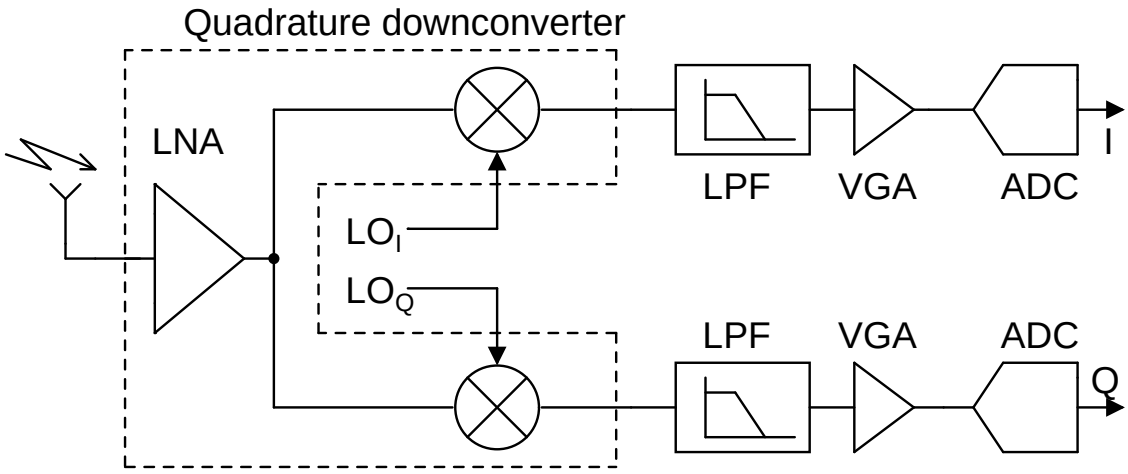

Figure 2.6: Direct conversion receiver architecture.

A fully differential implementation was chosen throughout the design to provide immunity from the noisy substrate. The noisiness of the substrate is attributed to the large switching activity associated with the frequency synthesizer, analog to digital converter (ADC), and digital to analog converter (DAC).

2.5.1 Implementation issues

- Since the RF signal is directly downconverted to baseband, the flicker noise from the mixer and the succeeding baseband blocks will be one of the important problems in the design.
- Any dc offsets created due to mismatches or Local Oscillator (LO) leakage will be in the signal band and will saturate the receiver if not corrected properly. Time varying dc offsets created in a dynamic environment should be adaptively detected and corrected.
- Even if a fully differential architecture is used, 2nd order distortion components will appear in the signal band in the presence of mismatches and corrupt the signal. So special care should be taken during the design to minimize systematic and random mismatches.
- Mismatch between the I and Q paths will result in imperfect cancellation of the image and results in SNR degradation.

CHAPTER 3

Low Noise Amplifier (LNA) Design

3.1 LNA requirements

- The Low Noise Amplifier (LNA) being the first block in the receiver chain sets the lower limit on the NF of the entire receiver chain.
- It should provide just sufficient gain to minimize the noise contribution from the other blocks following it.
- The gain should not be too high for two reasons. One reason is that a high gain at radio frequency degrades the amplifier's stability due to the unavoidable parasitic feedback loops. The other reason being the high linearity requirements imposed on the succeeding blocks, specifically the downconversion mixer.
- It should provide proper input termination to match the antenna impedance to ensure maximum power transfer and to avoid reflections at the antenna - LNA interface.
- The LNA should be sufficiently linear so that the intermodulation products generated in the presence of large interferer do not degrade the desired weak signal.
- It should provide sufficient reverse isolation to reduce the LO leakage from the mixer to the antenna. This is particularly important for a direct conversion receiver. The reason is as follows. The leaked LO signal gets reflected by moving objects, gets received by the antenna, mixes with the LO in the mixer and creates time varying DC offsets at the mixer output.

3.2 LNA specifications

A fully differential LNA has to be designed. Since the NF of the receiver chain is quite high (chapter 2), the noise figure of the LNA is relaxed. So the LNA has to be designed compromising NF for power consumption.

Table 3.1: Specifications for the LNA

Parameter	Value
Spectrum	2.405 to 2.485 GHz
S_{11}	< -20 dB
Gain	15/1 dB
IIP3	> -8 dBm
NF	< 9 dB

3.3 LNA architecture selection

3.3.1 Inductively degenerated common source LNA

One of the main specifications for the LNA is to obtain a real impedance match at the input. One method which is used almost everywhere [6; 7], for narrow band applications, is to use a inductively degenerated common source input stage as shown in Fig. 3.1(a). The input impedance looking into the gate of the transistor is shown in Fig. 3.1(b). The C_{gd} and g_{ds} are neglected for simplicity. The real part $R_{eq} = L_s \frac{g_m}{C + C_{gs}} = L_s \omega_T$ is derived from the noiseless inductor L_s. This fact is the main reason for the popularity of this architecture. The use of the additional capacitor C will be discussed shortly.

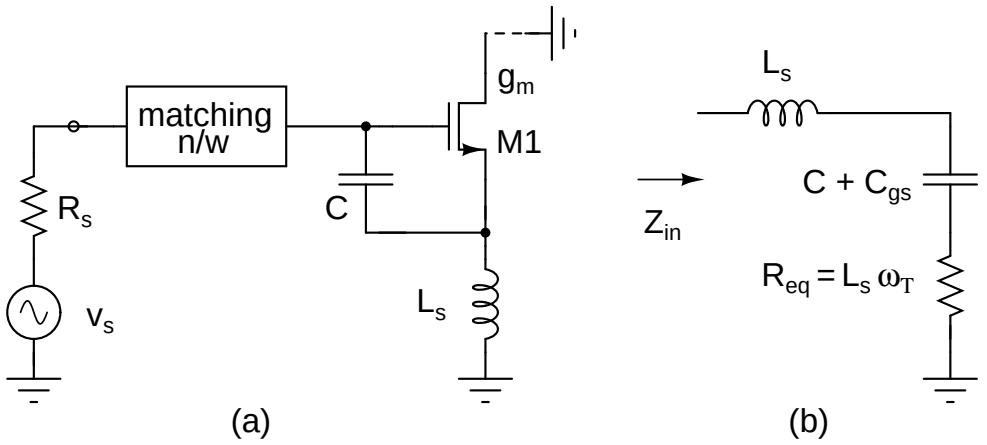

Figure 3.1: Inductively degenerated common source LNA input stage.

The Noise Factor for this configuration can be obtained from the noise contribution from all the noisy elements to the output current noise spectral density as

follows.

Contribution from R_s:

$$S_{i_{out},R_s} = \frac{4kTR_s}{4} \times \frac{R_{eq}}{R_s} \times Q^2 \times g_m^2 \tag{3.1}$$

where $Q = \dfrac{1}{(C + C_{gs})\omega_0 R_{eq}} = \dfrac{1}{L_s g_m \omega_0}$ and ω_0 is the operating frequency.

Contribution from M1: It can be shown that (refer to Appendix A), at the frequency at which impedance match is obtained,

$$\begin{aligned} S_{i_{out},M1} &= \frac{4\gamma kTg_m}{4} \\ &= \gamma kTg_m \end{aligned} \tag{3.2}$$

Here γ is a bias dependent quantity.

The Noise Factor is now given by,

$$\begin{aligned} \text{Noise Factor} &= \frac{S_{i_{out},R_s} + S_{i_{out},M1}}{S_{i_{out},R_s}} \\ &= 1 + \frac{\gamma}{g_m R_{eq} Q^2} \end{aligned} \tag{3.3}$$

The bandwidth of the impedance match is determined by Q. This value is usually kept not more than 5 so as to reduce the sensitivity of the input impedance match to tolerances in the passive components used in the matching network. So to design for a given NF with the given current, i.e. g_m and Q, R_{eq} gets fixed. Now to get the desired Q an additional capacitor C has to be added in parallel with C_{gs}. After this the L_s can be obtained from $R_{eq} = L_s \dfrac{g_m}{C + C_{gs}}$.

To maintain the desired Q at reduced power consumption results in increased values for C and L_s. This implies a reduced value of ω_T and increased die area at reduced power consumption.

3.3.2 Resistively terminated common source LNA

Another simple method for obtaining the real impedance match would be to shunt the common source input stage with a large resistor R_m (compared to R_s) as shown in Fig. 3.2, if NF is not of primary concern.

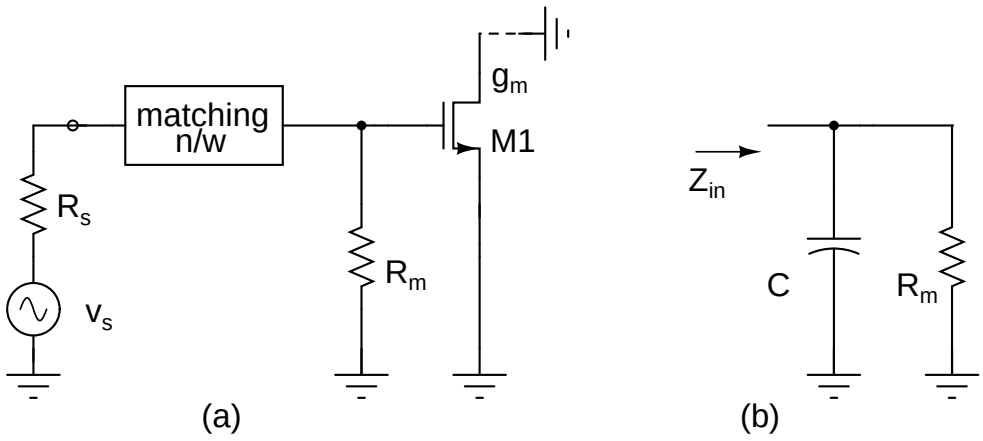

Figure 3.2: Resistively terminated common source LNA input stage.

The Noise Factor for this configuration can be obtained similarly as in the previous case.

Contribution from R_s:

$$S_{i_{out},R_s} = \frac{4kTR_s}{4} \times \frac{R_m}{R_s} \times g_m^2 \tag{3.4}$$

Contribution from R_m:

$$S_{i_{out},R_m} = \frac{4kTR_m}{4} \times g_m^2 \tag{3.5}$$

Contribution from M1:

$$S_{i_{out},M1} = 4\gamma kTg_m \tag{3.6}$$

The Noise Factor is now given by,

$$\begin{aligned} \text{Noise Factor} &= \frac{S_{i_{out},R_s} + S_{i_{out},R_m} + S_{i_{out},M1}}{S_{i_{out},R_s}} \\ &= 2 + \frac{4\gamma}{g_m R_m} \end{aligned} \tag{3.7}$$

Note that the minimum NF achievable is 3 dB due to resistive termination at the input.

Here again the bandwidth of the impedance match is determined by the Q of the matching network which is directly indicated by the gain, $\sqrt{\frac{R_m}{R_s}}$, provided by the matching network.

3.4 NF of single-ended and differential LNA

The NF expressions obtained before are for single-ended versions. If a differential version is to be obtained with the same NF, the Thevenin resistance faced by each of the inputs, for differential excitation, should be made equal to R_s. This can be achieved by a balun transforming R_s to $2R_s$ as shown in Fig. 3.3(b) [8]. Addition of such a balun provides an additional gain of 3 dB compared to the single-ended LNA.

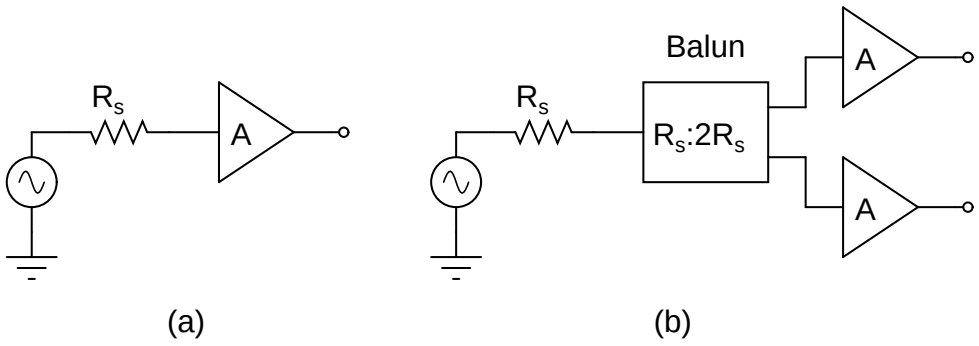

Figure 3.3: Single-ended and differential LNA.

3.5 LNA design procedure

Since the NF specification for the receiver is relaxed, the conventional inductively degenerated common source LNA will not suit the current application in terms of complexity and die area, due to the presence of L_s. So the simple common-source differential pair architecture was selected with the input being resistively terminated with a large resistor (compared to $R_S = 50\ \Omega$). With resistive termination the minimum NF achievable is 3 dB, which is acceptable.

Refer to the differential LNA simulation setup shown in Fig. 3.4.

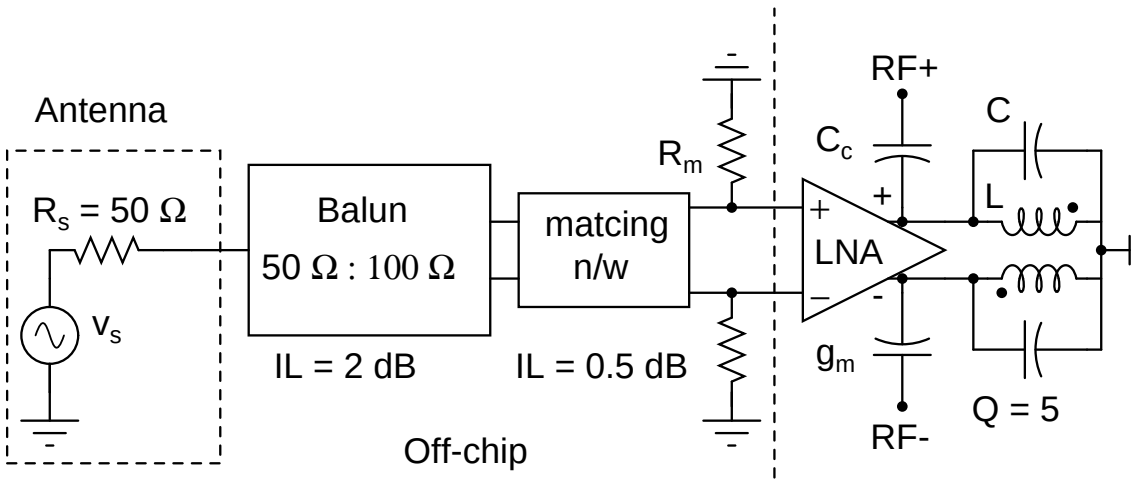

Figure 3.4: Test setup for the differential LNA.

3.5.1 Selection of the matching resistor, R_m

The gain obtained from the matching network alone, excluding the losses, is $\sqrt{\frac{R_m}{50}}$. This gain is a direct measure of the Q of the matching network. As the Q of the matching network increases, the sensitivity of the LNA input match and gain to component tolerances increases. Also the bandwidth over which S_{11} is below the acceptable value, typically -20 dB, also decreases.

This aspect is illustrated for the LC matching network shown in Fig. 3.5 for various values of the matching resistor R_m to get a 50 ohms input match at 2.44 GHz.

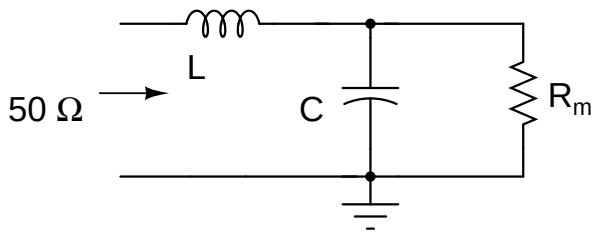

Figure 3.5: Impedance matching network used in the LNA simulation.

Refer to Table 3.2. BW refers to the bandwidth over which S_{11} is better than -20 dB. So $R_m = 900\ \Omega$, slightly smaller than 1 kΩ was selected. Another reason

Table 3.2: Selection of R_m

R_m, $k\Omega$	L, nH	C, fF	Q	BW, MHz
0.5	9.78	391.36	3	175
1	14.21	284.31	4.35	115
2	20.36	203.67	6.24	80
4	28.98	144.93	8.88	56

not to use a large R_m is to minimize stray signal pickups due to the parasitic capacitive coupling from other noise sources.

3.5.2 Selection of the LNA load

An LC tank with a finite quality factor is typically used for narrow band applications for the following reasons.

1. Desired gain can be achieved at low power since the mixer input capacitance and all the other parasitic capacitances can be absorbed in the tank.
2. It provides rejection of the out of band signals due to its selectivity.
3. It enhances the linearity of LNA since the signal can now swing above the supply rail. This advantage will be more significant as the technology scales down.
4. If differential inductors are used it also provides common-mode rejection at the LNA output.

The LC tank's quality factor is primarily determined by the inductor's quality factor, $Q = \dfrac{L\omega_0}{R_s}$. Here R_s is the equivalent series resistance of the inductor

modeling its losses. The load presented to the LNA at resonance is,

$$Z_L = (1+Q^2)R_s \simeq Q^2 R_s, \text{ for Q} > 3 \quad (3.8)$$

$$= L\omega_0 Q \quad (3.9)$$

The LNA gain, at resonance, excluding the insertion losses, is,

$$A = \frac{1}{2} \times \sqrt{\frac{100}{50}} \times \sqrt{\frac{R_m}{50}} \times g_m \times L\omega_0 Q$$

$$= \frac{1}{\sqrt{2}} \times \sqrt{\frac{R_m}{50}} \times g_m \times L\omega_0 Q \quad (3.10)$$

Here again the inductor Q is kept small so that the LNA gain variation, in the desired band, due to the inductor, capacitor tolerances is minimal. So a Q of around 5 was chosen. Now the power consumption in the LNA comes down as we increase the inductance since g_m can be reduced to get the same gain. Here it is assumed that the NF degradation due to reduced g_m is acceptable.
A differential symmetric square spiral inductor was chosen for the design for the following reasons.

1. Differential inductors occupy less area compared to two single-ended inductors which they replace.
2. Q of differential inductors is superior than the single ended inductors.
3. Additionally differential inductors provide common-mode rejection.

A differential 20 nH inductor with a Q of 5 was designed. Inductance beyond this value will be very large and have low self resonance frequency. Details about inductor modeling is given in Chapter 6.

3.5.3 Meeting the linearity requirement

The linearity of the LNA is primarily determined by the linearity of the transconductor alone since the use of the LC load provides more than sufficient headroom

at the output.

A simple NMOS differential pair transconductor was selected due to its good high frequency performance and ability to provide common-mode rejection.

It can be shown [2], assuming square law behavior for the MOSFETs in saturation, that the IIP3 for the differential pair transconductor is,

$$V_{IIP3} = 4\sqrt{\frac{2}{3}}(V_{gs} - V_t) \tag{3.11}$$

From simulations the overdrive, $V_{gs} - V_t = V_{ov}$, required to meet the linearity specifications was found.

3.5.4 Fixing the transconductance, g_m

Once V_{ov} is fixed, the differential pair is impedance scaled, i.e. scaling both I_{bias} and device width, to get the desired LNA gain of 15 dB.

3.5.5 Cascode stage and variable gain implementation

Cascode stage is essential to provide sufficient isolation between the LNA LC load and the input matching network. It also reduces the effect of C_{gd} on the LNA performance.
The LNA will be operating in two gain modes : 15 dB / 1 dB described in Chapter 2. So a gain step of 14 dB is to be implemented. This can be incorporated in the cascode stage by steering $\frac{4}{5}$ I_{in}, from the transconductor, to the supply in the low-gain mode. Refer to Fig. 3.6.

M3 and M4, whose gates are driven by CMOS inverters, are 4 times wider than M1. So when g = 1.8 V (high-gain mode), I_{in} is completely steered to the load. When g = 0 (low-gain mode), only $\frac{1}{5}$ I_{in} reaches the load, which results in a well defined 14 dB gain step, independent of process variations. Also by this arrangement the impedance seen by the drain of the differential pair transistors remains the same in both the gain modes. This implies that the input impedance

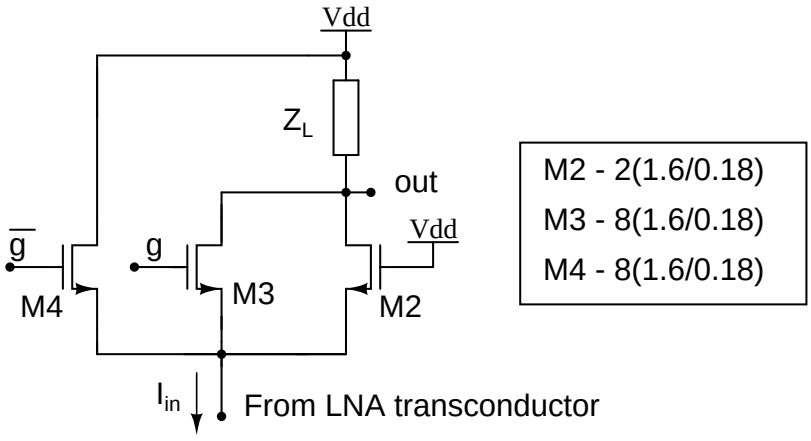

Figure 3.6: Variable gain implementation in the cascode stage.

match also remains the same in both the gain modes. The complete schematic of the designed LNA is shown in Fig. 3.7.

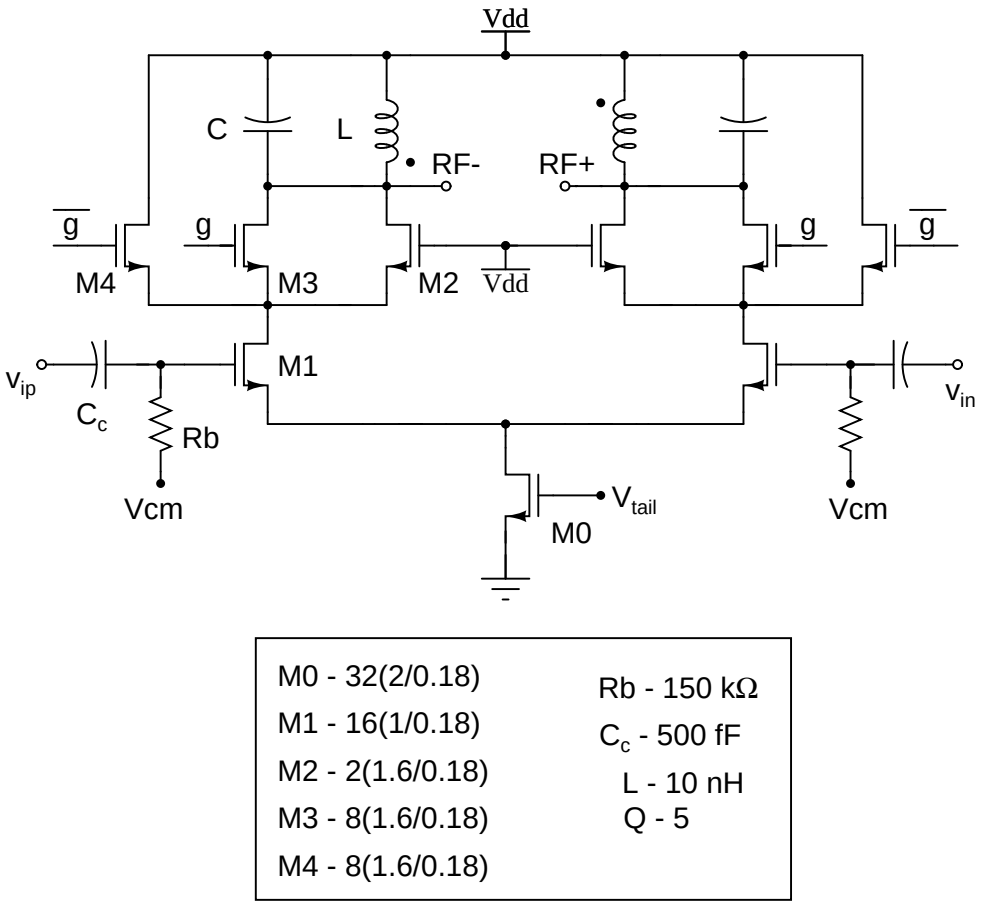

Figure 3.7: Schematic of the differential LNA.

3.6 Fixed transconductance bias generation

From equation 3.10, the LNA gain is directly proportional to the transconductance, g_m and quality factor, Q. If the LNA is biased with a constant current the variation of g_m with process and temperature was found to be around $\pm$ 20% around the nominal value. This is mainly due to the large variation of mobility over temperature and process. To reduce this variation, a fixed transconductance bias circuit was designed to servo the transconductance to a stable external resistor.

3.6.1 Basic fixed transconductance bias cell

The basic fixed gm bias generation cell is shown in Fig. 3.8 [9]. Assuming all the

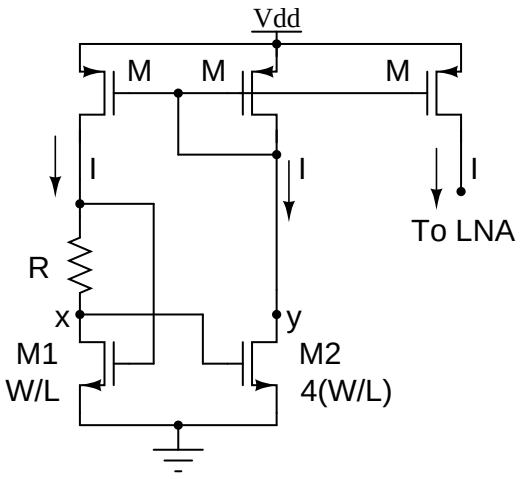

Figure 3.8: Basic fixed g_m bias generation cell.

transistors are in saturation, using the square law equation for the MOSFET, the voltage drop across the resistor R is,

$$\begin{aligned} IR &= V_{gs1} - V_{gs2} \\ &= (V_t + V_{ov}) - \left(V_t + \frac{V_{ov}}{2}\right) \\ &= \frac{V_{ov}}{2} \qquad (3.12) \\ g_m, M1 &= \frac{2I}{V_{ov}} = \frac{1}{R} \qquad (3.13) \end{aligned}$$

If the current I is used to bias another transistor with identical dimensions as M1, the transconductance of that transistor will also be tracking 1/R.

In reality the saturation current of the short channel MOSFET, cannot be described by a simple square law relation and, will depend , to a significant extent, on V_{ds} also. This is indicated by the finite output conductance of the device. The device used in the LNA has $\frac{g_m}{g_{ds}} = 15$. In Fig. 3.8 any variation in the supply voltage, V_{tp}, μ_p is directly reflected on the node y. This together with the finite output conductance of M2 causes deviation of g_m from $\frac{1}{R}$ as the supply, process conditions vary.

3.6.2 Improved fixed transconductance bias circuit design

1. The PMOS current mirrors were cascoded to provide accurate current mirroring.

2. To shield the drain of M2 against supply , V_{tp}, μ_p variations, an op-amp is connected between the nodes p and n and its output controls the gate of the top PMOS transistors as shown in Fig. 3.9. By doing this any supply variation is approximately divided by the op amp gain when it is felt at the drain of M2.

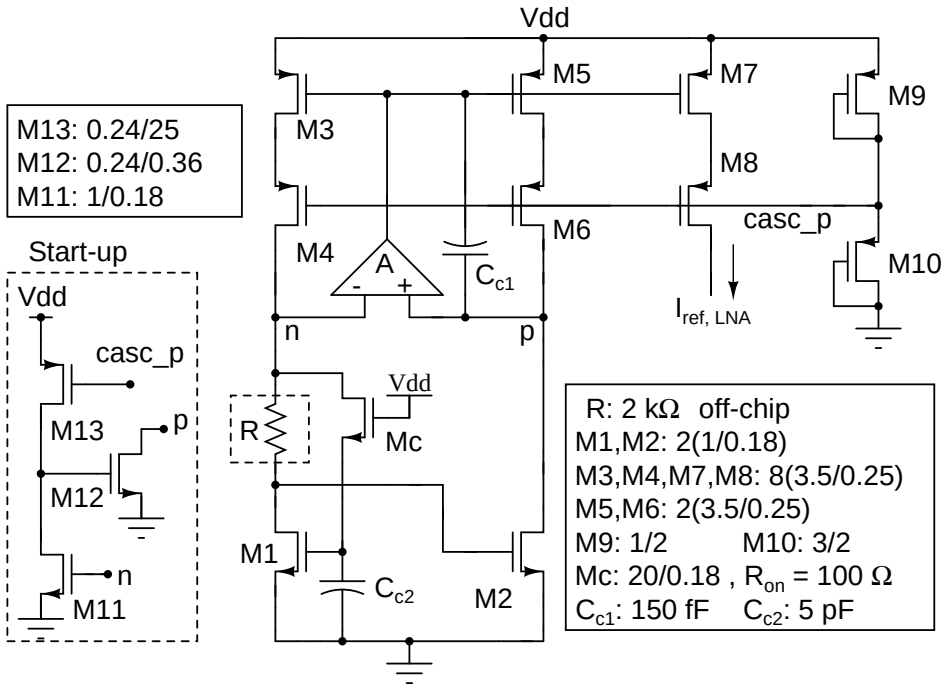

Figure 3.9: Complete fixed g_m bias generation circuit.

The branch comprising M2, M5, M6 was obtained after impedance scaling down by a factor of 4, to reduce power consumption.

M11, M12, M13 shown in the dotted lines implement a start-up circuit to prevent the bias circuit from settling into the zero current state. M13 is a weak device which is always on. Suppose if the circuit is in zero current state to start with, the potential of node n will be less than V_t. This causes M11 to enter into cut-off region. Now M13 starts to charge the gate of M12 and consequently M12 starts to pull current from the node p. This causes current to flow through M5 and M6 which in turn causes current to flow through M3 and M1. Thus zero current state is avoided. When the bias circuit is in proper operation the drain of M11 (strong device compared to M13) is pulled down to a very low potential thereby turning off M12.

The role of the two capacitors C_{c1}, C_{c2} and M_c in Fig. 3.9 will be discussed shortly.

Op-amp design

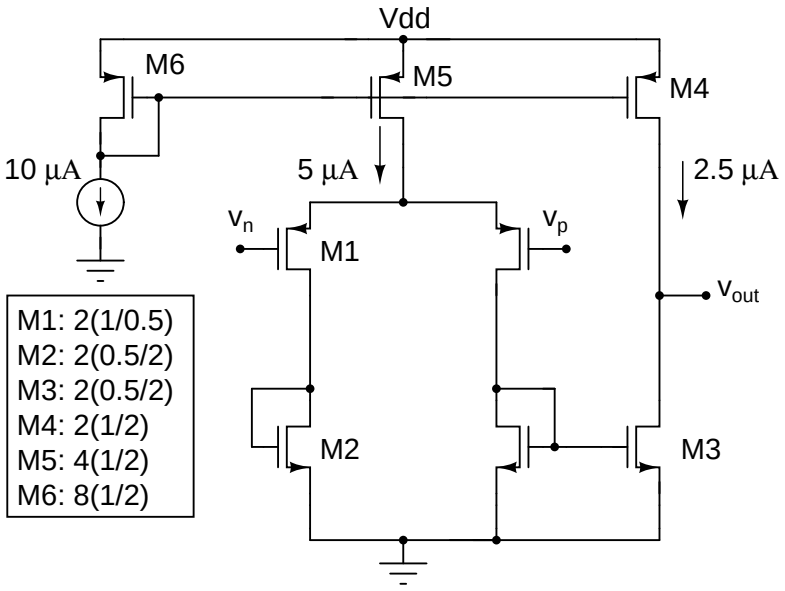

Figure 3.10: Op-amp used in the fixed g_m bias generation circuit.

The op-amp designed is a PMOS input current mirror based op-amp shown in Fig. 3.10. This topology was selected since the input common-mode level for the

op-amp will be around 0.7 V and it has to drive the top PMOS gates in Fig. 3.9. It was designed with a very low current of 20 μA to get a dc gain of around 35 dB.

Compensation of the feedback loops

Any negative feedback loop designed should be properly compensated to ensure stability and acceptable step response.

Since the resistor R is going to be off-chip the effect of the package parasitics namely the pad capacitances and bond wire inductances should be taken into account. Including the package parasitics the external resistor connection appears as shown in Fig. 3.11(a).

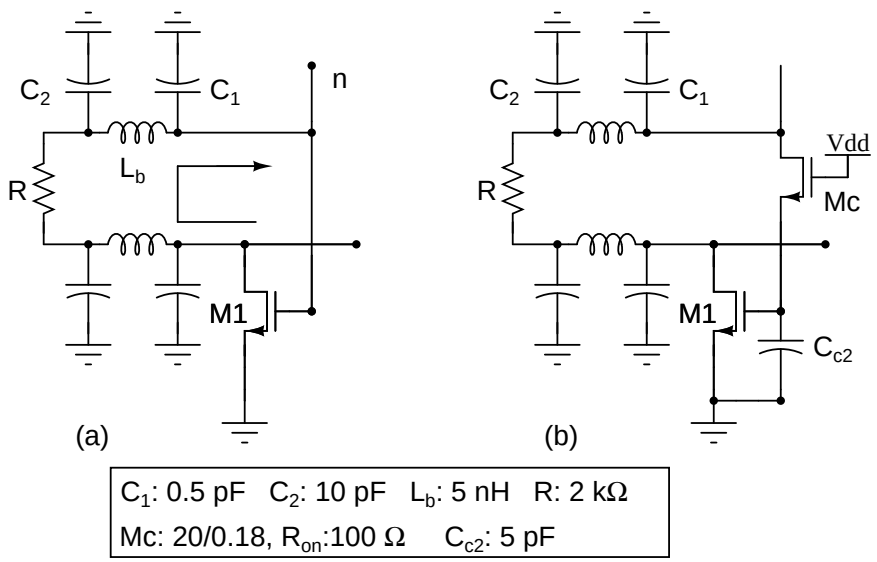

Figure 3.11: Minor loop stabilization.

There are two prominant feedback loops in the circuit in Fig. 3.9.

1. The main low frequency loop formed by the op-amp, PMOS current mirrors, and rest of the circuit is compensated by bypassing the opamp at high frequencies using the capacitor C_{c1} as shown in Fig. 3.9.

2. The minor high frequency loop is formed around the transistor M1 due to the presence of the high Q bond wire inductance as shown in Fig. 3.11(a). This loop is compensated by introducing a damping MOS resistor of 100 Ω from the node n to ground at high frequencies through the large capacitor C_{c2} as shown in Fig. 3.11(b).

Fig. 3.12 shows the step response when a 5 μA current is injected into the node n in Fig. 3.9.

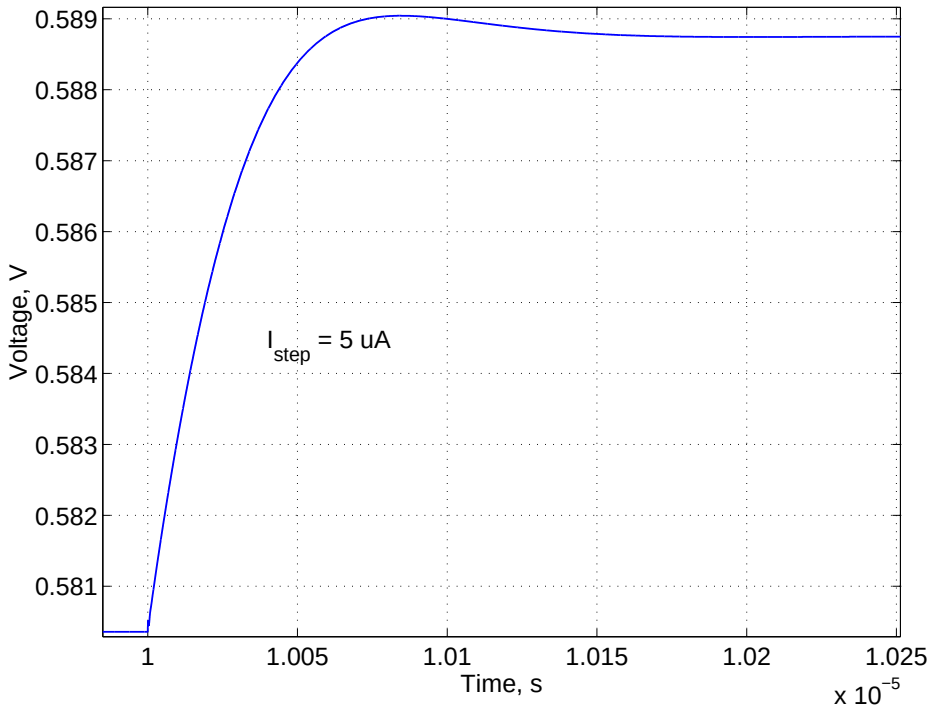

Figure 3.12: Step response of the fixed g_m bias circuit.

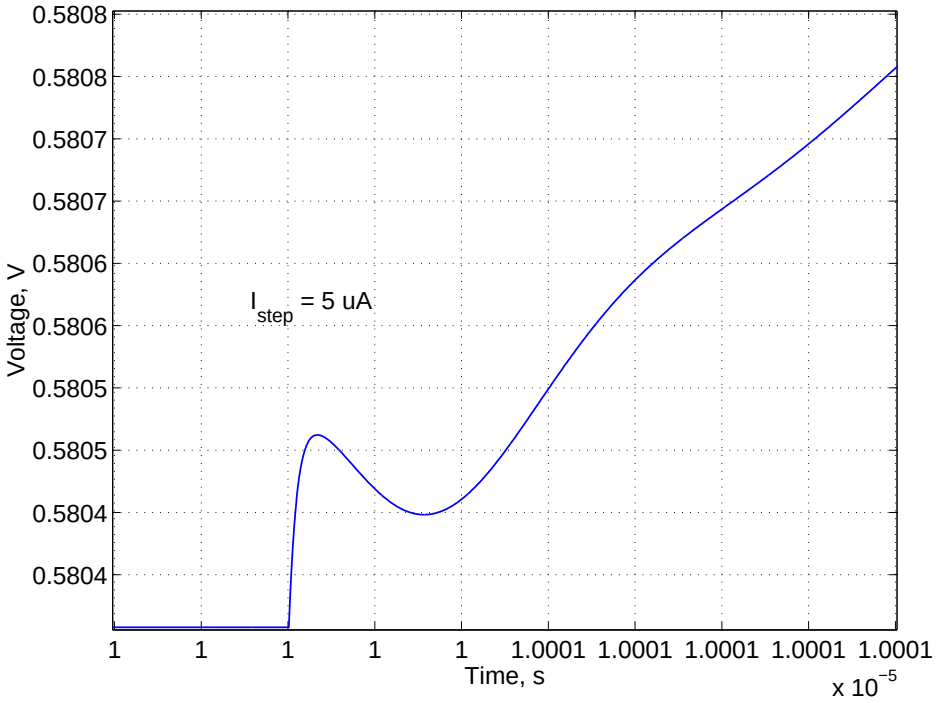

Figure 3.13: Minor feedback loop's step response.

Fig. 3.13 shows the zoomed in version of the step response to show the minor feedback loop's response discussed earlier.

3.6.3 Bias distribution

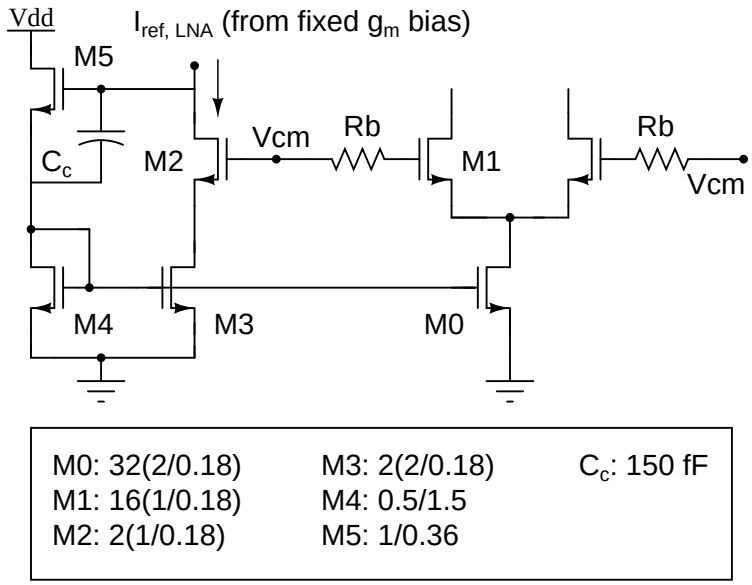

Figure 3.14: LNA bias distribution.

The current $I_{ref,LNA}$ generated from the circuit in Fig. 3.9 is used to bias the LNA as shown in Fig. 3.14. The transistors M3 and M2 are scaled down versions of M0 and M1 respectively, maintaining the same current density. The transistors M2 and M1 act as cascode stages resulting in accurate current mirroring. M5 acts as a battery between the gate of M3 and drain of M2. The capacitor C_c bypasses M5 at high frequencies improving the step response of the feedback loop formed between M2, M3, M4, and M5.

3.6.4 Simulation results for the LNA

Simulation results for the worst case process corners with respect to linearity and noise performance , and one typical corner are given in Table 3.3 and Table 3.4. The bias current consumption details are given in Table 3.5.

The gain of the LNA varies by just around 1 dB over process and temperature

Table 3.3: Simulation results for the LNA in high gain mode

MOS	T, °C	V_{dd}, V	Gain, dB	NF, dB	IIP3, dBm	P_{1dB}, dBm
TT	65	1.8	14.4	7.9	-4	-13.7
SS	80	1.7	13.7	8.5	-1.5	-11.5
FF	0	1.7	14.8	6.7	-8.1	-16.9

Table 3.4: Simulation results for the LNA in low gain mode

MOS	T, °C	V_{dd}, V	Gain, dB	NF, dB	IIP3, dBm	P_{1dB}, dBm
TT	65	1.8	0.3	15.7	-3.9	-13.5
SS	80	1.7	-0.3	16.6	-1.2	-11.1
FF	0	1.7	0.8	14.1	-8	-16.9

Table 3.5: Current consumption of the LNA

MOS	T, °C	V_{dd}, V	LNA	LNA_{bias}	Total
TT	65	1.8	1.12 mA	195 μA	1.315 mA
SS	80	1.7	1.34 mA	227 μA	1.56 mA
FF	0	1.7	0.82 mA	151 μA	0.97 mA

due to the fixed gm bias arrangement. This also leads to large variations in the bias currents over process corners. This results in linearity degradation at one extreme (FF corner and 0°C) and linearity enhancement at the other extreme (SS corner and 80°C).

The large increase in the NF, around 8 dB, in the low gain mode is due to the increased noise contribution from the variable gain stage transistors M2 and M4 in Fig. 3.7. Refer to Appendix B for the NF derivation for the LNA in the low gain mode.

CHAPTER 4

Downconversion Mixer Design

The function of a mixer is to perform frequency translation. It is different from a multiplier by the fact that its output should depend linearly only on the RF input and not on the LO amplitude. So it can be modeled as shown in Fig. 4.1. Conversion gain for such a mixer is $\frac{2}{\pi}$.

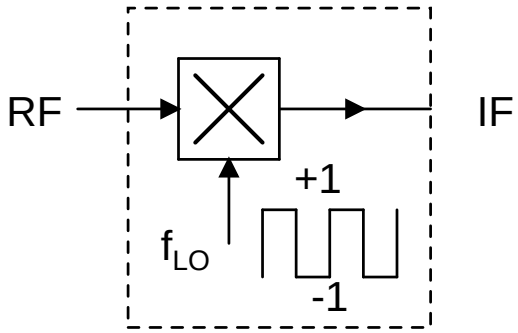

Figure 4.1: Mixer model.

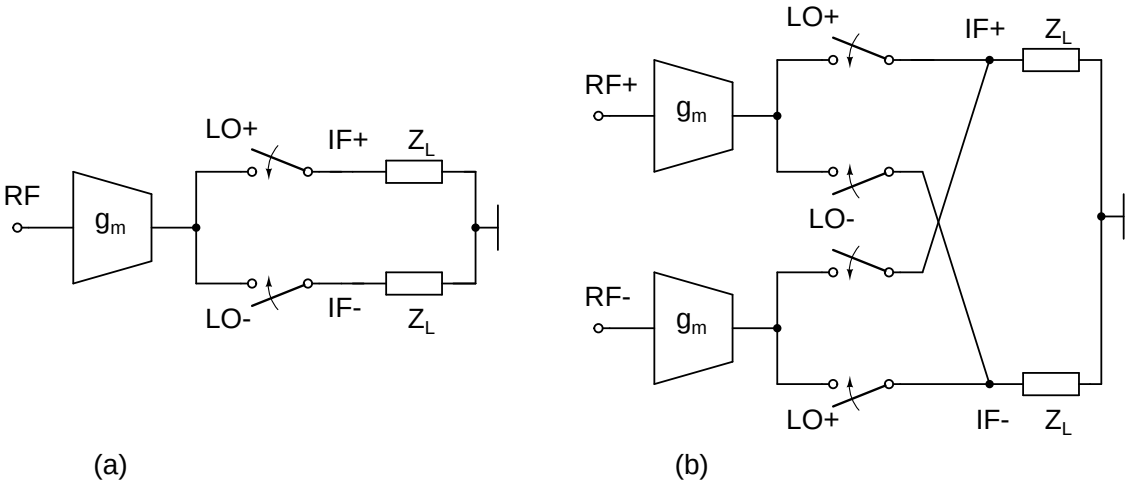

Figure 4.2: Practical implementation model for mixers. (a) single-balanced mixer, (b) double-balanced mixer.

In practical implementations, the RF input voltage is converted into a current using a transconductor, g_m, and the RF current undergoes the mixing action. The

frequency translated current is then made to flow through a load, Z_L, to generate the output voltage. This is illustrated in Fig. 4.2 for single-balanced and double-balanced mixers. The conversion gain in both the configurations, assuming ideal LO switching, is $g_m \frac{2}{\pi} Z_L$.

Double-balanced mixer is usually preferred due to its fully differential nature and absence of LO and RF feedthrough to the output ideally.

4.1 Downconversion Mixer requirements

- Since direct conversion architecture is used, the mixer should be designed to minimize the effect of flicker noise.
- Since highly linear op-amp RC low pass filter (LPF) follows the mixer, maximum gain limited by the output swing limits should be obtained. This eases the noise requirements of the LPF.
- Downconversion mixer should be highly linear due to the LNA gain preceding it and due to the presence of unfiltered interferers. Typically the whole receiver's linearity performance is limited by the downconversion mixer.
- As noted in chapter 2 even in fully differential implementations IM2 products appear due to mismatch in the circuits. Special care should be taken in the mixer layout to minimize systematic mismatches. Also LO and RF coupling should be minimized as much as possible.

4.2 Mixer topology comparison

Mixers can be broadly classified into two types:

- Passive mixers
- Active mixers

4.2.1 Passive mixers

Passive mixers with the switch transistors in triode region and used in current-mode operation, shown in Fig4.3(a), are known for their superior linearity and

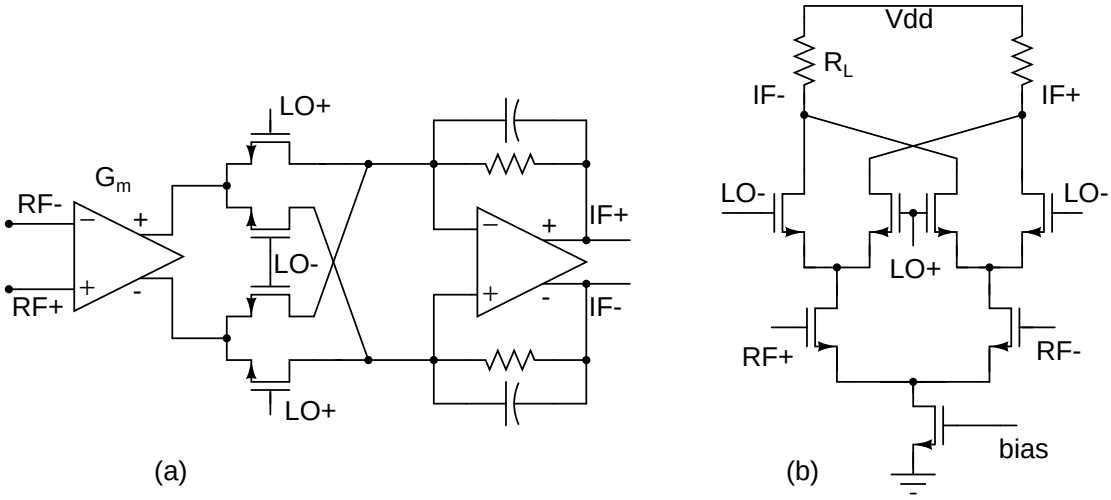

Figure 4.3: Mixer topologies: (a) Passive current-mode mixer (b) Active Gilbert mixer.

flicker noise performance at the cost of conversion loss [10]. Also passive mixers are bi-directional and require large LO drive compared to active mixers.

4.2.2 Active mixers

Active Gilbert mixer, shown in Fig4.3(b), provides conversion gain, reverse isolation, requires smaller LO drive. Linearity provided by active mixers is sufficient since the receiver will be operated in two gain modes. Only issue is that the switches in an active Gilbert mixer result in flicker noise at the output.

4.3 Downconversion Mixer design Procedure

A double balanced Gilbert mixer was designed. During the design, the I and Q mixers were cascaded with the already designed LNA block and the overall block was simulated for NF, IIP3, P_{1dB}, gain etc.

Table 4.1: Specifications for the LNA + Mixer

Parameter	Value
Spectrum	2.405 to 2.485 GHz
Gain	> 25/11 dB
IIP3	> -20/-10 dBm
P_{1dB}	> -30/-20 dBm
NF (DSB)	< 12 dB
I_{bias}	0.5 mA (each mixer)

4.3.1 LNA + Mixer specifications

4.3.2 Class-AB transconductor

The linearity of an active mixer is primarily limited by the input transconductor's non-linearity since the current switching, ideally, does not contribute to any non-linearity.

The transconductor used in the mixer should be more linear when compared to the LNA transconductor, since a gain of around 8 dB is present between the LNA transconductor input and the mixer input, in the high gain mode. Differential pair transconductor is simple to bias, provides common mode rejection, but poor in terms of linearity compared to other transconductor implementations reported in the literature [11].

Consider two identical transistors M1 and M2, in saturation region, whose *sum of gate source voltages is a constant*, as shown in Fig4.4(a).

The difference in their drain currents is,

$$I_{d1} - I_{d2} = \frac{\beta}{2}\left(V_{gs1} + V_{gs2} - 2V_t\right)\left(V_{gs1} - V_{gs2}\right) \tag{4.1}$$

Above relation is valid as long as,

$$|V_{g1} - V_{g2}| \leq 2\left(V_{cm} - V_t\right) \tag{4.2}$$

where $V_{cm} = \dfrac{(V_{gs1} + V_{gs2})}{2}$.

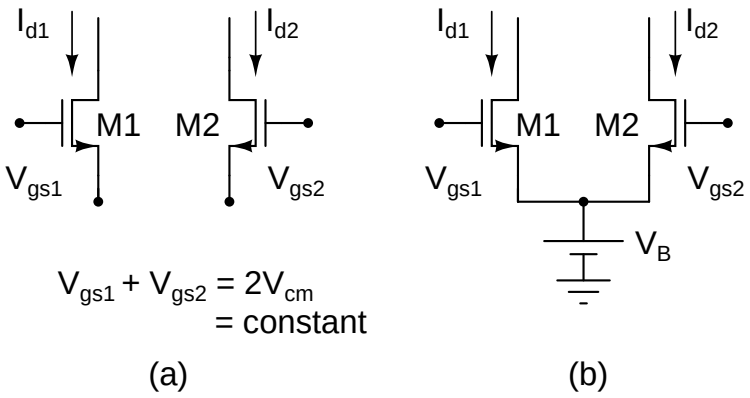

Figure 4.4: Class-AB principle.

Even though mobility degradation in short channel devices and other secondary effects introduce odd order distortion in the differential current, linearity is superior compared to the simple differential pair. The linear operating range of the class-AB transconductor can be increased by increasing V_{cm}. One simple way to maintain *constant sum of gate source voltages* is to just connect both the source nodes to a battery V_B as shown in Fig. 4.4(b). By doing this, common-mode rejection of the transconductor is lost. But this is acceptable, since the use of differential inductors as the LNA load provides significant common-mode rejection, as will be shown in Chapter 6, at the mixer input. Another implementation of a class-AB transconductor which provides common-mode rejection as well, will be discussed in Chapter 5.

Another disadvantage of the class-AB transconductor is the presence of second order distortion components as common-mode signals. So any mismatch between M1 and M2 or the output load will result in differential second order distortion components at the output. This does not occur with an ideal differential pair transconductor where even the single-ended output currents display only odd order distortion components [12].

Another important thing to note is that the current drawn from the supply for the class-AB transconductor varies with the input signal level. Maximum current drawn will be $2I_{DC}$. This occurs when $|V_{gs1} - V_{gs2}| = 2\,(V_{cm} - V_t)$ at which the current through one of the transistors becomes zero.

4.3.3 Mixer core

Flicker noise at the output of a Gilbert mixer occurs due to two mechanisms[13; 14].

The first mechanism is due to the modulation of the switching instants by the slowly varying flicker noise of the switches. To reduce the flicker noise at the output due to this mechanism, current switching should be made as abrupt as possible, flicker noise of the device and the bias current through the switches should be reduced.

The second, indirect, mechanism is due to the periodic charging and discharging of the tail node capacitance resulting in an average output noise current. So tail node capacitance and flicker noise of the switching device should be minimized to reduce flicker noise at the output due to this mechanism.

PMOS transistors were used as current commutating switches since they provide better flicker noise performance compared to NMOS devices, in the UMC 0.18 μm technology used.

The current switching can be made abrupt by increasing the LO drive and reducing the static overdrive of the switches. LO drive cannot be increased beyond 200 mV peak, singled-ended owing to excessive power consumption in the LO driver. So the overdrive of the switches has to be reduced without excessively loading the LO driver. This can be achieved by reducing the dc current through the switch transistors.

4.3.4 Current-reuse technique

The above observations with respect to flicker noise reduction indicates that the transconductor and the mixer core should not share the same bias current, as in a conventional Gilbert mixer, for optimum noise and linearity performance. Also from another point of view, if simple resistive loads to ground are used at the conventional Gilbert mixer output, their values get limited due to voltage headroom considerations, i.e. to prevent switch transistors from entering into triode

region when the LO drive is negative, if all the transconductor bias current flows through the switches. So the bias current through the switches should be made small than the bias current through the transconductor. This can be achieved by introducing a dc current source at the common source node of the switches to reduce the dc current flowing into the switches as shown in the single-balanced version in Fig. 4.5(a).

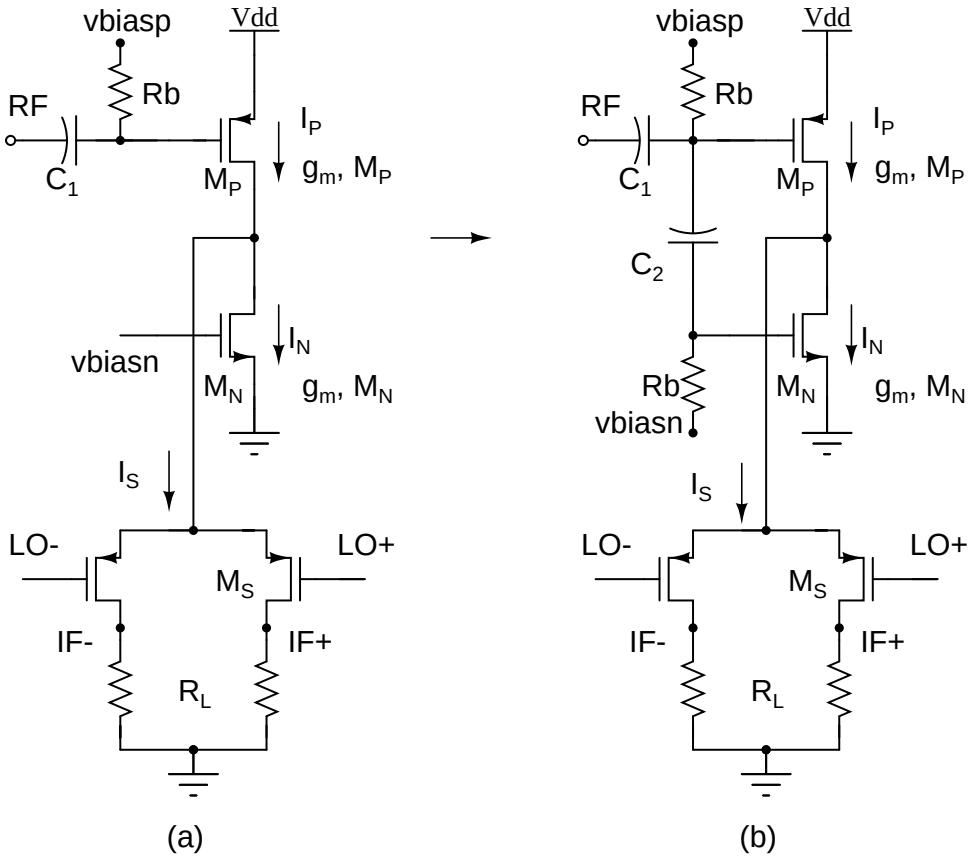

Figure 4.5: Current-reuse technique.

A still better way of utilizing the available resources would be to make the current source M_N to act like an additional transconductor, for RF signals, using a coupling capacitor C_2 as shown in Fig. 4.5(b) [15; 16]. By doing this the gain and noise performance of the mixer is improved for the given bias current. Linearity of the mixer in Fig. 4.5(b) will be slightly poorer than the previous arrangement due to the increased signal swing at the common source node of the switches.

The impedance looking into the mixer core , is approximately $\frac{1}{\sqrt{2}\,g_m, M_S}$, assuming the RF signal current has completely switched to one of the arms. It should

be noted that as the current through the switches is reduced this impedance increases. As a result the conversion gain reduces due to signal loss in the parasitic capacitance at the common source node. Also the RF signal swing at the common source node increases resulting in increased distortion by the switches. So the current through the switches should be properly selected such that reduced conversion gain and linearity degradation are within acceptable limits.

4.3.5 Mixer load

The mixer is supposed to drive a 3 pole Rauch (opamp-RC) low pass filter (LPF). So the first resistor in the filter should be incorporated as the mixer load. The mixer output stage should provide the appropriate common-mode level for the LPF, less sensitive to resistor variations over process and temperature. So the resistors were connected differentially across two NMOS current sources whose gates were directly connected to the detected common-mode at the middle of the two resistors.

The overdrive of the current source transistors should be increased as much as the output voltage swing permits to reduce their thermal noise contribution. In the design the overdrive was kept around 300 mV. Large lengths were used to reduce their flicker noise contribution. The common-mode reference for the LPF opamp , used for common-mode feedback, will be generated using an impedance scaled version of the mixer load transistors, to match the input and output common-mode levels of the LPF to a better accuracy. The high resistivity poly resistor used shows around $\pm 30\%$ variations over process corners. This variation was taken into account while simulating for noise and linearity performances.

The schematic of the designed mixer is shown in Fig. 4.6.

4.3.6 Mixer bias generation

In the grounded source class-AB transconductor the input common-mode level fixes the bias currents and the transconductance. The bias voltages required to

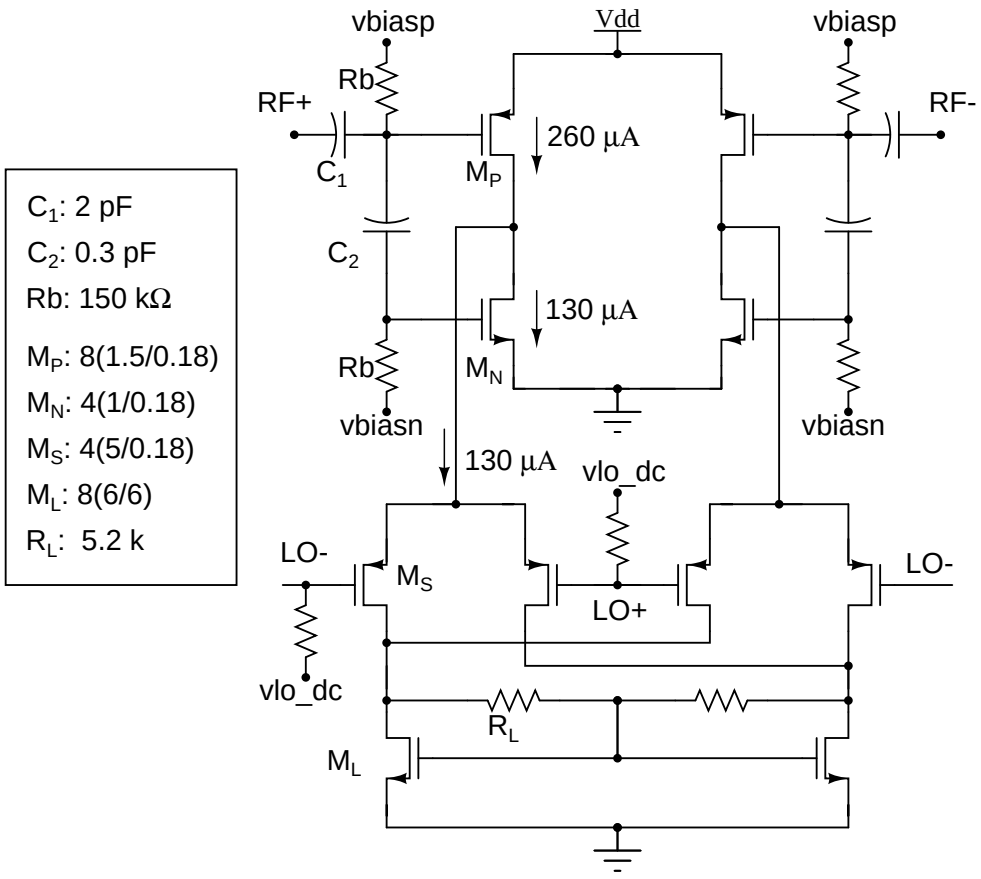

Figure 4.6: Schematic of the downconversion mixer.

generate the desired dc bias currents through PMOS and NMOS transconductors shown in Fig. 4.6 are obtained using a replica biasing arrangement shown in Fig. 4.7.

Refer to Fig. 4.6 and Fig. 4.7. Since the bias current of 260 μA through M_P is to be split equally between M_N and the switches, M_P is split into two and each half is scaled down to get M1 and M3. M2 is a replica scaled version of M_N. An opamp in negative feedback is used to maintain the drain voltages of M1 and M3 equal, which replicates the bias conditions in the actual mixer circuit. M5 acts as a battery of 550 mV between the gate of M3 and the drain of M_S to keep M_S in saturation.

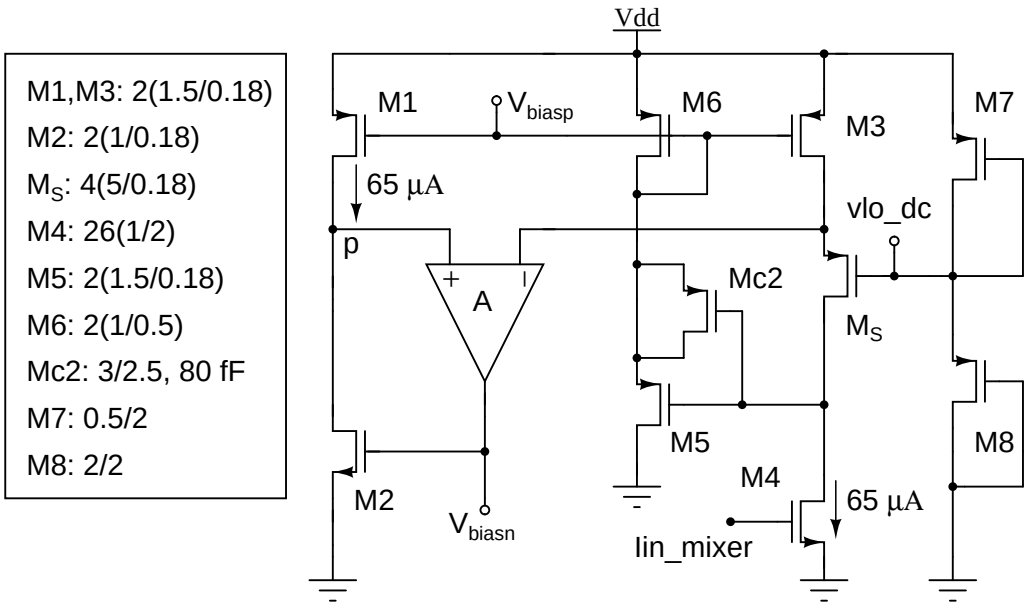

Figure 4.7: Mixer bias generation circuit.

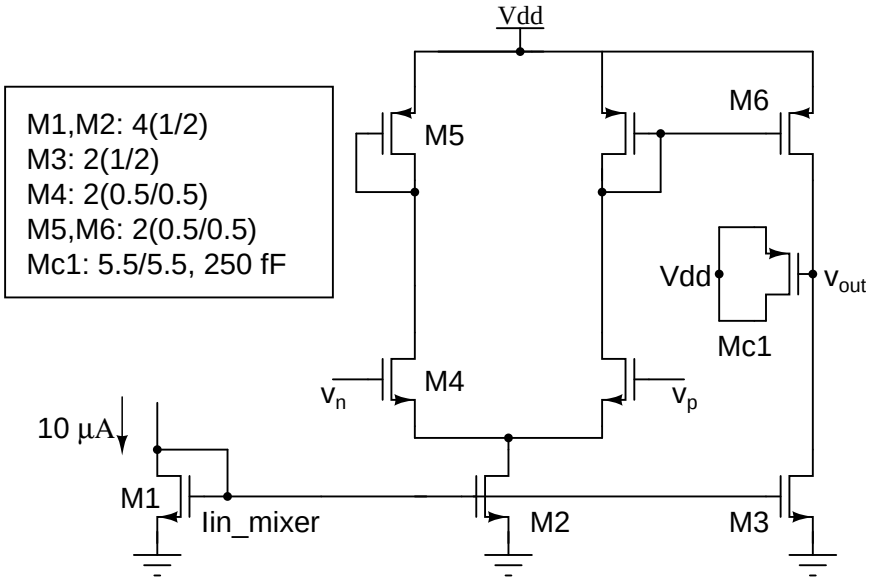

Figure 4.8: Op-amp used in the mixer bias generation circuit.

Op-amp design and compensation of the feedback loops

The op-amp designed is a NMOS input current mirror based opamp shown in Fig. 4.8. This topology was selected since the input common-mode level will be around 1.3 V and the op-amp output has to drive the gates of the NMOS transistor M2 shown in Fig. 4.7. The negative feedback loop comprising the opamp and M2

is compensated by creating a dominant pole at the output of the op-amp using a large capacitor, implemented using the PMOS transistor Mc1.

Referring to Fig. 4.7, the feedback loop formed between M3, M_S, M5 and M6 is compensated by bypassing M5 at high frequencies using the capacitor formed using Mc2.

Fig. 4.9 shows the step response when a 5 μA current is injected into the node p in Fig. 4.7.

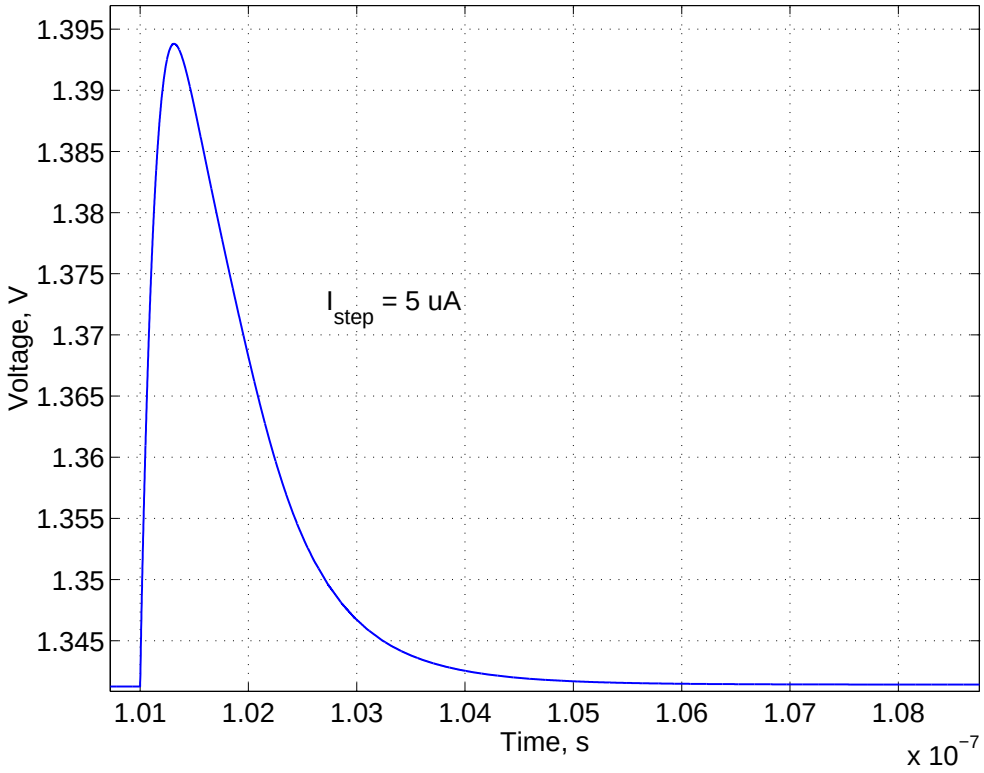

Figure 4.9: Step response of the downconversion mixer bias generation circuit.

4.3.7 Simulation results for the LNA + Mixer

Simulation results for the worst case process corners with respect to linearity and noise performance , and one typical corner are given in Table 4.2 and 4.3.

NF (DSB) was obtained by integrating the noise spectral density from 1 kHz to 1.5 MHz.

The bias current consumption details are given in Table 4.4.

Table 4.2: Simulation results for the LNA + Mixer in high gain mode

MOS	T, °C	Res.	V_{dd}, V	Gain, dB	NF, dB	IIP3, dBm	P_{1dB}, dBm
TT	65	TYP	1.8	26.8	9.5	-16.3	-26.5
SS	80	MIN	1.7	21.5	10.8	-13.9	-23.5
FF	0	MAX	1.7	31.6	7.8	-19.5	-29.2

Table 4.3: Simulation results for the LNA + Mixer in low gain mode

MOS	T, °C	Res.	V_{dd}, V	Gain, dB	NF, dB	IIP3, dBm	P_{1dB}, dBm
TT	65	TYP	1.8	12.8	20.2	-6	-15.17
SS	80	MIN	1.7	7.5	22.3	-3.4	-13
FF	0	MAX	1.7	17.6	17.6	-9.6	-18.7

Table 4.4: Current consumption of the complete quadrature downconverter

MOS	T, °C	V_{dd}, V	LNA	LNA_{bias}	Mixer	$Mixer_{bias}$	Total
TT	65	1.8	1.12 mA	195 μA	2(515) μA	164 μA	2.51 mA
SS	80	1.7	1.34 mA	227 μA	2(485) μA	158 μA	2.7 mA
FF	0	1.7	0.82 mA	151 μA	2(512) μA	163 μA	2.16 mA

The large variation in the gain ($\pm$ 5 dB) is primarily due to the large variation of the poly resistor load and transconductance of the mixer over process and temperature. Even with this large process variations, the designed RF front-end meets the system specifications.

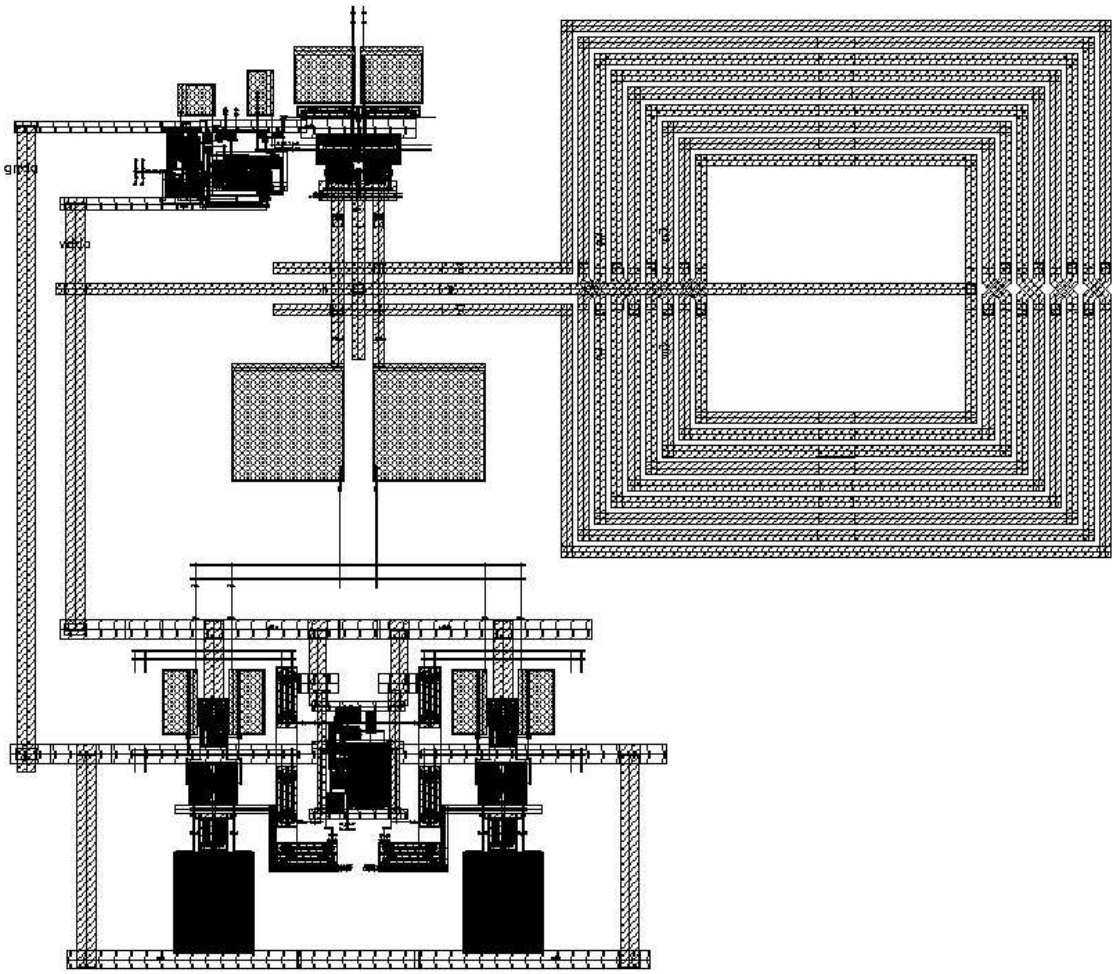

Figure 4.10: Layout of the quadrature downconverter.

Fig. 4.10 shows the layout of the designed quadrature downconverter.

CHAPTER 5

Quadrature Up-converter Design

A direct conversion transmitter architecture, shown in Fig. 5.1 has been selected owing to its simplicity and potential for high level integration and low power consumption[17].

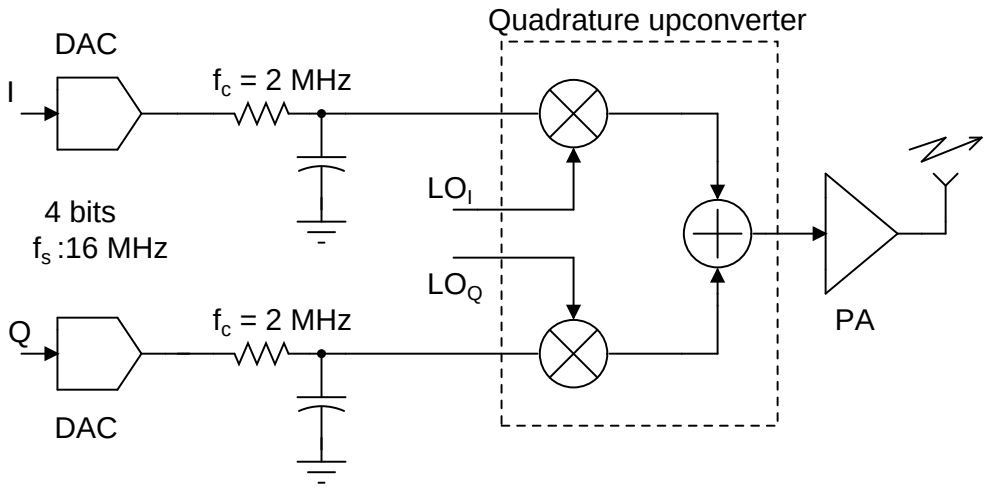

Figure 5.1: Direct conversion transmitter block diagram.

5.1 Up-conversion mixer requirements

- The main requirement of the up-conversion mixer is the linearity. Non-linearity in the mixer, primarily in the transconductor, creates intermodulation products that corrupts the desired baseband signal and also creates harmonic distortion components which get up-converted and affect the neighboring channels. So the transmitter has to confirm to transmit power spectral density (PSD) mask, given in IEEE 802.15.4[3] standard. It is reproduced below.

  The transmitted spectral products shall be less than the limits specified in Table 5.1. For both relative and absolute limits, average spectral power shall be measured using a 100 kHz resolution bandwidth. For the relative limit, the reference level shall be the highest average spectral power measured within 1 MHz of the carrier frequency.

  The transmit mixer should satisfy the transmit PSD mask with sufficient margin to account for the power amplifier (PA) nonlinearity.

Table 5.1: Transmit PSD limits

Frequency	Relative limit	Absolute limit
$\|f - f_c\| > 3.5$ MHz	-20 dB	-30 dBm

- Since a direct conversion architecture is used , any mismatch in the I and Q paths will result in the appearance of the image band. Also any mismatch in each of the I/Q mixer will result in dc offsets, which results in LO leakage to the output. The above effects are dependent on device matching and more importantly on the layout of the mixer. So special care should be taken to make the I and Q paths well matched.

5.2 Up-conversion mixer design procedure

5.2.1 Class-AB transconductor

Since linearity is of prime concern in a transmit mixer, class-AB transconductor discussed in chapter 4 would be a good choice. But a simple grounded source transconductor, with the bias arrangement discussed in chapter 4, cannot be used here since the low pass filter preceding the transmit mixer cannot be ac coupled and any common-mode, V_{cm}, shifts will significantly affect the bias currents of the transconductor.

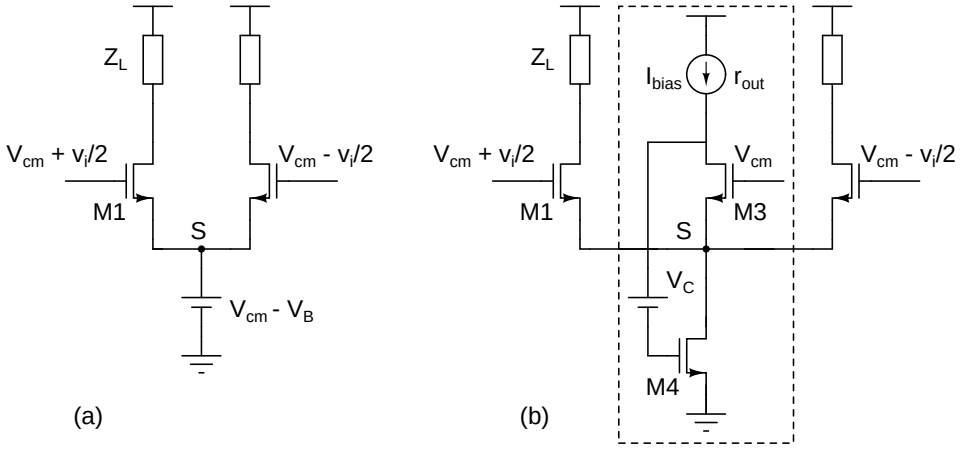

Figure 5.2: Class-AB transconductor implementation.

Another way of obtaining class-AB operation, as discussed in [18], would be to

connect the common source node of the two NMOS transistors to a battery of value $V_{CM} - V_B$ as shown in Fig. 5.2(a). Here $V_B > V_t$ determines the transconductor bias currents independent of the input common-mode level. This also means that the transconductor exhibits infinite common-mode rejection. A practical implementation of such a battery is shown in Fig. 5.2(b). M3, scaled down version of M1, acts as a voltage level shifter, generating $V_{CM} - V_B$ at the common source node. The output impedance offered by such a battery, shown in dotted lines, is approximately $\frac{1}{(g_{m3}r_o)g_{m4}}$, where r_o is the output impedance of the current source. The output impedance will be very low considering the fact that the total bias current flows through M4 and a small overdrive would be associated with it, to relax the output common mode level requirements of the preceding block, the digital to analog converter (DAC) in this case. V_C is a battery which helps to keep M3 in saturation.

The complete implementation of the transconductor is shown in Fig. 5.3.

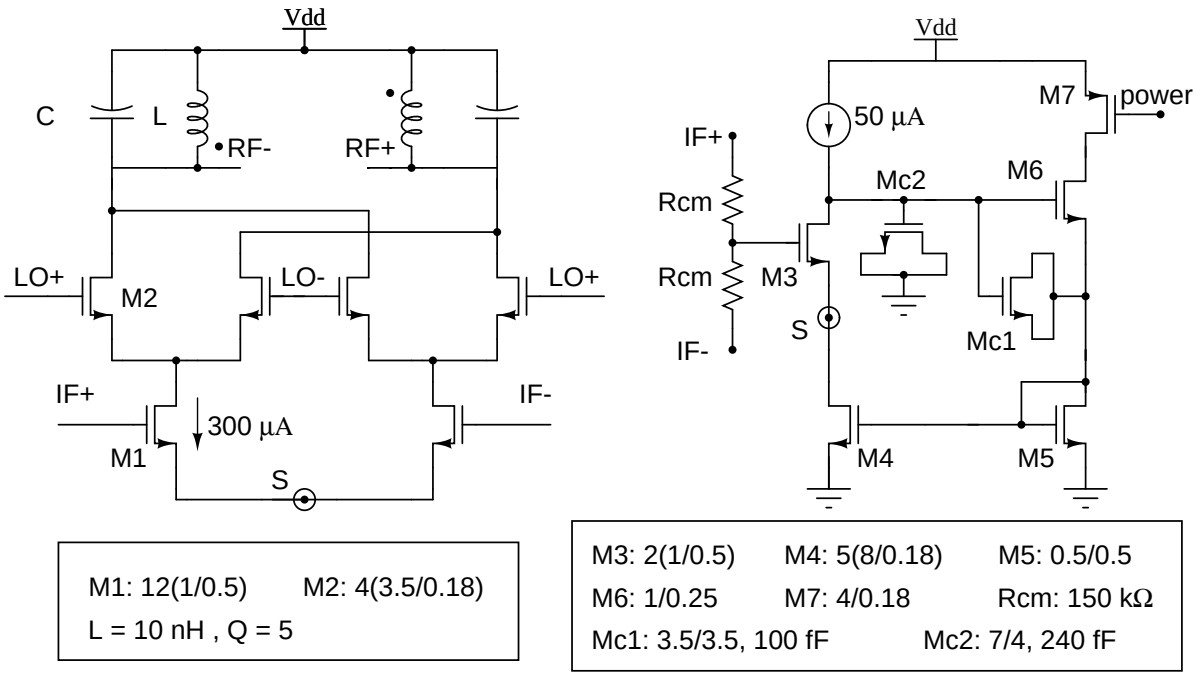

Figure 5.3: Schematic of the up-conversion mixer.

Note that the node S marked with a $\odot$ in the two parts are connected. Non-minimum lengths were used in the transconductor to increase the output resistance, improve matching and also to minimize the flicker noise getting up-

converted to the output RF spectrum.

M3 implements the level shifter discussed earlier. The gate of M3 is provided with V_{cm} by the resistive common detector implemented using large poly resistors R_m. M6 implements the battery V_C shown in Fig. 5.2(b). Mc1 and Mc2 are MOS capacitors used to compensate the negative feedback loop formed between M3, M4, M5, and M6. Mc2 introduces a dominant pole at the drain of M3. Mc1 bypasses M6 at high frequencies and improves the stability of the loop. M7 operated between triode and cut-off region is used to power down the transmit mixer block.

Fig. 5.4 shows the step response when a 5 μA current is injected into the node S in Fig. 5.3.

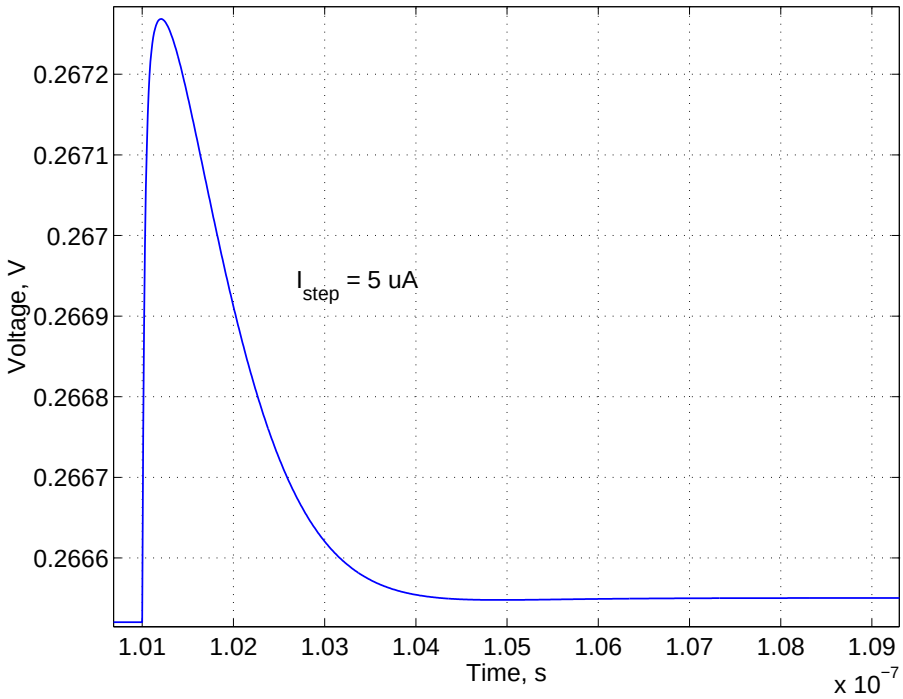

Figure 5.4: Step response of the transmit mixer's bias circuit.

Transconductor linearity requirements

The mixer was designed to handle input signals, from the DAC, as large as 200 mV, single-ended. Sufficient overdrive was given to M1 to achieve good linearity performance. The transconductor was initially designed for a HD_3 of 40 dB in its

output current, with 360 mV differential input.

To find whether mixer will satisfy the transmit PSD limits, Matlab was used to model the mixer with the transconductor's non-linearity with some margin for the switch non-linearity. Since the nonlinearity is primarily due to the transconductor alone, it is not necessary to model the frequency translation effects in Matlab. So just a complex baseband simulation with MSK symbols will be sufficient to obtain the transmit spectrum including mixer nonlinearity.

3000, ZigBee compliant, MSK symbols were used with a sampling frequency of 16 MHz. A first order low pass filter with a cut-off frequency of 2 MHz was used before the mixer. Fig. 5.5 shows the PSD plots with and without including the mixer nonlinearity.

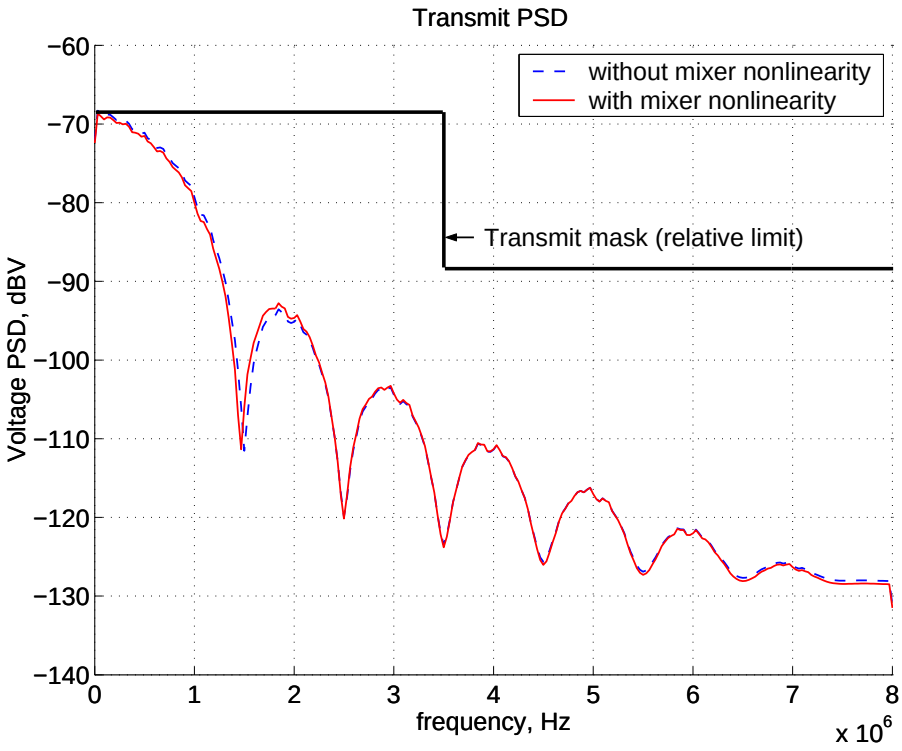

Figure 5.5: Matlab PSD plots.

From Fig. 5.5, we find that the nonlinearity introduced by the mixer is very small and satisfies the transmit PSD mask's relative limit with sufficient margin to accommodate the PA nonlinearity.

5.2.2 Mixer core

In a transmit mixer noise generated by the devices is of less importance since the signal levels are significantly large compared to the noise levels. Also the flicker noise from the switches is not a problem with up-conversion mixer since the output desired spectrum is at RF. So NMOS devices with minimum length were used and small overdrive was used to help in sharp switching with a 200 mV single-ended LO drive.

5.2.3 Mixer load

The 20nH differential inductor with a Q of 5, used for the LNA load, is used as the the mixer load. This is essential here since the mixer has to drive the large capacitive load of the PA.

5.2.4 Simulation results for the up-conversion mixer

The up-conversion mixer shown in Fig. 5.3 was simulated with 360 mV differential input and 400 mV differential LO drive.

Simulation results are shown in Table 5.2.

Table 5.2: Simulation results for the up-conversion mixer

MOS corners	T, °C	V_{dd}, V	V_{out}, mV	IIP3, dBV	P_{1dB}, dBV	I_{bias}, μA
TT	65	1.8	241	5.4	-3	650
SS	80	1.7	210	5.9	-2.9	647
FF	0	1.7	309	3.8	-3.6	655

5.3 Quadrature up-converter

The quadrature up-converter is obtained by summing the up-converted currents from the I and Q branches into the common resonant load, as shown in Fig. 5.6.

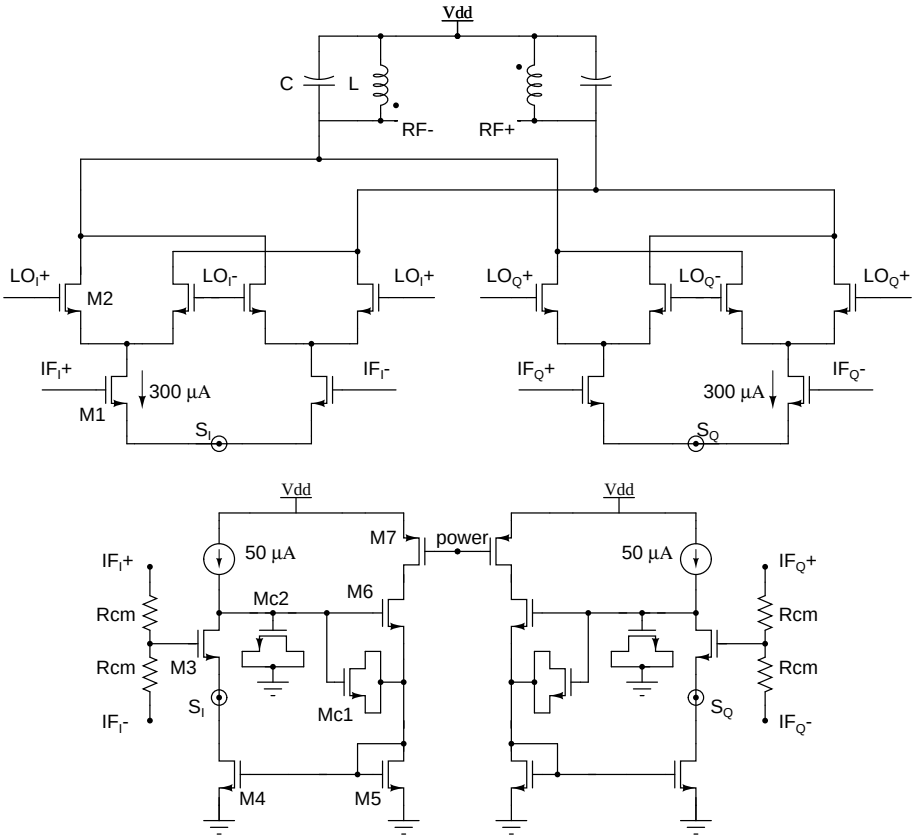

Figure 5.6: Schematic of the quadrature up-converter.

5.3.1 Simulation results for the quadrature up-converter

3000 random I/Q MSK symbols of amplitude 360 mV differential were created using Matlab and used for simulation. A first order LPF of corner frequency 2 MHz precedes each of the mixer blocks. Envelope following simulation, available in SPECTRE RF simulator from CADENCE, was used to obtain the output spectrum. Since Envelope following simulation consumes lot of time , it was used only to verify the final up-converter output spectrum with the results obtained from Matlab simulation. The simulation was performed for FF MOS corner at 0° C for the worst case linearity performance.

Since MSK modulation is used [19], the output peak amplitude will be twice the peak amplitude obtained from a single mixer with the same load. So from Table 5.2 peak output amplitude should be, ideally, 2×309 mV $= 618$ mV differential. In simulation it was found to be 585 mV differential. The PSD plots from envelope following simulation and Matlab simulation are shown in Fig. 5.7.

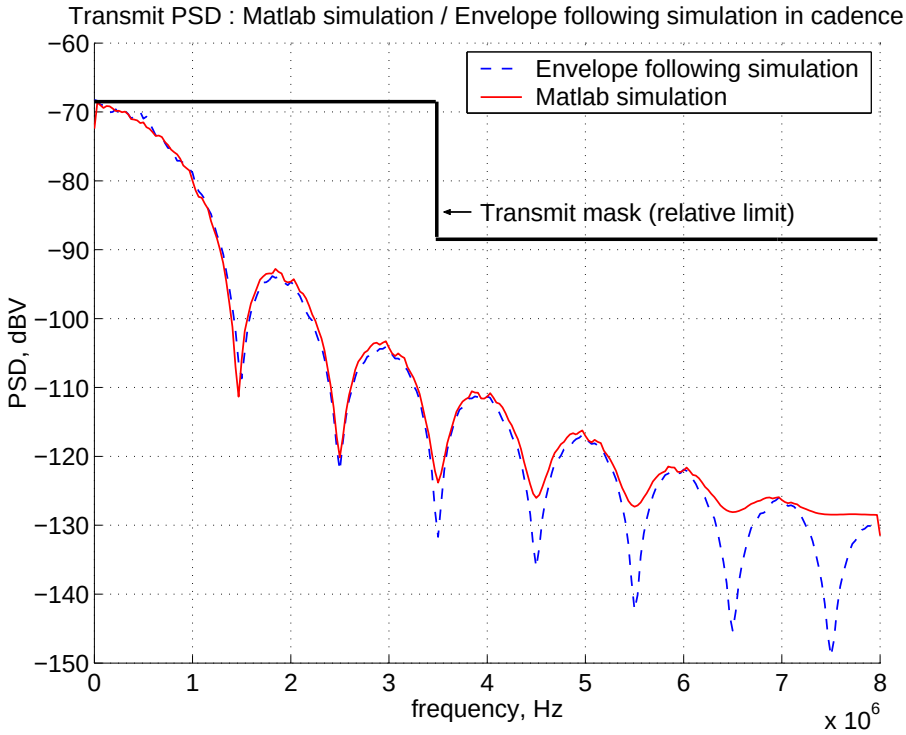

Figure 5.7: PSD plots from Matlab and Cadence envelope following simulation

Envelope following simulation results match well with the Matlab results.

Fig. 5.8 shows the layout of the quadrature up-converter.

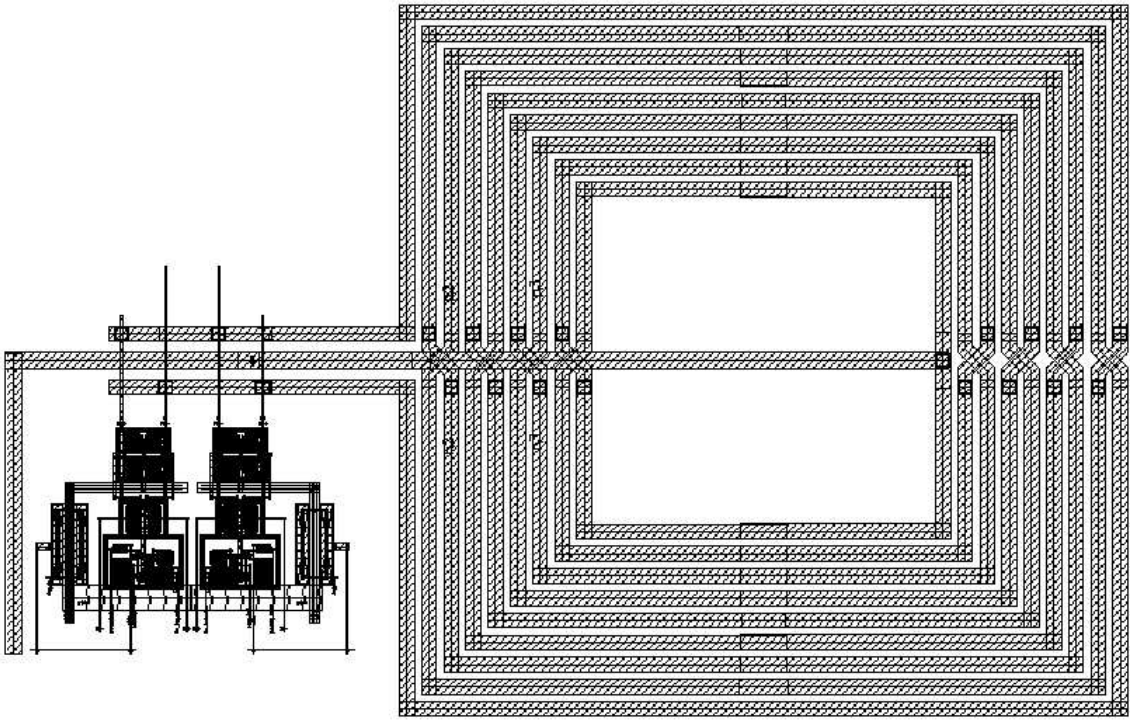

Figure 5.8: Layout of the quadrature up-converter.

CHAPTER 6

On-Chip Inductor Modeling

6.1 Importance of on-chip inductors

Inductors are typically used as resonant tank circuits in oscillators, tuned amplifiers and mixers. On-Chip inductors with high quality factors help in reducing the power consumption in these circuits while maintaining the required performance. Also use of resonant loads allows signals to swing above the supply. This makes inductors indispensable for power amplifiers and low voltage RF circuits in general.

Typically the Q of the on-chip capacitors are an order higher than that of the on-chip inductors. Quality factor of the Inductors fabricated in CMOS technology are inferior to that from other technologies like GaAS. This is due to the use of aluminium interconnects and the lossy nature of the Si substrate in a typical CMOS technology.

6.2 UMC 0.18 μm foundry options

The resistivity of the Si substrate in the UMC 0.18 μm process is 20 Ωcm. This value is quite high so that the eddy current losses in the Si substrate can be neglected. The process uses 6 metal layers with the top metal layer being made thicker (2.06 μm) for on-chip inductor design.

6.3 Inductor selection

A differential square spiral inductor was selected rather than two separate single-ended inductors for the LNA and up-conversion mixer load. The reasons are as

follows.

- Differential inductors are compact than the two single ended inductors they replace, since they utilize the the positive mutual inductance between adjacent coils also, in addition to the self inductances to get the total inductance. On the contrary if two single ended inductors are used they should be sufficiently spaced apart to minimize the negative mutual magnetic coupling between them[20].
- Differential inductors when excited differentially provide better Q compared to single-ended excitation [20].
- When a differential inductor is excited differentially its inductance can be represented as $L(1+k)$. Here L is the self inductance of one symmetric half spiral of the differential inductor and k is the mutual coupling co-efficient between the two symmetric spirals. For differential-mode excitation the mutual coupling is positive. But under common-mode excitation the mutual coupling becomes negative and the inductance value gets reduced to $L(1-k)$. So when a differential inductor is used in a tuned circuit (e.g. LNA load), for common-mode signals the LC tank gets detuned to a higher frequency. This results in attenuation of common mode signals at the desired band. In other words differential inductor provides common-mode rejection [21].

6.4 Inductor design

With all the process related information provided by the foundry, ASITIC [22] was used to determine the optimum inductor dimensions namely metal width (W), spacing (S), length(L), and turns (N), for 20 nH inductance and Q around 5. Q much larger than 5 is not desirable for the LNA and the up-conversion mixer loads since any tolerance in the capacitance values will significantly shift the resonant frequency. Also the value of Q can vary by $\pm$ 20% over process variations. So the inductor was designed with a slightly higher Q than 5.

The designed inductor dimensions are as follows: L = 230 μm, W = 4.7 μm, S = 2.3 μm, N = 9.

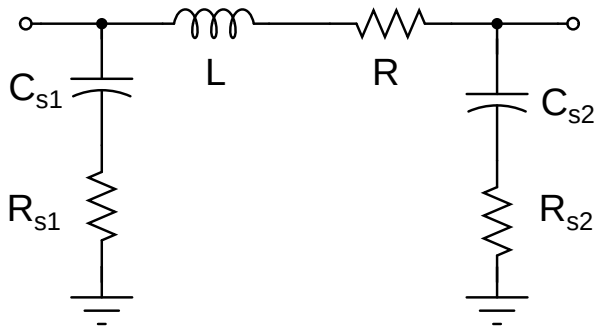

Figure 6.1: Inductor pi model from ASITIC.

6.5 Mutual inductance and parasitic capacitance modeling

ASITIC just provides a lumped pi model, as shown in Fig. 6.1, for the inductor around the desired frequency of interest. In the model, L is the equivalent inductance after taking the interwinding capacitance into account. So its value will be significantly larger than its dc value if the inductor's self-resonance frequency is close to the frequency of interest. R models the series resistance of the inductor, including the skin effect. C_{s1} and C_{s2} model the parasitic coupling to the substrate. R_{s1} and R_{s2} model the substrate losses.

The pi model cannot be used to model the mutual magnetic coupling effects. To model the mutual coupling, FastHenry [23], a tool to extract self, mutual inductance and resistance of arbitrary conductor structures, was used.

Each symmetric half of the designed differential inductor is segmented into 3 spirals connected in series. Then the self inductance, resistance associated with each coil and the mutual coupling between any coil to every other coil was obtained using FastHenry. The parasitic capacitances associated with the segmented coils were extracted from the inductor layout in CADENCE. The extracted capacitances were lumped at the ends of the corresponding spirals. Finally the series resistances were scaled by a suitable factor to incorporate the substrate losses. Fig. 6.2 shows the schematic of the inductor model with the parameters obtained for the designed inductor.

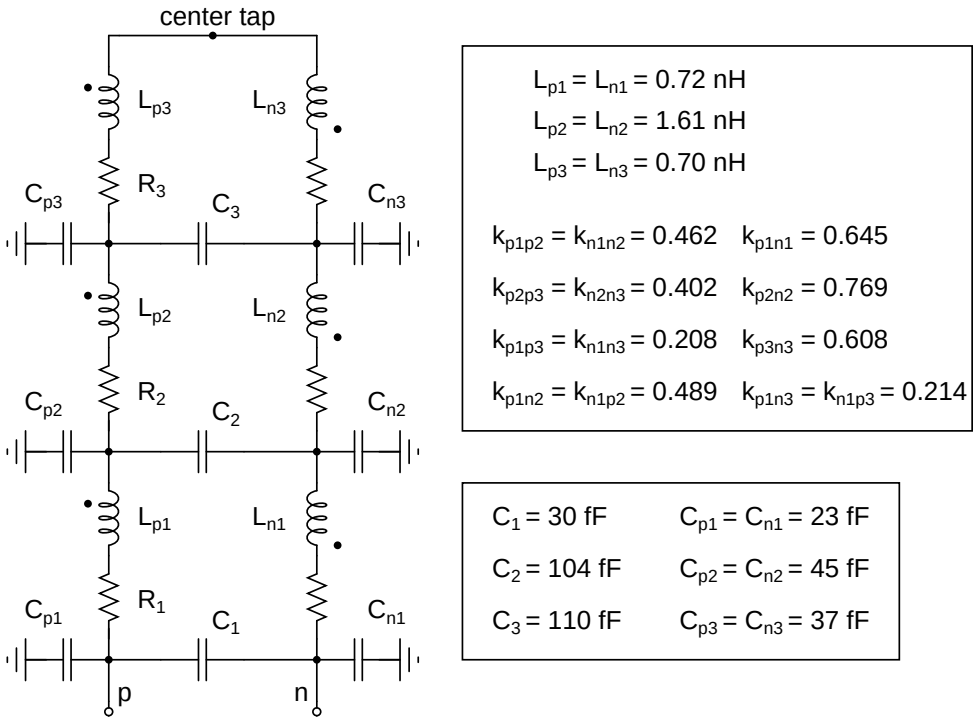

Figure 6.2: Inductor model used to capture the mutual magnetic coupling effects.

6.6 Simulation results for the inductor model

The differential inductor designed required additional 200 fF capacitance single ended to be added externally to center the LC tank at 2.44 GHz. The LC tank's impedance when the excitation was differential-mode and common-mode was simulated as a function of frequency and shown in Fig. 6.3. From the impedance plots it is clear that a CMRR of around 27 dB is obtained in the desired band from the differential LC tank alone.

The differential inductor was incorporated as the LNA load. The common-mode and differential-mode gain from the input of LNA transconductors as a function of frequency is shown in Fig. 6.4. The CMRR in the desired band is around 37 dB. The additional 10 dB of CMRR is due to the tail current source of the differential pair used in the LNA.

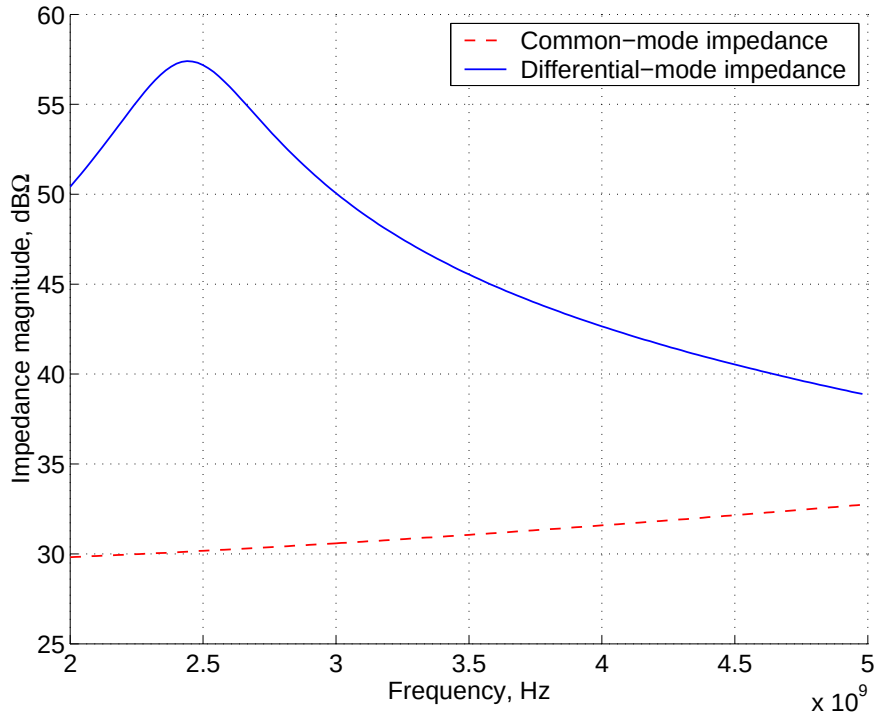

Figure 6.3: Impedance of the differential LC tank for common-mode and differential-mode excitations.

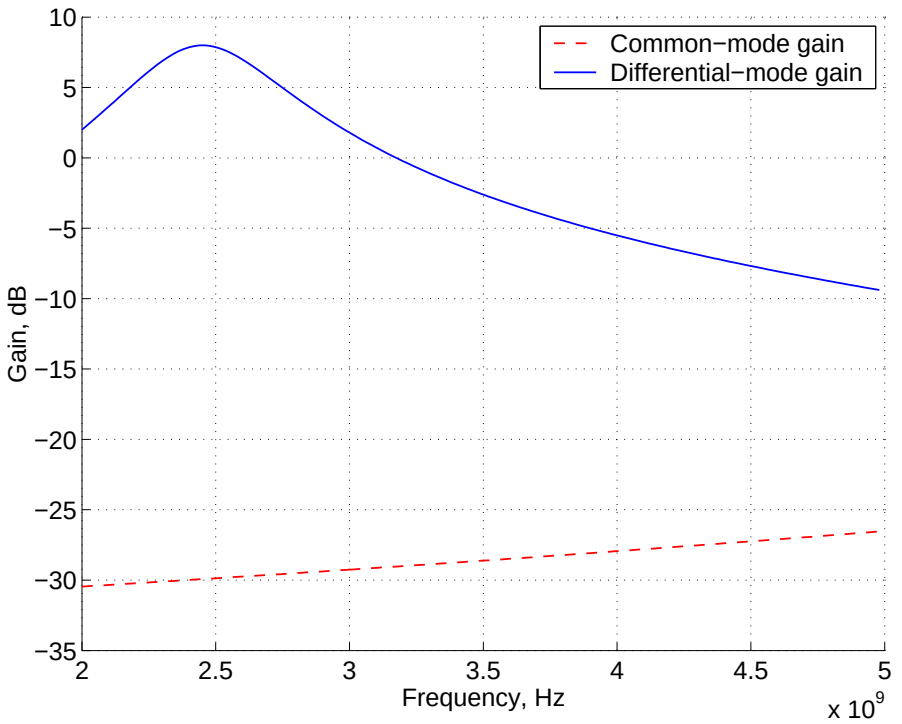

Figure 6.4: Common-mode and differential-mode gain from the input of the LNA transconductor to the LC load.

CHAPTER 7

Conclusion

Low power RF front-end blocks, namely, the low noise amplifier, quadrature down-conversion mixer, and quadrature up-converter, to be used in a IEEE 802.15.4 compliant ZigBee transceiver have been designed, laid out and verified through simulations in UMC 0.18 μm CMOS process.

7.1 Future work

- Integration of the designed blocks with the other blocks to complete the full transceiver design is to be done.
- The complete transceiver chip will be sent for fabrication.
- A test board is to be designed for the transceiver chip.
- Baseband signal processing algorithms for signal detection from the I/Q data from the ADC has to be implemented. A dc offset correction algorithm has to be implemented to remove static and dynamic dc offsets.

APPENDIX A

Output device current noise calculation for the inductively degenerated common source input stage

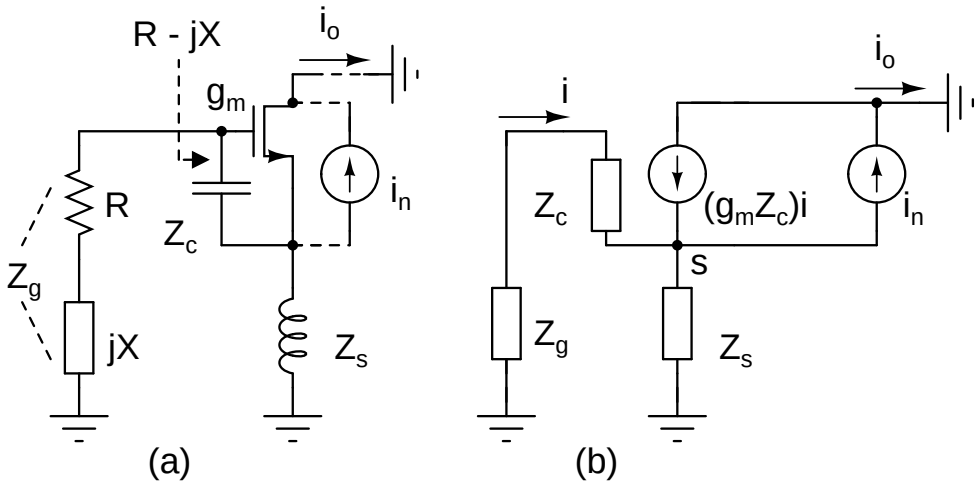

Figure A.1: Calculation of the output device noise current for the inductively degenerated common source input stage.

Refer to the inductively degenerated common source input stage, at the frequency of impedance match, shown in Fig. A.1(a). i_o is to be obtained at this frequency.

The three equations required to solve for i_o are as follow,

$$i_o = i_n - (g_m Z_c)i \tag{A.1}$$

$$i + (g_m Z_c)i - i_n = \frac{v_s}{Z_s} \tag{A.2}$$

$$v_s = -i(Z_g + Z_c) \tag{A.3}$$

Solving the above equations,

$$i_o = \frac{i_n}{1 + \frac{g_m Z_c Z_s}{Z_s + Z_g + Z_c}} \tag{A.4}$$

At the frequency of impedance match, $Z_s + Z_g + Z_c$ reduces to R_{eq} since Z_s is purely inductive and Z_c is purely capacitive. So,

$$\begin{aligned} i_o &= \frac{i_n}{1 + \frac{g_m \left(\frac{1}{sC}\right)(sL_s)}{R_{eq}}} \\ &= \frac{i_n}{1 + \frac{R_{eq}}{R_{eq}}} \\ &= \frac{i_n}{2} \end{aligned} \tag{A.5}$$

$$\tag{A.6}$$

$$\begin{aligned} S_{i_o} &= \frac{S_{i_n}}{4} \\ &= \frac{4\gamma k T g_m}{4} \\ &= \gamma k T g_m \end{aligned} \tag{A.7}$$

APPENDIX B

NF calculation for the resistively terminated common source LNA in the low gain mode

Refer to the single-ended version of the resistively terminated common source LNA, in the low gain mode, as shown in Fig B.1.

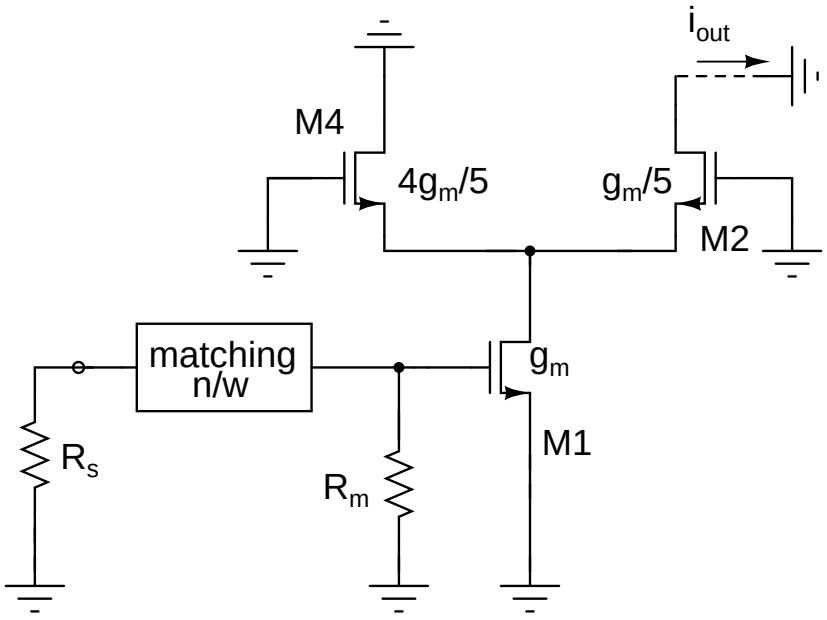

Figure B.1: Single-ended version of the resistively terminated common source LNA in the low gain mode.

The noise contribution from all the noisy elements to the output current noise spectral density is obtained as follows,

Defining $\alpha = \dfrac{\dfrac{g_m}{5}}{\dfrac{g_m}{5} + \dfrac{4g_m}{5}} = \dfrac{1}{5}$,

Contribution from R_s:

$$S_{i_{out},R_s} = \frac{4kTR_s}{4} \times \frac{R_m}{R_s} \times g_m^2 \times \alpha^2 \tag{B.1}$$

Contribution from R_m:

$$S_{i_{out},R_m} = \frac{4kTR_m}{4} \times g_m^2 \times \alpha^2 \tag{B.2}$$

Contribution from M1:

$$S_{i_{out},M1} = 4\gamma kTg_m \times \alpha^2 \tag{B.3}$$

Contribution from M2:

$$S_{i_{out},M2} = 4\gamma kT\frac{g_m}{5} \times (1-\alpha)^2 \tag{B.4}$$

Contribution from M4:

$$S_{i_{out},M4} = 4\gamma kT\frac{4g_m}{5} \times \alpha^2 \tag{B.5}$$

The Noise Factor is now given by,

$$\begin{aligned} \text{Noise Factor} &= \frac{S_{i_{out},R_s} + S_{i_{out},R_m} + S_{i_{out},M1} + S_{i_{out},M2} + S_{i_{out},M4}}{S_{i_{out},R_s}} \\ &= 2 + \frac{4\gamma}{g_m R_m}\left(1 + \frac{1}{5}\left(\frac{1-\alpha}{\alpha}\right)^2 + \frac{4}{5}\right) \qquad \text{(B.6)} \\ &= 2 + \frac{4\gamma}{g_m R_m}(5) \qquad \text{(B.7)} \end{aligned}$$

It is observed that in the noise factor expression, contribution from the active devices alone has increased by the gain step factor of 5, compared to the high gain mode noise factor expression, given in equation 3.7. This degradation arises from the cascode stage transistors implementing the variable gain function.

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