Design of a Tunable Passive Integrated Lowpass Filter

A Project Report

submitted by

SAMEER SINGH

in partial fulfilment of the requirements
for the award of the dual degree of

BACHELOR OF TECHNOLOGY
and
MASTER OF TECHNOLOGY

DEPARTMENT OF Electrical Engineering
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.

May 30, 2010

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a Tunable Passive Integrated Lowpass Filter**, submitted by **Sameer Singh**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr.Nagendra Krishnapura
Project Advisor
Assistant Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai
Date: May 30, 2010

ACKNOWLEDGEMENTS

I think I lucked out when the institute administration assigned Dr. Nagendera Krishnapura as my faculty advisor. Throughout the three and a quarter odd years that I spent shrinking spirals, he made me feel so comfortable, even in the tense environs of VLSI labs, that my two projects (and a half-baked unfinished one) felt more like pursuing a cherished hobby. His passion for circuitry rubbed of on me too, which made the whole process of testing Abhishek's filter and assisting in analog circuits lab course all the more enjoyable. I cannot thank you enough sir, for being so patient with me.

I would also like to thank Dr. Shanthi Pavan and Dr. Bhaskar Ramamurthy for teaching their courses on communication systems and analog circuits without using abstract mathematics and relating them to real mechanics. The twenty something credits I did under them were the only ones I could stay fully awake in without the help of department's coffee shop.

I thank all my friends in VLSI and DSD Labs Ankur, Sandeep, Jishnu, Sreelakshmi and Lokesh's for their refreshing companionship and project related discussions. During the days that I was testing, help from my seniors Siva, Prabu, Shankar, Vallabh, Chembian and Deepa proved invaluable for debugging the test board. Even later I found Prabu and Shankar lending their time without a second thought whenever I needed their advise. I can only hope to find such colleagues at my future workplace.

The company and support of Atulya, Satyavrat and gang helped me put up with Chennai during my extended stay as a Dual Degree student. Of course, Yash's impeccable comic timing needs a special menion here.

Finally, I would like to dedicate this work to my Ma and Didis who had to

endure with my endless campus life induced tantrums, making me their priority during a decade that has been so tough on all of us. I guess I have been really fortunate to have such awesome understanding parents and siblings. But then, as Page and Plant have said:

This is the mystery of the quotient
Upon us all a little rain must fall

ABSTRACT

This project involves the design of a lowpass LC ladder filter, implementing a Fifth order Butterworth transfer function, which is tunable between 400 MHz to 1 GHz in four steps. The filter is designed in 180 nm UMC CMOS technology with a supply voltage of 1.8 V. In an attempt to reduce total chip area, the inductors of the passive ladder are realized using a single coil tapped at multiple points to make use of positive mutual coupling. Also, the use of MOS transistors in accumulation with high specific capacitance, instead of the more linear metal-metal capacitors is explored. The complete laid out filter occupies an area of 1220 μ m$\times$740 μm out of which two-thirds is occupied only by the top most metal layer. The output is driven using test buffers for accurate measurement of filter characteristics.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS **i**

ABSTRACT **iii**

LIST OF FIGURES **1**

1 Introduction **2**

1.1 Motivation 2

1.2 Organization of the thesis 3

2 Filter architecture and implementation **4**

2.1 Filter Transfer Function 4

2.2 Implementation 4

2.3 Lossy Inductors 6

2.4 Loading Effects 10

2.5 Bandwidth Tuning 11

2.6 Element Values 14

3 Single spiral with multiple taps for ladder filter **17**

3.1 Modeling mutual coupling 17

3.2 Implementation of the spiral 18

3.3 Area comparison 22

3.4 Modeling of spiral in spectre 23

3.4.1 Distributed model 24

3.4.2 3-port system 25

4 Input Gm-cell **27**

4.1 Design 27

4.2 Simulation results 29

5 MOS capacitors for the ladder filter 31

5.1 Region of operation 31

5.2 Resistance offered by MOS capacitor 34

5.3 Effect on filter's linearity 36

6 Fifth order tunable passive Butterworth ladder filter using MOS capacitors 39

6.1 Bias generation and distribution 39

6.2 Termination resistor bank 41

6.3 Digital logic 41

6.4 5^{th} order LC ladder 42

6.5 Test buffer 43

7 Layout and Simulation Results 52

7.1 Layout 52

7.2 Simulation Results 52

7.2.1 AC simulations 53

7.2.2 Distortion and noise analysis 54

7.2.3 Step response 55

8 Conclusion and future work 61

8.1 Conclusion 61

8.2 Future work 61

LIST OF FIGURES

2.1 Poles and Magnitude Response of a normalized Butterworth . . 5

2.2 (a)Doubly terminated ladder (b)Singly terminated ladder 6

2.3 A spiral inductor and its equivalent circuit 7

2.4 Passive ladders implementing (a)$H(s)$, (b)$H(s-\delta)$ and (c)$H_{shifted}(s)$ 9

2.5 Poles and Magnitude plot of $H(s)$, $H(s-\delta)$ and $H_{shifted}(s)$ . . 10

2.6 Using a Gm-cell at input 11

2.7 Poles of upscaled and downscaled transfer functions. Poles of $H(s)$ and $H_{shifted}(s)$ of 1 rad/sec filter coincide. 14

2.8 Magnitude response for $n = 1.4$ 15

2.9 Single ended representation of final ladder and capacitor banks . 16

3.1 (a) Ladder with coupling between inductors, (b)Equivalent circuit with uncoupled inductors 18

3.2 Cancelling negative inductance M_{12} 19

3.3 Mutual coupling between three inductors and their circuit equivalent using uncoupled inductors 20

3.4 Layout of the full spiral in Virtuoso 21

3.5 Comparison of areas of single ended separate coils and a single tapped coil 23

3.6 Distributed pi-model of a sample inductor 25

3.7 Inductor as a 3-port system 26

4.1 A source degenerated nMOS 27

4.2 Schematic of the input Gm-cell 28

4.3 Variation of IM3 with input amplitude and frequency 30

5.1 (a) Cross section of a MOS capacitor (b) Voltage along a vertical cross-section with respect to Bulk (V_x) 32

5.2 CV characterstics of a typical MOS capacitor 33

5.3 (a)Representation of a MOS capacitor with series losses (b)Accumulation channel's resistance (c)Gate polysilicone resistance 35

5.4 IM3 vs Frequency comparison 37

5.5 Distortion comparison between Gm-cell and Moscaps 38

6.1 Block diagram of the filter with test buffers 40

6.2 Schematic for bias distribution amongst Gm-cells 45

6.3 Voltage and current references generation for Gm-cell and test buffers 46

6.4 Single ended schematic of termination resistor bank 46

6.5 Schematic for binary to thermometer code generation 47

6.6 Differential schematic and element values of capacitor banks implementing C_1 and C_2 and their respective shunt conductances . . 48

6.7 Differential schematic and element values of capacitor bank implementing C_3 49

6.8 Circuit implementation of the test buffer 50

6.9 Squared output noise for direct and filter paths 51

6.10 Comparison between distrotion levels of the filter and the buffer as a standalone device 51

7.1 Layout of the Filter with test buffers 56

7.2 Magnitude response of filter tuned for four bandwidths 57

7.3 Squared output noise of the four filter modes 58

7.4 Normalized step response of the four filters 59

7.5 Close-up of step response to look for undershoot 60

CHAPTER 1

Introduction

1.1 Motivation

Passive LC ladder filters are the oldest of all known architectures and the simplest (in terms of necessary components) implementation of a given transfer function. They require no power supplies, are not resticted by bandwidth limitations (as are opamp active-RC filters) and have a much wider dynamic range when compared to other types of design. But without active elements they cannot provide signal gain. Practical values of input and output impedances in a passive filter are too low for many applications. Most importantly they use bulky and untunable components. Essentially, the size of inductors and capacitors restrict the minimum bandwidth for which these filters can be used which ususally is a couple of GigaHertz and above.

To overcome these disadvantages, active designs are used at lower frequencies. Opamp-RC filters with careful circuit design can achieve very good accuracy withing the amplifier's operating frequency range, i.e. hundreds of kiloHertz. OTA-C filters are another popular architecture because of their wide frequency range of operation. Although these filters have limited linearity they provide reasonable performance till approximately 300 MHz.

The above discussion clearly presents need for a filter design with its bandwidth in the frequency range of 300 MHz to 1 GHz. In this thesis we explore a passive ladder architecture which can be operated in hundreds of MegaHertz range without letting the total chip area to get out of hand. Also, the filter is made tunable from 400 MHz to 1 GHz in four steps without changing the inductor spiral. The theory and design of each building block of the filter are discussed. The simulated results of the final layout extracted filter are presented and discussed.

1.2 Organization of the thesis

Chapter 2 introduces the filter type and architecture and touches upon its implementation.

Chapter 3 explains how a single spiral with multiple taps can be used to reduce the area occupied by filter's inductors.

Chapter 4 presents the design of the input voltage controlled current source.

Chapter 5 explores the use of MOS capacitors in accumalation instead of metal-metal capacitors for use in the LC ladder.

Chapter 6 presents the design of a Fifth Order Tunable Passive Butterworth Ladder Filter using MOS Capacitors.

Chapter 7 discusses the simulation results of the filter including lay out parasitics.

Chapter 8 presents the conclusion and scope of future work.

CHAPTER 2

Filter architecture and implementation

2.1 Filter Transfer Function

The magnitude response $|H(j\omega)|$ of a lowpass Butterworth filter with n poles is

$$|H(j\omega)| = \sqrt{\frac{1}{1+\omega^{2n}}} \tag{2.1}$$

Normalized for a band edge of 1 rad/sec, the transfer function $H(s)$ for such a filter with n=5 looks like

$$H(s) = \frac{1}{1+3.236s+5.236s^2+5.236s^3+3.236s^4+s^5} \tag{2.2}$$

As we can see the set of five poles (referenced hereon as a vector $[p]$) of this Butterworth function fall on a unit circle centered at origin:

$p_{1,2} = -0.3090 \pm 0.9510j$

$p_3 = -1.0000$

$p_{4,5} = -0.8090 \pm 0.5877j$

Poles and Magnitude response of $H(s)$ are shown in Fig. 2.1

2.2 Implementation

The LC ladder used for implementing this 5^{th} order function can be either singly or doubly terminated. The magnitude response of a ladder with equal termination resistances at both input and output is less sensitive to its components' values, but has attenuation of 6 dB at DC. Since, the inductors are also lossy it translates

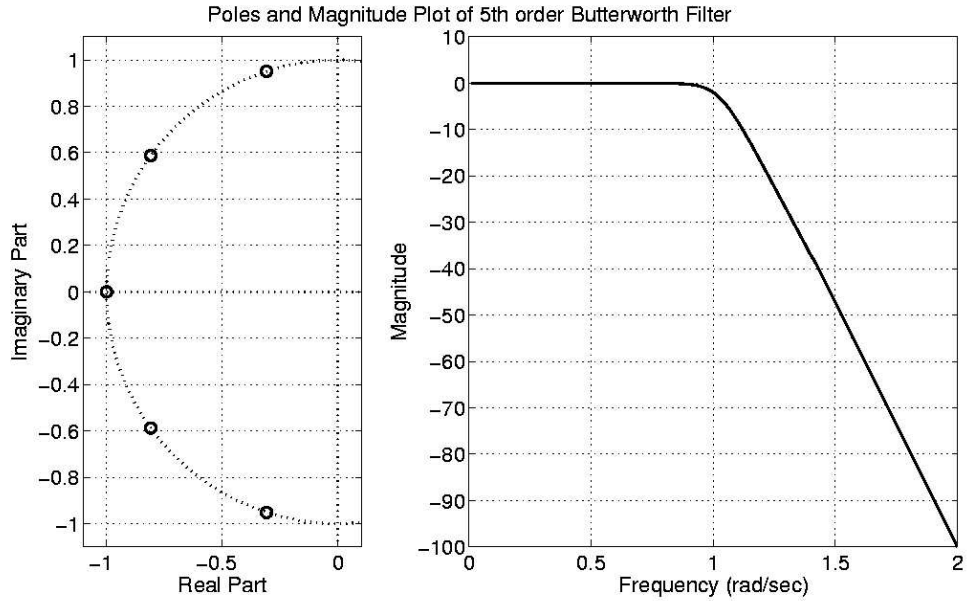


Figure 2.1: Poles and Magnitude Response of a normalized Butterworth

to an even lower pass band gain for the filter's transfer function. Thus, a singly terminated ladder structure is chosen (with termination resistance on the input side) and capacitances and inductances calculated accordingly.

The transfer function realized by a singly terminated ladder is:

$$H(s) = \frac{1}{(1+sRC_3)[(1+s^2C_1L_1)(1+s^2C_2L_2)+s^2C_1L_2]+sRC_2(1+s^2C_1L_1)} \tag{2.3}$$

A filter with band edge at 1 rad/sec and with termination resistance (R) of $1\,\Omega$ can be realized using:

$L_1 = 1.694\,\mathrm{H}$, $L_2 = 0.8944\,\mathrm{H}$

$C_1 = 1.545\,\mathrm{F}$, $C_2 = 1.382\,\mathrm{F}$, $C_3 = 0.3090\,\mathrm{F}$

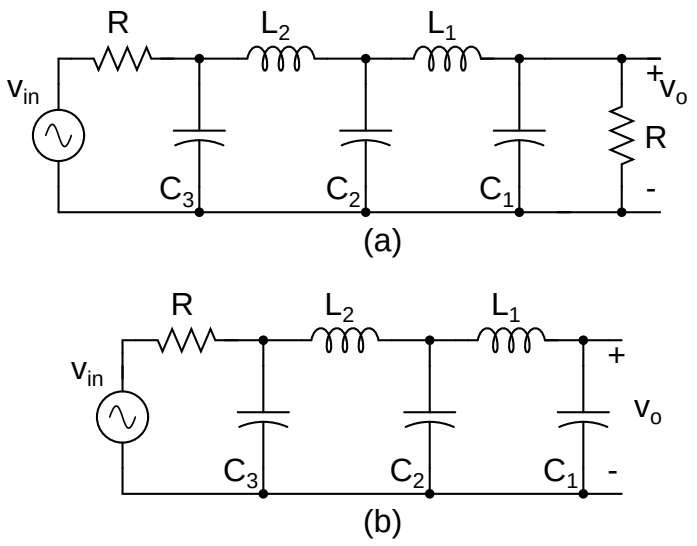


Figure 2.2: (a)Doubly terminated ladder (b)Singly terminated ladder

2.3 Lossy Inductors

Inductors are implemented on ICs as spirals using metal tracks. Their performance depends on parameters like their length, number of turns, spacing between tracks, track width, oxide thickness, number of layers, etc. A basic π model of the inductor is shown in Fig. 2.3. L_s is the sum of self and mutual inductances of the coil and C_s is the lumped representation of sidewall capacitances between adjacent turns of a spiral. Except for the series resistance (r_s) all components in the model are parasitics. Effect of oxide (C_{ox}) and bulk capcitances (C_{Si}) between metal tracks and substrate is discussed in Chapter 3.

The quality factor Q of an inductor is the ratio of its inductive reactance to its resistance at a given frequency, and is a measure of its efficiency. The filter response can be made impervious to r_s provided the quality factors of all inductors are equal and above a certain threshold. The aim is to make the magnitude response of the lossy filter proportional to that of an ideal or lossless filter by modifying the element values.

A simple model for lossy elements would be to assume each inductance L in series with a resistance r and each capacitance with a conductance g in parallel

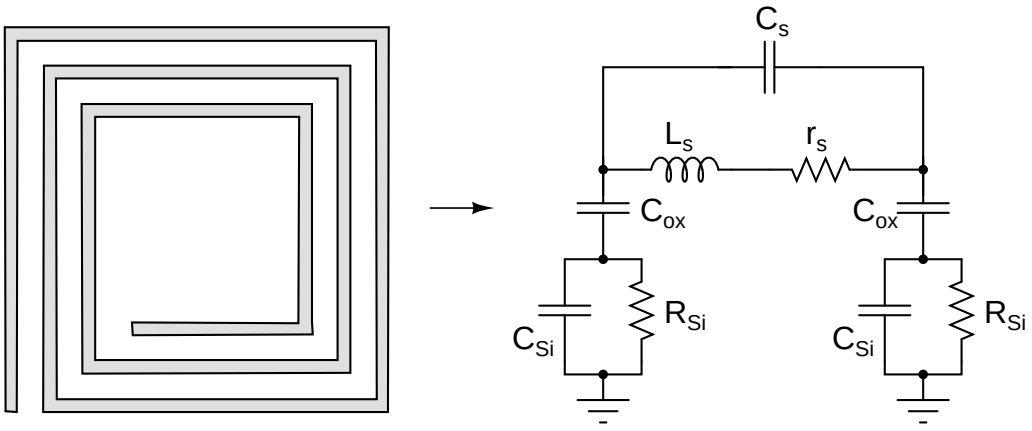


Figure 2.3: A spiral inductor and its equivalent circuit

with it. Then the impedance offered by these lossy elements is:

$$Z_L(s) = sL + r = L(s + \frac{r}{L}) = L(s + \delta_L) \tag{2.4}$$

$$Z_C(s) = \frac{1}{sC + g} = \frac{1}{C(s + \frac{g}{C})} = \frac{1}{C(s + \delta_C)} \tag{2.5}$$

If the quality factors of all the elements in the afore mentioned ladder are equal, i.e $\delta_{Li} = \delta_{Cj} = \delta$ for $i = 1, 2$ and $j = 1, 2, 3$ then

$$Z_{Li}(s) = L(s + \delta) \tag{2.6}$$

$$Z_{Cj}(s) = \frac{1}{C(s + \delta)} \tag{2.7}$$

When these new impedance functions are substituted in Eq. 2.2 all the s terms are replaced by $s + \delta$. Hence, the transfer function can now be written as $H(s + \delta)$ instead of $H(s)$. This is equivalent to shifting the $j\omega$ axis in s-plane towards right by δ rad/sec. This should also be evident from the fact that since now instead of ideal, lossless elements we are using lossy inductors and capacitors which have a finite quality factor, the ratio $Im([p])/Re([p])$ decreases.

The lowpass filter realized by $H(s+\delta)$ is not the Butterworth transfer function we wanted. Instead, due to low quality factor, roll off of magnitude is not as sharp and there is some attenuation in the pass band which reduces the filter's 3 dB bandwidth. To retain the earlier Butterworth function, these poles have to be shifted to left by the same amount, i.e. δ rad/sec. To achieve this shift, new element values need to be calculated such that the lossless prototype ladder's transfer function, $H_{highQ}(s)$, has poles shifted towards $j\omega$ axis by δ, which in presence of lossy elements move away from imaginary axis by δ. Thus, $H_{highQ}(s)$, the transfer function of lossless prototype ladder filter is given by $H_{highQ}(s) = H(s-\delta)$ where $H(s)$ is the desired transfer function.

For demonstration purposes, value of quality factor Q at 1 rad/sec is taken to be 5 in this chapter. This makes $\delta = r/L = g/C = 0.2$ rad/sec. Poles of $H_{highQ}(s)$ should be $[p] + \delta$, i.e.,

$p_{1,2} = -0.1090 \pm 0.9510j$

$p_3 = -0.8000$

$p_{4,5} = -0.6090 \pm 0.5877j$

From the above numbers we can easily see that the minimum required value of Q for this method to work is decided by the pair of poles closest to imaginary axis. For H_{highQ} to be stable and realizable using real elements all poles should lie in left half s-plane. Thus, the maximum δ possible for a fifth order Butterworth function is 0.309 rad/sec.

Our new transfer function which needs to be realize using lossy components is

$$H_{highQ}(s) = H(s-\delta) = \frac{1}{1 + 3.188s + 5.314s^2 + 5.802s^3 + 4.258s^4 + 1.904s^5} \tag{2.8}$$

A ladder which realizes $H_{highQ}(s)$ is shown in Fig. 2.4. It should be noted that resistors have been added in parallel with all the capacitors to achieve the

required quality factor, because the capacitors used in IC design have very low inherent loss and their Q approaches infinity. But, adding shunt conductances also means that at low frequencies there is some attenuation in signal. This is the reason we started of with a termination only at the input's side instead of a doubly terminated ladder so that the overall attenuation in pass band of filter is not too high. Pass band attenuation depends on the ratio of shunt resistors and termination resistance. This effectively means higher the quality of elements at our disposal, lower is the filter's DC attenuation.

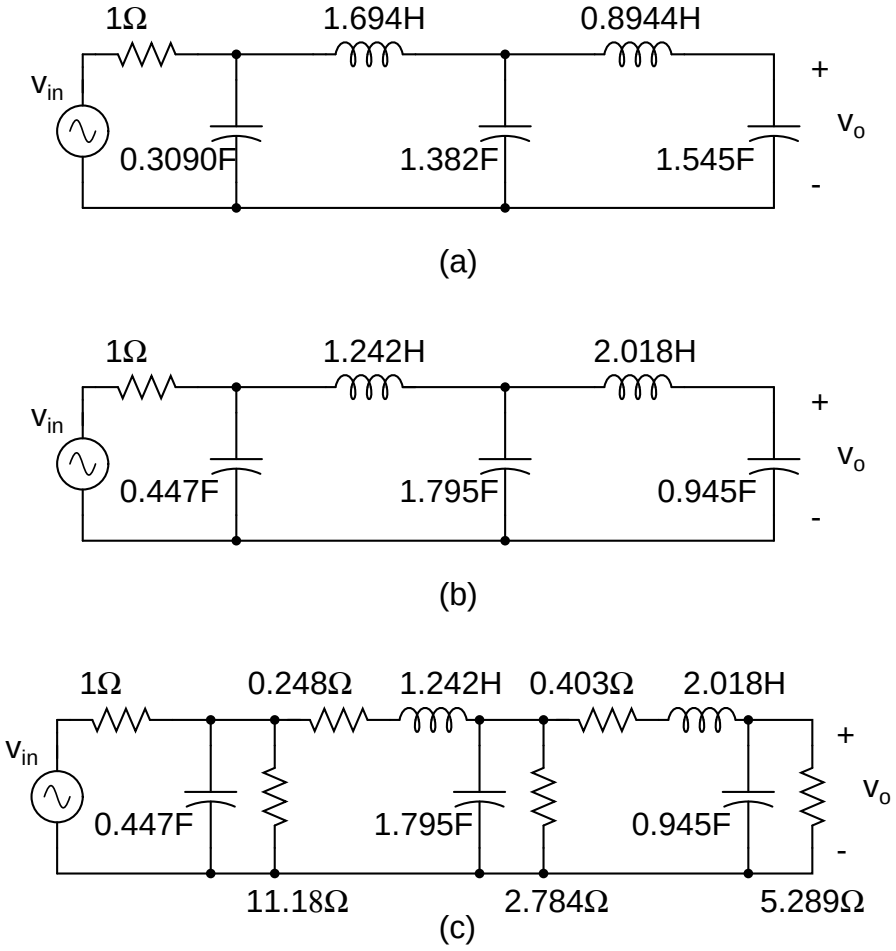


Figure 2.4: Passive ladders implementing (a)$H(s)$, (b)$H(s-\delta)$ and (c)$H_{shifted}(s)$

The transfer function realized by this lossy ladder is proportional to the ideal Butterworth response and is represented by:

$$H_{shifted}(s) = \frac{1}{1.904 + 6.162s + 9.970s^2 + 9.970s^3 + 6.162s^4 + 1.904s^5} \quad (2.9)$$

$$= \frac{0.5252}{1 + 3.236s + 5.236s^2 + 5.236s^3 + 3.236s^4 + s^5} \quad (2.10)$$

$$= 0.5252 \times H(s) \quad (2.11)$$

Fig. 2.5 compares the poles and magnitude response of the three transfer function discussed, i.e. an ideal Butterworth ($H(s)$ Fig. 2.4(a)), lossless prototype with poles shifted towards $j\omega$ axis ($H(s-\delta)$ Fig. 2.4(b)) and its implementation with lossy capacitors and inductors ($H_{shifted}(s)$ Fig. 2.4(c)).

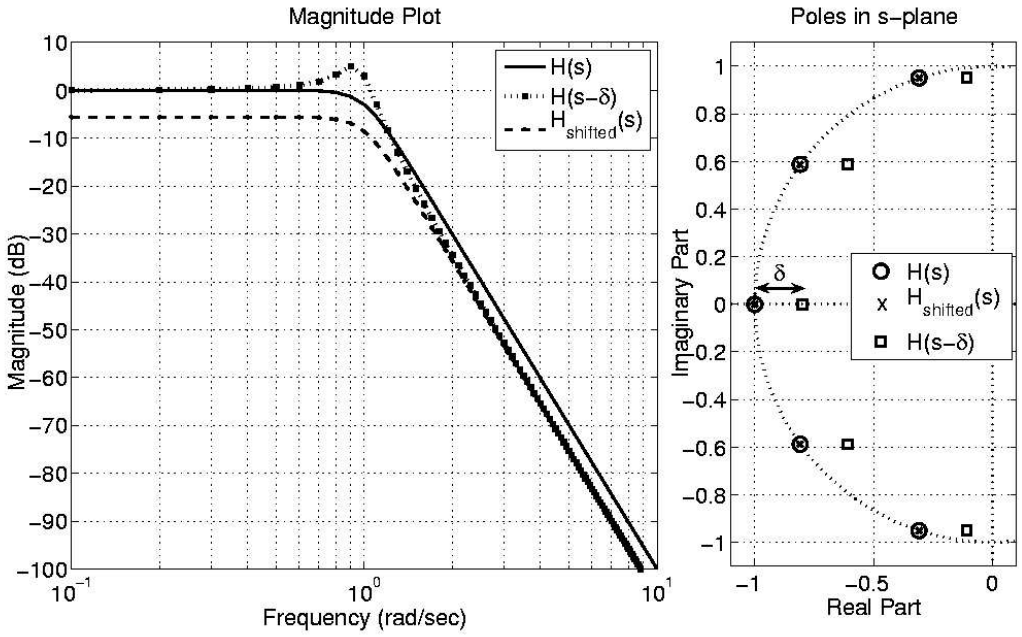


Figure 2.5: Poles and Magnitude plot of $H(s)$, $H(s-\delta)$ and $H_{shifted}(s)$

2.4 Loading Effects

This design will be used as a part of a larger design and does not act as a standalone filter, i.e. it will follow and be followed by different blocks. To minimize the effect of loading it should have a very high input impedance. But since the passive

ladder has a finite input impedance, it is driven using a voltage controlled current source (vccs). This can be done by converting input voltage source to its norton equivalent and replacing the current source by an input Gm-cell.

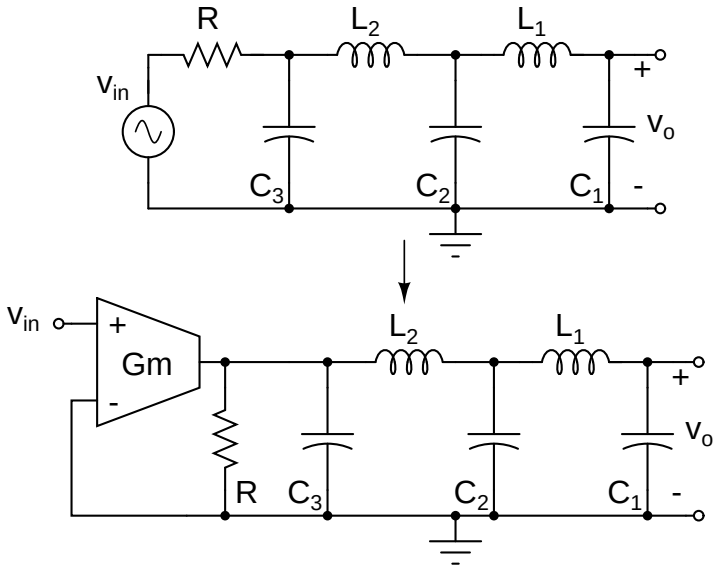


Figure 2.6: Using a Gm-cell at input

To maintain same DC gain as before the transconductance of this Gm-cell has to be $1/R$. Rest of the filter is made of passive components whose characterstics do not depend on their operating point and this block is the only source of distortion. Since, output noise is also dominated by the Gm-cell, the only other noise source being low-valued resistors used in ladder, swing limits and dynamic range of input signal are limited by its performance. Its implementation is discussed later in Chapter 6.

2.5 Bandwidth Tuning

The filter is desired to be operable in hundreds of megahertz range with its band width tunable from 400 MHz to 1 GHz in four steps. Usually when a filter's bandwidth needs to be increased by a factor n, it can be easily done by multiplying each element (except the termination resistance) by $1/n$. But tuning a spiral by adding/removing segments to obtain four different values of inductances proves to

be very cumbersome. Another way would be to have four separate spirals and to connect them in series as and when required. But to avoid the effect of mutual coupling between these coils they have to be placed far apart, which means using much more chip area than before and adding to losses due to resistance offered by interconnects and switches.

Therefore to avoid these practical problems, the inductor is left untouched and the bandwidth is tuned by changing the values of the three capacitances and termination resistance. This also means that quality factor Q of the elements remains same for all bandwidths. From the denominator in Eq. 2.3, a_i (the coefficients of s^i) can be written as,

$a_0 = 1$

$a_1 = R(C_1 + C_2 + C_3)$

$a_2 = C_1L_1 + (C_1 + C_2)L_2$

$a_3 = RC_3(C_1L_1 + (C_1 + C_2)L_2) + RC_1C_2L_1$

$a_4 = C_1C_2L_1L_2$

$a_5 = RC_1C_2C_3L_1L_2$

To decrease the 3 dB bandwidth (ω_{3dB}) by a factor n, the transfer function has to be changed from $H(s)$ to $H(n \times s)$, i.e. coefficients in the denominator should change from a_i to $a_i \times n^i$. Looking at their dependence on element values above and keeping in mind that L_1 and L_2 stay unchanged, ω_{3dB} can be converted to ω_{3dB}/n by

$C \longrightarrow C \times n^2$

$R \longrightarrow \frac{R}{n}$

As seen before, poles of an ideal Butterworth system fall on a circle of radius ω_{3dB} rad/sec centered at the origin. Hence, poles of $H(s)$ and $H(n \times s)$ lie on concentric circles with radii 1 rad/sec and $1/n$ rad/sec. But since the ratio $\delta = r/L$ remains same in both cases, $H_{shifted}(s)$ does not translate to an ideal Butterworth after frequency scaling. This happens because along with s, δ also needs to be multiplied by n to retain similar transfer function across bandwidths.

$H(s) \longrightarrow H(n \times s)$

$H(s-\delta) \longrightarrow H(n \times s - \delta) = H(n \times (s - \frac{\delta}{n}))$ instead of $H(n \times (s-\delta))$

In other words, for lower bandwidth filters the quality factor required to obtain back the ideal Butterworth transfer function keeps increasing. This can be easily seen from the fact that since poles of $H(n \times s)$ keep moving towards the $j\omega$ axis with increasing n, the value of δ which pushes the pole to right half s-plane goes on decreasing. Since, we cannot keep changing the r/L ratio for different frequencies, its effect has to be studied and then minimized.

When new element values extracted from $H(n \times s - \delta)$ are used in the lossy ladder, the poles are still pushed away from the imaginary axis by same δ rad/sec. Hence, the poles of $H_{shifted}(n \times s)$ end up not on the circle centered at the origin but $k1 = \delta \times (1 - 1/n)$ rad/sec to its left. This means its magnitude response will not have the flat Butterworth response, instead there is some pass band attenuation and the roll off is not as sharp.

If the bandwidth needs to be scaled up, we face a similar problem. ω_{3dB} can be converted to $\omega_{3dB} \times n$ by changing $H(s)$ to $H(s/n)$, which means,

$C \longrightarrow \frac{C}{n^2}$

$R \longrightarrow R \times n$

Again the poles of $H_{shifted}(s/n)$ are off from the ideal Butterworth by $k2 = \delta \times (n-1)$ rad/sec. But this time the poles have been pushed towards the $j\omega$ axis which means the magnitude response peaks within the pass band and the roll off does not get any worse. This effect is muted a little during actual implementation of the filter because of the finite resistance and parasitic capacitances of switches (used for tuning) in series with capacitors.

Plots in Fig. 2.7 and Fig. 2.8 show the poles and ac magnitude response respectively of $H(s)$, $H_{shifted}(s)$ and $H(s-a)$ for filters with bandedge at 1 rad/sec, 1.4 rad/sec and 0.714 rad/sec.

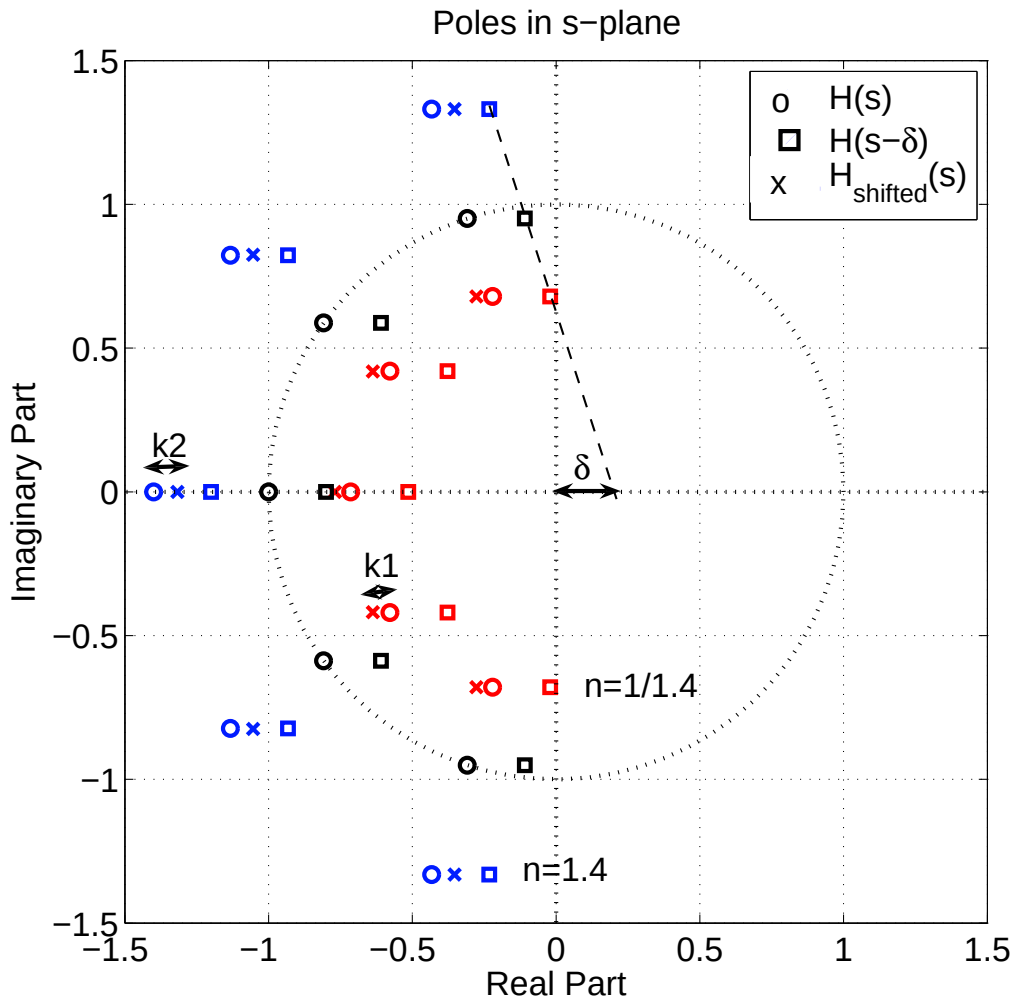


Figure 2.7: Poles of upscaled and downscaled transfer functions. Poles of $H(s)$ and $H_{shifted}(s)$ of 1 rad/sec filter coincide.

2.6 Element Values

Since the filter is to be tuned from 400 MHz to 1 GHz, the mean frequency (700 MHz) is used to calculate all the element values initially. After this, the capacitance and termination resistances are scaled up by $n = 1.428$ and down by $n = 1.75$, which gives comparable $k1$ and $k2$ shifts at either end. For a practical spiral in our process δ turns out to be about 770 Mrad/sec (122 MHz).

The transconductance of the Gm-cell also needs to be scaled accordingly for

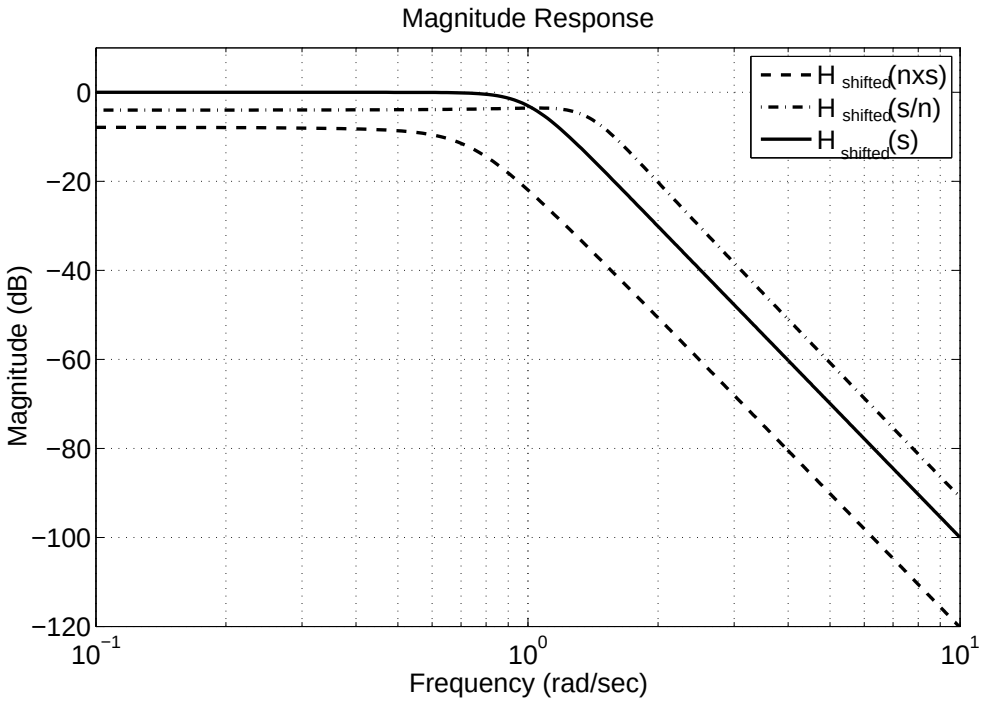


Figure 2.8: Magnitude response for $n = 1.4$

maintaining the DC gain. This is done by switching on and off identical Gm-cells connected in parallel. Each of these cells have a transconductance of 6.66 mS. Elements' values for the four different bandwidths are tabulated in 2.1.

Table 2.1: Element Values

Freq(MHz)	$R(\Omega)$	C_1(pF)	C_2(pF)	C_3(pF)
400	30	14	22.81	5.61
500	37.5	8.95	14.6	3.59
666.66	50	5.03	8.21	2.02
1000	75	2.24	3.65	0.89

$L_1 = 23.05\,\text{nH}$

$L_2 = 14.15\,\text{nH}$

For tuning the ladder each capacitor needs to be split into four, which can be connected in parallel using switches for realizing filters of lower bandwidths. The same is done with shunt conductances also. The switches are controlled using 2 binary bits, $b < 0 : 1 >$. Since filter characterstics are most sensitive to the

termination resistance (compared to other resistors used in ladder), it is made programmable with finer steps than required and 3 binary bits ($br<0:2>$) are used for control over different process corners. Although, this resistance needs to be varied from $30\,\Omega$ to $75\,\Omega$ for bandwidth tuning, it is instead made tunable from $24\,\Omega$ to $100\,\Omega$ to account for $\pm 30\%$ change in resistance due to process variations. Fig. 2.9 shows a basic block level implementaion of the ladder and the capacitor banks.

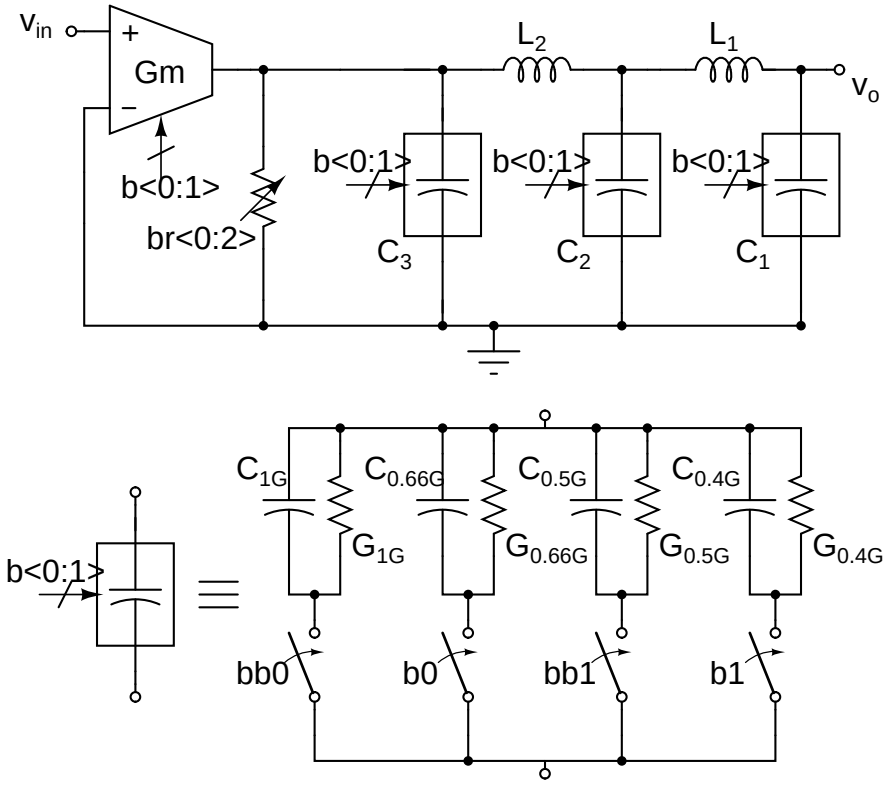


Figure 2.9: Single ended representation of final ladder and capacitor banks

CHAPTER 3

Single spiral with multiple taps for ladder filter

Instead of using separate spirals for realizing L_1 and L_2 in the ladder a single coil can be used which is tapped at three points. This way we can make use of positive mutual coupling between two parts of this coil, hence reducing chip area and relaxing the quality factor constraint (since for the same length of metal we get some extra inductance due to positive coupling). Use of mutual coupling to reduce size of spiral and its effect on a filter's response has been discussed extensively in [1].

3.1 Modeling mutual coupling

Mutual inductance between two adjacent inductors L_1 and L_2 with a coupling coefficient of k_{12} is given by, $M_{12} = k_{12}\sqrt{L_1 L_2}$. These two can be represented in a circuit as two uncoupled inductors of values $L_1 + M_{12}$ and $L_2 + M_{12}$ and an extra inductance $-M_{12}$ in series with C_2. This can be verified by writing KCL equations for schematics (a) and (b) in Fig. 3.1.

$$V_1 = sL_1 I + sM_{12}(I - I_1) + \frac{I_1}{sC_2} \tag{3.1}$$

$$V_2 = -sL_2(I - I_1) - IsM_{12} + \frac{I_1}{sC_2} \tag{3.2}$$

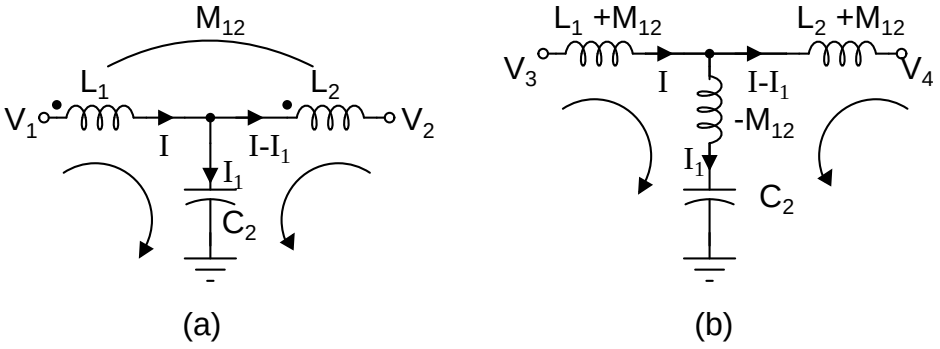


Figure 3.1: (a) Ladder with coupling between inductors, (b)Equivalent circuit with uncoupled inductors

$$
\begin{aligned}
v_3 &= (sL_1 + sM_{12})I - sM_{12}I_1 + \frac{I_1}{sC_2} && (3.3)\\
&= sL_1 I + sM_{12}(I - I_1) + \frac{I_1}{sC_2} && (3.4)\\
v_4 &= -sM_{12}I_1 - (I - I_1)(sL_2 + sM_{12}) + \frac{I_1}{sC_2} && (3.5)\\
&= -sL_2(I - I_1) - IsM_{12} + \frac{I_1}{sC_2} && (3.6)
\end{aligned}
$$

This negative inductance $-M_{12}$ adds a new term in transfer function's numerator, $1 - s^2 M_{12} C_2$, which introduces two right hand s-plane zeros at $\pm\sqrt{1/M_{12}C_2}$. These zeros cause undershoot in the step response and reduced stopband attenuation. But, the positive inductance of interconnect used to tap the spiral and connect C_2 can be used to reduce this effect, as shown in Fig. 3.2. Even if L_3 is not exactly equal to M_{12}, it pushes these zeros to a higher frequency or to the left half plane. But if this interconnect's resistance is large enough, it creates a left half plane zero at $1/C_2 R_{interconnect}$ which lowers the pass band gain.

3.2 Implementation of the spiral

Inductances required in this low pass filter, as mentioned in previous chapter, are 23.05 nH and 14.15 nH. Minimum L/r required to recover a response proportional

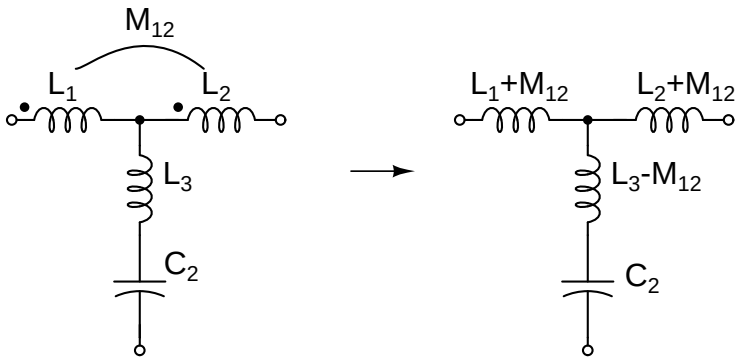


Figure 3.2: Cancelling negative inductance M_{12}

to an ideal Butterworth from a lossy ladder is 1.3 nsec. This fraction sets a minimum limit to how wide the metal tracks need to be. Wider tracks also lead to an increase in the overall spiral size and capacitance to bulk substrate (C_{ox} in Fig 2.3).

Reduced spacing between adjacent turns in a spiral increases its inductance but it means higher capacitive coupling between adjacent segments which brings down the self resonance frequency. This can be modeled with an added capacitance (capacitance between side-walls of tracks) in parallel with the inductance, (C_s), which provides a direct path across the inductor at higher frequencies bringing down the stop band attenuation. Spacing for this design is limited at 3 μm which keeps C_s low enough not to cause any problems in passband and give a stop band attenuation of around -60dB.

Coupling between adjacent turns in on chip coils can go up to 0.6. To reduce coupling between L_1 and L_2, some extra space is left before starting the second spiral. It should be noted that cancelling $-M_{12}$ as discussed in previous section would be so straight forward only if mutual inductance between two coils is small (few tenths of a nanohenry). Any larger L_3 would require an actual coil whose coupling with the two main spirals also needs to be accounted for. Extending the equivalent circuit of two coupled inductors in series, as presented in previous section, to three inductors, i.e. L_a, L_b and L_c of Fig. 3.3, we can get

$$L1 = L_a + M_{ab} + M_{ac} + M_{bc} \tag{3.7}$$

$$L2 = L_b + M_{ab} - M_{ac} - M_{bc} \tag{3.8}$$

$$L3 = L_c + M_{ac} + M_{bc} - M_{ab} \tag{3.9}$$

where,

L_a and L_b are self inductances of two main coils,

L_c is self inductance of coil used for tapping,

M_{ij} is the mutual inductance between L_i and L_j,

L_1 and L_2 are inductances to be realized for the passive ladder

L_3 is the net inductance in series with C_2.

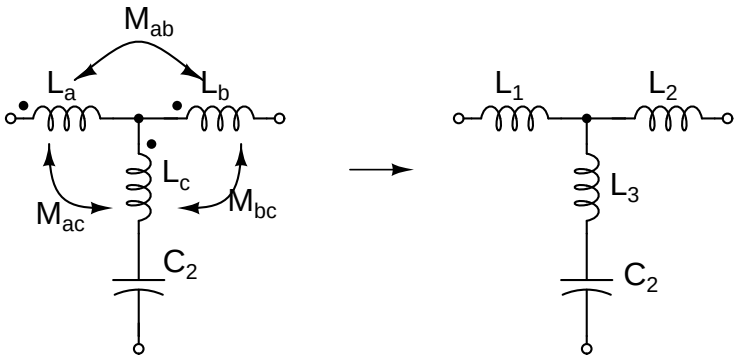


Figure 3.3: Mutual coupling between three inductors and their circuit equivalent using uncoupled inductors

In Fig. 3.3 coupling between the second spiral L_b and L_c, i.e. M_{bc} can be made very small or even negative by making sure that direction of currents in their branches is opposite. Similarly M_{ac} is increased by placing the cancelling coil (L_c) such that magnetic fluxes of the two coils add up. Plot of the final spiral's layout, Fig 3.4 shows one way of doing this. One segment of L_c runs from underneath L_2, but in the opposite sense, so that any positive coupling due to other segments is cancelled out. Although, now the second spiral needs an extra quarter turn to compensate for negative coupling. There is an extra spacing about 75 μm between L_1 and L_2 to keep coupling coefficient down to 0.198.

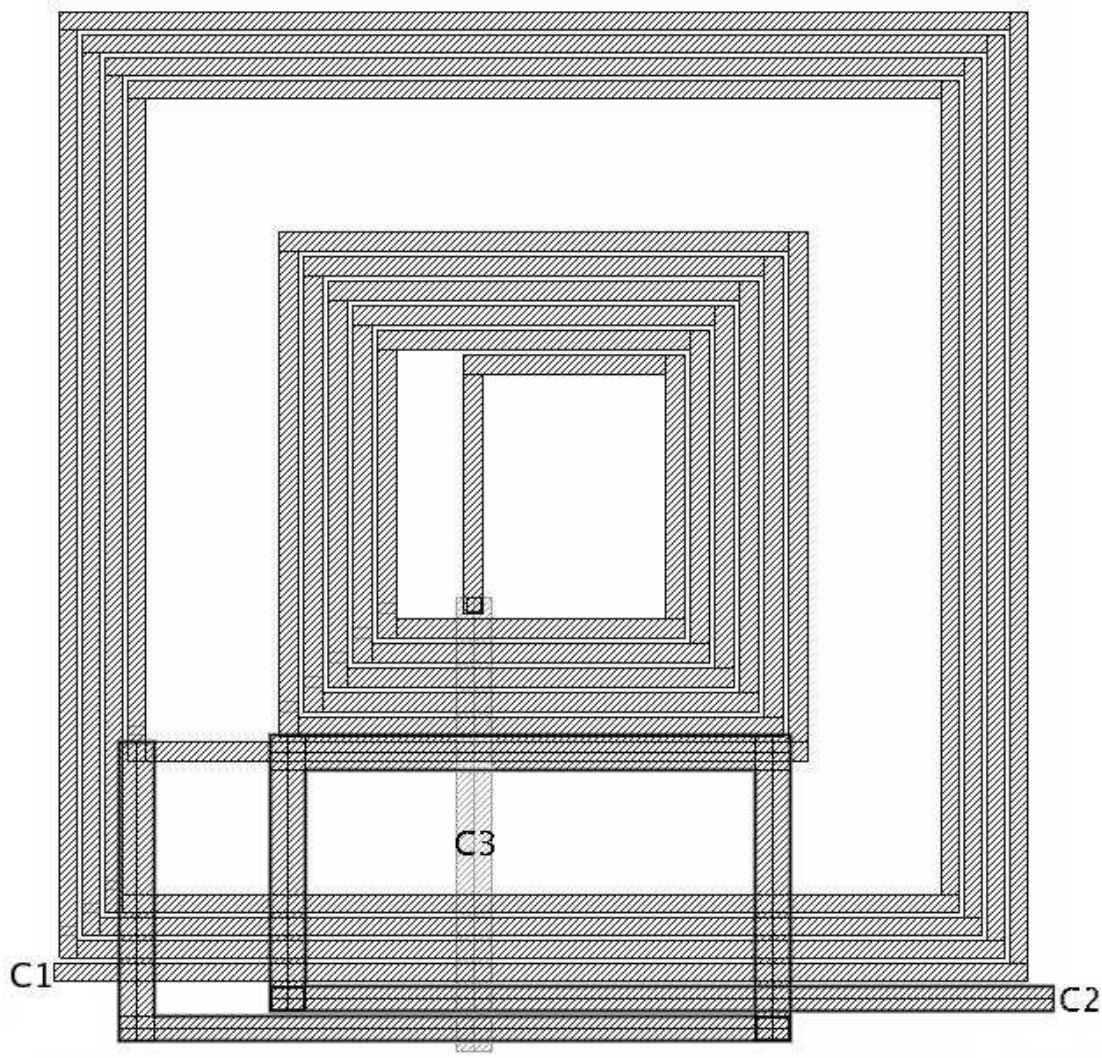


Figure 3.4: Layout of the full spiral in Virtuoso

The given structure was simulated in Fasthenry. Self and mutual inductance (along with their resistive impedance in brackets) are listed below

$L_a = 18.8\,\text{nH}$ $(17.83\,\Omega)$

$L_b = 12.1\,\text{nH}$ $(10.77\,\Omega)$

$L_c = 1.35\,\text{nH}$ $(3.77\,\Omega)$

$M_{ab} = 3.04\,\text{nH}$

$M_{bc} = -0.1\,\text{nH}$

$M_{ac} = 1.33\,\text{nH}$

These values when used in used in Eq.3.7 give,

$L_1 = 23.27\,\text{nH}\ (17.83\,\Omega)$

$L_2 = 13.91\,\text{nH}\ (10.77\,\Omega)$

$L_3 = 0.27\,\text{nH}\ (3.77\,\Omega)$

3.3 Area comparison

Using a single coil instead of two separate ones for realising two inductors helps in reducing overall chip area becasue

- positive mutual coupling brings individual inductances to be realised down by M_{12}
- two separate coils need to be placed far apart to preclude any coupling between two inductors
- quality factor constraints are very relaxed leading to thinner tracks and smaller spiral

The single coil used in this design is a square spiral of size $550 \times 550\,\mu m^2$. Whereas two uncoupled inductors of values 23.05 nH and 14.15 nH require spirals of sides approximately $450\,\mu$m and $350\,\mu$m in length. To fairly compare total area occupied, L_1 and L_2 should have same coupling coefficient in both techniques. The coupling factor of the coil designed in previous section from the value of final L_3 is,

$$k_{12} = \frac{L_3}{\sqrt{L_1 L_2}} = 0.015 \tag{3.10}$$

Separate coils of sizes mentioned before should be at a distance of atleast $75\,\mu$m to achieve such a low mutual coupling. Fig. 3.5 compares the area usage by single ended coils, in the two cases. A clearance of $25\,\mu$m is provided around each spiral. As can be seen, the separate spiral method employs 36% more area than the implemented spiral.

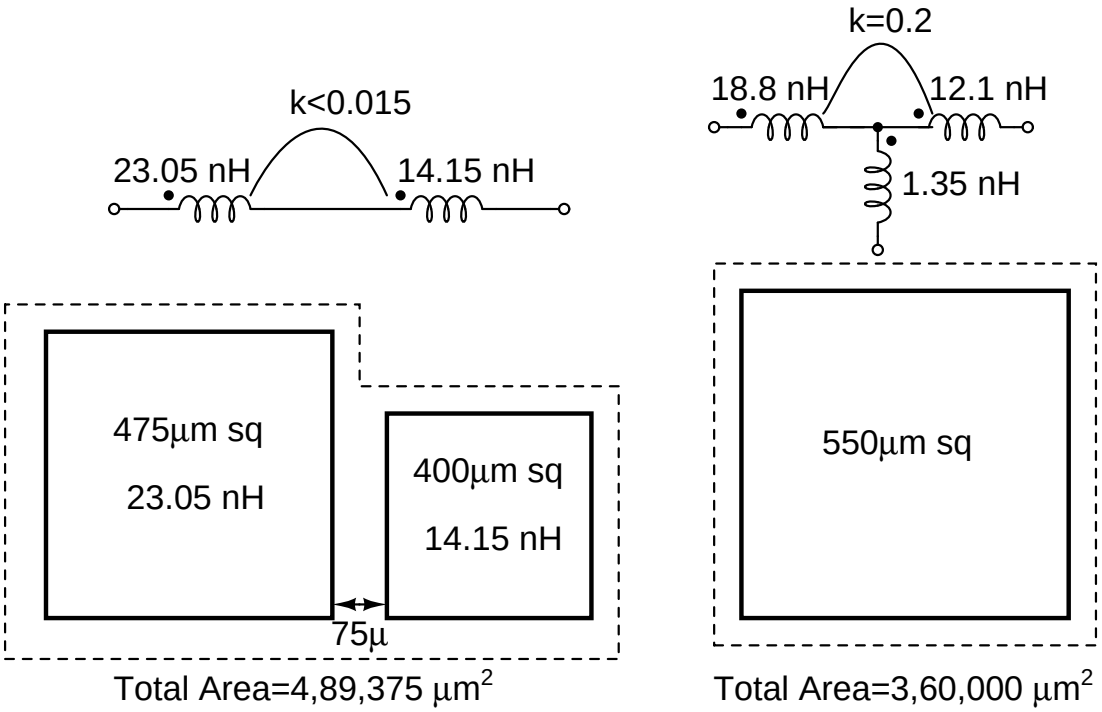


Figure 3.5: Comparison of areas of single ended separate coils and a single tapped coil

3.4 Modeling of spiral in spectre

A preliminary spiral is designed using EM Simulators like Asitic [2] and Fasthenry [3]. These simulators work fine for a planar coil and take less time which is useful during optimization and for deciding spiral parameters. For a thorough analysis of the final coil which involves effects of ground contact, sidewall and substrate capacitances, coupling between tracks in different metal layers and calculation of s-parameters over a large frequency range, the said design is implemented in AWR Microwave Office and simulated using EMSight 2.5D electromagnetic simulator. Following subsections discuss these two methods.

To assess the changes in resistance and inductance values due to skin depth, each metal track is divided into segments whose dimensions are less than the skin depth of the metal in the desired frequency range. Skin depth is calculated using Eq. 3.11 and comes out to be around 1.5 μm at 10 GHz. As seen from simulations, skin effect starts playing a role only after 3 GHz, but still grid size in Microwave

Office and variables *nhinc* and *nwinc* in Fasthenry should be decided such that segment sizes are less than the skin depth.

$$\delta_s = \sqrt{\frac{2\rho}{\omega\mu_0\mu_r}} \tag{3.11}$$

where, ρ is resistivity of conductor,

ω is frequency of operation in rad/sec

and μ_r is relative magnetic permeability of the conductor.

3.4.1 Distributed model

The lumped model shown in Fig. 2.3 is accurate only for low frequencies. The spiral, being a transmission line, should ideally be represented by an infinite number of such pi models in series. Instead, we can keep increasing the number of segments till there are no more significant changes in its frequency response. Capacitance between turns and to ground are calculated using extracted layout of spiral in UMC 180 nm technology. For this, the coil needs to be broken down into smaller segments, each of which is treated as a lumped element, to allow better modeling of sidewall capacitances. The minimum number of such segments required is equal to the spiral's number of turns. Metal resistances (R_{M1} and R_{M2} in Fig. 3.6) are used to identify these segments as separate nets during extraction without affecting the spiral.

In Fig. 3.6 L_{12}, L_{23} and L_{34} are a sum of both segment's self and mutual inductances. C_{12} and C_{23} are side wall capacitances and C_{S1}, C_{S2} and C_{S3} are capacitance to the ground plane as extracted from UMC180 capacitance tables. Instead of having a single pi model for the whole coil, a separate distributed model is created for the three inductors while using them in the schematic.

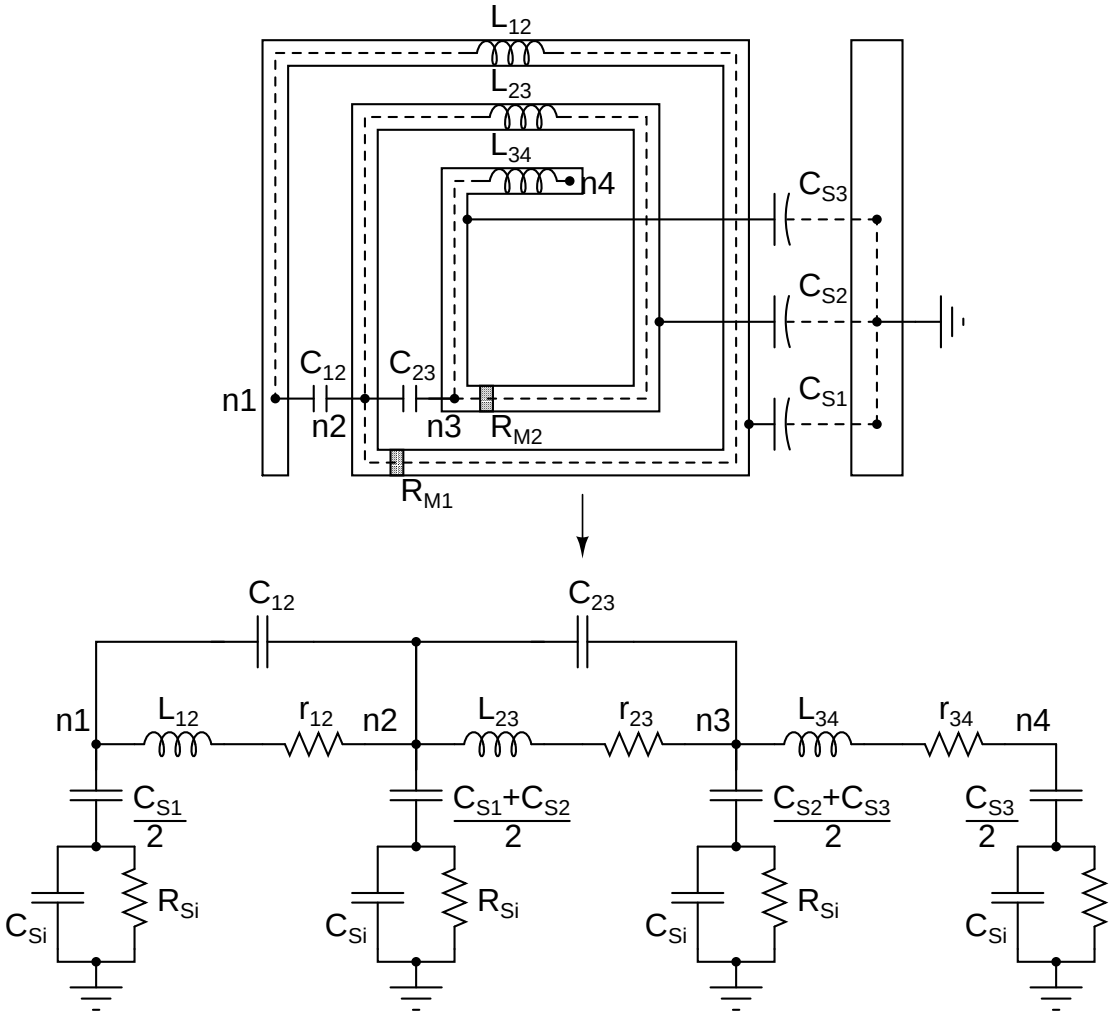


Figure 3.6: Distributed pi-model of a sample inductor

3.4.2 3-port system

The full spiral is essentially a 3 port system whose s-parameters as calculated by Microwave Office over the frequency range of interest can be used for ac-simulations in cadence. To make sure that an IC's environment is replicated, the enclosure in Microwave Office should include each metal and oxide layer along with the bulk substrate defined using UMC 180 nm technology's parameters. In RF CMOS processes such as we need for this design, the bulk substrate resistivity is large enough to ignore the effect of parasitics between metal tracks and ground plane at the bottom of substrate. But, since we also have metal to substrate contacts very close to the coil the capacitance to bulk, C_S, cannot be neglected

and needs to be modeled. This can be done by simply laying out the spiral close (similar to its distance from bulk contacts in chip layout) to the sides of enclosure (which are also grounded in EM simulators to provide for boundary conditions while solving for the fields). Since these ground contacts can be layed out such that they are close to only one side of the spiral, their role in increasing the effective capacitance to ground is limited.

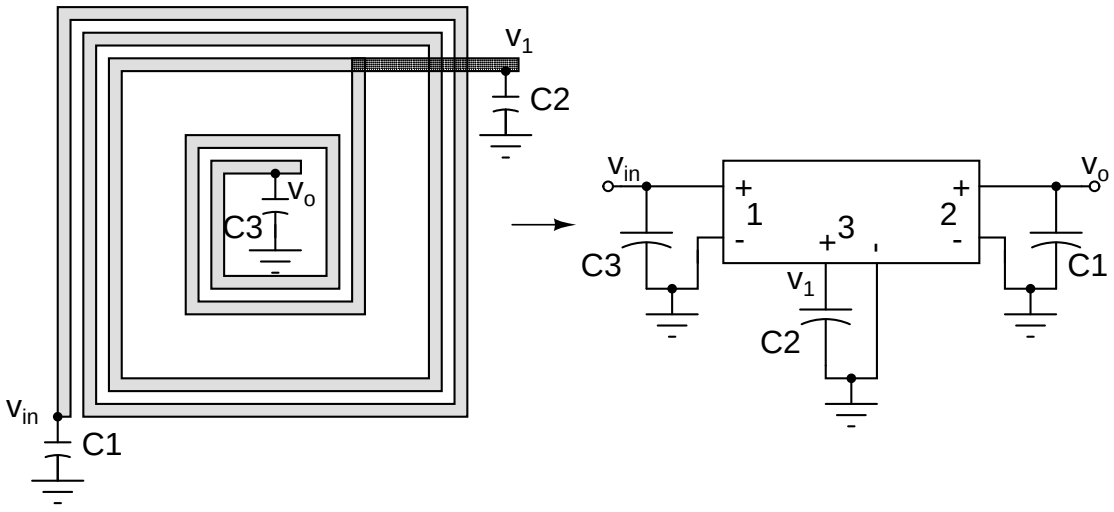


Figure 3.7: Inductor as a 3-port system

For simulation purposes, the 3 port s-parameters are used for calculating the magnitude response of the filter whereas all transient simulations (distortion analysis, step response, etc) is done using the distributed model.

CHAPTER 4

Input Gm-cell

As discussed in Chapter 2, at the filter's input a vccs is used to increase ladder's input impedance. Since it is the only non linear element in the whole filter, the Gm-cell's non-linearity and output noise decide the filter's dynamic range.

4.1 Design

To increase the Gm-cell's signal swing, source degenerated architecture is used. For a MOS transistor M_s (Fig. 4.1) whose source is connected to ground through a resistance R_s, drain incremental current can be written as

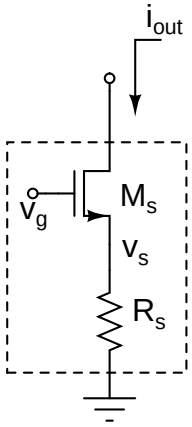


Figure 4.1: A source degenerated nMOS

$$i_{out} = (v_g - v_s)g_m = (v_g - i_{out}R)g_m \tag{4.1}$$

$$i_{out} = v_g \frac{g_m}{1 + g_m R} \tag{4.2}$$

Hence, the effective transconductance of this nMOS is $g'_m = g_m/1 + g_m R$. For $g_m R \gg 1$, g'_m becomes $1/R$. Since this resistance is independent of transistor's operating point, the transconductance stays completely linear as long as this condition is satisfied. This is done by drawing more current and/or using larger transistors. A differential Gm-cell using this architecture is shown in Fig. 4.2.

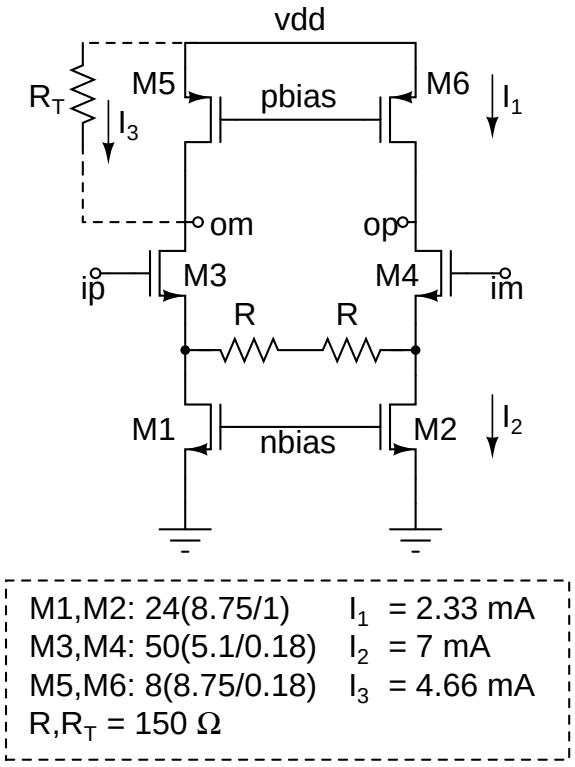


Figure 4.2: Schematic of the input Gm-cell

Each such cell has a transconductance of 6.66 mS and drives a part of the ladder's termination resistance of value 150 Ω. Realizing such a high transconductance, especially with 1.8 V supply and degenerated input pair, is tricky in our case because

- $g_m R \gg 1$ constraint requires larger transistor sizes
- large drain capacitances of input pair decreases bandwidth over which Gm-cell can be used
- low overdrive of input transistors decreases linearity

- finite impedance offered by tail current sources reduces effective gain of Gm-cell
- noise of tail current sources simply adds to the ouput unlike a simple differential pair

To get a large overdrive and hence better linearity, the input common mode is chosen to be $V_{ocm} = 1.1\,\mathrm{V}$. The output common mode is decided by quiescent current flowing through termination resistors. Since we want the output and input common modes to be same, this current has to be limited to,

$$I_3 = \frac{V_{supply} - V_{ocm}}{R_T} = \frac{1.8 - 1.1}{150} = 4.66\,mA \tag{4.3}$$

To increase DC current that can flow through M_3 and M_4, some current I_1 is diverted using transistors M_5 and M_6 whose output impedances should be high enough not to affect R_T's effective value. Combined parasitic drain capacitances at outputs of all five Gm-cells can be absorbed into C_3 which is also connected between output and ground. Thus, sizes of these pMOS and input nMOS transistors are limited. Hence, I_1 is limited by drain capacitance of M_5 and M_6 and is fixed to be half of I_3. Thus total current through tail nMOS sources is $I_2 = I_1 + I_3 = 7\,\mathrm{mA}$.

The bias distribution section in Chapter 6 discusses how the transconductance of this cell can be tuned according to the required termination resistance for a particular bandwidth mode of the filter.

4.2 Simulation results

IM3 simulations are done for a Gm-cell, with extracted parasitic capacitances, for varying input amplitude (for input tones of 880 MHz and 890 MHz) and for varying input frequency (at 0.5 V V_{ippd}) and the results are shown in Fig. 4.3. In these plots the y-axis denotes the ratio of powers of input and third order intermodulation tones. For example, if the input tones are at 490 MHz and 500 MHz the graph's

datum at 495 MHz will be given by

$$\mathrm{IM3}_{495} = 10 \times \log \frac{\text{power of tone at } 480\,\mathrm{MHz} + \text{power of tone at } 510\,\mathrm{MHz}}{\text{power of tone at } 490\,\mathrm{MHz} + \text{power of tone at } 500\,\mathrm{MHz}} \tag{4.4}$$

As can be seen from Fig. 4.3 the input amplitude at which intermodulation tones' power is 40 dB below that of input tones is 1.68 V V_{ippd}.

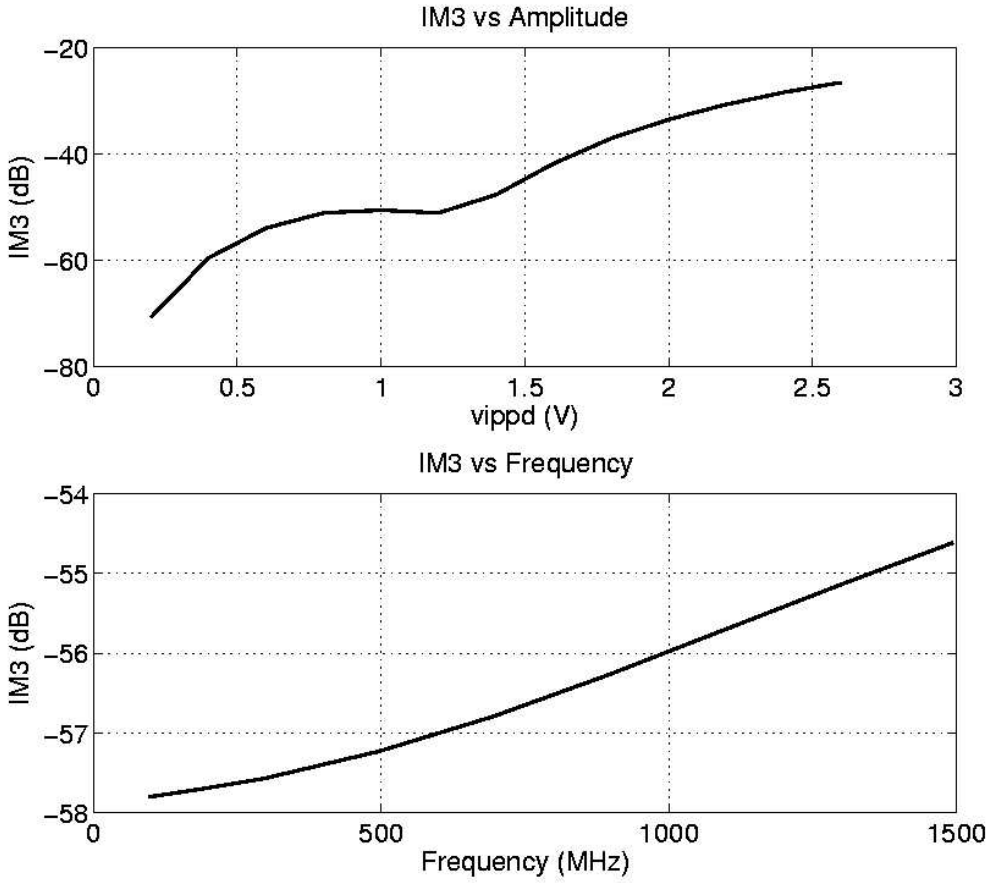


Figure 4.3: Variation of IM3 with input amplitude and frequency

CHAPTER 5

MOS capacitors for the ladder filter

Metal-metal capacitors are very linear but their specific capacitance is pretty low ($1\,\mathrm{fF}/\mu m^2$). The total capacitance to be used for this low pass filter sums up to about 42 pF. This means $42,000\,\mu m^2$ of chip area is used up in implementing the ladder's capacitance itself. Now, the inductors no longer dominate area usage. Also, since both these components use the top most metal layer in UMC 180 nm technology, it would mean their areas just add up. A solution to this would be to use MOS transistors in their accumulation region instead. They have limited linearity and their capacitance is dependent on biasing voltage, but since chip area required to implement the filter reduces to nearly half, it is definitely worth exploring. Unlike metal-metal capacitors which occupy the top most thick metal layer, these capacitors can potentially be laid out beneath the inductor spiral further reducing chip area.

5.1 Region of operation

We will go through a brief overview of the C-V characterstics of a MOS capacitor [4] before deciding upon their operating region. In a MOS transistor accumulation occurs when its gate is pulled down below the bulk by more than the flat band voltage, i.e. when $V_{GB} < V_{FB}$. As we can see in Fig. 5.1, voltage V_{GB} drops linearly across gate oxide and the electric field is towards negative x direction (from bottom of oxide to gate poly). This causes holes to accumulate at top of the substrate and electrons collect at bottom of the gate, which is exactly what we would expect from a parallel plate capacitor. In a parallel plate capacitor $C = \epsilon/d$

(capacitance per unit area), thus in this case where t_{ox} is the thickness of oxide

$$C_{Moscap} = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{5.1}$$

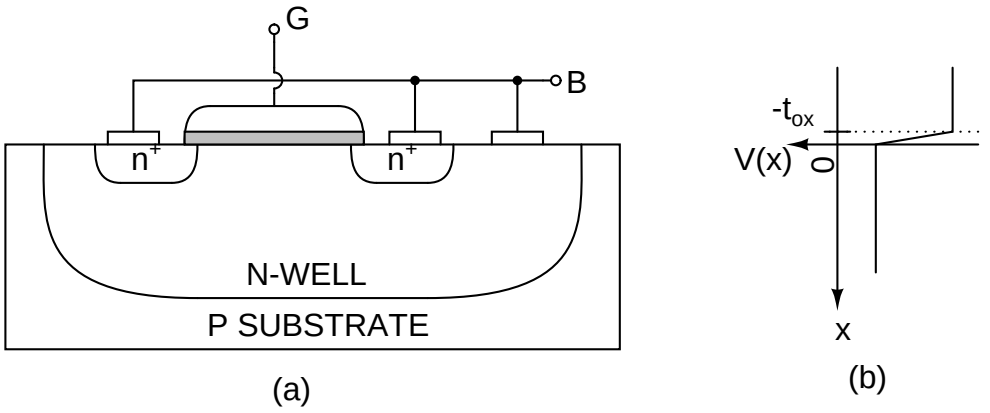


Figure 5.1: (a) Cross section of a MOS capacitor (b) Voltage along a vertical cross-section with respect to Bulk (V_x)

When the gate is biased between the flat band voltage and threshold voltage ($V_{FB} < V_{GB} < V_{TH}$), the transistor operates in depletion mode. In this region the potential drop across oxide is still linear (C_{ox} is present), but the depletion region also offers some capacitance in series with C_{ox}. The depletion width and hence depletion capacitance (C_d) depends on gate voltage applied. The total capacitance $C_{Moscap} = (C_{ox}C_d)/(C_{ox} + C_d)$ decreases with V_{GB}, as depletion width is directly proportional to applied bias.

Inversion occurs for $V_{GB} > V_{TH}$, when the silicon near the surface of the device (i.e. around x = 0) becomes inverted, meaning it actually starts acting like n-type silicon, despite being doped p-type (for an nMOS). This means is that electrons form at the surface, creating an inversion layer of charge. In inversion the depletion region stops growing and stays at its maximum, while charge is free to grow very large as V_{FB} is increased. Which means there is no depletion capacitance, but charge in n^+ gate and inversion layer increases, so that $C_{Moscap} = C_{ox}$. But since electrons in the p-type substrate have to be generated slowly by thermal excitation, the inversion layer cannot track high frequency (more than tens of Hertz) changes

in bias and we are left with depletion capacitance C_d.

Fig. 5.2 shows the variation in capacitance across a MOS transistor with the applied voltage V_{GB}. Since we intend to use these MOS capacitors in place of metal-metal capacitors, the region of operation should be deep accumulation or strong inversion because this region provides the maximum specific capacitance and change of charge with V_{GB} is most linear.

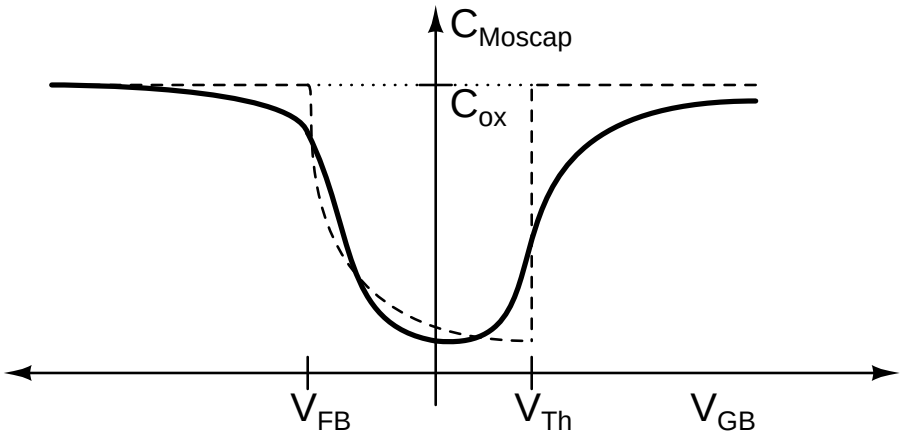


Figure 5.2: CV characterstics of a typical MOS capacitor

Use of nMOS transistors in an N-well as Mos capacitors in accumulation has been discussed in [5] and [6]. Apart from the fact that there is no extra carrier source necessary in accumulation mode we also have both bulk and gate terminals at our disposal. Also, the reduction in flat band voltage provided by this arrangement means that the transistor will be operating in deep accumulation region. Since, the bulk of N-Well is to be at a lower potential than the gate for the nMOS to be in accumulataion, the gate can connected to the inductor spiral whereas the bulk contact goes, directly or through a switch, to ground. For simulation purposes the 180 nm UMC technology's nMOS transistor models are used in accumulation, i.e. their gates are grounded and bulk, drain and source contacts shorted together and connected to the the common mode voltage. Another way to model MOS capacitors would be to use transistors in inversion, as they donot include the forward biased p-n junctions like the accumulation nMOS in P-well capacitors. But, these models give unexpected results (-80 dB IM3 distortion

throughout signal swing) during simulations because of which the accumualtion model only is for all the distortion analyses in this design.

5.2 Resistance offered by MOS capacitor

A MOS transistor in accumulation offers some resistance in series with the oxide capacitance (C_{ox} in Fig. 5.3), which originates from the channel resistance and high resistivity of gate polysilicon contact. Since contacts to the gate polysilicon can be made only at the lateral edge of each finger, the resistance offered by polysilicon comes into effect. As we are interested in an approximate comparison between impedance of the capacitance (at the frequency of interest) and MOS capacitor's series resistance, it is assumed that the oxide capacitance which in reality is distributed throughout the width of gate, is lumped and appears at the center of the channel (as depicted in Fig. 5.3(c)). This means that from the gate contact to the center the gate polysilicone offers a resistance R_p which is given by,

$$R_p = \frac{1}{2} \times \frac{W}{L} \times R_{sh,gate-polysilicon} \times \frac{1}{\text{number of fingers}} \tag{5.2}$$

Also, as seen in Fig. 5.3(b), the channel resitance also comes in series with the gate oxide capacitance and can be estimated as,

$$R_{channel} = \frac{1}{4 \times g_{ds}} \times \frac{1}{\text{number of fingers}} \tag{5.3}$$

As an example we take one of the MOS accumulation capacitors of value 3.4 pF to be used in this filter. This capacitor is implemented using a MOS transistor which has 24 fingers each of width and length 32 μm and 0.5 μm respectively. The channel resistance is estimated from simulation where this same mosfet is operating in inversion region (although a channel in inversion offers lower conductance than one in accumulation). The sheet resistance of gate polysilicone is 8 ohm/sq. Using this data, impedance of the three elements at 0.5 GHz (bandwidth at which this

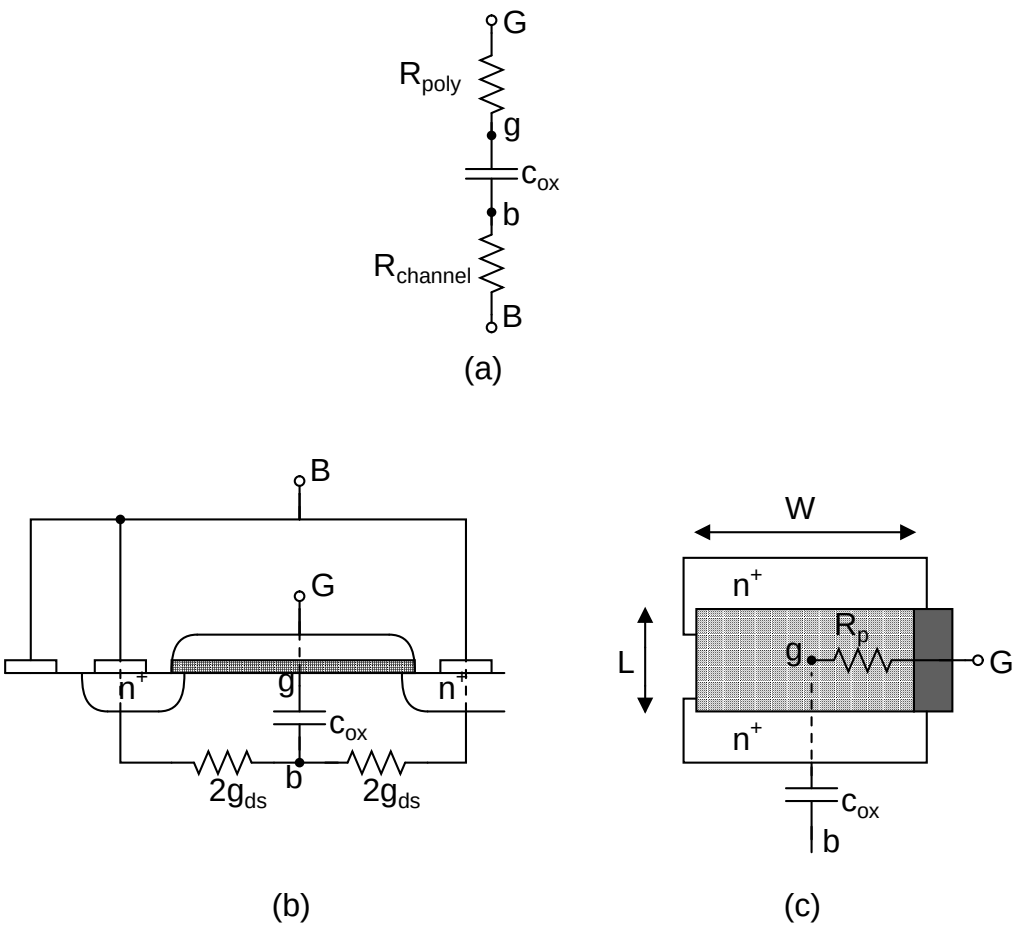


Figure 5.3: (a)Representation of a MOS capacitor with series losses (b)Accumulation channel's resistance (c)Gate polysilicone resistance

capacitor is being used) in Fig. 5.3(a) are calculated.

$R_{poly} = 11\,\Omega$

$R_{C_{ox}} = 93.66\,\Omega$

$R_{channel} = 0.85\,\Omega$

Impedance from the series resistances is just about comparable to the capcitance at the given frequency and the gate contact dominates the losses which is because of its high sheet resistivity. Its effect on capacitor's functioning will be higher in cases where wider channels are used. But, by using contacts from this gate polysilicon layer to one of the metal layers throughout the width of the channel, and laying out the metal path in parallel with gate, can help us in reduc-

ing R_{poly} and make series resistance negligible with respect to the accumulation capacitance.

The same capacitor when realized using longer channels has higher $R_{channel}$ resistance although the gate polysilicon impedance will be less now. For a MOS transistor with four fingers each $4\,\mu$m long and $25\,\mu$m wide, these values are re-calculated,

$R_{poly} = 4\,\Omega$

$R_{C_{ox}} = 93.66\,\Omega$

$R_{channel} = 12.5\,\Omega$

As we can see, the length of fingers being used in transistors can be varied to minimise the net series resistive losses of the MOS capacitor. For this design transitors with channel length of $0.5\,\mu$m are used for all capacitors.

5.3 Effect on filter's linearity

Using MOS capacitors instead of metal-metal capacitors saves chip area, but it eats into filter's dynamic range. Even in accumulation region these capacitors have limited linearity as their capacitance drops down with increasing V_{GB}. Also, since they have to be biased at common mode voltage (V_{cm}) and not the full 1.8 V supply, voltage swings suffer even more.

But, these capacitors are not the only contributors to distortion. As discussed in Chapter 4, the input Gm-cell itself is non-linear and if its non-linearity is much more than that of the MOS capacitors, over the desired signal swing, then only its distortion will determine the final filter's dynamic range.

IM3 simulations with input peak to peak differential amplitude (V_{ippd}) of 500 mV are carried out for a Gm-cell and a lowpass passive ladder with MOS capacitors (1 GHz bandwidth) individually across different frequencies to look for the worst distortion frequency. The plots shown in Fig.5.4 shows the results of simulations done with two tones spaced by 10 MHz and their mean frequency is

shown on the x axis.

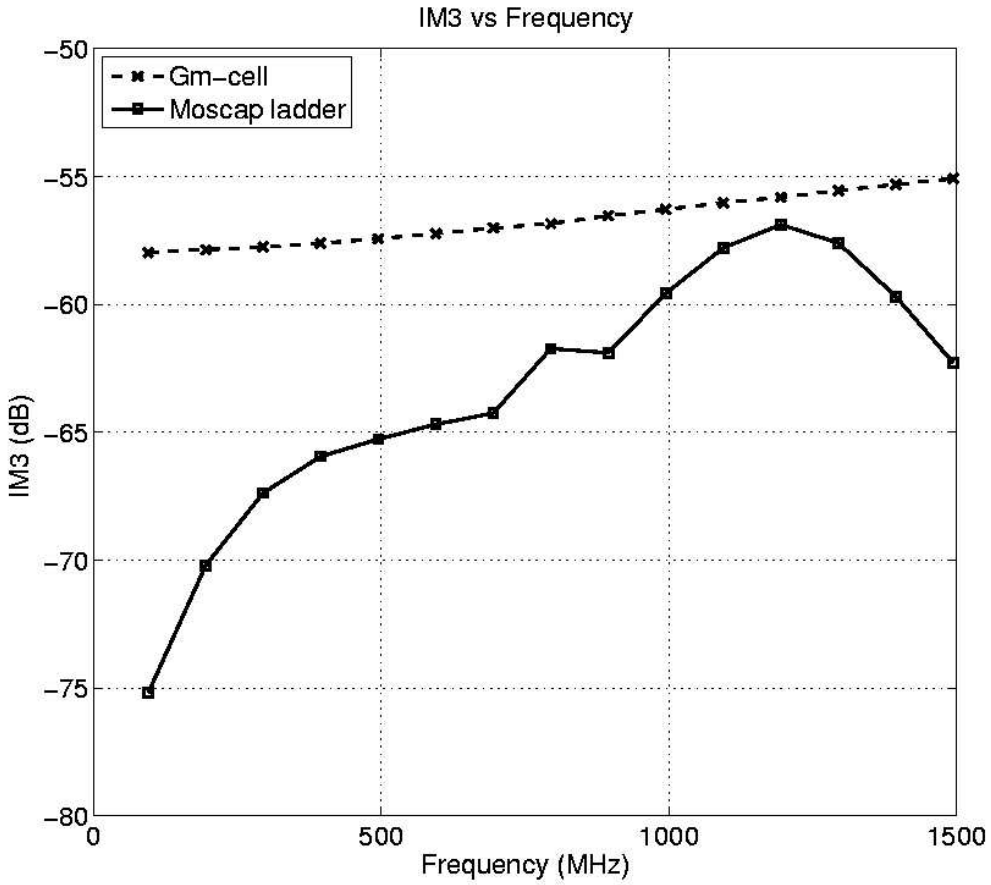


Figure 5.4: IM3 vs Frequency comparison

As can be seen from this plot, distortion keeps increasing with frequency in both cases. Thus, input frequencies for worst case distortion simulations are chosen to be somewhere close to band edge inside the pass band. Fig.5.5 shows 3^{rd} order intermodulation distortion with varying input amplitude, at input frequencies of 880 MHz and 890 MHz, for an isolated Gm-cell and a passive ladder using MOS capacitors. The -40dB IM3 input amplitude for a Gm-cell is 1.68 V V_{ippd} whereas that for lowpass ladder is 2.5 V V_{ippd}. Except for a range of input amplitudes, where harmonics cancellation is more pronounced due to source degeneration, distortion from Gm-cell clearly dominates the overall non linearity of filter.

From these IM3 simulations we have made it clear that by using MOS capaci-

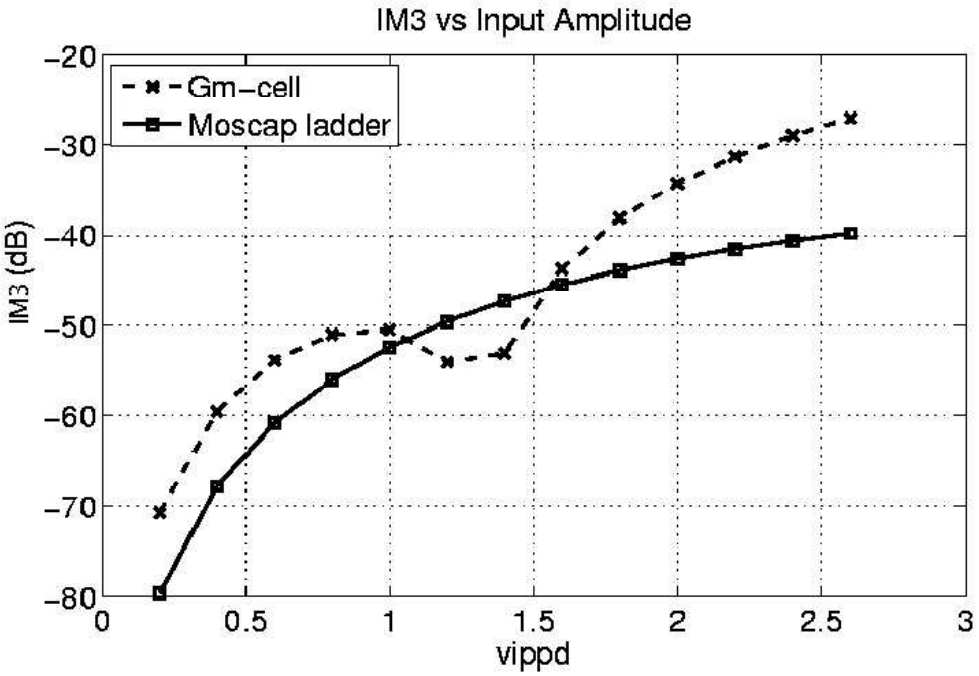


Figure 5.5: Distortion comparison between Gm-cell and Moscaps

tors we would be saving up on almost half of the chip area that would have been required for a filter with metal-metal capacitors, without decreasing filter's overall dynamic range, which is still decided by noise and non-linearities of Gm-cell.

CHAPTER 6

Fifth order tunable passive Butterworth ladder filter using MOS capacitors

A fifth order lowpass Butterworth ladder filter is designed in a 0.18 μm CMOS process with a supply voltage of 1.8 V. Its bandwidth is tunable in four steps between 400 MHz and 1 GHz. The filter is fully differential with a common mode voltage of 1.1 V. It uses a single coil for realizing two inductors as discussed in Chapter 3. Instead of metal-metal capacitors MOS capacitors in accumulation are used as discussed in Chapter 5. Both these techniques help in reducing chip area which otherwise would have been too large, for a passive filter at this bandwidth, to be of any practical use. This chapter focuses on design details of all blocks which make up the filter.

Fig. 6.1 shows the block diagram of the filter. The two test buffers are used for accurate characterisation of the filter by deembedding any effects from the chip and test board. Digital logic block is used for decoding the control bits used for tuning the filter's bandwidth. The chip uses a 10 μA reference current source to provide bias currents and voltages for the Gm-cell and test buffers using the bias distribution block. Finally the multiple tapped spiral and MOS capacitors are brought together to form the LC ladder which is the core of this filter. For better performance across process corners the termination resistance too is made tunable which in turn renders it not completely linear.

6.1 Bias generation and distribution

Effective transconductance of the input vccs can be changed by connecting the required number of Gm-cells in parallel. This is achieved by connecting 5 identical

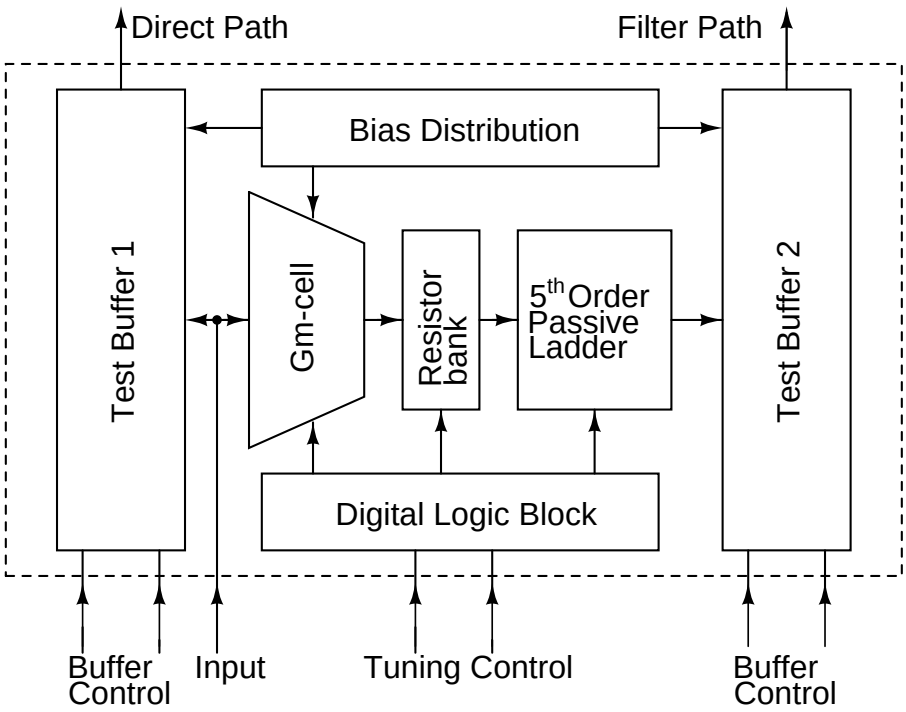


Figure 6.1: Block diagram of the filter with test buffers

cells in parallel and selectively turning them on using two control bits $b<0:1>$. The schematic in Fig. 6.2 shows this implementation. Since the outputs of all cells are always shorted, both tail nMOS and load pMOS need to be switched off, by connecting their biases to ground and V_{dd} respectively using switches M_1 to M_5, to maintain output common mode. Fig. 6.2 shows how gate bias of pMOS, M_5 and M_6, and tail current sources, $M1$ and $M2$, can be shorted to supply and ground respectively to switch ON a particular Gm-cell.

Gate bias (*pbias* and *nbias*) voltages are generated using a reference current source of $10\,\mu$A using the bias generation circuit of Fig. 6.3. The schematic also includes current distribution for the test buffers each of which require a bias current of $500\,\mu$A. M_{11}'s size is one third of M_{10} because as discussed in Chapter 4 the pMOS loads carry only a third of the total current in Gm-cell's each branch.

6.2 Termination resistor bank

The termination resistance is made programmable using 3 bits ($br<0:2>$ decoded to $res<0:7>$) to cover for variation over process corners. Fig. 6.4 shows its implementation. Ideally a switch should not add any series resistance. But this would require the pMOS switches to be very large, since current ranging from 2.66 mA to 5.6 mA flows through each conducting branch. A large switch adds to parasitic capacitance to ground in series with R_T which effects the magnitude response of filter. Thus, instead of making switches' ON resistance small, its made approximately one third of the total resistance offered by that branch. Although this means that the termination resistance too now is non-linear. Its effect on the filter's dynamic range can be seen from simulations and is discussed in the next chapter.

Digital bits for controlling input transconductance and R_T bank are given in Table.6.1

Table 6.1: Digital bits for tuning the filter

Freq (MHz)	R_T (Ω)	G_m (mS)	$b<0:1>$	$br<0:2>$
400	30	33.33	00	001
500	37.5	26.66	01	011
666.66	50	20	10	101
1000	75	13.33	11	110

6.3 Digital logic

The only digital blocks in the filter is a 3 bits binary to thermometer converter and a two bit decoder. While tuning the termination resistor bank by one step, all the previously conducting branches still need to be ON and only the last resistor needs to be switched ON or OFF, which requires a thermometer code. Since the switches in resistor bank are pMOSes the control bits ($Res<0:7>$) are active low. Fig. 6.5 shows the schematic by which it was implemented.

6.4 5^{th} order LC ladder

The capacitor banks are tuned using the same controls bits as the Gm-cell $b < 0:1 >$. Differential schematic of these blocks are shown in Fig. 6.6 and Fig. 6.7 along with the element values. As can be seen the shunt conductances are also broken up into four so that they can be tuned along with the capacitors. All MOS capacitors' bulks are grounded and their gates are connected to the signal path, i.e the inductor spiral. Capacitor C_3 is done away with in 1 GHz bandwidth mode since the summed up parasitic drain capacitance of the five Gm-cells is sufficient. Also, by default the ladder realizes 1 GHz lowpass filter since no switches are used this mode to avoid any extra resistance and capacitance offered by the switches in series with the capacitances and shunt conductances.

But these switches cannot be avoided completely, as they are essential for realizing other three bandwidths, which leads to other complications. Taking for example the second (666.66 MHz bandwidth) branch in Fig. 6.6, when $b1$ is 1.8 V, ON resistance of M_{1a} to ground falls in series with capacitance C_{b1} which leads to reduced bandwidth and a magnitude response which droops in the pass band itself. Also, if the sizes are increased in an attempt to lower this series resistance, their drain parasitic capacitance to ground makes sure that its branch never really fully switches OFF as there is always a capacitive path to ground (although much reduced because these two capacitances are in series). Thus, switch sizes are made larger for smaller bandwidths, i.e. when the capacitances are larger so as to have least effect on filter's transfer function.

From Fig. 6.6 and Fig. 6.7 its clear that the two nMOS switches in series can be replaced by just one, either of whose terminals are biased at ground (for capacitor branches) using large resistors. The swithces in series with shunt conductances need not be biased at all. This clearly appears to be a better design as it also cuts down the resistance offered by these switches to half. But since the combined area of swithces and the large resistances remains almost same as the two switches prototype, we opt for the design with inherent symmetry in its layout. Also,

switches' resistance is negligible when compared to shunt resistances.

Due to the combined effect of extracted capacitances and switches' parasitic effects the filter's bandwidth in all four modes drops down by around 5%. In an attempt to retain the nominal bandwidths, the transistors used as capacitors have to be made smaller by a fraction of their calculated value. Since, the inductances have not been scaled down, final filter characterstics deviate further from ideal Butterworth.

Inductor spiral for L_1 and L_2 has already been discussed in Chapter.3, which completes the design of 5^{th} order LC Ladder.

6.5 Test buffer

The filter discussed above will be used as part of a larger design and doesnot act as a stand alone device. Since the filter has not been designed to drive huge capacitive load of the package and the test board, test buffers are used to prevent any loading of the filter.

In order to accurately characterize the filter while testing, gain of the buffer is negated using switch control. Details of this testing technique can be found in [7]. This can be achieved by negating the gain of the buffer using switch control. The buffer is essentially two simple transconductances implemented differentially. The outputs of these two are shorted but in opposite sense. If only one of these is switched ON at a time, the output's sign depends on which differential pair is working.

Design of the buffer should be such that distortion generated by it is much less than that of the filter itself. Hence, the input nMOS pair should be as linear as possible which can be done by

- using 3.3 V supply
- reducing the swing limits as seen by its input pair

- increasing their overdrives

Circuit schematic of the test buffer is shown in Fig. 6.8. Transistors M_{11} and M_{12} form the positive and negative paths of the buffer respectively. M_9 and M_10 are cascode transistors used to enhance output impedance of the transconductor. Their drains are connected in the opposite sense to allow the gain to be either of ± 1. their gates are controlled using digital logic which is pulled to logic level 0 when both paths are off. Resistor R_d acts as a dampening resistor to avoid possible oscillations with the bond wires' inductance. M_s transistors are used to switch on/off the two paths and the whole buffer.

In order to prevent loading on the filter the input transistors are driven using common drain amplifier stages. The source follower stage is implemented using a pMOS input stage M_8 and an active load M_7. The signal is attenuated by a factor of 3/8 between the source follower and transconductance stage to reduce input swing to the the transconductances, thereby improving buffer linearity. Current for these buffers is distributed using the bias distribution block.

Although an attenuated input to the transconductance stages increases the buffer's swing limits it can pose problems while filter's output noise measurements. Thus, for noise measurements an extra transconductance stage is added whose inputs come directly without attenuation from the common drain amplifier. Also to increase gain further the tail current sources in this transconductance stage are done away with. This way the input transistors have a very high overdrive, which reduces the noise from the buffer. Even with these measures the noise levels of 400 MHz and 500 MHz filters fall below that of the filter. Noise at the buffer outputs is plotted in Fig. 6.9 for the filter and direct paths when the filter is tuned for 1 GHz and 0.66 GHz 3 dB bandwidths. Three bits ($bt < 0 : 2 >$) are used for switching between each transconductance.

Fig. 6.10 compares the distortion levels of the filter's least non linear mode (1 GHz) and that of the buffer.

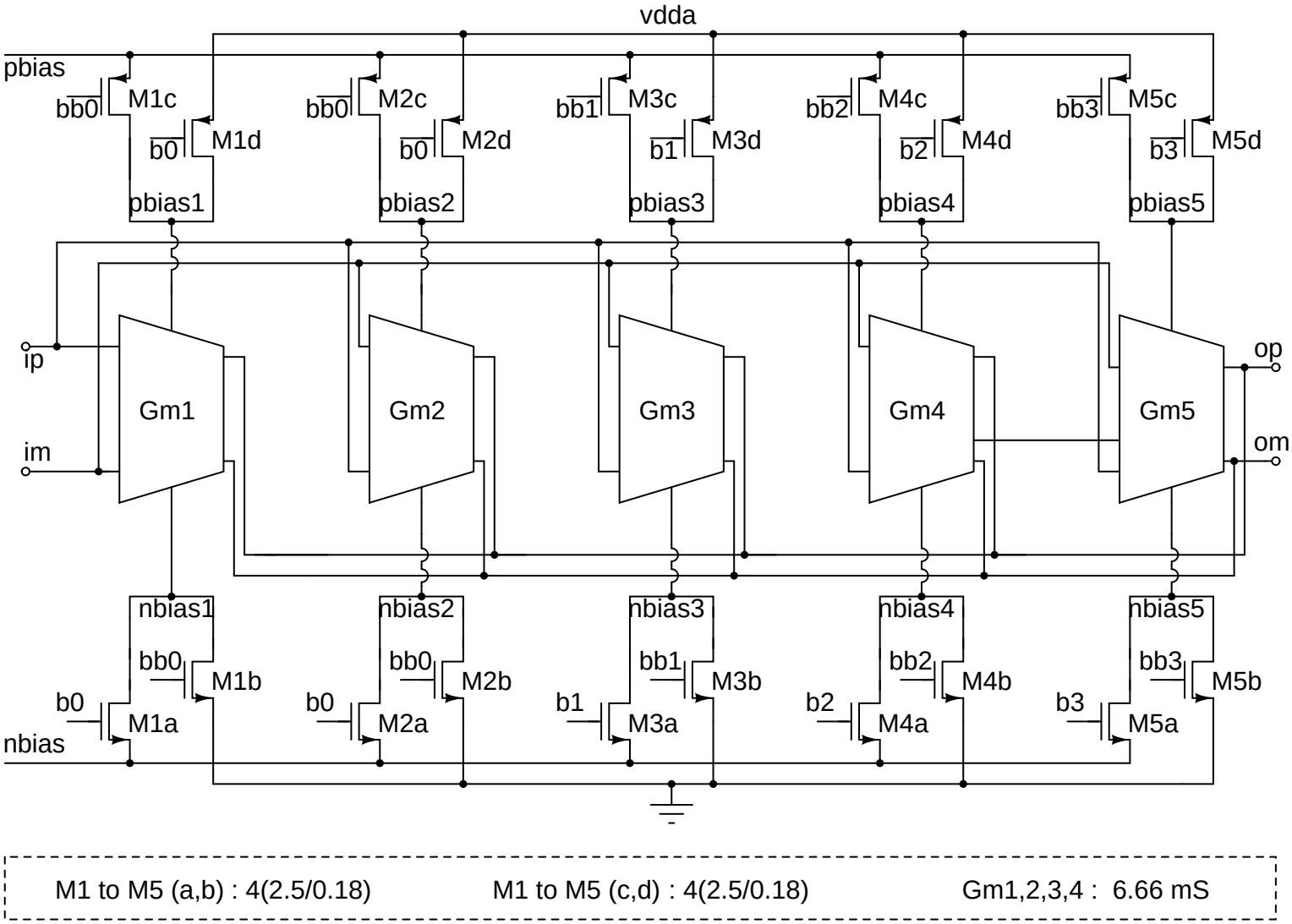


Figure 6.2: Schematic for bias distribution amongst Gm-cells

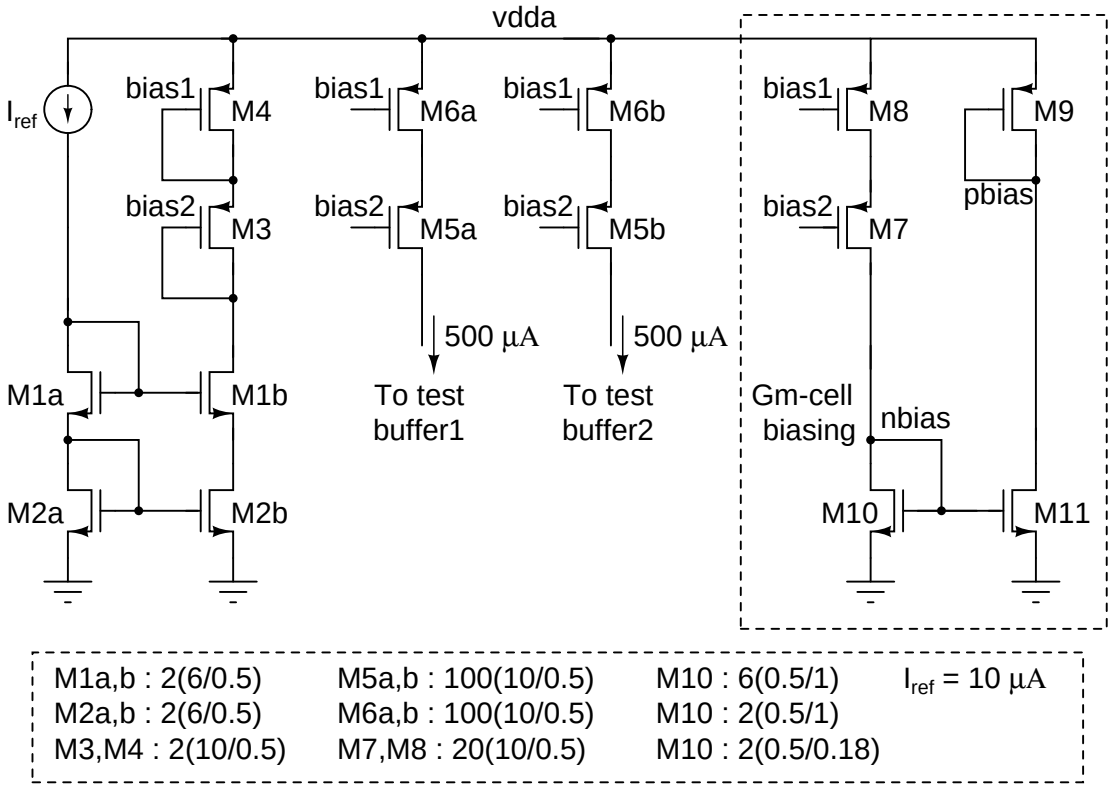


Figure 6.3: Voltage and current references generation for Gm-cell and test buffers

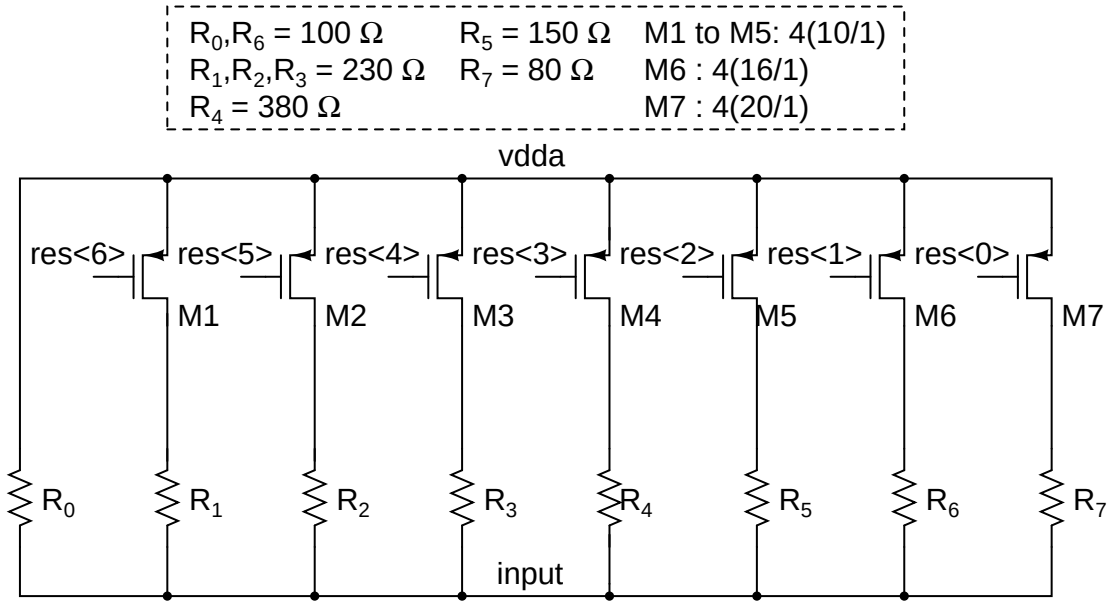


Figure 6.4: Single ended schematic of termination resistor bank

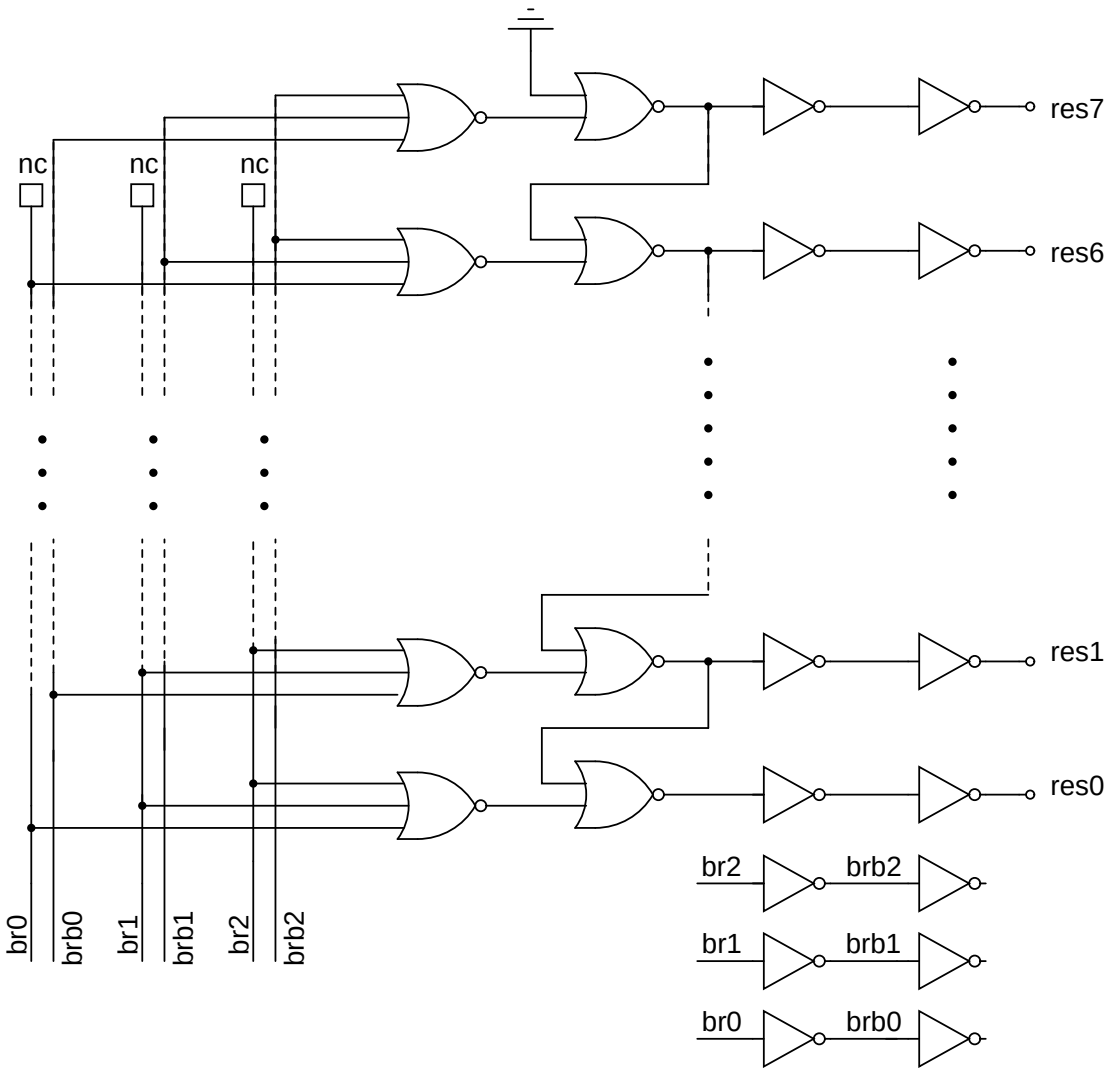
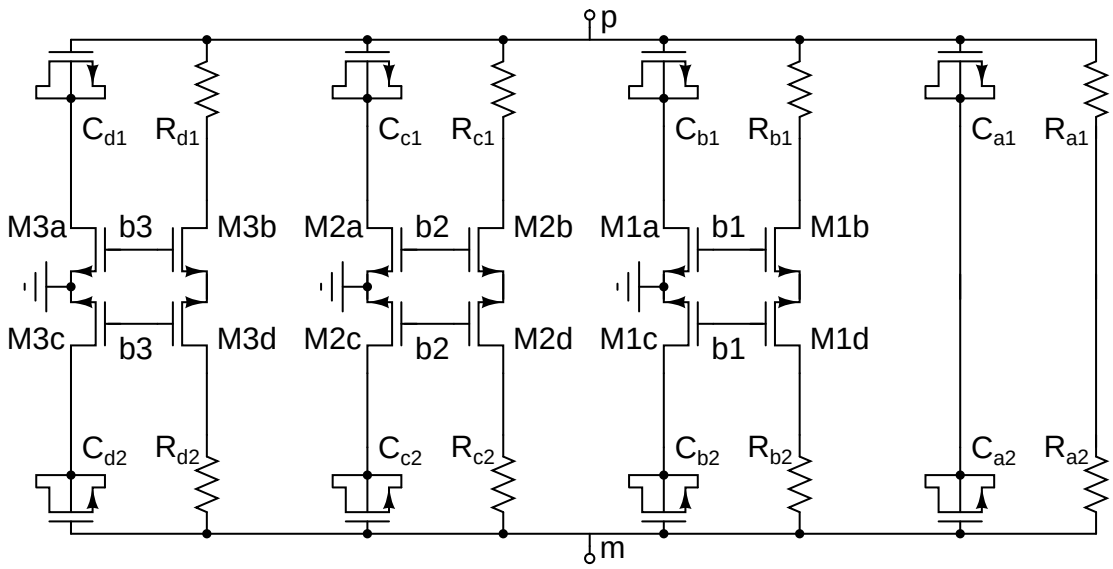


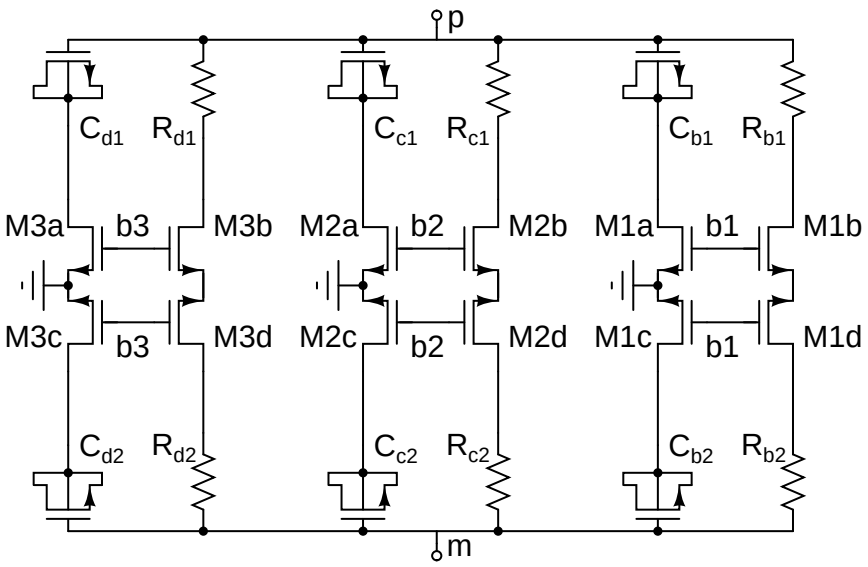
Figure 6.5: Schematic for binary to thermometer code generation



For C1 :	$R_{a1,2}$ = 928 Ω	$C_{a1,2}$ = 1.4 pF
M1a,b,c,d = 20(3/0.18)	$R_{b1,2}$ = 513 Ω	$C_{b1,2}$ = 2.52 pF
M2a,b,c,d = 28(3/0.18)	$R_{c1,2}$ = 345 Ω	$C_{c1,2}$ = 3.40 pF
M3a,b,c,d = 32(3/0.18)	$R_{d1,2}$ = 270 Ω	$C_{d1,2}$ = 4.50 pF

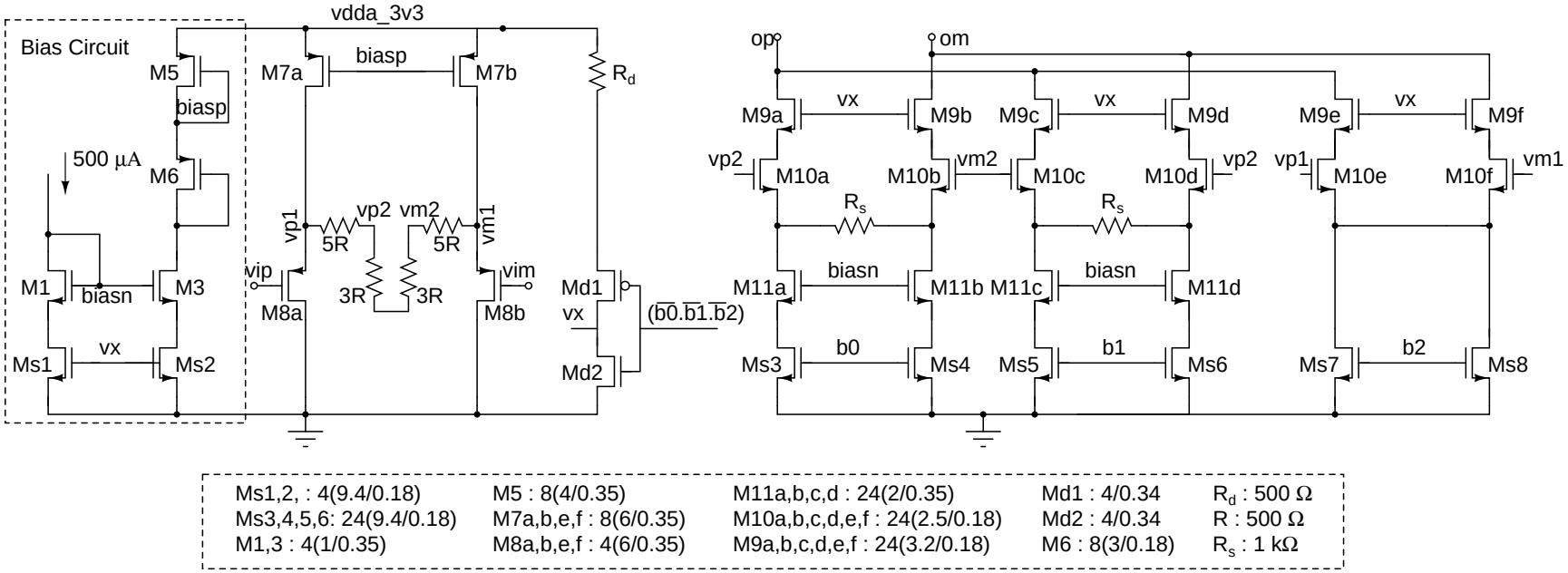
For C2 :	$R_{a1,2}$ = 590 Ω	$C_{a1,2}$ = 2.2 pF
M1a,b,c,d = 20(3/0.18)	$R_{b1,2}$ = 315 Ω	$C_{b1,2}$ = 4.15 pF
M2a,b,c,d = 28(3/0.18)	$R_{c1,2}$ = 215 Ω	$C_{c1,2}$ = 5.93 pF
M3a,b,c,d = 32(3/0.18)	$R_{d1,2}$ = 165 Ω	$C_{d1,2}$ = 7.50 pF

Figure 6.6: Differential schematic and element values of capacitor banks implementing C_1 and C_2 and their respective shunt conductances



M1a,b,c,d = 10(6/0.18)	$R_{b1,2}$ = 1.21 kΩ	$C_{b1,2}$ = 1.00 pF
M2a,b,c,d = 14(6/0.18)	$R_{c1,2}$ = 866 Ω	$C_{c1,2}$ = 1.39 pF
M3a,b,c,d = 16(6/0.18)	$R_{d1,2}$ = 674 Ω	$C_{d1,2}$ = 1.81 pF

Figure 6.7: Differential schematic and element values of capacitor bank implementing C_3



Ms1,2, : 4(9.4/0.18)	M5 : 8(4/0.35)	M11a,b,c,d : 24(2/0.35)	Md1 : 4/0.34	R_d : 500 Ω
Ms3,4,5,6: 24(9.4/0.18)	M7a,b,e,f : 8(6/0.35)	M10a,b,c,d,e,f : 24(2.5/0.18)	Md2 : 4/0.34	R : 500 Ω
M1,3 : 4(1/0.35)	M8a,b,e,f : 4(6/0.35)	M9a,b,c,d,e,f : 24(3.2/0.18)	M6 : 8(3/0.18)	R_s : 1 kΩ

Figure 6.8: Circuit implementation of the test buffer

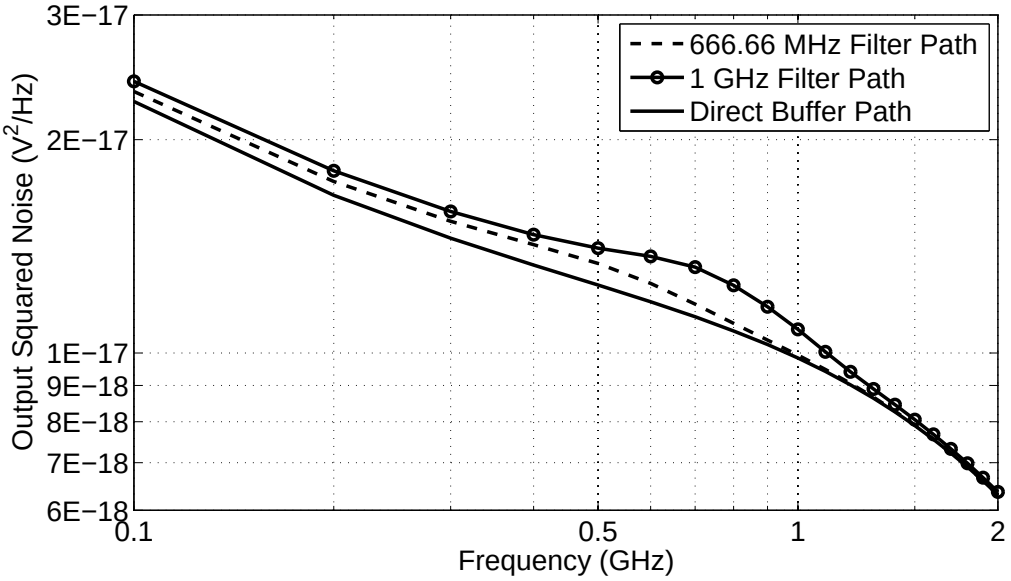


Figure 6.9: Squared output noise for direct and filter paths

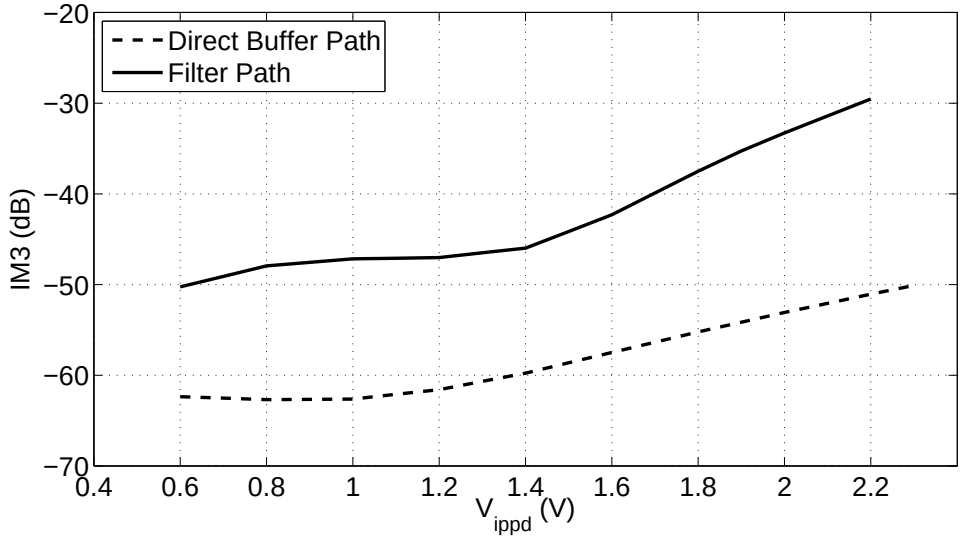


Figure 6.10: Comparison between distrotion levels of the filter and the buffer as a standalone device

CHAPTER 7

Layout and Simulation Results

7.1 Layout

The designed LC ladder filter was laid out using CADENCE Virtuoso Tool. Fig. 7.1 shows the layout of the design. The bounding box has dimensions of $1220\,\mu m \times 740\,\mu m$ but out of this $605000\,\mu\mathrm{m}^2$, i.e. two thirds of the total area, is occupied only by the top metal layer. This means that the whole transistor circuitry for this filter can be pushed below the inductor metal tracks or this design can be integrated with some other active filter design to obtain a widely tunable filter without using any extra chip area.

7.2 Simulation Results

Simulations of the entire filter are done after laying out and extracting the various blocks. But since the inductances are simulated using an EM simulator and Mos capacitors are laid out in N-wells, which renders them unrecognizable by ASSURA, Cadence's extracted views of these two blocks cannot be used during simulations. As mentioned in Chapter. 5, the inductor coil is modeled as a 3-port systems whose s-parameters are imported from Microwave Office over 10 MHz to 40 GHz range for the ac simulations. Although this would mean that process and temperature variations of the spiral's inductance and resistive values are ignored. For transient analysis the three inductors are replaced with their distributed pi models. To over come the non-extractable Mos capacitors problem, parasitic capacitances (obtained from the extracted view) are added to each node in the schematic itself. These parasitic capacitances are implemented using the metal-

metal capacitor models so that their variation across process corners is similar to the actual parasitic capacitances.

Also, across corners termination resistance has to maintained at its desired value by tuning it using control bits $br<0:2>$. This is very easily done by keeping the output common mode as close to 1.1 V as possible. If we ignore the change in quiescent current that flows through termination resistance (which as it turns out changes the common mode only by tens of millivolts), this common mode voltage tracking is the best method to maintain the correct value of termination resistances while simulating across corners and even while actual testing of the filter. Keeping it close to 1.1 V also minimizes the slight variations in capacitance of accumulation MOS transistors due to change in their V_{GB} bias.

7.2.1 AC simulations

The filter is tuned through its four modes of operation using control bits as mentioned in Table. 6.1. Fig. 7.2 shows the magnitude response of filter for different bandwidths. These plots are for simulations done at typical process corners. Variation of bandwidth across corners in different modes is listed in Table. 7.1. As expected the worst corners are the same in every bandwidth mode, i.e. in $ss - resmax - mimcapsmax$ corner bandwidth is least and maximum in $ff - resmin - mimcapsmin$. We know already that none of the implemented transfer functions are ideal Butterworth and apart from having a fractional DC gain, their poles do not exactly fall on an origin centered circle. So, the table also includes magnitude of maximum ripple in the pass band if any.

Table 7.1: Variation of filter bandwidth across corners

Nominal BW	Minimum	Typical	Maximum	DC gain (dB)	Ripple (dB)
400 MHz	358 MHz	372 MHz	393 MHz	−4.854	–
500 MHz	479 MHz	490 MHz	522 MHz	−3.687	–
666.66 MHz	648 MHz	669 MHz	695 MHz	−2.493	0.04
1000 MHz	977 MHz	985 MHz	999 MHz	−1.419	0.78

7.2.2 Distortion and noise analysis

The dynamic range of the filter in different bandwidth modes is measured using the SNDR plot. Input amplitude over which the sum of output noise and third order intermodulation tones' power remains below 1% of the signal power is taken as the filter's dynamic range. The output squared noise integrated over 10 MHz to 5 GHz bandwidth is used to find the minimum input signal whereas the −40 dB IM3 amplitude is taken as maximum signal swing to find the filter's dynamic range. Worst distortion frquencies are found to be near the band edge inside the pass band for each filter, by doing IM3 simulations at 500 mV V_{ippd} across varying inupt frequency.

Even though, the overall filter's maximum signal swing was decided by Gm-cell's non-linearity, it is expected to reduce because of use of non-resistive load in the termination ladder. As we go on adding extra branches in parallel in the termination load for lower bandwidth modes the portion of resistance being realised by pMOS switches keeps increasing, i.e. non-linearities are more for lower bandwidth modes. As can be seen in Table 7.2 swing limits for 1 GHz filter is almost the same as that of a input Gm-cell, but it keeps decreasing in each consecutive mode. But because of tuning down of 3 dB bandwidth, lowering of pass band gain and use of extra copies of the Gm-cells in parallel, smaller bandwidth modes have lower output noise levels (Fig. 7.3). Table 7.2 lists these figures as well as the calculated SNDR values for different bandwidth modes.

Table 7.2: Distortion and Noise in different bandwidth modes

BW (MHz)	−40 dB IM3 V_{ippd}	Integrated noise (V^2)	SNDR (dB)	Power (mW)
400	0.9 V	1.347×10^{-9}	72.73	125.8
500	1 V	2.274×10^{-9}	71.38	100.7
666.66	1.2 V	4.396×10^{-9}	70.01	75.6
1000	1.5 V	1.036×10^{-8}	68.31	50.5

7.2.3 Step response

Undershoot in step response of the filter can be used to gauge the effect of the negative inductance in series with C_2. Since, it has been compensated using the tapping coil's inductance and amounts to only 0.27 nH, i.e. effective coupling factor of $k_{12} = 0.27/(\sqrt{18.8 \times 12.1}) = 0.02$ the undershoot is expected to be negligible. An ideal 5^{th} order Butterworth system has ringing in its step response, thus the step response of different bandwidths also helps us compare the implemented filter's transfer function with an ideal one.

Fig. 7.4 shows normalized transient output from a unit step input to the filter at four bandwidth settings. 666.66 MHz filter has a response closest to Butterworth, since element values were calculated at 700 MHz whereas 400 MHz has the lowest quality factor as discussed in Chapter 2. Also, as seen from Fig. 7.5, there is no noticeable undershoot in any of the responses. This shows that the right hand s-plane zeros introduced because of mutual coupling between the two main coils have been compensated using positive inductance of the tapping coil.

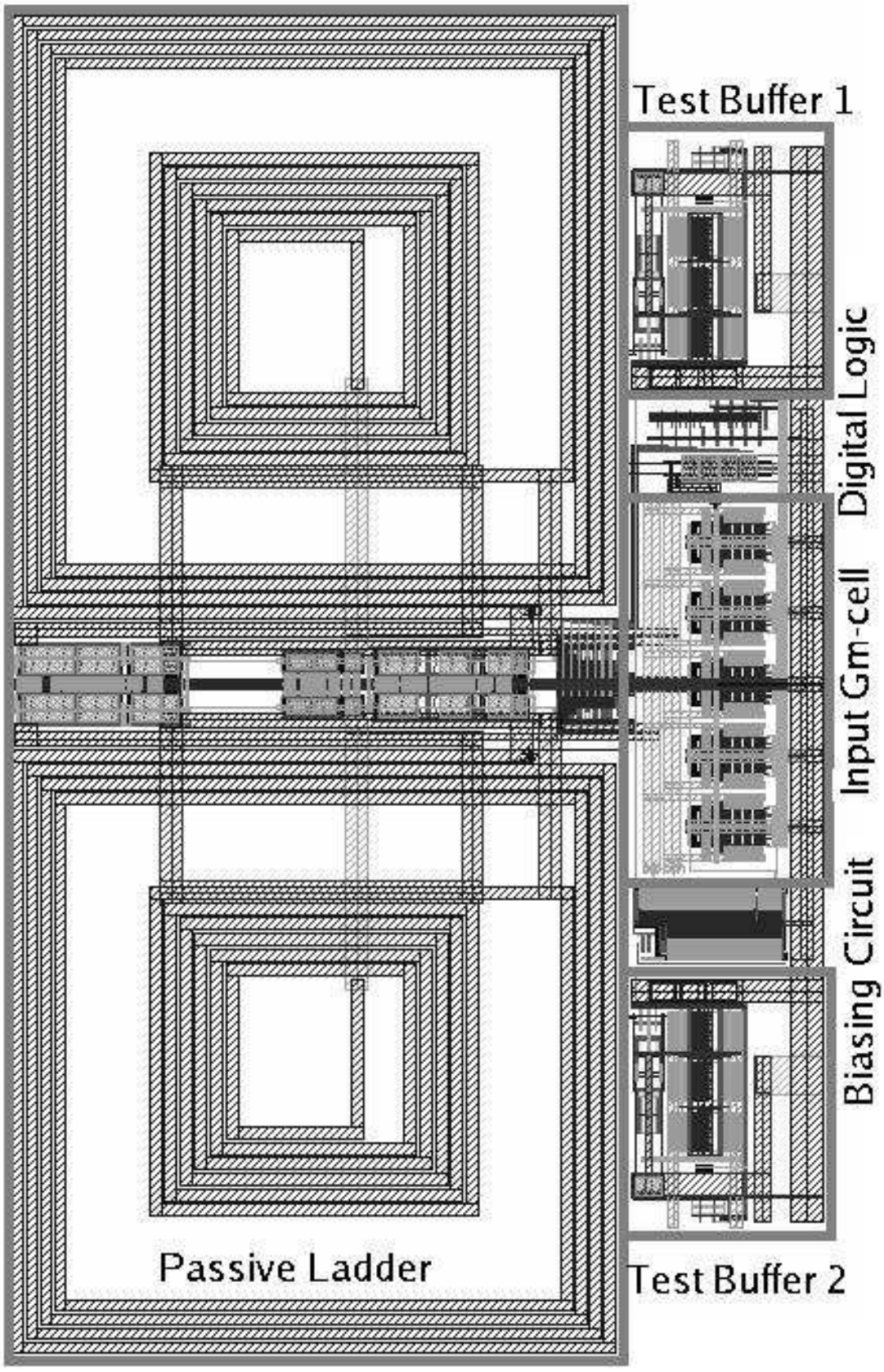


Figure 7.1: Layout of the Filter with test buffers

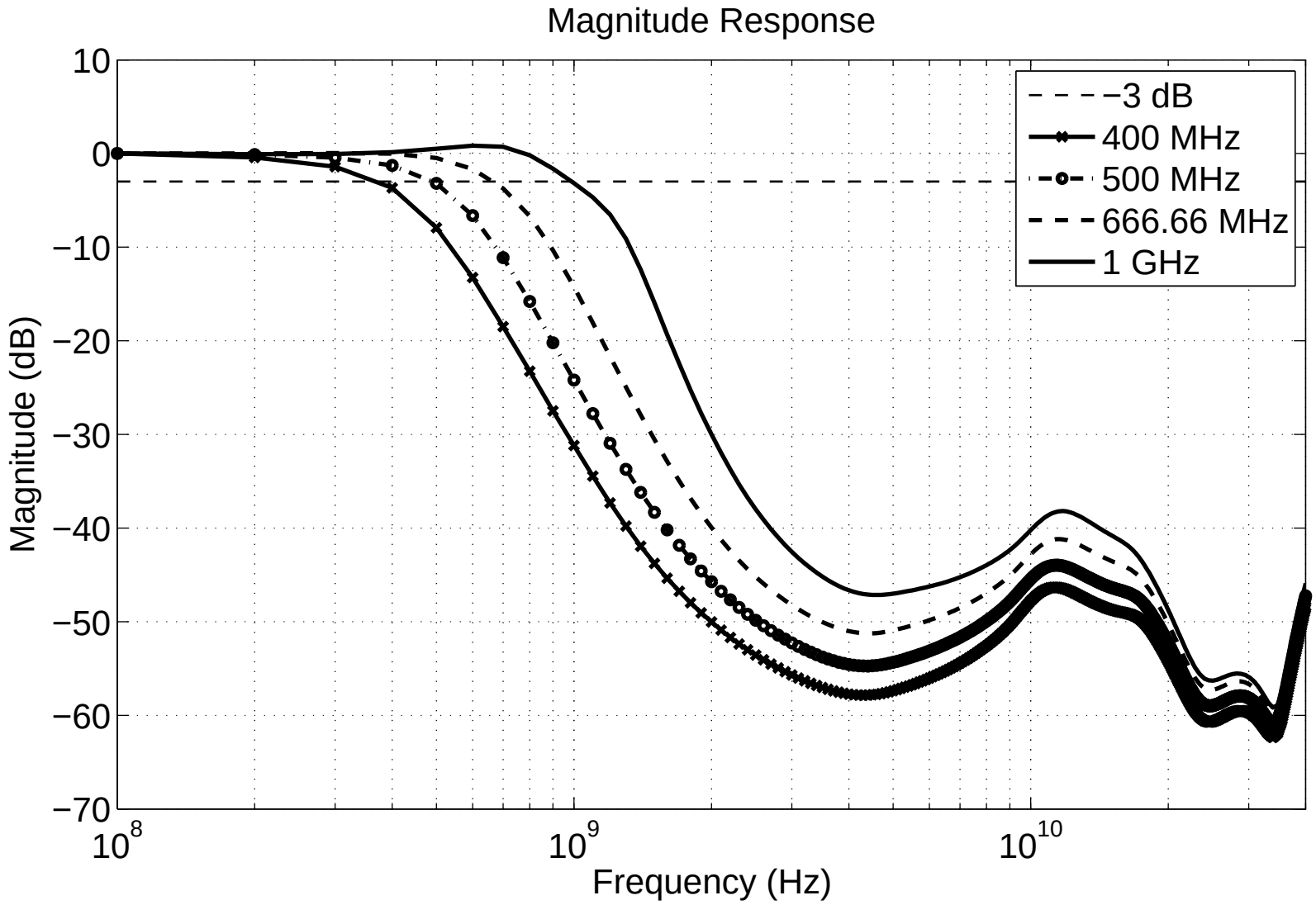


Figure 7.2: Magnitude response of filter tuned for four bandwidths

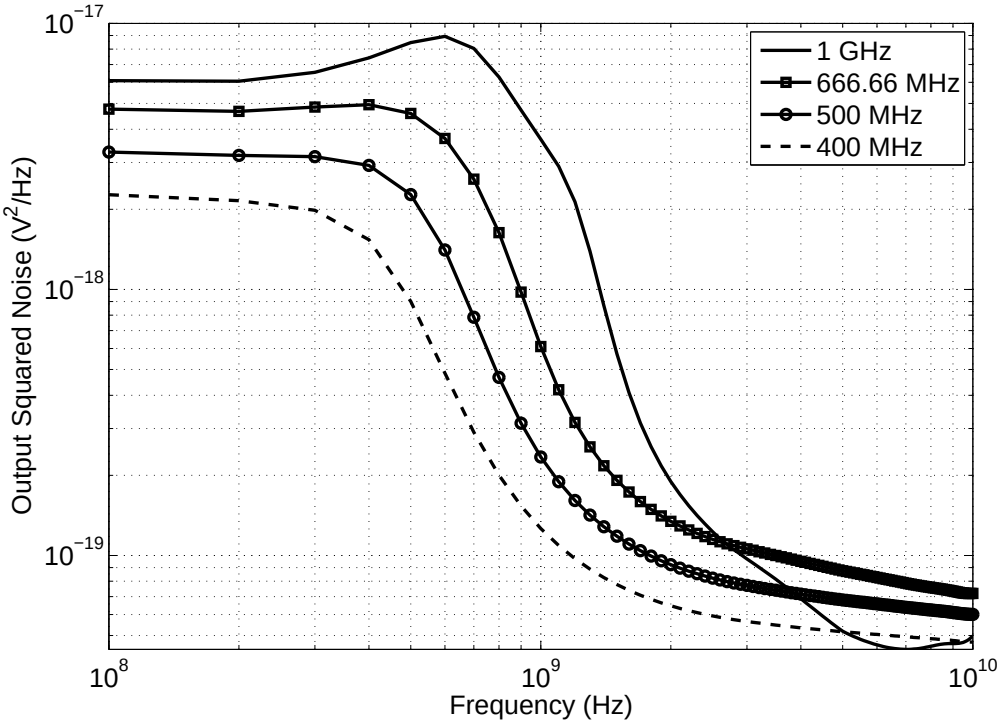


Figure 7.3: Squared output noise of the four filter modes

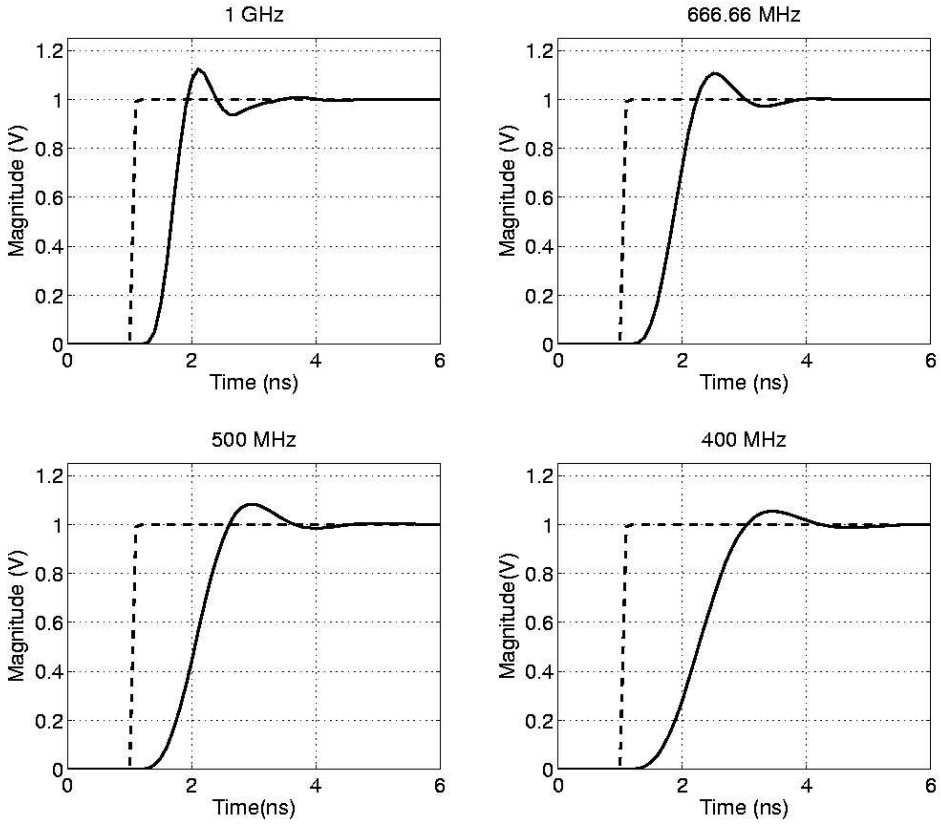


Figure 7.4: Normalized step response of the four filters

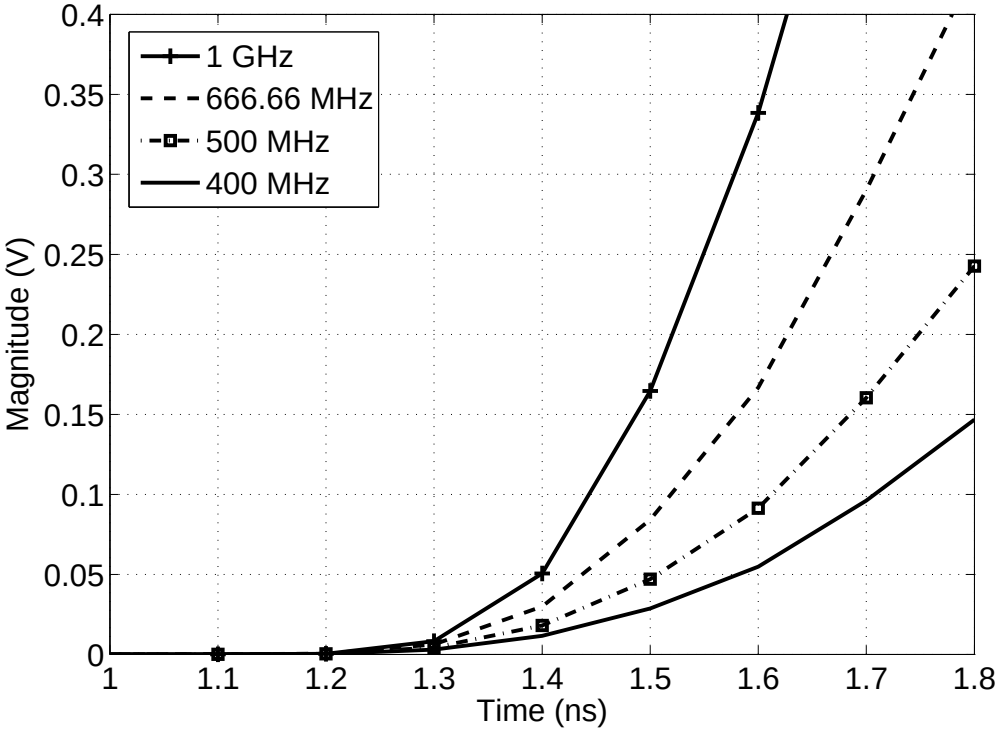


Figure 7.5: Close-up of step response to look for undershoot

CHAPTER 8

Conclusion and future work

8.1 Conclusion

The design and implementation of a tunable lowpass passive filter was discussed in this thesis. The regular problems presented by a passive filter like non optimal input and output impedances and difficulty in tunability are dealt with. Since, the bandwidth of interest is lower than the conventional frequency range in which passive filters are used, steps are taken to reduce the overall area of the chip without affecting its functionality, i.e. use of positive mutual coupling between inductors and MOS capacitors instead of metal-metal capacitors. The programmable termination resistance helps to cover for changes in element values over process corners such that the bandwidth in any mode does not vary from its nominal value by more than 5.65%. Cancellation of zeros by using inductance of tap made in the spiral ensures that there is no undershoot in the step response of filter. Even though the termination resistance and capacitances in ladder are not completely linear the input vccs' non linearity dictates the filter's dynamic range and use of source degenerated input Gm-cells ensures that in all modes of the filter it stays above 68 dB

8.2 Future work

In the presented design termination resistance is limited by the transconductance of the Gm-cell, which in turn decides how large the inductors need to be. Thus, a trade off between dynamic range and the chip area can be made according to requirement. Use of a simple differential Gm-cell would allow higher transconductance with low power usage and will translate to lower inductance values. Smaller

inductor spirals also mean that the capacitance between metal tracks and bulk substrate is less and a better stop-band attenuation can be achieved.

REFERENCES

[1] N. Krishnapura, V. Gupta, and N. Aggarwal, "Compact lowpass ladder filters using tapped coils," *International Symposium on Circuits and Systems (ISCAS)*, vol. 21, no. 6, 2009.

[2] "Asitic: Analysis and simulation of spiral inductors and transformers for ics."

[3] "FastHenry : http://www.fastfieldsolvers.com/."

[4] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 1999.

[5] A. Porrett, T. Melly, C. Enz, and E. Vittoz, "Design of high-q varactors for low-power wireless applications using a standard cmos process," *IEEE Journal of Solid State Circuits*, vol. 35, no. 3, pp. 337–345, 2000.

[6] S. Pavan, Y. Tsividis, and K. Nagaraj, "Modeling of accumulation mos capacitors for analog design in digital vlsi processes," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 143–146, 1999.

[7] T. Laxminidhi, *Accurate Design and Characterization of High Frequency Continuous-Time Filters*. PhD thesis, PhD Thesis, Department of Electrical Engineering, IIT-Madras, Chennai – 600036, Nov 2007.