# HIGH PERFORMANCE FLASH A-D CONVERSION USING DISTORTION COMPENSATION AND BACKGROUND OFFSET CORRECTION

*A THESIS*

***submitted by***

**V.V.SRINIVAS**

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DEPARTMENT OF ELECTRICAL ENGINEERING
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# THESIS CERTIFICATE

This is to certify that the thesis entitled "**HIGH PERFORMANCE FLASH A-D CONVERSION USING DISTORTION COMPENSATION AND BACKGROUND OFFSET CORRECTION**" submitted by **V.V.Srinivas** to the Indian Institute of Technology , Madras for the award of the degree of the Master of Science is a bonafide record of the research work carried out by him under my supervision. The contents of the thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Chennai-36 Research Guide

Date : ( )

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# ABSTRACT

A flash ADC design technique has been proposed that compensates for static nonlinearity of the up-front sample and hold circuit, so that high speed and high linearity can be obtained at the same time. The proposed technique functions in synergy with a new background comparator offset correction scheme. The design of the building blocks of the ADC are discussed in certain detail and the important simulation results for each block are presented. The excess quantization noise generated due to the background autozero process is derived. Measurement results are given for a 160 Msps 6-bit flash converter designed in a 0.35-$\mu$m CMOS process. The ADC consumes 50 mW from a 3.3 V power supply and gives 5.3 effective number of bits at Nyquist frequency for a clock speed of 160 MHz.

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# CHAPTER 1

# INTRODUCTION

## 1.1 INTRODUCTION

High speed flash analog to digital converters find a wide range of applications, from disk drive read channels to wireless transceivers. The block diagram of a typical flash ADC is shown in Figure 1.1. A track and hold (or a sample and hold) samples the continuous-time input and holds it for half a clock cycle. This held value is compared against a set of references, typically generated using a resistor ladder. In practice, there will be offsets in the comparators, which need to be corrected. The comparator outputs are processed by the digital back end to yield an N bit digital word that is representative of the continuous-time input. The track and hold is not strictly necessary, as one could use the inherent sampling properties of the comparators to sample the input. However, clock skews in the comparator array are bound to result in poor dynamic performance. It has therefore become commonplace to use some form of track and hold mechanism at the input of a flash converter. The comparator array now processes a "held" signal, so that clock skews are no longer an issue. The track and hold also serves to drive the large capacitance of the comparator array while presenting only a small load at the converter input.

Incorporating a track and hold upfront causes several problems. Since this necessarily will be operating at high speeds, it is usually not possible to use feed-

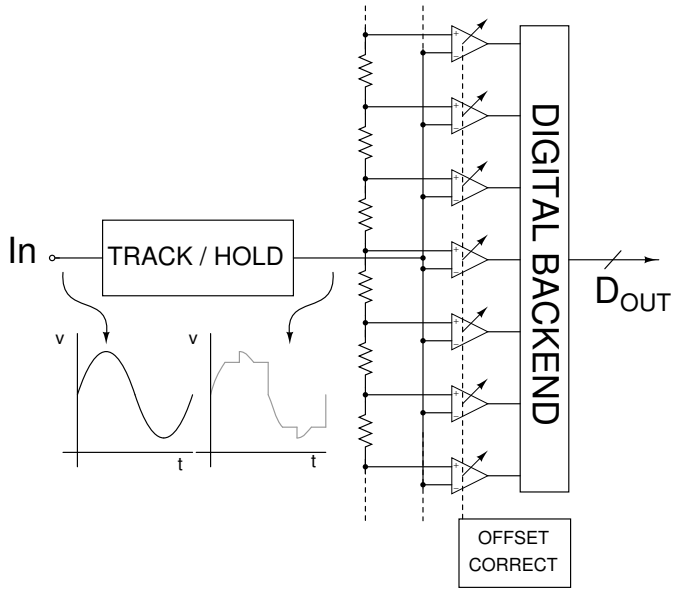


Figure 1.1: Block diagram of a typical flash ADC.

back based linearizing techniques - fast, open loop circuits are called for. These open loop track and hold circuits exhibit significant static nonlinearity (nonlinearity which is independent of input frequency), causing distortion, thereby limiting the peak input signal swing of the converter. For example, many published designs with upfront track and holds are able to handle signals of about 1 $V_{pp}$ (differential) even in a 3.3 V supply [1][2][3][4]. The design as reported in [5] handles a signal swing of 1.6 $V_{pp}$. Reduction of input swing results in a smaller LSB size, so offsets in the comparator need to be smaller. This leads to increased device sizes and power dissipation. It is thus seen that use of a larger input swing (while somehow eliminating distortion) could reduce power dissipation of the entire ADC.

In this thesis, we present a technique to compensate for the static nonlinearity of an open loop track and hold, so that high speed and low distortion could be achieved at the same time. This technique works in synergy with a new back-

ground offset scheme that cancels comparator offsets. This scheme exploits the bubble-correction logic to make the auto-zeroing process completely transparent to the user. A unique feature of the proposed technique is that the layout complexity is the same as a regular flash ADC.

## 1.2 ORGANIZATION OF THE THESIS

The thesis is organized as follows. In chapter 2, the mechanism of distortion in a flash ADC due to T/H nonlinearity and ways of compensating it are discussed. The top level architecture of the six bit flash ADC designed is discussed in Chapter 3. In chapters 4,5,6 and 8 the block design of track & hold, comparator, clock generator and reference generator are discussed. Chapter 7 discusses about the existing background offset correction schemes and the disadvantages associated with them. The digital logic and the counter design are discussed in Chapter 9. The degradation in SNR due to background autozero is found in Chapter 10. In Chapter 11, the extension of this technique to folding is discussed. Chapter 12 discusses about the board that was designed to test the chip. In Chapter 13, measurement results of the 6-bit 160 Msps flash ADC designed in a $0.35\,\mu\mathrm{m}$ CMOS process are presented. Conclusions are given in Chapter 14.

# CHAPTER 2

# REFERENCE PREDISTORTION

## 2.1 DISTORTION IN A FLASH ADC DUE TO TRACK AND HOLD NONLINEARITY

Consider a 3-bit flash ADC with an ideal track and hold (T/H) with unity gain. The input output characteristic of the T/H is shown in Figure 2.1. The reference voltages given to the seven comparators are $V_{ref1}, V_{ref2}, \ldots, V_{ref7}$ which are same as $\Delta, 2\Delta, \ldots, 7\Delta$ where $\Delta$ denotes the LSB of the converter. If the analog input is $n\Delta + \epsilon$, where $n$ is an integer and $0 < \epsilon \leq \Delta$, the T/H output will also be $n\Delta + \epsilon$, thereby causing the lower $n$ comparator outputs to go high, resulting in a digital code word of $n$. In essence, the ADC output is a faithful representation of the input to within an LSB.

Now consider what happens when there is a static nonlinearity in the track and hold, as shown in Fig. 2.2, where the non-ideal characteristics of the T/H have been exaggerated for clarity. If the analog input is $n\Delta + \epsilon$, we see that the output of the T/H is smaller than the input, and $n$ comparator outputs will *not* be high. This manifests as ADC nonlinearity. It is apparent from the input-output characteristics of a real T/H as shown in Fig. 2.2 that the outputs of comparators 5, 6 & 7 will never go high since the output of T/H never exceeds $V_{ref5}$ which is the reference of the $5^{th}$ comparator.

The above discussion suggests the following - the ADC would behave in a distortion-free manner *if, in spite of the T/H nonlinearity* we make sure that for an analog input of $n\Delta + \epsilon$, the lower $n$ comparators have high outputs, thereby resulting in a digital output code of $n$. One way of accomplishing this is to predistort the reference voltages to the comparators according to the following. The ideal references $(\Delta, 2\Delta, \ldots, 7\Delta)$ are applied as the inputs to track and holds that are identical to the one used in the signal path. The outputs of the track and holds are used as the new references to the comparators. Under these circumstances, if the analog input is $n\Delta + \epsilon$, the lower $n$ comparators will have high outputs, even though the track and hold is nonlinear, because their reference voltages ($V_{ref1}, \ldots, V_{ref7}$ in Figure 2.3) have been distorted by precisely the same amount as the track and hold would distort the input signal. Thus, distortion free operation will result.

Macromodel simulations were done in MATLAB to verify the above assertion. First, a 6-bit flash ADC with linearly increasing reference levels is driven by a track and hold with a weakly cubic nonlinearity The resulting signal power normalized

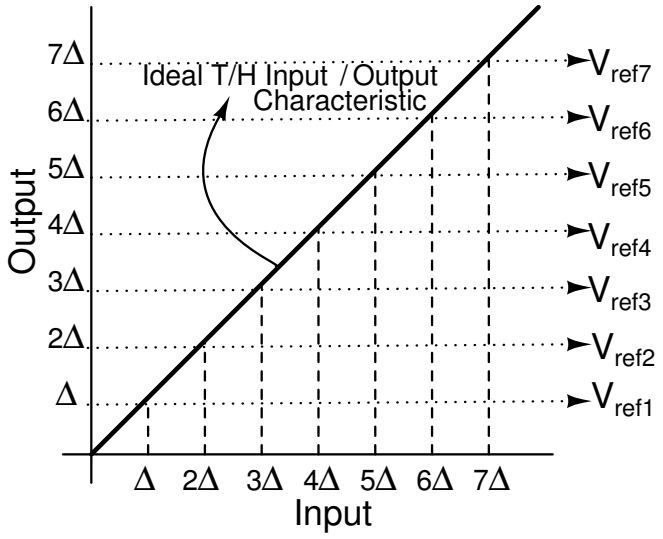


Figure 2.1: Flash ADC behavior with an ideal track and hold.

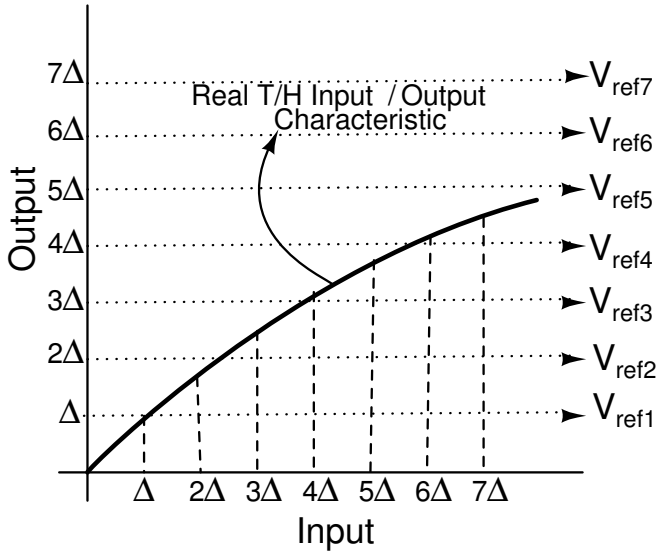


Figure 2.2: Flash ADC behavior with a real track and hold having static nonlinearity.

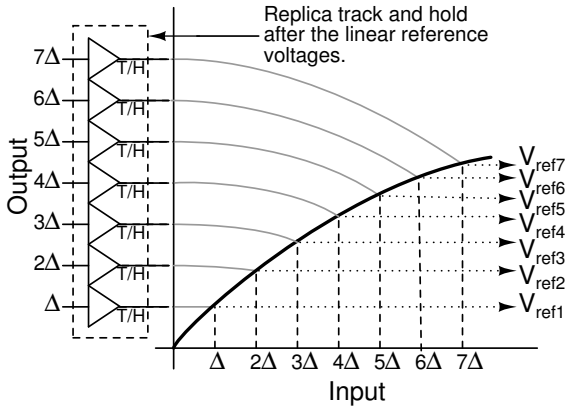


Figure 2.3: Flash ADC behavior with a track and hold having static nonlinearity and references predistorted.

output spectrum is shown on the left in Figure 2.4. As expected, there is a significant amount of third harmonic distortion in the ADC output spectrum. When the references are predistorted by replica track and holds, (but with the nonlinear T/H driving the comparator array remaining the same), the resulting ADC spectrum, shown towards the right of the figure, shows no distortion. Note that reference predistortion inherently corrects for the systematic gain error of the track and hold. A technique that scales the ADC reference based on the T/H gain was proposed in [6]. Note however, that that technique does not correct for distortion.

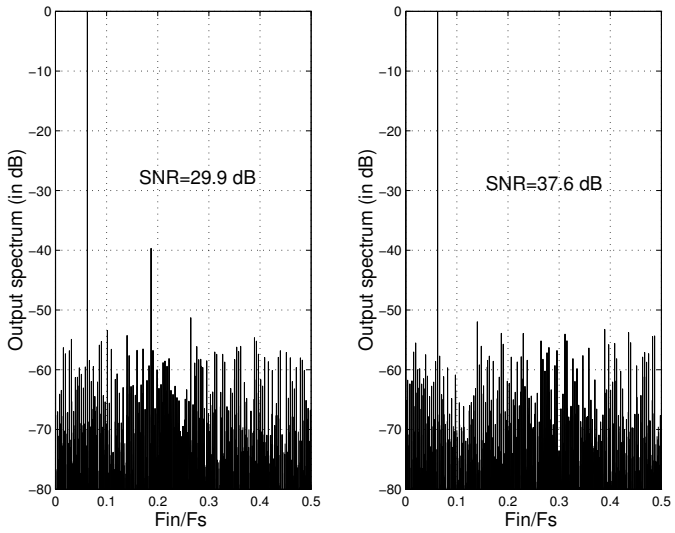


Figure 2.4: ADC output spectrum with track and hold having static nonlinearity and references linear in one case and references predistorted in the next case.

## 2.2 DYNAMIC VERSUS STATIC DISTORTION

One potential issue with the distortion compensation technique discussed above is the performance at high input frequencies. In order to examine this issue, simulations were done at two different clock speeds. The track & hold was at the transistor level in these simulations. The quantizer was implemented in MATLAB with either the linear or predistorted references as the case may be. Figure 2.5 shows the SNDR of the ADC output as the input frequency is varied with linear and predistorted references for two different clock speeds. The thin lines indicate the SNDR for a clock speed of 100 MHz whereas the thick lines indicate the variation of SNDR for a clock speed of 200 MHz. Note that as the input frequency increases, the SNDR degrades in both cases (linear and predistorted references) due to the dynamic distortion of the front-end track & hold for the two different clock speeds. However, at any given input frequency notice that the ADC with

predistorted references has superior performance.

If the reference predistortion scheme is implemented exactly as shown in Fig. 2.3,

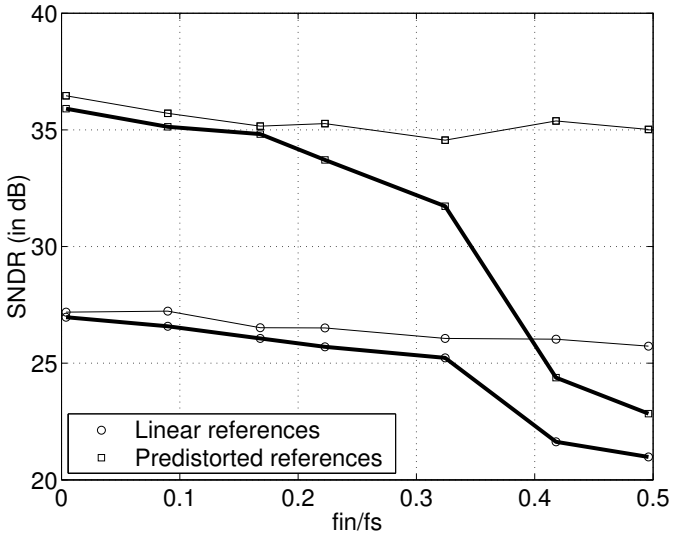


Figure 2.5: Simulated SNDR with varying input frequency for linear and predistorted references. The sampling rate is 100 MHz (thin lines) and 200 MHz (thick lines).

the proposed technique would consume enormous amounts of power in a flash ADC with a nontrivial solution due to the number of replica T/H's present. Offsets in these replica track and holds would also be a potential issue. A solution to this problem is the repeated use of the same replica track-and-hold to predistort the references of all comparators.

Another issue that needs to be addressed in a flash ADC is the mitigation of comparator offsets caused by random device mismatch. This can be done in the background, i.e the offsets of the comparators can be corrected one by one. In the next chapter, we show how reference predistortion can be efficiently combined with background offset correction, in effect realizing the scheme of Fig. 2.3 while using only one replica T/H in the reference path.

# CHAPTER 3

# ARCHITECTURE OF THE FLASH ADC

## 3.1 BLOCK DIAGRAM OF THE FLASH ADC

The top level block diagram of the flash ADC is as shown in Figure 3.1. The DAC that is present in the block diagram is for testing purposes. The salient features of each block are discussed in the chapters that follow.

## 3.2 PRINCIPLE OF OPERATION

The input is held using a track and hold circuit and then it is compared against a set of references using an array of comparators. The comparator is a cascade of a preamplifier and a latch. The clock generator block shown in Figure 3.1 generates the clocks needed by various blocks in the ADC. The comparator has two important phases of operation - autozero and amplify. Figure 3.2 shows the simplified schematic of the comparator when it is being autozeroed. The capacitors Cc are charged differentially to the reference voltage $(Vrefp - Vrefm)$ in this phase. These reference voltages are the predistorted references generated using linear reference and replica track and hold circuit. During its amplifying phase the preamplifier is configured as shown in Figure 3.3. The reference is subtracted from the input using the capacitors and then a decision is made depending on the polarity of the voltage. Ideally speaking if there are no switch leakage currents

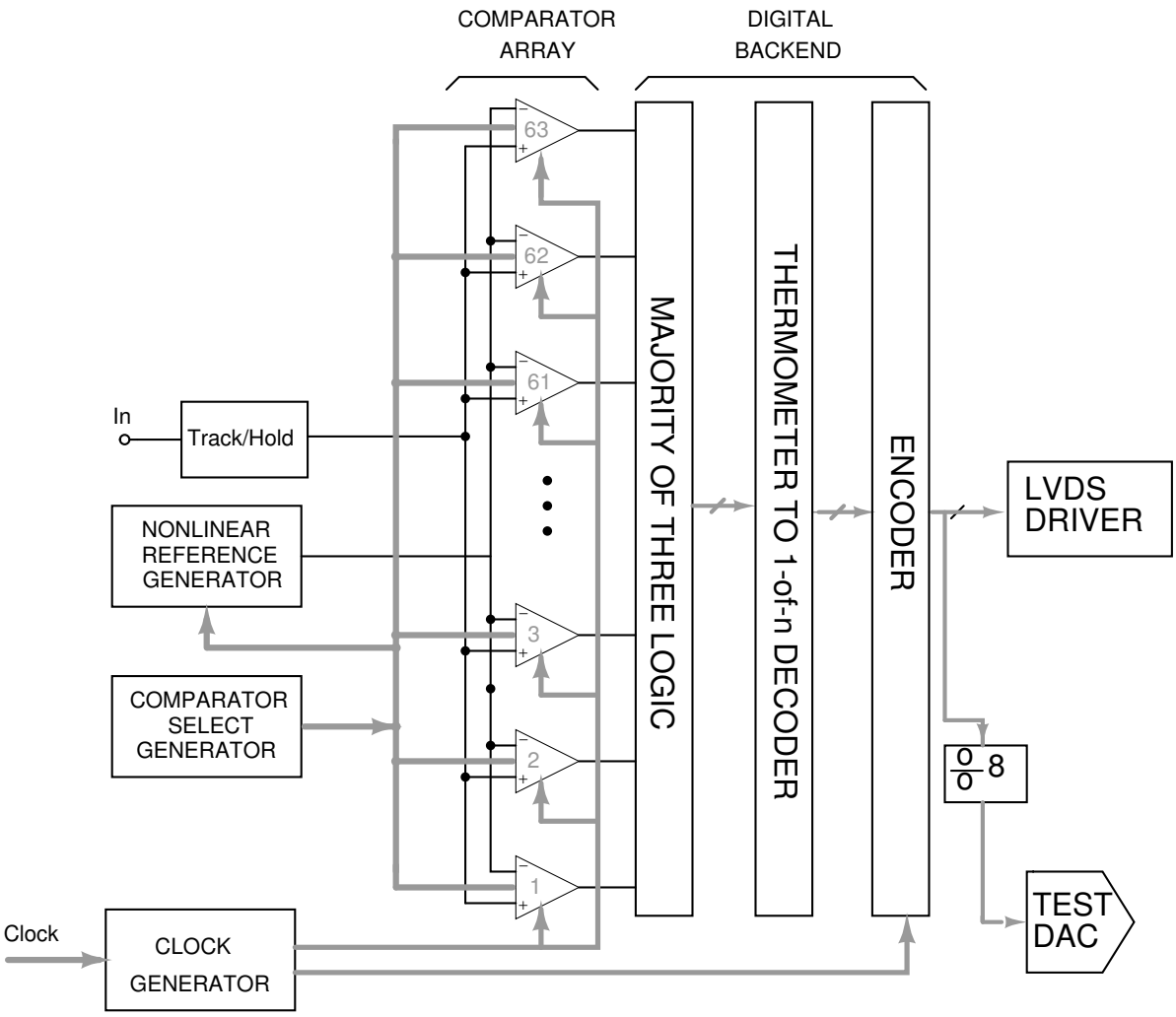


Figure 3.1: Flash ADC architecture.

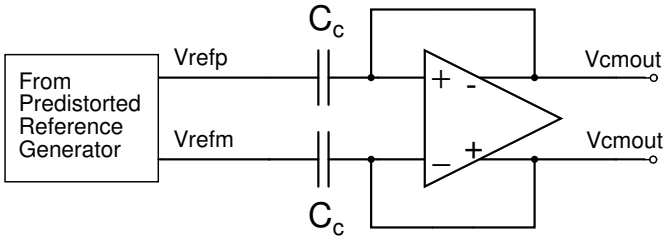


Figure 3.2: Autozeroing of comparator.

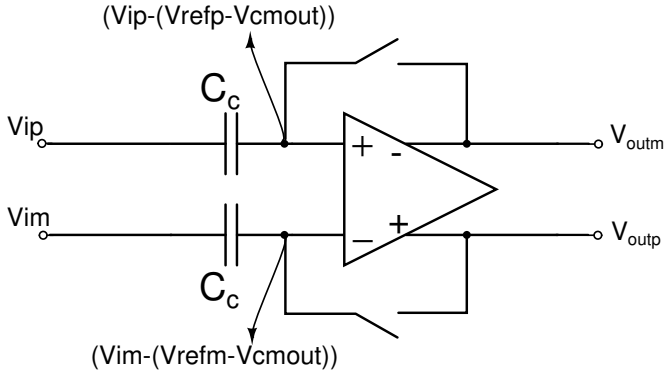


Figure 3.3: Comparator during its normal operation.

one needs to autozero the 63 comparators just once at the beginning of the conversion. In reality there will be leakage currents associated with the switches and this will slowly drain away the charge present in the capacitors. To mitigate this the capacitors charge can be refreshed periodically. Also this refreshing need not be done in every clock cycle but can be done only as often as demanded by the switch leakage current magnitude and the size of the capacitor. The refereshing of the capacitor charge can be done in background wherein one comparator is removed from conversion cycle and it is autozeroed as shown in Figure 3.4 wherein the $k^{th}$ comparator is being autozeroed.At any point of time it is enough if only one predistorted reference is available. This is achieved by selectively choosing a linear reference, passing it through a replica track and hold circuit. During this time the appropriate comparator has to be selected which is to be autozeroed.

When a comparator is being autozeroed it gives out a random decision. The quantized output might be in error because of this and there can be a degradation in the SNR of the ADC. The majority logic which follows the comparator array is used to make full advantage of the background offset correction scheme without much degradation in the SNR of the ADC. The loss in SNR because of the background offset correction will be discussed in Chapter 9.

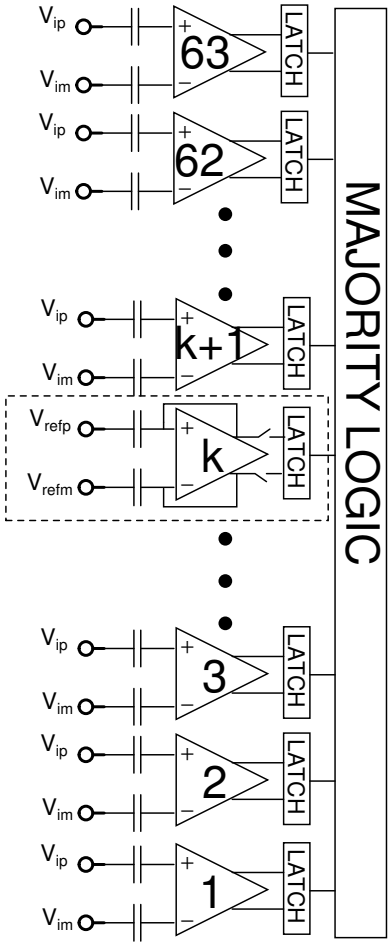


Figure 3.4: $k^{th}$ comparator is autozeroed.

A 6-bit binary weighted current steering DAC has been incorporated in the ADC to aid debug. This works at $\frac{1}{8}^{th}$ the clock frequency of the ADC. This DAC gives a differential current as its output and to convert it into a voltage resistors are placed on board. To interface with the external world, LVDS (low voltage differential signaling) drivers were designed. LVDS is an IEEE standard for high data rate digital transmission. These drive an on board LVDS receiver. The LVDS receiver gives out CMOS compatible digital outputs which can be captured using a logic analyzer.

# CHAPTER 4

# TRACK AND HOLD DESIGN

## 4.1 ARCHITECTURE OF THE TRACK AND HOLD

Closed loop architectures for the track and hold circuit will give good linearity compared to their open loop counter parts. But their speed will be limited because one has to ensure stability of the feedback loops formed[7]. So we have to go for open loop architectures if high speed of operation is desired. The simplest open loop track and hold circuit that one can think of is as shown in Figure 4.1. The operation of this circuit is quite simple. When $\Phi_{clk}$ is high, the output, Vout tracks the input, Vin and when $\Phi_{clk}$ is low the output is held constant. The problem with this circuit is that the on resistance of the switch varies as the input varies in the track phase. Variation in the on resistance of the switch with signal swing will

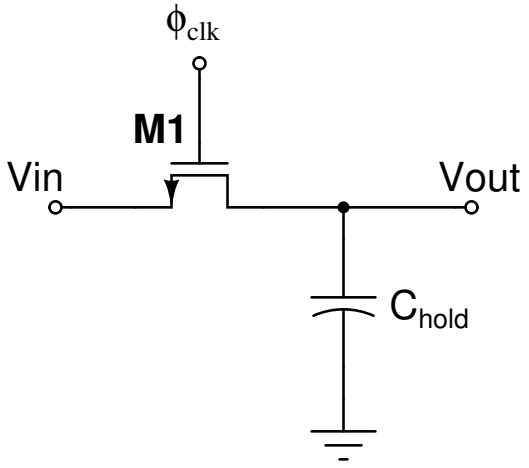


Figure 4.1: Simple track and hold circuit.

lead to a variation in the bandwidth of the circuit formed by M1 and the holding capacitor Chold. This will lead to distortion as the gain is dependent on the signal. The other problem associated with this circuit is signal dependent charge injection when the switch is turned off which will lead to distortion. To overcome these problems a constant-gate overdrive switch is used for sampling. An input buffer is needed to prevent the loading of the circuit driving the track and hold circuit and an output buffer is needed to drive the load offered by the comparator array.

### 4.1.1 Switch size and capacitor size

The capacitor should be chosen such that the SNR because of the capacitor and the switch resistance at the output of the track and hold is say 60 dB (The SNR due to quantization noise in a 6-bit ADC is 37.8 dB and we want the SNR due to switch resistance to be much higher than that.). The signal swing is 0.85 V single ended peak and we need a SNR of 60 dB

$\Rightarrow \frac{\frac{A^2}{2}}{\frac{kT}{C}} = 10^6$

$\Rightarrow C = 11.5fF$

If the capacitor is greater than 11.5 fF than the SNR due to switch resistance will be greater than 60 dB.

The switch size has to be such that the tracking bandwidth is equal to the sampling frequency and the smaller the size of the switch the better it is as charge injection will be less. When a NMOS switch of size $(\frac{1}{0.35})\mu$m was driven with an overdrive of Vdd it presented an on resistance of 2 k$\Omega$. We want the tracking bandwidth to be atleast 160 MHz.

$\Rightarrow \frac{1}{2\pi r_{on} C} \geq 160 \times 10^6$

$\Rightarrow C \leq 497fF$

If the capacitor is too low (compared to 11fF) we will be limited by $\frac{kT}{C}$ noise and also the distortion of the track and hold circuit will be significant as the non-linear capacitors of the switch will be dominant. If the capacitor is too high (compared to 497fF) the tracking bandwidth will be low. A value of 200fF which is in between these two values was chosen.

### 4.1.2 Input Buffer

The function of the input buffer is to prevent the loading of the circuit driving the track and hold. A NMOS source follower as shown in Figure 4.2 is the input buffer. First we will try to calculate the current Io needed in the buffer (refer to Figure 4.2). The current should be sufficient so that there will not be any slewing taking place when the output is tracking the input. The maximum rate of change of the voltage at the output is given by $A\omega$ when the excitation is $A \sin \omega t$. The current through the capacitor is given by C$\frac{dV_{out}}{dt}$. The maximum of $\frac{dV_{out}}{dt}$ is given by $A\omega$. The current is C$A\omega$. In our case $A = 0.85$ and $\omega = 2\pi \times 80 \times 10^6$

$\Rightarrow I = 85.5\ \mu$A

The current has to be greater than $85.5\ \mu$A so that slewing will not take place. One more constraint that needs to be satisfied by the current Io is that when the output is held at its maximum possible voltage and in the next clock cycle the output has to go to the minimum possible voltage ( this happens when the input is at Nyquist rate) the current Io should be high enough. In other words, we should have Io$\geq$ C$\frac{\Delta V}{\Delta t}$ $= 200 \times 10^{-15} \times \frac{1.7}{3 \times 10^{-9}}$(the maximum swing possible is $3.4\ V_{pkpk}$ differential )$= 113.3\ \mu$A. A current of $125\ \mu$A was chosen for Io.

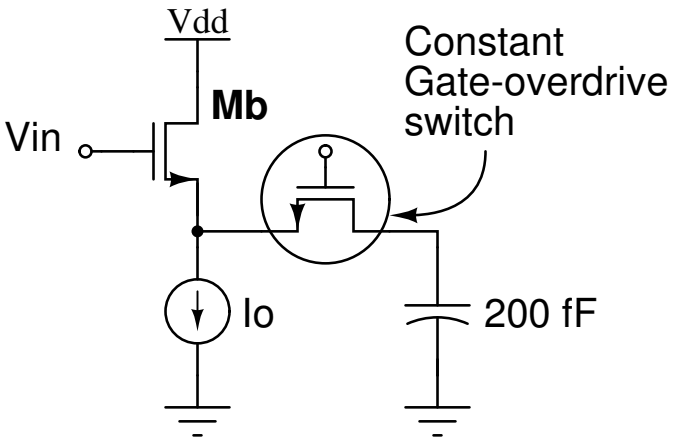


Figure 4.2: Input buffer driving the sampling capacitor.

### 4.1.3 Output Buffer

The function of the output buffer is to drive the load presented by the comparator array. The natural choice for the output buffer is a PMOS source follower because the input common mode is dropped by a threshold and over-drive of the NMOS source follower transistor. The common mode can be got back to the same level as the input by using a PMOS source follower with appropriate gate over-drive voltage. The source and bulk of the PMOS are connected together as shown in Figure 4.3. This was done to get rid of the attenuation and the distortion that would be introduced because of the body effect. The current $I_{buf}$ had to be made 1 mA in the output buffer so that it could drive the comparator array along with the extra parasitic capacitors in the layout.

### 4.1.4 Schematic of the track and hold circuit

Figure 4.4 shows the schematic of the track and hold half-circuit used in this work. M2 drives the sampling capacitor through an NMOS sampling switch M1. In order to reduce dynamic nonlinearity, the sampling switch is implemented as a "constant gate-overdrive" switch [1]. The functioning of the circuit is as follows. In

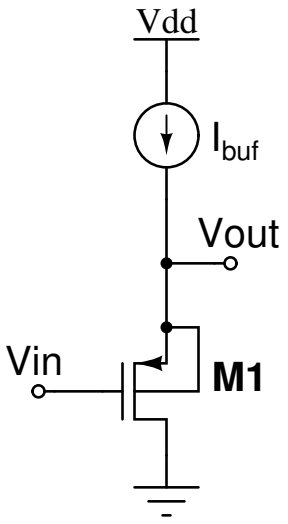


Figure 4.3: Output buffer driving the comparator array.

hold phase $\phi_1$ is high and $\phi_2$ is low. The sampling switch M1 is off and output is held constant. During this phase the capacitor $C_{BAT}$ is charged to Vdd. At the end of hold phase, tracking phase begins by making $\phi_1$ low and $\phi_2$ high. Note that $\phi_1$ and $\phi_2$ have to be non-overlapping clocks. During the tracking phase the Vgs of M1 is Vin+Vdd-(Vin-$Vgs_{M2}$). We know that $Vgs_{M2} = V_{T_{M2}} + \Delta V_{M2}$. The gate to source voltage of M1 is given by $Vgs_{M1}$ = Vin+Vdd-(Vin-$Vgs_{M2}$) = Vdd + $Vgs_{M2}$. The gate overdrive of M1 is $Vgs_{M1} - V_{T_{M1}} = Vdd + \Delta V_{M2}$, assuming $V_{T_{M1}} = V_{T_{M2}}$. This is a valid assumption as source to bulk voltages of M1 and M2 are identical and hence the change in $V_T$ because of the body effect will be the same. The gate overdrive of M1 is Vdd + $\Delta V_{M2}$ in the tracking phase and this is independent of the input voltage Vin. This way the switch on resistance is maintained constant irrespective of the input voltage.

The comparator array is driven by the PMOS source follower comprising of M3 and I2. The body and source of M3 are tied together to avoid distortion and attenuation which arise due to the body effect. The dominant source of static nonlinearity in the track and hold is the body effect of M2 in the input buffer. Other distortion

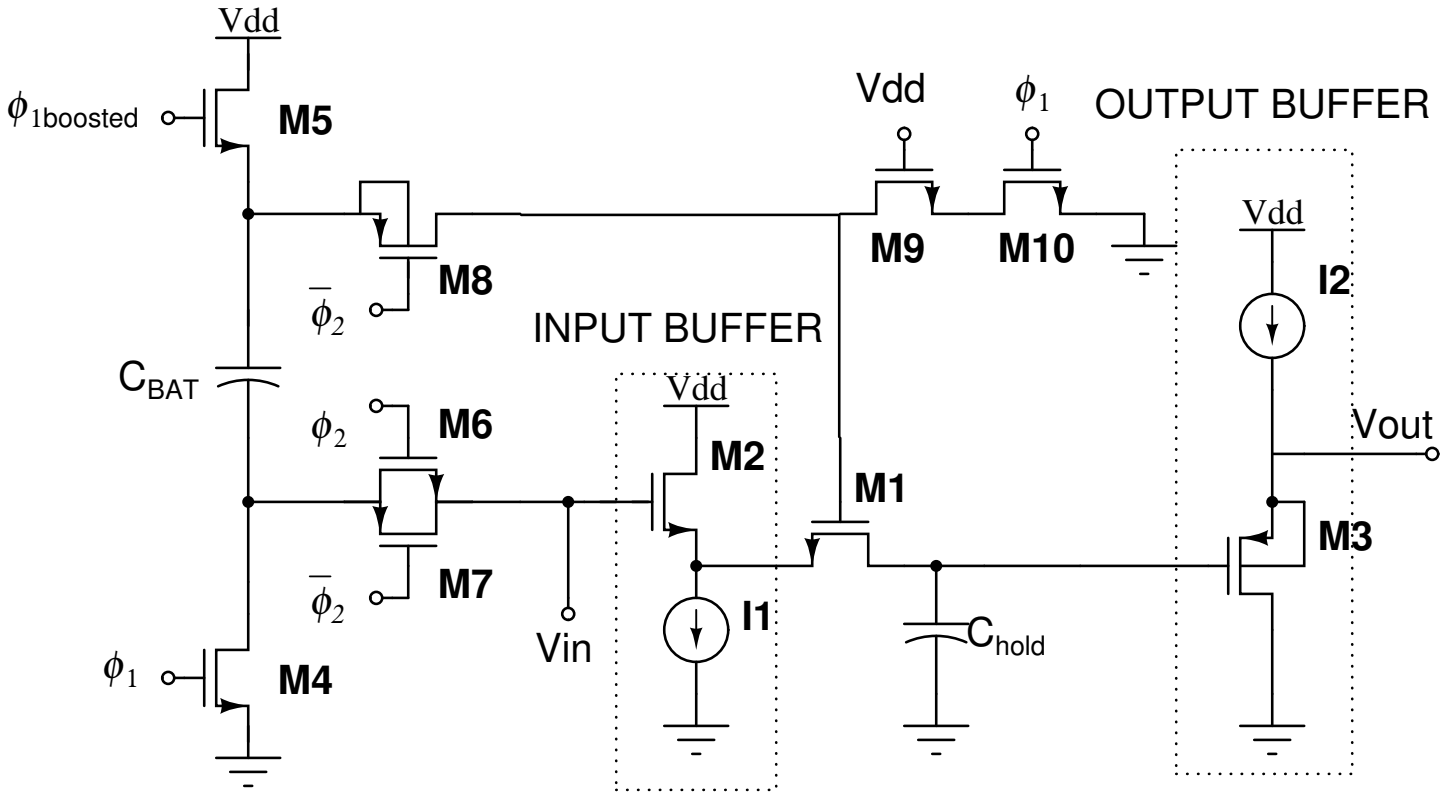


Figure 4.4: Track & hold half circuit.

mechanisms are the output impedances of M2 & M3 and the current sources I1 and I2.

### 4.1.5 Replica track and hold

The schematic of the replica and hold circuit is as shown in Figure 4.5. The transistor M1 in Figure 4.5 is a scaled version of M2 of Figure 4.4 and transistor M4 is a scaled version of M3 of Figure 4.4. The transistors M2 and M3 in Figure 4.5 which control the current through the NMOS and PMOS source followers are also scaled appropriately so that these are just a scaled versions of the input and output buffers used in the track and hold present in the signal path. This ensures that the references stored across the capacitors are predistorted in the same manner as the input is distorted by the track and hold circuit.

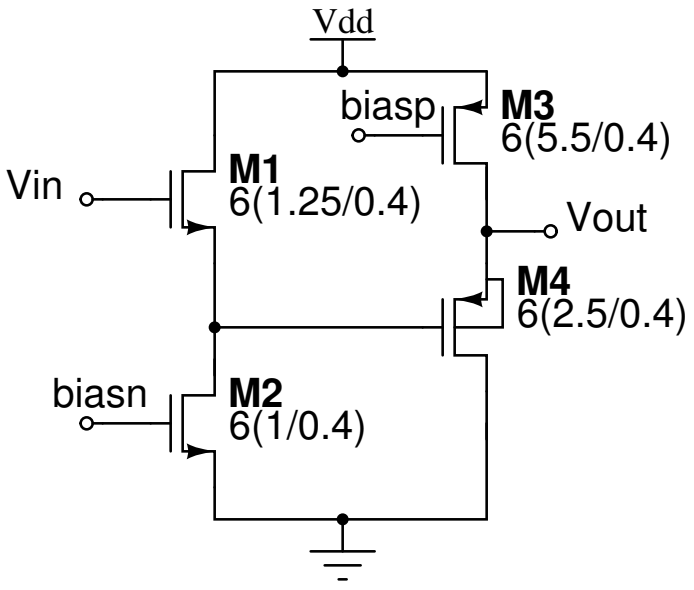


Figure 4.5: Replica track & hold half circuit.

### 4.2 SIMULATION RESULTS

The track and hold was simulated across process variations and supply variations to ensure its functionality across corners. During these simulations, the track and hold was presented with a simulated load of 63 comparators. The input and output voltages of the track & hold circuit are as shown in Figure 4.6 for a typical process corner, cmostm and a supply voltage of 3.3 V at a temperature of 70 °C. It can be observed from this plot that the output of the track & hold does not swing as much as its input voltage but there is an attenuation. This attenuation is, mainly because of the body effect present in the input buffer, which is a NMOS source follower stage. The $HD_3$, which is a measure of the linearity, of the track and hold output for 100 MHz clock speed and an input of 48.4375 MHz is tabulated in Table 4.1 for various process corners. The simulation is repeated for a clock speed of 160 MHz and an input of 77.5 MHz and the results are tabulated in Table 4.2.

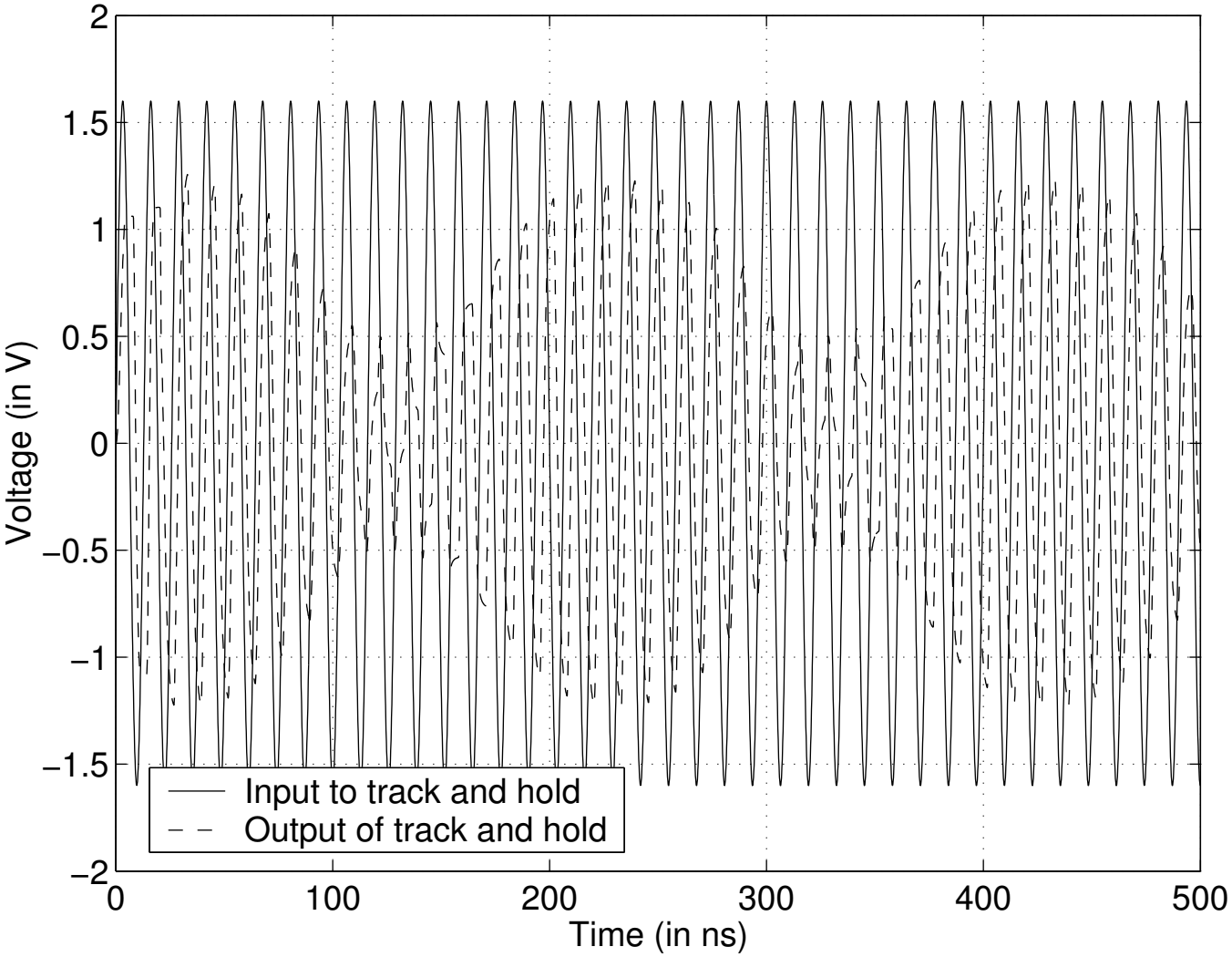


Figure 4.6: The input and output the track & hold circuit in cmostm corner for a clock speed of 160 MHz and an input of 77.5 MHz.

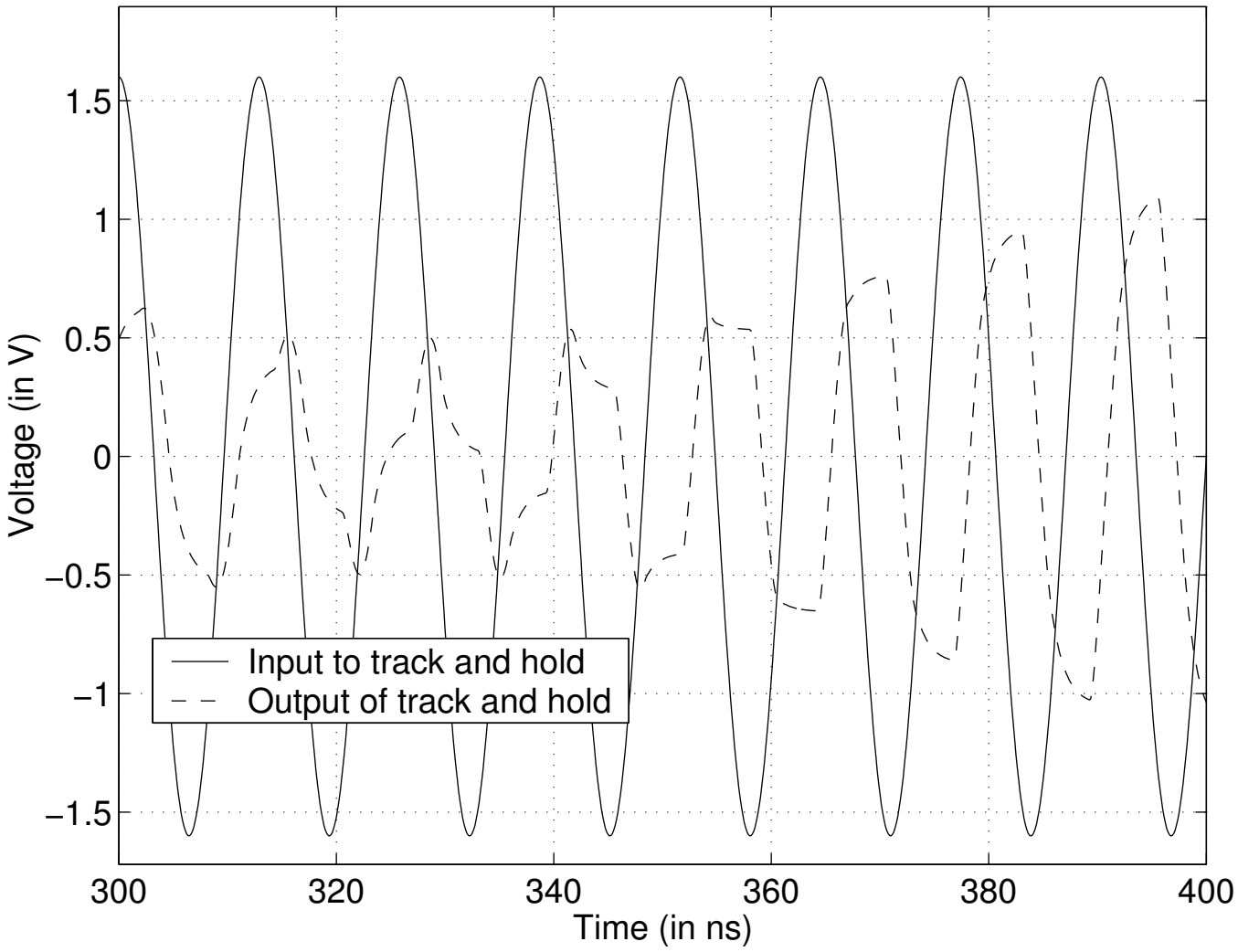


Figure 4.7: Zoomed in version of Figure 4.6 from 300 nS to 400 nS.

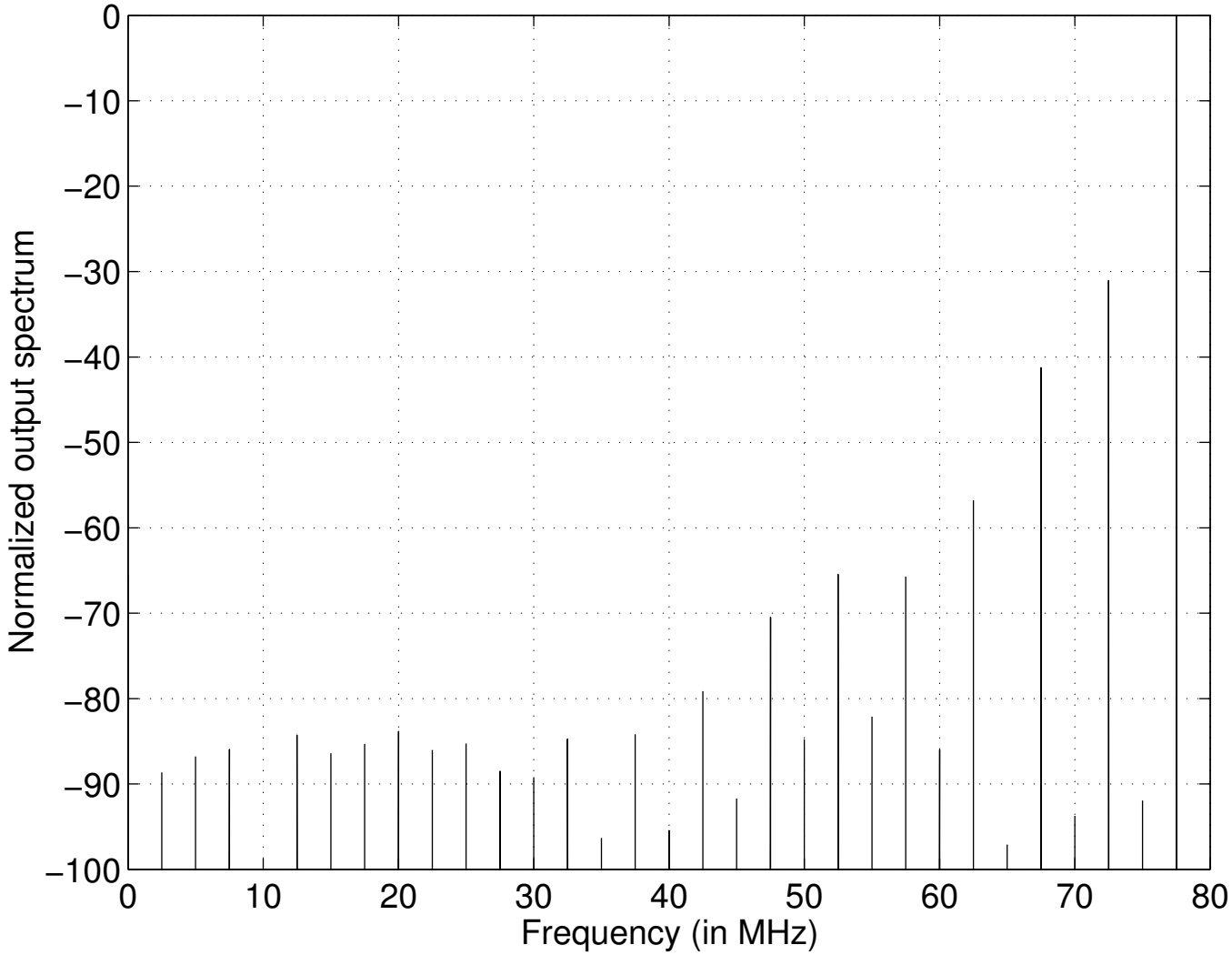


Figure 4.8: The output spectrum of the track & hold circuit in cmostm corner for a clock speed of 160 MHz and an input of 77.5 MHz.

Table 4.1: Harmonic distortion component of the track and hold output at a temperature of 70 °C and a clock speed of 100 MHz.

| Process corner | Supply | HD3 (in dB) |
|---|---|---|
| cmostm | 3.3 | -46.8 |
| cmosws | 3.3 | -47.7 |
| cmoswz | 3.3 | -48.6 |
| cmoswp | 3.3 | -45.5 |
| cmoswo | 3.3 | -30.9 |
| cmostm | 3.0 | -40.2 |
| cmosws | 3.0 | -37.6 |
| cmoswz | 3.0 | -50.5 |
| cmoswp | 3.0 | -43.4 |
| cmoswo | 3.0 | -26.8 |

Table 4.2: Harmonic distortion component of the track and hold output at a temperature of 70 °C and a clock speed of 160 MHz.

| Process corner | Supply | HD3 (in dB) |
|---|---|---|
| cmostm | 3.3 | -31.0 |
| cmosws | 3.3 | -33.3 |
| cmoswz | 3.3 | -34.0 |
| cmoswp | 3.3 | -35.4 |
| cmoswo | 3.3 | -24.2 |
| cmostm | 3.0 | -27.5 |
| cmosws | 3.0 | -30.4 |
| cmoswz | 3.0 | -33.6 |
| cmoswp | 3.0 | -32.0 |
| cmoswo | 3.0 | -20.6 |

# CHAPTER 5

# COMPARATOR DESIGN

## 5.1 COMPARATOR

A simplified schematic of the comparator and representative waveforms during its operation are shown in Figure 5.1. It consists of a preamplifier and a latch. The preamp gain effectively reduces latch offset when referred to the comparator input. During regular operation, the autozero signal AZ is low. The preamp inputs are connected to the track & hold outputs. The switches are operated according to the timing diagram shown toward the left in the lower part of Fig. 5.1. When the T/H output is tracking the input signal, the preamp is reset by making PRST high. It begins to amplify when PRST goes low. The preamp outputs are connected to the latch inputs through the switches LC, so that the latch input capacitances can be charged to an amplified version of the preamp differential input. While the latch is being charged regeneration is disabled by making LE low. The preamps are of the dynamic gain type [1][6]. Once LC goes low, LE goes high so that the latch can regenerate. During this time, the preamp is reset again. At the end of the regeneration period, the decisions are processed by the majority logic and the rest of the digital back end. The latch is reset so that memory of past decisions is removed.

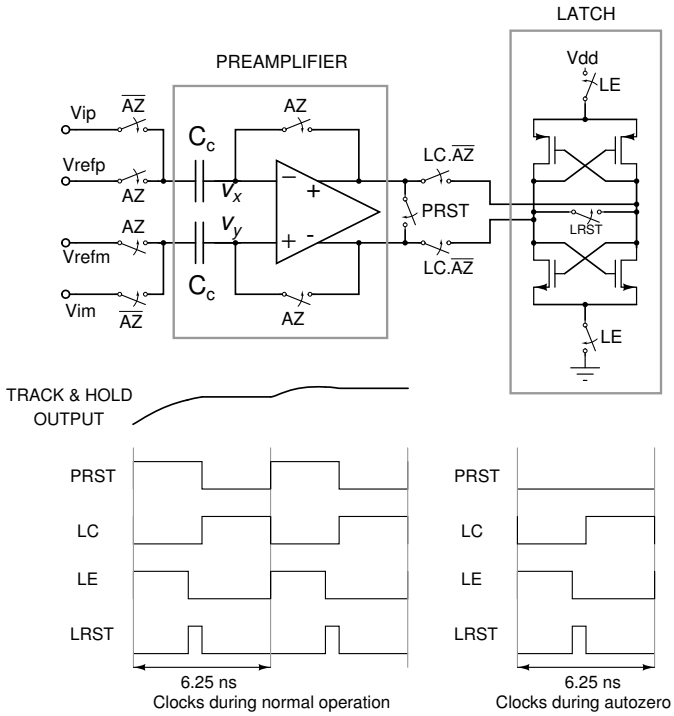


Figure 5.1: Comparator schematic and timing diagram of the clocks.

## 5.2 OFFSET CANCELLATION

The preamps suffer from offset because of device mismatches. This offset is estimated and canceled during an autozero phase (AZ). When AZ is high, the input of the preamp is disconnected from the T/H output ($V_{ip}$ and $V_{im}$). The preamp reset signal is set to zero and the inputs are connected to the desired references ($V_{refp}$ and $V_{refm}$), generated by the nonlinear reference generator as shown in Figure 5.2. Let the DC gain of the preamp be denoted by $A_{pre}$ and its input referred offset be denoted by $V_{off}$. The offset is modeled as a battery of value $V_{off}$ in series with an input terminal of an ideal differential opamp of gain $A_{pre}$. During the autozero mode i.e., when AZ is high we have

$$(v_x + V_{off} - v_y)A_{pre} = v_y - v_x \tag{5.1}$$

$$\Rightarrow v_x - v_y = -\frac{A_{pre}}{1 + A_{pre}} V_{off} \tag{5.2}$$

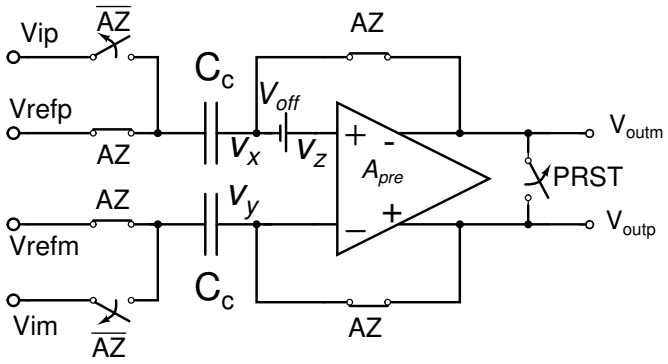


Figure 5.2: Configuration of the preamplifier when it is autozeroed.

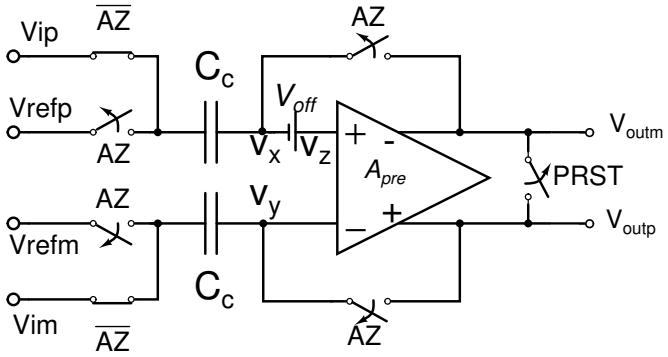


Figure 5.3: Configuration of the preamplifier in amplify phase.

In regular operation i.e., when AZ is low, the preamplifier is configured as shown in Figure 5.3. The preamp is connected to the track & hold output ($V_{ip}$ and $V_{im}$). The reference voltages ($V_{refp}$ and $V_{refm}$), which are generated from predistorted reference generator, are disconnected from the preamp. The differential input to the ideal differential amplifier now is given by

$$v_z - v_y = (V_{ip} - (V_{refp} - v_x) + V_{off}) - (V_{im} - (V_{refm} - v_y)) \tag{5.3}$$

$$= (V_{ip} - V_{im}) - (V_{refp} - V_{refm}) + (v_x - v_y) + V_{off} \tag{5.4}$$

$$= (V_{ip} - V_{im}) - (V_{refp} - V_{refm}) - \frac{A_{pre}}{1 + A_{pre}} V_{off} + V_{off} \tag{5.5}$$

$$\Rightarrow v_z - v_y = (V_{ip} - V_{im}) - (V_{refp} - V_{refm}) + \frac{V_{off}}{1 + A_{pre}} \tag{5.6}$$

The new input referred offset now after autozeroing the preamp is $\frac{V_{off}}{1+A_{pre}}$ as against $V_{off}$ when there is no offset correction being done. Hence the input referred offset of the preamp gets divided by the DC gain of the preamp because of autozero

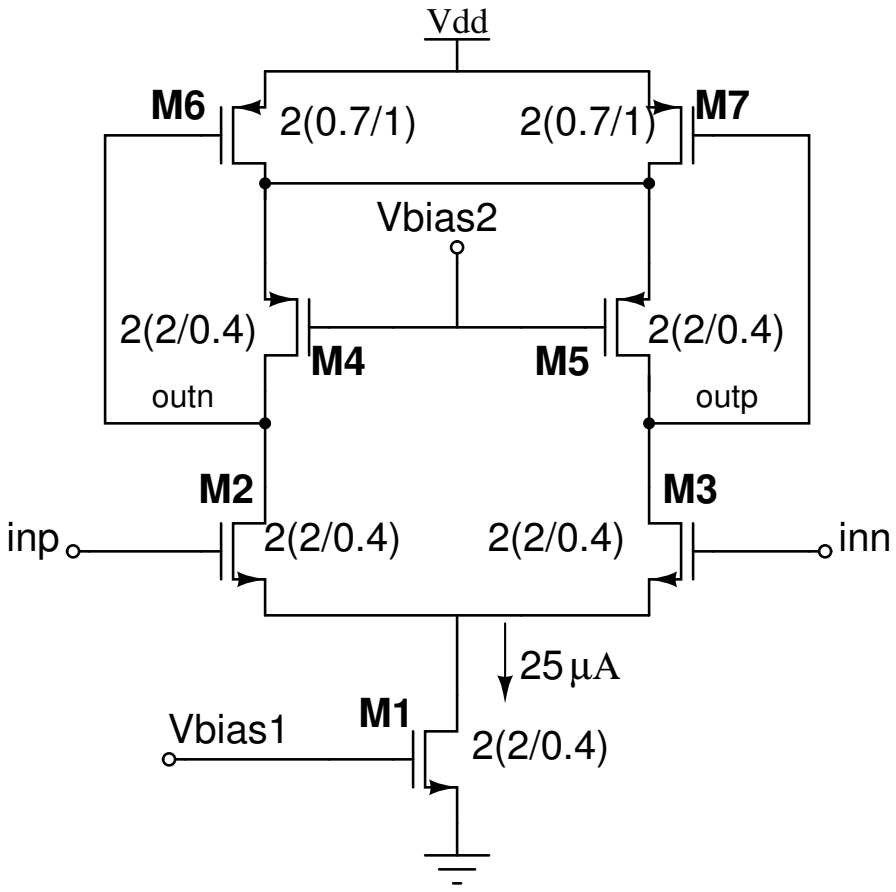


Figure 5.4: Schematic of the preamplifier.

operation. The LE and LRST signals are still active during autozero period, so that the latch puts out a random decision when the preamp is being autozeroed.

### 5.3 PREAMPLIFIER

The schematic of the preamplifier is as shown in Fig 5.4. M2 and M3 constitute the input pair of the preamplifier. M6 and M7 provide common mode feedback. These transistors are operated in saturation region so as to maximize the common mode loop bandwidth. M4 and M5 are the active loads so that we get a high impedance during differential operation and the preamplifier works as an integrator giving us the maximum possible dynamic gain.

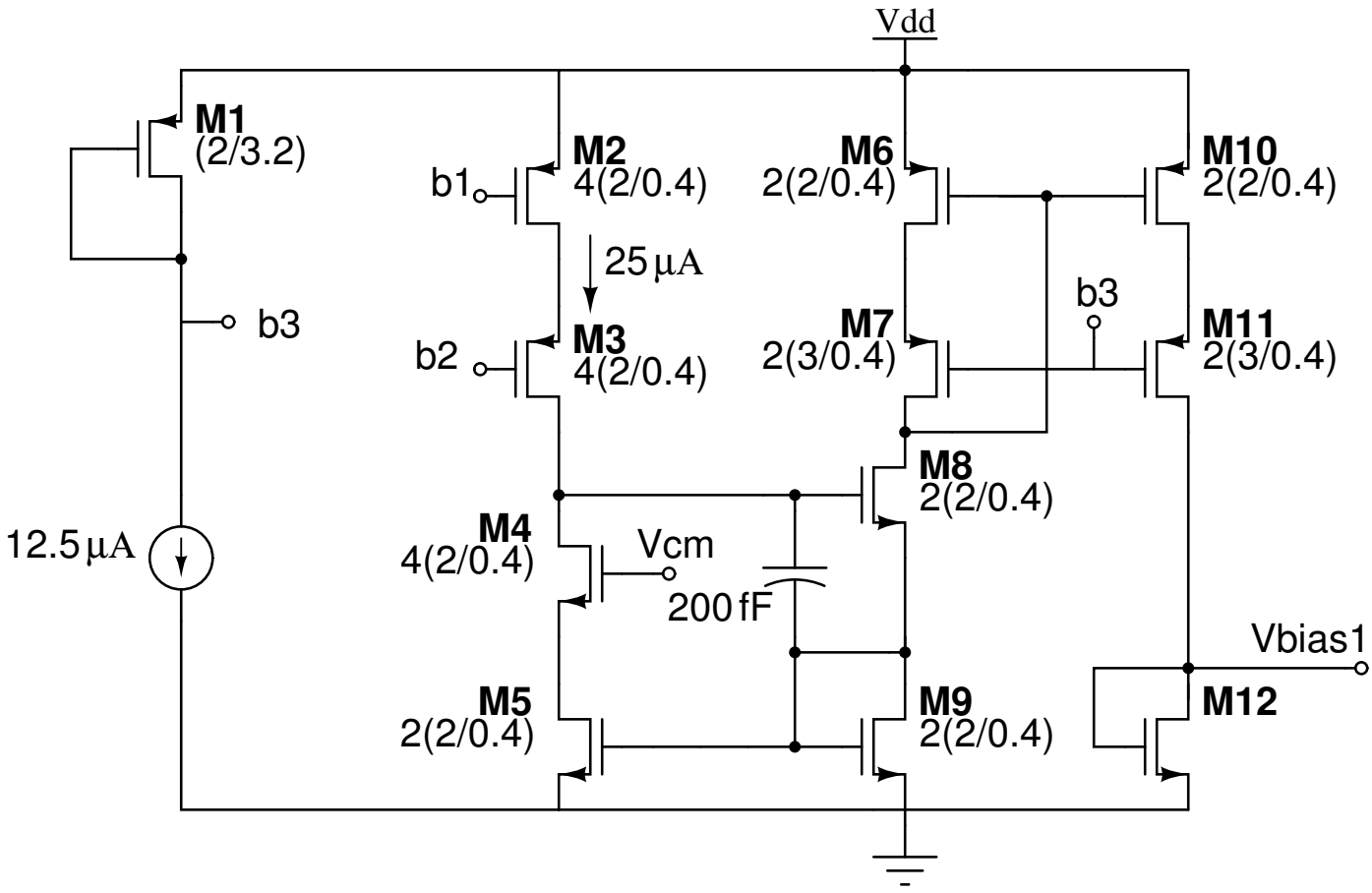


Figure 5.5: Generating bias for tail NMOS transistor.

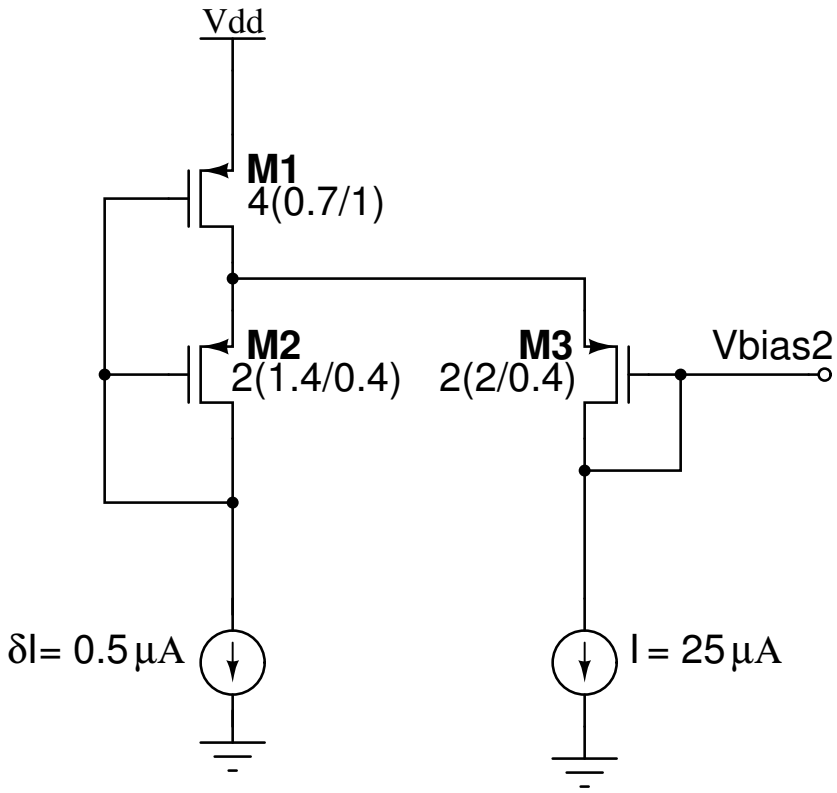


Figure 5.6: Generating bias for PMOS transistors.

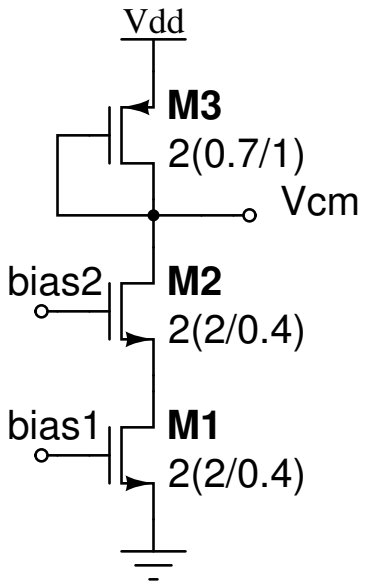


Figure 5.7: Generating common mode voltage for the preamplifier.

### 5.3.1 Choosing the coupling capacitor Cc

We have seen in the previous section the role of the coupling capacitors Cc connected in series with the preamp inputs. Now we will try to fix the value of this capacitor. This capacitor is realized using the two poly layers available in the process. There will be a bottom plate parasitic capacitor(Cb) associated with this which arises because of the capacitance from the bottom poly layer of the capacitor to the substrate. In the present technology this is around 30% of the actual capacitor. We have a choice of keeping this Cb at the input of the preamp as shown in Figure 5.8 or keeping it at the other side as shown in Figure 5.9 . The arrangement in Figure 5.8 will attenuate the signal by $\frac{Cc}{Cc+Cb} \approx 0.77$ before it gets amplified by the preamp. This is not desirable as the dynamic gain of the preamp will decrease. So the bottom plate capacitor is kept away from the input of the preamp as shown in Figure 5.9. There will still be attenuation of the signal because of the parasitic capacitors of the preamp. Ideally we would like to have a large value for Cc so that this attenuation is negligible. But higher the value of Cc, higher will be Cb. The

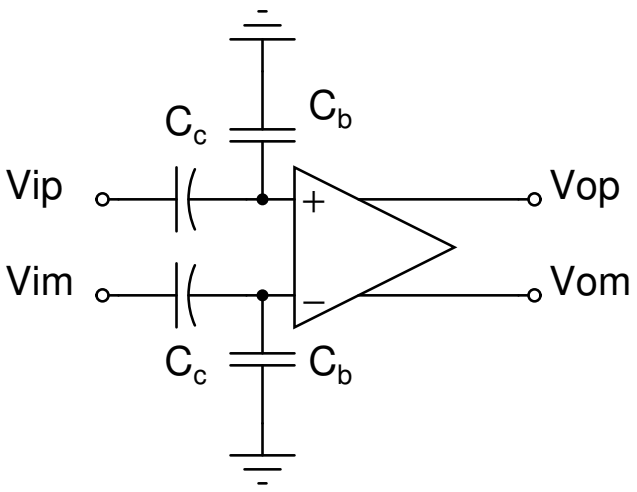


Figure 5.8: Bottom plate capacitor at the input of the preamp.

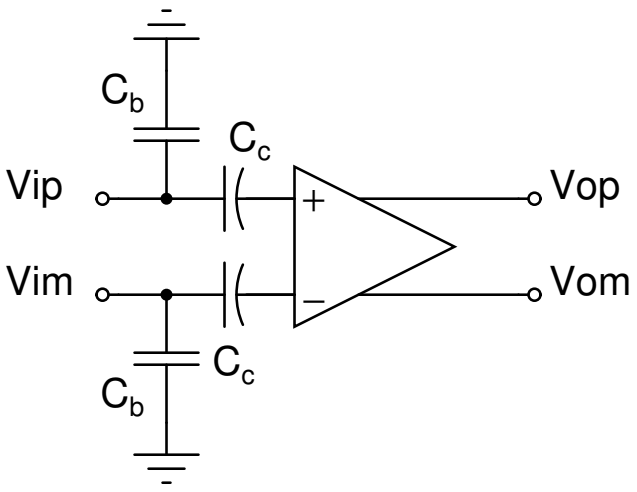


Figure 5.9: Bottom plate capacitor not at the input of preamp.

current in the track & hold circuit which drives these Cb's will have to be higher. So a value of Cc should be chosen such that the load on the track & hold is not increased significantly and the signal attenuation due to the parasitic capacitors of the preamp is negligible. The parasitic capacitance of the preamp is 5.6 fF. A value of 50 fF for Cc gave an attenuation of only 0.9. Hence a value of 50 fF was chosen for Cc.

### 5.3.2 Biasing

The preamplifier needs two bias voltages Vbias1 and Vbias2 as shown in Figure 5.4 for its operation. The voltage Vbias1 is generated using a circuit as shown in Figure 5.5. The simplest biasing arrangement one can think of to generate Vbias1 is to pass current through a diode connected transistor. This voltage when used to bias the preamplifier will not result in the same current due to finite output impedance of the transistor. The next best thing to do is to use the gate voltage of the transistor M5 in Figure 5.5. Here the Vds of M5 will be same as that of the tail transistor M1 of the preamp. So if the preamp tail transistor(M1 in Figure 5.4) gate is connected to the gate of M5 in Figure 5.5 the mirroring will be precise. But in an IC we know it is better to transfer a bias current rather than a bias voltage. It is accomplished using the transistors M6,M7,M10 and M11 in Figure 5.5. The transistor M12 is realized as parallel combination of two identical sized transistors. These two transistors are placed at far ends of the comparator array so that current errors due to transistor mismatch are minimized.

The bias voltage Vbias2 is generated using an arrangement as shown in Figure 5.6. The Vbias2 should be such that the transistors M4,M5,M6 and M7 in Figure 5.4 should be in saturation. The voltage Vbias2 should be below Vdd by Vdsat of M6(or M7) and Vgs of M4(or M5). If Vbias2 is equal to this value then the top PMOS transistors of the preamplifier (M6 and M7) will be in the edge of saturation region. To ensure that the top PMOS transistors are well within saturation region Vbias2 should be lower than this value. This is ensured by choosing the size of the transistor M3 in Figure 5.6 to be less than that of M4 (or M5) of Figure 5.4.

Table 5.1: The DC operating conditions of the transistors in the preamp.

| Transistor | Vdsat (in mV) | Vds (in mV) | gm (in $\mu$S) | gds (in $\mu$S) |
|---|---|---|---|---|
| M1 | 160 | 880 | 222 | 2.7 |
| M2 (or M3) | 127 | 929 | 155 | 2.1 |
| M4 (or M5) | 260 | 766 | 92.8 | 3.1 |
| M6 (or M7) | 618 | 725 | 31.6 | 1.4 |

The common mode voltage is generated using the circuit shown in Figure 5.7. The transistor M3 is made to have the same current density as the top most PMOS transistors of the preamp which are used for providing the common mode feedback. The Vgs drop of M3 from Vdd will give us the output common mode of the preamp which is same as the input common mode. This voltage is used in the precision biasing circuit as the gate voltage of M4 in Figure 5.5. The gate overdrives and margins of Vds over Vdsat for various transistors are tabulated in Table 5.1.

### 5.3.3 Dynamic Gain

The preamp is given only a finite amount of time for amplifying the input signal. The gain that can be achieved in this finite time is called dynamic gain. In our case the preamp amplifies only when PRST signal is low. To find the dynamic gain of the preamp the following procedure is adopted. Firstly the preamp is autozeroed for 20 ns so that the capacitors are charged to appropriate references. Then the preamp is disconnected from the references and excited with a differential voltage. The ratio of the output voltage to the input voltage at the end of amplify phase of the preamp gives us the dynamic gain. The differential input to the preamp and its output are as shown in Figure 5.10. One can notice that the preamp output is zero when PRST signal is high and it amplifies the input signal when PRST signal is low. In amplify phase the output reaches a value of 68 mV for an input of 10 mV.

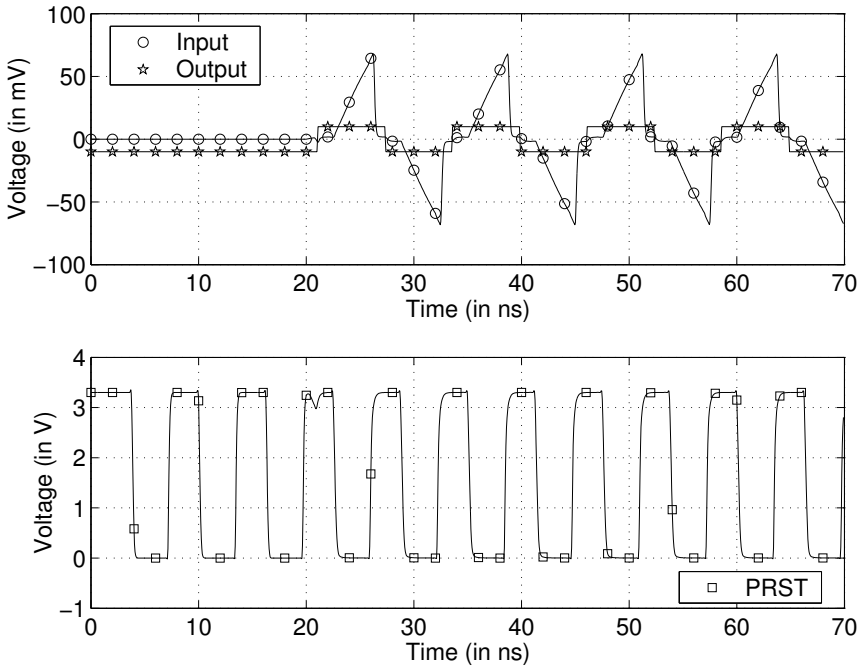


Figure 5.10: Differential output of the preamp for a differential input and the preamp reset signal.

Hence the dynamic gain of the preamp is $\frac{68}{10} = 6.8$.

### 5.3.4 DC Gain

We have seen earlier that the input referred offset of the preamp gets divided by its DC gain due to autozero operation. To find the DC gain, consider the small signal equivalent picture of the preamp when excited with a differential signal as shown in Figure 5.11. Here only the half circuit is considered for analysis since for any differential circuit it is enough to analyze only the half circuit for finding the gain. The drain of M6 is grounded in small signal picture because this node falls on the axis of symmetry and any node that falls on axis of symmetry in a fully differential circuit can be considered a ground for small signal analysis. The gain now is that of a common source stage with an active load, which is $\frac{g_{m2}}{g_{d2}+g_{d4}}$. For the typical mean corner this value is $\frac{155}{2.1+3.1} = 29.8$.

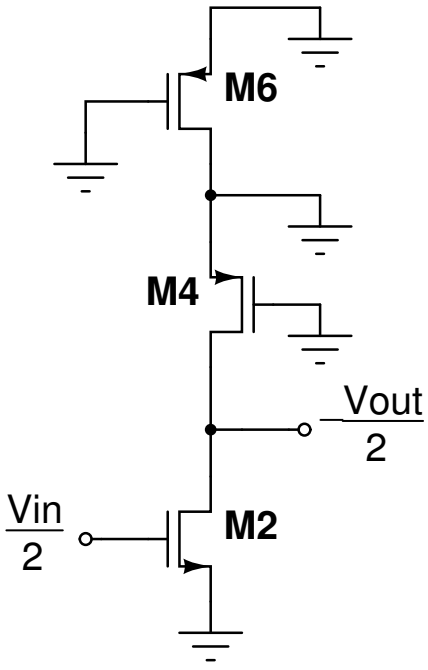


Figure 5.11: Small signal picture of the preamp for finding the DC gain.

### 5.3.5 Common Mode Loop Stability

The preamplifier is a fully differential amplifier and hence needs a common mode feedback loop to fix the output common mode voltage. This is done by the transistors M6 and M7 in Figure 5.4. Let us try to find out the common mode loop transfer function. It is enough to consider one half of the circuit for this analysis. To find the loop gain let us break the common mode loop as indicated in Figure 5.12. The transfer function from node A to node B is given by $-\frac{g_{m6}}{sC_c}$, assuming the output impedances of the transistors to be infinite. The closed loop transfer function is given by $\frac{-\frac{g_{m6}}{sC_c}}{1+\frac{g_{m6}}{sC_c}} = -\frac{1}{1+\frac{sC_c}{g_{m6}}}$. The common mode loop behaves like a first order system with a time constant of $\frac{g_{m6}}{C_c}$. The test bench for studying the dynamics of the common mode loop is as shown in Figure 5.13. The inputs of the preamp are connected to the common mode voltage. The outputs of the preamp are shorted and this node is excited by a current source. For a current step of 0.1 $\mu$A which occurs at 10 ns, the response is as shown in Figure 5.14. It can be noticed from the plot that

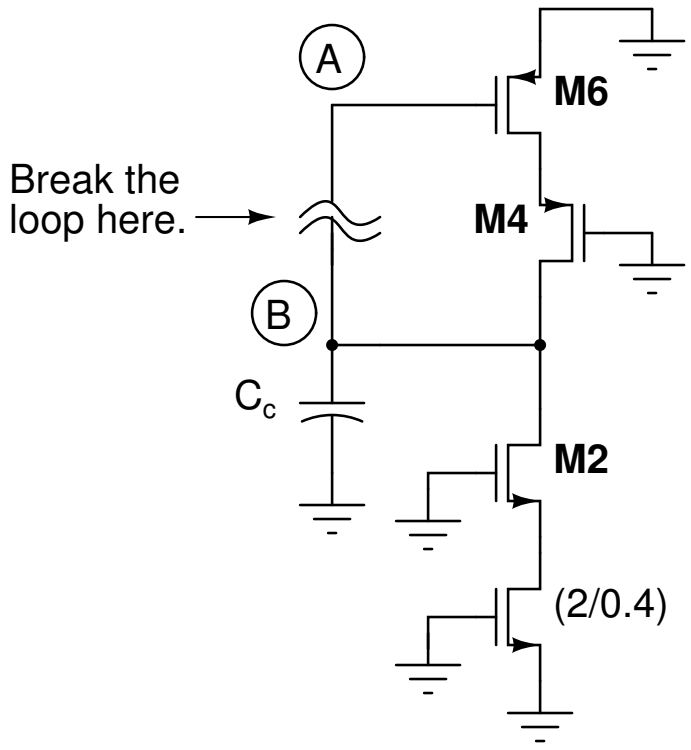


Figure 5.12: Small signal picture of the preamp half circuit for analyzing common mode loop.

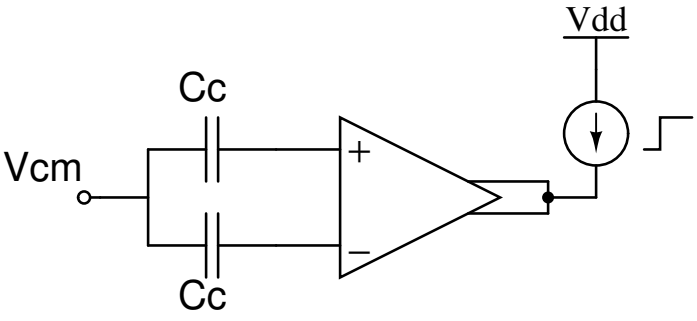


Figure 5.13: Test bench for testing the common mode loop.

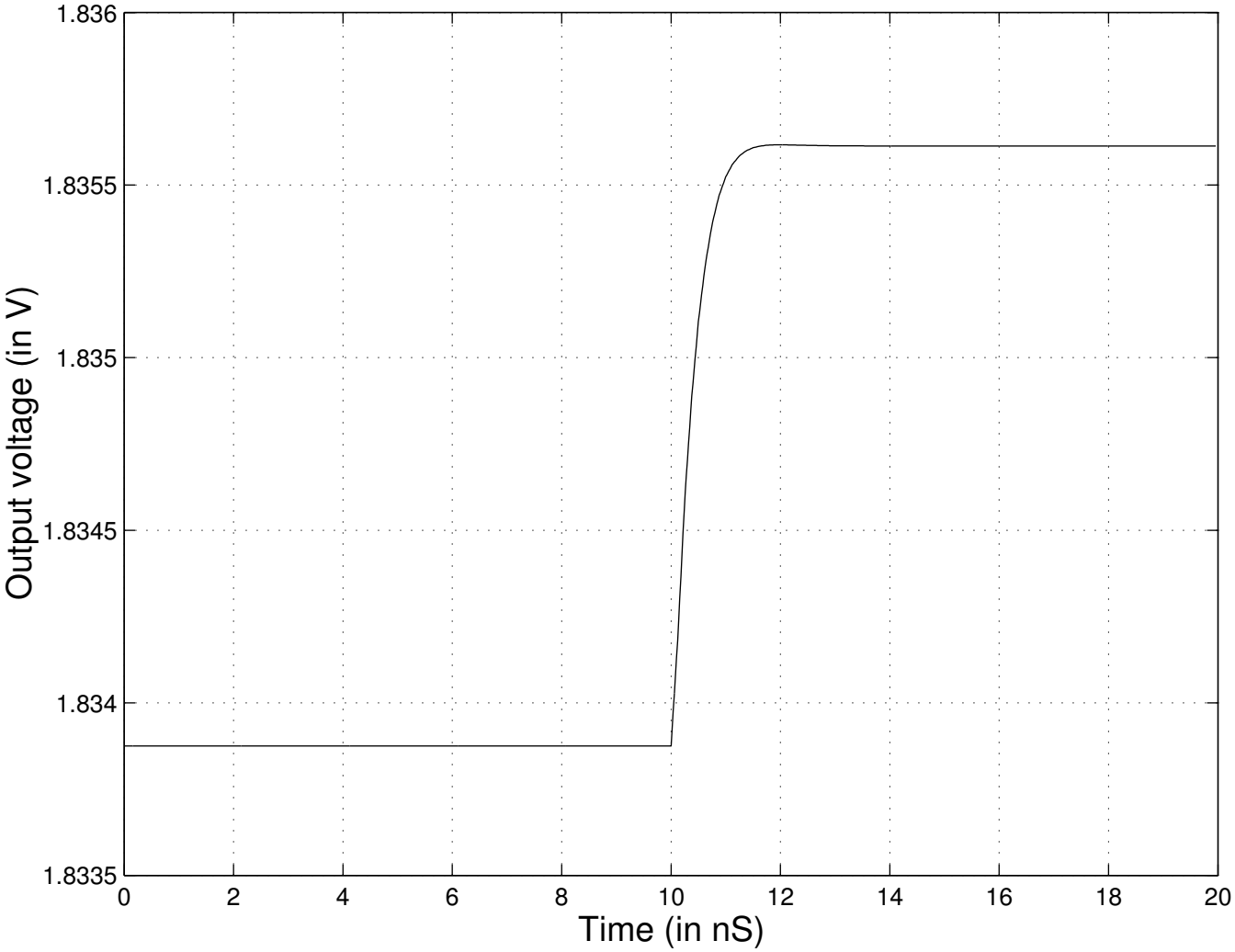


Figure 5.14: Response of the common mode loop to current step.

the output settles in 2 ns. The time constant for the common mode loop was found out to be $\frac{C_c}{g_{m6}}$ in our common mode loop analysis. This value is $\frac{45.8 \text{ fF}}{31.6\ \mu\text{S}}$ =1.45 ns in typical process corner.

### 5.4 LATCH

The schematic of the latch is as shown in Figure 5.17. This latch is essentially a back to back connected inverter. The regenerative action of the latch can be made active by closing switches M1 and M6. When the latch is connected to preamp it is disconnected from supply and ground using the transistors M1 and M6. After the

end of preamplifier gain phase M1 and M6 are switched on so that the latch starts regenerating and at the end of regeneration period the outputs are processed by digital logic to give the corresponding digital output bits. At this point of time one of the outputs of the latch will be at Vdd and the other will be at ground potential. To facilitate the decision in the next clock cycle this memory of the latch is erased by switching on M7 for a short period of time so that the differential voltage is made zero.

The outputs of the latch along with the various clocks which are used in operating the latch are as shown in Figure 5.15. When LC is high the preamp charges the parasitic capacitors at the input of the latch to an amplified version of its input. During this period LE is made low so that the latch does not load the preamp. After LC is made low LE is made high. The moment LE is made high the latch starts regenerating the input and we get a valid digital output at the end of regeneration period. After LE is made low the latch is reset using the LRST signal. The LRST has an overlap period with the LC clock. This is done so that the latch inputs are reset to the output common mode voltage of the preamp. The outputs of the latch go to Vdd and ground alternately. This is the desired output since the stimulus given to the comparator for this simulation was such that the differential input was above the reference in alternate clock cycles. Figure 5.16 is a zoomed in version of the Figure 5.15 from 35 ns to 43 ns. The regenerative time constant for the latch was 125 pS in typical corner of the process. The latch was giving a valid decision (which can be used by digital circuits that follow) in 600 pS. The output of the latch is given to a precharge and evaluate type of inverter which is as shown in Figure 5.18. The output of this inverter is high when inv_clk is low and the moment inv_clk goes

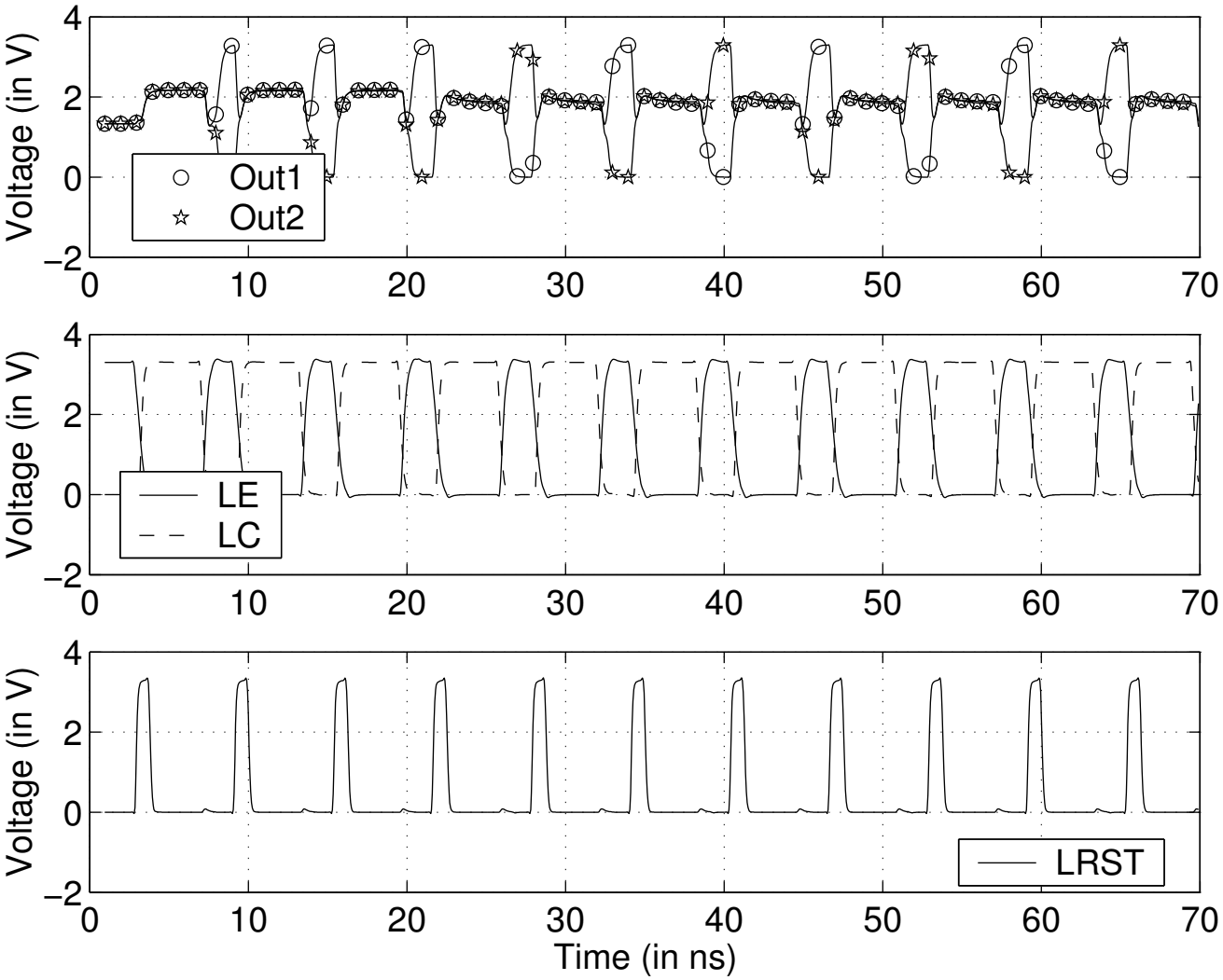


Figure 5.15: Various clocks to the latch and its output.

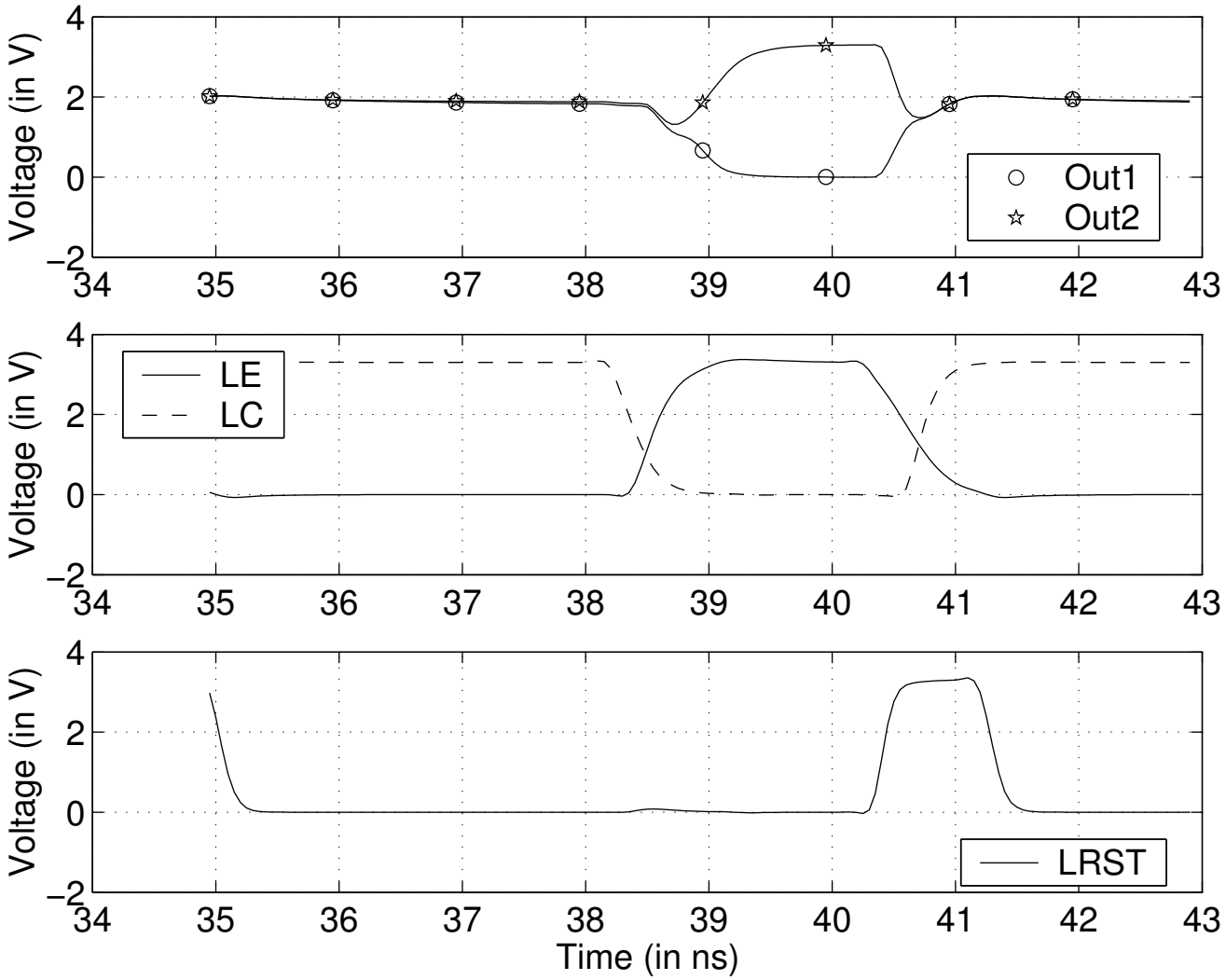


Figure 5.16: Various clocks to the latch and its output.

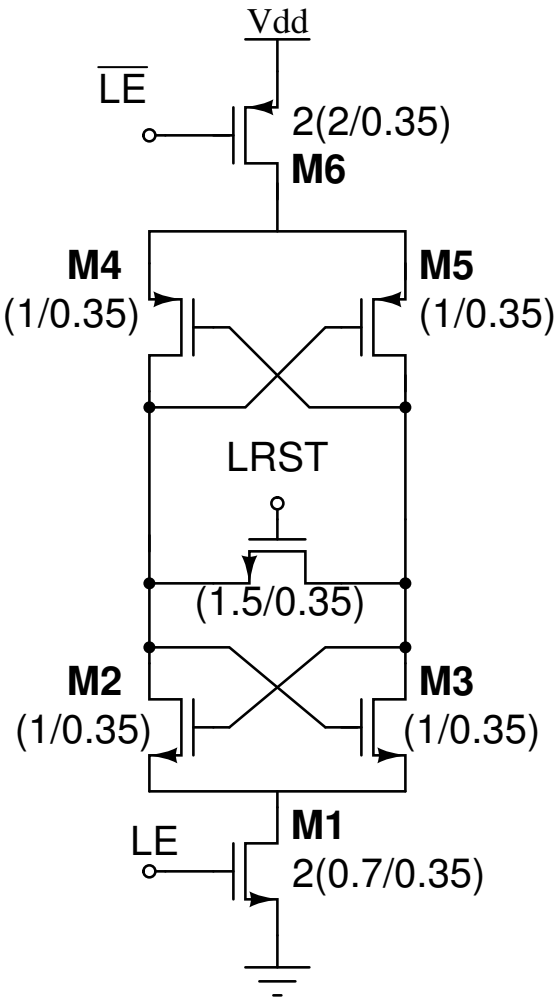


Figure 5.17: Schematic of the latch.

high the output is evaluated to low or high depending on the input. The inv_clk was delayed from LE by 0.8 ns.

## 5.5 OFFSET CALCULATIONS

The preamp and latch will have input referred offsets $V_{offpreamp}$ and $V_{offlatch}$ respectively because of the device mismatches. The overall input referred offset of the comparator is given by

$$V_{off} = \sqrt{\left(\frac{V_{offpreamp}}{1 + A_{pre}}\right)^2 + \left(\frac{V_{offlatch}}{A_{dy}}\right)^2} \tag{5.7}$$

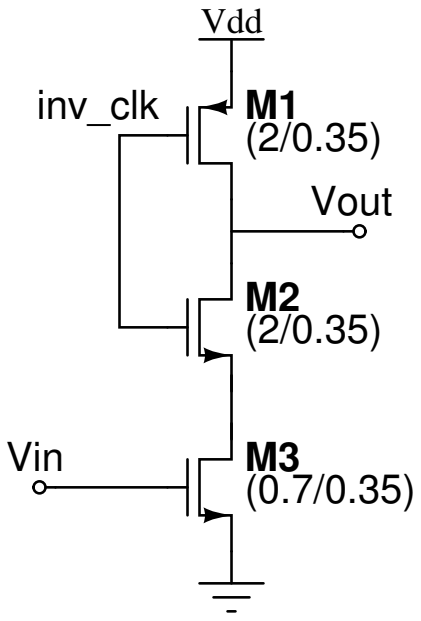


Figure 5.18: Schematic of precharge and evaluate type of inverter.

The preamp offset $V_{offpreamp}$ is given by

$$V_{offpreamp} = \sqrt{{V_{offnmos}}^2 + \left(\frac{g_{mp}}{g_{mn}}\right)^2 {V_{offpmos}}^2} \tag{5.8}$$

where $V_{offnmos}$ is the mismatch between the input pair transistors M2 and M3 and $V_{offpmos}$ is the mismatch between the load transistors M4 and M5 of Figure 5.4. The offset in $V_T$ between two transistors of width $W$ and length $L$ is given by [8], $V_{off} = \frac{A_{V_T}}{\sqrt{WL}}$, neglecting the spatial component. $A_{V_T}$ is a technology dependent parameter. The values of this parameter, $A_{V_T}$ for NMOS and the PMOS transistors in the technology in which the ADC is realized are 8.2 mV$\mu$m and 14.9 mV$\mu$m respectively. So we have, $V_{offnmos} = \frac{A_{V_{TNMOS}}}{WL} = \frac{8.2}{4\times0.4} = 6.5$ mV and

$V_{offpmos} = \frac{A_{V_{TPMOS}}}{WL} = \frac{14.9}{4\times0.4} = 11.8$ mV.

$\Rightarrow V_{offpreamp} = \sqrt{(6.5)^2 + (\frac{92}{155})^2(11.8)^2} = 9.5$ mV.

On similar lines we can find the offset of latch and it is given by

$V_{offlatch} = \sqrt{(13.9)^2 + (\frac{92}{155})^2(25.2)^2} = 20.4$ mV.

The offset of comparator is given by $\sqrt{(\frac{9.5}{1+30})^2 + (\frac{20.4}{6.8})^2} = 3$ mV. The "3-sigma"

value of the offset is 9 mV and this is less than the $\frac{LSB}{4}$ of the converter which is 10 mV.

# CHAPTER 6

# CLOCK GENERATOR DESIGN

## 6.1 CLOCK GENERATION TECHNIQUES

The ADC needs various clocks for each block for its functioning. These clocks should be aligned properly for the correct functioning of the ADC when all the blocks are interconnected. The two important things that one needs to be able to do for realizing the clocks are

- Changing the duty ratio.
- Generating non overlapping clocks.

### 6.1.1 Changing Duty Ratio

The duty ratio of a clock can be either decreased or increased using a n-starved inverter or a p-starved inverter respectively. The schematic of a n-starved inverter is shown in Figure 6.1. In this type of inverter the discharging current is limited by the transistor M3 as shown in Figure 6.1. This will make the fall times slower. This when passed through a normal CMOS inverter would give sharper rise and fall times. Using a cascade of n-starved inverter and a normal inverter the on time period of the clock can be decreased and the duty ratio can be made less than half. The schematic of a p-starved inverter is shown in Figure 6.2. In this type of inverter the charging current is limited by the transistor M1 as shown in

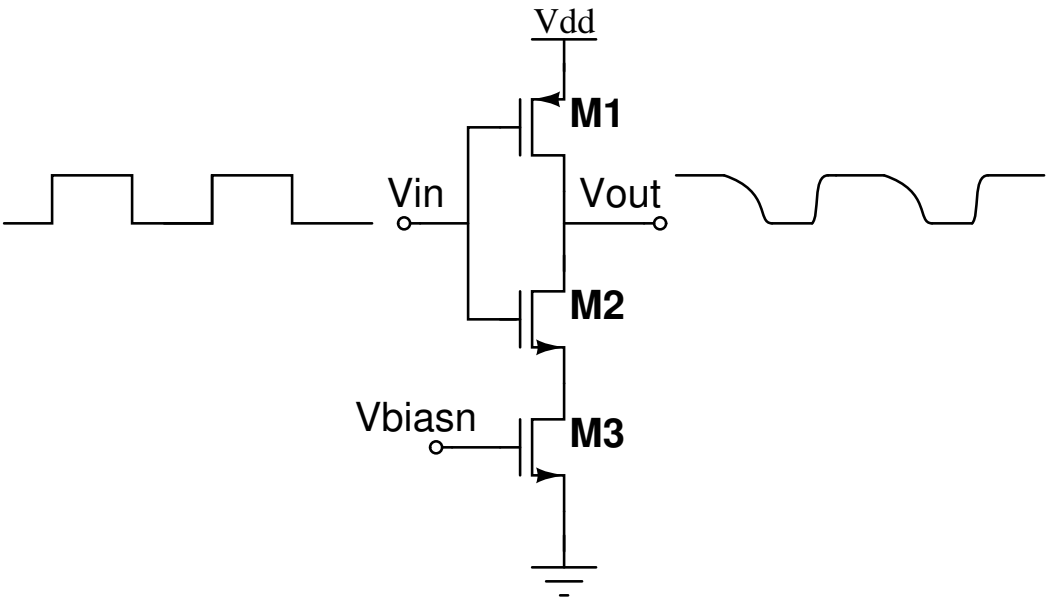


Figure 6.1: Schematic of n-starved inverter.

Figure 6.2. This will make the rise times slower. This when passed through a normal CMOS inverter would give sharper rise and fall times. Using a cascade of p-starved inverter and a normal inverter the on time period of the clock can be increased and the duty ratio will be more than half. In an inverter where both the

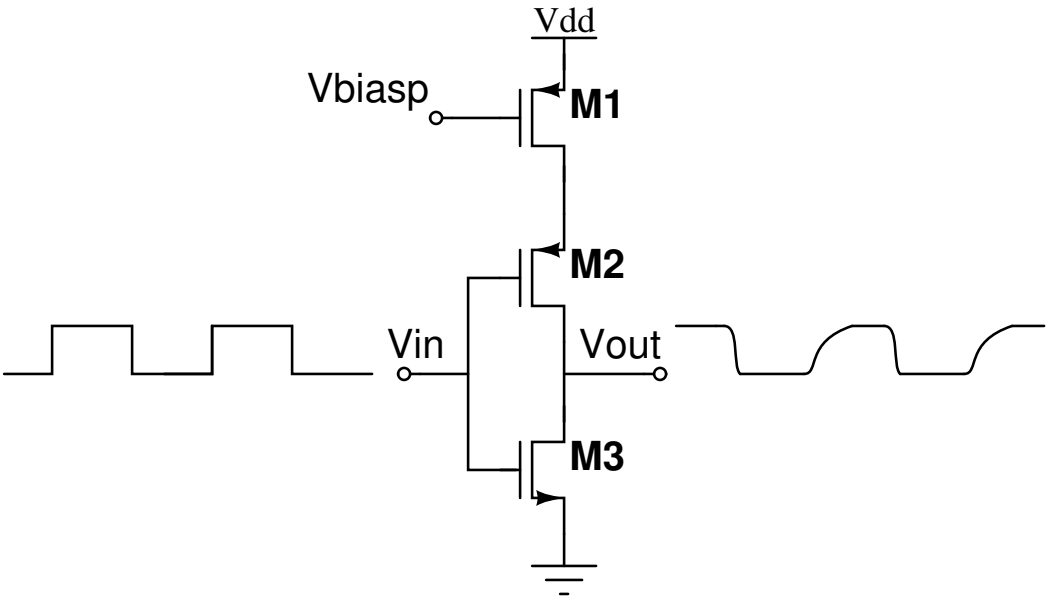


Figure 6.2: Schematic of p-starved inverter.

charging and discharging currents are limited as shown in Figure 6.3 both the rise

time and fall times at the output will be slower. When this is used in cascade with a normal CMOS inverter, a delay element is realized.

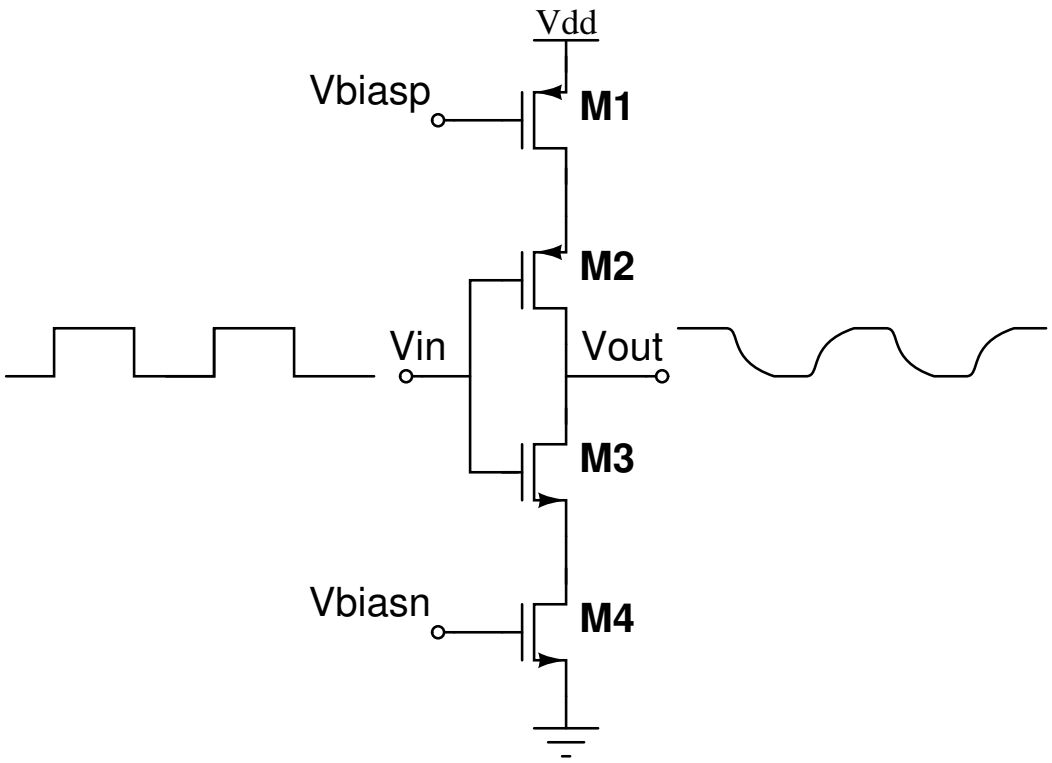


Figure 6.3: Schematic of starved inverter.

### 6.1.2 Generating non overlapping clocks

The schematic for generating non-overlapping clocks is as shown in Figure 6.4. $T_{inv}$ is the delay of the inverter whose output is $\overline{CLK}$. The delay element $T_d$ shown in Figure 6.4 can be realized using a chain of inverters. Let us assume that the NOR gate does not introduce any delay. Even if the NOR gate introduces delay one can think the delay of the NOR gate to be absorbed into the delay element. Initially let us assume that the signal CLKA is high and CLKB is low. This choice is only to make the analysis simple. If one starts from any other initial condition for CLKA and CLKB the results will not differ. When CLK goes high, CLKA goes low after a delay of $T_d$. After a delay of $T_d$ from the falling edge of CLKA, CLKB goes high. It remains high till the $\overline{CLK}$ is low. The moment $\overline{CLK}$ goes high, CLKB goes low

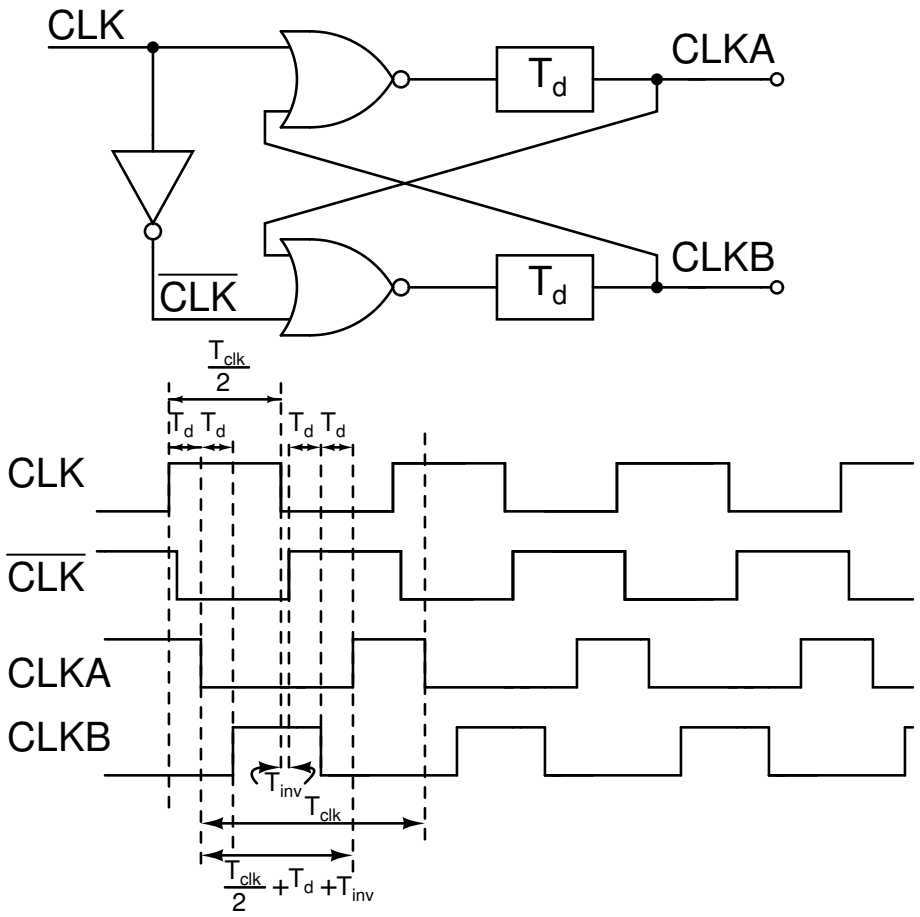


Figure 6.4: Generating non-overlapping clocks.

after a delay of $T_d$. Now the signal CLKA which was low goes high after a delay of $T_d$ from the falling edge of CLKB. Now the situation is identical to the state from which we started our analysis. So the process repeats itself. The important thing to note is the non overlap period $T_d$, between the two clocks CLKA and CLKB. If the NOR gates in Figure 6.4 are replaced by NAND gates we will get clocks with an overlap period of $T_d$. When these overlapping clocks are inverted we will get clocks with a non overlapping period of $T_d$. If only NAND gates are to be used then this scheme can be employed.

## 6.2 CLOCK GENERATION CIRCUIT

Using a combination of the starved inverters and the non-overlapping clock generation circuit the clocks needed by the ADC are generated. Initially we should be able to generate a clock waveform which goes all the way from ground to Vdd. This is necessary because the signal sources available at frequencies of hundreds of MHz give out a sinusoidal signal around a common mode of zero voltage. From this signal we should be able to generate square wave of same frequency. This is achieved by the circuit shown in Figure 6.5. The signal from the external source, EXT_CLK is AC coupled to an inverter using an off chip 10 nF capacitor. This in-

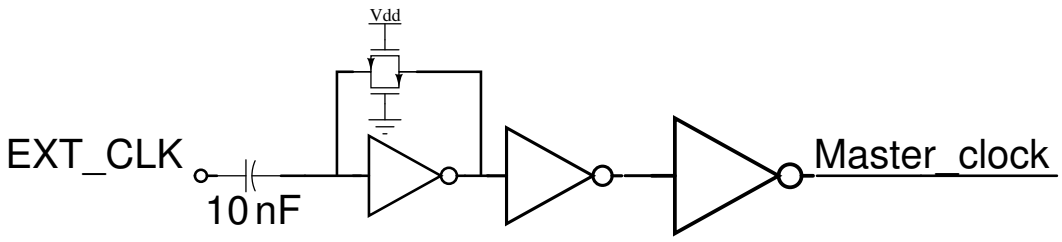


Figure 6.5: Generating a rail to rail clock waveform from a sinusoidal signal of small amplitude.

verter is biased at its natural common mode by connecting its output and input using a transmission gate which acts as a resistor. Following this inverter there are two inverters with increasing size so that the final output, Master_clock is a square wave of sharp rise and fall times. The schematic of the clock generator is as shown in Figure 6.6 which uses Master_clock as its input. The starved inverter used in this schematic is designed such that when it is used in cascade with a CMOS inverter the combination gives a delay of 0.8 ns. The p-starved inverter was designed such that when it was used in cascade with a CMOS inverter the on-time period of the clock increased by 0.8 ns. In case of the n-starved inverter the on-time period decreased by 0.8 ns. We will now look at how the various clocks need to be aligned.

When the signal is held by the track & hold circuit the preamplifier should be amplifying and the latch should be disabled. This means when 'phi' is high, RST (the preamplifier reset signal) should be low and LC (this controls the switch connecting preamp and latch) should be high. LE (the latch enable signal) should be low during this period. In the track mode of the track & hold circuit 'phi_bar' is high. The preamplifier is to be reset in this period. LE should be made high so that a decision is made by the latch. After the end of regeneration period 'INV_CLK' should be made high so that the decision is passed on to the majority logic that follows. The encoder which is a precharge and evaluate type of encoder is clocked by the signal 'ROM_CLK'. This signal is derived from 'INV_CLK' by delaying it. The output of the encoder is latched using D flip flops which are clocked by the signal 'DFF_CLK'. This is a delayed version of 'ROM_CLK'. These clocks have to drive the load constituted by the switches of the 63 comparators and the interconnects. This is achieved by the clock buffer circuit shown in Figure 6.7. The increasing size of the inverters in Figure 6.7 indicate the increasing driving strengths which is achieved by increasing the sizes of the transistors in the inverter.

### 6.3 SIMULATION RESULTS

The clock waveforms are shown in Figure 6.8 for an input clock frequency of 160 MHz at $70^0$C. In these simulations the clocks were loaded with the comparator load and the interconnects load. When 'phi' is high, the input is held by track & hold circuit. During this time one can observe that 'RST', which is the reset signal for the preamp, is low (refer Figure 6.8) so that the preamp is in amplify mode. The moment LC goes low and RST goes high LE becomes high so that latch is enabled. INV_CLK's rising edge is delayed from that of LE so that the decision is

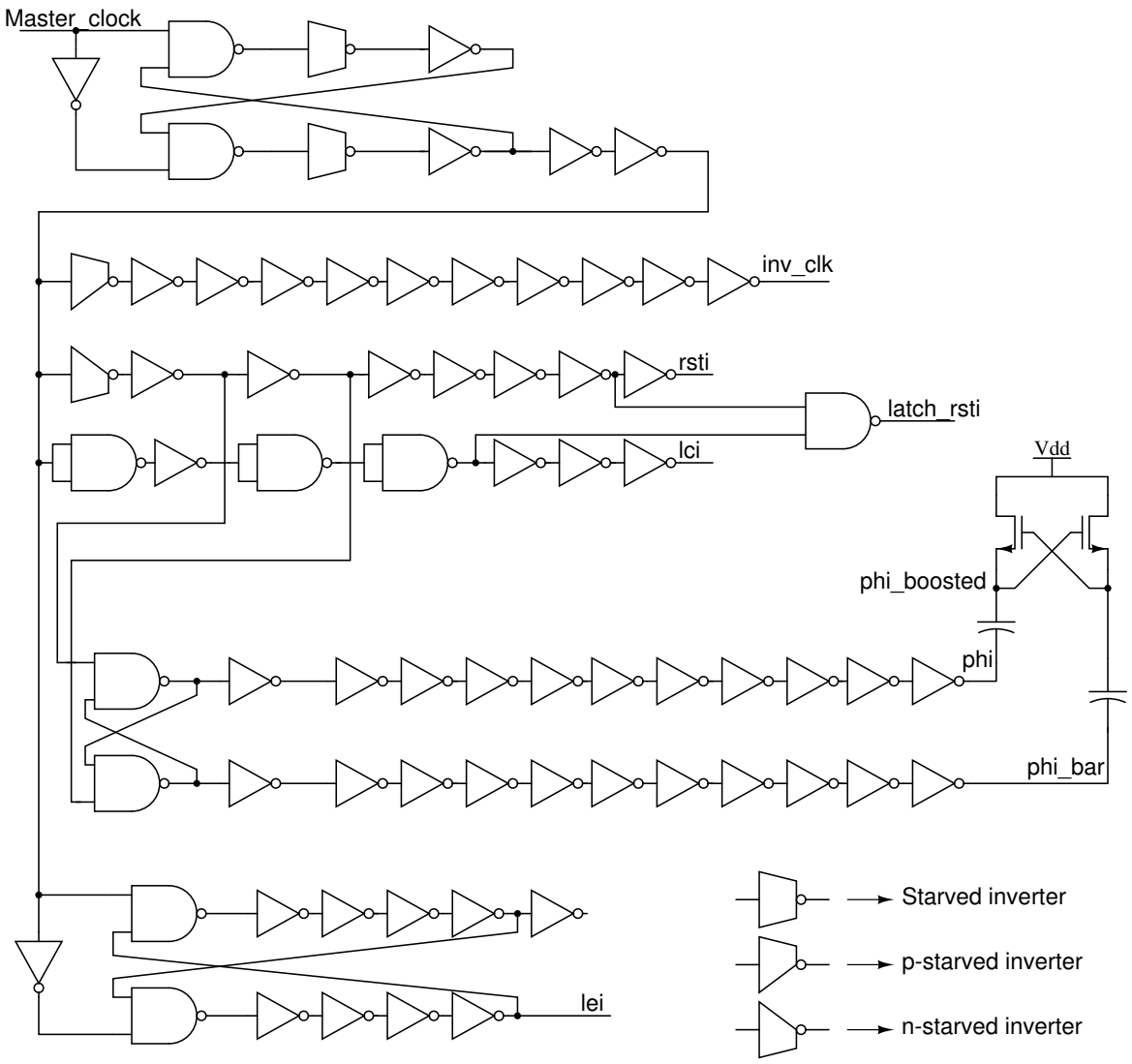


Figure 6.6: The clock generation block.

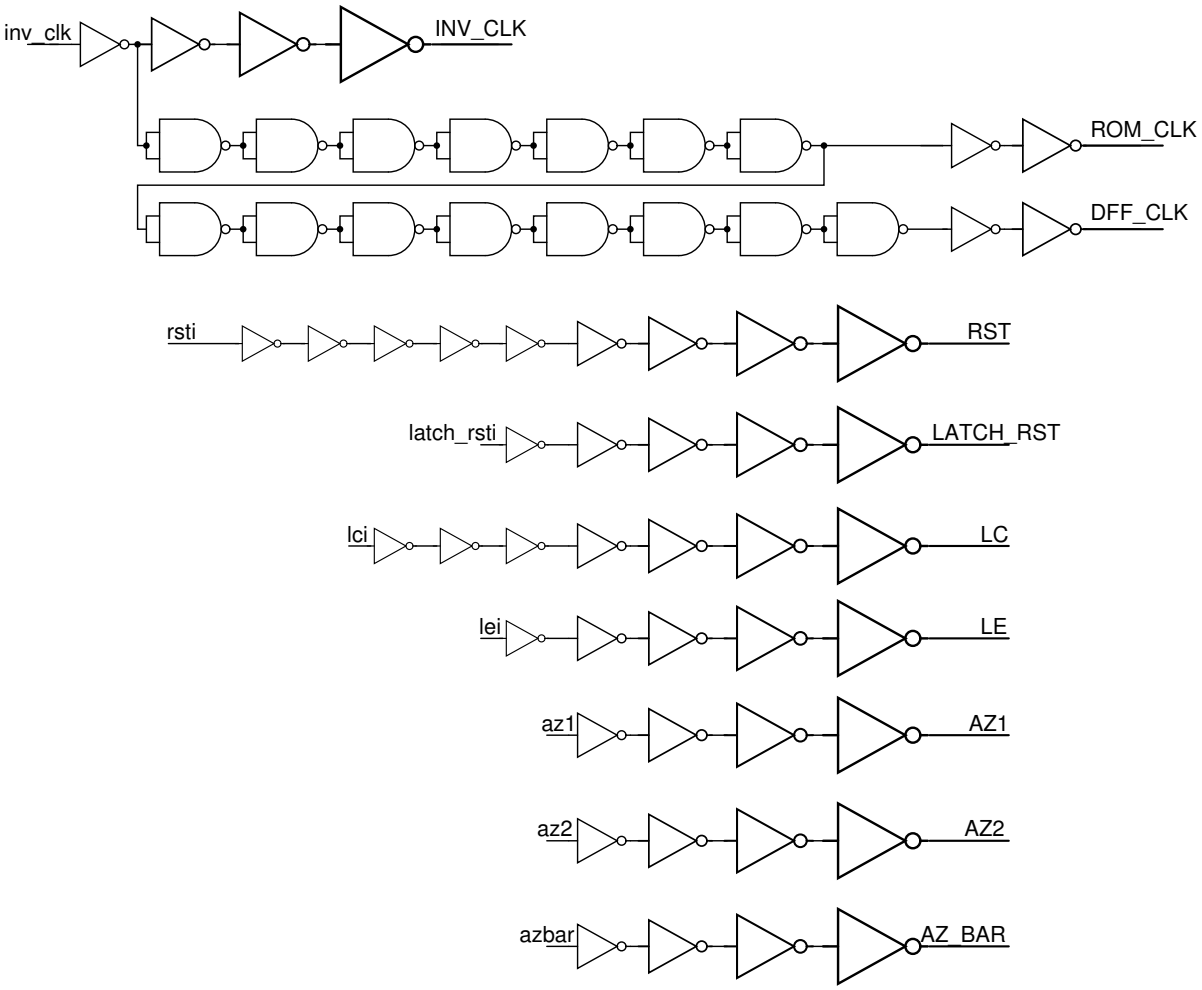


Figure 6.7: Clock buffers and additional clocks generated.

captured by the digital logic at the end of regeneration period of the latch. The clocks ROM_CLK and DFF_CLK are a delayed versions of INV_CLK.

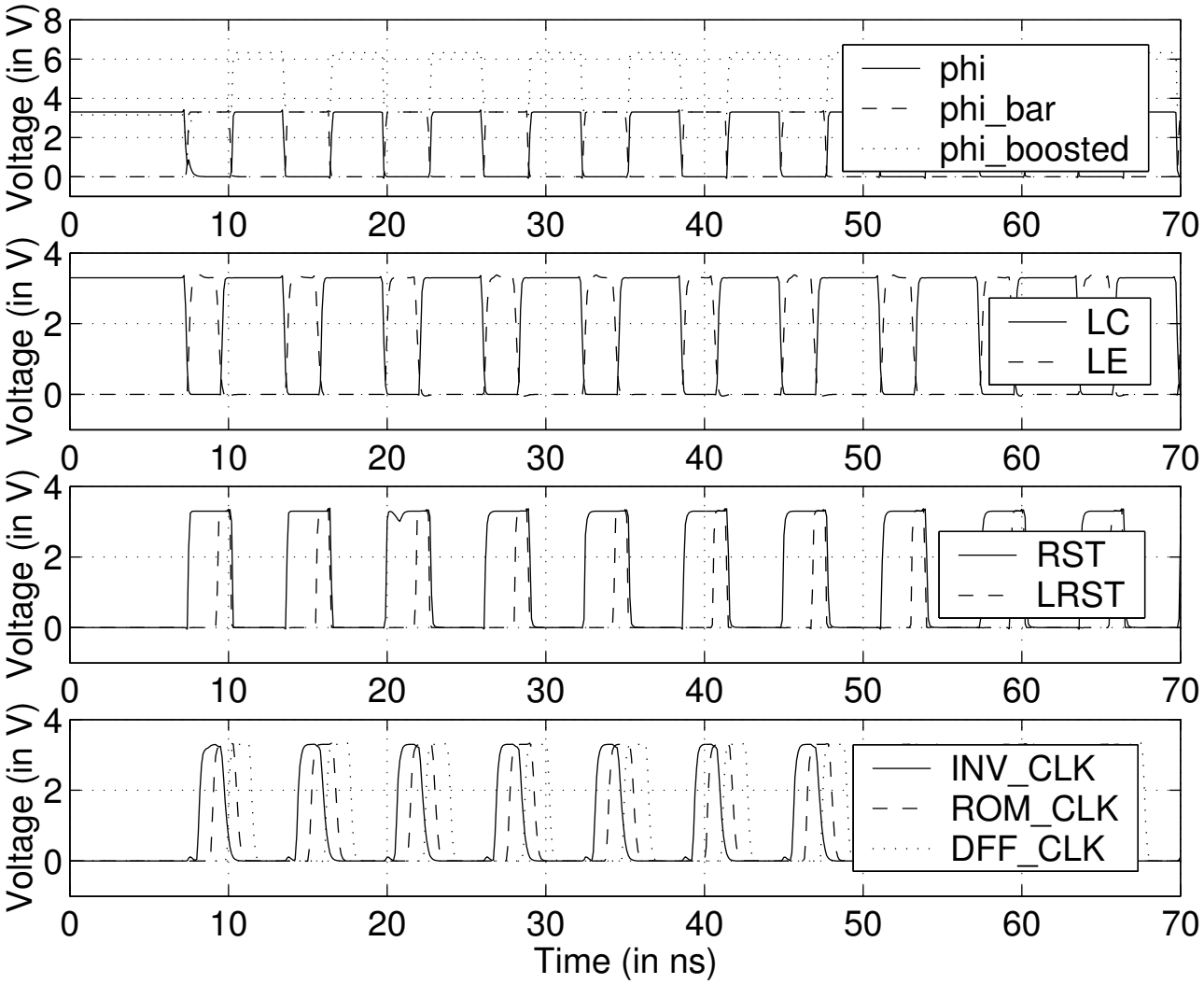


Figure 6.8: The various clock signals generated.

# CHAPTER 7

# SURVEY OF EXISTING BACKGROUND OFFSET CORRECTION SCHEMES

## 7.1 NEED FOR BACKGROUND AUTOZERO

When a comparator is autozeroed it is unavailable for conversion. In some applications the ADC has an idle time where all the comparators can be autozeroed [9] without degrading the overall performance of the system. But in applications where continuous functioning of the ADC is demanded autozero has to be done in every clock cycle or it has to be done in background. Autozeroing of the comparator in every conversion cycle of the ADC will reduce the time available for preamp and latch[10]. With increasing frequency having a dedicated time slot for autozero in every clock cycle is not desirable. In previous works this problem was addressed using background autozero [6], background interpolated autozeroing [11] and interleaved autozeroing [2][12][13]. In all these schemes the autozeroing of comparators takes place in the background without affecting the normal conversion cycle of the converter. We will look at each autozeroing scheme in certain detail in the next few sections and highlight the disadvantages of each scheme.

## 7.2 BACKGROUND AUTOZERO AS REPORTED IN [6]

The background autozero scheme, as suggested in [6], requires five extra comparators which constitute an auxiliary comparator array as shown in Figure 7.1. The second stage preamps shown in Figure 7.1 are used for interpolation. The autozeroing scheme is as follows. During autozeroing of a comparator the auxiliary comparator array needs to replace five comparators from the main array. This is so because when a second stage interpolating preamp is to be autozeroed the two first stage preamps connected to it have to be connected to the reference ladder. This in turn disables the other four second stage preamps. So the auxiliary comparator array has to replace five comparators. During autozero period the outputs of the comparators above 'k+4' are downward shifted by 5 and given to the encoder. The digital output is obtained by adding the digital outputs from the encoder of main comparator array and the auxiliary comparator array. This gives the correct digital output the reasoning for which is as follows. When the input is below 'k' the main comparator array gives correct binary code and the auxiliary comparator array gives an output of zero. Addition of these two will result in correct digital output. When the input lies above 'k+4', the output of main comparator array will be shifted down by five and the output of the auxiliary comparator array will be five. The addition of these two will again result in correct digital output. When the input lies between 'k' and 'k+4' the main comparator output will be 'k' and the auxiliary comparator output will be input dependent and the addition of these two will give the correct digital output. The configuration of the converter during the second part of autozero cycle will be as shown in Figure 7.2. Note that here the

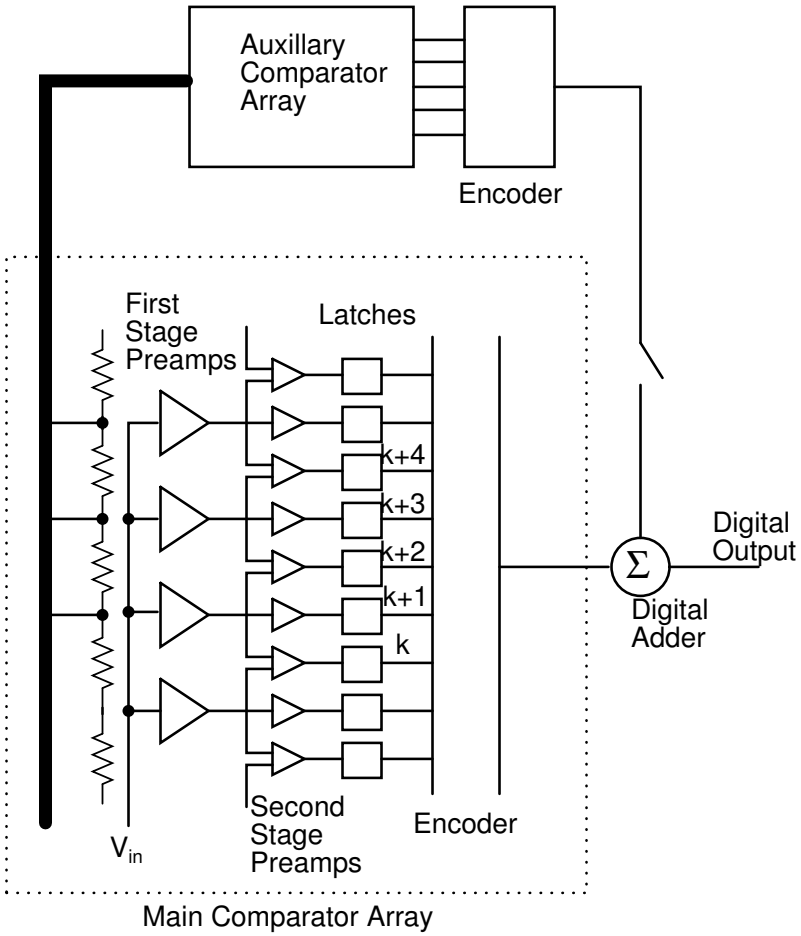


Figure 7.1: Configuration during the first part of an autozero cycle.

comparator outputs above 'k+4' are shifted down by 5 and given to the encoder. This requires extra wiring at the latch outputs.

The disadvantages of this scheme are as follows

- Five extra comparators are needed.
- The extra wiring at the latch outputs increases the parasitic capacitance at that node.
- A control circuit is needed to downward shift the comparator outputs in the second part of the autozero cycle.

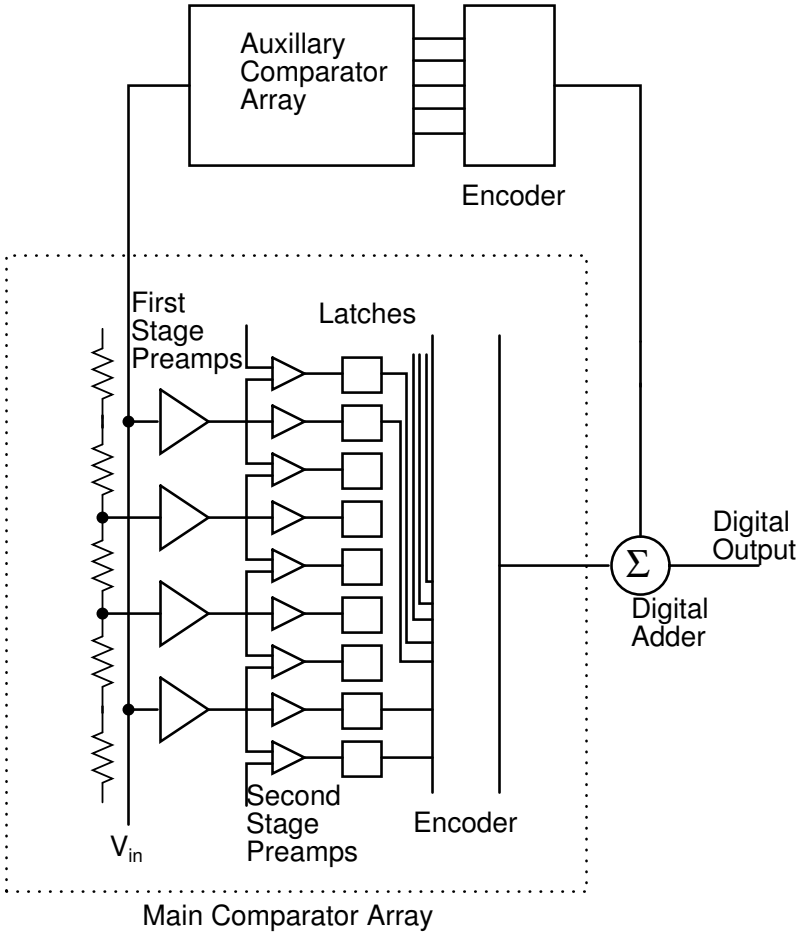


Figure 7.2: Configuration during the second part of an autozero cycle.

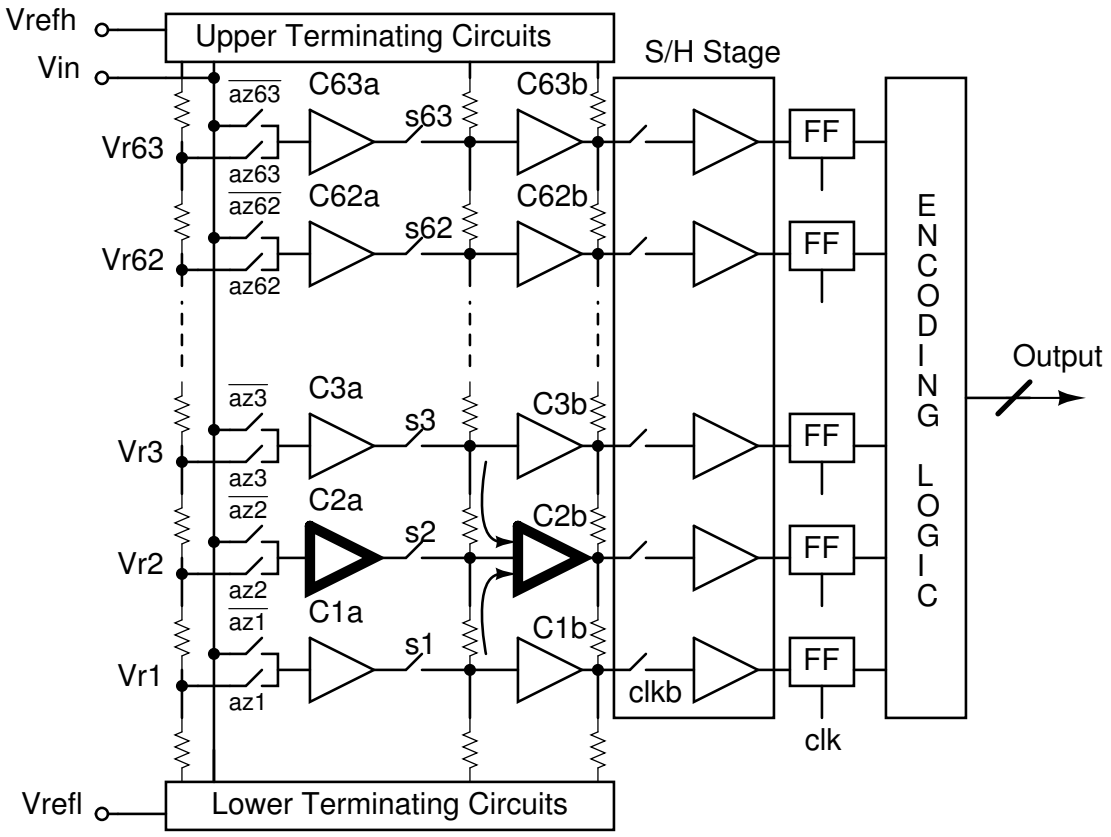


Figure 7.3: Background interpolated autozero.

### 7.3 BACKGROUND AUTOZERO AS REPORTED IN [11]

The ADC as reported in [11] has a comparator which has three stages as shown in Figure 7.3. When the first stage comparator of a comparator block is autozeroed, it is disconnected from the subsequent comparator stages. During this period the input to the second stage comparator which follows this is interpolated from neighboring first stage comparator outputs. For example when the comparator C2a shown in Figure 7.3 is to be autozeroed its output is disconnected from C2b. The input to C2b is obtained by interpolating the outputs of C3a and C1a. This way the conversion of the ADC takes place without getting interrupted by the autozero process. The timing diagram for the various switches is as shown in Figure 7.4. The autozero control signal starts from bottom and reaches the top. A shift register propagates the control signal upward. The trigger signal 'aztr' is period-

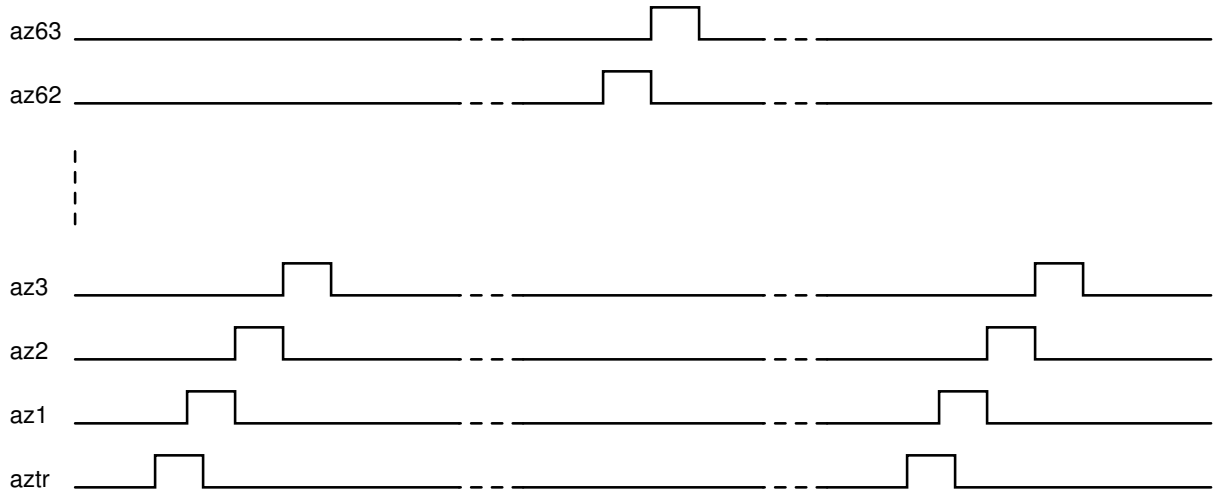


Figure 7.4: Background interpolated autozero timing diagram.

ically input into the lowest shift register after the previous signal has propagated to the last register thereby completing the autozeroing of all the comparators. The disadvantages of this scheme are as follows

- Any first stage comparator is redundant as the conversion takes place even when it is removed from the signal path for autozeroing.
- The interpolation technique used in a flash ADC is not used to its full advantage in this scheme.

## 7.4 BACKGROUND AUTOZERO AS REPORTED IN [2][12][13]

In [2][12][13] background autozero is carried out using a technique called interleaved autozeroing (IAZ). The block diagram of the ADC is as shown in Figure 7.5. It consists of 64 comparators to achieve continuous A/D conversion without an extra autozeroing period. In this scheme the comparators are autozeroed in turns while the other 63 comparators perform the conversion. The timing diagram for the IAZ is as shown in Figure 7.6. Initially, during $t_0$, all comparators C1-C64 are autozeroed before conversion with the voltages VRL-VR63. During the next pe-

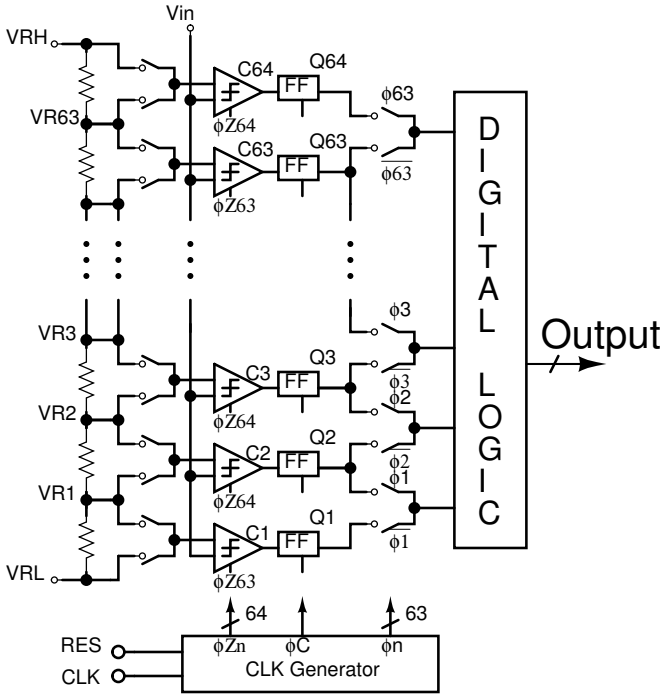


Figure 7.5: Background interleaved autozero.

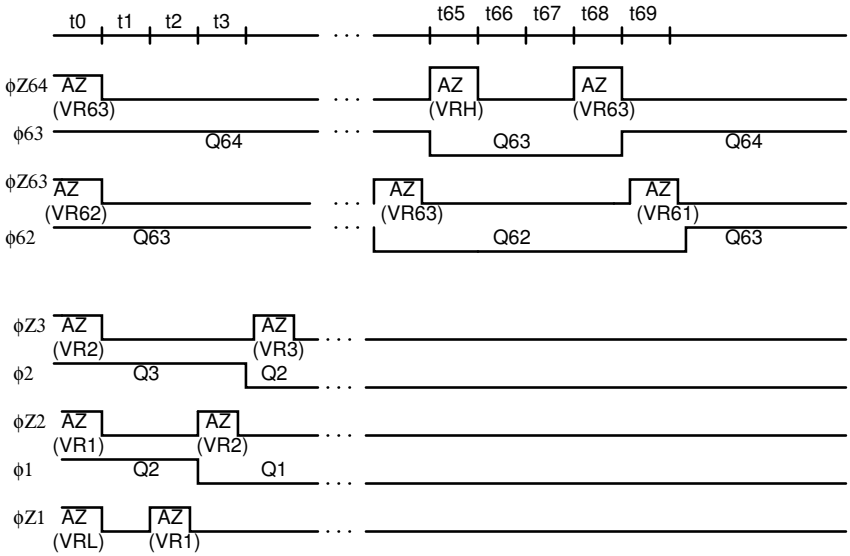


Figure 7.6: Background interleaved autozero timing.

riod $t_1$, the comparators C2-C64 are used in conversion. During $t_2$, C1 , which was autozeroed with VRL during $t_0$ is autozeroed to VR1 with the conversion still using C2-C64. During the next period $t_3$, C2, which was autozeroed with VR1 during $t_2$, is autozeroed with VR2 and the conversion uses C1 and C3-C64. After C64 is autozeroed with VRH, during $t_{65}$, the sequence is reversed and C64 is autozeroed with VR63 during $t_{68}$. This sequence is repeated to C1-VRL and then reverses at C1. This entire sequence repeats continuously during A/D conversion. When a comparator is being autozeroed its output is unselected by the 64-63 selector and the other comparator outputs are transmitted to the encoding block. The digital logic following the encoder gives out the digital output. The disadvantages of this scheme are as follows

- An extra comparator is required in the ADC.
- This scheme requires generation of complex waveforms for autozeroing the comparators.

## 7.5 BACKGROUND AUTOZERO IN THE PRESENT WORK

The background offset correction scheme which is employed in the flash ADC of this work does not require any extra comparators. No extra wiring is needed at the comparator outputs which would have otherwise increased the parasitic capacitance at that node. The control circuit for choosing the comparator that is to be autozeroed consists of a simple 6-bit counter and six input nand gates. The bubble-correction logic, which is a modular structure poses no layout problems. Since only one reference voltage is being accessed at a time, the ladder need not run along the comparator array. It can be designed so that all the resistors lie in

close proximity. This avoids any potential INL that could be introduced due to resistor gradients [14] across the integrated circuit. The background offset scheme used in this work is discussed in detail in the next chapter.

# CHAPTER 8

# REFERENCE GENERATOR DESIGN

## 8.1 DISTORTED OFFSET CORRECTION

In this work, offset correction (and reference storage) of the comparator preamps is performed in a background fashion. A comparator selector, which is basically a six bit counter, selects the comparator that needs to be autozeroed. Simultaneously, it also selects the appropriate predistorted reference required for that particular comparator. The background offset and distortion correction scheme is explained in detail in the next section.

## 8.2 BACKGROUND OFFSET & DISTORTION CORRECTION

A single-ended schematic of the reference generator is shown toward the top of Figure 8.1. It functions as follows - a 6-bit resistor ladder generates a set of linearly increasing references. The 6-bit counter output is used to select the comparator being autozeroed and the appropriate ladder tap. This "linear" reference is then predistorted by a track-and-hold circuit that is a replica of the one in the signal path. Thus, the reference levels stored in the comparators are distorted precisely by the same amount as the input signal. So, as elaborated in Chapter 2, distortion free operation will result. The biasing details of the ladder are shown in Figure 8.2. Vcm_in is chosen to be equal to the ADC input common-mode voltage, ensuring

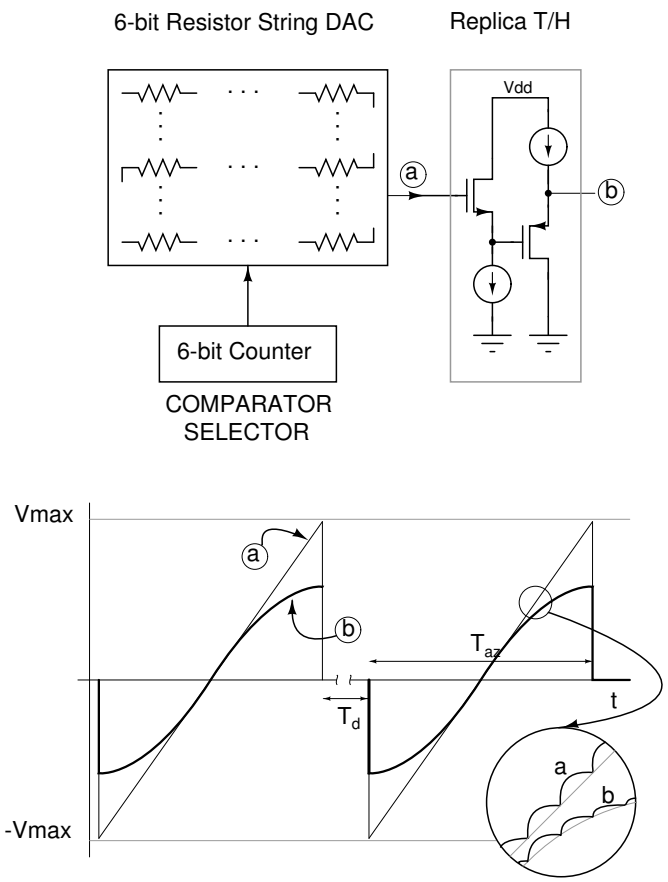


Figure 8.1: Nonlinear reference generator.

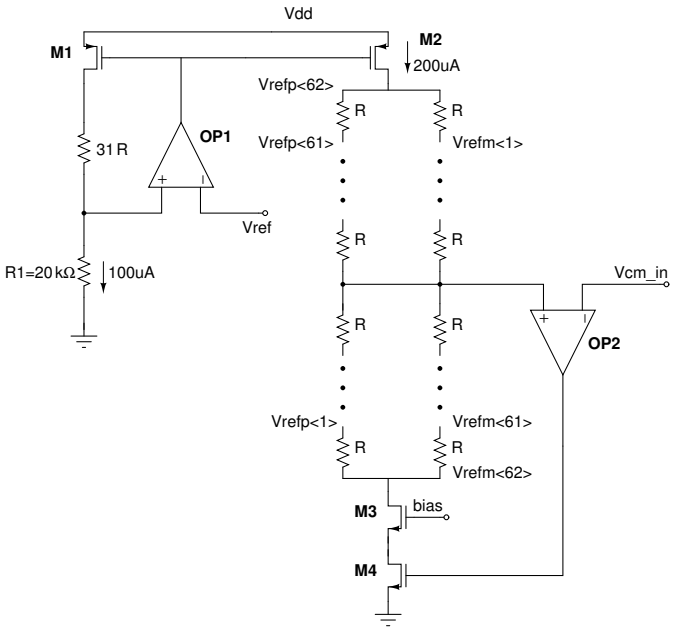


Figure 8.2: Linear reference generator.

that the common mode levels of the references and the input are identical at the preamp inputs. The current in the ladder ( and hence the LSB size) is controlled by Vref. The LSB size is of the form $\frac{Vref\ R_2}{R_1}$. Vref can be controlled externally so that the ADC characteristics can be studied for various full scale input ranges. The resistor ladder and predistorted reference outputs are shown in the lower part of Figure 8.1. The counter starts at one and keeps incrementing by one until it reaches 63. The corresponding ladder output is a linear staircase waveform shown as the ramp. The output of the reference generator (whose nonlinearity is grossly exaggerated for clarity) is distorted in the same way as the main input. The inset shows the staircase waveforms of the resistor ladder and replica track-and-hold outputs. A deadzone, whose duration is denoted by $T_d$ is introduced between successive cycles of comparator array autozeroing. The duration of the deadzone time depends on the size of the comparator coupling capacitors and the leakage currents that would corrupt the stored references. In the technology chosen for our implementation, calculations showed that reference (& offset) storage would change only by a small fraction of an LSB over several hundreds of microseconds. A 25 ns (four conversion cycles) autozero duration per comparator and a dead time of 160 $\mu$s were chosen. Since the counter only increases by one everytime, the speed demands of the resistor ladder are modest. This enables further power reduction as large valued resistors can be used in the resistor ladder.

### 8.2.1 Linear Reference Generation

The schematic for generating the linear references is as shown in Figure 8.2. A current is passed through a series of resistors and the mid-point voltage of the ladder which dictates the common mode of the references is controlled using a negative

feedback loop. The resistors used are poly resistors available in the technology. These resistors vary with temperature and process corner. The total variation of the resistance is $\pm 25\%$ in the present technology. If the current is a constant, then the LSB of the converter which is determined by the IR drop will keep varying with process. In order to keep the LSB invariant the current also needs to be varying such that IR is a constant. One way of achieving this is to generate the current as $\frac{Vref}{R1}$. This R1 is of the same type as the resistor used in the ladder. By same type I mean both resistors being either poly resistors or both being nwell resistors and so on. Now the LSB is of the form $\frac{Vref}{R1} \times R$. This quantity will not vary with process corner as this does not depend on the absolute value of the resistor but depends only on the matching of the resistors . The current generation is done as shown towards the left part of Figure 8.2. Due to negative feedback the voltage at the positive terminal of the opamp OP1 will be $Vref$. The current through M1 now is $\frac{Vref}{R1}$. This current is mirrored into the resistor ladder using the transistor M2. The resistor 31R connected to the drain of M1 is to minimize the error in current mirroring from M1 to M2 which may arise due to the mismatch in the drain to source voltages of M1 and M2.

### 8.2.2 Choosing The Resistor Value

The value of the resistor in the ladder should be such that when a reference is selected it should settle in four clock cycles because an autozero duration for each comparator was chosen to be four clock cycles. If a very small resistor is chosen it would demand a large current in the ladder and this will lead to more power dissipation. If a large resistor is chosen the current required in the ladder will be small but the settling would be poor. There exists a optimum value of resistor and

hence the current. Simulations were done to find an optimum value of current so that the references settle in four clock cycles. A current of 200 $\mu$A was found to be sufficient enough. The value of resistor can be found out from the knowledge of the LSB of the converter. The full scale input range is 3.4 $V_{pkpkdifferential}$. The LSB is $\frac{3.4}{64} = 53.12$ mV. We should have $2 \times 100\mu\text{A} \times R = 53.12$ mV.

$\Rightarrow R = 265.6\ \Omega$

### 8.2.3 Choosing The Deadzone Duration $T_d$

The coupling capacitor of the preamp is 45 fF. The leakage currents of the switch given in the process documents are as follows

Area leakage current (JS)=0.01 fA/ $\mu$m$^2$

Sidewall leakage current (JSS)=0.13 fA/ $\mu$m

The dimensions of the switch which shorts the output of the preamp to its input during the autozero phase are $W = 0.7\mu$m and $L = 0.35\mu$m. The total leakage current is given by $((0.01 \times 0.7 \times 0.35) + 0.13 \times (2 \times 0.7 + 2 \times 0.35))$ fA =0.273 fA. Let us try to find the time in which the capacitors loose say $\frac{1}{100}^{th}$ the LSB. The single ended LSB is 26 mV before the replica track & hold circuit. After the replica track & hold the single ended LSB is 20 mV due to the NMOS source follower body effect. We have to find the time in which the capacitors loose 0.2 mV. This time is given by $\Delta t = \Delta V \times \frac{C}{I} = 0.2 \times 10^{-3} \times \frac{45}{0.273} = 33$ ms. The deadzone duration is chosen as 160 $\mu$s which is actually 100 times the duration of one autozero cycle. This is two orders of magnitude less than the 33 ms value. So the leakage in the capacitor charge in this time is only $(\frac{1}{10^4})^{th}$ its original value. This was a good choice as it will be shown in the next chapter that the loss in SNR due to background autozero is negligible for this choice of $T_d$.

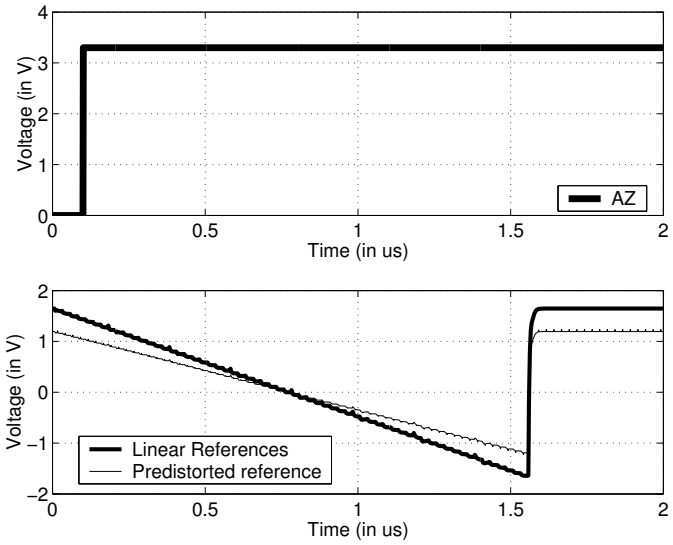


Figure 8.3: Autozeroing for one cycle.

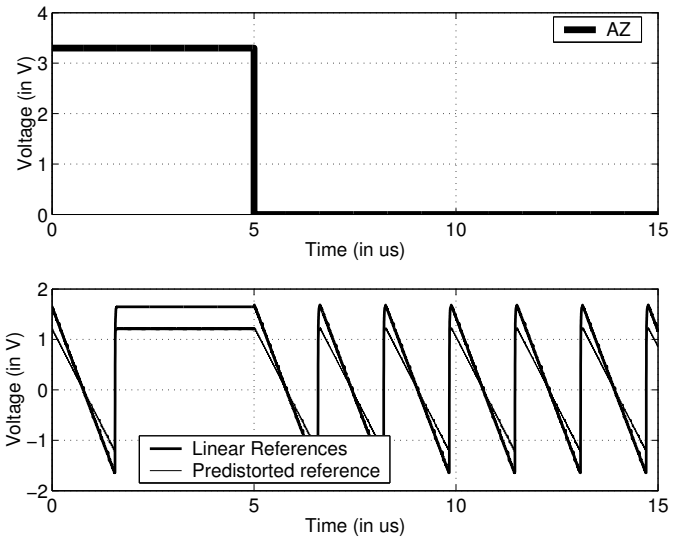


Figure 8.4: Continuous autozeroing of the comparators.

## 8.3 SIMULATION RESULTS

The background autozero can be controlled externally using the signal AZ. The functioning is as follows. The AZ signal is an active low control signal which goes to the six bit counter. When this signal is low the six bit counter keeps counting continuously and the background autozero takes place continuously. The moment AZ goes high the counter continues counting and stops at all one state of the counter. Now there will be no background autozero taking place. The back-

ground autozero process will resume once the AZ signal is made low. Figure 8.3 shows the linear references and the predistorted references when autozeroing is done for one cycle. Note that the predistorted references appear to be attenuated when compared to the linear references. This is predominantly due to the NMOS source follower whose gain is close to 0.8 due to the body effect. When the counter output is zero, $63^{rd}$ reference is selected and the $63^{rd}$ comparator is selected for autozeroing. As the counter keeps incrementing the comparators are autozeroed in a serial fashion from the $63^{rd}$ to the first one. When counter reaches all one state the $63^{rd}$ comparator is selected again and the counting will continue or stop depending on the AZ signal being low or high. Figure 8.4 shows the linear references and the predistorted references when the autozeroing takes place continuously. The AZ signal is made low at 5 $\mu$s and continuous background autozero starts after this. The autozero that happens in the beginning even when AZ is high is because of the initial state of the counter which is arbitrary and it happens to be all zero state in this simulation. So the counter counts till it reaches all one state and stops there since the AZ signal is high. Variations in common mode output voltage of the reference ladder with the process corners is tabulated in Table 8.1. The input common mode also does vary similarly with process corners because the buffers in the reference path are a replica of the buffers present in the signal path.

Table 8.1: Simulation results of the predistorted reference generator at a temperature of 70 °C

| Process corner | Supply | Output common mode voltage (in V) |
|---|---|---|
| cmostm | 3.0 | 2.10 |
| cmosws | 3.0 | 2.10 |
| cmoswz | 3.0 | 1.75 |
| cmoswp | 3.0 | 2.10 |
| cmoswo | 3.0 | 2.40 |

### 8.3.1 Simulation Results of Layout Extracted ADC

The simulation results of the layout extracted ADC are tabulated below for typical process corner "cmostm". The normalized output spectrum of the ADC is as

| | |
|---|---|
| Supply voltage | 3.3 V |
| Temperature | $27^{o}$C |
| $F_{in}$ | 48.4375 MHz |
| $F_s$ | 100 MHz |
| $V_{in}$ | 3.2 $V_{pp}$ differential |
| SQNR | 37.5 dB |
| SFDR | 44.0 dB |
| Power | 50 mW |

Table 8.2: Simulation results of layout extracted ADC

shown in Figure 8.5. The SQNR and the SFDR numbers of the ADC for an input frequency of 48.3475 MHz and a clock frequency of 100 MHz are tabulated in Table 8.3.

| Corner | SQNR (in dB) | SFDR (in dB) |
|---|---|---|
| cmostm | 37.6 | 44.0 |
| cmosws | 37.8 | 45.0 |
| cmoswo | 36.5 | 41.6 |
| cmoswz | 32.0 | 38.8 |
| cmoswp | 36.1 | 40.1 |

Table 8.3: Simulation results of layout extracted ADC for five different process corners

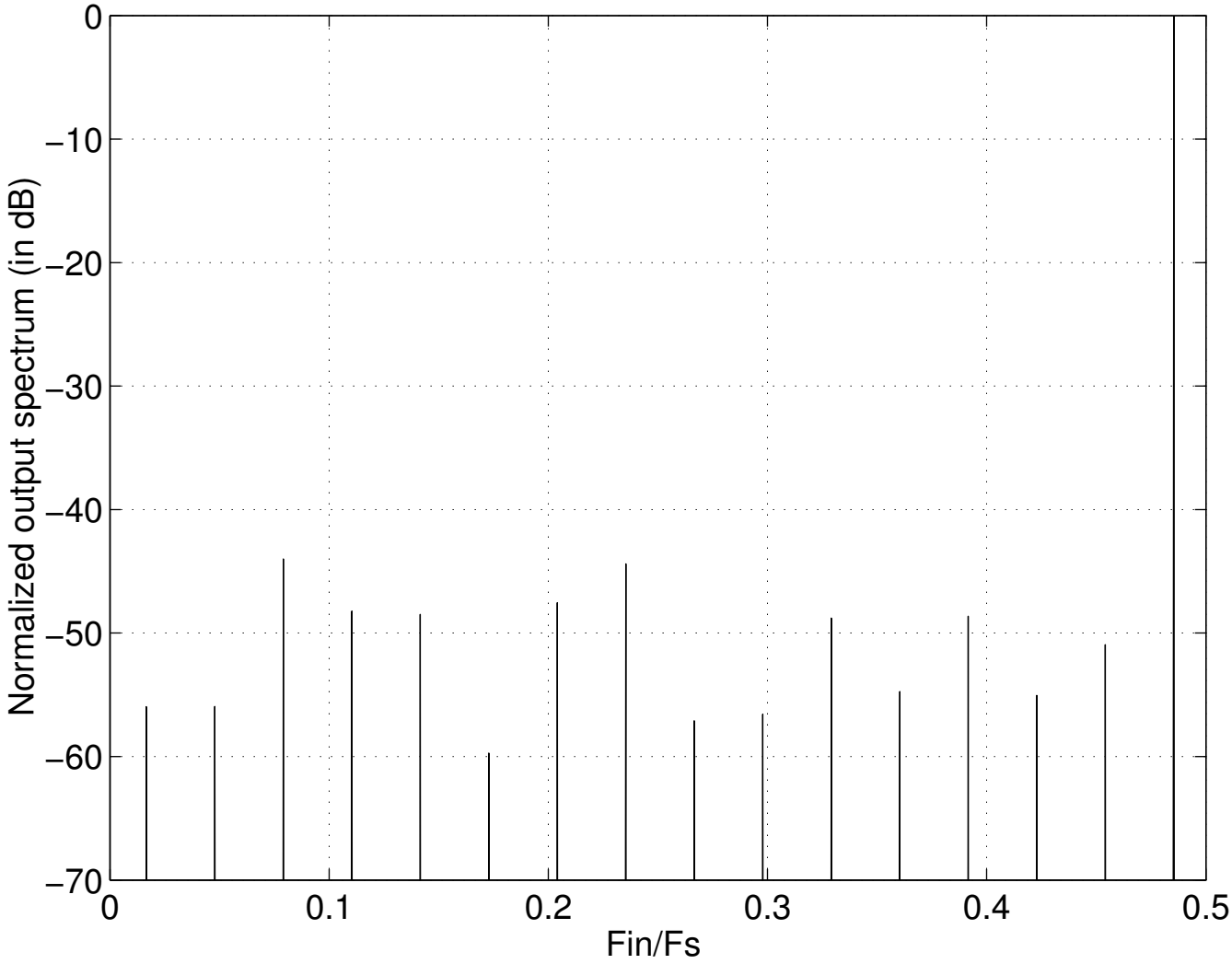


Figure 8.5: The normalized output spectrum of the ADC in cmostm corner for a clock speed of 100 MHz and input of 48.4375 MHz.

# CHAPTER 9

# DIGITAL LOGIC

## 9.1 MAJORITY AND 1-OF-N LOGIC

The comparator array gives out a 63 bit thermometer code. This thermometer code is to be processed by a majority logic block to get rid of the "bubbles" in the code and then it is to be converted to 1-of-63 code representation. The block level diagram of the digital logic is shown in Figure 9.1. Here the comparator outputs go to a majority logic block and transition detector before going as inputs to the encoder. To implement the logic as it is shown in Figure 9.1 we would need to implement AB+BC+CA. It is easier to implement $\overline{AB+BC+CA}$ than AB+BC+CA . So the logic is modified as shown in Figure 9.2. This is the actual logic which is implemented in the ADC. $\overline{AB+BC+CA}$ is obtained by using the circuit shown in Figure 9.3.

## 9.2 ENCODER

The encoder used in this work is a precharge and evaluate type of encoder. The schematic of the encoder is shown in Figure 9.4. The working of this is as follows. When ROM_CLK is low the output, OUT is evaluated to zero. The moment ROM_CLK goes high the output, OUT remains low or goes high depending on the input signal, IN. If the input signal is low then OUT remains low and if the input signal is high, OUT goes high. For a 6-bit binary output six such stages are needed

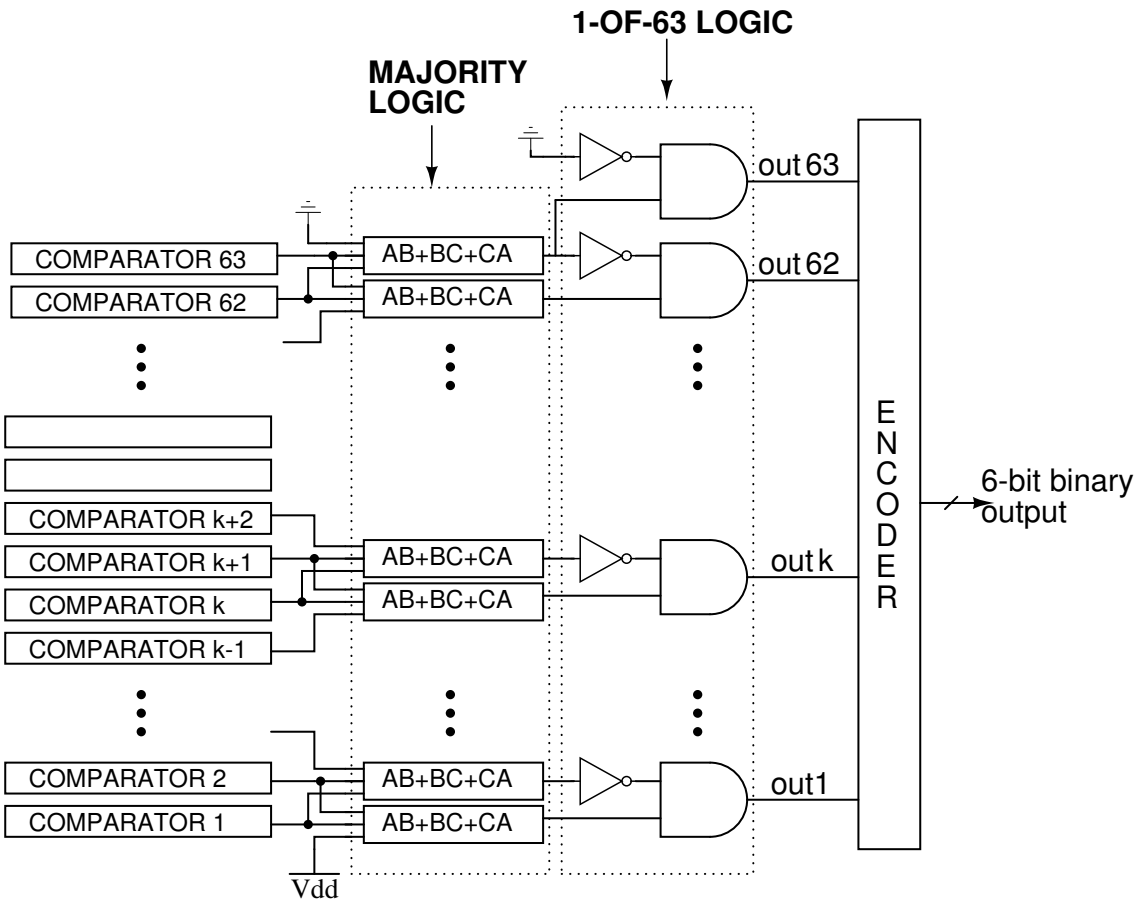


Figure 9.1: Block level diagram of digital logic.

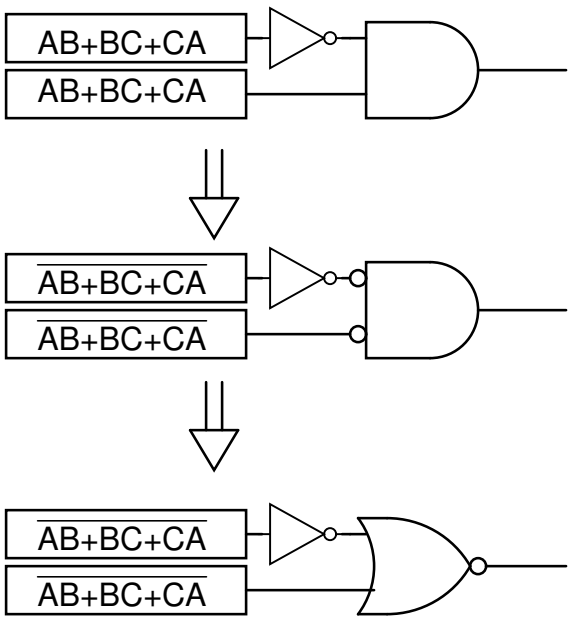


Figure 9.2: Modified implementation of majority and 1-of-63 logic.

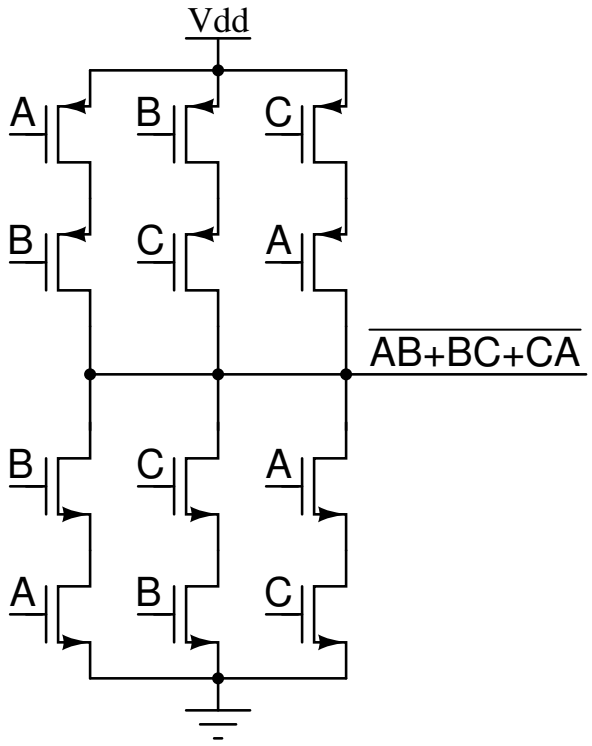


Figure 9.3: Circuit to implement $\overline{AB+BC+CA}$

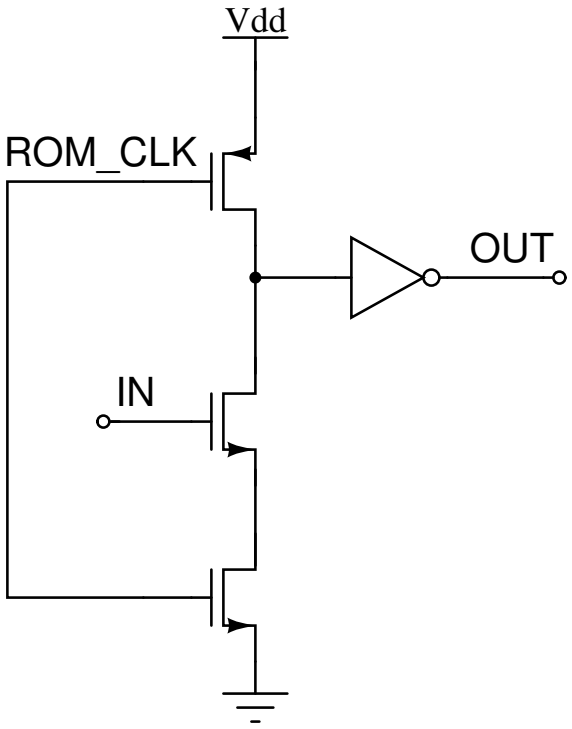


Figure 9.4: Schematic of a unit cell of precharge and evaluate type of encoder.

with the IN signal of each stage controlled appropriately by the 1-of-63 logic outputs. For example to evaluate the least significant bit of the digital output, the circuit will look as shown in Figure 9.5. This bit has to be high whenever one of the $1^{st}$, $3^{rd}$ ,$5^{th}$ , $\ldots 61^{st}$ or $63^{rd}$ outputs of the 1-of-63 logic is high. This is achieved by connecting the gates of the NMOS transistors M1,M2,M3,. . . , M30 and M31 of Figure 9.5 to these outputs of the 1-of-63 logic block.

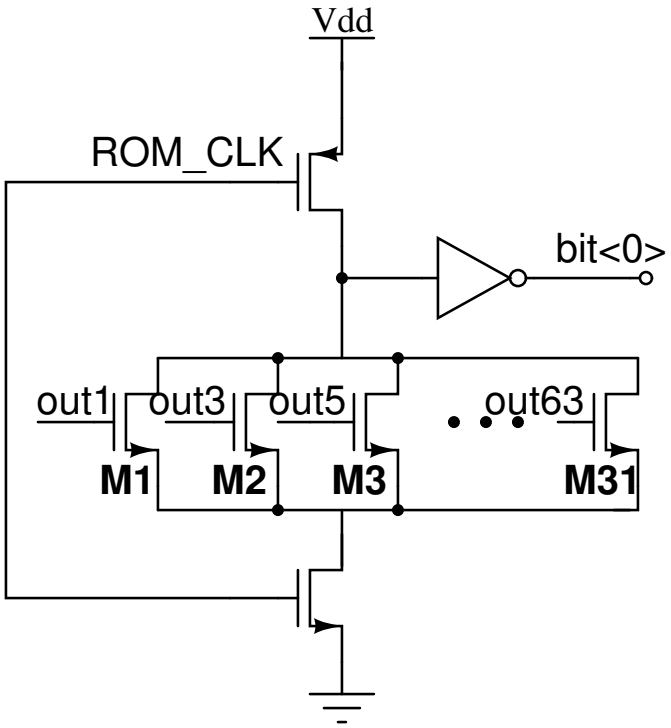


Figure 9.5: Schematic of a portion of encoder to evaluate the least significant bit.

### 9.3 6-BIT COUNTER

The schematic of the 6-bit counter is shown in Figure 9.6. The clock to the flip flops are derived form the Master_clock, which was described how it was derived in Chapter 7, by dividing it by four. This was done because as said earlier the autozero of each comparator takes four clock cycles. The logic is designed such that if 'AZ' signal is high then the counter starts counting from its present state till it reaches the all one state. As long as 'AZ' signal is high the counter remains

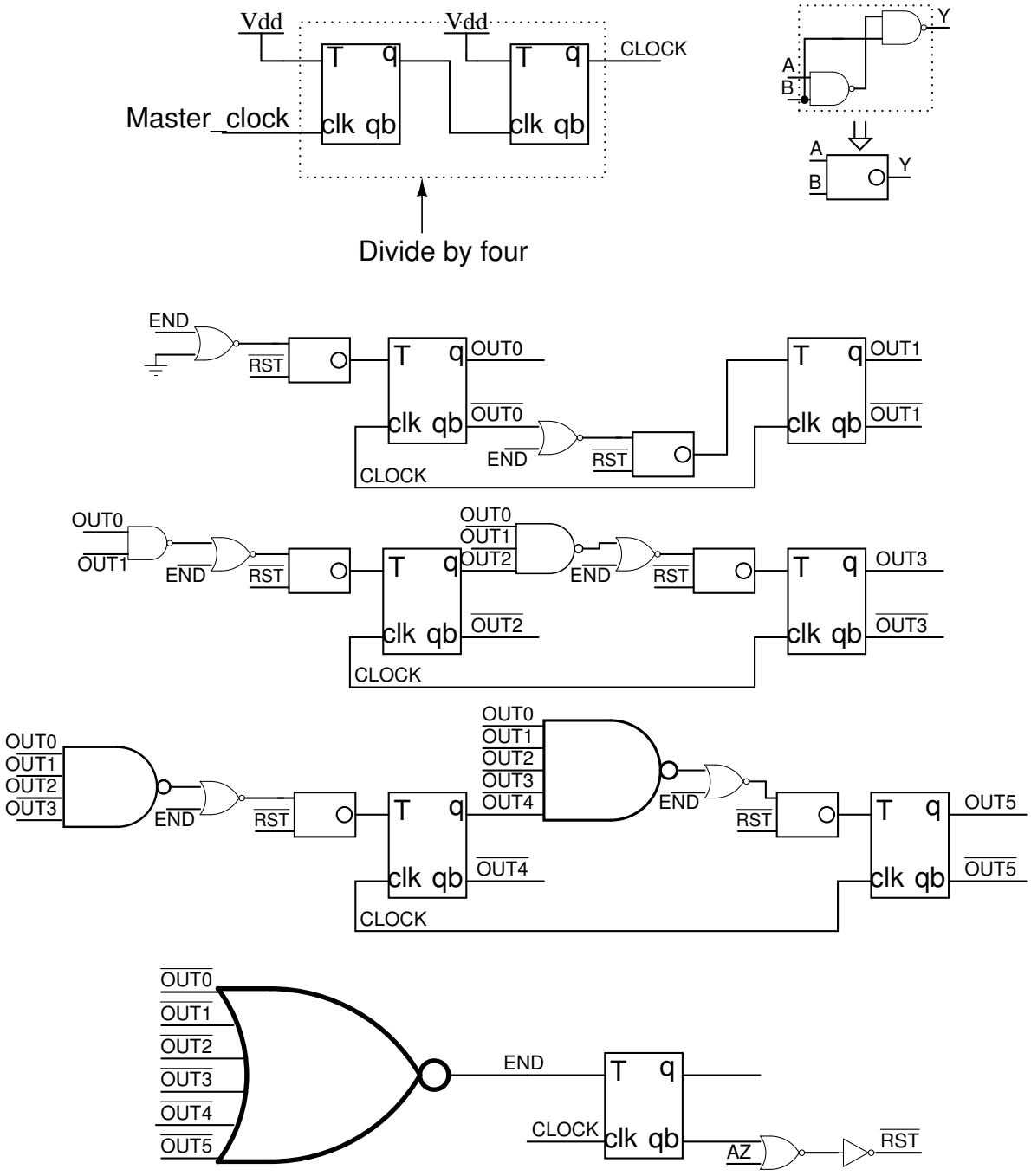


Figure 9.6: Schematic of the 6-bit counter.

at this state. The moment 'AZ' signal goes low the counter reaches all zero state and it starts incrementing in steps of one. Once the counter reaches the all one state the counting continues or stops depending on if the 'AZ' signal is low or high respectively. So the autozeroing frequency of the comparators can be controlled using the 'AZ' signal which can be controlled externally. If continuous background autozeroing of the comparators is desired then one has to connect the 'AZ' signal to ground. By controlling the time period and duty ratio of the 'AZ' signal one can autozero the comparators with a desired dead zone between two autozero cycles.

# CHAPTER 10

# DEGRADATION IN SNR DUE TO BACKGROUND AUTOZERO

## 10.1 LOSS IN SNR

When a comparator is being autozeroed, it is unavailable for conversion. The preamp is removed from the signal path and put in a negative feedback loop as discussed in Chapter 5. The latch following the preamp, however, is allowed to make a decision, which could be a 1 or 0 with equal probability. The comparator which is being autozeroed makes a wrong decision with a probability of 0.5. This will lead to an increase in the quantization error and the overall SNR of the converter is degraded. This loss in SNR is calculated in the next section.

## 10.2 CALCULATING THE LOSS IN SNR

If the input is very "far away" from the reference voltage of the comparator being autozeroed, then the majority-of-three logic will correct for a "bubble" caused by the random decision of the comparator being autozeroed, as shown in Figure 10.1. In this figure, the input lies between $(k+2)\Delta$ and $(k+3)\Delta$, while the $k^{th}$ comparator is being autozeroed. $\Delta$ denotes the LSB size. Notice that in this case, no penalty is incurred by autozeroing the comparator. An input "close" to the threshold of the comparator being autozeroed will result in increased quantization error. We

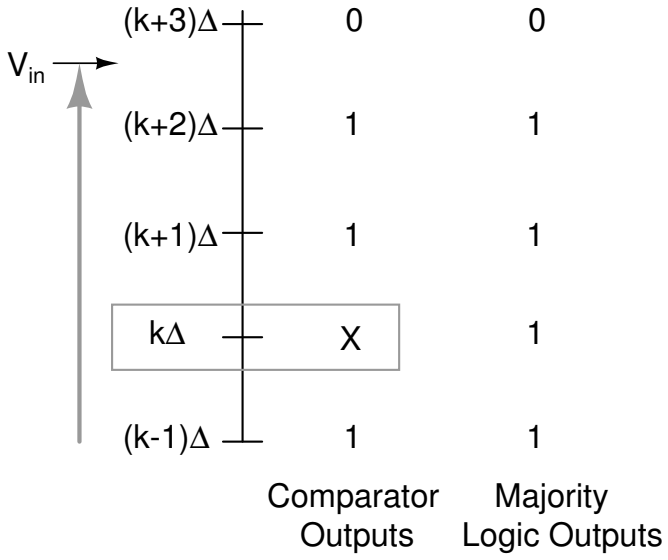


Figure 10.1: The comparator outputs when $k^{th}$ comparator is being autozeroed.

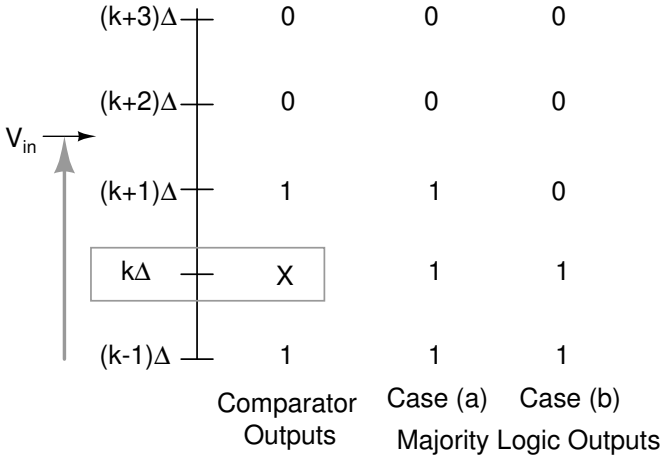


Figure 10.2: The comparator outputs when input lies in the range $(k+1)\Delta + \epsilon$.

refer to such situations as collisions Next we consider four cases in which collision occurs.

### 10.2.1 Case 1

Assume that comparator $k$ is being autozeroed. The input lies in the range $(k+1)\Delta + \epsilon$ (where $0 \leq \epsilon \leq \Delta$) as shown in Figure 10.2. The $k^{th}$ comparator puts out a correct decision "1" with probability 0.5 as shown in Case (a) of Figure 10.2. In this case there will not be any increase in the quantization error as the digital output that results is a correct representation of the analog input within one LSB. When

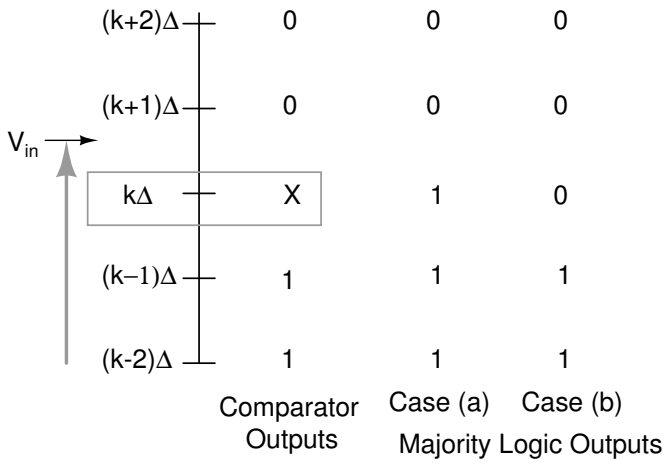


Figure 10.3: The comparator outputs when input lies in the range $k\Delta + \epsilon$.

$k^{th}$ comparator puts out a wrong decision "0" which is the Case (b) in Figure 10.2, a bubble appears one position below the top of the comparator thermometer code output. The majority correction logic corrects this bubble but the quantization error will be $\Delta + \epsilon$ rather than the usual $\epsilon$.

### 10.2.2 Case 2

The input lies in the range $k\Delta+\epsilon$ (where $0 \leq \epsilon \leq \Delta$) as shown in Figure 10.3. The $k^{th}$ comparator puts out a correct decision "1" with probability 0.5 as shown in Case (a) of Figure 10.3. In this case there will not be any increase in the quantization error. When $k^{th}$ comparator puts out a wrong decision "0" which is the Case (b) in Figure 10.3, the quantization error will be $(\Delta + \epsilon)$.

### 10.2.3 Case 3

The input lies in the range $(k-1)\Delta + \epsilon$ (where $0 \leq \epsilon \leq \Delta$) as shown in Figure 10.4. The $k^{th}$ comparator puts out a wrong decision "1" with probability 0.5 as shown in Case (a) of Figure 10.4. In this case the quantization error is $(-\Delta + \epsilon)$. When $k^{th}$ comparator puts out a correct decision "0" which is the Case (b) in Figure 10.4, there is no increase in the quantized error.

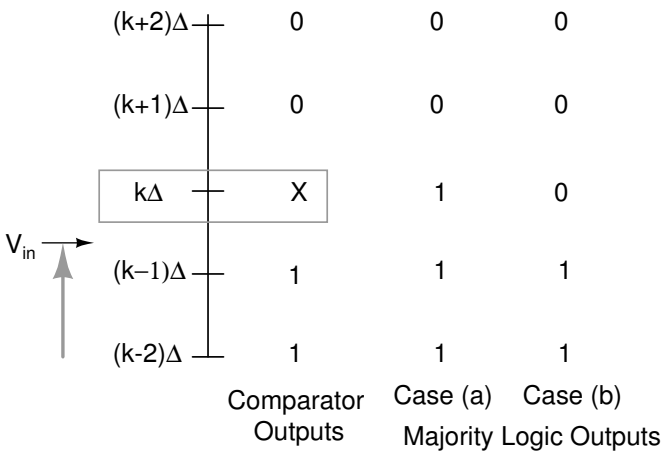


Figure 10.4: The comparator outputs when input lies in the range $(k-1)\Delta + \epsilon$.

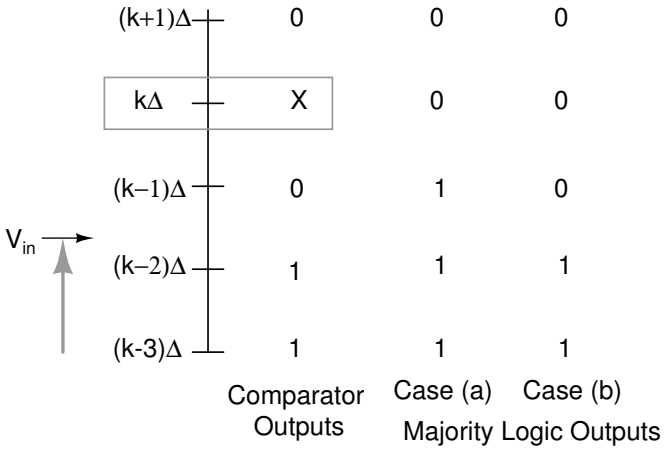


Figure 10.5: The comparator outputs when input lies in the range $(k-2)\Delta + \epsilon$.

### 10.2.4 Case 4

The input lies in the range $(k-2)\Delta+\epsilon$ (where $0 \leq \epsilon \leq \Delta$) as shown in Figure 10.5. The $k^{th}$ comparator puts out a wrong decision "1" with probability 0.5 as shown in Case (a) of Figure 10.5. In this case the quantization error is $(-\Delta+\epsilon)$. When $k^{th}$ comparator puts out a correct decision "0" which is the Case (b) in Figure 10.5, there is no increase in the quantized error. These four cases where there is a likelihood of increased quantization error are shown in Table 10.1, along with their respective probabilities.

$k^{th}$ comparator being autozeroed, $0 \leq \epsilon < \Delta$

| Input Range | Quantization Error |
|---|---|
| $(k+1)\Delta+\epsilon$ | $\epsilon\|_{p=0.5}, (\Delta+\epsilon)\|_{p=0.5}$ |
| $k\Delta+\epsilon$ | $\epsilon\|_{p=0.5}, (\Delta+\epsilon)\|_{p=0.5}$ |
| $(k-1)\Delta+\epsilon$ | $\epsilon\|_{p=0.5}, (-\Delta+\epsilon)\|_{p=0.5}$ |
| $(k-2)\Delta+\epsilon$ | $\epsilon\|_{p=0.5}, (-\Delta+\epsilon)\|_{p=0.5}$ |

Table 10.1: Quantization errors and their probabilities.

The mean square quantization error due to the proposed background autozero scheme can be calculated as follows. We assume that the input signal is uncorrelated with the autozero sequence. From Table 10.1, it is seen that the probability of a collision during any given conversion cycle is $\frac{(k+2)\Delta-(k-2)\Delta}{64\Delta} = \frac{1}{16}$ assuming the input to be uniformly distributed. If a collision occurs, the quantization error is $\epsilon$, $\Delta+\epsilon$ or $(-\Delta+\epsilon)$ with probabilities of 0.5, 0.25 & 0.25 respectively. Recall that $\epsilon$ is uniformly distributed between 0 & $\Delta$. Now we will try to find the distribution of the quantization error, $q_e$ in terms of the variable $\epsilon$. When there is no collision, $q_e$ is $\epsilon$. The probability of no collision is $1-\frac{1}{16} = \frac{15}{16}$. When collision occurs the error is $\epsilon$ with a probability of 0.5. So the probability that $q_e$ will take the value $\epsilon$ is

$\frac{15}{16} + \frac{1}{16} \times 0.5 = \frac{31}{32}$. The probability that $q_e$ will take the value $\Delta + \epsilon$ is $\frac{1}{16} \times 0.25 = \frac{1}{64}$. The probability that $q_e$ will take the value $(-\Delta + \epsilon)$ is $\frac{1}{16} \times 0.25 = \frac{1}{64}$. Hence the quantization error during any cycle an be expressed (in terms of the random variable $\epsilon$) as

$$q_e = \begin{cases} \epsilon \ , & p = \frac{31}{32} \\ \Delta + \epsilon \ , & p = \frac{1}{64} \\ -\Delta + \epsilon \ , & p = \frac{1}{64} \end{cases} \tag{10.1}$$

Quantization noise power is given by

$$\sigma_{q_e}^2 = < {q_e}^2 > - < q_e >^2 \tag{10.2}$$

As the distribution of $q_e$ is known, $< {q_e}^2 >$ and $< q_e >^2$ can be found as follows

$$< {q_e}^2 > = \frac{31}{32} < \epsilon^2 > + \frac{1}{64} < (\Delta + \epsilon)^2 > + \frac{1}{64} < (-\Delta + \epsilon)^2 > \tag{10.3}$$

$$= \frac{31}{32} < \epsilon^2 > + \frac{1}{32}\Delta^2 + \frac{1}{32} < \epsilon^2 >$$

$$= < \epsilon^2 > + \frac{1}{32}\Delta^2$$

$$< q_e > = \frac{31}{32} < \epsilon > + \frac{1}{64} < (\Delta + \epsilon) > + \frac{1}{64} < (-\Delta + \epsilon) > = < \epsilon > \tag{10.4}$$

$$\sigma_{q_e}^2 = < {q_e}^2 > - < q_e >^2 = < \epsilon^2 > + \frac{1}{32}\Delta^2 - < \epsilon >^2 \tag{10.5}$$

$\epsilon$ is a random variable which is distributed uniformly in the interval $(0, \Delta)$. Therefore $< \epsilon^2 > - < \epsilon >^2 = \frac{\Delta^2}{12}$. *If the background autozero process was running continuously,* quantization noise power would be $\sigma_{qe}^2 = \frac{\Delta^2}{12} + \frac{\Delta^2}{32} = \frac{11}{96}\Delta^2$ or an SNR penalty of $10 \log_{10} \left( \frac{\frac{11}{96}}{\frac{1}{32}} \right) = 1.38$ dB. Extensive MATLAB simulations with a uniformly distributed random input confirmed the analysis carried out above. For a full scale sine wave input the MATLAB simulations showed a degradation of 1.5 dB in the

SNR. The MATLAB code for calculating the degradation in SNR is included in Appendix A.

However, as discussed in the previous section, there is a dead-time $T_d$ between two successive background-autozero cycles as indicated in Fig. 8.1. In our implementation, $T_{az} = 63 \times 25\ \text{ns} \approx 1.6\,\mu s$. If we choose $T_d = 99\,T_{az}$ (which is still a conservative value for $T_d$), the decrease in SNR can be calculated to be about 0.02 dB.

# CHAPTER 11

# EXTENSION TO FOLDING

## 11.1 PRINCIPLE OF FOLDING

Folding is a type of analog preprocessing that is used to reduce the number of comparators in a flash-type converter [15]. A simplified block diagram of a folding ADC is as shown in Figure 11.1. The coarse ADC gives the information about the MSB's and the fine ADC gives the information about the LSB's. Figure 11.2 shows the input being folded by a factor of three. Some information is lost in folding and to determine the MSB's a coarse ADC is used. Figure 11.3 shows the simplified diagram of a 6-bit flash ADC folded by a factor of 3. Observe that here we need only 21 latches as against 63 needed in the normal flash ADC. The coarse ADC consists of two comparators. A folder is realized by connecting the outputs of three preamps in an appropriate manner [15].

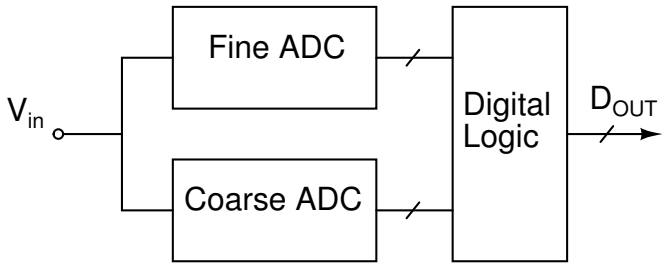


Figure 11.1: Simplified block diagram of a generic folding ADC .

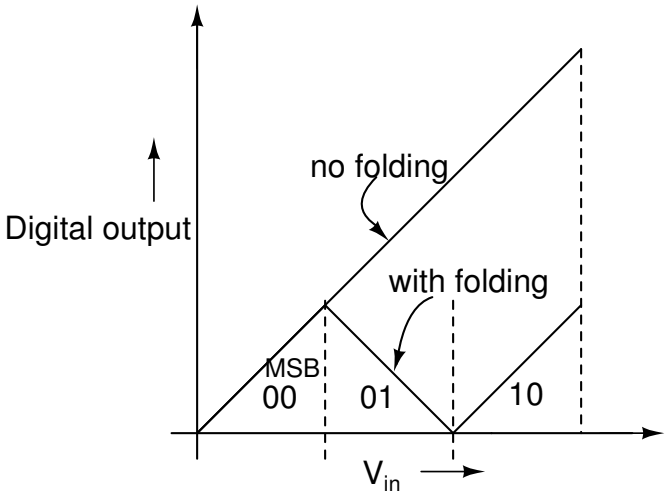


Figure 11.2: Input folded by a factor of three.

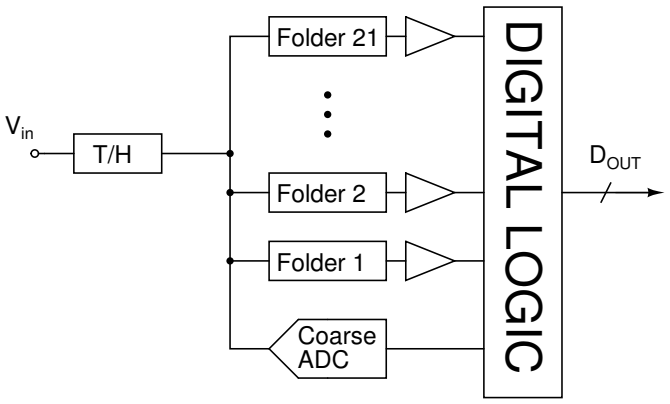


Figure 11.3: A 6-bit flash ADC folded by a factor of 3..

## 11.2 FOLDER

The schematic of the folder is as shown in Figure 11.4. The folder consists of three preamps whose outputs are connected as shown in Figure 11.4. The preamp topology is identical to that used in the ADC except for the tail current source which is a cascaded configuration now. This was necessary because a low output impedance of the current source gives rise to a significant offset in the folder input-output characteristics. The coupling capacitors which precede the preamps are charged with appropriate references during autozero cycle. For example the preamps in the first folder will have their capacitors charged to Vref1, Vref22 and Vref43 respectively.

A preliminary design of the folding ADC was done at the schematic level which employed a time interleaved track and hold [1]. The folding factor was 3 which reduced the number of latches from 63 to 21. The dynamic gain of the folder was 10 in the schematic.

## 11.3 EXTENSION OF PRESENT ARCHITECTURE TO FOLDING

The folding will look as shown in Figure 11.5 in the case of a conventional flash ADC. Note that the outputs of the preamps which are far apart have to be connected together. For example the outputs of the $1^{st}$, $22^{nd}$ and $43^{rd}$ preamps have to be connected. But these are far apart since the comparators are placed such that their thresholds gradually increase from bottom to top as demanded by the reference ladder. This will make the layout complex and the preamp dynamic gain will be poor because of the interconnects which connect the outputs of the preamps and the latch. The folding when implemented in the present ADC will look as shown

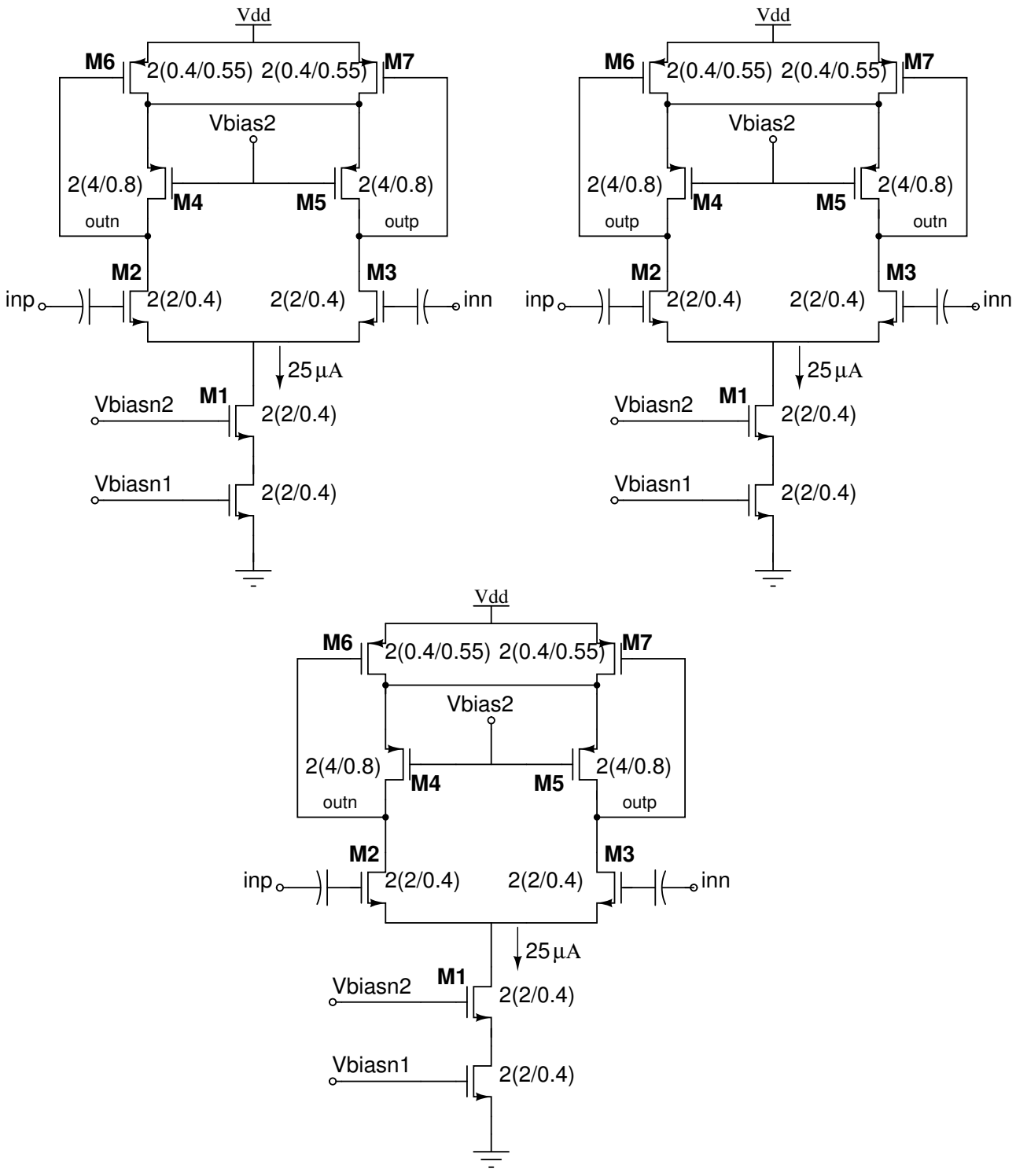


Figure 11.4: Schematic of a folder.

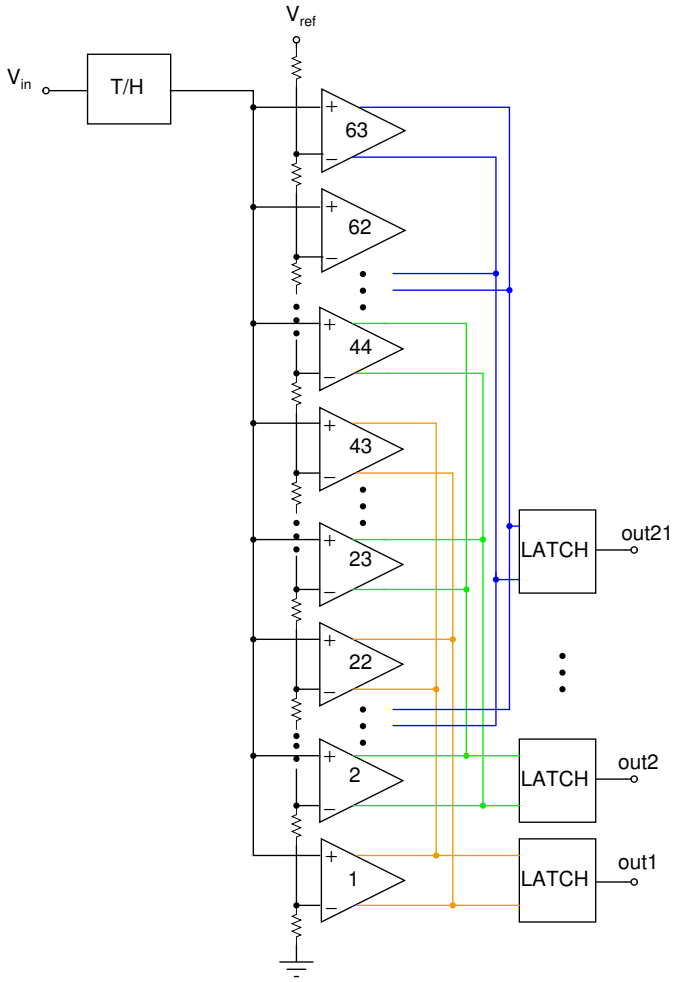


Figure 11.5: Folding in a conventional flash ADC.

in the Figure 11.6. Here the preamps whose outputs are to be connected can be placed next to each other. This is possible because it is just a matter of choosing the appropriate reference voltage while autozeroing the comparator. In the present architecture if folding is used the power dissipation can be further reduced. For example when we do folding by a factor of 3, the number of latches will come down from 63 to 21.

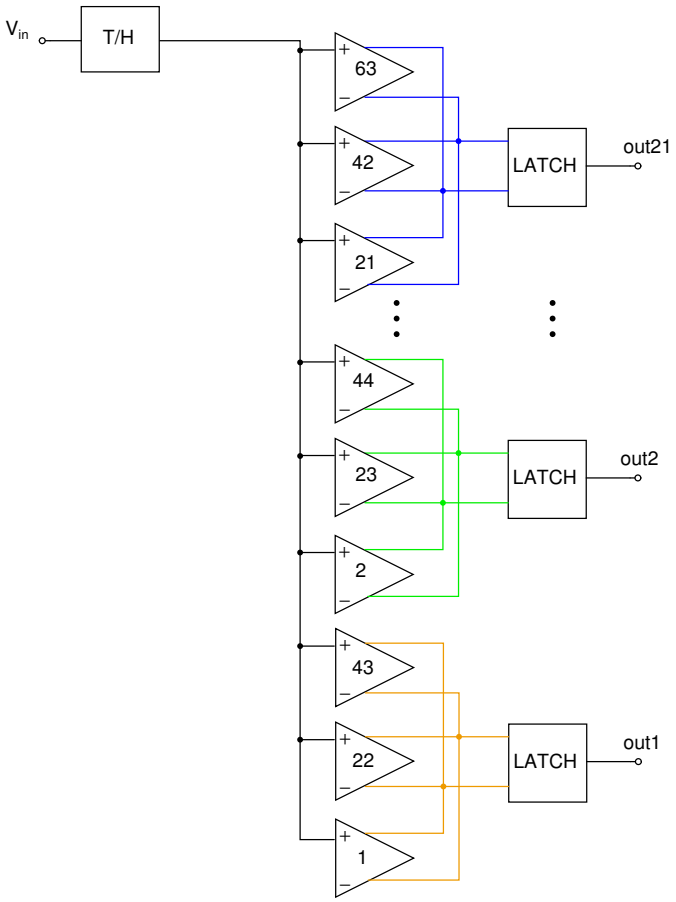


Figure 11.6: Folding in the present flash ADC.

# CHAPTER 12

# BOARD DESIGN

## 12.1 PRINTED CIRCUIT BOARD

To test the performance of the ADC designed a PCB (Printed circuit board) is necessary. This PCB was designed with the help of OrCAD layout software. This was a two layered board and was fabricated through Zeta electronics , Chennai. The dimensions of the board are 4″× 5″ and the material is FR4 glass epoxy. The thickness of the board is 1.6 mm. A snapshot of the board with all the components populated on it is as shown in Figure 12.1.

## 12.2 QUANTITIES GENERATED ON THE BOARD

The quantities which are generated on board are

1. Reference voltages
2. Reference currents.
3. Differential inputs to the ADC around a common mode.
4. High frequency clock using a crystal oscillator.

We will see in certain detail how each of these quantitites are generated and what are the issues involved.

Figure 12.1: The PCB designed for testing the ADC.

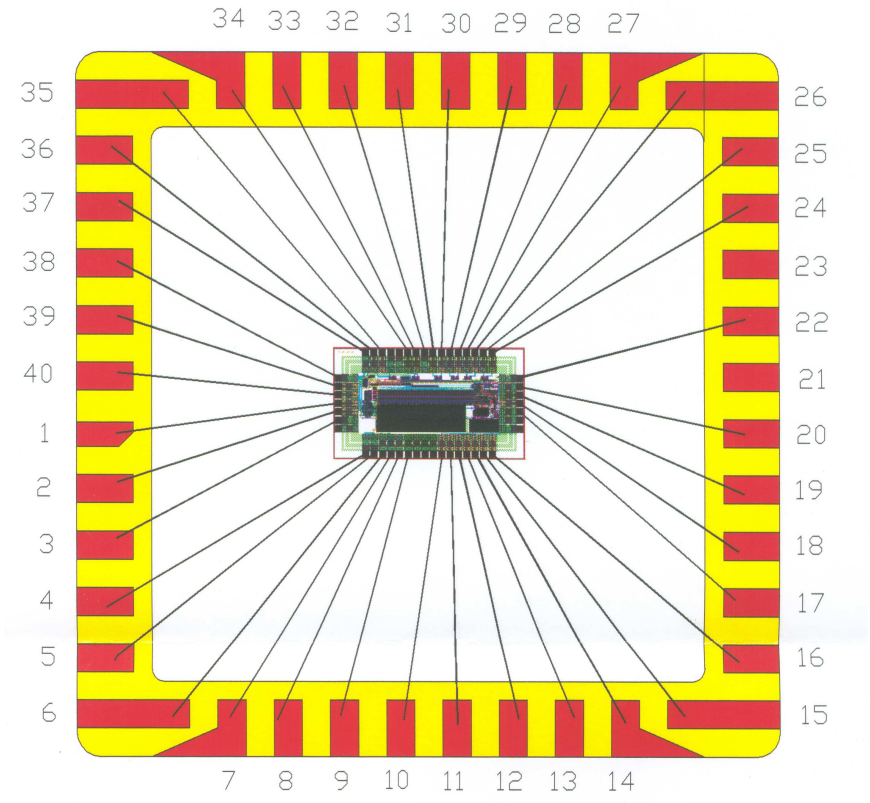


Figure 12.2: The bonding diagram of the die.

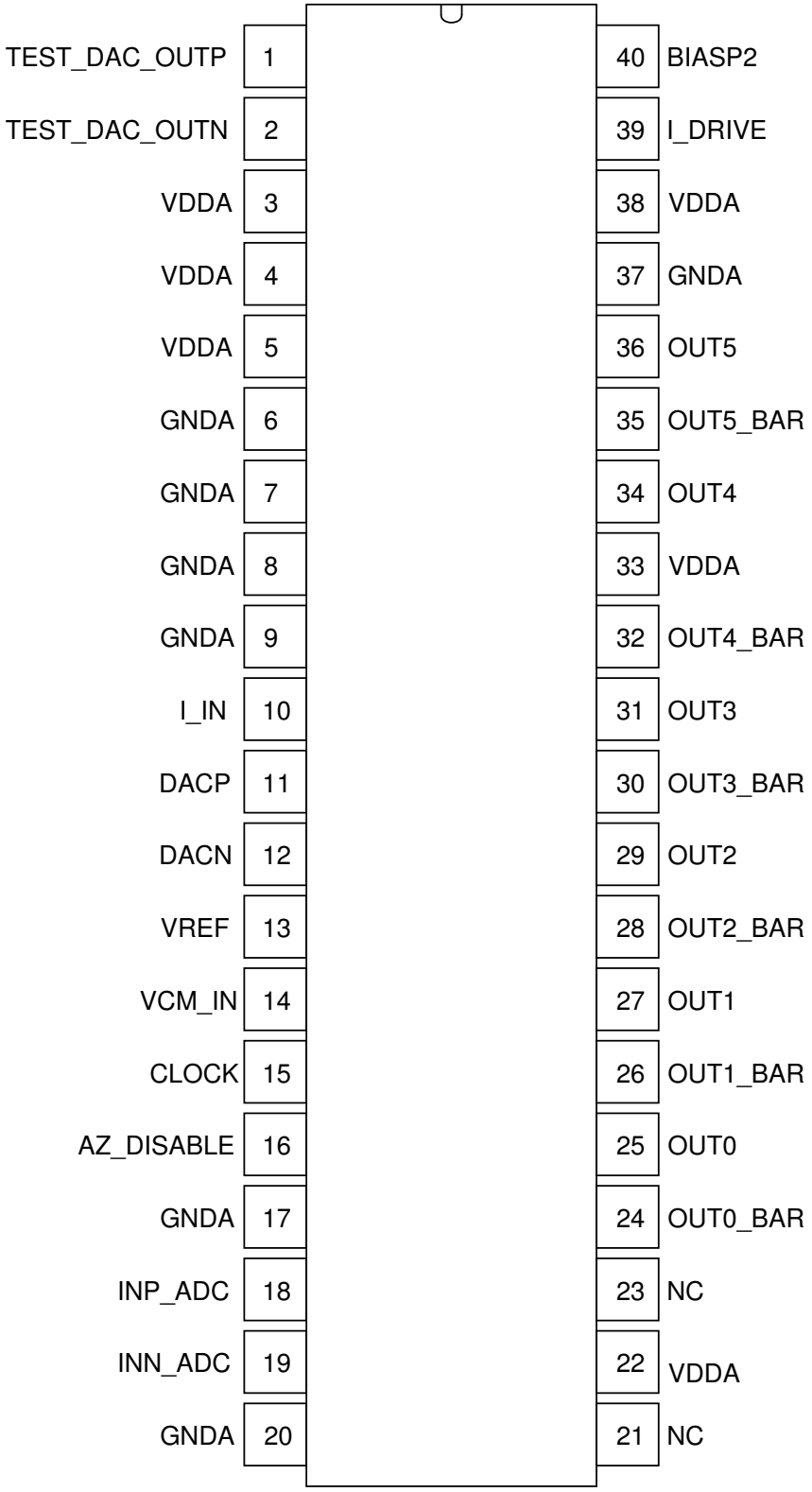


Figure 12.3: The pinout diagram of the ADC.

### 12.2.1 Reference Voltages

Two reference voltages are needed for the ADC. One is for fixing the common mode (VCM_IN, pin 14 in Figure 12.3) and the other is for fixing the lsb size of the converter( VREF, pin 13 in Figure 12.3). The nominal values of these two voltages are 2 V. But we need to have a mechanism to vary these voltages so that the performance of the ADC can be studied for different common mode voltages and different full scale ranges of the input. One way to generate the voltages is first have a fixed voltage which is very stable across temperature and supply variations and then use an opamp in a non-inverting amplifier configuration to get the desired voltage. The chip that gives a fixed voltage of 1.25 V is REF3112 chip from Texas Instruments. This voltage is given to the positive terminal of the OPA335 amplifier which is a single supply, low offset CMOS operational amplifier from Texas Instruments. This opamp is used in non-inverting configuration with a variable resistor in the feedback. By varying this resistor the output voltage can be varied. The resistor values were choosen such that for a full variation of the variable resistor the output voltage vaires form 1.5 V to 2.1 V. The output voltages of the two opamps are filtered using low-pass filters. A simplified schematic of the circuit which generates these voltages is shown in Figure 12.4.

### 12.2.2 Reference Currents

The ADC needs five current sources. Out of these one is used for generating bias voltages(I_IN, pin 10 in Figure 12.3), one for biasing the testing dac(BIASP2, pin 40 in Figure 12.3), one for biasing the LVDS drivers(I_DRIVE, pin 39 in Figure 12.3) and two for debug purposes.(DACP, DACN pin 11 and pin 12 in Figure 12.3). These currents are generated using LM334 chip of the National Semiconductor.

### 12.2.3 Generating Differential Voltages for the ADC

The schematic of the circuit to generate the differential input to the ADC is as shown in Figure 12.5. Using this circuit we have the option of generating a differential dc input or a differential sine wave input to the ADC by appropriately swiching on or off the switches $S_1$, $S_2$,$S_3$ and $S_4$.

#### 12.2.3.1 Generating DC Ramp

The switches $S_1$ and $S_2$ are closed while the switches $S_3$ and $S_4$ are open (refer to Figure 12.5). The input $V_{in}$ given to positive terminal of OPA335 is from a a 16-bit NI (National Instruments) data acquisition card. The $\frac{Vcm}{2}$ and $V_{cm}$ voltages given to the negative terminals of the opamps are generated from the circuit which we have discussed in the previous section. The outputs of the opamps give us the voltages $V_{cm} + V_{in}$ and $V_{cm} - V_{in}$. These voltages will be noisy because of the noisy nature of $V_{in}$. A low pass filter constituted by a 1 k$\Omega$ resistor and a 10 $\mu$F capacitor is used to filter the noise. By linearly increasing the voltage $V_{in}$, a ramp input can be given to the ADC. The static performance of the ADC like INL and DNL can now be measured

#### 12.2.3.2 Generating Sine Wave Input

The switches $S_3$ and $S_4$ are closed while the switches $S_1$ and $S_2$ are open (refer to Figure 12.5). The centre tapped transformer ADT1-1WT from minicircuits is driven by a signal generator. The centre tap of the secondary is connected to Vcm so that the trnsformer gives a differntial output centred at Vcm. The 1 k$\Omega$ resistors after the switches $S_3$ and $S_4$ are for providing high impedance when one sees from the primary side of the transformer.

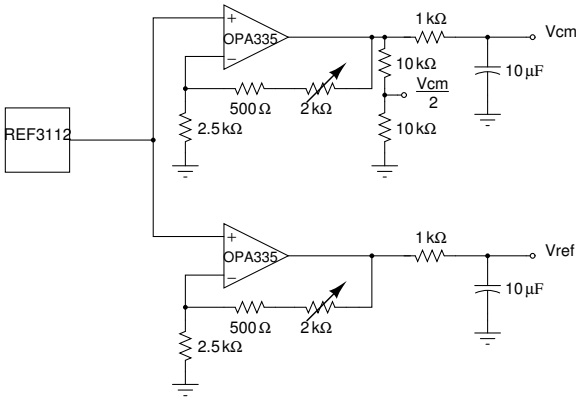


Figure 12.4: Generating the reference voltages.

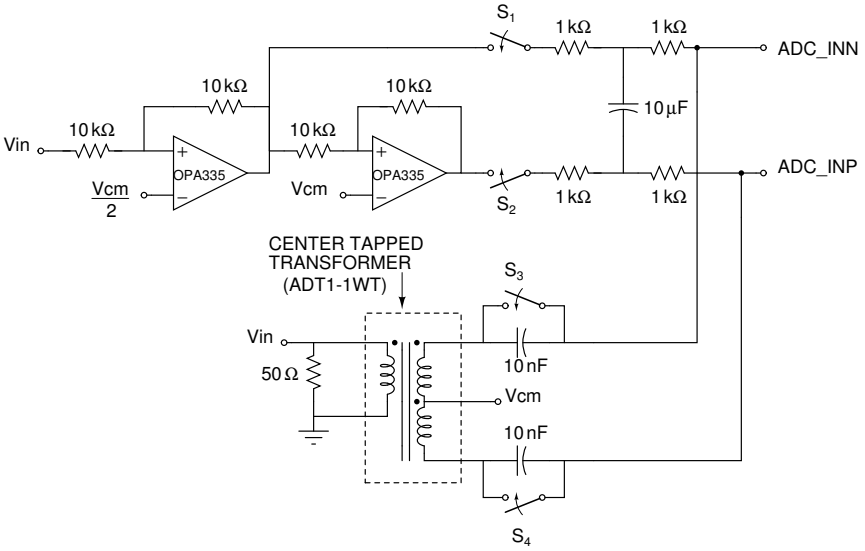


Figure 12.5: Schematic of the circuit driving the ADC.

### 12.2.4 Generating Clock On Board

It is difficult to get a signal generator which gives clocks swinging rail to rail at high frequencies. One way to overcome this is by generating clock on the board using a crystal oscillator and a PLL. The PLL chip used for this purpose was CY-24115 from Cypress semiconductors. By varying the control pins given for this chip and by choosing different crystals, clock frequencies ranging from 40 MHz to 200 MHz could be produced on board.

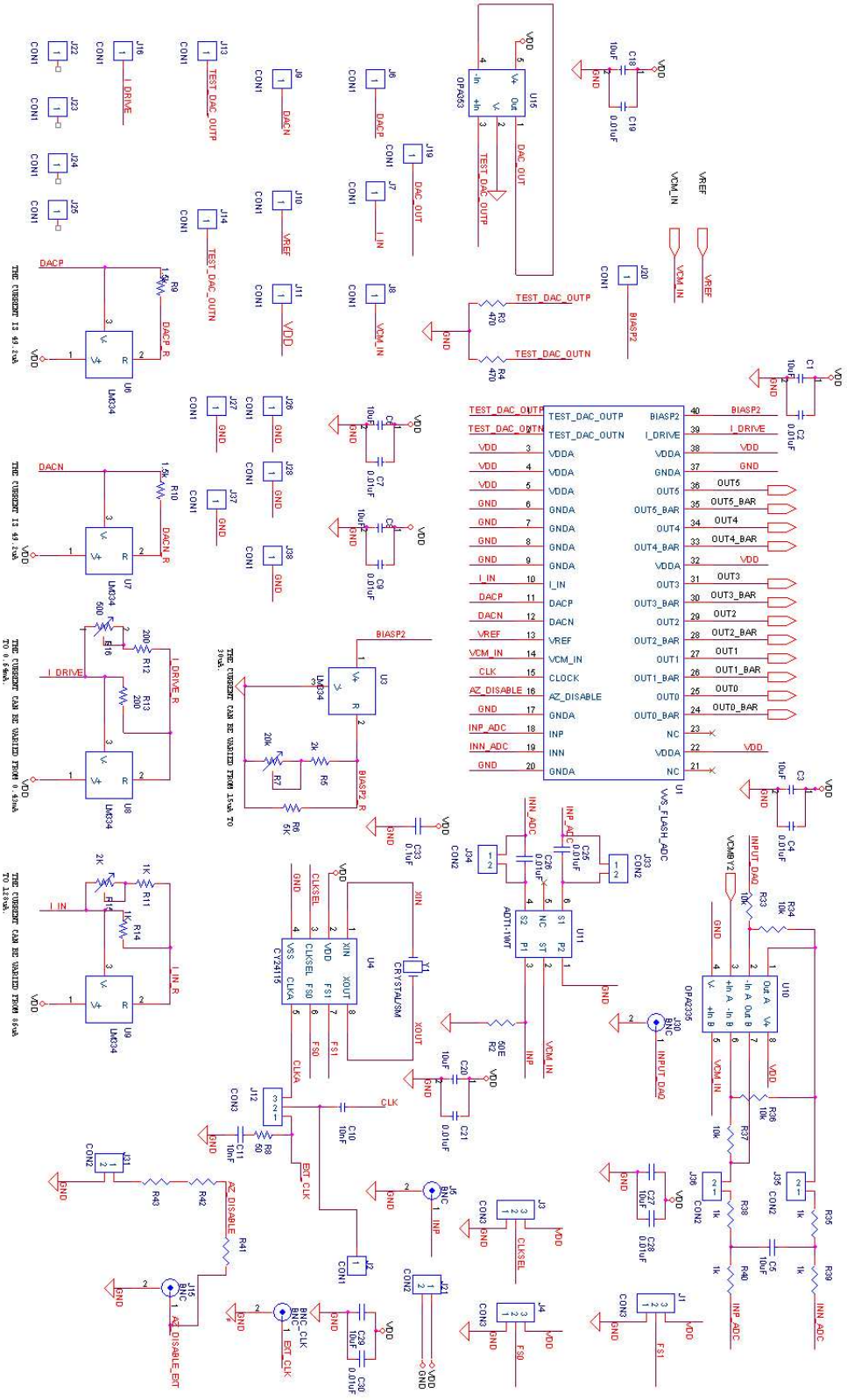

Figure 12.6: Schematic of the portion of the board showing the ADC and some of the components around it.

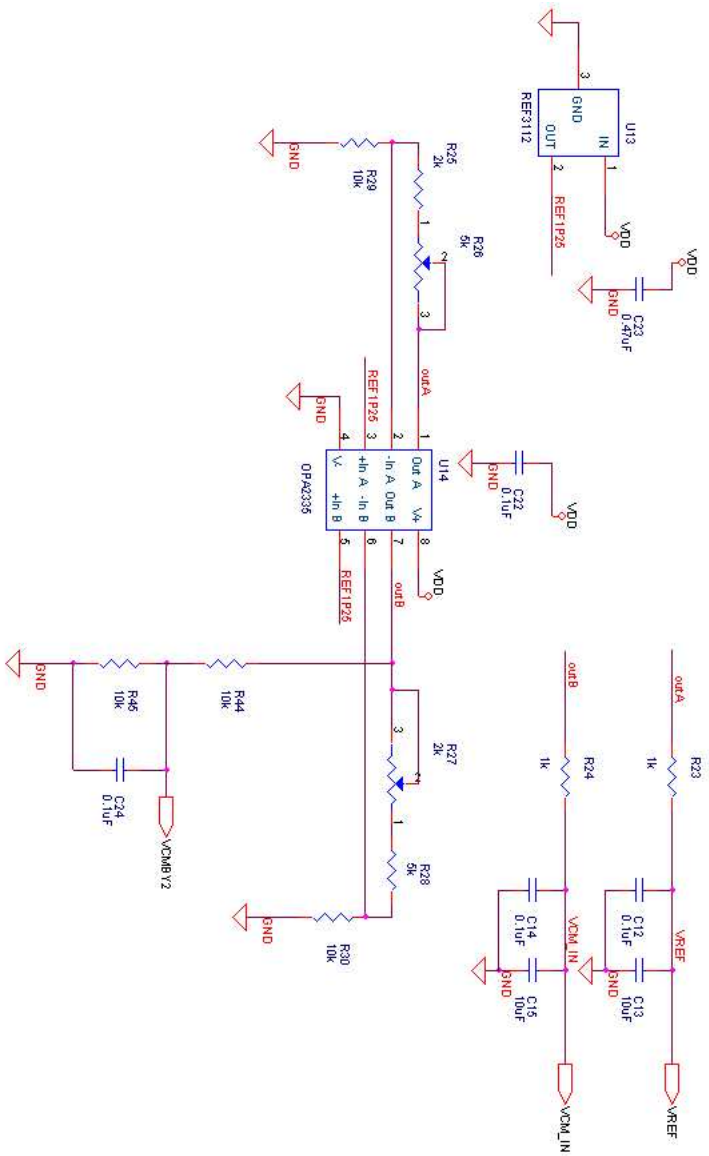


Figure 12.7: Schematic of the portion of the board where references are generated.

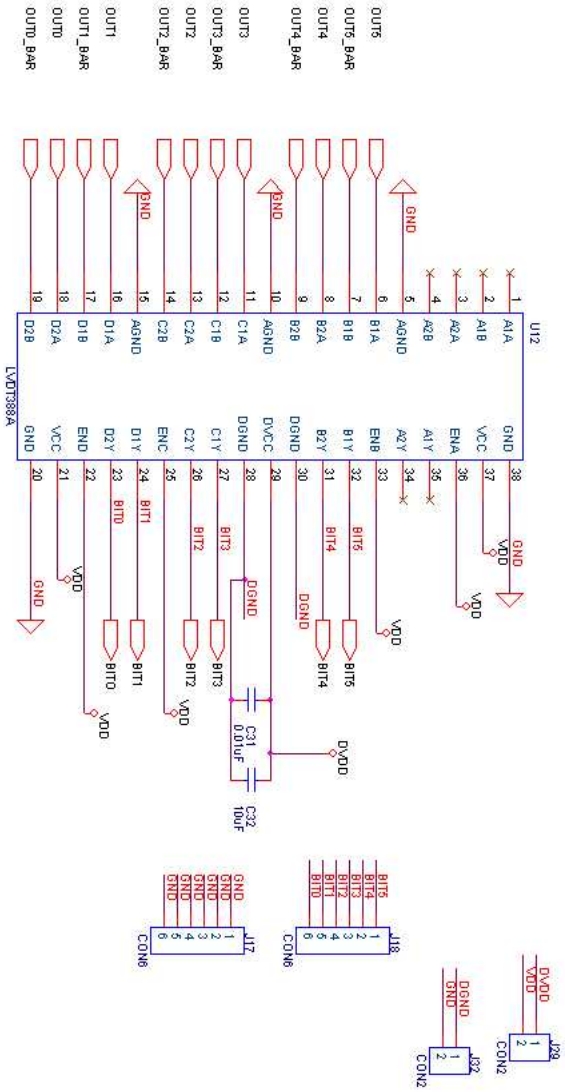


Figure 12.8: Schematic of the portion of the board showing the LVDS receiver.

## 12.3 SCHEMATIC OF THE BOARD

The schematic of the board is split into three portions for ease of representation. The three portions are as shown in Figure 12.6, Figure 12.7 and Figure 12.8. Figure 12.6 shows the portion of the board which has the ADC, the circuit for giving stimuklus to the ADC and the current refernces. In Figure 12.7 the portion of the board where the voltage references are generated is shown. Figure 12.8 shows the LVDS receiver which gives the final digital bits.

# CHAPTER 13

# EXPERIMENTAL RESULTS

## 13.1 DIE PHOTO

The flash ADC was fabricated in a 0.35 $\mu$m CMOS process through AMS (Austria Micro Systems). The active area is 0.8 mm$^2$. The micro-photograph of the chip is shown in Fig. 13.1, where the major blocks of the ADC are marked. The die is mounted in a 40 pin Dual Inline Package (DIP). The test chip also consists of a 6-bit current steering test-DAC to aid debug. Digital output drivers are of the LVDS type. The nominal full-scale input range is chosen to be 3.4 $V_{pp,diff}$. Such large signal levels are possible, thanks to the distortion correction technique proposed. A preliminary version of the ADC was attempted as reported in [16][17]. The ADC was targetted to work at 100 MHz. This did not function as expected because of some design and layout flaws.

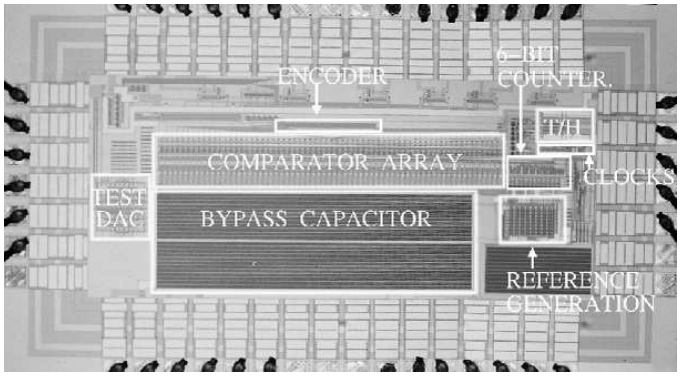


Figure 13.1: Chip microphotograph.

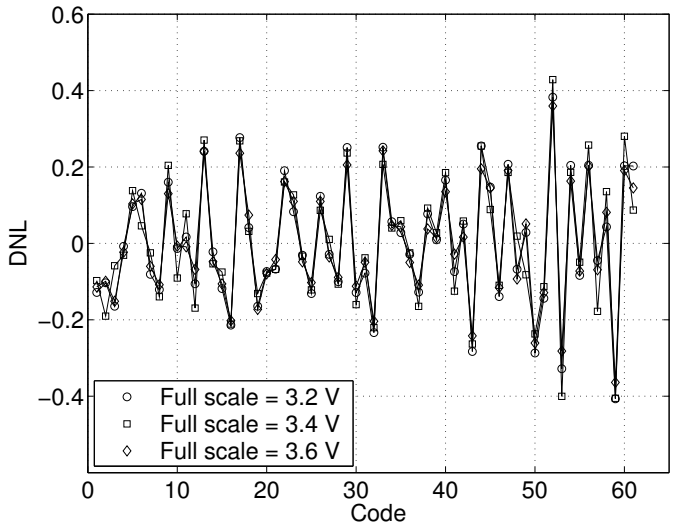


Figure 13.2: DNL of the ADC for different full scale input ranges.

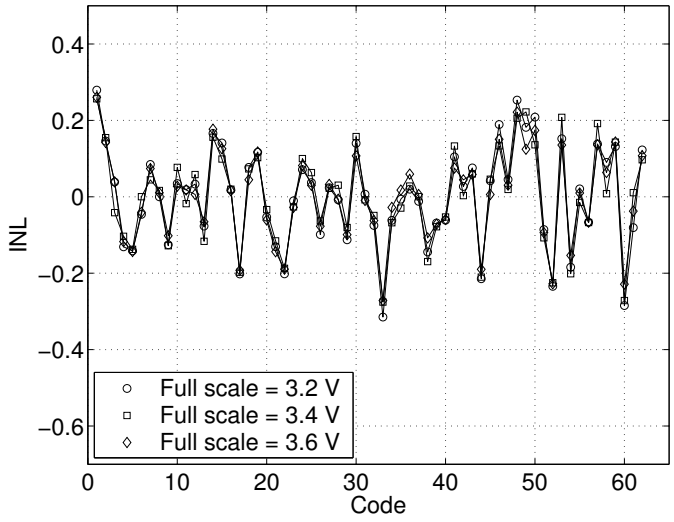


Figure 13.3: INL of the ADC for different full scale input ranges.

## 13.2 DC MEASUREMENTS

The DC characteristics of the ADC were measured using a 16-bit Data Acquisition Card. The DNL plots of the ADC for different LSB sizes are shown in Fig. 13.2. The maximum DNL is 0.52 LSB, occurring when the LSB size is the smallest. The ADC INL plots are shown in Fig. 13.3 for different full scale input ranges. One can notice that the INL does not vary significantly with the full scale input range of the converter owing to distortion cancellation scheme.

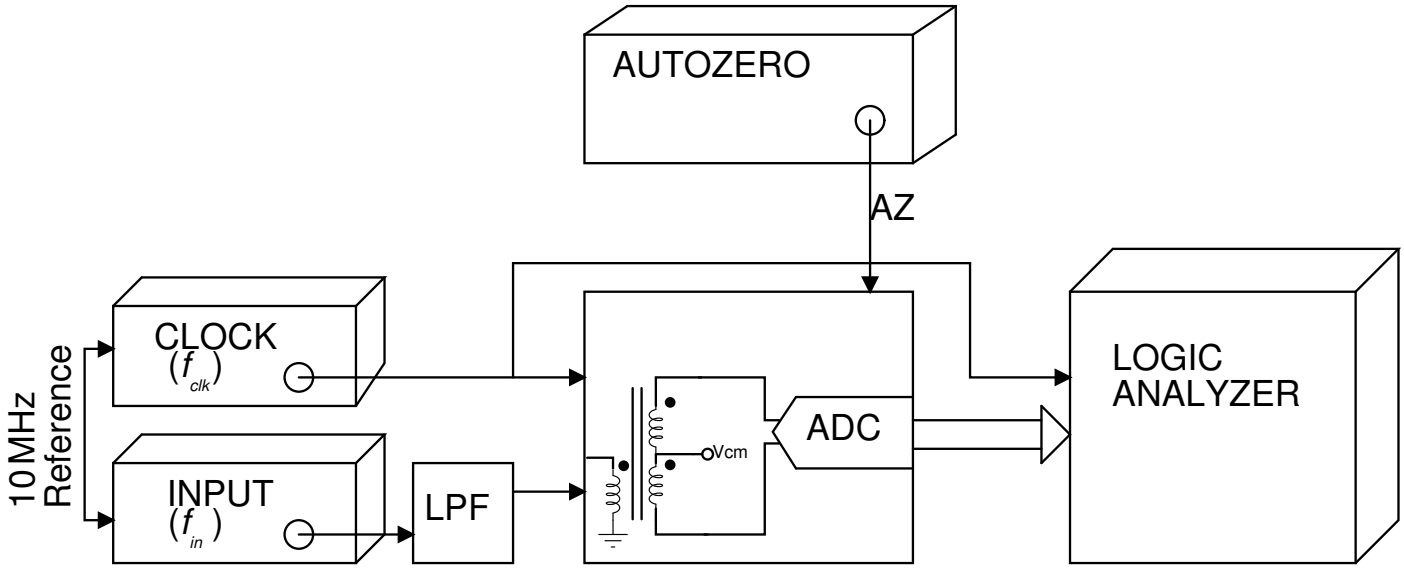


Figure 13.4: Test setup for measuring the dynamic performance.

### 13.3 DYNAMIC MEASUREMENTS

The test setup for measuring the dynamic performance of the ADC is as shown in Figure 13.4. The input sine wave and the clock signal are generated by synchronized RF signal sources. The input is filtered using a passive lowpass filter in order to remove harmonics. The THD of the filtered input sine wave is typically about 50 dB. The LVDS digital outputs are converted into CMOS levels on the board using a commercially available LVDS receiver chip. The CMOS outputs are captured by a logic analyzer and transferred to a computer for FFT computation.

Figure 13.5 shows the output spectrum of the ADC for an input frequency of 19.9 MHz and a clock frequency of 160 MHz. The SNDR of the ADC with the input signal frequency varying for two different clock speeds is as shown in Figure 13.6. From the plot we can deduce that we get a 5.8-bit performance at Nyquist rate for a clock speed of 100 MHz. The ADC gives 5.3 effective number of bits at Nyquist rate for a clock speed of 160 MHz. The dashed lines in Figure 13.6 indicate the SNDR of the ADC when the background autozeroing is taking place continuously.

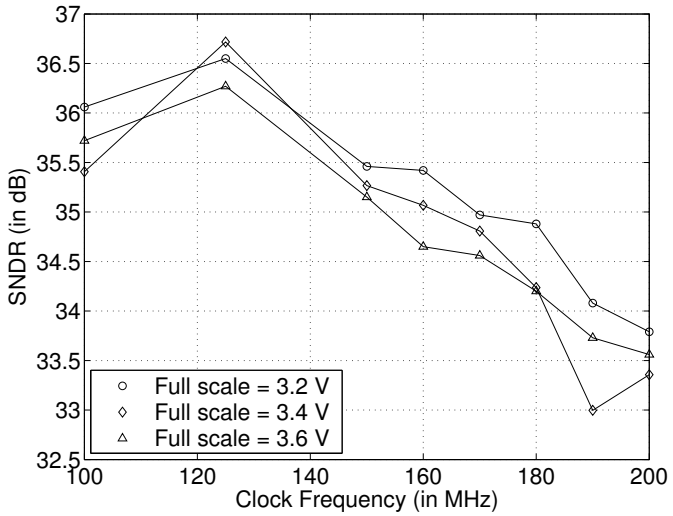


Figure 13.5: Normalized output spectrum of the ADC

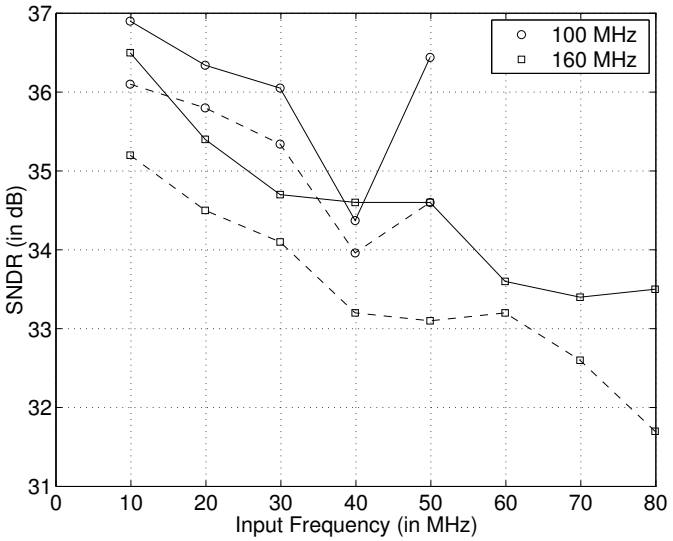


Figure 13.6: SNDR versus input frequency for two different sampling frequencies with and without continuous background autozero.

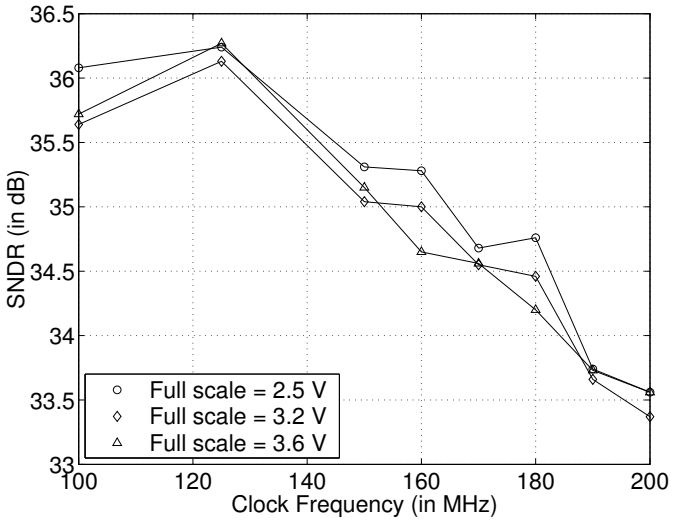


Figure 13.7: SNDR versus clock frequency for three different full scale input ranges of the ADC.

Under these circumstances the SNDR degrades by not more than 1.8 dB across all input frequencies. The measured degradation in SNDR because of the continuous autozero is not far from the calculated value of 1.5 dB.

Figure 13.7 shows the variation of SNDR with the sampling frequency for three different full scale input ranges of the converter. For this measurement, the input frequency is set to 49.9 MHz. We observe that the SNDR does not vary much across the variation in full scale input of the converter due to the distortion cancellation scheme employed in the ADC. The performance of the ADC is summarized in Table 13.1.

## 13.4 BACKGROUND AUTOZERO

The 6-bit counter that is used for background autozeroing can be controlled using an external control voltage. An experiment was done in which the background autozeroing was done continuously and then the autozeroing is not done for a long time. The SNDR of the ADC output was calculated just before the beginning

Table 13.1: Summary of ADC performance.

| | |
|---|---|
| Resolution | 6 bits |
| Technology | 0.35-$\mu$m CMOS 2P4M |
| Supply voltage | 3.3 V |
| Nominal input range | 3.4 $V_{pp}$ differential |
| DNL | 0.43 LSB |
| INL | 0.32 LSB |
| SNDR | 36.0 dB @$f_{in}$ =49.9 MHz, $f_s$ =100 MHz<br>33.6 dB @$f_{in}$ =79.9 MHz, $f_s$ =160 MHz |
| Power consumption | 50 mW @ $f_s$ =160 MHz |
| Active Area | 2.0×0.4 mm$^2$ |
| Chip package | DIP40 |

Table 13.2: SNDR for various input frequencies and signal swings for a supply voltage of 3.3 V , $Vcmin = 1.8$ V and $f_{clock} = 100$ MHz.

| $f_{in}(inMHz)$ | $V_{ref}(inV)$ | SNDR (in dB) | SFDR (in dB) |
|---|---|---|---|
| 9.9 | 1.5 | 36.8 | 49.9 |
| | 1.6 | 37.4 | 52.2 |
| | 1.8 | 37.7 | 52.2 |
| | 2.0 | 37.7 | 52.7 |
| 19.9 | 1.5 | 37.1 | 50.9 |
| | 1.6 | 36.9 | 49.5 |
| | 1.8 | 36.9 | 49.5 |
| | 2.0 | 37.7 | 51.2 |
| 29.9 | 1.5 | 36.7 | 49.3 |
| | 1.6 | 36.9 | 51.9 |
| | 1.8 | 36.4 | 50.1 |
| | 2.0 | 37.2 | 51.7 |
| 39.9 | 1.5 | 36.1 | 45.9 |
| | 1.6 | 36.3 | 47.8 |
| | 1.8 | 36.8 | 47.1 |
| | 2.0 | 37.1 | 47.2 |
| 49.9 | 1.5 | 33.9 | 41.4 |
| | 1.6 | 35.4 | 43.1 |
| | 1.8 | 34.1 | 40.5 |
| | 2.0 | 35.5 | 45.7 |

Table 13.3: SNDR for various input frequencies and signal swings for a supply voltage of 3.3 V , $Vcmin = 1.8$ V and $f_{clock} = 160$ MHz.

| $f_{in}(inMHz)$ | $V_{ref}(inV)$ | SNDR (in dB) | SFDR (in dB) |
|---|---|---|---|
| 9.9 | 1.5 | 36.2 | 50.7 |
| | 1.6 | 36.7 | 50.4 |
| | 1.8 | 37.1 | 49.9 |
| | 2.0 | 37.5 | 52.7 |
| 19.9 | 1.5 | 36.5 | 49.9 |
| | 1.6 | 36.6 | 51.3 |
| | 1.8 | 36.9 | 51.9 |
| | 2.0 | 37.1 | 52.4 |
| 29.9 | 1.5 | 36.2 | 47.4 |
| | 1.6 | 36.2 | 48.1 |
| | 1.8 | 36.6 | 47.2 |
| | 2.0 | 36.9 | 49.0 |
| 39.9 | 1.5 | 35.8 | 45.4 |
| | 1.6 | 36.0 | 48.3 |
| | 1.8 | 36.0 | 44.4 |
| | 2.0 | 36.1 | 45.5 |
| 49.9 | 1.5 | 34.1 | 38.9 |
| | 1.6 | 35.8 | 46.5 |
| | 1.8 | 34.6 | 40.4 |
| | 2.0 | 35.5 | 41.2 |
| 59.9 | 1.5 | 35.6 | 47.4 |
| | 1.6 | 34.7 | 43.6 |
| | 1.8 | 34.6 | 40.3 |
| | 2.0 | 34.7 | 39.1 |
| 69.9 | 1.5 | 34.5 | 45.1 |
| | 1.6 | 34.5 | 40.5 |
| | 1.8 | 32.5 | 36.4 |
| | 2.0 | 32.5 | 33.7 |
| 79.9 | 1.5 | 34.2 | 39.3 |
| | 1.6 | 33.7 | 37.4 |
| | 1.8 | 32.0 | 33.4 |
| | 2.0 | 31.9 | 32.8 |

Table 13.4: SNDR for various clock frequencies and signal swings for a supply voltage of 3.3 V , $Vcmin = 1.8$ V and $f_{in} = 49.9$ MHz.

| $f_{clock}(inMHz)$ | $V_{ref}(inV)$ | SNDR (in dB) | SFDR (in dB) |
|---|---|---|---|
| 100 | 1.5 | 36.1 | 48.1 |
| | 1.6 | 35.8 | 43.8 |
| | 1.8 | 35.6 | 45.0 |
| | 2.0 | 34.9 | 45.6 |
| 125 | 1.5 | 36.2 | 48.7 |
| | 1.6 | 36.1 | 49.1 |
| | 1.8 | 36.1 | 46.5 |
| | 2.0 | 35.5 | 45.2 |
| 150 | 1.5 | 35.3 | 46.0 |
| | 1.6 | 35.2 | 44.6 |
| | 1.8 | 35.0 | 43.8 |
| | 2.0 | 34.3 | 42.8 |
| 160 | 1.5 | 35.3 | 46.1 |
| | 1.6 | 35.0 | 43.9 |
| | 1.8 | 35.0 | 43.8 |
| | 2.0 | 33.8 | 41.4 |
| 170 | 1.5 | 34.7 | 42.7 |
| | 1.6 | 34.9 | 42.5 |
| | 1.8 | 34.6 | 42.6 |
| | 2.0 | 33.8 | 41.0 |
| 180 | 1.5 | 34.8 | 43.5 |
| | 1.6 | 34.3 | 42.2 |
| | 1.8 | 34.5 | 42.2 |
| | 2.0 | 33.4 | 40.6 |
| 190 | 1.5 | 33.7 | 43.0 |
| | 1.6 | 33.3 | 39.7 |
| | 1.8 | 33.7 | 41.8 |
| | 2.0 | 32.9 | 39.5 |
| 200 | 1.5 | 33.6 | 41.1 |
| | 1.6 | 33.9 | 41.3 |
| | 1.8 | 33.4 | 39.6 |
| | 2.0 | 32.8 | 39.7 |

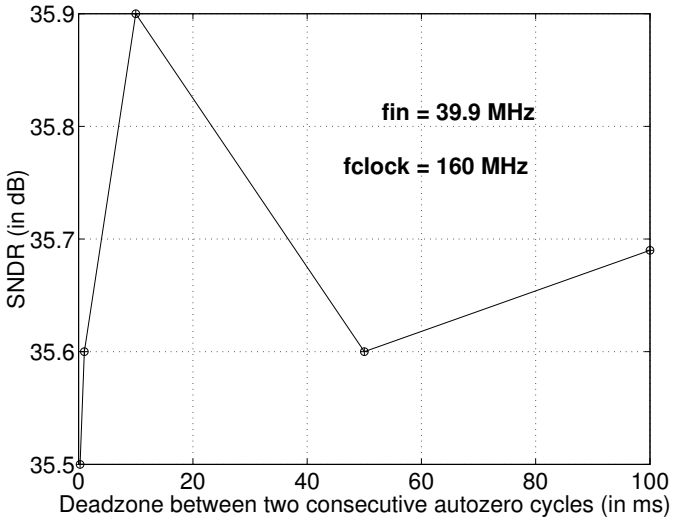


Figure 13.8: SNDR versus deadzone duration between two consecutive autozero cycles.

of the next autozero cycle. This experiment will give us an indication of how long the references are valid if no autozeroing is done in the background for a long time. Figure 13.8 shows the variation of SNDR with increasing period between the consecutive autozero cycles for an input frequency of 39.9 MHz and a clock frequency of 160 MHz. From this plot one can infer that even if the the autozeroing is done once in every 100 ms the SNDR degrades by only a negligible amount.

## 13.5 COMPARISON WITH EARLIER WORKS

Table 13.5 compares the present ADC performance with earlier published works which were reported in 0.35-$\mu$m CMOS process. The ENOB's are quoted at the Nyquist frequency. To make a fair comparison among the different ADC's we normalize the signal bandwidth and the effective number of bits (ENOB) by the following expression [18]:

$$\text{Energy}/(\text{conversion\_step}) = \frac{P_{diss}}{2^{ENOB} \times f_{samp}}$$

The proposed ADC has a lesser Energy/conv_step when compared to other ADC's owing to the distortion compensation scheme. This can further be reduced if one

Table 13.5: Comparison with published works.

| Paper | ENOB | Active area (in $mm^2$) | Energy/conv_step (in pJ) |
|---|---|---|---|
| [2] | 5.0 | 1.2 | 14.84 |
| [5] | 5.5 | 0.8 | 11.00 |
| [9] | 5.1 | 0.8 | 21.86 |
| This work | 5.3 | 0.8 | 7.93 |

uses a lower supply voltage for the digital circuits.

# CHAPTER 14

# CONCLUSIONS

## 14.1 CONCLUSION

A technique to correct for the static nonlinearity of the front-end track & hold in a flash ADC was proposed. This enables the use of larger signal swings than were otherwise possible, resulting in power reduction in all the ADC building blocks. In a 3.3 V supply, a peak-to-peak differential input swing of 3.6 V was possible, thanks to distortion compensation. The implementation of the distortion canceling principle was merged with background comparator offset correction. Measurement results for a 6-bit 100 Msps flash ADC were presented. The measured results show that the ADC gives an ENOB (effective number of bits) of 6 at a clock speed of 100 MHz and an ENOB of 5.3 at a clock speed of 160 MHz. The energy per converter step for this ADC is the lowest when compared to the previous published works in the same technology which was possible by the distortion cancellation scheme.

## 14.2 SCOPE FOR FUTURE WORK

The present architecture can be extended to folding architecture with minimal changes in the layout. A time interleaved track and hold can be used to increase the speed of operation.

# APPENDIX A

The following is the MATLAB code written to find the loss in SNR because of continuous background autozero taking place in the ADC.

```
clear all;
close all;
l=6;%no. of bits for quantization
N=2^l; %no. of quantization levels
A=1;
Ns=1e3;%no. of samples
%X=A*rand(1,Ns);
vref([1:N-1])=linspace(A/N,A-A/N,N-1);
X=A/(2)+A/(2)*sin([1:Ns]);     % Sinusoidal input
%X=A*rand(1,Ns);               % Uniformly distributed input
SQNRv=[];Evarv=[];
for i=1:1:length(X),
vref([1:N-1])=linspace(A/N,A-A/N,N-1);
r=rand(1,1);
a=rem(i,N); %The autozeroing takes place after every 64 cycles
if ((a~=0)&(r(1)<0.5)) vref(a)=0;
elseif ((a~=0)&(r(1)>0.5)) vref(a)=A; end

            for j=1:1:N-1,
if (X(i)>=vref(j)) c_out(j)=1; else c_out(j)=0; end
% c_out is comparator output
            end
   c_out([1:N-1])=0;
            n=find((X(i)-vref)>0);
            c_out(n)=1;
     ml_out(1)=(1&c_out(1))|(1&c_out(2));
     %ml_out is majority logic output
     ml_out(1)=ml_out(1)|(c_out(1)&c_out(2));

ml_out([2:N-2])=bitand(c_out([1:N-3]),c_out([2:N-2]));
 maj1=bitand(c_out([2:N-2]),c_out([3:N-1]));
 ml_out([2:N-2])=bitor(ml_out([2:N-2]),maj1);
 maj2=bitand(c_out([1:N-3]),c_out([3:N-1]));
ml_out([2:N-2])=bitor(ml_out([2:N-2]),maj2) ;
```

```
    ml_out(N-1)=bitand(c_out(N-2),c_out(N-1));
    vref([1:N-1])=linspace(A/N,A-A/N,N-1);
  if (sum(ml_out)==0) Xq(i)=0;else Xq(i)=vref(sum(ml_out)) ; end;
end
eq=Xq-X;
Svar=var(X);
Evar=var(eq);
SQNR=10*log10(Svar/Evar); %SNR with continuous autozeroing
Loss=10*log10(12*2^(2*l)*mean(Evar))      % Penalty in SNR
```

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1. Venkata Srinivas, Shanthi Pavan, Ashish Lachhwani and Lingam Sasidhar, " A Distortion Compensating Flash Analog to Digital Converter Technique," communicated to *IEEE Journal of Solid-State Circuits*.

# CURRICULUM VITAE

1. **Name** **V.V.Srinivas**

2. **Date of Birth** $2^{nd}$ Dec, 1979

3. **Permanent Address :** Street No.12,
   D.No:9-6-133, Yadagiri Nagar, Saidabad(P.O),
   Hyderabad. 500059.

4. **Present Address:** Room No.3021,
   Cauvery Hostel, IITMadras, Chennai. 600036.
   Phone : 9841247575

5. **Educational Qualifications**

| Qualification | Institution | Year | Marks obtained |
|---|---|---|---|
| B.Tech | IITMadras, Chennai | 2001 | $\frac{7.73}{10}$ |
| Intermediate | LFJC, Hyderabad | 1997 | $\frac{914}{1000}$ |
| SSC | Vidya Dayini Model High School | 1995 | $\frac{529}{600}$ |

# GENERAL TESTING COMMITTEE

The GTC members are

1. Dr.Y.Shanthi Pavan (Guide)
2. Dr.B.Srikrishna
3. Dr.A.Meher Prasad