Design of a 16-bit Continuous Time Delta-Sigma Modulator for Digital Audio

A Project Report

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RAMALINGAM PANDARINATHAN

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CERTIFICATE

This is to certify that the report titled **Design of a 16-bit Continuous Time Delta-Sigma Modulator for Digital Audio**, submitted by **Ramalingam Pandarinathan**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Y. Shanthi Pavan
Advisor,
Assistant Professor,
Dept. of Electrical Engineering,
IIT-Madras, 600 036

Dr. Nagendra Krishnapura
Co-Advisor,
Assistant Professor,
Dept. of Electrical Engineering,
IIT-Madras, 600 036

Place: Chennai
Date: 28 June 2006

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ABSTRACT

The project involves the design of a continuous-time delta-sigma modulator for analog-to-digital conversion. The primary motivation for building continuous-time delta-sigma converters is that the requirements on the anti-aliasing filter are greatly reduced in comparison to their discrete-time counterparts. The proposed third order modulator is operated at 3.072MHz and is intended for high-fidelity audio applications. It employs a 4-bit internal quantizer and targets a resolution of 16-bits for a signal bandwidth of 24KHz. The modulator's loop filter is implemented with active RC integrators. Dynamic Element Matching is used to eliminate SNDR degradation due to mismatch in DAC elements. Appropriate design techniques are used to make the design robust with respect to process and temperature variations. The design was implemented in 0.18μm CMOS process from UMC. It occupies an area of 0.8mm^2 excluding the bond pads. The design consumes a power of 157μW from a 1.8V supply. The simulated SQNR for the modulator is 106 dB. The design has been sent for fabrication.

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CHAPTER 1

Introduction

1.1 Motivation

With the advent of *system-on-a-chip (SoC)* style of design the emphasis is on integrating all components of an electronic system into a single chip. In this design strategy most of the on-chip signal processing is done in the digital domain. This is because digital signals are less susceptible to corruption by noise and VLSI processes are optimized for high-density digital design. Nevertheless all real world signals are analog and hence data converters are needed to interface with the digital signal processing core. Thus, analog-to-digital converters (ADC) play an important role in SoC style of design.

Any ADC is characterized by its resolution, conversion speed and power consumption. The basic idea is to maximize the first two parameters while minimizing the third. One architecture that is gaining popularity over the years is the delta-sigma ($\Delta\Sigma$) modulator. These modulators are used in applications where it is required to get high resolutions at lower conversion speeds. One such application is high-fidelity audio. $\Delta\Sigma$ ADC's are the preferred choice for high resolution low power converters operating at low speeds.

Most of the $\Delta\Sigma$ ADC's have been built using discrete-time (DT) circuitry. The speed of these converters depends on the settling time of the circuit waveforms. One way of getting around this limitation is to use continuous-time (CT) circuitry in place of DT. In practice CT $\Delta\Sigma$ modulators do operate at higher speeds but achieve lower resolution than their lower speed counterparts.

In this thesis the design of a low power high resolution CT $\Delta\Sigma$ modulator is presented. The modulator is designed for digital audio applications. The thesis discusses the theory and design of the building blocks of the modulator.

1.2 Organization

Chapter 2 introduces the concept of $\Delta\Sigma$ modulators, various ways of designing the modulator, measuring its performance and the equivalence between a CT and a DT modulator.

Chapter 3 discusses the important issues related to the design of a $\Delta\Sigma$ modulator.

Chapter 4 explains the design of the loop filter which plays a major role in achieving the converter's high resolution.

Chapter 5 presents the design of a 4-bit flash ADC which consumes almost zero static power.

Chapter 6 gives the design of the internal resistive DAC which should have the resolution of the overall converter.

Chapter 7 deals with the generation of reference voltage for the flash and DAC and the bias current for the loop filter op amps.

Chapter 8 concludes the thesis with the simulation results.

CHAPTER 2

$\Delta\Sigma$ Modulator Concepts

In this chapter we discuss what a delta-sigma modulator is and how it converts an analog signal into a digital one. We also discuss the various design choices in $\Delta\Sigma$ modulator design and how the performance of a $\Delta\Sigma$ modulator is measured.

2.1 A Brief Introduction to $\Delta\Sigma$ Modulator

This section provides a brief overview of the $\Delta\Sigma$ modulator concepts.

2.1.1 Operating Principles

Figure 2.1 shows the basic architecture of a $\Delta\Sigma$ ADC. The important blocks of the $\Delta\Sigma$ modulator are:

1. Loop filter H(z)
2. Clocked quantizer and
3. Digital to analog converter (DAC)

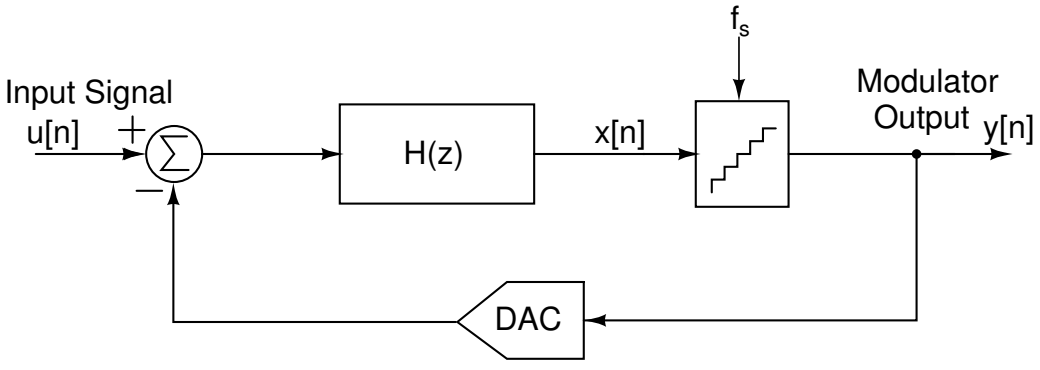


Figure 2.1: Block Diagram of a $\Delta\Sigma$ Modulator

The basic architecture is analogous to an amplifier that is realized using an op amp and negative feedback. In this analogy, the negative feedback reduces

the effect of the noise added by the op amp at the output of the amplifier at low frequencies where the op amp gain is high. At high frequencies the op amp gain is low and hence the noise is not reduced. Thus, an analog input signal is modulated into a digital sequence whose spectrum approximates the analog input in a narrow frequency range.

For the system shown in figure 2.1 the quantizer is the only non-linear element. A linear model for the system is shown in figure 2.2 where the quantizer is replaced by an adder. We assume that the adder has two *independent* inputs. The quantization noise added by the quantizer is denoted as e[n] and it is assumed that it is independent of the input signal u[n].

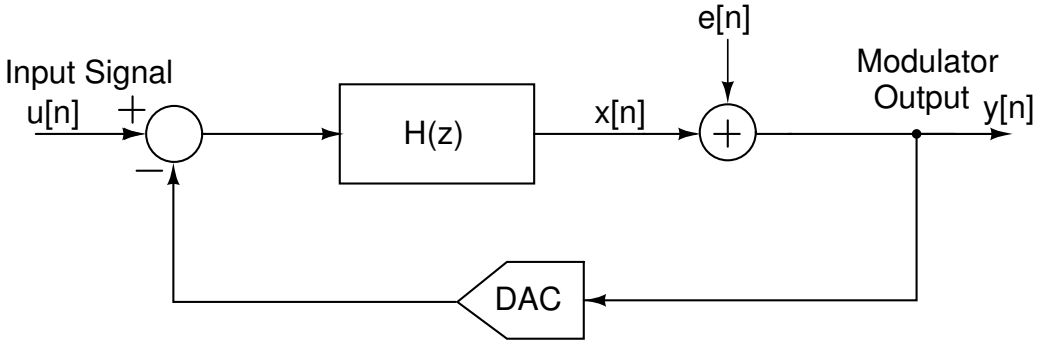


Figure 2.2: Linear model of the Modulator

The output of the modulator y can be written as:

$$Y(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{2.1}$$

$$= STF(z)U(z) + NTF(z)E(z) \tag{2.2}$$

where STF(z) and NTF(z) are the signal transfer function and noise transfer function respectively. From equation (2.1) we see that the zeros of NTF(z) are equal to the poles of H(z). The loop filter H(z) has a large magnitude in the frequency band of interest. As a result STF(z) will approximately be unity over the frequency band of interest and the output will resemble the input very closely at these frequencies. Also NTF(z) will approximately be zero over the same frequency band. Thus, the quantization noise is reduced within the band of interest.

For a first order $\Delta\Sigma$ modulator H(z) is a simple discrete time integrator i.e.

$H(z) = 1/(z-1)$. Now from equation (1.1)

$$STF(z) = z^{-1}, NTF(z) = 1 - z^{-1} \tag{2.3}$$

Since H(z) $\rightarrow \infty$ at dc, input signals around dc will be reproduced faithfully at the output. The signal transfer function is simply a delay, while the noise transfer function is a discrete time high pass filter. Since NTF(z) has a high pass response the quantization noise is "shaped away" from low frequencies.

The modulator minimizes the quantization noise in a bandwidth much smaller than the sampling frequency f_s. To obtain a higher resolution from the converter the signal must be bandlimited to a value much smaller than f_s. This is achieved by sampling the signal at frequencies much higher than the Nyquist rate i.e. $f_s >> f_N$. Hence, $\Delta\Sigma$ modulators are also called *oversampling converters* and the *oversampling ratio* of the converter is defined as:

$$OSR = \frac{f_s}{f_N} \tag{2.4}$$

2.2 Design Choices

There are many design choices for $\Delta\Sigma$ modulators.The major ones are described here.

2.2.1 Order of H(z) and Oversampling Ratio

The order of the loop filter is the maximum power of z in the denominator polynomial of H(z). The loop filter H(z) can have an order of two, three or even higher. A loop filter of order m is built as a cascade connection of m integrators with feedforward and feedback co-efficients as shown in figure 2.3.

For a signal that is bandlimited to f_0 the minimum sampling rate is the Nyquist rate f_N which is twice the signal bandwidth. Sampling at a rate much higher than the Nyquist rate is advantageous because for every doubling of the OSR the

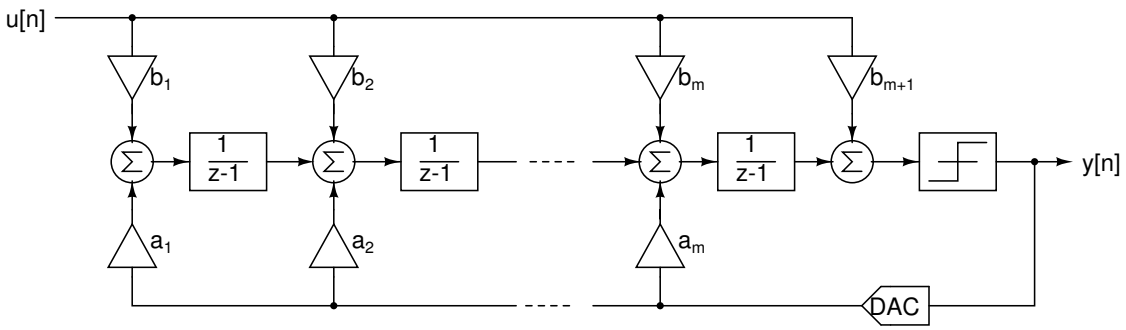


Figure 2.3: General mth order $\Delta\Sigma$ Modulator

quantization noise power in the signal bandwidth reduces by one-half. Hence, an improvement of 3dB/octave of oversampling is obtained. On the other hand for a mth order $\Delta\Sigma$ modulator an improvement of $6m+3$dB/octave is obtained because of its noise shaping property. This can be derived as follows:

The noise transfer function of a m-th order modulator is:

$$NTF(z) = (1 - z^{-1})^m \tag{2.5}$$

The magnitude of the noise transfer function is found by letting $z = e^{j\omega T} = e^{j2\pi f/f_s}$ and is given by:

$$|NTF(f)| = 2^m sin^m(\frac{\pi f}{f_s}) \tag{2.6}$$

Let Δ be the step size of the quantizer.
The quantization noise power of the modulator over the frequency band from 0 to f_0 is given by:

$$P_e = \frac{\Delta^2}{12 f_s} \int_{-f_0}^{f_0} |N_{TF}|^2 \, \mathrm{d}f \tag{2.7}$$

$$= \frac{\Delta^2}{12 f_s} \int_{-f_0}^{f_0} 2^{2m} sin^{2m}(\frac{\pi f}{f_s}) \, \mathrm{d}f \tag{2.8}$$

Assuming that $f_s \gg f_0$ i.e. OSR$\gg$1, $sin((\pi f)/f_s)$ can be approximated as $(\pi f)/f_s$,

we have

$$P_e = \frac{\Delta^2}{12}\frac{\pi^{2m}}{2m+1}(\frac{2f_0}{f_s})^{2m+1} \tag{2.9}$$

$$= \frac{\Delta^2}{12}\frac{\pi^{2m}}{2m+1}(\frac{1}{OSR})^{2m+1} \tag{2.10}$$

Doubling the OSR of a modulator employing m-th order noise shaping reduces the quantization noise power within the signal bandwidth by:

$$10(2m+1)\log 2\, dB/octave = 6m + 3\, dB/octave \tag{2.11}$$

This is equivalent to a gain of m+1.5 bits/octave.

Using a higher order modulator has its own drawbacks. A system with order of H(z) greater than 2 is conditionally stable. Input signals close to the full scale can cause overloading of the quantizer. Infact, the input signal needs to be significantly smaller than the bounds of the quantizer output levels to keep the modulator stable. Overloading the quantizer reduces the dynamic range of the converter. The placement of poles and zeros of H(z) is also critical for higher order modulators. The architecture of the modulator and the technology in which it is implemented will place a limit on the maximum possible sampling frequency and hence, the OSR.

2.2.2 Quantizer Resolution

It is possible to replace the single-bit quantizer of figure 2.3 with a multibit quantizer. Multi-bit quantizers offer the following advantages:

1. For a fixed full-scale, the quantization error reduces by 6dB for every bit added to the resolution of the quantizer.

2. It improves the stability of higher order modulators. Due to improved stability the NTF can be chosen more aggressively. Hence, better SNR can be obtained.

3. Since the DAC input to the loop filter changes less from sample to sample, the required slew rate of the input op amp of the loop filter is reduced. This in turn lowers power dissipation.

4. Non-idealities in the quantizer do not degrade the system performance much because the quantizer is preceded by several high gain integrators. As a result the input referred error is small.

The drawbacks of using a multi-bit quantizer are the increase in complexity of the quantizer and the non-idealities in the feedback DAC. Any non-ideality in the feedback DAC is directly referred to the input. So a small error in one DAC level corrupts the converter performance greatly. Hence, it becomes necessary to compensate for multibit DAC errors. On the other hand the biggest advantage of single-bit design is that it is inherently linear.

2.2.3 Low pass vs. Band pass

In low-pass oversampling converters, the transfer function H(z) has a high gain near dc, and thus the quantization noise is small around dc. In a bandpass oversampling converter H(z) has a high gain near some frequency f_c. As a result the quantization noise around f_c is small. Most of the quantization noise can be removed through the use of a narrow bandpass filter.

In a second order bandpass oversampling converter with $f_c = f_s/4$, H(z) has its poles at $e^{\pm j\pi/2} = \pm j$. H(z) is thus a resonator that has infinite gain at the frequency $f_s/4$.

OSR for BP converters is defined as half the sampling frequency divided by the bandwidth of interest. Thus, an $f_s/4$ converter with a signal occupying the frequency range $(f_s/4 - f_s/64, f_s/4 + f_s/64)$ has a bandwidth of $f_s/32$, and hence OSR = 16.

2.2.4 Discrete-time vs. Continuous-time

Discrete time $\Delta\Sigma$ modulators are constructed with switched-capacitor(SC) loop filters. SC filters are attractive because they offer good accuracy and good linearity. The difference equations describing a SC circuit are independent of the clocking frequency and hence the transfer function of a SC circuit scales automatically with the clock frequency. The continuous-time loop (CT) loop filters have inferior accuracy, linearity and have large variations in their time constants. The CT loop filter transfer function also does not scale naturally with clock frequency. The CT loop filters require calibration and this calibration is valid only at a single clock frequency.

The CT $\Delta\Sigma$ modulators are increasingly becoming popular due to the following advantages they offer:

1. CT modulators possess *inherent anti-aliasing*. The use of a CT filter postpones the inevitable sampling of the signal, which now takes place at the output of the loop filter. Thus, imperfections of the sampling process and the folding of the wideband noise, both take place at a much less sensitive point in the loop.

   Inherent anti-aliasing simplifies system design by eliminating the anti-alias filter, which typically appears at the input of every other ADC. It improves system performance because it eliminates the noise-folding associated with sampling the incoming signal.

2. The maximum clock rate of a CT modulator is determined by the regeneration time of the quantizer and the update rate of the feedback DAC, whereas in a SC modulator the clock rate is determined by the op amp settling time requirements. In practice, a CT modulator operates with a clock frequency which is 2-4 times greater than that of SC modulators [1].

The above two advantages are driving the development of CT ADC's with bandwidths in the multi-MHz range. These ADC's are geared towards wired and

wireless communications systems.

2.2.5 Single stage vs. Multistage

It is possible to build higher order modulators out of two or more lower order modulators where the later modulator inputs are the *quantization noise* from the previous stages. The advantage of this approach is that since the lower order modulators are more stable, the overall system should remain stable. Such an arrangement has been called MASH(Multi-stAge noise SHaping) [2].

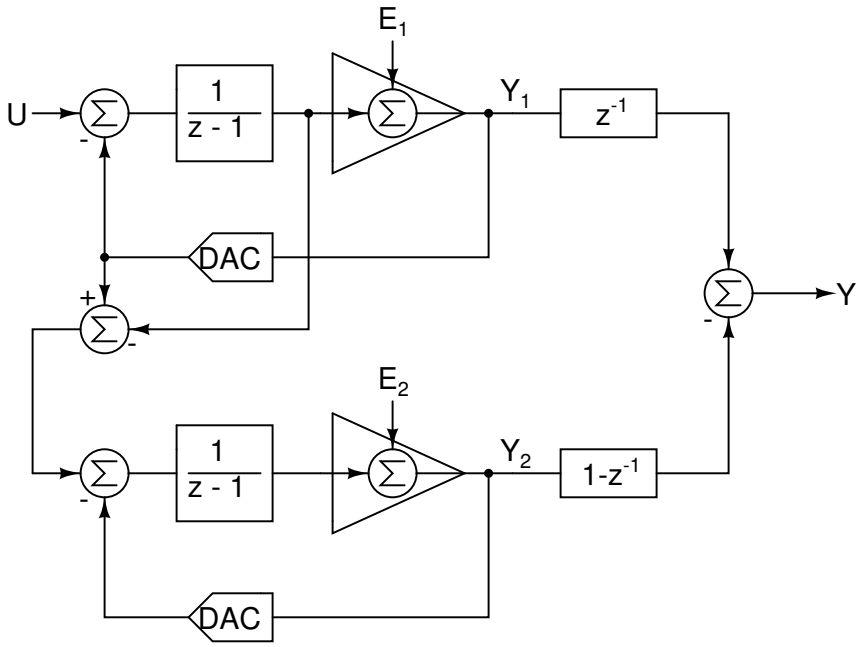


Figure 2.4: A multistage $\Delta\Sigma$ modulator

The arrangement for realizing a second order modulator is shown in figure 2.4 where a first order modulator's quantization noise is shaped by another first-order modulator:

$$Y_1 = z^{-1}U + (1 - z^{-1})E_1 \tag{2.12}$$

$$Y_2 = z^{-1}E_1 + (1 - z^{-1})E_2 \tag{2.13}$$

The second modulator's output is differentiated and added to the output of the

first modulator.

$$Y = z^{-1}Y_1 + Y_2(1 - z^{-1}) \tag{2.14}$$

$$= z^{-2}U - (1 - z^{-1})^2 E_2 \tag{2.15}$$

Thus, a MASH approach has the advantage that higher order noise filtering can be achieved using lower order modulators. In practice, mismatches between the components in the stages result in imperfect noise cancellation. Such mismatches in the above example causes first order noise to leak through from the first modulator and hence reduce dynamic range performance.

2.3 Performance Measures

In this section we explain the various performance measures of a $\Delta\Sigma$ modulator such as signal-to-noise(SNR) ratio and dynamic range(DR) and how to measure them.

2.3.1 Signal to Noise Ratio (SNR)

To find the SNR of a Nyquist rate converter the signal power is divided by the integrated noise power from 0 to $f_N/2$, which is the same frequency as $f_s/2$. For a $\Delta\Sigma$ modulator which is an oversampling converter, the noise is integrated over the bandwidth from 0 to $f_N/2$, which is now $f_s/(2.OSR)$. This is equivalent to saying that the modulator is followed by a low pass filter having brick wall response with a cut-off frequency of $f_N/2$.

2.3.2 Dynamic Range

The dynamic range of the modulator is the range of input amplitudes for which the SNR of the converter is greater than zero.

2.3.3 Maximum SNR and Maximum Stable Amplitude

Maximum SNR is found from the DR plot as the peak of the SNR vs. input tone magnitude curve. A second order $\Delta\Sigma$ modulator is stable for all input tones of amplitude upto 0dB [3]. Higher order modulators become unstable before 0dB is reached. The modulator goes into instability when the output of the final integrator of the loop filter saturates. As a result the quantizer produces a long consecutive sequence of either zero or one at its output. When this happens the signal encoding property of the modulator is lost and its SNR automatically degrades. The maximum stable amplitude (MSA) is the largest input tone amplitude which keeps the output of the final loop-filter integrator bounded. The MSA is the maximum input amplitude for which the modulator SNR is greater than zero.

2.3.4 Spurious Free Dynamic Range

To measure the SFDR of the converter a tone is applied at the input of the ADC and the largest spur between 0 and $f_s/(2(OSR))$ is recorded, where a spur is a tone visible above the noise floor. This process is repeated for all frequencies and phases to determine the worst case spur. Then, SFDR is the largest magnitude difference between between the amplitudes of the input tone and the largest spur in dB, over all input tone amplitudes.

2.4 CT/DT Modulator Equivalence

The quantizer in a CT $\Delta\Sigma$ modulator is clocked. Hence, there is a sampling action that takes place inside the modulator and sampled circuits are DT circuits. As shown in upper left diagram of figure 2.5 the sampling can be made obvious by placing a sampler before the quantizer.

In order to show the equivalence between the CT and DT modulator , the external inputs are set to zero and both loops are opened around the quantizer. This leads to the bottom two diagrams of figure 2.5.

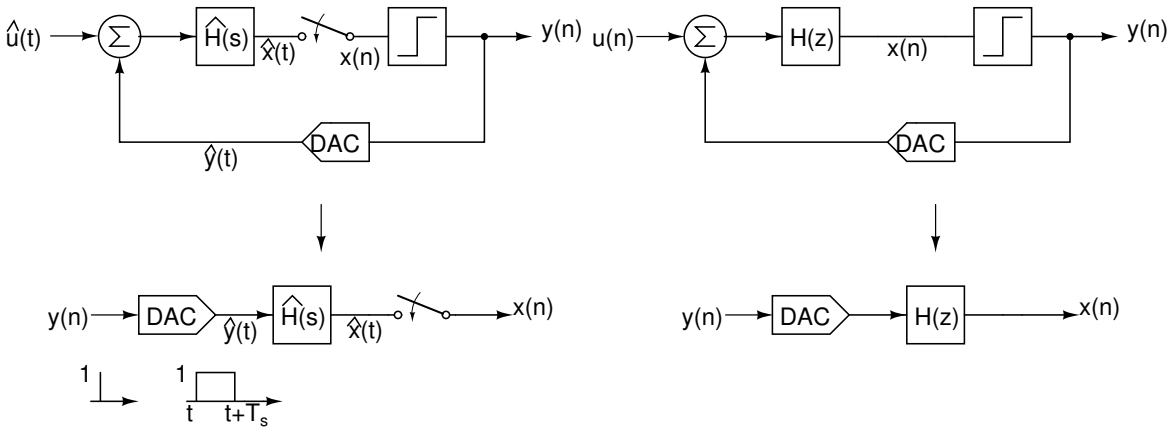


Figure 2.5: Open-loop CT $\Delta\Sigma$ modulator and its DT equivalent

In the CT open-loop diagram, the output of the quantizer is a discrete time quantity. The DAC generates a CT pulse $\hat{y}(t)$ from the output sample y(n) of the quantizer. This pulse is filtered by the CT loop filter to generate $\hat{x}(t)$ which is then sampled to produce the quantizer input x(n). The input and output of the CT and DT open loop configurations are DT quantities. The CT modulator will produce the same sequence of output bits y(n) as the DT modulator if their quantizer have the same inputs at all sampling instants.

$$x(n) = \hat{x}(t)|_{t=nT_s} \tag{2.16}$$

This would be true if the open loop configurations shown in figure 2.5 have the same impulse responses at all sampling times.

$$Z^{-1}\{H(z)\} = L^{-1}\{\hat{R_D}(s)\hat{H}(s)\}|_{t=nT_s} \tag{2.17}$$

where $\hat{R_D}(s)$ is the impulse response of the DAC. Since the CT and DT impulse responses are the same, this transformation is called the impulse-invariance transformation [4].

2.5 Summary

Delta-sigma modulation is a technique of obtaining high resolution conversions by the principle of oversampling, noise shaping.and filtering. The noise from a low resolution quantizer is shaped away from the signal bandwidth and removed later by filtering. The performance of the modulator is determined by taking the spectrum of the output bit stream generated by the internal quantizer. The modulator is characterized by some of the usual ADC performance measures such as DR and SNR. Since there is no one-to-one correspondence between input and output samples and each input sample contributes to a whole train of output pulses, DNL and INL have no meaning in $\Delta\Sigma$ modulators.

CHAPTER 3

Implementation Issues in $\Delta\Sigma$ Modulators

In this chapter we take a brief look at the the effect of various circuit non-idealities that affect the performance of a $\Delta\Sigma$ modulator.

3.1 Op Amps

The loop filter of a $\Delta\Sigma$ modulator is usually built by using op amps that are wired up as integrators. If the op amp deviates from its ideal behaviour, the performance of the modulator becomes worse. We discuss the various problems associated with op amp non-idealities here.

3.1.1 Finite Op Amp Gain

Figure 3.1 shows a first order DT $\Delta\Sigma$ modulator built using switched capacitors(SC).

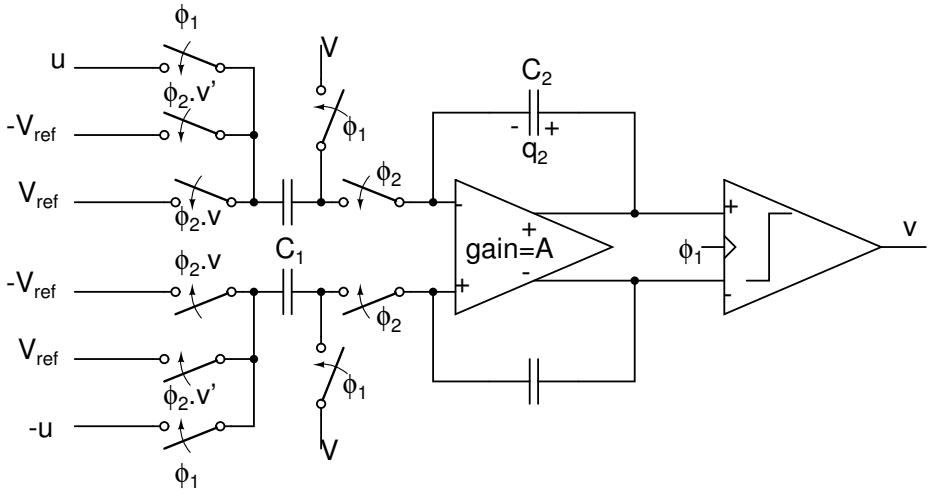


Figure 3.1: SC implementation of a first order $\Delta\Sigma$ Modulator

If the gain of the op amp is A, then the difference equation for the charge $q_2(n)$ on the integrating capacitor C_2 is:

$$q_2(n) = q_2(n-1) + C_1(u(n) - v(n-1) - \frac{q_2(n)}{C_2(1+A)}) \tag{3.1}$$

Assuming that $C_1 = C_2$ and A$\gg$1,the z-transform of the voltage across capacitor C_2 is given by:

$$Y(z) = \frac{zU(z) - V(z)}{z(1+1/A) - 1} \tag{3.2}$$

$$= p\frac{zU(z) - V(z)}{z - p} \tag{3.3}$$

where, p = 1-1/A. The pole has now moved to a frequency that is slightly less than unity. Hence, the integrator is *lossy* or *leaky*. The dc gain of the integrator is no longer infinity. The noise transfer function of the modulator is now:

$$NTF(z) = 1 - pz^{-1} \tag{3.4}$$

The zero of the NTF is now moved off from the unit circle to z = p, inside the unit circle. This changes the gain of the NTF at dc from zero to $1 - p = 1/A$. As a result the attenuation of the quantization noise in the baseband decreases and the SNR degrades. Similar problems do occur in a BP modulator when the resonators have finite Q.

A rule of thumb that is applicable for both CT and DT modulators is that the dc gain of the op amp, $A > OSR$ [5]. This condition ensures that the additional noise that is generated by the finite op amp gain is less than 0.2dB as against that when $A = \infty$ [1]. Higher op amp gain also minimizes the input referred noise of the modulator.

3.1.2 Gain Bandwidth(GBW)

One of the most important parameter for low power $\Delta\Sigma$ modulator is the gain bandwidth of the amplifiers that will realize the loop filter. It can be shown that

the transfer function of a real integrator is:

$$H(s) = \frac{GBW}{s^2.R.C + s(GBW.R.C + 1)} \tag{3.5}$$

In literatures it is suggested that the unity-gain bandwidth of the op amp must be at least an order of magnitude greater than the sampling rate [6].

3.1.3 Finite Slew Rate

In a $\Delta\Sigma$ modulator, the input signal is oversampled. This implies that the input signal is slow compared to the sampling process. Hence, we are more concerned about the slewing of the internal signals, like the output of the loop filter op amps. The phenomenon of slewing is non-linear. As a result input signal harmonics appear in the output spectrum which degrades the SNDR.

3.1.4 Limited Output Swing

A mth order loop filter has m op amps that are connected as integrators. If the integrator op amps do not have sufficiently large output swings, modulator behaviour will be altered. It may lead to clipping of integrator outputs which results in an increased noise floor. In order to avoid clipping of integrator outputs [7], the modulator parameters are scaled so that each integrator gives almost the same peak to peak swing at its output.

3.1.5 Gain Nonlinearity

If the gain of an op amp is not a linear function of its input voltage, then harmonics of large input signals will appear at its output. The gain of the op amp should be made independent of the input signal level as far as possible. The degree of independence is determined by the resolution of the modulator. It is necessary that the first op amp of the loop filter is highly linear because the non-linearities of the later stages get divided by the large gain of the preceding stages when referred

back to the input.

3.2 Mismatch and Tolerance

In a $\Delta\Sigma$ modulator the components in the forward path (e.g loop filter) need not have tolerances better than the overall resolution of the converter. But the DAC in the feedback path needs to have the same degree of matching as the overall resolution of the converter.

3.2.1 Component Mismatch and Tolerance

In a CT $\Delta\Sigma$ modulator the time constant of the RC-integrator is determined by the absolute value of the resistor and capacitor, which can have combined tolerances as high as $\pm 30\%$. This effect can lead to instability of the CT $\Delta\Sigma$ modulators. In order to get around this problem, CT modulators generally have tunable integrating capacitors so that the RC time -constant of the integrator can be set to its nominal value. In a DT modulator, the integrator time constant is the ratio of the switched input capacitor to the integrating capacitor and hence the gain variation is relatively small.

3.2.2 Quantizers

The quantizer in a $\Delta\Sigma$ modulator is preceded by several high gain stages. Hence, any error in the multibit quantizer such as level spacing errors are negligible once they are input referred. The comparator that is used in the quantizer in turn may suffer from problems of hysteresis and metastability. We consider these issues in greater detail in chapter 5.

3.2.3 Multibit DAC Level Mismatch

$\Delta\Sigma$ modulators employing one bit quantizers are relatively popular because they are easy to build and they require an internal DAC with only two levels. A DAC with only two levels is inherently linear. For a modulator that employs multibit internal quantizer the internal DAC also needs to be multibit. Hence, any error in the spacing between the DAC levels will be directly input referred . As a result the noise shaping property of the modulator is lost. This is the reason why the overall resolution of the converter is only as good as the matching across the DAC elements.

The above problem can be circumvented by using the techniques of *dynamic element matching (DEM)* wherein the same output code is represented by a different set of mismatched DAC elements each time. A more detailed discussion on DEM is presented in chapter 6.

3.3 Intrinsic Noise

Intrinsic noise refers to noise that is generated in the device itself as opposed to noise that couples in from an external interfering source. Intrinsic noise cannot be eliminated since it is a property of the device but its value can be altered by proper choice of circuit topology and component sizes. The various sources of intrinsic noise are:

1. In a SC DT $\Delta\Sigma$ modulator the voltage sampled on the input capacitor has an uncertainty kT/C [6] where k is Boltzmann's constant, T is absolute temperature, and C is the sampling capacitor. The value of the sampling capacitor is determined from the resolution of the conveter. For relatively high resolutions large values of sampling capacitors might be necessary which cannot be possibly integrated on-chip.

2. Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. The thermal noise contribution of

the first loop filter op amp needs to be kept small. Since the thermal noise contribution is inversely proportional to g_m of the input differential pair, it can be reduced by proper sizing of the transistors.

3. The MOS flicker noise is also called 1/f noise since it has a spectral density that inversely varies with frequency. The input referred 1/f noise of a $\Delta\Sigma$ modulator is very nearly equal to the input-referred 1/f noise of the op amp in the first integrator. One method for decreasing the 1/f noise is to increase the gate area of MOS transistors of the first op amp that contribute to the op amp noise.

3.4 Clock Jitter

Timing jitter in the quantizer clock degrades the performance of CT $\Delta\Sigma$ modulators. The effect of clock jitter is more severe in CT modulators than DT.

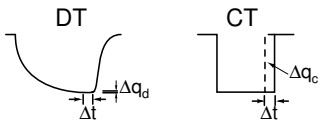


Figure 3.2: Clock jitter effect in DT vs CT design

A typical circuit voltage waveform for a SC DT modulator is shown on the left of figure 3.2. Most of the charge transfer takes place at the beginning of the clock cycle. The amount of charge lost due to timing error is hence relatively small. It is denoted as Δq_d in the figure. The DAC output current of a CT modulator is shown on the right of figure 3.2. The charge is transferred at a constant rate over the clock cycle and hence Δq_c from the same timing error is a relatively larger percentage of the total charge. In a DT design clock jitter can happen only at the input sample and hold and hence only the input waveform is affected. In a CT design the sampling occurs at the input of the quantizer. Thus the jitter affects a signal that is the sum of the input and the quantization noise - a signal with more power than the input. Hence, CT $\Delta\Sigma$ modulators are more sensitive to clock

jitter than their DT counterparts. For a detailed discussion on clock jitter refer to Chapter 5 of [8].

3.5 Excess Loop Delay

Excess loop delay is a problem encountered in CT $\Delta\Sigma$ modulators. It is the delay between the arrival of the sampling clock and the change in the outbit bit as seen at the feedback point in the modulator. Ideally, the DAC current responds instantaneously to the sampling clock pulse. In practice though, the transistors in the latch and the quantizer have non-zero switching times. Hence, there is a delay between the quantizer clock and current pulse at the DAC output. This delay is called excess loop delay. It is significant because it affects the equivalence between the CT and DT representation of the loop filter $\hat{H}(s)$ and H(z). Excess loop delay increases the in-band noise of the modulator and also decreases the maximum stable input amplitude [8]. Hence, the dynamic range of the converter is also reduced.

The $\Delta\Sigma$ modulator is analogous to an amplifier realized using an op amp with feedback. In this analogy the amplifier's second pole is due to the loop delay. Ideally we would like the loop delay to be zero which would place the second pole at ∞. Greater the separation between the first and the second pole of the closed loop system higher is the stability. Now, as the loop delay increases the associated second pole starts moving closer to the first pole. This in turn degrades the phase margin of the system. In the worst case when the loop delay becomes excessive the system becomes unstable.

Excess loop delay can be compensated by use of return-to-zero (RZ) DAC pulses and feedback coefficient tuning [8].

CHAPTER 4

Loop Filter

The loop filter of a $\Delta\Sigma$ modulator is responsible for shaping the quantization noise away from the signal band. The first few sections give a general overview of the loop filter while the later sections are devoted to the design of a 3rd order CT loop filter.

4.1 High-Order Single-Quantizer Modulators

The general block diagram of a $\Delta\Sigma$ modulator with a single quantizer is shown in figure 4.1. The modulator is divided into two parts:

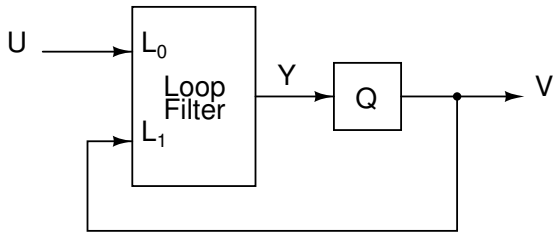


Figure 4.1: General structure of a single quantizer $\Delta\Sigma$ modulator

1. The linear part - loop filter containing the memory elements.
2. The non-linear part - quantizer which is memoryless.

The modulator is modelled as a two-input system with a single output. The output of the modulator in terms of its inputs U and V is:

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{4.1}$$

The quantizer is modelled as before. It adds an error signal to its input.

$$V(z) = Y(z) + E(z) \tag{4.2}$$

Using the above two equations the output of the modulator V can be written as a linear combination of the input signal U and the quantization error E:

$$Y(s) = STF(z)U(z) + NTF(z)E(z) \tag{4.3}$$

where,

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \quad and \quad NTF(s) = \frac{1}{1 - L_1(z)} \tag{4.4}$$

From equation (4.4) L_1 must have a large magnitude in the signal band 0 to $f_s/(2.OSR)$ to reduce the NTF magnitude within the signal bandwidth. L_0 must have a large magnitude in the same band so that the STF magnitude is unity. Hence, L_0 and L_1 should have their poles closer to $z = 1$. From figure 4.1, equations (4.1)-(4.4) and due to the shared circuitry used to realize L_0 and L_1 these two functions have the same poles.

There must be at least one clock cycle delay in the loop containing the quantizer and L_1 in figure 4.1. Else, a given value of y(n) would change the quantizer output which in turn changes the loop filter input. This sample is then filtered through L_1 and y(n) would change instantly. Thus the value of y(n) would change continuously during the same period. This delay is accounted for in the noise shaping function $L_1(z)$.

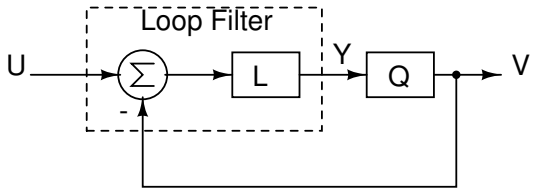


Figure 4.2: Single feedback topology

When the loop filter has a single input (figure 4.2) and only the difference u(n) - v(n) enters the loop filter then $L_0 = -L_1 = L$ and equation (4.4) becomes:

$$STF(z) = \frac{L(z)}{1 + L(z)} \quad and \quad NTF(z) = \frac{1}{1 + L(z)} \tag{4.5}$$

where L is the transfer function of the common loop filter portion. Now L along

with the quantizer determines the properties of the modulator.

Figure 4.3 shows another special case where a direct path is added to the structure shown in figure 4.2. While L_1 remains unchanged, L_0 changes to $L + 1$. Hence, the NTF remains the same as given in equation (4.5) while the STF becomes:

$$STF(z) = \frac{L(z) + 1}{1 + L(z)} = 1 \tag{4.6}$$

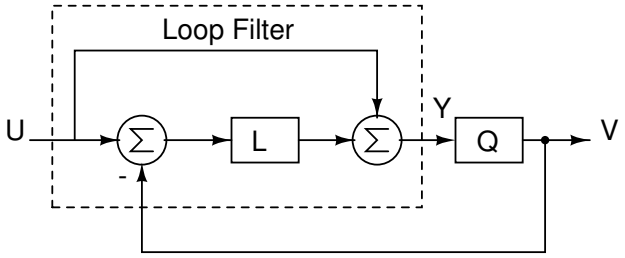


Figure 4.3: Single feedback topology with a feedforward path

Since the signal transfer function is unity the input U appears at the output directly. The loop filter input is given by:

$$U - V = U - (STF.U + NTF.E) = -NTF.E = \frac{-E}{1 + L} \tag{4.7}$$

The above equation suggests that the loop filter input no longer contains the input signal, only the filtered quantization noise. This simplifies the design of the loop filter since it need not have high linearity.

4.2 Loop Filter Architecture

In this section two different loop filter architectures are discussed. They are as follows:

1. Cascaded Integrators with distributed feedback and distributed input coupling (CIFB)

2. Cascaded Integrators with distributed feedforward and input coupling (CIFF)

4.2.1 CIFB Architecture

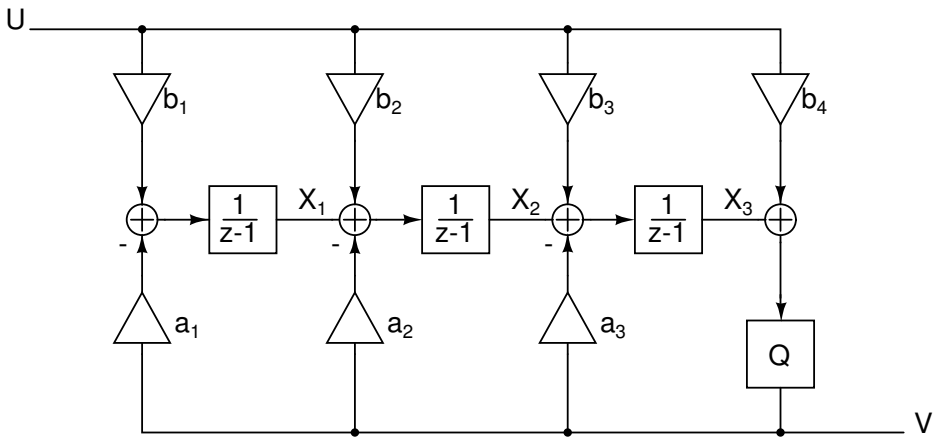


Figure 4.4: Third order CIFB architecture

Figure 4.4 shows the block diagram of a 3rd order loop filter with a CIFB structure. It contains a cascade of three integrators where each integrator is fed the input signal as well as the feedback signal with different weight factors b_i and a_i. The signal filter transfer function is:

$$L_0(z) = \frac{b_1}{(z-1)^3} + \frac{b_2}{(z-1)^2} + \frac{b_3}{(z-1)} + b_4 \tag{4.8}$$

$$= \frac{b_1 + b_2(z-1) + b_3(z-1)^2 + b_4(z-1)^3}{(z-1)^3} \tag{4.9}$$

while the feedback filter has the transfer function

$$L_1(z) = \frac{-a_1}{(z-1)^3} + \frac{-a_2}{(z-1)^2} + \frac{-a_3}{(z-1)} \tag{4.10}$$

$$= -\frac{(a_1 + a_2(z-1) + a_3(z-1)^2)}{(z-1)^3} \tag{4.11}$$

The NTF for this structure is of the form:

$$NTF(z) = \frac{1}{1 - L_1(z)} = \frac{(z-1)^3}{D(z)} \tag{4.12}$$

where,

$$D(z) = a_1 + a_2(z-1) + a_3(z-1)^2 + (z-1)^3 \tag{4.13}$$

All the zeros of the NTF for this structure lie at dc. The co-efficients a_i are found by comparing D(z) to the denominator of the desired NTF and equating the like powers of z.

The STF for the above structure is given by:

$$STF(z) = \frac{b_1 + b_2(z-1) + b_3(z-1)^2 + b_4(z-1)^3}{D(z)} \tag{4.14}$$

The co-efficients b_i are again found by matching the co-efficients with the numerator of the desired STF.

An interesting choice for a_i and b_i is as follows:

$$a_1 = b_1, a_2 = b_2, a_3 = b_3 \quad and \quad b_4 = 1 \tag{4.15}$$

From equation (4.14) for these values of the co-efficients the STF is exactly unity. The output of the modulator is given by:

$$V(z) = U(z) + NTF(z)E(z) \tag{4.16}$$

Hence, the input to the ith integrator for $a_i = b_i$ is:

$$X_{i-1}(z) + b_i U(z) - a_i V(z) = X_{i-1}(z) - a_i NTF(z)E(z) \tag{4.17}$$

Thus, the input signal does not appear at the input of any integrator. Only the filtered quantization noise is processed by the loop filter. An important advantage gained by the loop filter not having to process the input signal is that the non-linearities of the integrators will not introduce harmonic distortion at the modulator output.

In this architecture the first integrator will have the largest input signal component and minimum amount of quantization noise, while the last one will contain a small part of the input signal and the maximum amount of noise [9]. Since the output of an integrator represents the input of the subsequent stage, it follows that the linearity of the first integrating stage is more critical than the linearity of the

final ones. Hence, in this architecture both the first as well as the last integrators are power hungry.

4.2.2 CIFF Architecture

Figure 4.5 shows the block diagram of a 3rd order loop filter with a CIFF architecture. The zeros of the NTF are realized using the feedforward path instead of the feedback path.

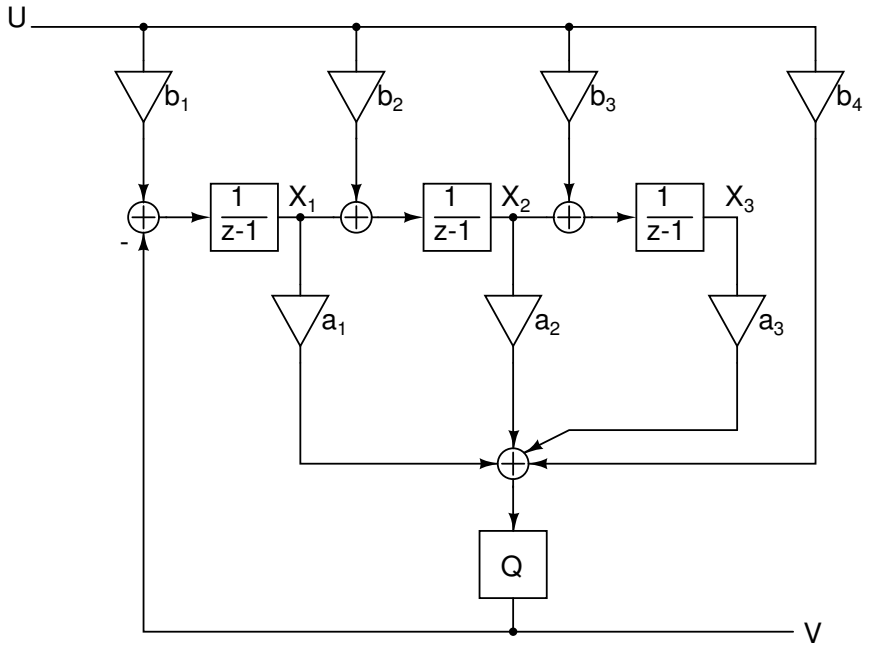


Figure 4.5: Third order CIFF architecture

The transfer function of the feedback filter is:

$$L_1(z) = \frac{-a_1}{(z-1)} + \frac{-a_2}{(z-1)^2} + \frac{-a_3}{(z-1)^3} \tag{4.18}$$

The signal filter function is:

$$L_0(z) = b_1(\frac{a_1}{(z-1)} + \frac{a_2}{(z-1)^2} + \frac{a_3}{(z-1)^3}) + b_2(\frac{a_2}{(z-1)} + \frac{a_3}{(z-1)^2}) + b_3\frac{a_3}{(z-1)} + b_4 \tag{4.19}$$

The values of NTF(z) and STF(z) can be calculated as before using equation (4.4). The important result is obtained when $b_1 = b_4 = 1$ and $b_2 = b_3 = 0$. Then from

equations (4.18) and (4.19), $L_0(z) = 1 - L_1(z)$ holds, and the STF turns out to be unity. The input to the loop filter is now given by:

$$U(z) - V(z) = U(z) - (U(z) + NTF(z)E(z)) = -NTF(z)E(z) \tag{4.20}$$

Thus, the loop filter need not process the input signal and hence, this configuration has the low-distortion property which was discussed earlier for the CIFB structures.

For this topology the first integrator will contain small amount of the input signal and a large amount of filtered quantization noise [9]. The last integrator will introduce large amount of in-band distortions but this will be shaped by the loop filter. Again only the linearity of the first integrator is critical. Hence, only the first integrator is power hungry for this topology. So, for low power applications the CIFF structure is preferred over the CIFB topology.

4.3 Selection and Implementation of Loop Filter Transfer Function

The first step in the design of a $\Delta\Sigma$ modulator is the choice of the modulator order and its noise transfer function(NTF). A third order modulator with an OSR of 64 and a 4-bit internal quantizer gives a signal-to-quantization noise ratio of around 120 dB. The NTF of the modulator has an out-of-band gain (OBG) of 2.5. OBG is defined as the gain of the NTF at frequencies close to $\omega = \pi$. A modulator with the above characteristics was simulated in MATLAB. The output spectrum of the modulator output is shown in figure 4.6.

The following steps were followed to find the transfer function of the CT loop filter:

1. Using the Sigma-Delta toolbox in MATLAB the NTF of a 3rd order DT $\Delta\Sigma$

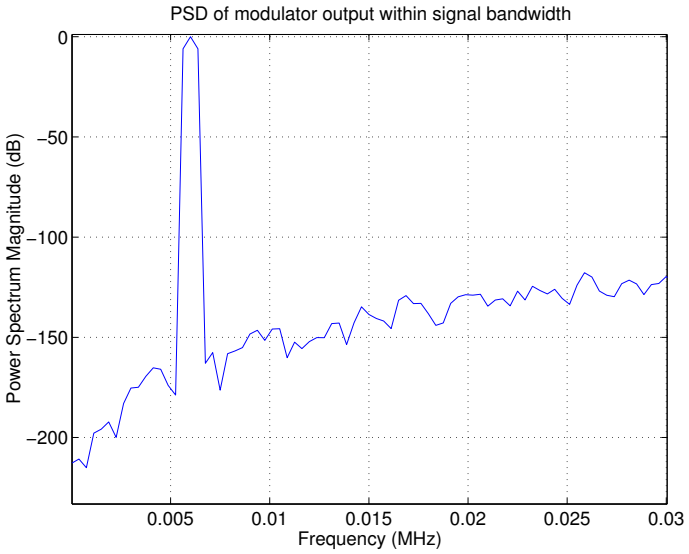


Figure 4.6: PSD of the modulator output within signal bandwidth

modulator with an OBG of 2.5 is determined.

$$NTF(z) = \frac{(z-1)^3}{(z-0.417)(z^2-0.8778z+0.3804)} \tag{4.21}$$

2. The DT loop filter transfer function L(z) is given by:

$$L(z) = \frac{NTF(z)-1}{NTF(z)} \tag{4.22}$$

$$= -1.7052\frac{z^2-1.3216z+0.4934}{(z-1)^3} \tag{4.23}$$

3. The impulse invariance transformation is used to determine the transfer function L(s) of the equivalent CT modulator. The sampling interval is 1s.

$$L(s) = -\frac{1.2244}{s} - \frac{0.8639}{s^2} - \frac{0.2930}{s^3} \tag{4.24}$$

The above equation for L(s) can implemented by a cascade of three integrators and a summer. Figure 4.7 shows the block diagram for the implementation of L(s).

It is now necessary to perform dynamic-range scaling. Dynamic scaling is

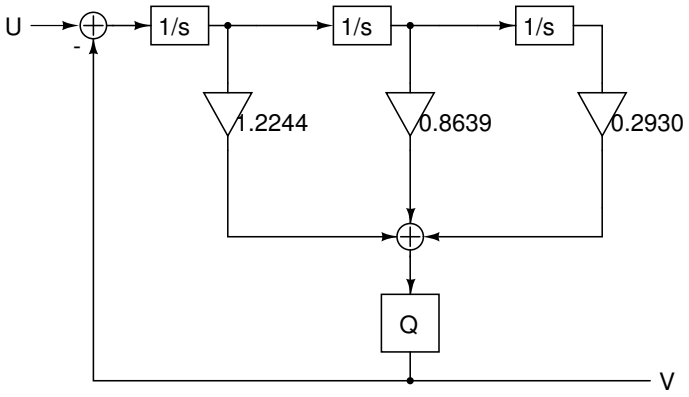


Figure 4.7: Block diagram of 3rd order CT loop filter for $T_s = 1s$

necessary to ensure that all nodes have approximately, the same power level, so that all nodes will clip near the same level, and there will be no unnecessarily large noise gains from nodes with small signal levels. After dynamic scaling all nodes have the same maximum output level. Dynamic scaling is done as follows: The maximum output level of each integrator is determined. The maximum outputs of all integrators are set to the same level by adjusting their gains. To increase the output level at a node by a factor of k, the input branches should be multiplied by k while the output branches should be divided by k. The block diagram of the CT loop filter after scaling is shown in figure 4.8.

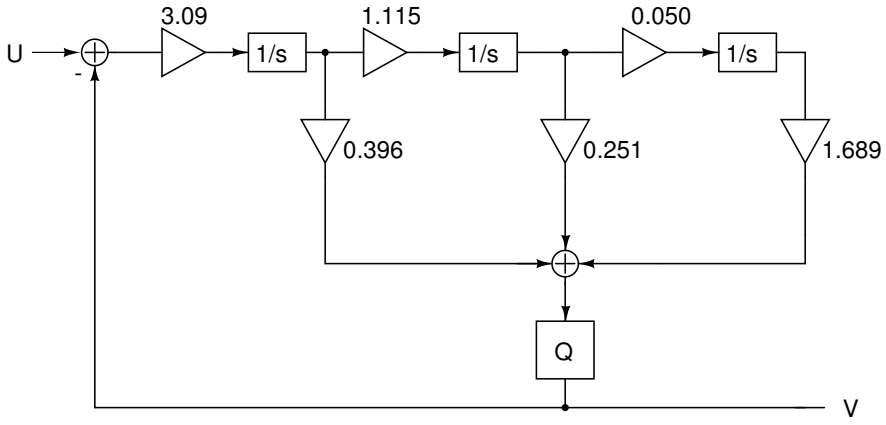


Figure 4.8: Block diagram of 3rd order CT loop filter after dynamic-range scaling for $T_s = 1s$

Figure 4.9 shows the prototype model for the modulator loop filter built using ideal op amps.

The prototype model shown in figure 4.9 needs to be frequency scaled to the

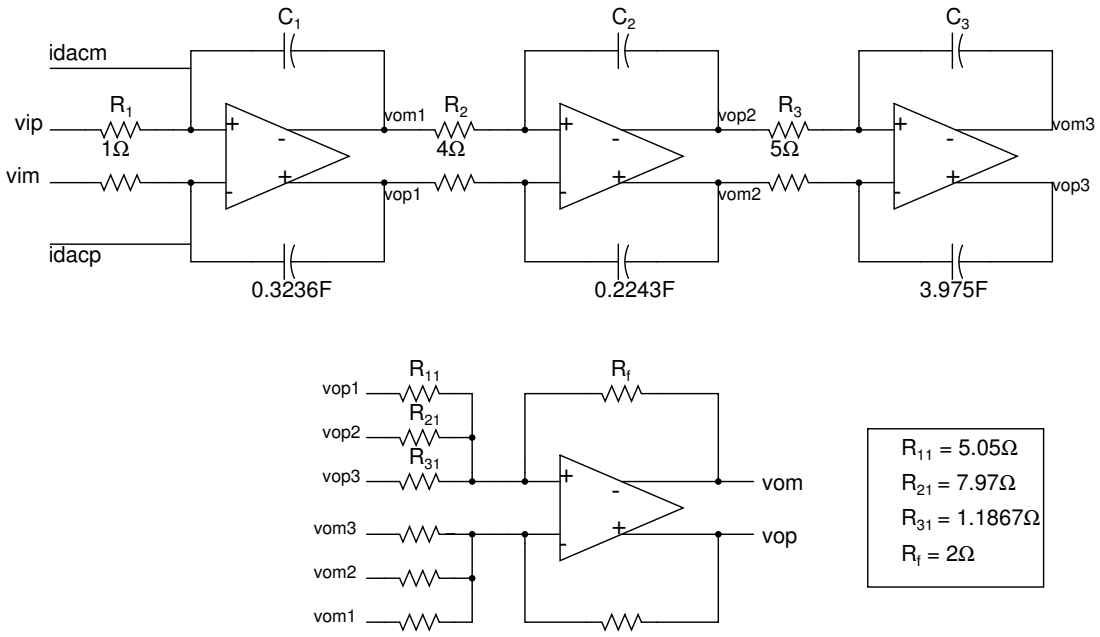


Figure 4.9: Loop filter with ideal op amps for $f_s = 1Hz$

frequency of operation of the modulator i.e $f_s = 3.072MHz$. Also all impedances in the prototype model are scaled by $100K$ to get a practically realizable loop filter operating at 3.072 MHz. The loop filter obtained after both frequency and impedance scaling is shown in figure 4.10.

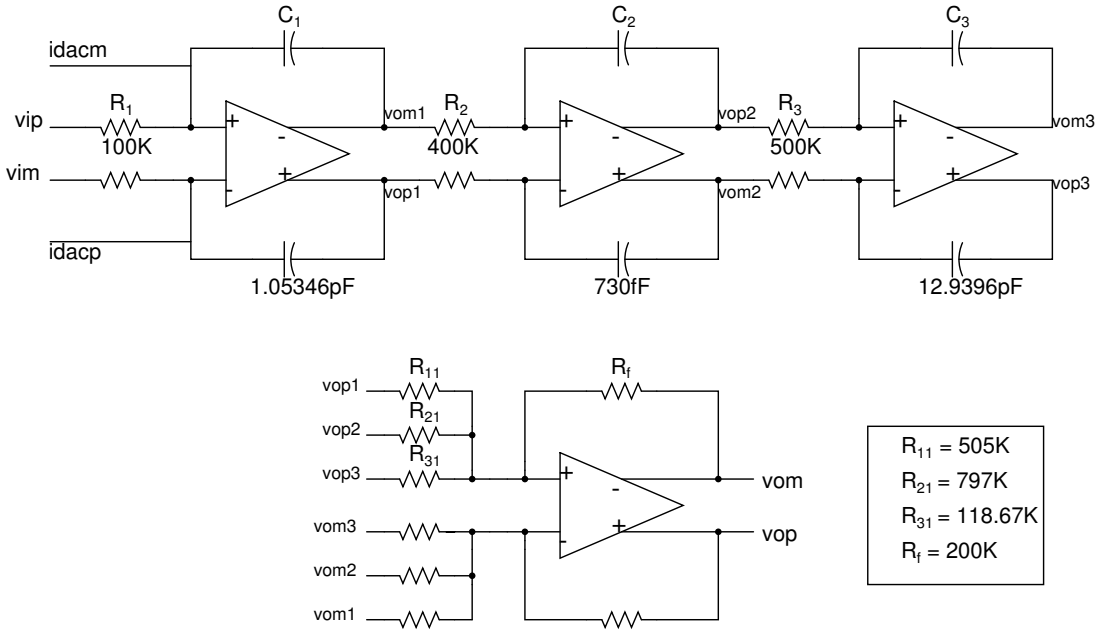


Figure 4.10: Loop filter with ideal op amps for $f_s = 3.072MHz$

4.4 First Integrator Op amp

The first integrating op amp needs to be carefully designed since it determines the overall linearity of the data converter. Any non-linearity of the succeeding op amps becomes insignificant when referred back to the input. The first integrating op amp is a two-stage op amp. The first stage of the op amp is telescopic while the second is a class AB stage. Figure 4.11 shows the schematic of the first op amp.

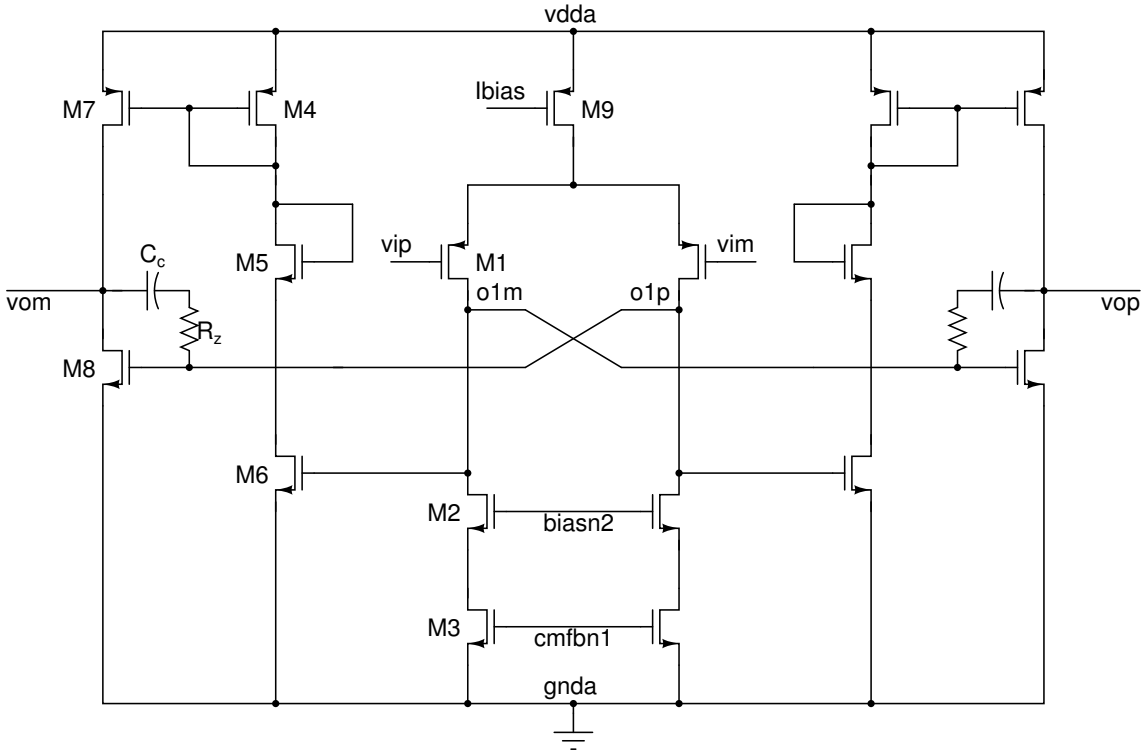


Figure 4.11: First Integrator Op amp

Noise is an important consideration while choosing the op amp input stage. The major source of noise at low frequencies is the $1/f$ noise of the MOS transistors. Typically, p-channel transistors have less $1/f$ noise than the n-channel transistors. Hence, using p-channel transistors for the input stage of the first integrator op amp minimizes the overall input referred noise of the loop filter. Transistors M2-M3 form the cascode current source load for the differential pair. Cascoding enhances the output impedance of the current source.

The second stage of the op amp is a class AB power amplifier. Hence, it has a

Transistor	Size	Current(μA)
M1	20(0.5/2)	2
M2	12(1/1)	2
M3	20(3/6)	2
M4	8(1/0.25)	0.8
M5	8(1/0.18)	0.8
M6	8(0.5/0.25)	0.8
M7	8(1/0.25)	0.8
M8	12(0.5/0.25)	0.8
M9	80(1/1)	4

Table 4.1: First integrating op amp transistor sizing and currents

low quiescent operating current. The differential output of the first stage is fed to transistors M6 and M8 of the second stage. The current through M6 is mirrored to the output by the current mirror pair M4-M7. The output current sourced/sinked by the op amp is the sum of the currents carried by M7 and M8. The second stage of the op amp is frequency compensated. The capacitor C_c realizes dominant pole compensation. It controls the dominant pole of the op amp. Addition of C_c leads to a right-half-zero, which makes compensation more difficult. The resistor R_z is used to move this zero to the left-half-plane. This technique is called lead compensation.

4.4.1 Common-Mode Feedback circuits

In fully-differential circuits with feedback, the feedback determines the differential signal voltages, but does not affect the common mode voltages. Hence, additional circuitry is needed to control the output common mode voltage and set it to some specified voltage. This circuitry is referred to as the *common-feedback feedback (CMFB) circuitry.*

First stage CMFB circuitry

Figure 4.12 shows the CMFB circuitry that sets the output common mode of the first stage of the op amp. To illustrate the operation of the CMFB circuitry

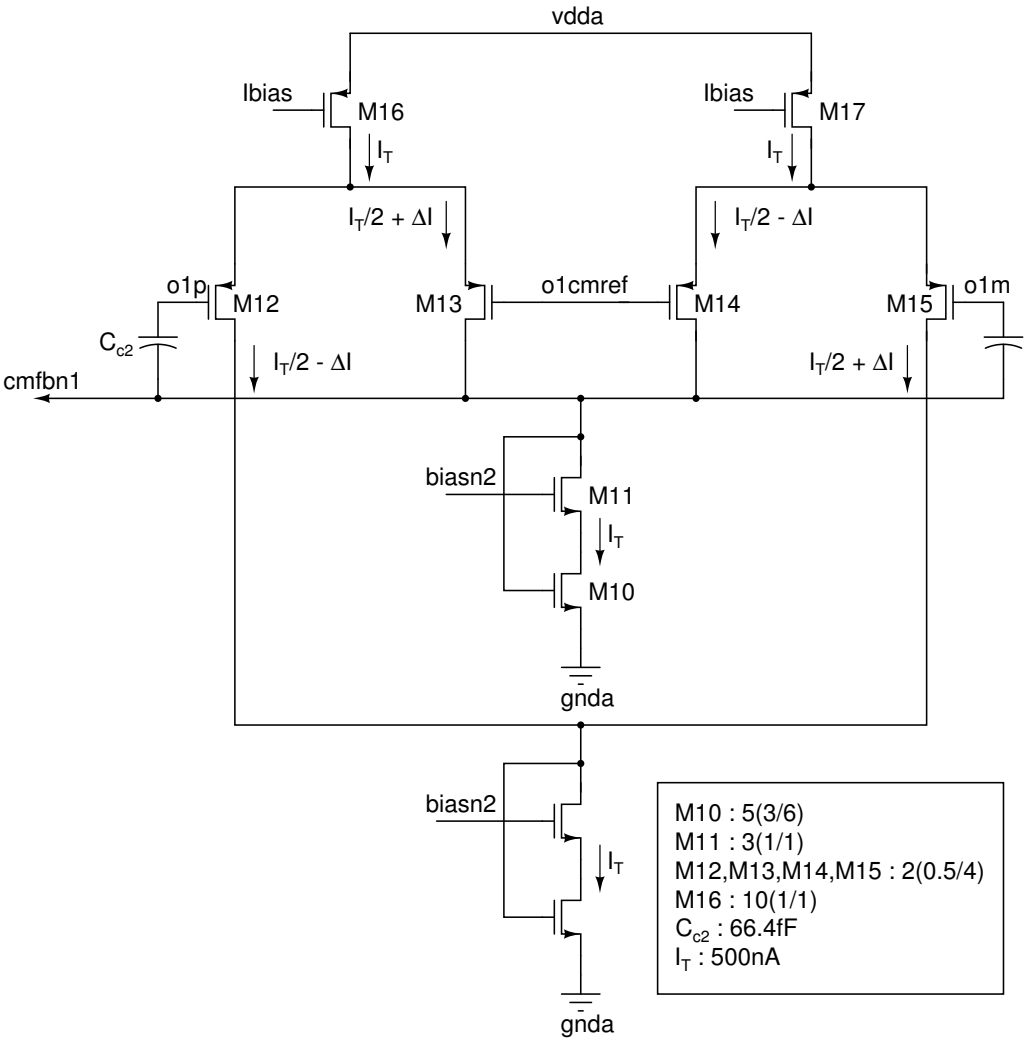


Figure 4.12: First stage CMFB circuit

assume that the first stage outputs o1p and o1m have equal magnitude but are of opposite signs. Since the two differential pairs have the same differential input voltage, the current in M12 will be equal to the current in M14 while the current in M13 will equal the current in M15. As long as o1p and o1m are equal in magnitude and are of opposite signs the current through the M10-M11 current source is a constant and equals I_T. The voltage across diode connected M10 controls the bias voltage of the first stage output of the op amp

Now consider the case where the common mode voltage of the first stage output is higher than the desired voltage. This causes the current in M13-M14 to increase, which causes the current in the diode connected transistor M10 to increase, which in turn causes its gate voltage to increase. This voltage is used to set the current levels in the NMOS current sources at first stage output of the op amp. Thus, both current sources will have larger pulling down currents to ground. This causes the common mode voltage to decrease and brings it back to the desired value. As long as the common mode loop gain is large enough and the differential signals are not large enough to turn off transistors in the differential pair, the common mode voltage will be set to the desired value.

The CMFB circuits must be compensated. Otherwise, the injection of common mode signals can cause them to ring or even make it unstable. Hence, compensating capacitors have been connected between the first stage outputs and the fixed reference voltage cmfbn1. The step response of the first stage common mode loop is shown in figure 4.13

Second Stage CMFB circuitry

Figure 4.14 shows the CMFB circuitry that sets the output common mode of the first stage of the op amp. The desired value of the output common mode voltage equals V_{vm}. The output common-mode level is $V_{out,CM} = (vop + vom)/2$, where vop and vom are the single ended outputs. The output common-mode level is sensed by the averaging resistors connected between vop and vom. This voltage is then compared with the required output common-mode V_{cm} by the error amplifier. The output of the error amplifier controls the bias voltage of the output

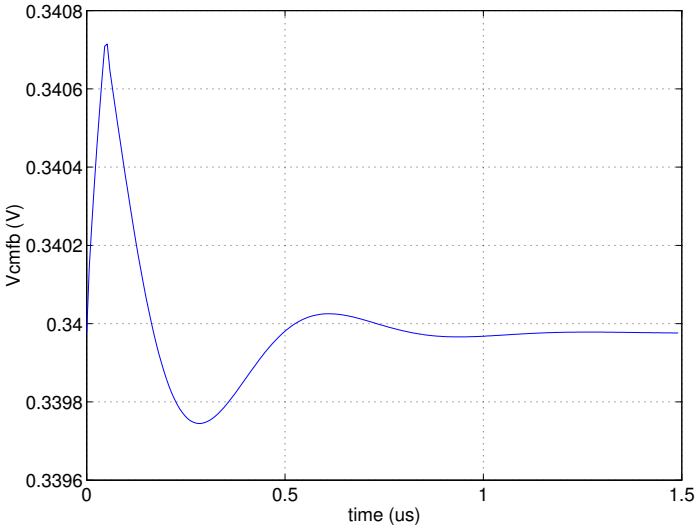


Figure 4.13: First stage CMFB circuit step response

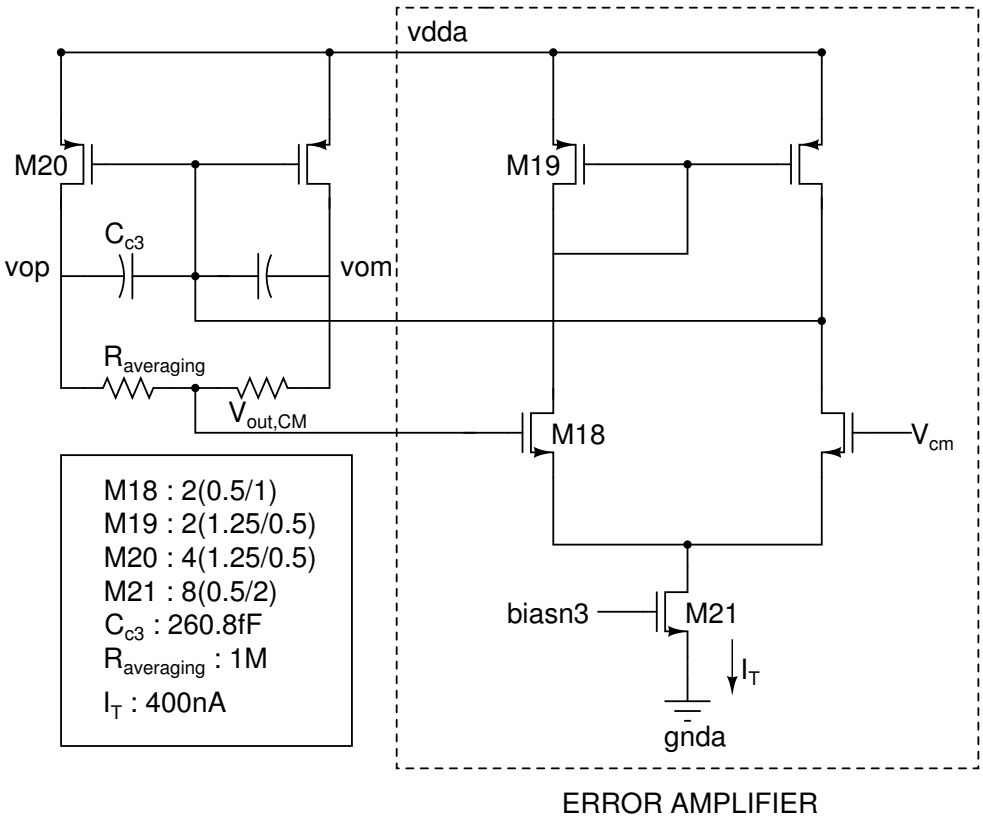


Figure 4.14: Second stage CMFB circuit

stage of the op amp.

In order to illustrate the working of the common-mode loop consider the case when the output common-mode exceeds the desired voltage V_{cm}. This causes the current in M18 to decrease and the output voltage of the error amplifier increases. This voltage is the bias voltage that sets the current levels in the PMOS current sources at the output of the op amp. The current sources at the output will now pull lower currents from the supply, which will cause the output common-mode voltage to decrease, bringing it back to V_{cm}. Capacitors are connected between the op amp output and the error amplifier output for compensating the common mode feedback loop. The step response of the second stage common mode loop is shown in figure 4.15

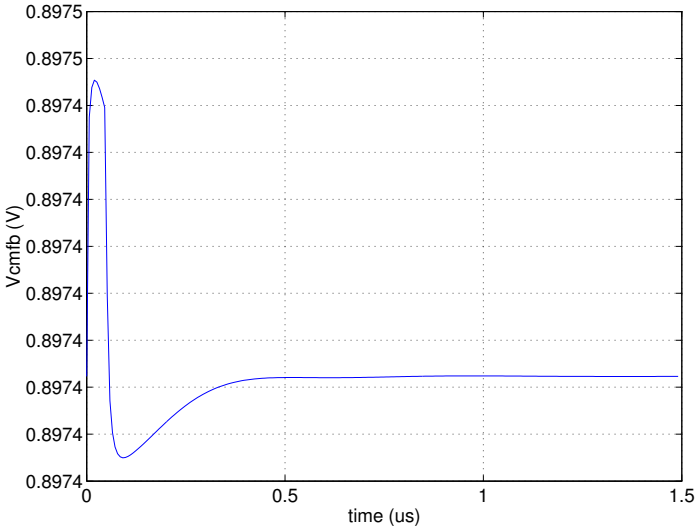


Figure 4.15: Second stage CMFB circuit step response

4.4.2 Noise Analysis

At low frequencies the major source of noise is the flicker noise or 1/f noise of the MOS transistors. In the designed op amp since the second stage is a class AB power amplifier it has a low output impedance and hence, a low voltage gain. Since the first stage has high gain most of the noise comes from the transistors in the first stage. In the noise calculation presented the noise added by the second stage is neglected. The noise contribution of the first stage transistors is tabulated

below:

Transistor	1/f Noise (f_n)	Thermal Noise (i_d)	f_n at o/p	i_d at o/p
M_1	$V_{n1}^2 G_1^2 R_1^2 G_2^2 R_2^2$	$I_{n1}^2 R_1^2 G_2^2 R_2^2$	30.96%	6.66%
M_3	$V_{n3}^2 g_{M3}^2 R_1^2 G_2^2 R_2^2$	$I_{n3}^2 R_1^2 G_2^2 R_2^2$	43.34%	18.82%
M_2, M_9	0	0	0	0

Table 4.2: Transistor noise contributions

The symbols used in the above table are explained below:

G_1 = Input stage transconductance = g_{M1}

R_1 = Output impedance of the first stage

G_2 = Equivalent second stage transconductance = $g_{M6} + g_{M8}$

R_2 = Output impedance of the second stage

g_{M3} = Transconductance of M3

V_{n1} = Flicker noise at the input of M1

V_{n3} = Flicker noise at the input of M3

I_{n1} = Thermal noise current of M1

I_{n3} = Thermal noise current of M3

The total noise at the outpop amp the op amp is given by:

$$v_{n,out}^2 = 2(V_{n1}^2 G_1^2 R_1^2 G_2^2 R_2^2 + I_{n1}^2 R_1^2 G_2^2 R_2^2 + V_{n3}^2 g_{m3}^2 R_1^2 G_2^2 R_2^2 + I_{n3}^2 R_1^2 G_2^2 R_2^2) \quad (4.25)$$

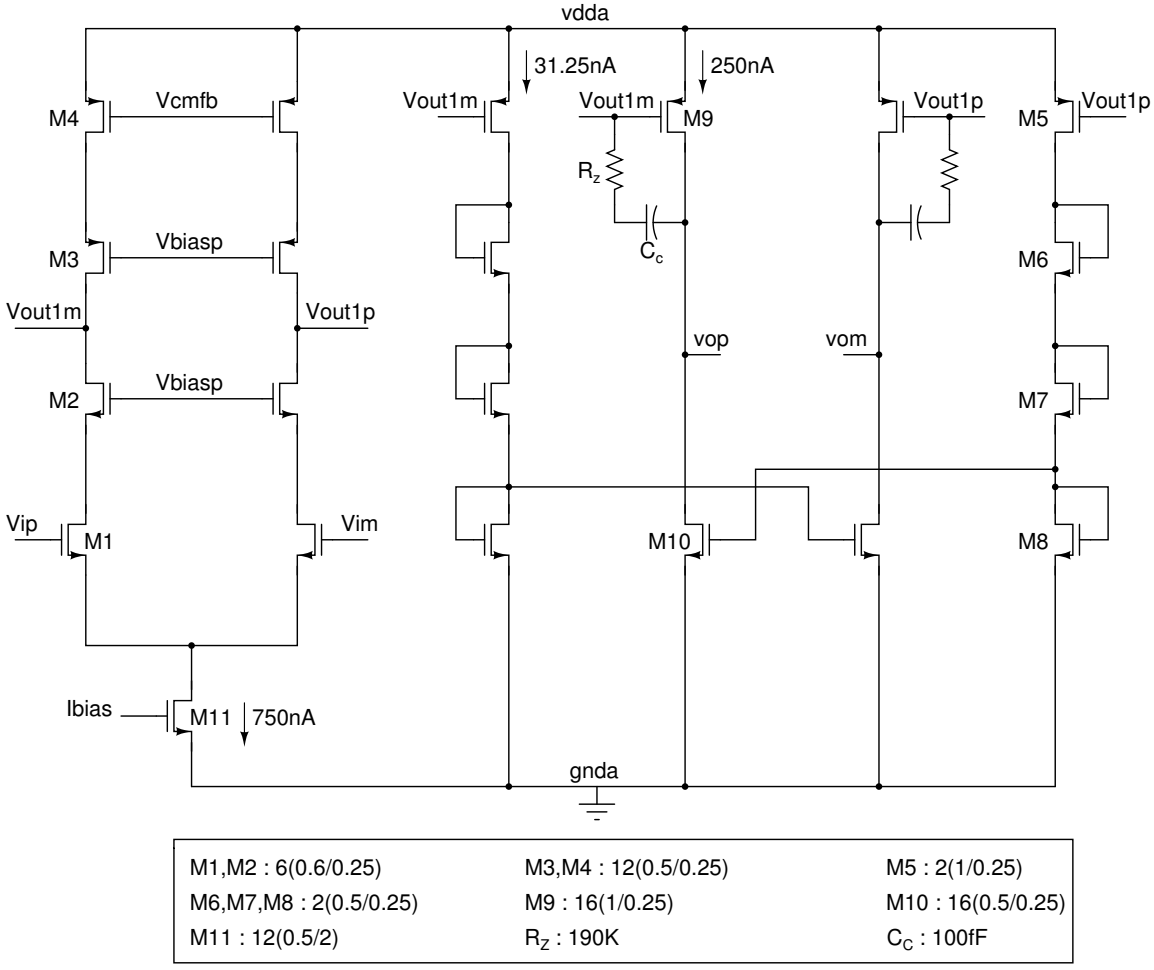
The gain of the op amp is $G_1 R_1 G_2 R_2$. Hence, the input referred noise of the op amp is given by:

$$v_{n,i/p}^2 = 2(V_{n1}^2 + I_{n1}^2 \frac{1}{g_{M1}^2} + V_{n1}^2 \frac{g_{M3}^2}{g_{M1}^2} + I_{n3}^2 \frac{1}{g_{M1}^2}) \quad (4.26)$$

The total noise at the input of the op amp integrated over 20Hz to 24KHz is $8.65\mu V$.

4.5 Second Integrator Op amp

The second integrating op amp has less stringent specifications on gain, unity gain bandwidth, slew rate and speed in comparison to the first op amp. It also has a two stage architecture wherein the first stage is a telescopic op amp while second is a class AB stage. Figure 4.16 shows the schematic of the second op amp.



M1,M2 : 6(0.6/0.25)	M3,M4 : 12(0.5/0.25)	M5 : 2(1/0.25)
M6,M7,M8 : 2(0.5/0.25)	M9 : 16(1/0.25)	M10 : 16(0.5/0.25)
M11 : 12(0.5/2)	R_Z : 190K	C_C : 100fF

Figure 4.16: Second Integrator Op amp

The input stage is a pair of n-channel differential transistors. The PMOS current source loads as well as the differential pair are cascoded to increase the first stage output impedance and hence the gain. The differential output of the first stage is fed to transistors M5 and M9 of the second stage. The current through M5 is mirrored to the output by the current mirror pair M8-M10. The resistor R_z and the capacitor C_c are used for frequency compensation of the op amp.

4.5.1 CMFB circuitry

CMFB circuitry is employed to fix the common-mode voltage of the the first as well as the second stage outputs.

First stage CMFB circuitry

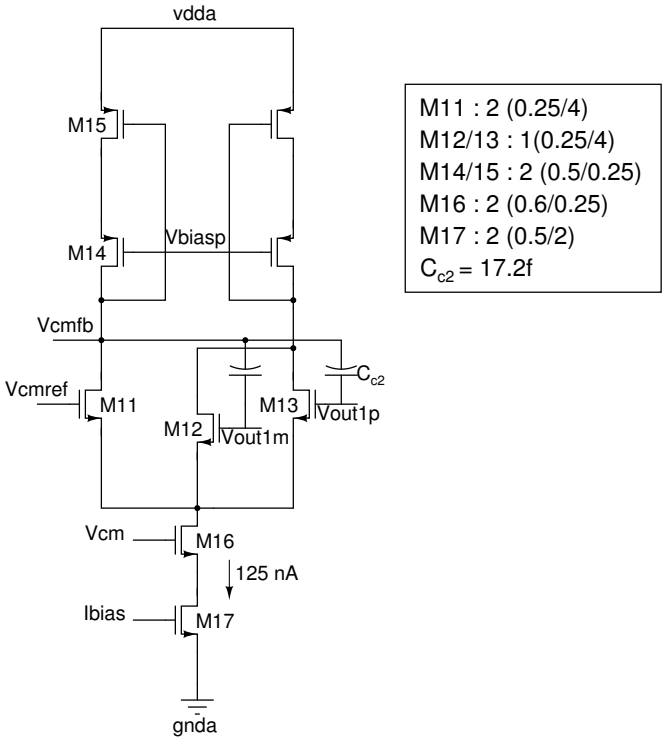


Figure 4.17: First stage CMFB circuit

Figure 4.17 shows the CMFB circuit used to set the first stage output common mode. The CMFB circuit works as follows: Let the output common mode voltage exceed the desired voltage. The currents through transistors M12 and M13 increases while the current though M11 decreases . This causes the gate voltage of the cascoded current source transistor M15 to increase. This voltage is used to set the current level in the PMOS current sources at the output of the first stage. The PMOS current sources will now be pulling lower currents from the supply, and hence the outputs return back to the desired common-mode voltage. The step response of the CM loop is shown in figure 4.18

Second Stage CMFB circuitry

Figure 4.19 shows the CMFB circuitry that sets the output common mode of

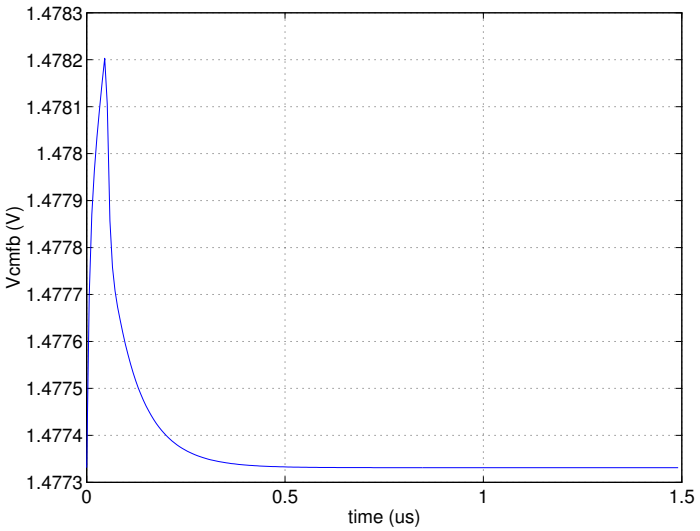


Figure 4.18: First stage CMFB circuit step response

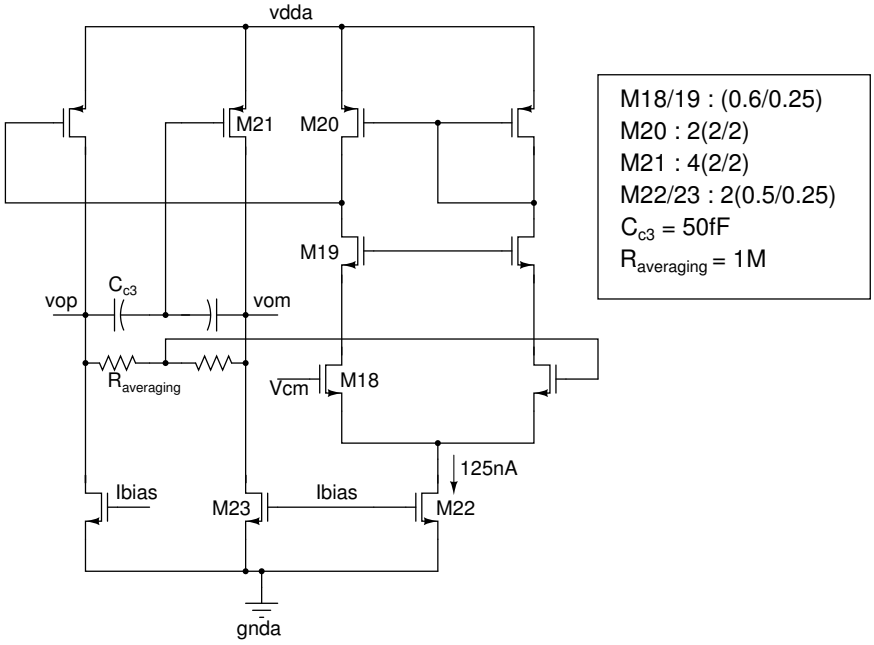


Figure 4.19: Second stage CMFB circuit

the first stage of the op amp. The desired value of the output common mode voltage equals V_{cm}. This circuit is identical in operation to that of the first op amp second stage CMFB circuit. The step response of the second stage common mode loop is shown in figure 4.20

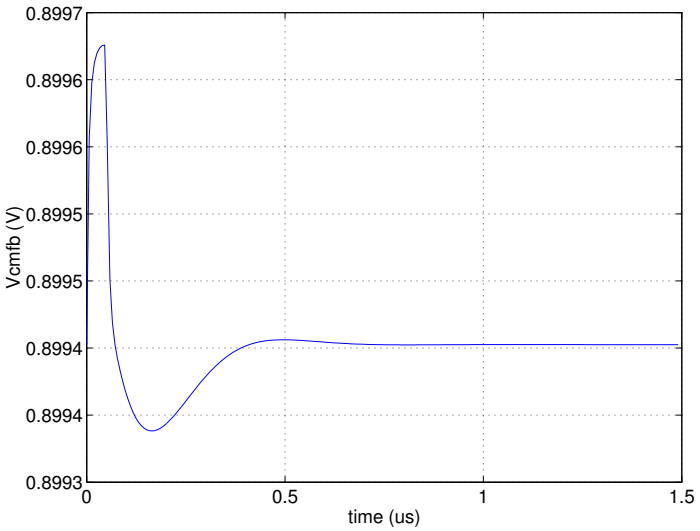


Figure 4.20: Second stage CMFB circuit step response

The third and the fourth op amp of the loop filter have an architecture that is identical to the second op amp.

4.6 Optimization of Loop Filter

The designed loop filter op amps have characteristics that are quiet different from the ideal op amp used for implementing the loop filter in figure 4.10. The loop filter with the designed op amps will have a NTF that is different from one which it is designed for. Hence, it becomes necessary to tune the loop filter i.e the gains of the integrator and the summer to get back the desired NTF. This is done as follows:

1. Each op amp of the loop filter is modelled in MATLAB.

2. The state space model for the loop filter is developed.

3. From the state space model the loop filter transfer function and hence the NTF of the loop filter is determined.

4. Using the *fminsearch* function in MATLAB the loop filter parameters are fine tuned, so that after tuning the loop filter NTF matches the ideal NTF.

Figure 4.21 shows the ideal loop filter NTF and the NTF of the loop filter implemented in the design after optimization.

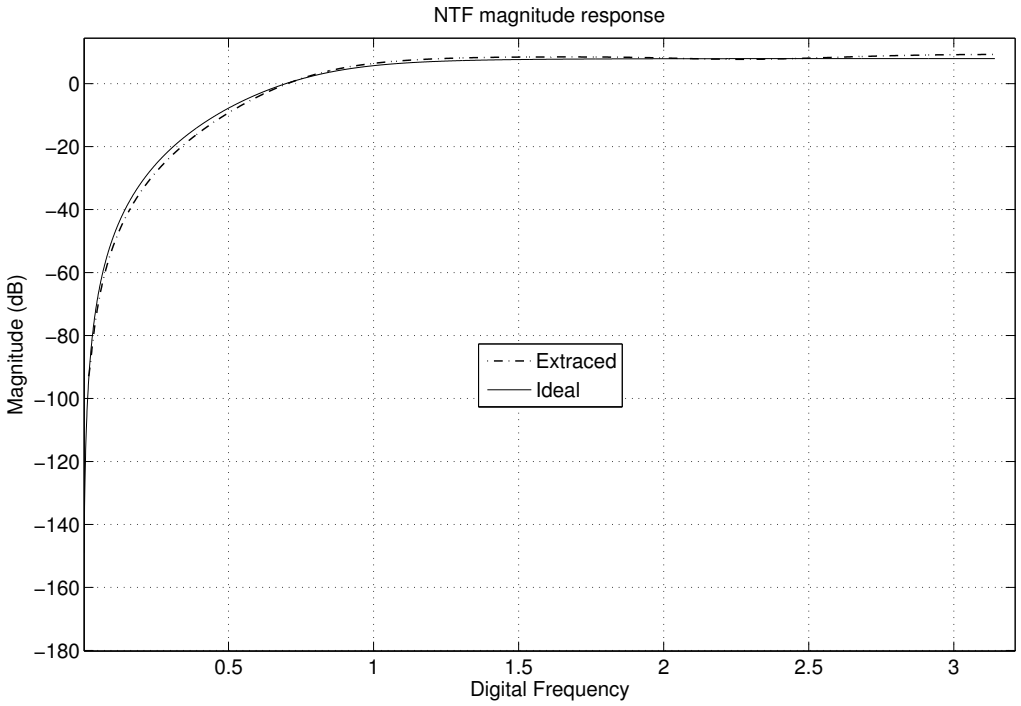


Figure 4.21: Loop filter NTF

The schematic of the loop filter implemented in the design is shown in figure 4.22.

The nodes of the loop filter have been scaled such that each integrator has approximately the same maximum output level. The outputs of the three loop filter integrators along with the final summer output is shown in figure 4.23.

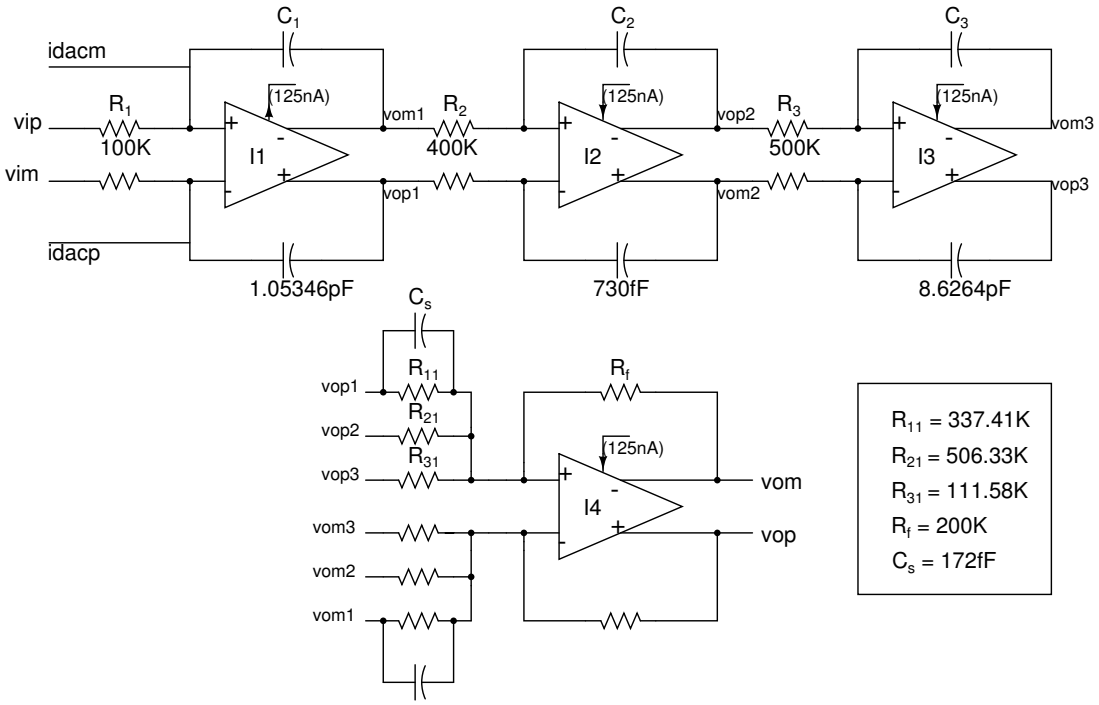


Figure 4.22: Loop filter schematic

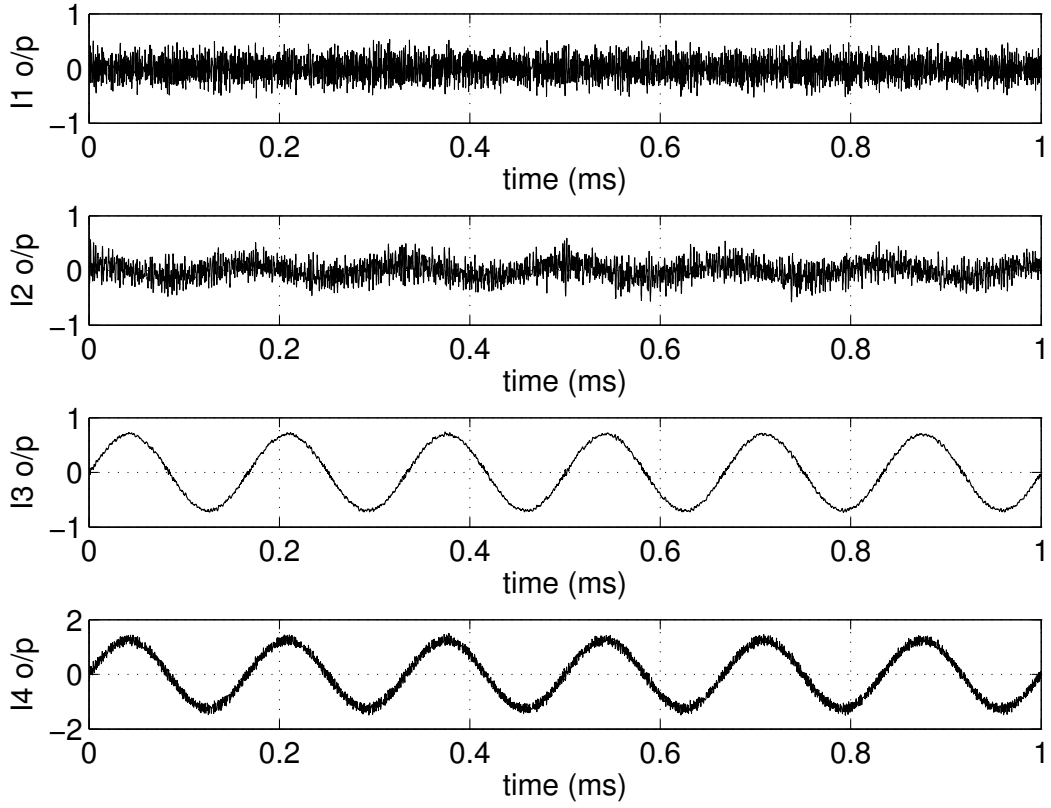


Figure 4.23: Loop filter integrator outputs and the loop filter output

4.7 RC Tuning

The value of the integrating resistors and capacitors vary across process corners. The variation in the RC time constant of the integrators can be problematic. When the RC time constants go down the poles of the NTF move away from the origin towards the higher frequencies which increases the out-of-band gain of the NTF. The modulator now operates at the verge of instability. Hence, some kind of coarse tuning of RC time constants is necessary.

Integrator	RC_{min}	RC_{max}
I1	$0.64R_1C_1$	$1.703R_1C_1$
I2	$0.65R_2C_2$	$1.683R_2C_2$
I3	$0.65R_3C_3$	$1.68R_3C_3$

Table 4.3: Variation of Integrator RC constants

The tuning of the loop filter RC time constants is made possible by making each of the integrating capacitors programmable. Programmable integrating capacitor is realized by a capacitor bank shown in figure 4.24.

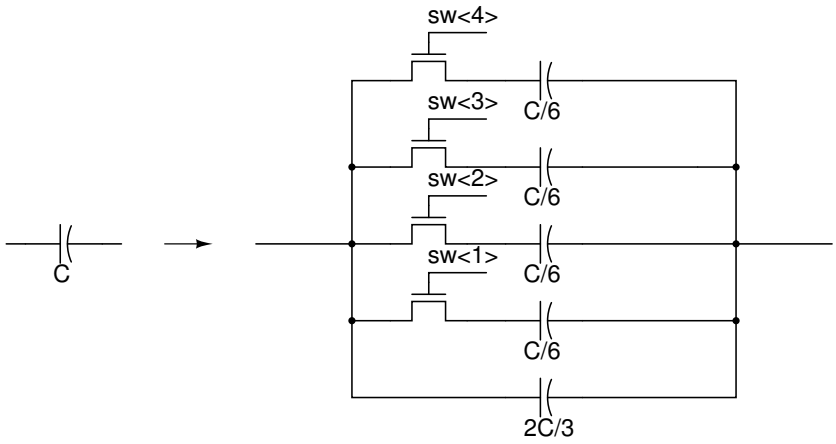


Figure 4.24: Capacitor bank

The MOS switches are connected to the input (virtual ground) of the integrator while the capacitors are connected to the output. Hence, the signal swing across the MOS switches is small and the distortion introduced by the switches is low. On the other hand connecting the MOS switches at the output would introduce significant distortion because the integrators have large output swings.

The control signals for the MOSFET switches are generated externally. The loop filter capacitors can now be tuned from (2/3)C to (4/3)C. Hence, each integrator's RC time constant can now be tuned from 0.67RC to 1.33RC.

CHAPTER 5

Flash ADC

5.1 Introduction

Flash converters are the standard approach for realizing very-high-speed converters. Figure 5.1 shows the basic architecture of a 4-bit differential Flash ADC.

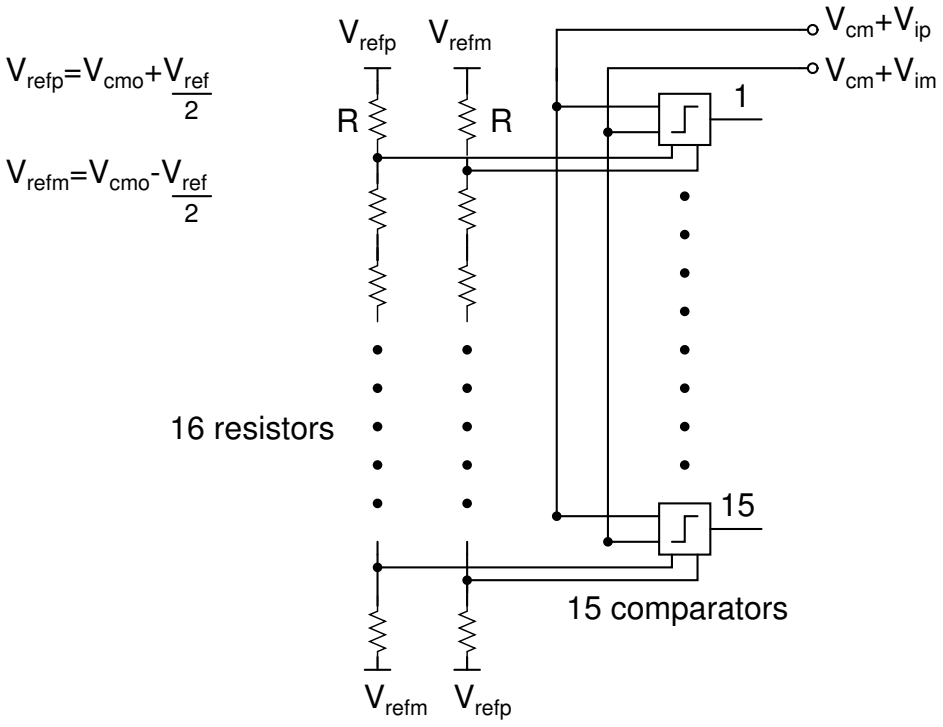


Figure 5.1: The Flash converter

The differential input signal is fed to $2^N - 1$ comparators in parallel (in this case N = 4). Each comparator is also connected to a different node of two resistor strings. The two resistive ladders provide the differential reference voltage for the comparators. Whenever the differential input voltage to a comparator exceeds its differential reference voltage, the output of the comparator goes high. Otherwise the output of the comparator goes low. The Flash ADC gives a thermometer code at its output.

The basic building blocks of the 4-bit flash are:

1. Resistive ladder.
2. Latch
3. Comparator.

5.2 Resistive Ladder

The resistive ladder is a string of sixteen 100K resistors that generates the differential reference voltage for the comparators. Larger resistors in the ladder minimize the power consumed by it. For one of the resistive ladders the top and bottom voltages are $1.65V$ and $0.15V$ respectively. For the other ladder it is the vice-versa. The voltage difference between two successive nodes of the resistive ladder is 93.75 mV. The LSB voltage of the flash ADC is twice this voltage and equals 187.5 mV. The center node of the two resistive ladders are at $V_{cm} = 0.9V$.

5.3 Latch

The latch consists of two back-to-back inverters as shown in figure 5.2.

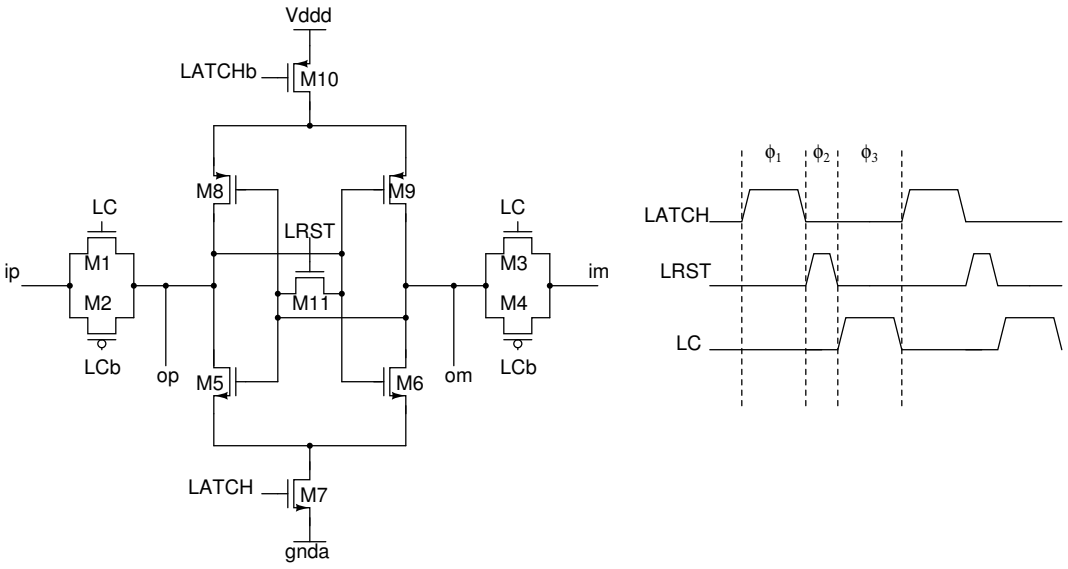


Figure 5.2: Regenerative latch

Transistor	W/L
M1,M2,M3,M4	1(0.24/0.18)
M5,M6,M7,M8,M9,M10	1(0.5/0.18)
M11	2(0.24/0.18)

The latch has a three phased operation. The three phases are:

1. Track
2. Regeneration and
3. Reset

In the track phase,ϕ_3, the parasitic capacitance at the inputs of the latch get charged to the differential input voltages ip and im. The latch as such is in the OFF state because the control signal 'LATCH' is low. Since no path exists between Vddd and gnda the latch burns zero static power in this phase.

In the regeneration phase, ϕ_1, the latch can be represented by a simplified circuit consisting of two back-to-back inverters, as shown in figure 5.3.

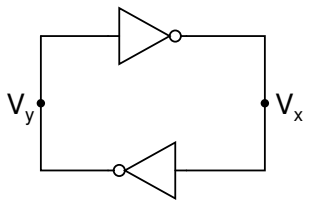


Figure 5.3: Simplified model in Regeneration phase

If the output voltages of the two inverters are close to each other at the end of the track phase, and the inverters are operating in the linear region , they can be modelled as voltage controlled current sources driving RC loads as shown in figure 5.4. A_v is the low-frequency gain of each inverter and is equal to $g_m R_L$, where g_m is the inverter's transconductance.

For the linearized model

$$\frac{A_v}{R_L}V_y = -C_L(\frac{dV_x}{dt}) - \frac{V_x}{R_L} \tag{5.1}$$

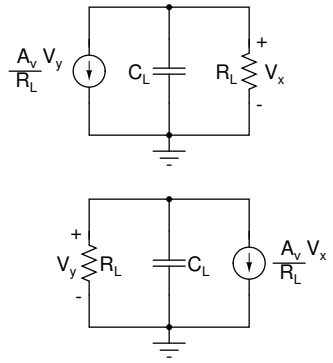


Figure 5.4: Linearized model in Regeneration phase

and

$$\frac{A_v}{R_L}V_x = -C_L(\frac{dV_y}{dt}) - \frac{V_y}{R_L} \tag{5.2}$$

Solving equations (5.1) and (5.2)

$$\frac{\tau}{A_v - 1}\frac{d\Delta V}{dt} = \Delta V \tag{5.3}$$

where $\Delta \mathrm{V} = V_x - V_y$ is the voltage difference between the output voltages of the inverters and $\tau = R_L C_L$ is the time constant at the output node of each inverter.

Equation (5.3) is a first-order differential equation whose solution is:

$$\Delta V = \Delta V_0 e^{(A_v - 1)t/\tau} \tag{5.4}$$

where ΔV_0 is the voltage difference at the end of the track phase. Thus, the voltage difference increases exponentially in time with a time constant given by

$$\tau_{latch} = \frac{\tau}{A_v - 1} \cong \frac{R_L C_L}{A_v} = \frac{C_L}{g_m} \tag{5.5}$$

If ΔV_{logic} is the necessary voltage difference to be obtained in order for the succeeding logic circuitry to safely recognize the correct output value, then the

time required for this to happen is given by:

$$T_{latch} = \frac{C_L}{g_m} ln(\frac{\Delta V_{logic}}{\Delta V_0}) \tag{5.6}$$

If ΔV_0 is small, this latch time will be large and perhaps greater than the allowed time for the regeneration phase. The differential output voltage of the latch does not increase enough to be recognized as the correct logic value by succeeding circuitry. This is referred to as *metastability*.

In the reset phase,ϕ_2, the outputs of the latch are re-initialized to the common mode voltage of the latch. It is important to ensure that no memory is transferred from one decision cycle to the next. If the latch toggles in one direction it might have a tendency to stay in that direction. This is referred to as *hysteresis*. In order to eliminate it, the latch outputs are reset before entering the track mode.

Due to random mismatches in the threshold voltages of the transistors in the latch, the latch has an offset voltage. For, the latch to give correct decisions at its output the difference between its input voltage must be greater than the offset voltage of the latch. The offset voltage of the latch due to random mismatches can be calculated as follows:

Let g_{mp} and g_{mn} denote the transconductances of the PMOS and NMOS transistors forming the cross-coupled inverter pair in the latch respectively. Let ΔV_{tp} and ΔV_{tn} denote the variation in the threshold voltage of the PMOS and NMOS transistors about their nominal value respectively. The output offset current of the cross coupled inverter pair due to the random mismatches is given by:

$$I_{offset} = g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn} \tag{5.7}$$

The output offset current can be represented by an equivalent input offset voltage given by:

$$V_{offset} = \frac{g_{mp}\Delta V_{tp} + g_{mn}\Delta V_{tn}}{g_{mp} + g_{mn}} \tag{5.8}$$

Thus the standard deviation of the offset voltage of the latch is:

$$\sigma_{offset} = \frac{\sqrt{g_{mp}^2 \sigma_{V_{Tp}}^2 + g_{mn}^2 \sigma_{V_{Tn}}^2}}{g_{mp} + g_{mn}} \tag{5.9}$$

The sizes of transistors M5,6,8,9 should be chosen such that the random offset voltage of the latch is much smaller than the LSB voltage of the flash.

5.4 Comparator

The latch discussed in the previous section is the basic building block of the comparator shown in figure 5.5.

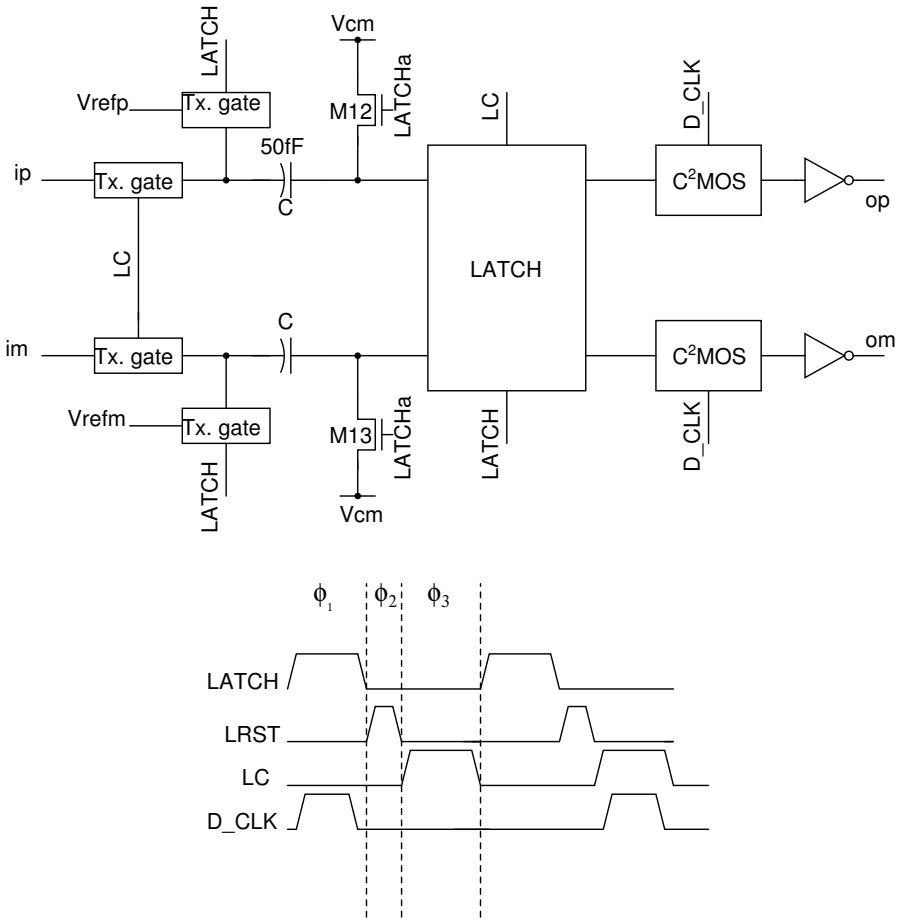


Figure 5.5: Comparator

During phase ϕ_1 the bottom plate of the capacitors get connected to the reference voltage and the top plate gets connected to Vcm. At the end of phase ϕ_1

Transistor	W/L
TX gates	1(0.24/0.18)
M12,M13	1(0.24/0.18)

the total charge on the upper capacitor is given by:

$$C(Vcm - Vrefp) \tag{5.10}$$

and that on the lower capacitor is :

$$C(Vcm - Vrefm) \tag{5.11}$$

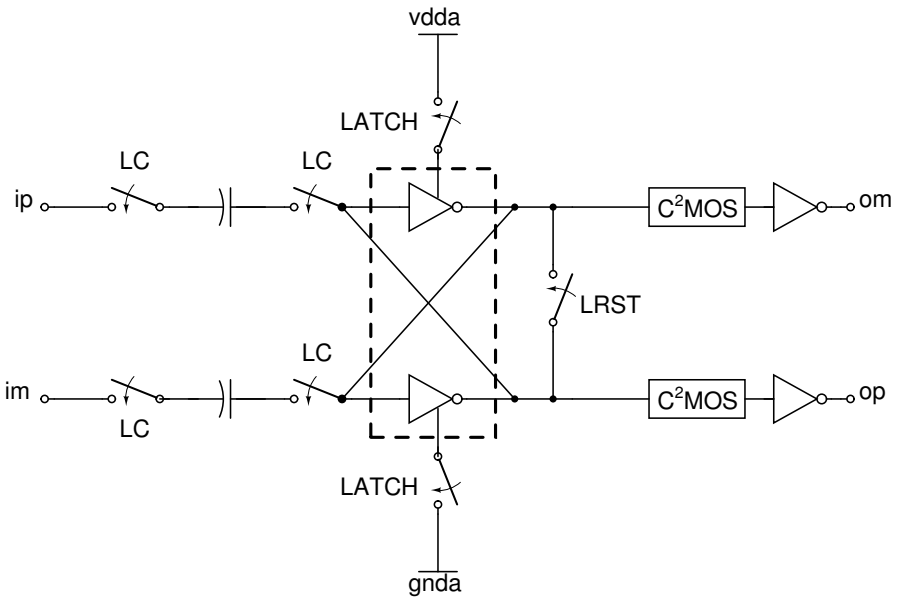


Figure 5.6: Comparator in phase ϕ_3

In phase ϕ_3 the bottom plates of the capacitor are connected to the inputs while the top plates are floating. Since the total charge on the capacitors must be conserved the voltage at the two inputs of the latch are:

$$Vcm + (V_{ip} - V_{refp}) \tag{5.12}$$

and

$$Vcm + (V_{im} - V_{refm}) \tag{5.13}$$

In this phase the regenerative latch is in the track mode as explained in the earlier section.

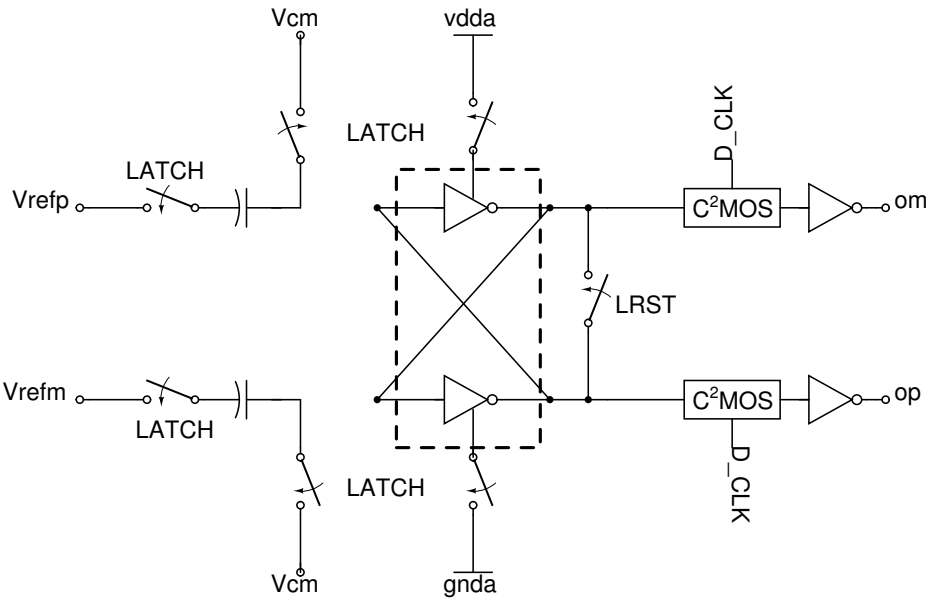


Figure 5.7: Comparator in phase ϕ_1

In phase ϕ_1 the latch goes into the regeneration mode. The positive feedback action in the latch forces its output to go high when $(V_{ip} - V_{im}) > (V_{refp} - V_{refm})$ i.e. when the differential input voltage exceeds its differential reference voltage. The comparator gives both true and complementary outputs. At the same time the capacitor at the input gets charged to $V_{refp/refm} - Vcm$. The C^2MOS latches the output of the latch after the regeneration is complete.

After the regeneration is over, the outputs of the latch are reset in phase ϕ_2 to prepare it for the next conversion cycle.

The comparator is connected to the resistive ladder only during ϕ_1. In this phase the comparator draws a small amount of transient current from the ladder to charge the 50fF capacitor. In order to minimize the variation in the ladder node voltages, each ladder node is connected to ground by a 1pF capacitor.

5.5 Flash Clocks

The operation of the Flash requires a pair of nonoverlapping clocks - LATCH and LC. These clocks determine when the charge transfer occurs and they must be non-overlapping in order to guarantee proper operation of the flash.

One simple method for generating nonoverlapping clocks is shown in figure 5.8. Inverting the clocks CK_a and CK_b gives the nonoverlapping clocks. The delays t_{d1} and t_{d2} are realized using a cascade of even number of inverters. The two clocks at the output have the same frequency as the input clock signal.

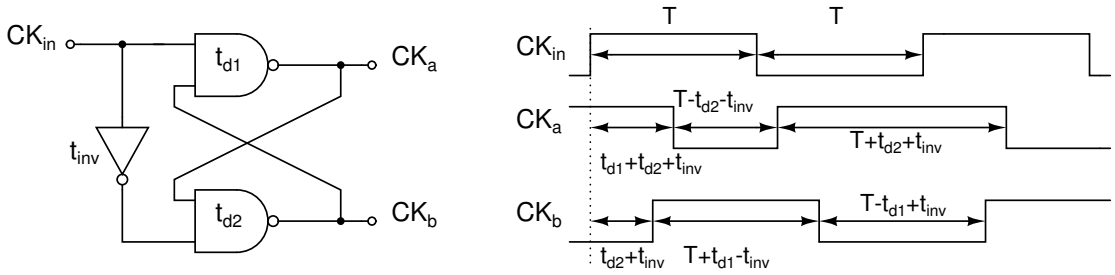


Figure 5.8: NAND clock generator

The latch reset pulse, LRST, must be of sufficient duration to reset the output of the latch to its common mode value. Failing to do so the comparator will take erroneous outputs due to hysteresis. The comparator will consume zero static power if it is ensured that the LRST pulse and the LATCH pulse are never high at the same time.

The clock to the C^2MOS, D_CLK, should go high only after the output of the latch has reached one of the two logic levels. The D_CLK pulse and the latch reset pulse should be nonoverlapping. Else, the output of the comparator would again be wrong.

CHAPTER 6

Feedback DAC

6.1 Introduction

The primary advantage of noise-shaping modulators employing multibit quantizers is that the quantization noise power reduces by 6dB for every additional bit. An additional benefit of multibit quantization is that it enhances system stability. But these gains comes at a price. The integral linearity of the noise shaping converter is no better than the integral linearity of the internal multibit DAC. For a DAC with 3-V full-scale and 16 bit resolution the DAC LSB voltage is about $46\mu V$. Hence, the permissible deviation of the DAC output levels from their ideal values is of the order of $23\mu V$!!!. To achieve such a high degree of linearity the DAC components must be precisely matched. However, CMOS VLSI process are optimized for high density digital design than high performance analog design.

This chapter discusses the design of the internal multibit DAC along with dynamic element matching (DEM) algorithms that help in relaxing the matching requirements of the internal DAC. Finally, the implementation of a DEM algorithm, data weighted averaging, is presented.

6.2 Internal DAC topology

The most common architecture for the internal DAC employs $2^N - 1$ parallel unit elements, where N is the number of bits of the internal quantizer. In such a DAC, the kth output level is generated by turning on k approximately equal valued elements and summing up their charges or currents. Figure 6.1 shows the schematic of the 4-bit DAC implemented in the design.

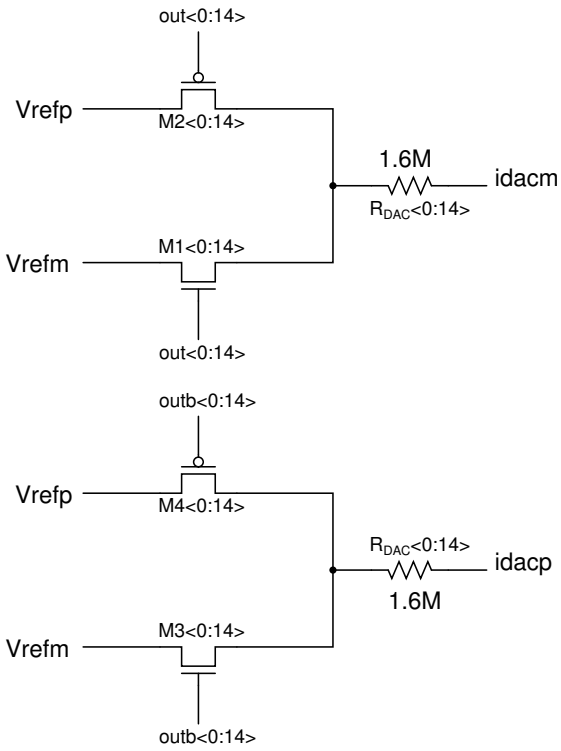


Figure 6.1: Internal DAC schematic

The DAC implemented in the design is a differential resistive DAC. A resistive DAC has been preferred over the conventional current steering DAC because it is less noisier and easier to implement. When the input control bit to any DAC element in the lower section is 1 it sources a current of half LSB while it sinks the same amount of current if the control bit is zero. The vice-versa is true for DAC cells in the upper section.

To illustrate the effect of nonideal DAC on the the $\Delta\Sigma$ DAC, a fourth order modulator with an internal quantizer of 4-bits was simulated for an ideal DAC and the same DAC with 1% mismatch in the DAC components. The output power spectrum of the ADC in the two cases is shown in figure 6.2.

When the DAC is nonideal the low frequency noise shaping of the $\Delta\Sigma$ modulator is lost and harmonics related to DAC errors appear at the output of the modulator within the signal bandwidth. To reduce these effects dynamic matching techniques (DEM) are applied.

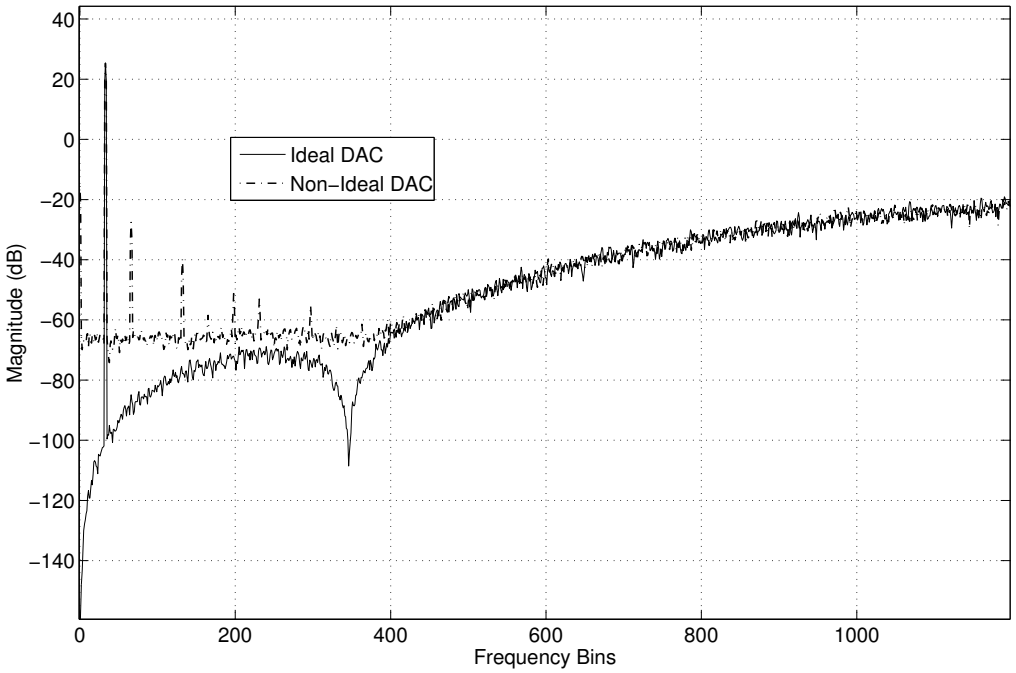


Figure 6.2: Magnitude Spectra for a fourth order $\Delta\Sigma$ modulator using a DAC with 1% component mismatches

6.3 Dynamic Element Matching(DEM)

DEM aims to modulate mismatch errors away from the signal bandwidth in order to remove them by post filtering. The DAC elements are selected in such a way that the DAC errors sum to zero over multiple sample instances. The static DAC errors are converted into a wide-band noise signal. This can be explained by considering the case of a 3 element DAC in which element 1 is 1% high, element 2 is 3% low and element 3 is 2% high. For any given digital output code the error remains fixed. Figure 6.3 shows the error at the output of the DAC, as a fraction of full scale, for the digital input sequence of 0,1,1,1,1,1,1,1,2,2,2,2,2,3. The numbers at the top indicates the elements that are ON for that clock period.

By choosing the DAC elements at random the DAC error at the output averages out to zero quickly thereby moving the distortion due to DAC component mismatch to higher frequencies. Subsequent filtering leaves the signal band free of distortion. Two different DEM techniques are discussed in this section.

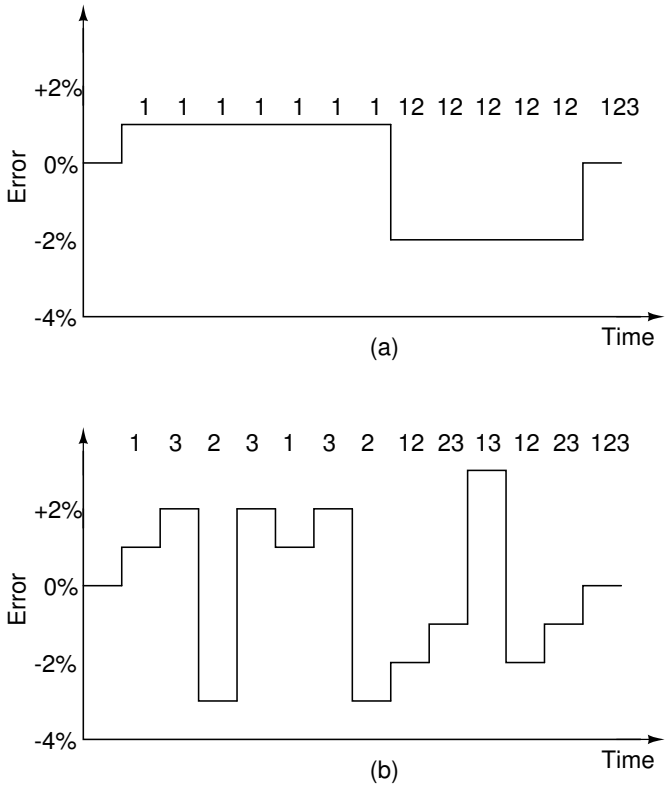


Figure 6.3: DAC output:(a)no DEM and (b) DEM for element selection

6.3.1 Randomization

When the different DAC elements are selected at random, as was the case in the above example, the system linearity is improved because only a portion of the noise falls in the signal bandwidth. This is because the DAC distortion becomes white and is spread uniformly in the entire spectrum as shown in figure 6.4.

With ideal randomization, there will be no correlation between the mismatch error at one time and mismatch error at any other time. Therefore, the mismatch error gets converted into a white noise. A linear feedback shift register randomizes the order in which the DAC elements are chosen.

6.3.2 Data Weighted Averaging (DWA)

The DWA technique uses all the DAC elements at the maximum possible rate. At the same time it ensures that each DAC element is used the same the number of times. This is done by sequentially selecting the DAC elements, beginning with

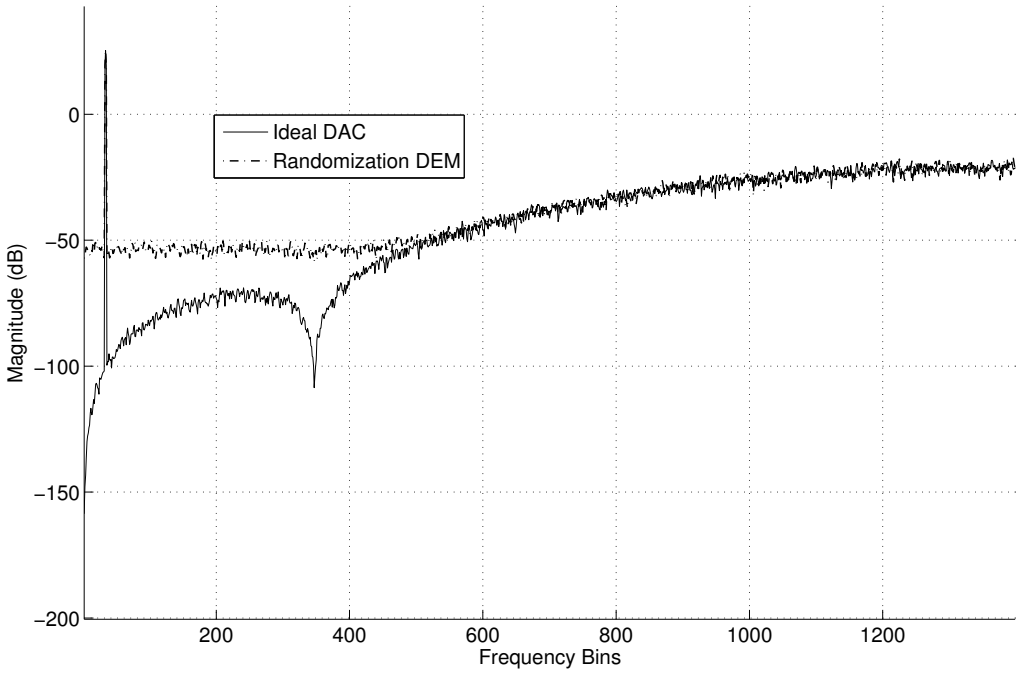


Figure 6.4: Magnitude Spectra for a fourth order $\Delta\Sigma$ modulator using randomization DEM

the next available unused element. Figure 6.5 explains the concept of the DWA algorithm.

The first three DAC elements are turned ON when the input bit pattern is 011 as shown in figure 6.5(a). When the input sequence 010 is applied the next two elements are turned on as shown in figure 6.5(b). Finally when the input sequence 100 is applied the last two DAC elements along with the first two are selected. This selection procedure continues as the input data is applied.

The element averaging is controlled only by the input sequence. Hence, this algorithm is called data weighted averaging. Since all the DAC elements are used at the maximum possible rate it ensures that the DAC errors quickly sum to zero thereby moving distortion to higher frequencies. Figure 6.6 shows the output spectrum of a DAC employing DWA with 1% component mismatch.

An added advantage of the DWA technique is that the distortion spectra from the DAC linearity errors are first order noise shaped [10]. This offers a dynamic range improvement of $9dB/octave$.

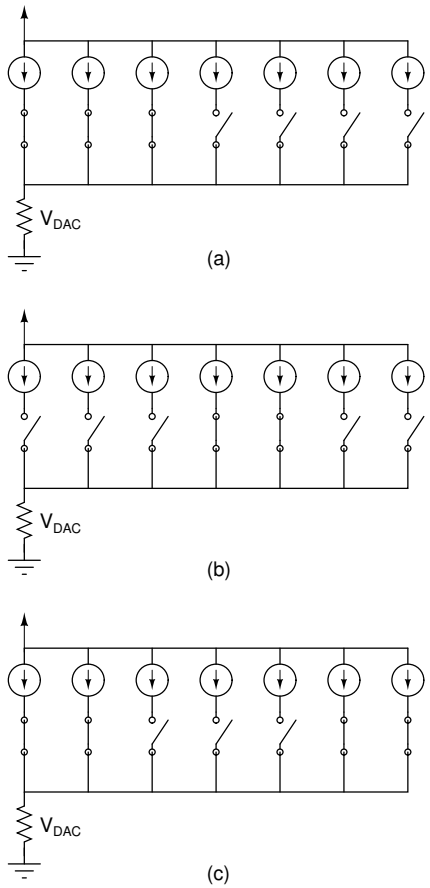


Figure 6.5: DWA element selection for a 3-bit DAC with an input sequence of 011,010,100

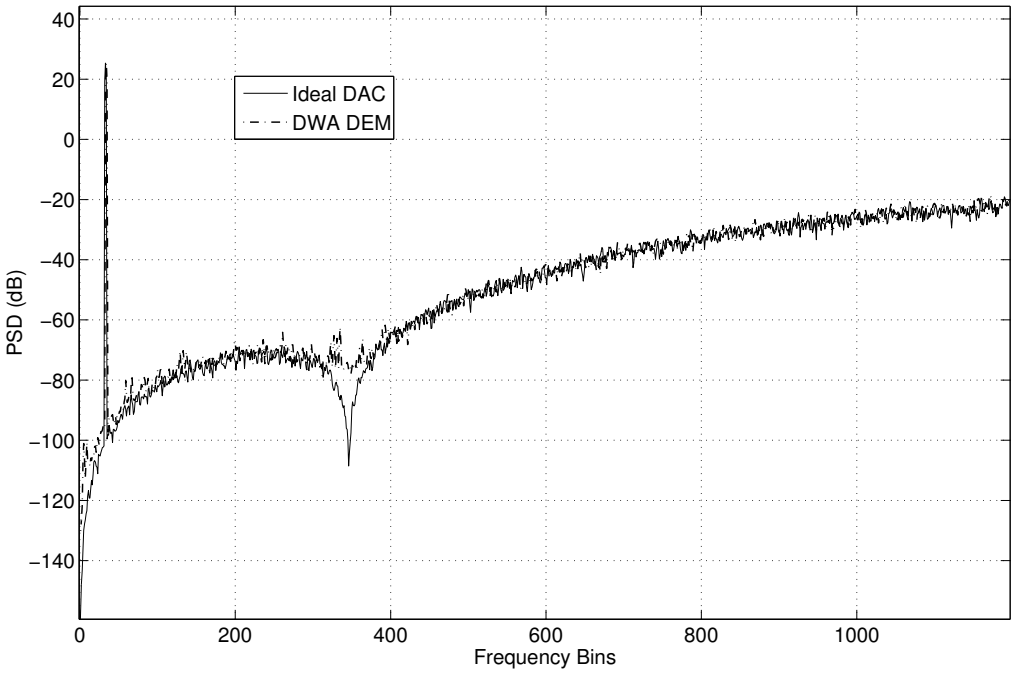


Figure 6.6: Magnitude Spectra for a fourth order $\Delta\Sigma$ modulator using data weighted averaging DEM

6.4 DWA Implementation

The DWA algorithm not only offers better performance than other DEM techniques, it is also simple to implement. Figure 6.7 shows the block diagram of DWA algorithm implemented in the design.The basic building blocks are:

1. Thermometer to Binary Converter
2. Accumulator
3. Barrel Shifter
4. Latch

6.4.1 Thermometer to Binary Converter

The flash ADC gives a 15-bit thermometer code at its output. A thermometer code can be converted to its binary equivalent by counting the number of ones in

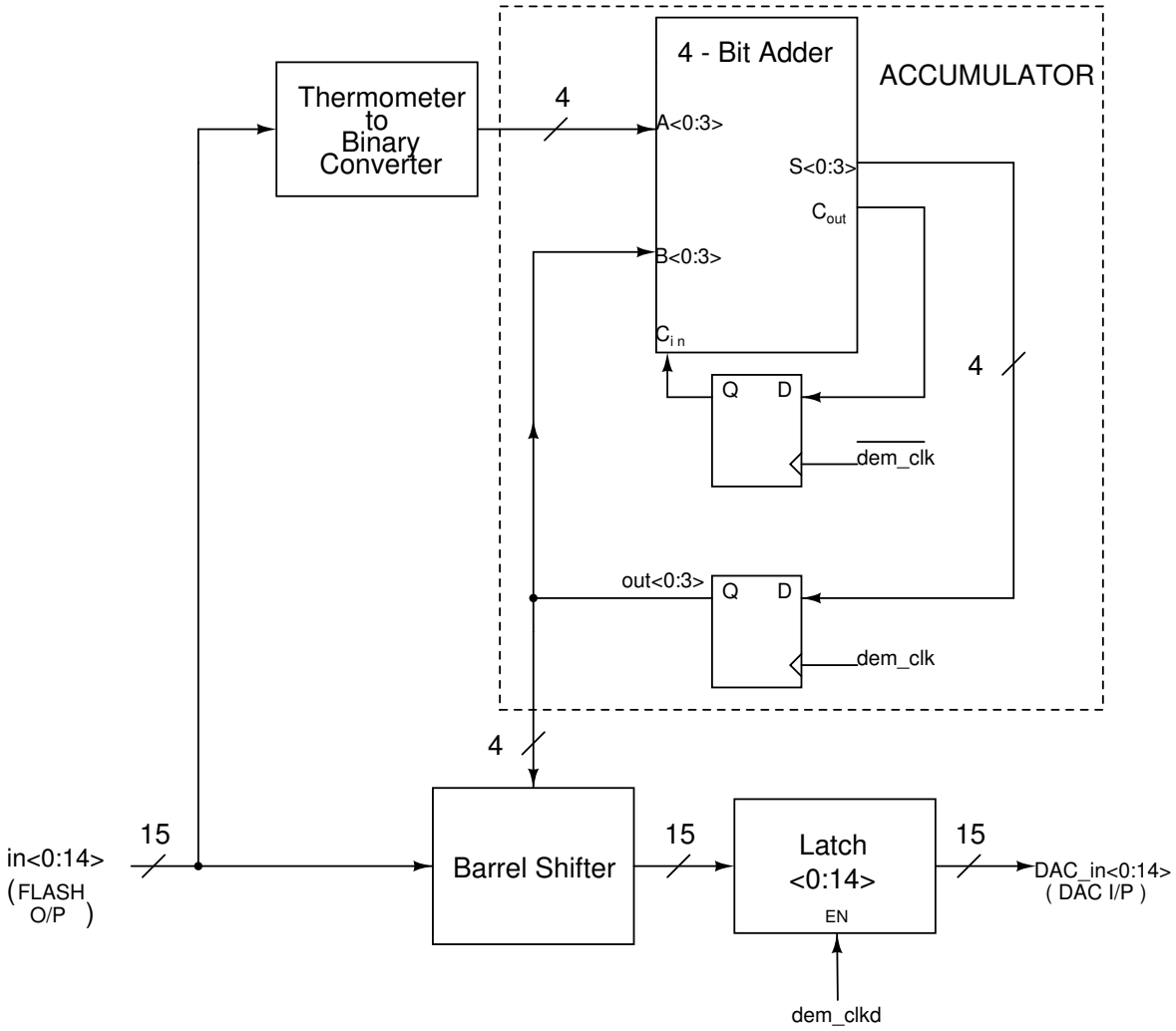


Figure 6.7: Schematic for the DWA implementation

it. In figure 6.8 the 2-bit adders and the 3-bit adder have been built using a basic full adder cell. The multi-bit adders have ripple carry architecture.

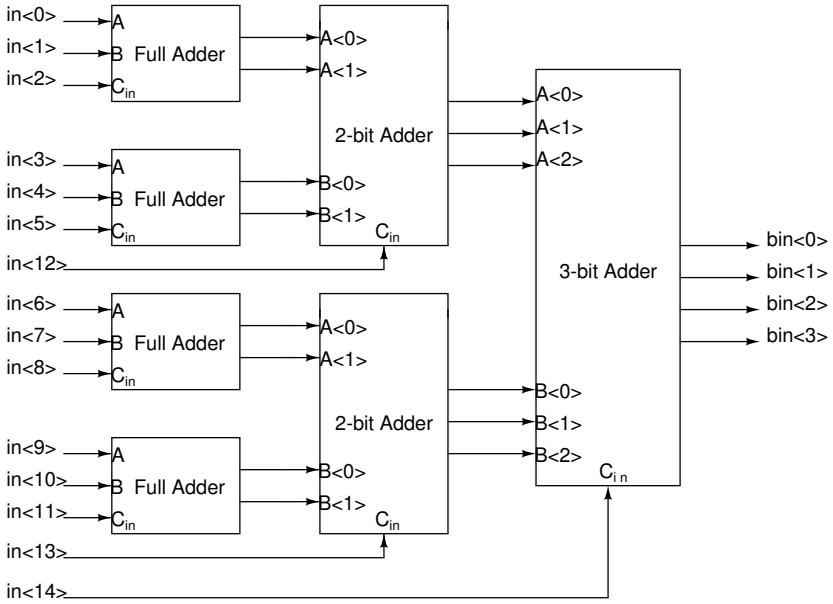


Figure 6.8: Thermometer to Binary Converter

6.4.2 Accumulator

The accumulator generates the control signals for turning on the basic current cells of the DAC, starting with the next available unused element. The DAC is thermometer coded. The operation of the accumulator is illustrated with the help of an example. Let the 15 basic DAC current cells be labelled CS1,CS2...,CS14 and CS15.

Current Pointer Ptn.	**Input Data**	**Accumulator Output**	**Updated Pointer Ptn.**
CS1	0011	0001 + 0011 = 0100	CS4
CS4	0101	0100 + 0101 = 1001	CS9
CS9	1000	1001 + 1000 = 10001	CS2 (17 MOD 15 =2)

The pointer points to the next available unused element.

The first three DAC elements are selected when the input sequence 0011 is applied. The next available unused element is obtained by summing the Current

pointer position 1 with the input pattern 0011. This gives the updated pointer position CS4.

When the input sequence 0101 is applied DAC elements CS4 to CS8 are selected. The output of the accumulator is 1001 which gives the updated pointer position CS9.

When the next data sequence 1000 is applied the last 7 DAC elements CS9 to CS15 and the first DAC element CS1 are activated. The updated pointer position is calculated as follows:

When dem_clk goes high the carry bit of the accumulator output is set to 1 and the the remaining 4-bits are 0001. When dem_clk goes low the sum and carry outputs of the accumulator are added. This gives the updated pointer position CS2.

6.4.3 D-flip flop

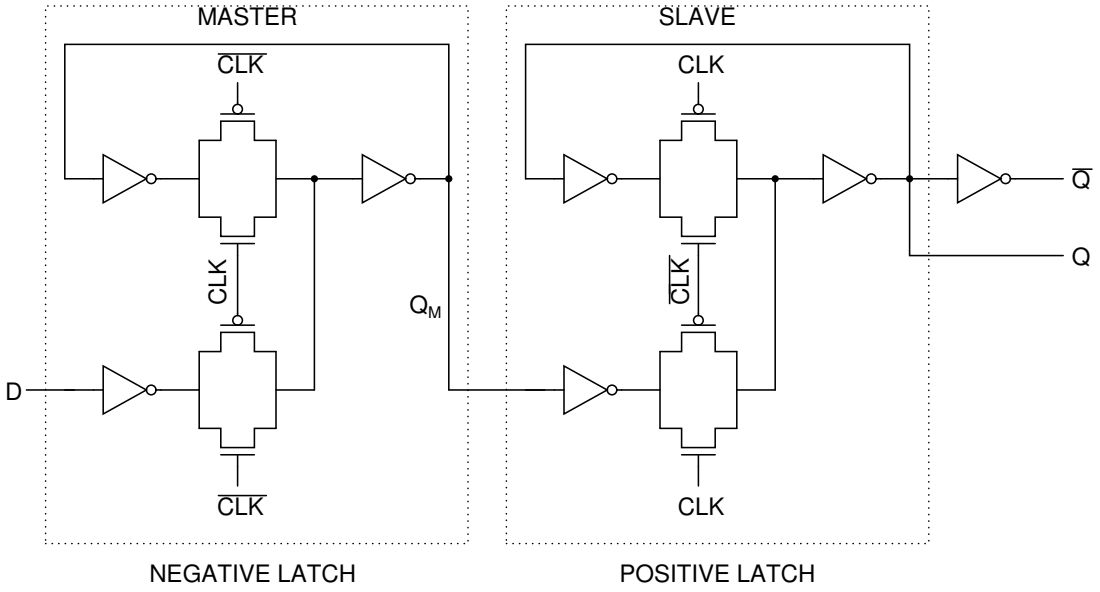


Figure 6.9: D-flip flop schematic

On the low phase of the clock the master stage is transparent, and the D input is passed to the master stage output Q_M. During this phase the slave stage is in the hold mode. On the rising edge of the clock, the master stage stops sampling the input, and the slave stage starts sampling. The value of Q is the value of

D right before the rising edge of the clock, achieving the positive edge triggered effect.

6.4.4 Barrel Shifter

Figure 6.10 shows the block diagram of the barrel shifter implemented in the design. The input to the barrel shifter is the 15-bit thermometer code generated by the internal flash ADC. The barrel shifter has four stages. Each stage is built using 16 multiplexers.

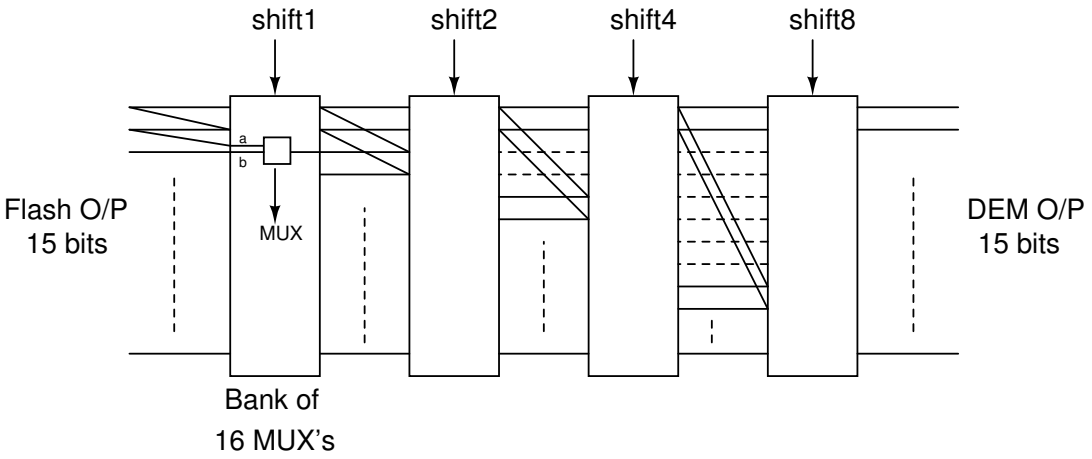


Figure 6.10: Barrel Shifter

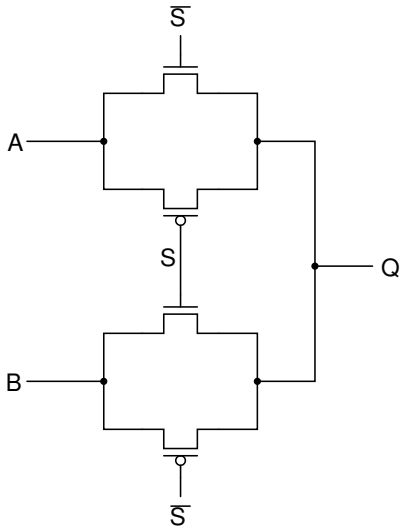


Figure 6.11: Multiplexer schematic

The control signals for the barrel shifter are generated by the accumulator.

The nth stage circularly rotates its 15-bit input by 2^{n-1} if its control signal is 1. Else the stage output is the same as its input.

6.4.5 Latch

The output of the barrel shifter will contain glitches since each input bit pattern gets delayed differently by the chain of full adders in the accumulator. A latch samples the output of the barrel shifter after it has settled to its final value. The clock to the latch is a delayed version of the clock applied to the accumulator. The outputs of the latches are the control signals that turn ON and OFF the basic cells of the resistive DAC. Figure 6.12 shows the schematic of the positive latch.

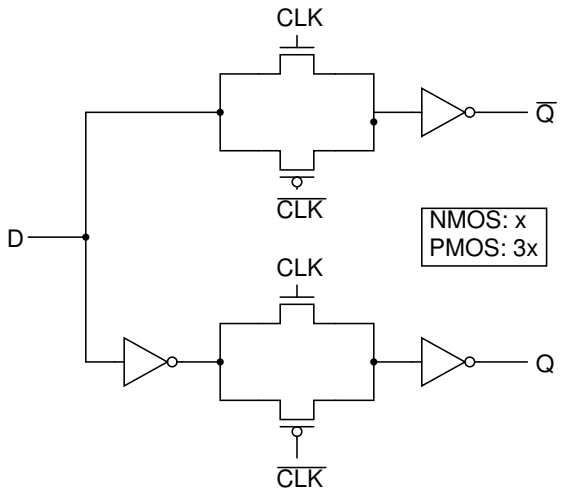


Figure 6.12: DAC latch

Ideally there should be no skew between the true and complementary clocks to the latch. Any skew between these clocks will lead to a skew between Q and $\bar{Q}$. Skew between Q and $\bar{Q}$ causes distortion at the output of the modulator because the differential DAC cells do not turn ON or OFF simultaneously. The NMOS to PMOS transistor sizing in the latch is 1:3 so that Q and $\bar{Q}$ have approximately equal rise and fall times.

CHAPTER 7

Reference Generator

This chapter discusses the design of the reference voltages and currents for the designed modulator. The different references that need to be generated are:

1. The reference voltages for the internal flash ADC. The top and bottom node of the resistive ladder are held at 1.65 V and 0.15 V respectively.

2. The references for the feedback DAC. The feedback DAC must be capable of sourcing as well as sinking a current of around $7\mu A$.

3. The reference currents for the loop filter op amps. Each loop filter op amp has an input bias current of $125nA$.

7.1 Generation of Reference Currents

Figure 7.1 shows the schematic that is used for generating reference currents for the various blocks of the reference generator. The inputs to the reference generator are - a bias current of $500nA$ and an input voltage of $0.9V$ denoted as Vcm_cc in figure 7.1. The input bias current is mirrored to generate the tail current of $500nA$ for op amp R1. The negative feedback around R1 forces the voltage across the $1.8M$ resistor to be equal to $0.9V$. The current through M1 is mirrored to M3 via M2 and to M8 via M7. Hence, M3 is a current source of $500nA$ while M8 a current sink of $500nA$. The currents through M2 and M7 can be mirrored to create more current sources and sinks respectively.

The current through M7 is mirrored to M9. The negative feedback around opamp R2 forces the drain voltage of M4 to $1.65V$. The current through M4 is mirrored to generate current sources of $8\mu A$ (M5) and $2.375\mu A$ (M6). Similarly

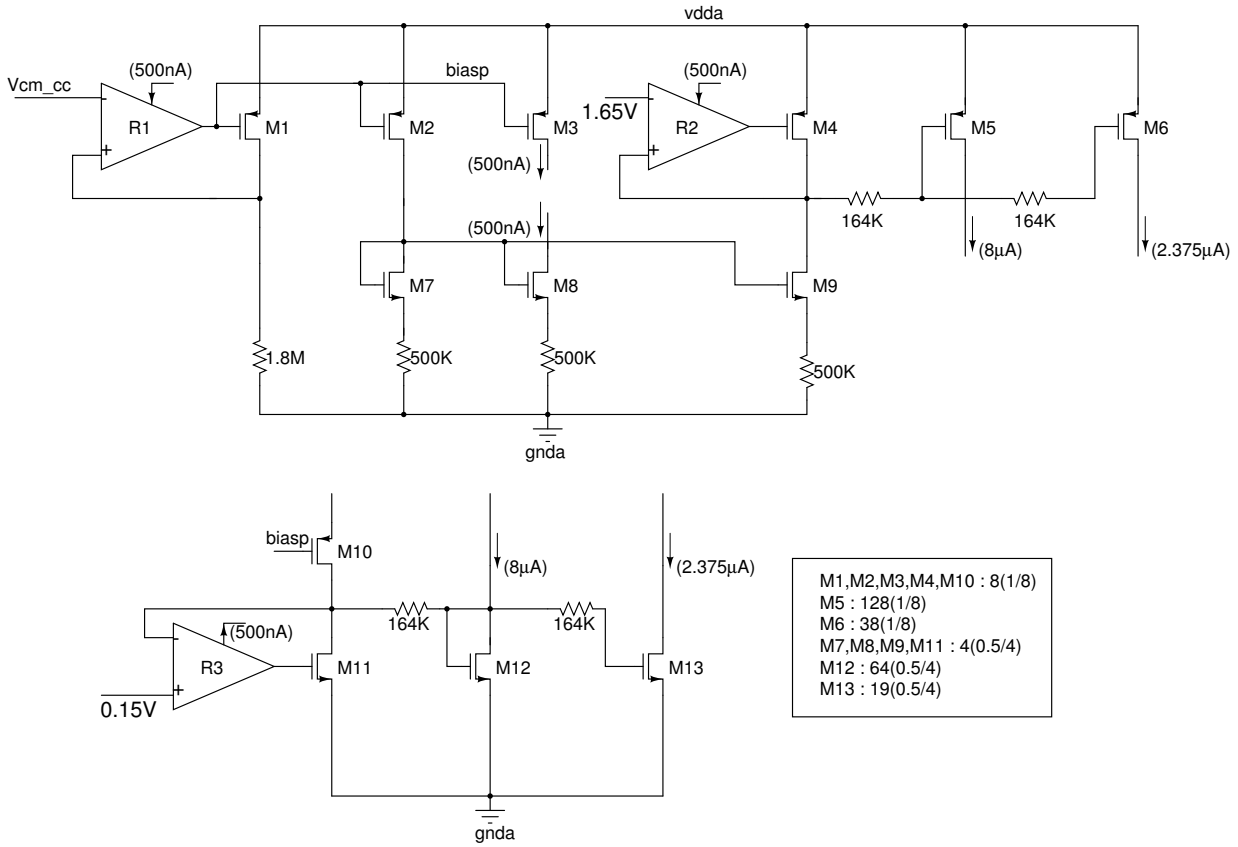


Figure 7.1: Generation of reference currents

the negative feedback around op amp R3 forces the drain voltage of M11 to $0.15V$. M12 and M13 serve as current sinks of $8\mu A$ and $2.375\mu A$ respectively.

The reference voltages for op amps R2 and R3 are generated using a resistive divider. Op amps R2 and R3 are single stage op amps. They require a tail current of $500nA$ which is generated internally. The resistors connected to the gate of M5, M6, M12 and M13 forms a low pass filter with the gate capacitors of the corresponding transistors. This helps in filtering out the noise in the reference generator.

7.2 ADC References

The reference voltages for the flash ADC are generated using the arrangement shown in figure 7.2. The op amp shown in the figure 7.2 has an identical architecture to that of the first op amp of the loop filter.

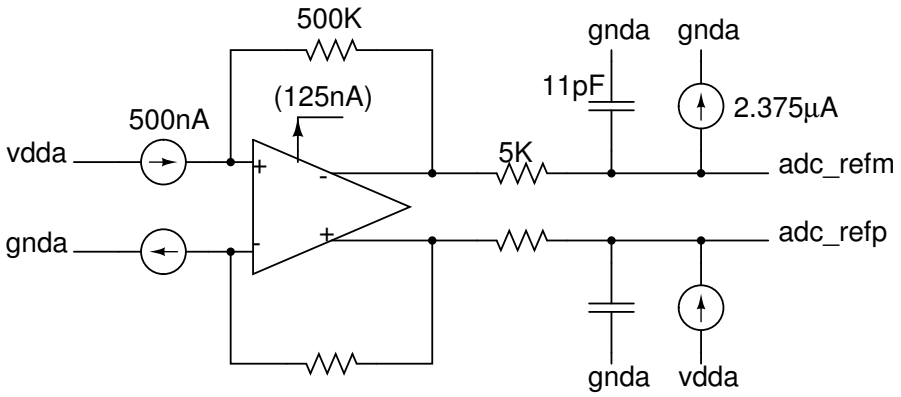


Figure 7.2: Generation of ADC references

The voltage drop across the 500K resistors is $0.75V$. The CMFB loop of the op amp forces its output voltages to $1.65V$ and $0.15V$. A low pass filter is connected at the output of the op amp to filter out any noise present in the ADC references. Since, the flash ladder requires a current of $2.375\mu A$ the opamp ideally need not supply any current. The currents used in the generation of ADC references are generated by the current generators discussed in the previous section.

The ADC references are noisy due to the periodic switching of the flash comparator. The flash comparator is connected to the resistive ladder for only one phase of the input clock as explained in chapter 5. Whenever the comparator connects to the ladder it draws a small amount of current from it. The noise generated by the switching of the comparator is noise shaped by the loop filter.

7.3 DAC References

Eventhough the flash and the DAC require the same references they are generated separately. This is because if the flash references were used for the DAC then any noise in the flash references will appear directly at the output of the DAC. The internal DAC should have the same resolution as the overall resolution of the converter. Hence, the references for the ADC and the DAC are generated independently.

The DAC references are generated using the arrangement shown in figure 7.3. The op amp used in the schematic is identical to the first op amp of the loop filter.

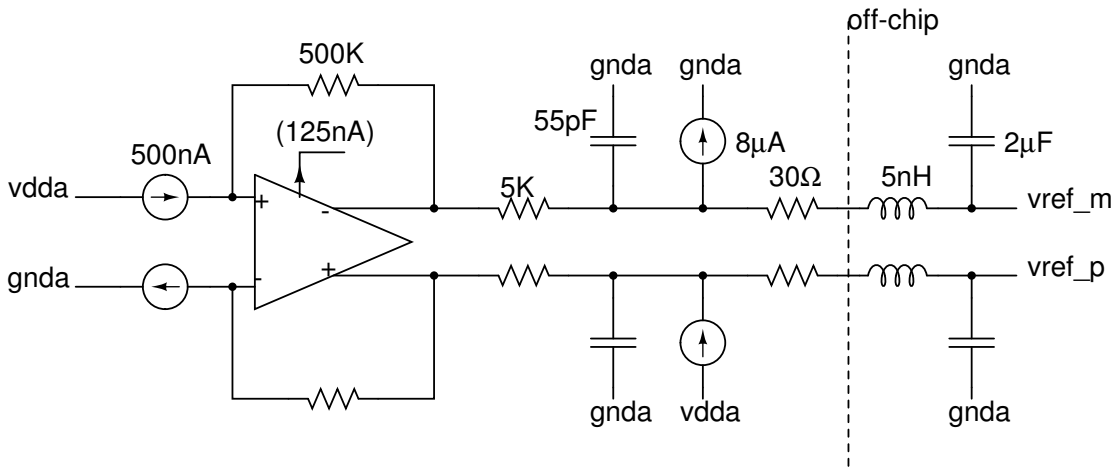


Figure 7.3: Generation of DAC references

The CMFB loop of the op amp forces its output voltages to $1.65V$ and $0.15V$. The ouput node vref_p sources a current of $7.5I_{LSB}$ to the DAC while the node vref_m sinks the same amount of current, where I_{LSB} is the DAC LSB current. The DAC references need to be precise and should have minimum noise due to the switching of the DAC. This is because the noise in the DAC references is not shaped away from the signal band by the loop filter. Hence, an off-chip capacitor of $2\mu F$ is conncted to ground from both DAC reference voltages. This forms a low pass filter with the internal $5K$ resistor which has a cut-off frequency of $16Hz$. Thus, any noise in the frequncy range of interest, 20Hz - 24KHz, gets filtered out.

The off-chip inductor of $5nH$ is due to the bond pads and the packaging interconnects. At high frequencies this inductor forms a LC circuit with the internal $55pF$ capacitor because of which the reference generator begins to oscillate. To reduce the Q of the resulting tank circuit a 30Ω resistor is connected in series with the off-chip capacitor.

The op amp R2 in the reference current generation section is necessary to ensure that the drain voltage of transistor M4 is set to $1.65V$. This is because transistors M5 and M6 which source currents to the DAC and ADC respectively have their drains held at $1.65V$ by the output CMFB loop of the op amp. The matching of the drain voltages is necessary to ensure exact mirroring of currents. Similarly op amp R3 ensures that the drain voltage of M11 is equal to the drain voltage of M12 and M13 which sink currents fom the DAC and ADC respectively.

Without op amps R2 and R3 there will be large errors in the currents sourced and sinked to the ADC and the DAC.

7.4 Op Amp Bias Currents

The loop filter opamps along with op amps used for generating ADC and DAC references require a tail current of $125nA$. The tail current for these op amps is generated using the circuit shown in figure 7.4.

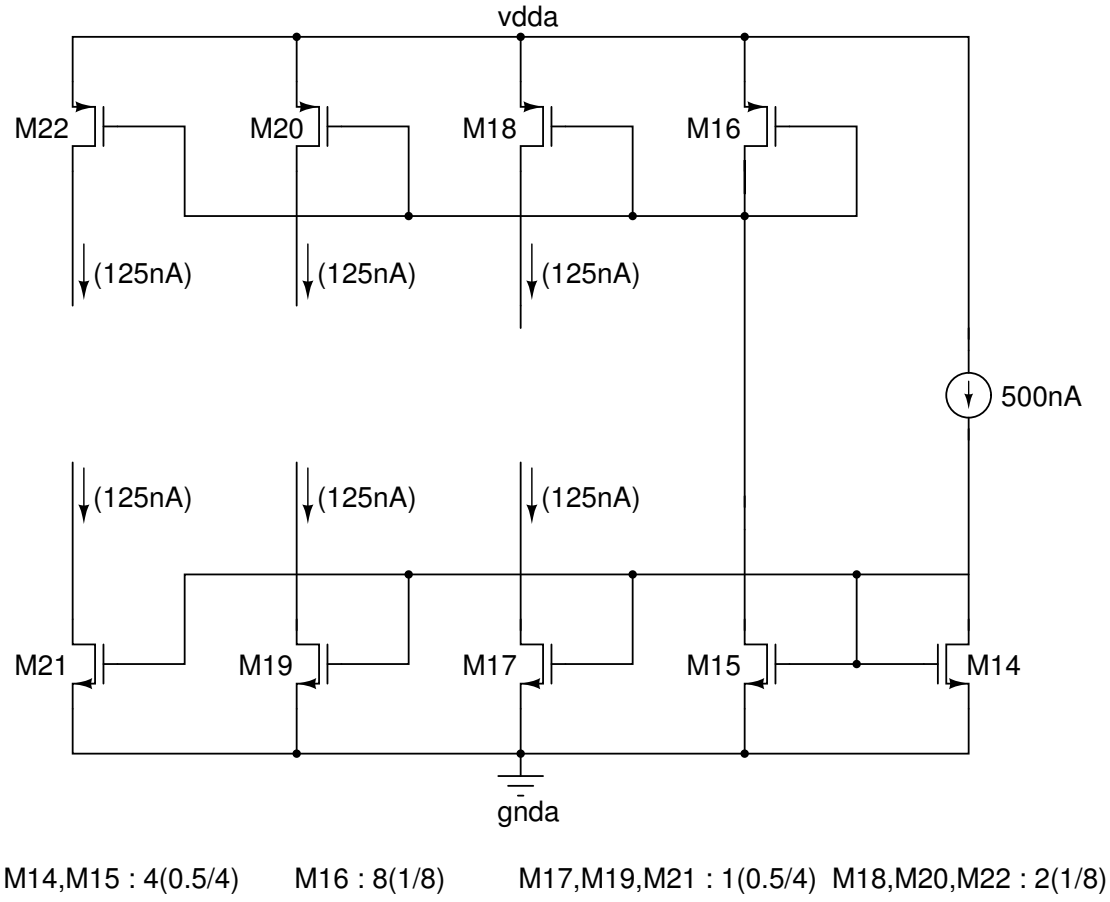


Figure 7.4: Generation of op amp bias currents

Transistors M18, M20 and M22 provide the bias current to op amps I2, I3 and I4 of the loop filter, M17 supplies the tail current to op amp I1 of the loop filter and M19 and M21 provide the reference current to the op amps used in the generation of ADC and DAC references.

CHAPTER 8

Layout, Simulation Results and Conclusions

8.1 Layout

The designed third order CT $\Delta\Sigma$ modulator was laid out in CADENCE along with the associated tuning circuitry. The top level layout of the design is shown in figure 8.1. It occupies an area of $0.8mm^2$.

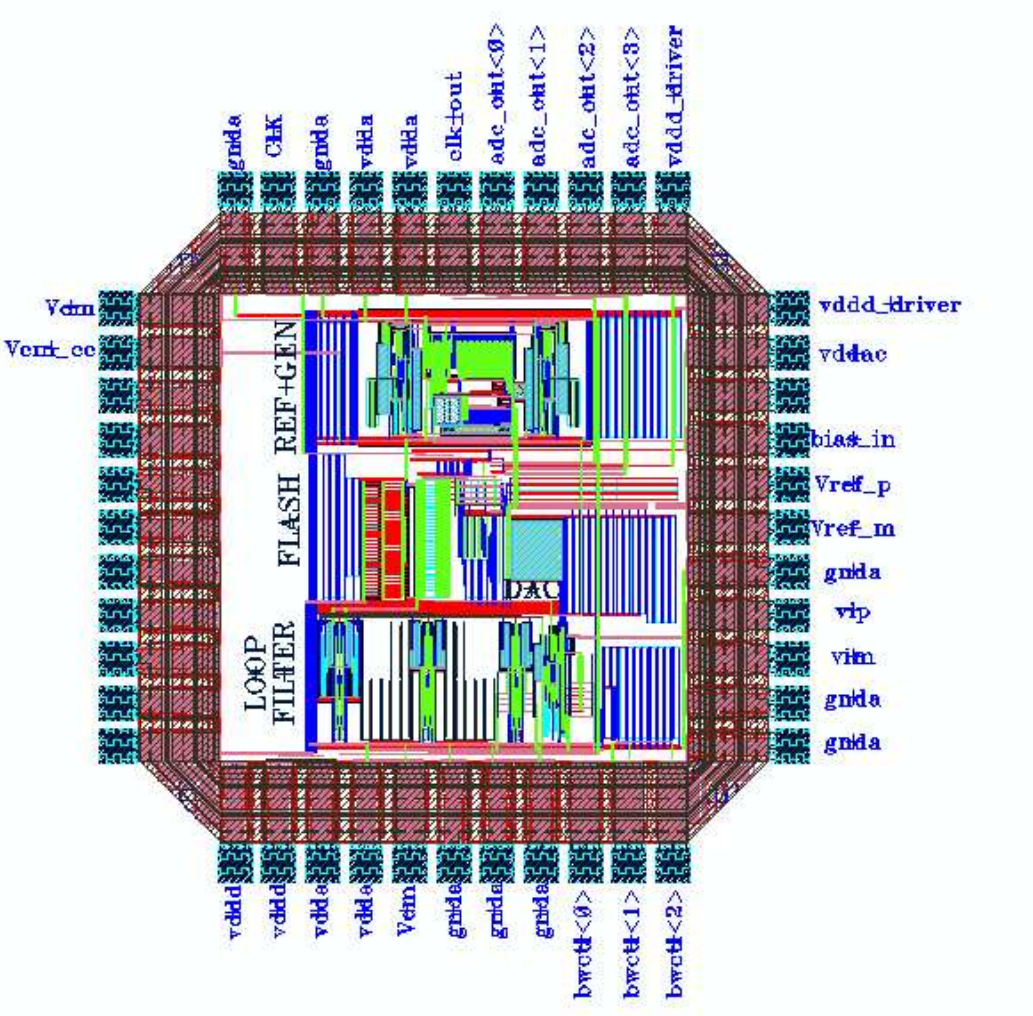


Figure 8.1: Chip layout

Pin	Description
vip, vim	Differential input to the modulator
CLK	Input clock at $3.072MHz$
bias_in	$500nA$ input bias current
bwctl$\langle 2:0 \rangle$	Control signals for tuning the integrating capacitors of the loop filter
Vcm_cc	External voltage of around $0.9V$ for on-chip generation of a precise $500nA$ current source
Vcm	$0.9V$ Reference voltage source
vdda	$1.8V$ analog power supply
vddd	$1.8V$ digital power supply
vdddac	$1.8V$ power supply for the internal clock generator
vddd_driver	$1.8V$ power supply for the output CMOS drivers
adc_out$\langle 3:0 \rangle$	4-bit output of the modulator
clk_out	Clock for synchronizing the ADC output
Vref_p,Vref_m	DAC references
gnda	Circuit ground

Table 8.1: ADC pin-out

8.2 Simulation Results

A CT delta-sigma modulator is very intensive on simulation time. In order to ease this during the design and simulation phase each of the building blocks had an associated Verilog-A view or an ideal view wherein the functionality of the block was realized using ideal active elements. Thus during the design and simulation phase only a few blocks can be run at the transistor level. This greatly reduces the design iteration time.

The results of the various simulations run on the design is tabulated below. The input signal to the modulator is a $2.4V_{pp,d}$ sinusoid at a frequency of $6KHz$. The following notations are used in the table:

1. Ideal - Ideal view
2. Verilog - Verilog-A view
3. Schem - Schematic view

4. Extr - Extracted view

Loop filter	**Flash ADC**	**Clock Generator**	**DEM**	**DAC**	**References**	**HD2 (dB)**	**HD3 (dB)**
Ideal	Verilog	Ideal	Verilog	Schem	Ideal	112.8	125
Ideal	Verilog	Ideal	Verilog	Extr	Ideal	111.9	121
Ideal	Extr	Ideal	Verilog	Extr	Ideal	111.3	118.2
Ideal	Extr	Extr	Verilog	Extr	Ideal	126.6	114.8
Ideal	Verilog	Ideal	Extr	Schem	Ideal	111.3	128
Extr	Verilog	Ideal	Verilog	Schem	Ideal	111.3	117.6
Extr	Schem	Ideal	Verilog	Schem	Ideal	113.1	110.5
Extr	Extr	Ideal	Verilog	Extr	Ideal	112.3	128.1
Schem	Schem	Ideal	Verilog	Extr	Extr	112.1	108.3
Extr	Schem	Ideal	Verilog	Extr	Extr	107.6	110.5

Table 8.2: Simulation Results

The SNR in each of the above simulation setups was found to be in excess of 100 dB. The designed ADC hence, has a resolution of 16-bits. The output PSD of the modulator when extracted views are used for all the building blocks listed above except the reference generator for which ideal view is used is shown in figure 8.2.

The power consumption statistics of the designed modulator is presented below:

Source	Current	Power
vdda	$54\mu A$	$97.2\mu W$
vddd	$20\mu A$	$36\mu W$
vddac	$13\mu A$	$23.4\mu W$
Total	$87\mu A$	$157\mu W$

Table 8.3: ADC power consumption

The achieved specifications of the ADC are tabulated below:

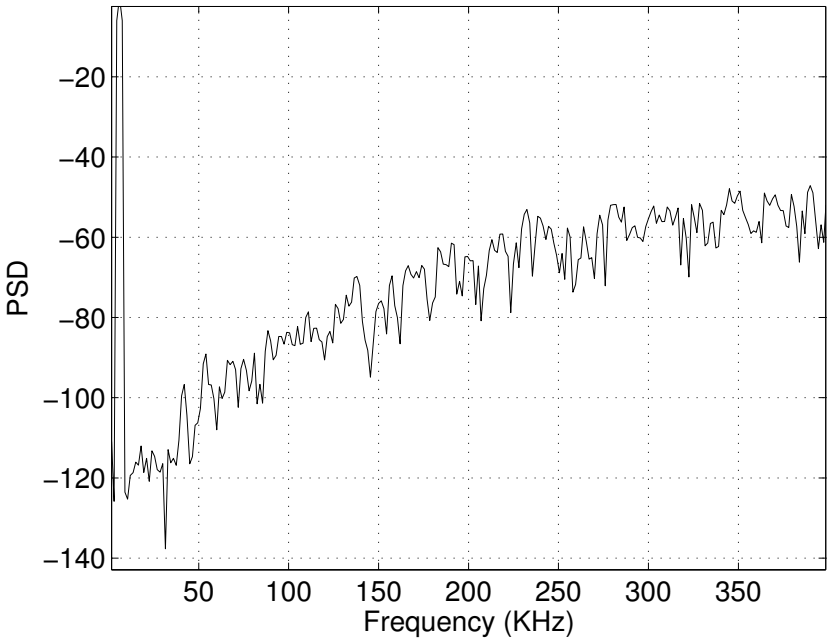


Figure 8.2: PSD of modulator output

Feature	Achieved Specification
Resolution	16-bits
SNR	106 dB
Sampling rate	$3.072MHz$
Signal bandwidth	$24KHz$
Power dissipation	$157\mu W$

Table 8.4: Achieved ADC specifications

8.3 Conclusions

A low power 3rd order CT $\Delta\Sigma$ modulator for high-fidelity digital audio applications has been designed. Feed forward architecture is used for the loop filter to reduce the power consumption. In addition, the loop filter op amps are operated in the subthreshold region for further minimizing the power consumed by the modulator. Moreover, the 4-bit flash ADC has a salient feature that it consumes almost zero static power. The integrating capacitors of the loop filter can be tuned externally to make the modulator work across all process corners and temperature variations. The DWA algorithm has been implemented in the design of the feedback DAC which greatly relaxes the matching requirements across the various DAC levels and provides first-order noise shaping of the DAC mismatch. Simulations over the design show that the modulator is expected to have 16-bit resolution. The design has been successfully laid out and sent for fabrication.

8.4 Future Work

There are certain avenues for improvement in this design. Firstly, the total power burnt by the modulator can be reduced by minimizing the power consumed by the analog section. Secondly, on chip tuning of the integrating capacitors can be implemented. These improvements will certainly make the modulator an *unique* state of the art ADC.

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