WIDELY PROGRAMMABLE OPAMP-RC FILTERS

A Project Report

submitted by

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CERTIFICATE

This is to certify that the report titled **Widely Programmable Opamp-RC Filters**, submitted by **M. N. V. Prasadu**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this report, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Finally, I would like to thank my parents who are always a constant source of inspiration for me. This work is dedicated to them for their eternal love and support.

ABSTRACT

This thesis discusses the design of widely programmable high frequency continuous-time opamp-RC filters.

Previous authors such as Harrison has investigated ways of overcoming bandwidth restrictions of opamp, favoring opamp-RC filters over Gm-C filters for bandwidths above 10 MHz. However, the scaling techniques proposed by Harrison suffers from passband droop while scaling down the bandwidth. Constant capacitance scaling technique has been extended to opamp-RC filters to reduce the pass band droop considerably.

A state space model of the filter was developed using quasi-static model of MOSFET. MATLAB optimization routine is used to fit the filter response, obtained from state space model, to ideal in face of opamp nonidealities and parasitic capacitances.

An opamp-RC filter was designed in deep submicron CMOS process. The opamp-RC filter achieves a cutoff frequency of 300 MHz and an input signal swing of 2.2 Vp-p for -40dB distortion. The dynamic range achieved is 57.4 dB.

A segmentation model was developed to extend the validity of quasi-static models to RF simulations. The model uses BSIM3v3 quasi-static model. The model predicts non-quasi-static effects of MOSFET at high frequencies when used to simulate a 500 MHz Gm-C filter.

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CHAPTER 1

INTRODUCTION

Opamp-RC filters have potential dynamic range advantages over Gm-C filters since feedback can allow a larger signal swing with acceptable linearity. Radio receiver applications have notably high dynamic range requirements, as large blocking signals may be present in the adjacent channels.

Signal swings of transconductor based filters[1] are limited to less than a volt. This provides sufficient dynamic range for hard-disk-drive disk read channels, but is marginal for communications applications. The opamp bandwidth restrictions have favored Gm-C filters over 10 MHz. But these restrictions can be overcome using opamp architecture proposed in ([2], p.105). This work presents the design of widely programmable 43-300 MHz lowpass opamp-RC Chebyshev filter with 1 dB passband ripple. This filter allows high dynamic range at such frequencies.

Still, frequency scaling of opamp-RC filters is not as trivial as that of Gm-C filters, which can be precisely scaled using constant-C scaling ([3],[1]). Resistor tuning alone, won't achieve precise frequency scaling as the opamps are not ideal. Simple resistor tuning causes droop in frequency response as we scaledown the bandwidth ([2], p.108). In this work, efforts are made to extend constant-C scaling technique to opamp-RC filters.

Quasi-static model of MOSFET breaks down if input changes are too fast ([4], p.347). As suggested by authors like Tsividis, one way to extend the validity of Quasi-static models is to consider MOSFET as connection of several short devices, and to model each segment quasi-statically. For filters with cutoff frequencies close to 500 MHz, these non-quasi-static effects are prominent. Finally, a segmentation model is developed which models MOSFET as three smaller segments in series. The model uses BSIM3v3 quasi-static model. The model is used to simulate 500 MHz Gm-C lowpass filter[1].

1.1 Organization of Thesis

Chapter 2 explains the realization of opamp-RC filter from RLC ladder filter prototype with 1 rad/sec cutoff frequency.

Chapter 3 explains the design of basic building blocks of the filter.

Chapter 4 explains the state space model of the filter. This chapter also explains the optimization routines used to fit filter response to ideal.

Chapter 5 gives the simulation results for the extracted layout of the filter.

Chapter 6 explains the modeling of Non-quasi-static effects of MOSFET using segmentation model. The model is also used to simulate a 500 MHz Gm-C filter[1]. The simulation results are compared with those obtained by Quasi-static model.

CHAPTER 2

ARCHITECTURE OF OPAMP-RC FILTER

This chapter explains the realization of the filter architecture from RLC ladder filter with cutoff frequency of 1 rad/sec and with 1 dB passband ripple. Sections 2.1 and 2.2, explains how inductor and resistor can be realized using transconductors and capacitor. Section 2.3 presents how ladder filter is converted to opamp-RC filter.

2.1 Realization of inductor

2.1.1 Single ended inductor

A singly terminated inductor can be realized using two transconductors and a capacitor, as shown in the figure 2.1. Equating the looking in impedance at node

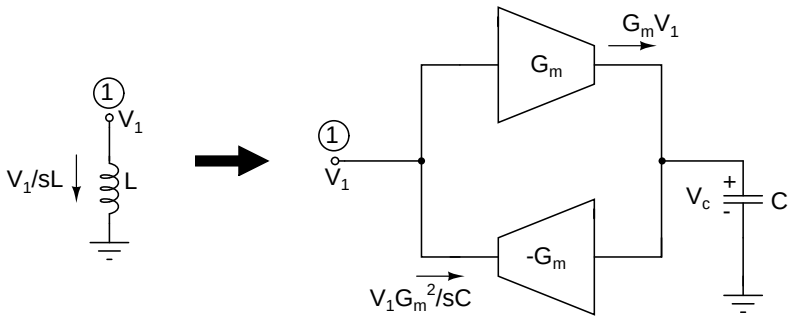


Figure 2.1: Realization of single ended inductor

1, in both the cases shown figure 2.1, we have:

$$\frac{1}{sL} = \frac{{G_m}^2}{sC} \tag{2.1}$$

$$L = \frac{C}{{G_m}^2} \tag{2.2}$$

2.1.2 Double ended inductor

Similarly, a double ended inductor can be realized using two single ended architectures, as shown in the figure 2.2. In this case also, the equivalent inductance

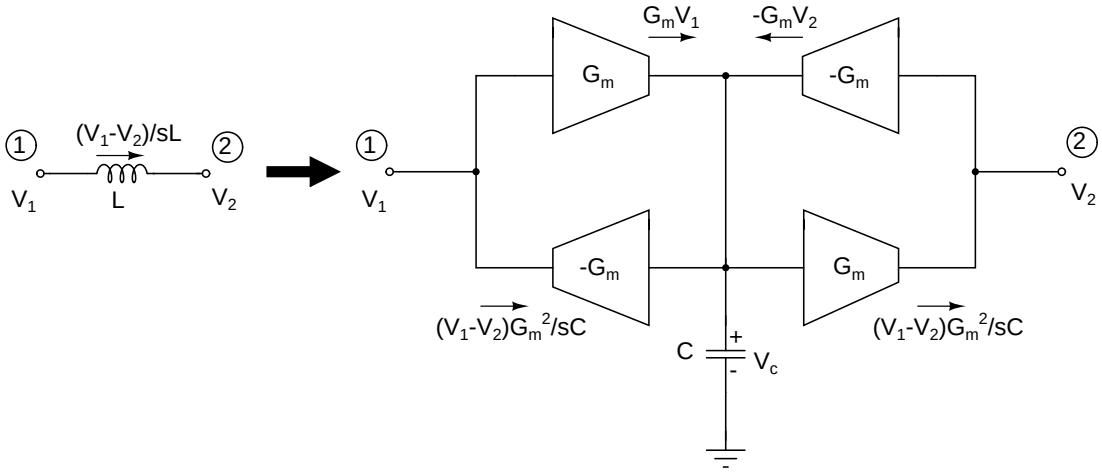


Figure 2.2: Realization of double ended inductor

between nodes 1 and 2 is given by,

$$L = \frac{C}{{G_m}^2} \tag{2.3}$$

2.2 Realization of resistor

Resistor can be realized using transconductors as shown in figure 2.3. The resistor, realized using this architecture, serves only half the purpose of a resistor. The architecture models only the net resistive current flowing into node 2. The prime requisite is that, a current of $\frac{V_1 - V_2}{R}$ should flow into node 2, which can be met by choosing $G_m = \frac{1}{R}$. Node 1 of figure 2.3 will be the input node of figure 2.4.

2.3 Filter architecture

The architecture of opamp-RC filter is derived from the ladder filter, shown in figure 2.4. It has a cutoff frequency of 1 rad/sec and a pass band ripple of 1 dB.

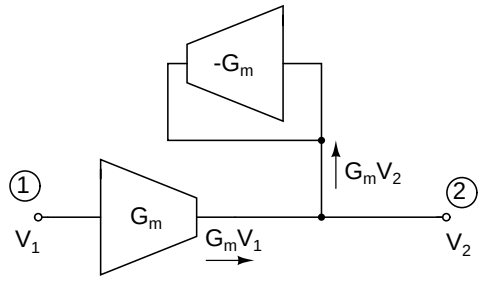


Figure 2.3: Realization of resistor

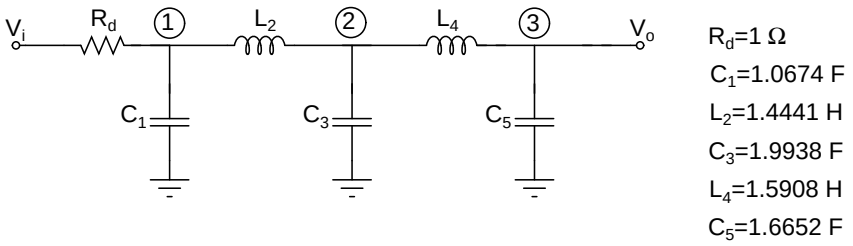


Figure 2.4: Singly terminated ladder filter

2.3.1 Frequency & impedance scaling

The ladder filter, shown in figure 2.4, is frequency scaled to 300 MHz, by the following transformation:

$$L \rightarrow \frac{L}{\omega_{new}} = \frac{L}{2\pi \times 300 \times 10^6} \tag{2.4}$$

$$C \rightarrow \frac{C}{\omega_{new}} = \frac{C}{2\pi \times 300 \times 10^6} \tag{2.5}$$

After frequency scaling, the new inductor and capacitor values are given below: $C_1 = 566.27\ pF$, $L_2 = 766.12\ pH$, $C_3 = 1057.74\ pF$, $L_4 = 843.94\ pH$, $C_5 = 883.42\ pF$. As these capacitor values are too large to realize, the network is impedance scaled by a factor of $k = 1666.67$, using the transformations given below.

$$R \rightarrow k \times R = 1666.67 \times R \tag{2.6}$$

$$L \rightarrow k \times L = 1666.67 \times L \tag{2.7}$$

$$C \rightarrow \frac{C}{k} = \frac{C}{1666.67} \tag{2.8}$$

Resulting ladder filter is shown in figure 2.5.

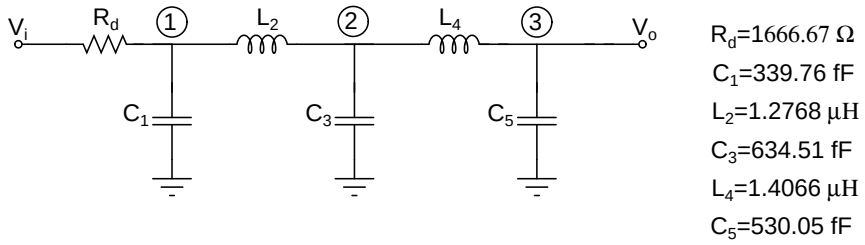


Figure 2.5: Frequency and impedance scaled version of ladder filter

Actually this holy number of $k = 1666.67$ is arrived at after many scalings. First Gm is chosen to be 4 mS, same as in 500 MHz Gm-C filter[1]. Next the bandwidth is scaled down to 300 MHz, by reducing Gm to 2.4 mS and then the total power is scaled down by a factor of four, resulting in final Gm=600 μS. Corresponding R_d value is 1666.67 Ω.

2.3.2 Gm-C architecture

RLC ladder filter, shown in figure 2.5, is converted into Gm-C filter by replacing both inductors with their corresponding Gm-C architectures. The resistor is also replaced with it's corresponding G_m architecture.

The value of G_m is chosen to be 600 μS. The values of C_1, C_3 and C_5 remain unchanged. The values of C_2 and C_4 are obtained using formula 2.3.

$$C_2 = L_2 \times {G_m}^2 = 1.2768\ \mu H \times 600\ \mu S^2 = 459.65\ fF \tag{2.9}$$

$$C_4 = L_4 \times {G_m}^2 = 1.4066\ \mu H \times 600\ \mu S^2 = 506.25\ fF \tag{2.10}$$

The Gm-C filter, shown in figure 2.6, has five Gm-C integrators, with negative feed back from one stage to it's preceding stage. The first integrator has a local feed back.

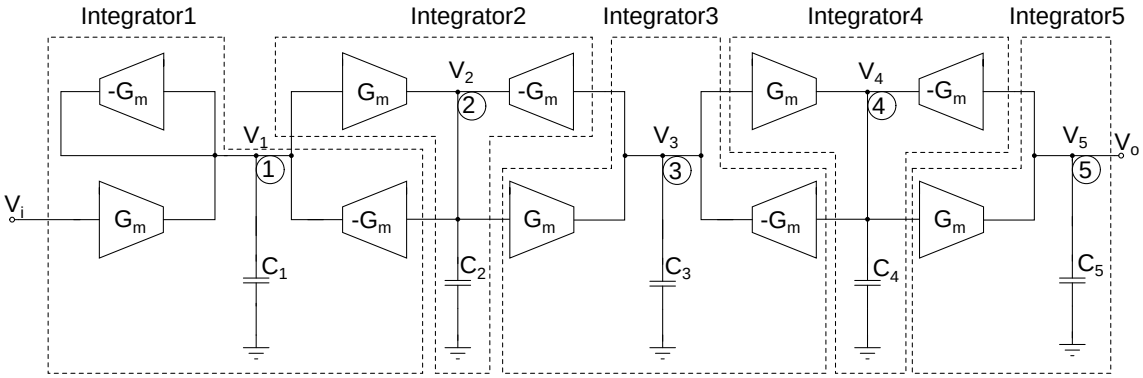


Figure 2.6: Gm-C architecture of the filter

2.3.3 Opamp-RC architecture

Each Gm-C integrator is replaced by opamp-RC integrator with $R_i = \frac{1}{G_m}$. The differential version of the opamp-RC architecture is shown in figure 2.7

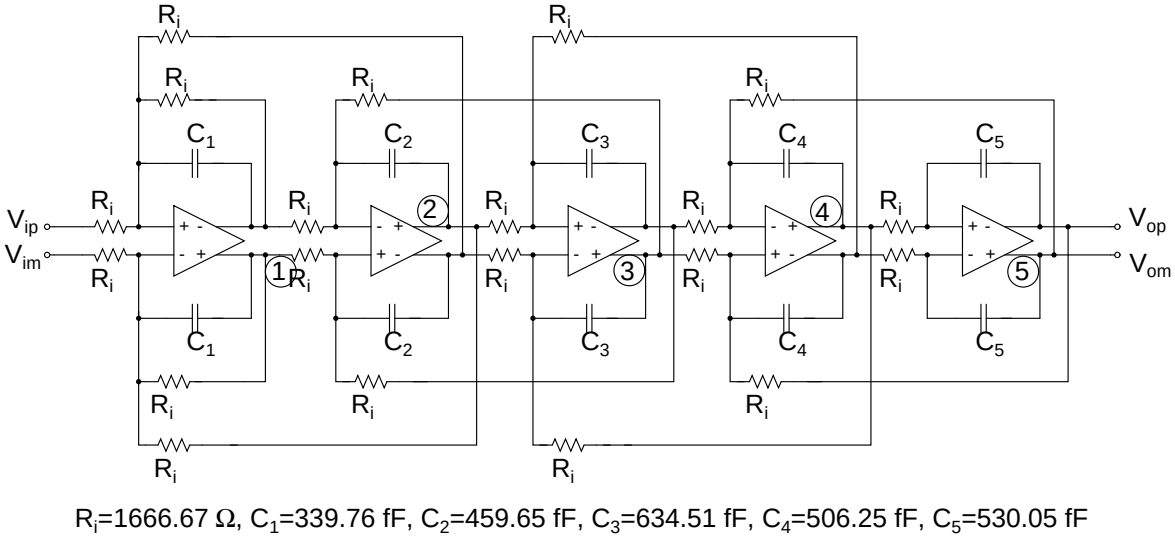


Figure 2.7: Opamp-RC architecture

2.3.4 Nodescaling

Node scaling ensures that the signal swing at all the five nodes, shown in figure 2.6, is maximized, but less than the maximum swing at the output node. This maximizes the dynamic range at each node. Node scaling can be done by adjusting

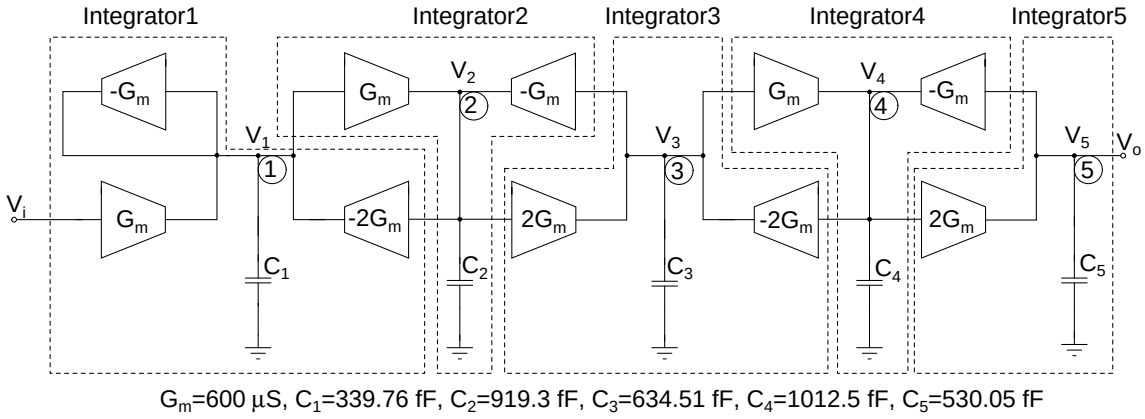


Figure 2.8: Node scaled Gm-C filter

integrating capacitors and transconductors, in such a way that the total transfer function remains unaltered. The swing at a particular node can be reduced by decreasing effective impedance at that node, i.e, by increasing the integrating capacitance at the node by a factor α. This leads to a reduction in the current supplied by the transconductors feeding out from the node, affecting the total transfer function. To avoid this, G_m of transconductors feeding out from the node are raised by the same factor α.

Node scaled version of Gm-C filter is shown in figure 2.8 and it's corresponding opamp-RC filter is shown in figure 2.9. R_z is used, in series with integrating capacitor, to minimize the effect of right half plane zero. The effect of R_z is clearly explained in appendix-A. Initially R_z is chosen to be $1/g_{m3} = 1/(6.86\ mS) = 145\ \Omega$. Integrating capacitors and R_z are further tweaked to fit the filter response to ideal, as explained in chapter 4. The final optimized values of integrating capacitors and R_z are given below:

$$C_1 = 401.85\ fF \tag{2.11}$$

$$C_2 = 898.74\ fF \tag{2.12}$$

$$C_3 = 692.29\ fF \tag{2.13}$$

$$C_4 = 873.18\ fF \tag{2.14}$$

$$C_5 = 410.97\ fF \tag{2.15}$$

$$R_z = 79.3\ \Omega \tag{2.16}$$

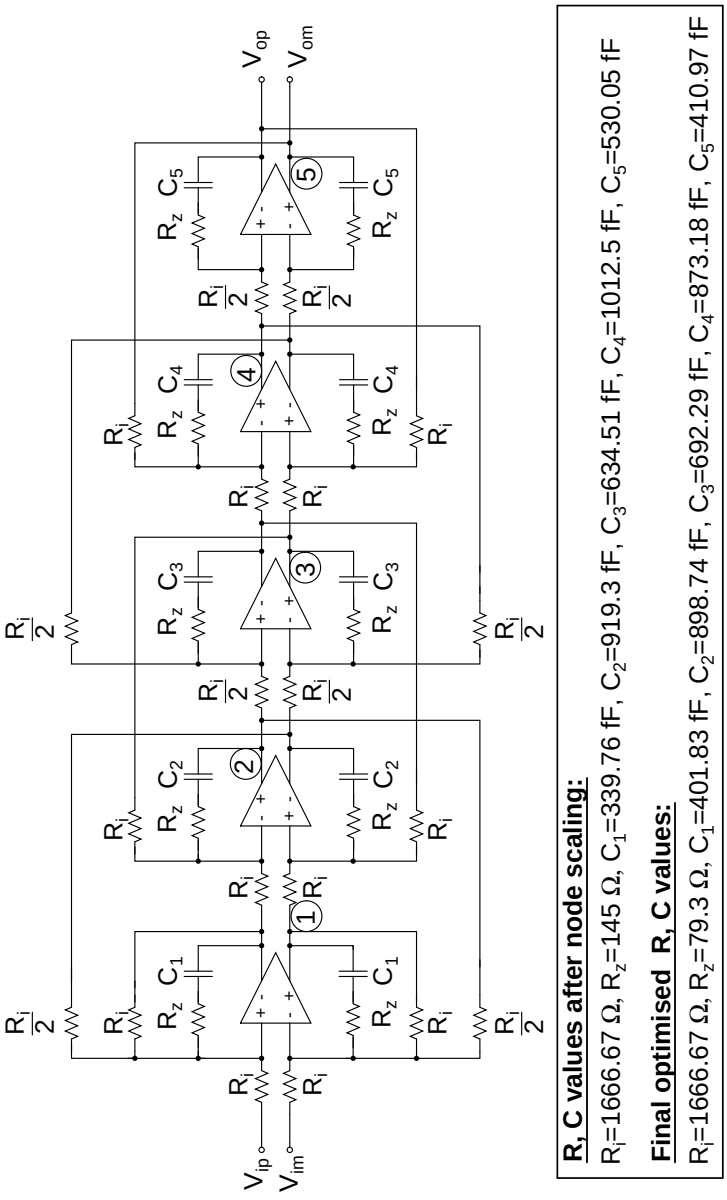


Figure 2.9: Node scaled opamp-RC filter

CHAPTER 3

FILTER DESIGN

3.1 Opamp design

The basic architecture of opamp is taken from the PhD thesis of J.N.Harrison[2]. Figure 3.1 shows the schematic of the opamp([2], p. 105). The opamp is con-

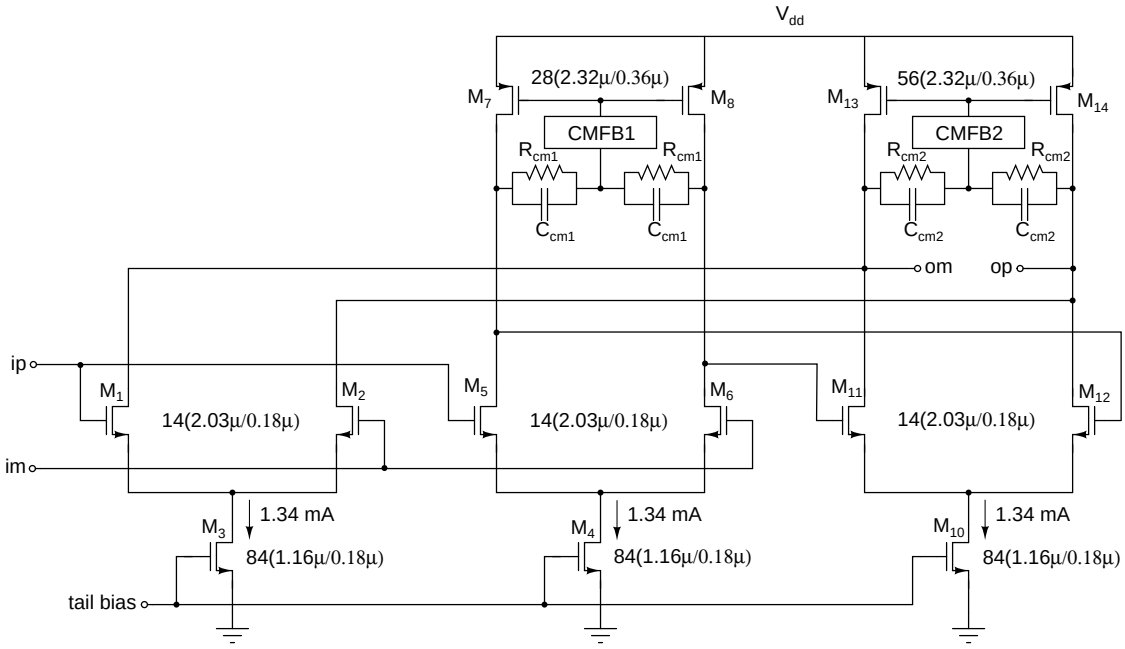


Figure 3.1: Two stage opamp with feedforward compensation

structed from two cascaded NMOS differential pairs with local common-mode feedback and feed forward compensation. The two differential pairs, shown to the right in figure 3.1, forms the main signal path. The differential pair on the left is used for frequency compensation, which forms high-frequency feed forward path. The feed forward path pulls the phase back to -90°, providing sufficient phase margin. Feed forward compensation increases the bandwidth of opamp there by making opamp a candidate to be used in high frequency filters.

3.1.1 NMOS-NMOS opamp

An NMOS input stage and NMOS output stage becomes more viable, as transistor threshold voltage V_T approaches $\frac{V_{dd}}{2}$ ([2], p.104) , than a PMOS-NMOS or an NMOS-PMOS opamp. The maximum signal swing of cascaded identical stages like this is $4V_T$ peak to peak differential. With V_{dd} much larger than V_T, this is sub-optimal. With $V_{dd} = 1.8\ V$ and $V_T = 0.5\ V$, the single ended signal swing achieved is almost equal to half rail-to-rail.

3.1.2 Compensation

A two stage opamp is generally used for opamp-RC filters, as single stage opamps do not provide sufficient gain with resistive loading. Feed forward compensation is preferred over to Miller compensation for the reasons given in ([2], p.105).

Miller compensation causes the two dominant poles to split apart, moving one dominate pole closer to origin. This causes the frequency response to start roll off at much lower frequencies with -20 dB/dec, making the opamp look like a single pole system, where as the feed forward compensation won't effect the two dominant pole locations and allows the frequency response to roll of at two pole rate (due to the main signal path) at low frequencies, and at one-pole rate (due to the feedforward path) at high frequencies. This is better shaping frequency response, and it avoids compensating capacitors.

3.1.3 Programmable opamp

The opamp shown in Fig:3.1, is not programmable. For scaling the frequency response of the filter, it is not just sufficient to switch the resistors. It results in drooping of the frequency response at lower bandwidths ([2], p.108). To overcome this issue, constan-C scaling is used, meaning opamp should also be programmed along with resistors.

For a given specification of the noise, constant-C scaling proves better choice

[3]. To scale down the bandwidth by a factor x, all conductances are scaled down the factor x, while maintaining all capacitances constant. There are obviously three conductances to be scaled: R_i, R_z and opamp transconductances. While this section describes the programability of opamp, sections 3.4 and 3.5 discuss the programability of integrating resistor R_i and compensating resistor R_z respectively.

Assuming the filter is optimized for highest bandwidth, the properties of constant-C scaling can be summarized as follows:

1. the output noise remains constant for all bandwidths.

2. capacitors remain constant.

3. bandwidth is scaled down by scaling down the transconductors and scaling up the resistors by the same factor.

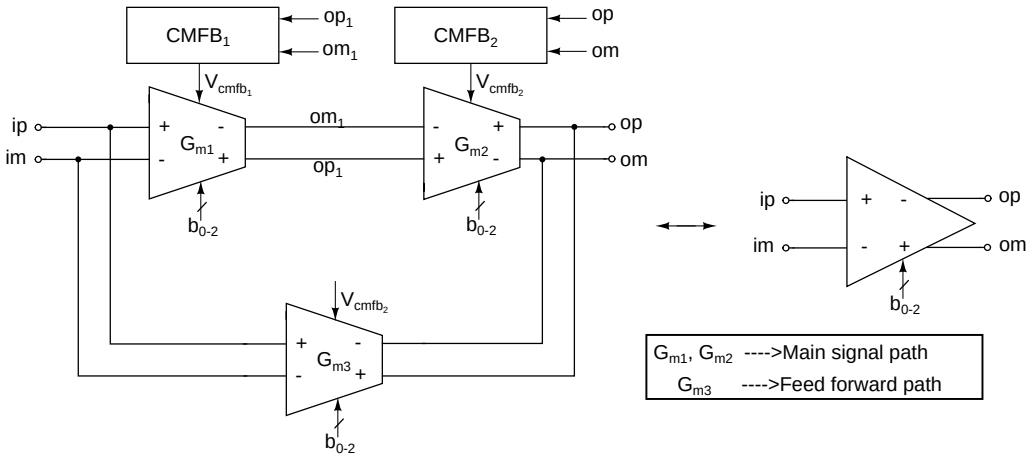


Figure 3.2: Programmable two stage opamp with feed forward compensation

Figure 3.2 shows the schematic of programmable opamp. Each transconductor is digitally programmed using a binary control word $b_2b_1b_0$. G_m is maximum for $b_2b_1b_0 = 111$ setting. For 001 setting, G_m is reduced by a factor of 7.

Programmable transconductor

Programmable transconductor, shown in figure 3.3, is made by connecting unit transconductors in a binary weighted manner[1]. The unit transconductor cell

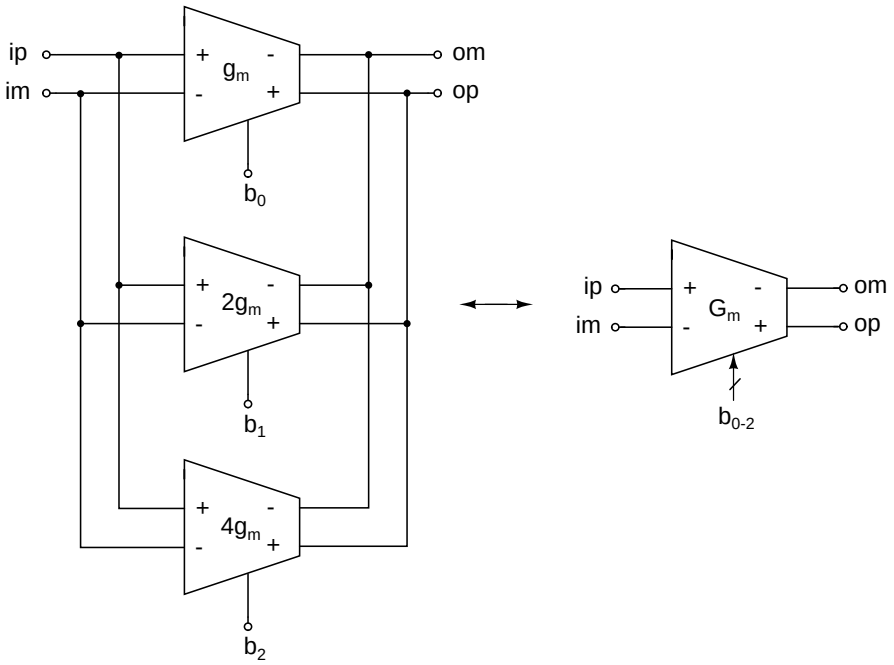


Figure 3.3: Programmable transconductor

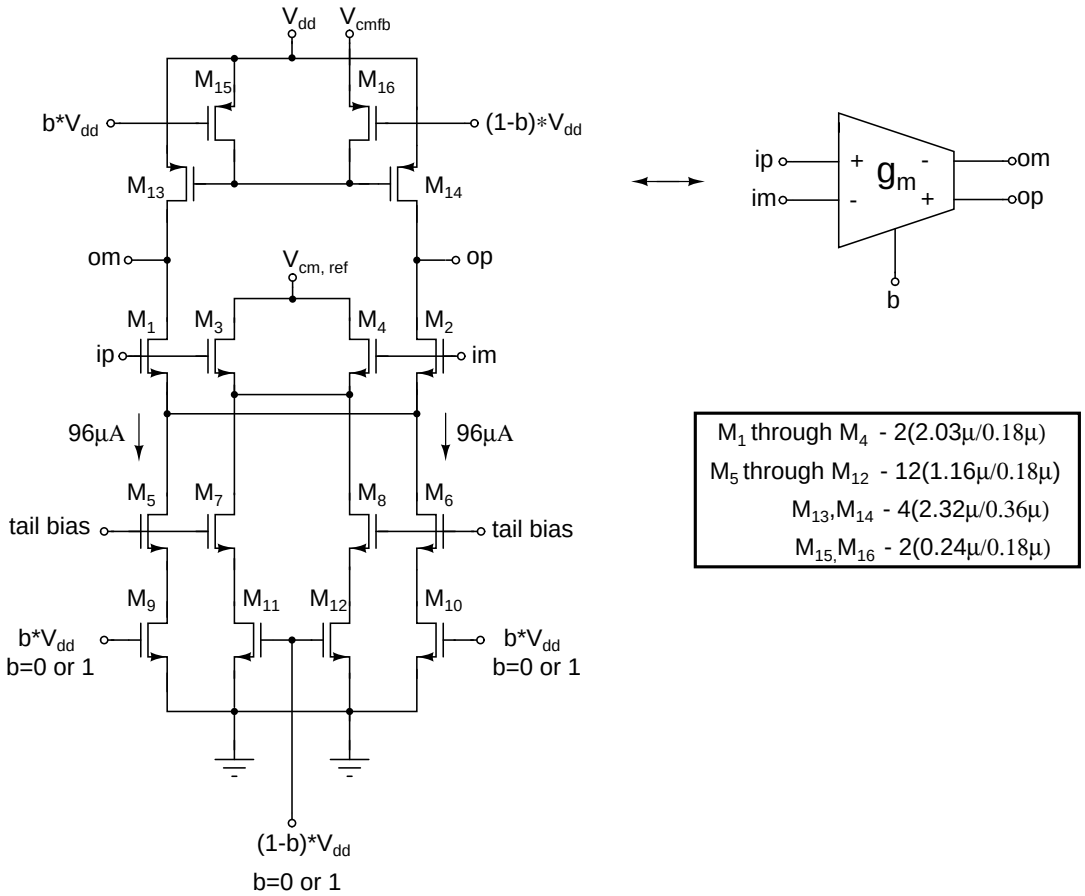


Figure 3.4: Constant-C unit Gm-cell.

is shown in figure 3.4. It is realized using a differential pair. M_1-M_2 form the main differential pair of the transconductor and M_3-M_4 form a dummy differential pair. M_5-M_6 and M_7-M_8 form the main and dummy current sources respectively. The unit transconductor is switched ON/OFF by switching the main current sources. This is accomplished by using transistors M_9-M_{10} operating in triode region, controlled by bit b . M_{11}-M_{12} also operate in triode region and turns dummy current sources ON and OFF. They are controlled by bit $\overline{b}$. Main current source and dummy current source are mutually exclusive. This ensures that either main differential pair or dummy differential pair is connected to the input, thus maintaining the input capacitance constant independent of b [1]. A fixed transconductance bias circuit (explained in section 3.2) is used to maintain the g_m of the transconductor intact over process and temperature.

$V_{cm,\,ref}$ is the DC voltage equal to output common-mode DC level of the transconductor. V_{cmfb} is the voltage derived from common-mode feedback circuit that maintains the common mode level of the outputs *op* and *om* equal to $V_{cm,\,ref}$. M_{15} and M_{16} are used as switches and turn the load current sources ON/OFF.

3.1.4 Common mode feedback circuit

Separate common mode feed back circuits are used for both the stages. Fixed transconductance bias circuit causes the tail current of differential pair to change with process and temperature, so as to keep the g_m constant. If simple resistor feedback is used, as in ([2], p.105), the common mode voltage varies with process and temperature. Separate common mode feed back circuits for the two stages is the fix for the above problem.

CMFB1

Figure 3.5 shows the common mode feed back circuit for first stage. R_{cm}, C_{cm} form the common mode detection circuit, the input of which comes from output of first stage. Resistor sensing is used to enhance linearity. Capacitors are introduced,

in parallel with common mode sensing resistors, to increase the stability of the common mode feed back circuit. The detected common mode is compared with a common mode reference. The error is amplified using NMOS error amplifier. M_7 is a low output impedance source follower that drives the compensating capacitor C_c. The PMOS loads M_3, M_4 are diode connected to increase the stability at the cost of slight offset in common mode voltage.

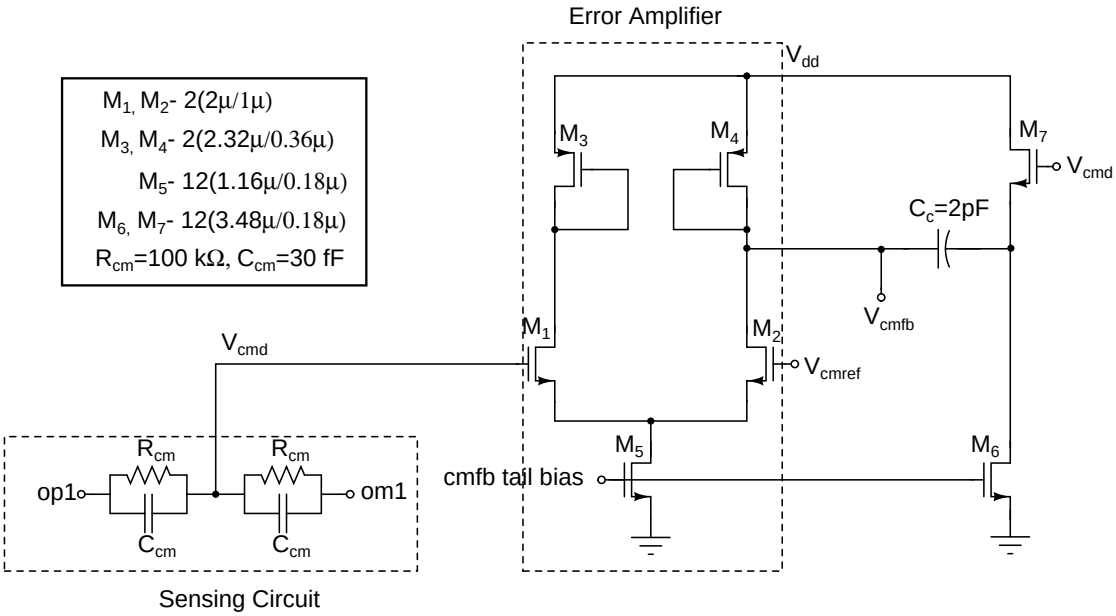


Figure 3.5: Common mode feed back of first stage.

CMFB2

Figure 3.6 shows the common mode feed back circuit for the second stage. The circuit operation is similar to that of first stage common mode feed back.

3.1.5 Frequency response of opamp

Figure 3.7 shows the frequency response of the opamp, for worst case load(second integrator's load) of $900fF$ in parallel with $\frac{R_i}{4} = \frac{1667}{4} = 416.75\Omega$. Performance parameters of the opamp are given below:

1. DC gain=32 dB

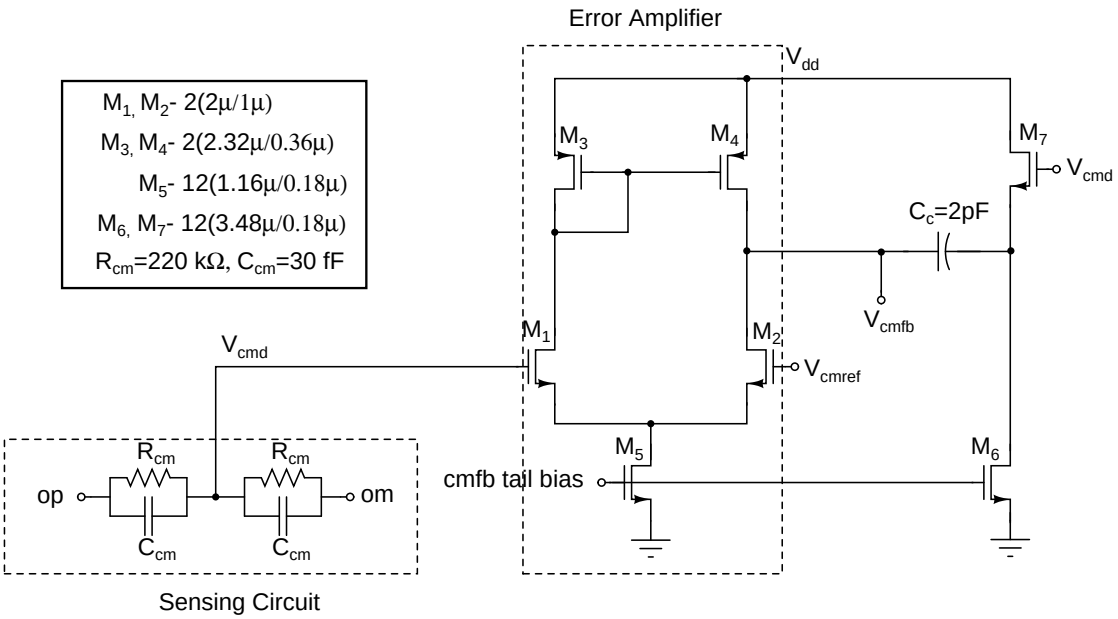


Figure 3.6: Common mode feed back of second stage.

2. Unity Gain Bandwidth=2.24 GHz

3. Phase Margin=41^o

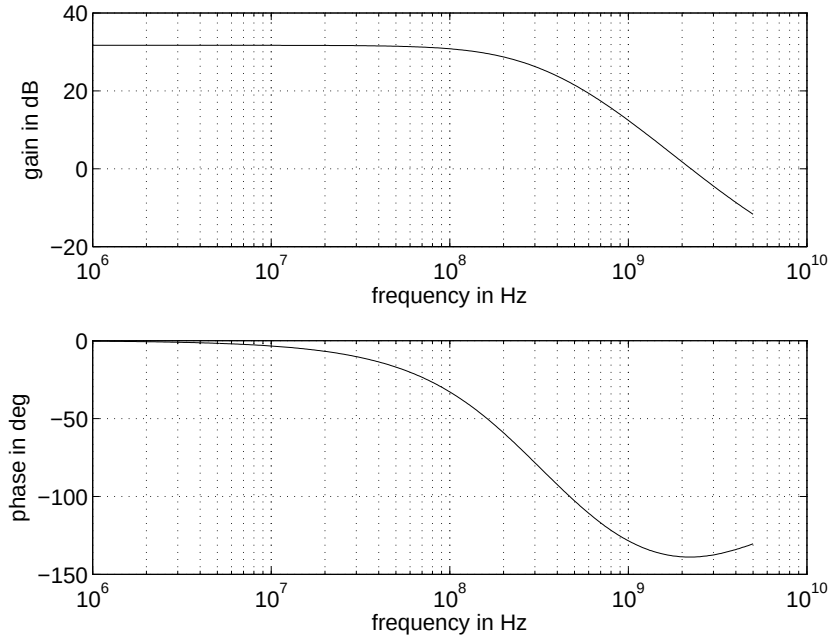


Figure 3.7: Opamp Bode plot for a load of $900fF$ in parallel with 416.75Ω

3.2 Fixed transconductance bias

Figure 3.8 shows the fixed Gm bias circuit employed in this design. This is a technology scaled version of the circuit used in [1]. For a detailed discussion on the evolution and operation of this circuit, the reader is referred to [5]. The salient features of this bias generator are the following:

- The generator does not rely on the MOSFET square law.
- The circuit is robust with power supply variations.
- The generated bias current is very tolerant of the large output conductances of short channel MOSFETs.

Referring to the figure 3.8, M_1 and M_2 are the devices whose transconductance is servoed to the stable off-chip conductance $\frac{1}{R}$. The current through $M_7,\ M_8$ and $M_{18},\ M_{19}$ is denoted as I_1. The voltage drop across the resistor, I_1R, is applied to the differential pair formed by $M_1\&M_2$, resulting in drain currents $I + \Delta i$ and $I - \Delta i$ respectively. M_5 and M_6 are sized appropriately to carry a current 2I. The currents flowing through $M_9\&M_{10}$ are seen to be $(I - \Delta i + I_1)$ and $(I - \Delta i)$ respectively. $M_{11},\ M_{12}$ must carry identical currents, so

$$I - \Delta i + I_1 = I + \Delta i \tag{3.1}$$

$$\Rightarrow I_1 = 2\Delta i \tag{3.2}$$

Clearly,

$$\Delta i = g_{m,M_1}\left(\frac{I_1 R}{2}\right) \tag{3.3}$$

$$\Rightarrow g_{m,M_1} = \frac{1}{R} \tag{3.4}$$

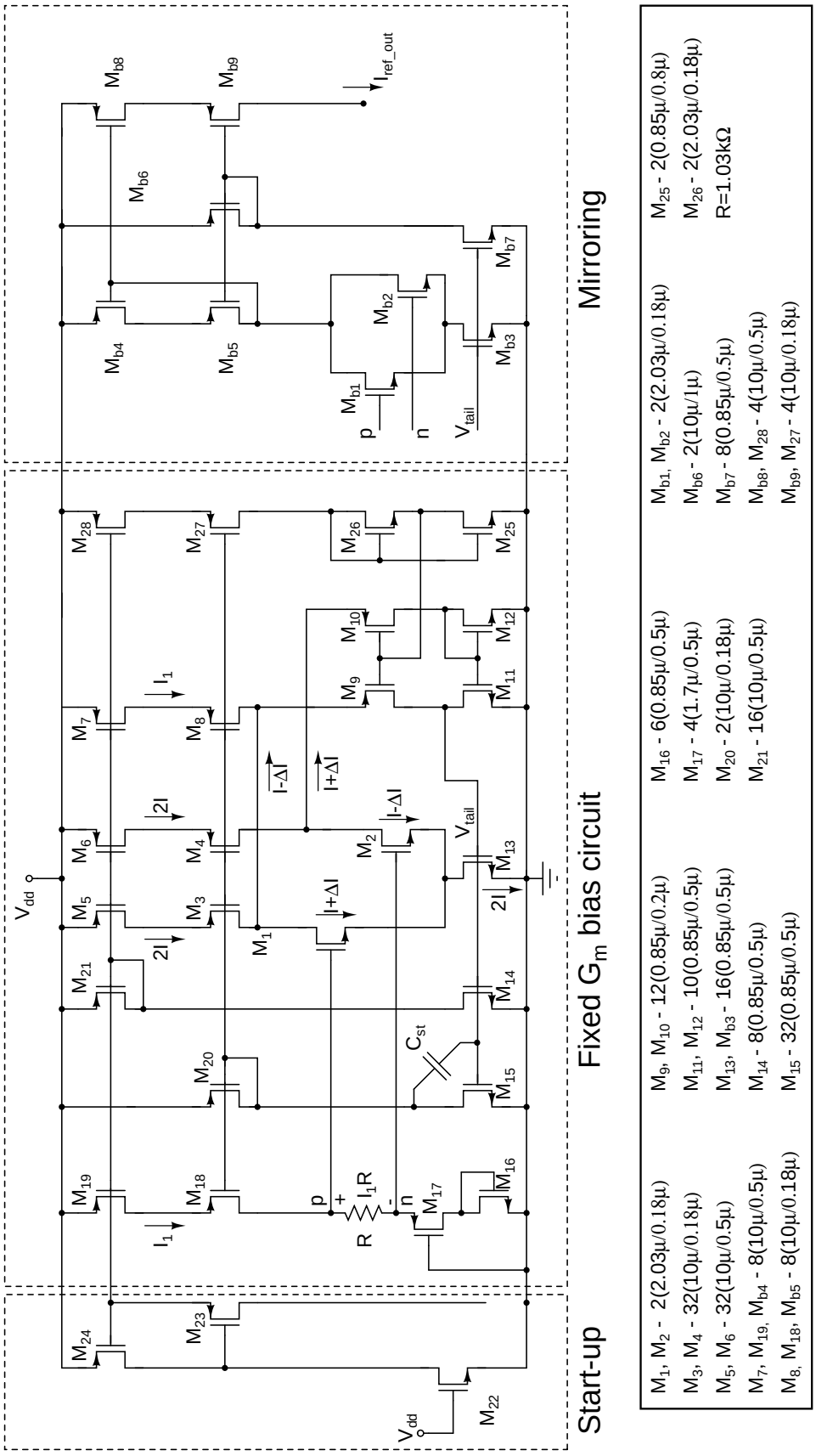


Figure 3.8: Fixed Gm bias generation.

3.3 Bias distribution

The current generated by fixed Gm bias has to be distributed to all transconductors as accurately as possible. The current distribution circuit proposed in [6], serves this purpose. The circuit is shown in figure 3.9. The main advantages of this bias distribution are

- Excellent precision in mirroring
- Easy to layout

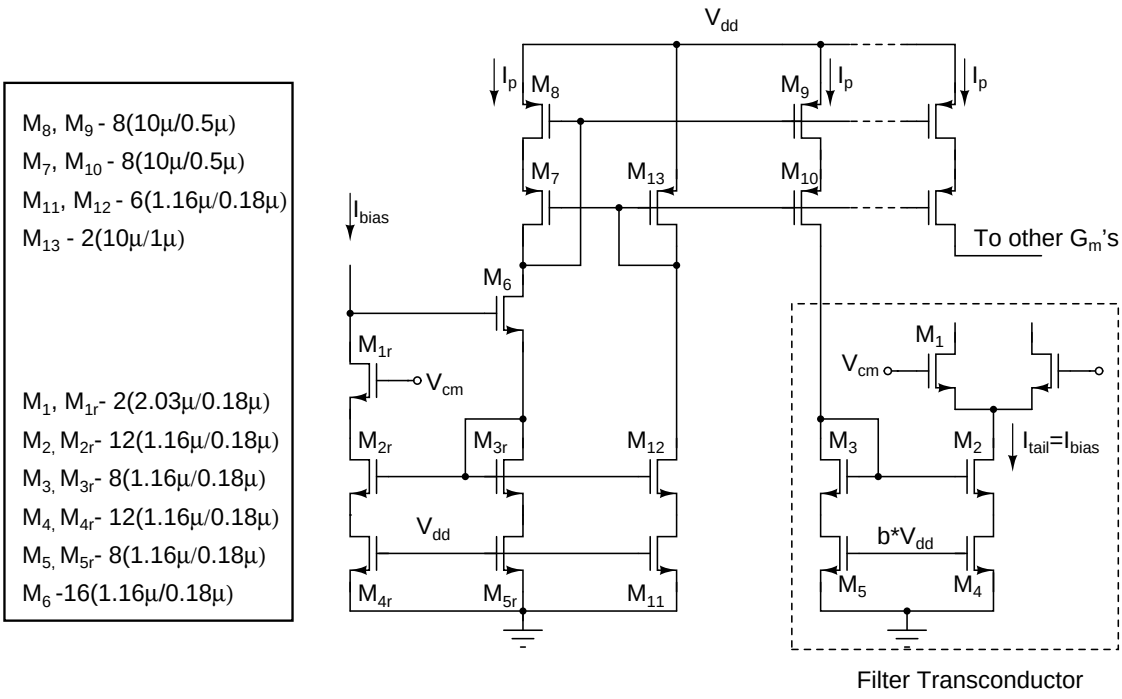


Figure 3.9: Bias distribution.

Bias current generated from fixed Gm bias, I_{bias}, is fed to the distribution circuit. Transistors $M_{1r}, M_{2r}, M_{3r}, M_{4r}$, and M_{5r} replicate the filter transconductor formed by M_1, M_2, M_3, M_4 and M_5 respectively. I_p is a predistorted version of I_{bias}. The ratio of I_p to I_{bias} is given as:

$$\frac{I_p}{I_{bias}} = \frac{2}{3} \times \frac{1 + \lambda V_{GS,M_{3r}}}{1 + \lambda V_{DS,M_{2r}}} \tag{3.5}$$

where λ is channel length modulation parameter. The predistorted current, I_p, is mirrored accurately using cascoded PMOS current mirror, and it's multiple copies

are distributed to all transconductors.

The ratio of transconductor tail current I_{tail} to I_p is given as:

$$\frac{I_{tail}}{I_p} = \frac{3}{2} \times \frac{1 + \lambda V_{DS,M_2}}{1 + \lambda V_{GS,M_3}} \tag{3.6}$$

$$\Rightarrow I_{tail} = I_p \times \frac{3}{2} \times \frac{1 + \lambda V_{DS,M_2}}{1 + \lambda V_{GS,M_3}} \tag{3.7}$$

Clearly, V_{DS,M_2} is equal to $V_{DS,M_{2r}}$ and V_{GS,M_3} is equal to $V_{DS,M_{3r}}$. Substituting I_p from equation 3.5 in equation 3.7, we get:

$$I_{tail} = \left(\frac{2}{3} \times \frac{1 + \lambda V_{GS,M_{3r}}}{1 + \lambda V_{DS,M_{2r}}} \times I_{bias}\right) \times \frac{3}{2} \times \frac{1 + \lambda V_{DS,M_2}}{1 + \lambda V_{GS,M_3}} \tag{3.8}$$

$$= I_{bias} \tag{3.9}$$

3.4 Programmable integrating resistor

Programmable integrating resistor is realized by a bank of three binary weighted resistors, as shown in figure 3.10. The resistance of the bank can be varied in binary steps, by programming the MOS switches in series with the resistors. Resistors are realized using high resistive poly silicon. MOS switches are connected at the input side(virtual ground) of the opamp while resistors at the output side of the opamp, so that the signal swing across MOSFET will be very small minimizing distortion. The gate voltage of switches is boosted up to $3.4V$, so that the linearity of MOS switch is improved. The series combination of switch and resistor adds up to a total resistance of $1.667k\Omega$, for full bandwidth($b_0 = 1,\ b_1 = 1,\ b_2 = 1$).

The resistance of poly silicon varies with temperature and process corners and for the MOSFET, the variation is much more severe. There should be a mechanism of maintaining the total resistance constant and equal to $1.667k\Omega$, across operating temperatures and all process corners. This is achieved by adjusting the gate voltage, V_c, of the the MOS switch, such that the total resistance remains constant. The series resistance of the MOS switch and the resistor is servoed to a stable offchip resistance. V_c is generated from control voltage generator, discussed in

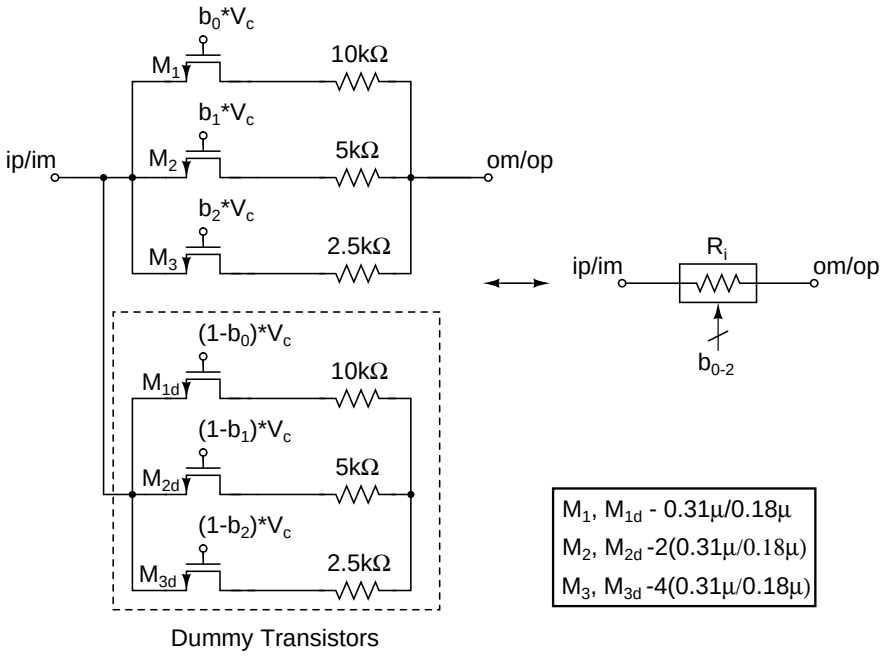


Figure 3.10: Programmable integrating resistor.

section 3.6.

Dummy transistors are used to maintain capacitance constant when transistors are being switched ON/OFF. M_{1d}, M_{2d} and M_{3d} are the dummies corresponding to M_1, M_2 and M_3 respectively. When a transistor is turned OFF, it's corresponding dummy is turned ON. To maintain constant capacitance on both sides of MOSFET, dummy transistors should be used at the internal node(between MOS switch and resistor) also. But the capacitance at the internal node should be very small, ideally zero. Let us say $b_2 = 1,\ b_1 = 1,\ b_0 = 0$, switch M_1 is open and $10k\Omega$ resistor should be hanging at the output of the opamp. But the series combination internal node capacitance and $10k\Omega$ resistor will load the opamp at high frequencies. This results in drooping of magnitude response of the filter, as we scale down the bandwidth. Hence, the internal node capacitance is maintained as small as possible. That is why, dummy transistors are not connected at the internal node.

3.5 Programmable compensating resistor

Compensating resistor R_z is realized using a bank of three binary weighted MOS transistors. M_1 forms LSB, and M_3 forms MSB. Programability is achieved by turning them ON/OFF. The resistance of MOS transistors is servoed to a stable offchip resistance. Dummy transistors are used to maintain constant-C scaling. The gate control voltage V_{cz} is generated from Control voltage generator, discussed in section 3.6.

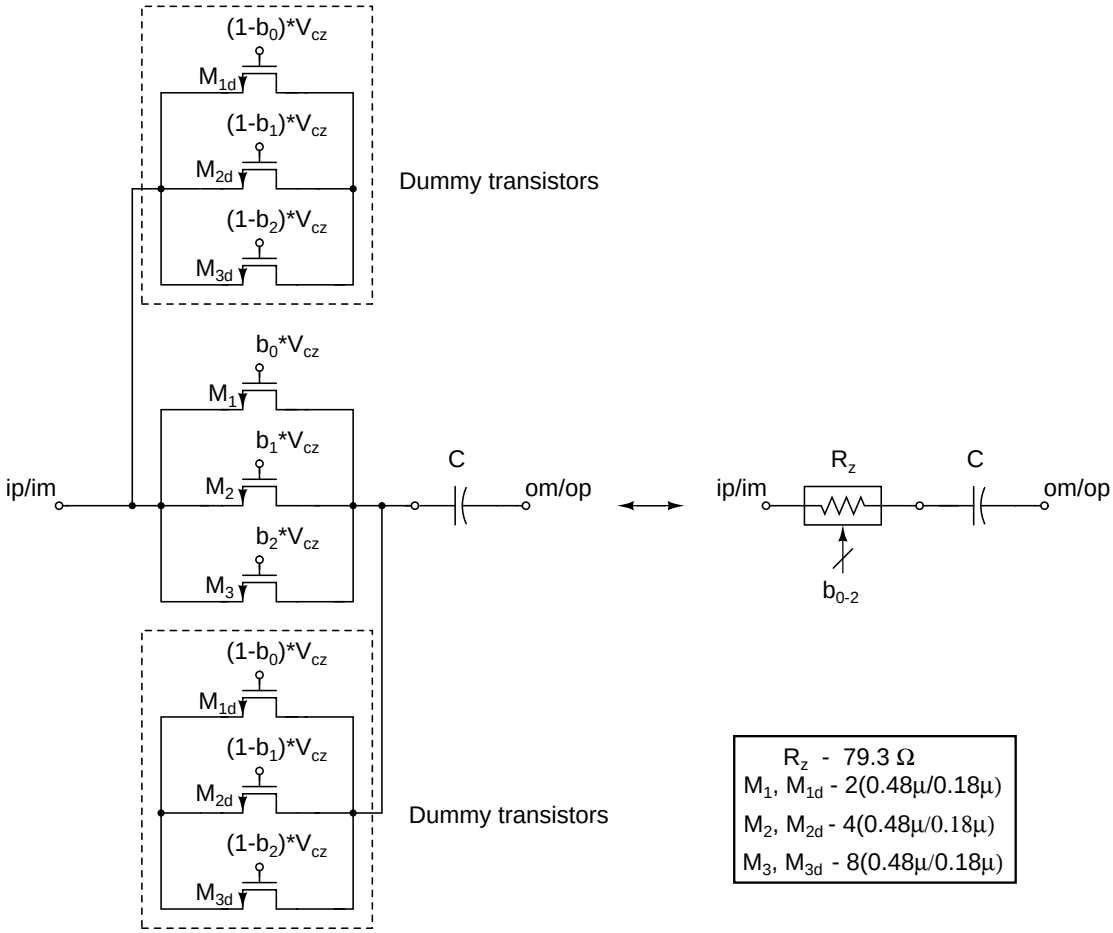
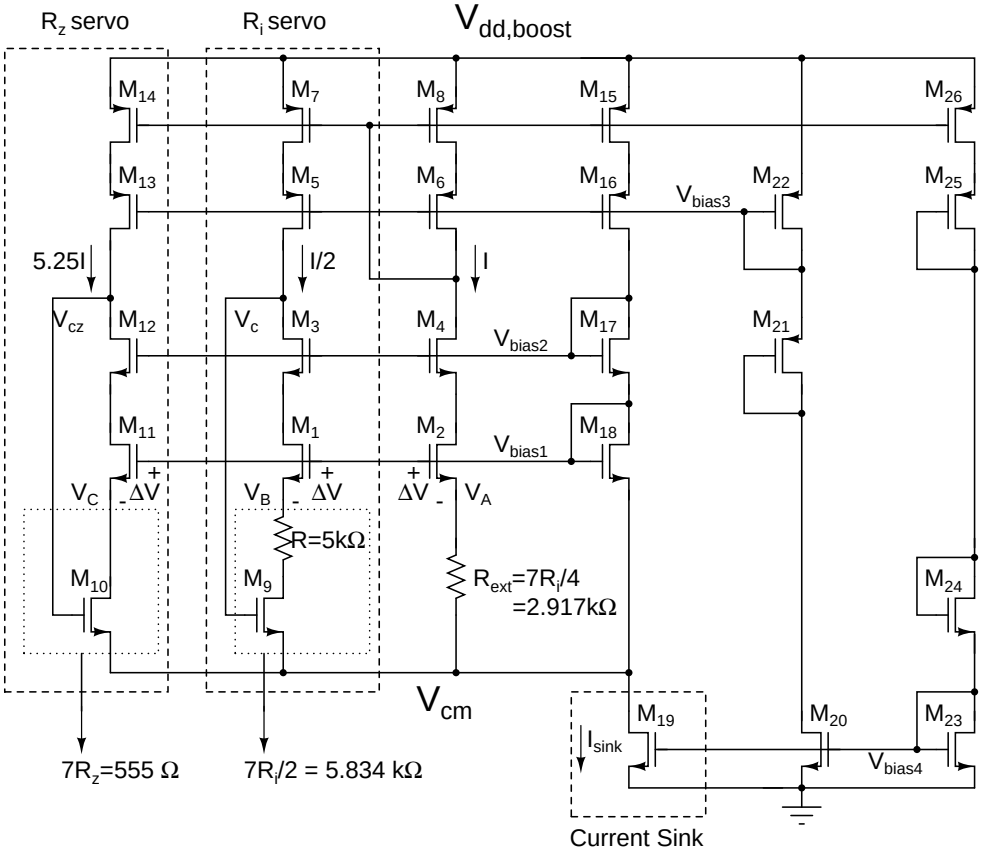


Figure 3.11: Programmable compensating resistor.

3.6 Control voltage generator

Figure 3.12 shows the schematic diagram of the control voltage generator. The voltage across the circuit is $V_{dd,boost} - V_{cm}$. The current flowing into V_{cm}, will increase the V_{cm} level, as V_{cm} is generated by passing current though a diode connected device. Care has to be taken to divert the current to ground through a current sink, so that V_{cm} remains unaltered. There are two servoing circuits shown in dotted lines, R_i servo and R_z servo.



3.3V devices:		
M_1, M_3 - 4(2µ/1µ)	M_{13}, M_{14} - 42(4µ/1µ)	M_{20} - 10(2µ/0.35µ)
M_2, M_4 - 8(2µ/1µ)	M_{15}, M_{16}, M_{21} - 2(4µ/1µ)	M_{23} - 2(2µ/0.35µ)
M_5, M_7 - 4(4µ/1µ)	M_{17}, M_{22}, M_{24} - 2(2µ/1µ)	M_{25}, M_{26} - 2(4µ/1µ)
M_6, M_8 - 8(4µ/1µ)	M_{18} - 2(2µ/1.3µ)	
M_{11}, M_{12} - 42(2µ/1µ)	M_{19} - 48(2µ/0.35µ)	

1.8V devices:
M_9 - 2(0.31µ/0.18µ)
M_{10} - 2(0.48µ/0.18µ)

Figure 3.12: Control voltage generator for MOS resistors.

R_i servo

$M_9 - R$ combination is formed by two LSB's of R_i in parallel and hence its resistance should be equal to $7R_i/2$.

V_{bias1} is chosen such that the voltage across R_{ext} is very small, a few mV. The current densities of M_1 and M_2 are made equal, so that $V_{GS,M1} = V_{GS,M2} = \Delta V$. So the voltage across $M_9 - R$ combination is same as that across R_{ext}. But the current forced through $M_9 - R$ combination is half of the current through R_{ext}. The negative feedback adjusts the gate voltage of M_9, V_c, such that a current of $I/2$ flows thorough M_9. Clearly, now total resistance of $M_9 - R$ combination is $2R_{ext} = 7R_i/2 = 5.834\ k\Omega$.

The PMOS current mirrors are cascoded for achieving high precision in mirroring. Similarly the cascoded devices M_3 and M_4 increase the impedance looking into the drains of M_3 and M_4 so that a higher voltage difference is tolerated between drains of M_3 and M_4. The difference is attenuated by a factor of $(g_m r_o)_{M3|M4} \times (g_m r_o)_{M1|M2}$, when looking from sources of M_1 and M_2, so that the voltages V_A and V_B are almost equal.

R_z servo

M_{10} is formed by one LSB of R_z and hence its resistance should be equal to $7R_z = 555\ \Omega$.

The servoing operation is similar to R_i servo. From the schematic, it is clear that $V_C = V_A$. The current forced though M_{10} is $5.25I$. Negative feedback adjusts the gate voltage of M_{10}, V_{cz}, such that a current of $5.25I$ flows through M_{10}. Clearly, now the on-state resistance of M_{10} is $R_{ext}/5.25 = 2.917\ k\Omega/5.25 = 555.6\ \Omega$.

3.7 Layout

Designed filter is laid out using CADENCE and the top level layout of the filter is shown in figure 3.13.

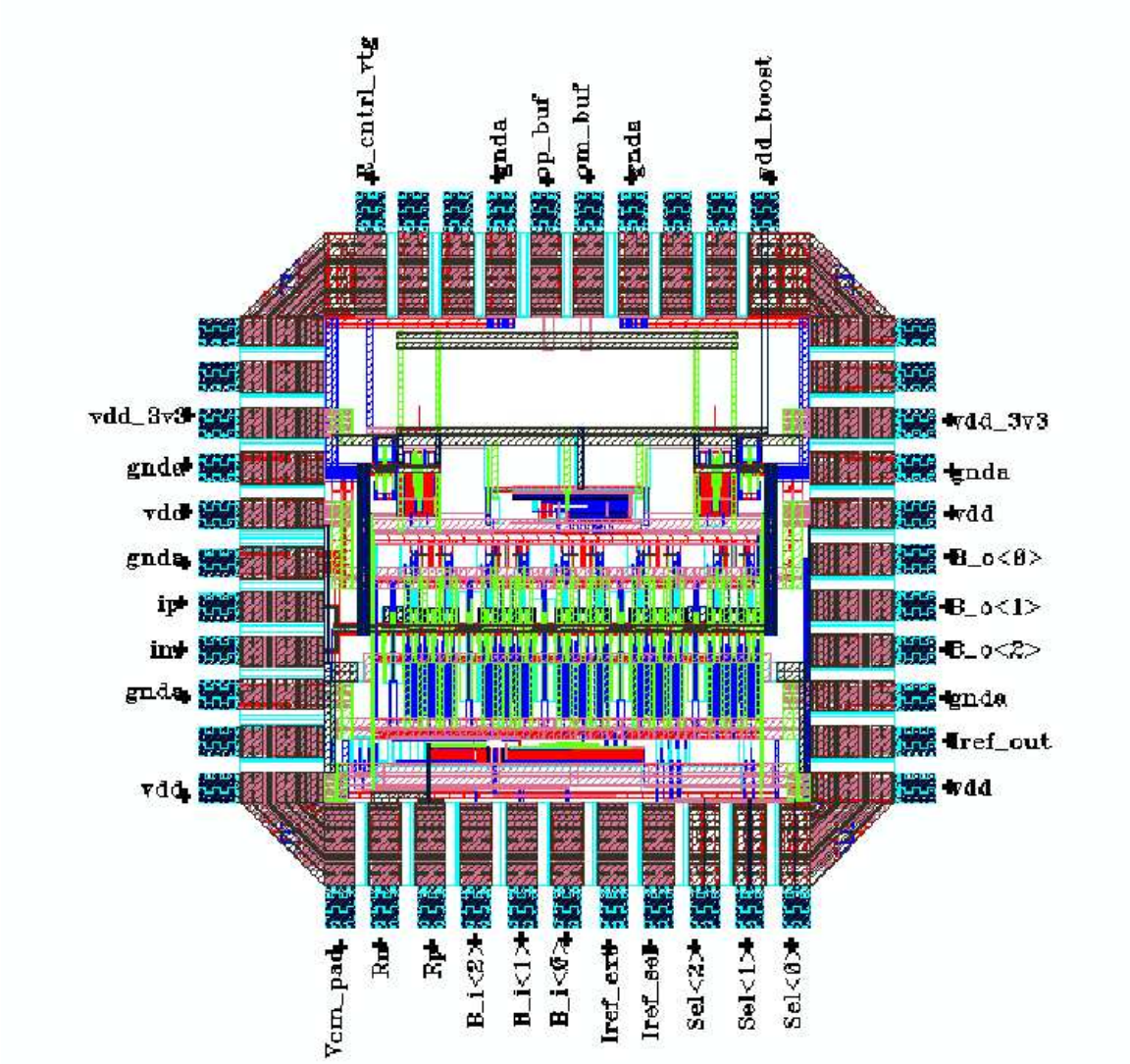


Figure 3.13: Complete layout of the filter.

CHAPTER 4

STATE SPACE MODEL OF THE FILTER

The main aim of developing state space model of the filter is to fit the frequency response of the filter to the ideal frequency response.

All MOS transistors are modeled using complete Quasi Static model. Chapter 7&9 of [4] gives clear explanation of Quasi-static model. Section 4.1 gives brief introduction to state space model. State space matrices A,B,C and D are derived for the filter in Section 4.2. Finally, section 4.3 presents the optimization routine.

4.0.1 Small signal model of transconductor using QS model

Figure 4.1 shows the small signal model of a simple transconductor, using QS model. All the internal parasitics are shown in figure. For taking dummy transis-

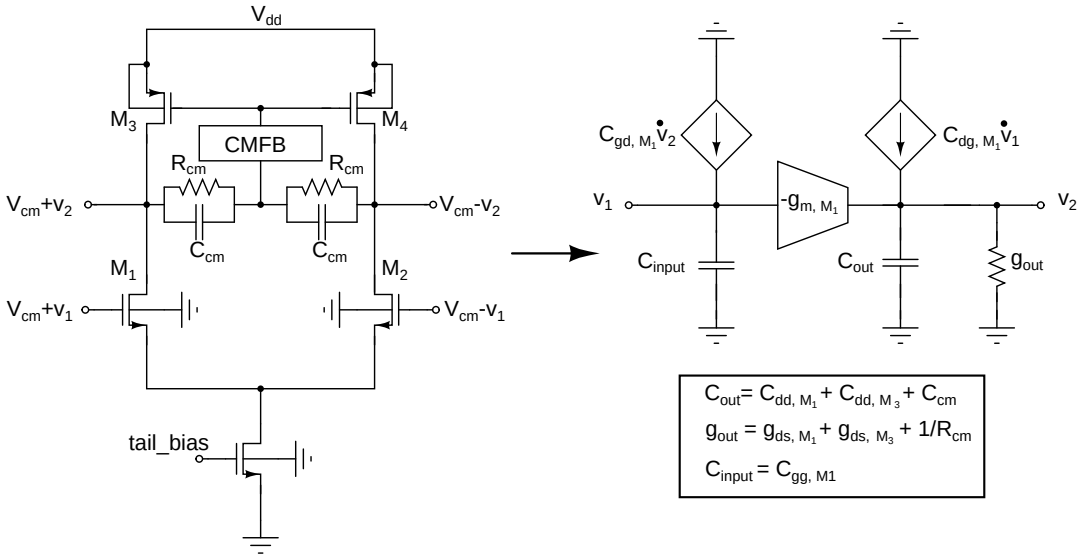


Figure 4.1: Small signal model of transconductor

tors into account we have to add C_{gg} of dummy transistor to the input capacitance C_{input}.

4.1 Introduction to state space model

A brief introduction about state space modeling is given here. More information on state space modeling can be found in [7].

A state space representation is a mathematical model of a physical system as a set of input, output and state variables related by first-order differential equations. To abstract from the number of inputs, outputs and states, the variables are expressed as vectors and the differential and algebraic equations are written in matrix form. The state space representation (also known as the "time-domain approach") provides a convenient and compact way to model and analyze systems with multiple inputs and outputs. With p inputs and q outputs, we would otherwise have to write down $q \times p$ Laplace transforms to encode all the information about a system.

4.1.1 State variables

The internal state variables are the smallest possible subset of system variables that can represent the entire state of the system at any given time. State variables must be linearly independent; a state variable cannot be a linear combination of other state variables. The minimum number of state variables required to represent a given system, n, is usually equal to the order of the system's defining differential equation. If the system is represented in transfer function form, the minimum number of state variables is equal to the power of denominator of transfer function after it has been reduced to a proper fraction.

4.1.2 LTI systems

The most general state space representation of an LTI system with p inputs, q outputs and n state variables is written in the following form:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{4.1}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{4.2}$$

$\dim[\mathbf{A}(\cdot)] = n \times n, \dim[\mathbf{B}(\cdot)] = n \times p, \dim[\mathbf{C}(\cdot)] = q \times n, \dim[\mathbf{D}(\cdot)] = q \times p,$
$\dot{\mathbf{x}}(t) := \frac{d\mathbf{x}(t)}{dt}$.

$\mathbf{x}(\cdot)$ is called the "state vector", $\mathbf{y}(\cdot)$ is called the "output vector", $\mathbf{u}(\cdot)$ is called the "input (or control) vector", $\mathbf{A}(\cdot)$ is the "state matrix", $\mathbf{B}(\cdot)$ is the "input matrix", $\mathbf{C}(\cdot)$ is the "output matrix", and $\mathbf{D}(\cdot)$ is the "feedthrough (or feedforward) matrix".

If the circuit nodes are coupled capacitively, deriving the state space model given by equations 4.1 and 4.2, becomes a bit cubersome. In such a case the Descriptor state equations can be used as given below:

$$\mathbf{H}\dot{\mathbf{x}}(t) = \mathbf{A_d}\mathbf{x}(t) + \mathbf{B_d}\mathbf{u}(t) \tag{4.3}$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \tag{4.4}$$

where, $\mathbf{A} = \mathbf{H^{-1}A_d}$ and $\mathbf{B} = \mathbf{H^{-1}B_d}$.

4.2 State space model of the filter

The complete schematic of the filter with 20 state variables is shown in figure 4.2. All the state variables(v_1 to v_{20}) are shown in the figure. The internals (small signal model) of the opamp are shown in figure 4.3.

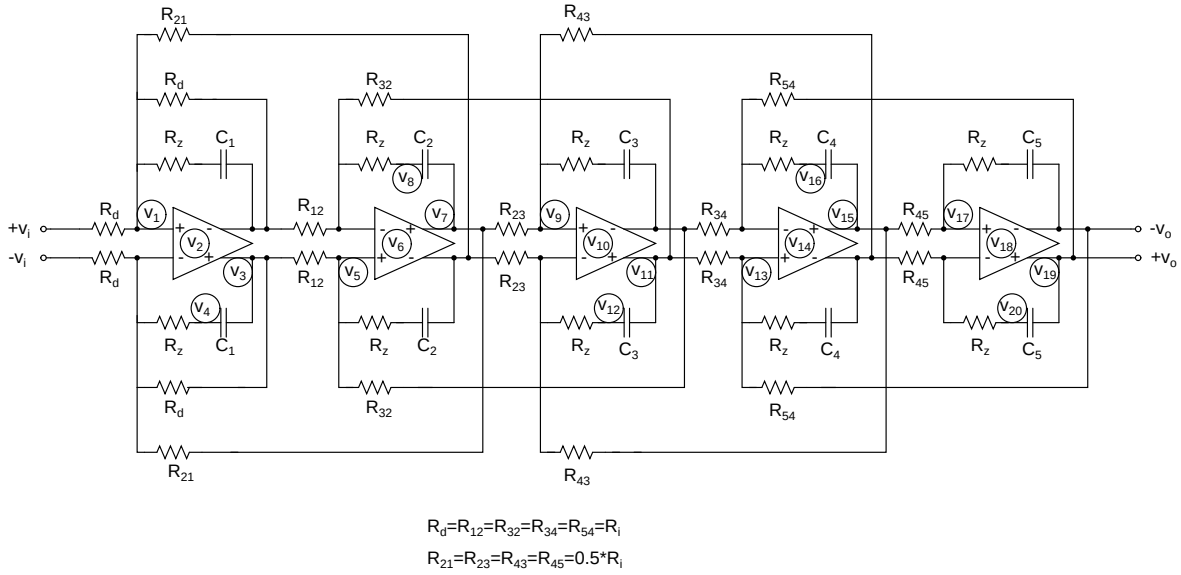


Figure 4.2: Complete schematic of the filter with state variables

4.2.1 A,B,C & D matrices of the filter

The state space equations of the filter, given by equations 4.3 and 4.4, can be expanded in to the following form. The **D** matrix is a null matrix as there is no feed forward path from input to output.

$$\begin{bmatrix} \mathbf{H_{11}} & \mathbf{H_{12}} & \mathbf{H_{13}} & \mathbf{H_{14}} & \mathbf{H_{15}} \\ \mathbf{H_{21}} & \mathbf{H_{22}} & \mathbf{H_{23}} & \mathbf{H_{24}} & \mathbf{H_{25}} \\ \mathbf{H_{31}} & \mathbf{H_{32}} & \mathbf{H_{33}} & \mathbf{H_{34}} & \mathbf{H_{35}} \\ \mathbf{H_{41}} & \mathbf{H_{42}} & \mathbf{H_{43}} & \mathbf{H_{44}} & \mathbf{H_{45}} \\ \mathbf{H_{51}} & \mathbf{H_{52}} & \mathbf{H_{53}} & \mathbf{H_{54}} & \mathbf{H_{55}} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \\ \dot{\mathbf{x}}_3 \\ \dot{\mathbf{x}}_4 \\ \dot{\mathbf{x}}_5 \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d_{11}}} & \mathbf{A_{d_{12}}} & \mathbf{A_{d_{13}}} & \mathbf{A_{d_{14}}} & \mathbf{A_{d_{15}}} \\ \mathbf{A_{d_{21}}} & \mathbf{A_{d_{22}}} & \mathbf{A_{d_{23}}} & \mathbf{A_{d_{24}}} & \mathbf{A_{d_{25}}} \\ \mathbf{A_{d_{31}}} & \mathbf{A_{d_{32}}} & \mathbf{A_{d_{33}}} & \mathbf{A_{d_{34}}} & \mathbf{A_{d_{35}}} \\ \mathbf{A_{d_{41}}} & \mathbf{A_{d_{42}}} & \mathbf{A_{d_{43}}} & \mathbf{A_{d_{44}}} & \mathbf{A_{d_{45}}} \\ \mathbf{A_{d_{51}}} & \mathbf{A_{d_{52}}} & \mathbf{A_{d_{53}}} & \mathbf{A_{d_{54}}} & \mathbf{A_{d_{55}}} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d_1}} \\ \mathbf{B_{d_2}} \\ \mathbf{B_{d_3}} \\ \mathbf{B_{d_4}} \\ \mathbf{B_{d_5}} \end{bmatrix} \mathbf{u} \quad (4.5)$$

$$\mathbf{y} = \begin{bmatrix} \mathbf{C_1} & \mathbf{C_2} & \mathbf{C_3} & \mathbf{C_4} & \mathbf{C_5} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \end{bmatrix} \quad (4.6)$$

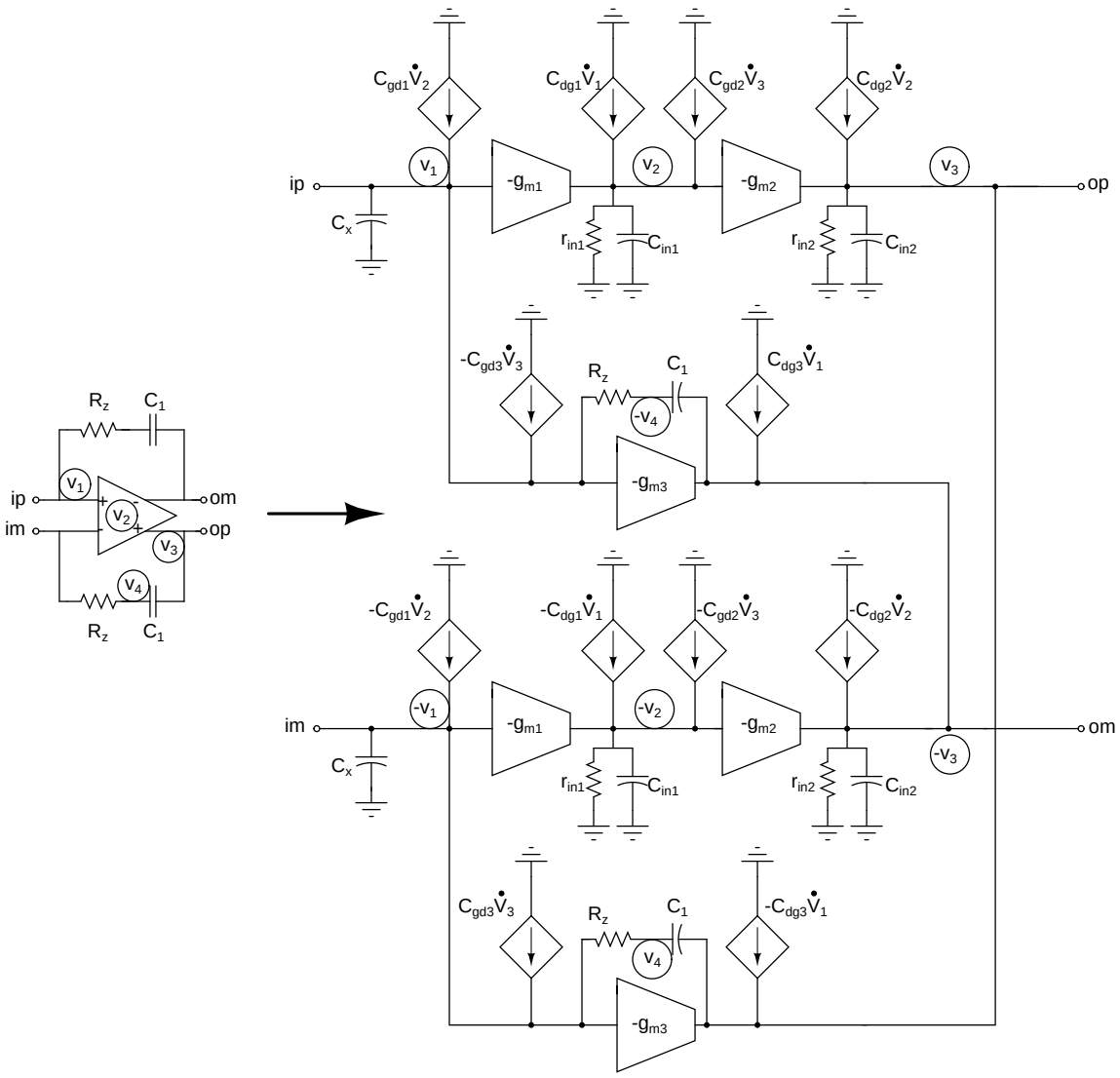


Figure 4.3: Opamp with integrating capacitor C1 & Compensating resistor R_z

where,

$$\mathbf{x_1} = \begin{bmatrix} v_1 & v_2 & v_3 & v_4 \end{bmatrix}^T \tag{4.7}$$

$$\mathbf{x_2} = \begin{bmatrix} v_5 & v_6 & v_7 & v_8 \end{bmatrix}^T \tag{4.8}$$

$$\mathbf{x_3} = \begin{bmatrix} v_9 & v_{10} & v_{11} & v_{12} \end{bmatrix}^T \tag{4.9}$$

$$\mathbf{x_4} = \begin{bmatrix} v_{13} & v_{14} & v_{15} & v_{16} \end{bmatrix}^T \tag{4.10}$$

$$\mathbf{x_5} = \begin{bmatrix} v_{17} & v_{18} & v_{19} & v_{20} \end{bmatrix}^T \tag{4.11}$$

$$\mathbf{u} = \begin{bmatrix} v_{ip} \end{bmatrix} \tag{4.12}$$

$$\mathbf{y} = \begin{bmatrix} v_{19} \end{bmatrix} \tag{4.13}$$

The dimensions of the sub matrices are given below:
$\dim[\mathbf{H_{ij}}(\cdot)] = 4 \times 4,\ \dim[\mathbf{A_{d_{ij}}}(\cdot)] = 4 \times 4,\ \dim[\mathbf{B_{d_i}}(\cdot)] = 4 \times 1,\ \dim[\mathbf{C_i}(\cdot)] = 1 \times 4.$

The output node is v_{19}. Hence,

$$\mathbf{C_i} = [\mathrm{O}]_{4\times 1},\ \ \mathbf{i} = 1, 2, 3, 4 \tag{4.14}$$

$$\mathbf{C_5} = \begin{pmatrix} 0 & 0 & 1 & 0 \end{pmatrix} \tag{4.15}$$

The descriptor state equations can be viewed as follows:

- $\mathbf{H}$: Shows the capacitive(or inductive) coupling among the state variables.
- $\mathbf{A_d}$: Shows the resistive coupling among the state variables.
- $\mathbf{B_d}$: Shows the resistive coupling of the state variables with the input.

Most of the submatrices, given in equation 4.5, are null matrices.

- $\mathbf{H_{ij}} = [\mathbf{O}]_{4\times 4}, i \neq j$, if there is no capacitive coupling between states $\mathbf{x_i}$ and $\mathbf{x_j}$.
- $\mathbf{A_{d_{ij}}} = [\mathbf{O}]_{4\times 4}, i \neq j$, if there is no resistive coupling between states $\mathbf{x_i}$ and $\mathbf{x_j}$.
- $\mathbf{B_{d_i}} = [\mathbf{O}]_{4\times 1}$, if there is no resistive coupling between states $\mathbf{x_i}$ and input.

The state space equations are written for first integrator and then they are extended for the whole filter to get complete state space model. The first row of

matrix equation 4.5 shows how the set of nodes, represented by $\mathbf{x_1}$, are coupled to other nodes.

4.2.2 State space equations for first integrator

The first integrator is coupled to input and second integrator through resistors, and is isolated from all the rest. Hence, the first row of 4.5 can be simplified as:

$$\mathbf{H_{11}}\dot{\mathbf{x}}_\mathbf{1} = \mathbf{A_{d_{11}}}\mathbf{x_1} + \mathbf{A_{d_{12}}}\mathbf{x_2} + \mathbf{B_{d_1}}v_i \tag{4.16}$$

While writing state space equations the following convention is maintained.

The net capacitive current flowing out of a node = The net resistive current coming into the node.

Following this convention, the state space matrices of first integrator are obtained and they are given below:

$$\mathbf{H_{11}} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_1 & C_x & -C_{gd1} & C_{gd3} & 0 \\ v_2 & -C_{dg1} & C_{in1} & -C_{gd2} & 0 \\ v_3 & C_{dg3} & -C_{dg2} & C_{in2}+C_1 & -C_1 \\ v_4 & 0 & 0 & -C_1 & C_1 \end{array}\right) \tag{4.17}$$

$$\mathbf{A_{d_{11}}} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_1 & -\frac{1}{R_{21}}-\frac{2}{R_d}-\frac{1}{R_z} & 0 & -\frac{1}{R_d} & -\frac{1}{R_z} \\ v_2 & -g_{m1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_3 & g_{m3}-\frac{1}{R_d} & -g_{m2} & -\frac{1}{r_{in2}}-\frac{1}{R_d}-\frac{1}{R_{12}} & 0 \\ v_4 & -\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \end{array}\right) \tag{4.18}$$

$$\mathbf{A_{d_{12}}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_1 & 0 & 0 & -\frac{1}{R_{21}} & 0 \\ v_2 & 0 & 0 & 0 & 0 \\ v_3 & \frac{1}{R_{12}} & 0 & 0 & 0 \\ v_4 & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.19}$$

$$\mathbf{B_{d_1}} = \left(\begin{array}{c|c} & v_i \\ \hline v_1 & \frac{1}{R_d} \\ v_2 & 0 \\ v_3 & 0 \\ v_4 & 0 \end{array}\right) \tag{4.20}$$

Only the first integrator is connected to the input. For all other integrators, there is no direct coupling from input. Hence,

$$\mathbf{B_{d_i}} = [\mathbf{O}]_{4\times 1},\ i = 2, 3, 4, 5. \tag{4.21}$$

4.2.3 State space equations for second integrator

The second integrator is coupled to first and third integrators and is isolated from others. Hence, the second row of 4.5 can be simplified as:

$$\mathbf{H_{22}}\dot{\mathbf{x}}_\mathbf{2} = \mathbf{A_{d_{21}}}\mathbf{x_1} + \mathbf{A_{d_{22}}}\mathbf{x_2} + \mathbf{A_{d_{23}}}\mathbf{x_3} \tag{4.22}$$

$\mathbf{H_{22}}$ can be obtained from $\mathbf{H_{11}}$, by replacing C_1, in matrix equation 4.17, with C_2.

$$\mathbf{H_{22}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_5 & C_x & -C_{gd1} & C_{gd3} & 0 \\ v_6 & -C_{dg1} & C_{in1} & -C_{gd2} & 0 \\ v_7 & C_{dg3} & -C_{dg2} & C_{in2} + C_2 & -C_2 \\ v_8 & 0 & 0 & -C_2 & C_2 \end{array}\right) \tag{4.23}$$

It can be noted that $\mathbf{A_{d_{21}}}$ is the transpose of $\mathbf{A_{d_{12}}}$, because the coupling

between $\mathbf{x_1}$ and $\mathbf{x_2}$ is bilateral.

$$\mathbf{A_{d_{21}}} = \left(\begin{array}{c|cccc} & v_1 & v_2 & v_3 & v_4 \\ \hline v_5 & 0 & 0 & \frac{1}{R_{12}} & 0 \\ v_6 & 0 & 0 & 0 & 0 \\ v_7 & -\frac{1}{R_{21}} & 0 & 0 & 0 \\ v_8 & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.24}$$

The submatrix $\mathbf{A_{d_{22}}}$ is similar to $\mathbf{A_{d_{11}}}$, except for the fact that there is no local feed back(R_d) for second integrator.

$$\mathbf{A_{d_{22}}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_5 & -\frac{1}{R_{12}} - \frac{1}{R_{32}} - \frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \\ v_6 & -g_{m1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_7 & g_{m3} & -g_{m2} & -\frac{1}{r_{in2}} - \frac{1}{R_{21}} - \frac{1}{R_{23}} & 0 \\ v_8 & -\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \end{array}\right) \tag{4.25}$$

The submatrix $\mathbf{A_{d_{23}}}$ is similar to $\mathbf{A_{d_{12}}}$, and it can be obtained by replacing R_{12} and R_{21} in equation 4.19, with R_{23} and R_{32} respectively.

$$\mathbf{A_{d_{23}}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_5 & 0 & 0 & -\frac{1}{R_{32}} & 0 \\ v_6 & 0 & 0 & 0 & 0 \\ v_7 & \frac{1}{R_{23}} & 0 & 0 & 0 \\ v_8 & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.26}$$

In a similar fashion, the ABCD matrices can be obtained for all other integrators also.

4.2.4 State space equations for third integrator

Third integrator is coupled to second and fourth integrators only. Hence, the third row of matrix equation 4.5 can be simplified as:

$$\mathbf{H_{33}\dot{x}_3} = \mathbf{A_{d_{32}}x_2} + \mathbf{A_{d_{33}}x_3} + \mathbf{A_{d_{34}}x_4} \tag{4.27}$$

where,

$$\mathbf{H_{33}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_9 & C_x & -C_{gd1} & C_{gd3} & 0 \\ v_{10} & -C_{dg1} & C_{in1} & -C_{gd2} & 0 \\ v_{11} & C_{dg3} & -C_{dg2} & C_{in2}+C_3 & -C_3 \\ v_{12} & 0 & 0 & -C_3 & C_3 \end{array}\right) \tag{4.28}$$

$$\mathbf{A_{d_{32}}} = \left(\begin{array}{c|cccc} & v_5 & v_6 & v_7 & v_8 \\ \hline v_9 & 0 & 0 & \frac{1}{R_{23}} & 0 \\ v_{10} & 0 & 0 & 0 & 0 \\ v_{11} & -\frac{1}{R_{32}} & 0 & 0 & 0 \\ v_{12} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.29}$$

$$\mathbf{A_{d_{33}}} = \left(\begin{array}{c|ccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_9 & -\frac{1}{R_{23}}-\frac{1}{R_{43}}-\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \\ v_{10} & -g_{m1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_{11} & g_{m3} & -g_{m2} & -\frac{1}{r_{in2}}-\frac{1}{R_{32}}-\frac{1}{R_{34}} & 0 \\ v_{12} & -\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \end{array}\right) \tag{4.30}$$

$$\mathbf{A_{d_{34}}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_9 & 0 & 0 & -\frac{1}{R_{43}} & 0 \\ v_{10} & 0 & 0 & 0 & 0 \\ v_{11} & \frac{1}{R_{34}} & 0 & 0 & 0 \\ v_{12} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.31}$$

4.2.5 State space equations for fourth integrator

Fourth integrator is coupled to third and fifth integrators only. Hence, the fourth row of matrix equation 4.5 can be simplified as:

$$\mathbf{H_{44}\dot{x}_4} = \mathbf{A_{d_{43}}x_3} + \mathbf{A_{d_{44}}x_4} + \mathbf{A_{d_{45}}x_5} \tag{4.32}$$

where,

$$\mathbf{H_{44}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{13} & C_x & -C_{gd1} & C_{gd3} & 0 \\ v_{14} & -C_{dg1} & C_{in1} & -C_{gd2} & 0 \\ v_{15} & C_{dg3} & -C_{dg2} & C_{in2}+C_4 & -C_4 \\ v_{16} & 0 & 0 & -C_4 & C_4 \end{array}\right) \tag{4.33}$$

$$\mathbf{A_{d_{43}}} = \left(\begin{array}{c|cccc} & v_9 & v_{10} & v_{11} & v_{12} \\ \hline v_{13} & 0 & 0 & \frac{1}{R_{34}} & 0 \\ v_{14} & 0 & 0 & 0 & 0 \\ v_{15} & -\frac{1}{R_{43}} & 0 & 0 & 0 \\ v_{16} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.34}$$

$$\mathbf{A_{d_{44}}} = \left(\begin{array}{c|ccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{13} & -\frac{1}{R_{34}}-\frac{1}{R_{54}}-\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \\ v_{14} & -g_{m1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_{15} & g_{m3} & -g_{m2} & -\frac{1}{r_{in2}}-\frac{1}{R_{43}}-\frac{1}{R_{45}} & 0 \\ v_{16} & -\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \end{array}\right) \tag{4.35}$$

$$\mathbf{A_{d_{45}}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{13} & 0 & 0 & -\frac{1}{R_{54}} & 0 \\ v_{14} & 0 & 0 & 0 & 0 \\ v_{15} & \frac{1}{R_{45}} & 0 & 0 & 0 \\ v_{16} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.36}$$

4.2.6 State space equations for fifth integrator

Fifth integrator is coupled to fourth integrator only. Hence, the last row of matrix equation 4.5 can be simplified as:

$$\mathbf{H_{55}}\dot{\mathbf{x}}_\mathbf{5} = \mathbf{A_{d_{54}}}\mathbf{x_4} + \mathbf{A_{d_{55}}}\mathbf{x_5} \tag{4.37}$$

where,

$$\mathbf{H_{55}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{17} & C_x & -C_{gd1} & C_{gd3} & 0 \\ v_{18} & -C_{dg1} & C_{in1} & -C_{gd2} & 0 \\ v_{19} & C_{dg3} & -C_{dg2} & C_{in2}+C_5 & -C_5 \\ v_{20} & 0 & 0 & -C_5 & C_5 \end{array}\right) \tag{4.38}$$

$$\mathbf{A_{d_{54}}} = \left(\begin{array}{c|cccc} & v_{13} & v_{14} & v_{15} & v_{16} \\ \hline v_{17} & 0 & 0 & \frac{1}{R_{45}} & 0 \\ v_{18} & 0 & 0 & 0 & 0 \\ v_{19} & -\frac{1}{R_{54}} & 0 & 0 & 0 \\ v_{20} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.39}$$

$$\mathbf{A_{d_{55}}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{17} & -\frac{1}{R_{45}}-\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \\ v_{18} & -g_{m1} & -\frac{1}{r_{in1}} & 0 & 0 \\ v_{19} & g_{m3} & -g_{m2} & -\frac{1}{r_{in2}}-\frac{1}{R_{54}} & 0 \\ v_{20} & -\frac{1}{R_z} & 0 & 0 & -\frac{1}{R_z} \end{array}\right) \tag{4.40}$$

$$\mathbf{A_{d_{45}}} = \left(\begin{array}{c|cccc} & v_{17} & v_{18} & v_{19} & v_{20} \\ \hline v_{17} & 0 & 0 & -\frac{1}{R_{54}} & 0 \\ v_{17} & 0 & 0 & 0 & 0 \\ v_{17} & \frac{1}{R_{45}} & 0 & 0 & 0 \\ v_{17} & 0 & 0 & 0 & 0 \end{array}\right) \tag{4.41}$$

The final descriptor state space equations for the filter are given below:

$$\begin{bmatrix} \mathbf{H_{11}} & \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{O} \\ \mathbf{O} & \mathbf{H_{22}} & \mathbf{O} & \mathbf{O} & \mathbf{O} \\ \mathbf{O} & \mathbf{O} & \mathbf{H_{33}} & \mathbf{O} & \mathbf{O} \\ \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{H_{44}} & \mathbf{O} \\ \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{H_{55}} \end{bmatrix} \begin{bmatrix} \dot{\mathbf{x}}_1 \\ \dot{\mathbf{x}}_2 \\ \dot{\mathbf{x}}_3 \\ \dot{\mathbf{x}}_4 \\ \dot{\mathbf{x}}_5 \end{bmatrix} = \begin{bmatrix} \mathbf{A_{d_{11}}} & \mathbf{A_{d_{12}}} & \mathbf{O} & \mathbf{O} & \mathbf{O} \\ \mathbf{A_{d_{21}}} & \mathbf{A_{d_{22}}} & \mathbf{A_{d_{23}}} & \mathbf{O} & \mathbf{O} \\ \mathbf{O} & \mathbf{A_{d_{32}}} & \mathbf{A_{d_{33}}} & \mathbf{A_{d_{34}}} & \mathbf{O} \\ \mathbf{O} & \mathbf{O} & \mathbf{A_{d_{43}}} & \mathbf{A_{d_{44}}} & \mathbf{A_{d_{45}}} \\ \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{A_{d_{54}}} & \mathbf{A_{d_{55}}} \end{bmatrix} \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \mathbf{x}_3 \\ \mathbf{x}_4 \\ \mathbf{x}_5 \end{bmatrix} + \begin{bmatrix} \mathbf{B_{d_1}} \\ \mathbf{O} \\ \mathbf{O} \\ \mathbf{O} \\ \mathbf{O} \end{bmatrix} \mathbf{u} \quad (4.42)$$

$$\mathbf{y} = \begin{bmatrix} \mathbf{O} & \mathbf{O} & \mathbf{O} & \mathbf{O} & \begin{pmatrix} 0 & 0 & 1 & 0 \end{pmatrix} \end{bmatrix} \begin{bmatrix} \mathbf{x_1} \\ \mathbf{x_2} \\ \mathbf{x_3} \\ \mathbf{x_4} \\ \mathbf{x_5} \end{bmatrix} \quad (4.43)$$

The model can be easily extended when integrating resistors and compensating resistors are replaced with architectures given in sections 3.4 and 3.5. The small signal model of A MOS resistor is shown in figure 4.4. Frequency Response of the filter can be obtained from A,B,C and D matrices, using matlab built in routines *ss2tf* and *freqs*.

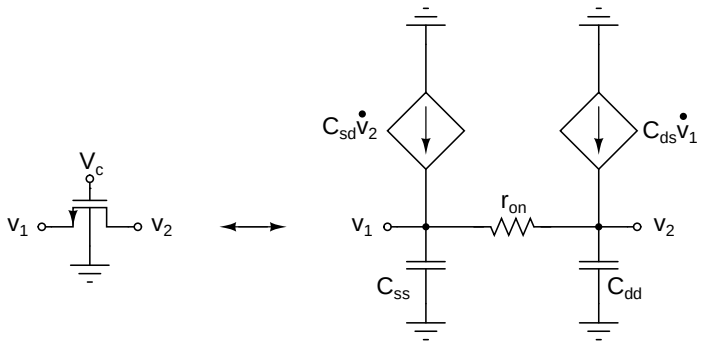


Figure 4.4: Small signal model of MOS resistor

4.3 Optimization

This section discusses the optimization routine required for fitting the frequency response of the filter obtained from state space model, to the ideal filter response.

The finite DC gain of opamp causes peak in the magnitude response([2], p.100),

at cutoff frequency. The peak can be reduced by adjusting the integrating capacitors and compensating resistor, R_z, appropriately. Indeed the filter transfer function, obtained from state space model, is a function of every capacitor and resistor used in the model. MATLAB built in optimization routine, *fminsearch*, is used to minimize the error between real and ideal frequency responses.

Optimization is done in two steps:

- Schematic level optimization
- Layout level optimization

4.3.1 Schematic level optimization

The following steps are followed during schematic level optimization.

1. For a given biasing conditions, DC analysis is done on the schematic to obtain operating points of opamp, R_i and R_z.

2. Optimization Vector=[C_1, C_2, C_3, C_4, C_5, R_z]. The initial vector of integrating capacitors is taken from figure 2.9. R_z is chosen to be $\frac{1}{g_{m3}}$, where g_{m3} is transconductance of the feed forward stage.

3. Optimization routine is run to fit the response given by state space model to the ideal response. Ideal response can be directly obtained from MATLAB built in routine *cheby* or it can be obtained from a state space model for figure 2.7 with ideal opamps.

4. *Fminsearch* is used to optimize the error between ideal and actual frequency responses. The error function is made a function of the variables to be tweaked. *Fminsearch* gives the tweaked values of C_1, C_2, C_3, C_4, C_5 and R_z, for minimum possible error.

5. The optimized values of integrating capacitors and R_z are put back into schematic, to get the optimized frequency response. Layout of the filter is drawn using these optimized capacitors and R_z.

4.3.2 Layout level optimization

Layout parasitics results in peaking at cutoff frequency. Integrating capacitors and R_z should be again tweaked to fit it back to ideal response. But now the layout parasitics have to be taken into account in the state space model. We use MATLAB built in routine *fminsearch* again to fit the frequency response of state space model to that obtained from simulator for the extracted layout, by tweaking parasitic capacitances. The procedure is given below:

1. AC simulation is run, with extracted layout, to obtain the frequency response.

2. Optimization vector=Parastic capacitors of opamp, R_i and R_z. Integrating capacitors, R_i and R_z should be same as those used in layout and they are fixed. The only things to be tweaked are parasitic capacitances.

3. Optimization routine is run to fit the response given by state space model to the frequency response given by simulator. *fminsearch* gives the tweaked values of parasictic capacitances, for minimum possible error. These tweaked values are put back into state space model, so that the model gives same response as the simulator.

4. Optimization routine given in 4.3.1 is used to get the new values of integrating capacitors and R_z, which fits the frequency response of the state space model to ideal response. Accordingly layout is corrected.

The final optimized values of integrating capacitors and R_z, used in layout, are given below.

$$C_1 = 401.85fF \tag{4.44}$$

$$C_2 = 898.74fF \tag{4.45}$$

$$C_3 = 692.29fF \tag{4.46}$$

$$C_4 = 873.18fF \tag{4.47}$$

$$C_5 = 410.97fF \tag{4.48}$$

$$R_z = 79.3\Omega \tag{4.49}$$

CHAPTER 5

SIMULATION RESULTS & CONCLUSION

5.1 Frequency response of the filter

Figures 5.1 shows the normalized frequency response of the filter for various bandwidth selections.

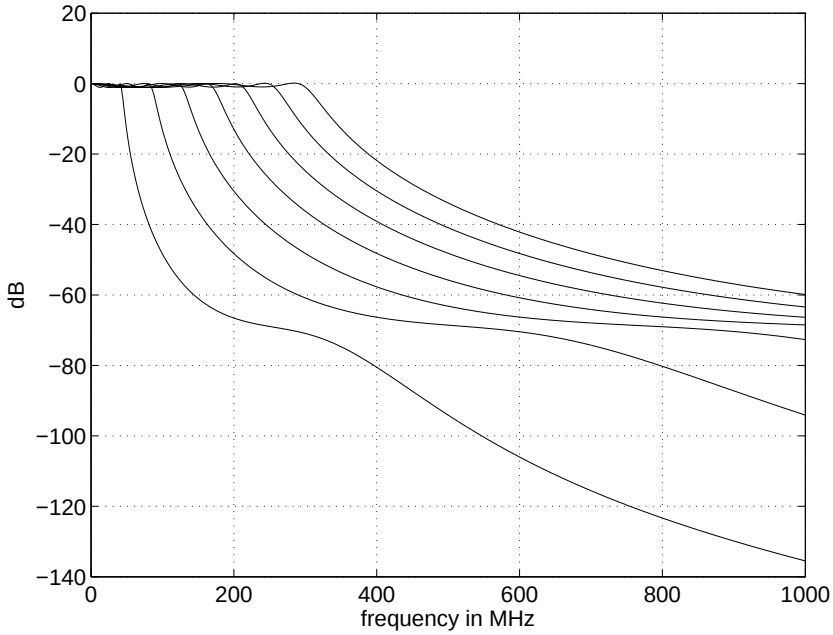


Figure 5.1: Normalized frequency response of the filter.

The passband response of the filter is shown in figure 5.2. The two imperfections of peaking at high cutoff frequency and passband droop, mentioned in ([2], p.106), are reduced to as minimum as possible.

1. The peak in the frequency response at high cutoff frequencies is 110 mdB.

2. The passband droop is 350 mdB from full band to the lowset bandwidth.

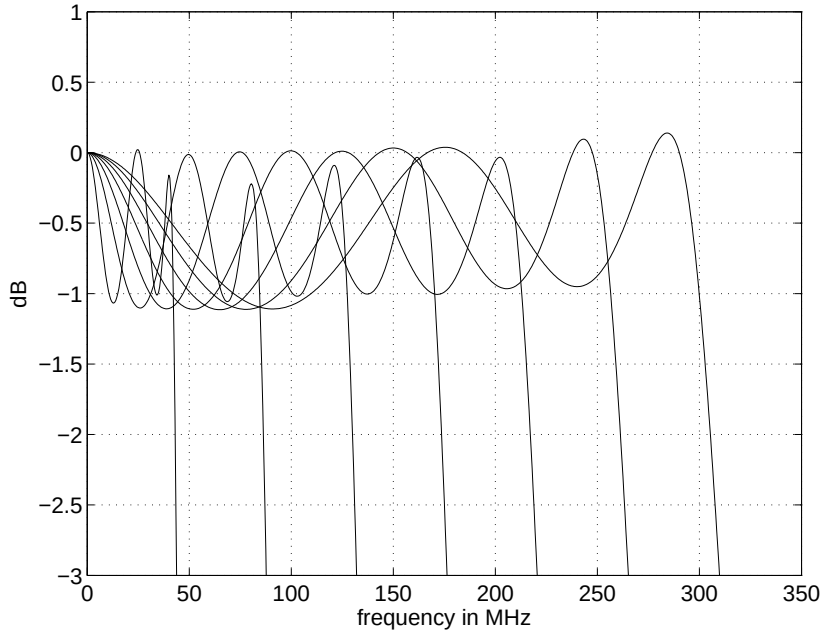


Figure 5.2: Normalized frequency response in passband.

5.2 Equivalent output noise

Figure 5.3 shows the equivalent output noise for all the seven bandwidths. The total integrated noise remains same for all the bandwidths, a property of constant-C scaling. The total integrated noise at the output is 793.54 μV(r.m.s).

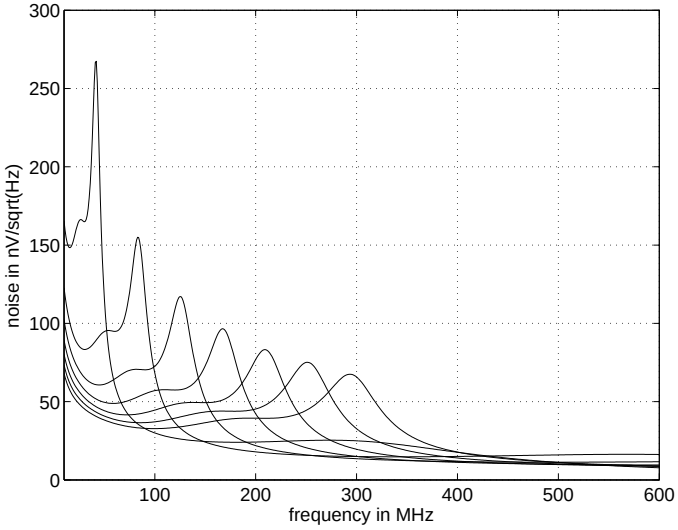


Figure 5.3: Equivalent noise at the output of the filter.

5.3 Performance

The maximum signal swing is 2.2 Vp-p for -40 dB third harmonic distortion, for lowest bandwidth selection. The input tone is chosen to be 14MHz, so that third harmonic lies at the cutoff frequency. Table 5.1 compares the performance of the filter with other works.

Table 5.1: Comparison with other works

Specification	This Work	Harrison[2]	S.Pavan & Nidhi [1]
Type of the filter	Chebyshev lowpass	Elliptic low pass	Chebyshev lowpass
Topology	opamp-RC	opamp-RC	Gm-C
Technology	0.18 μm	0.18 μm	0.35 μm
DC gain	-1.26 dB for full BW -1.38 dB for lowest BW	0 dB	-0.71 dB
Order	5	5	5
Power	20 mA @ 1.8 V	20 mA @ 1.8V	30 mA @ 3.3 V
Tuning Range	43-300 MHz	50-350 MHz	70-500 MHz
Input signal swing for -40dB THD	2.2 Vp-p	0.5 Vp-p	0.5 Vp-p
Integrated Noise at output	793.4 μV r.m.s	448 μV r.m.s	366 μV r.m.s
Dynamic Range	57.4 dB	52 dB	52 dB

5.4 Conclusion

Design of widely programable 43-300 MHz opamp-RC filter is presented. Fixed Gm bias is used for opamps, making sure that the variation in Gm of transconductor is less than 0.5% with process and temperature variations. The MOS resistors are servoed to stable external offchip resistance, making sure the variations less than 1% across process and temperature variations. Opamps are made programmable for precise scaling of bandwidth. Constant-C scaling technique is extended to opamp-RC filters achieving better bandwidth scaling.

State space model is used to model the filter. The response of the filter is fitted to ideal by tweaking integrating capacitors and compensating resistor. MATLAB optimization routine is used for this purpose. Thanks to MATLAB built in routine $fminsearch$, State space modeling and Quasi static model of MOSFET, which made the job easier.

CHAPTER 6

MODELING NON-QUASI-STATIC EFFECTS OF MOSFET

6.1 Introduction

The quasi-static model of a MOSFET is valid only for low frequencies. As the frequency of operation approaches the transition frequency, f_T of the device, the QS model becomes invalid. The measured filter response deviates considerably from that simulated using Quasi-static models, at RF frequencies. This chapter is an effort to extend the validity of Quasi-static models for RF circuit simulations. A segmentation model is developed using BSIM3v3 quasi static model.

In reality, the channel of a MOSFET can be modelled as a bias dependent RC distributed transmission line. But in the quasi static approach, the gate capacitance is lumped to the external source and drain nodes as shown in Figure 6.1, there by ignoring the finite time required for channel charge build-up. The one way to extend the validity of quasi-static models in that case is to consider the device as a connection of several shorter devices[8] and to model each section quasi-statically. Figure 6.2 shows a MOSFET broken down into 3 equal channel

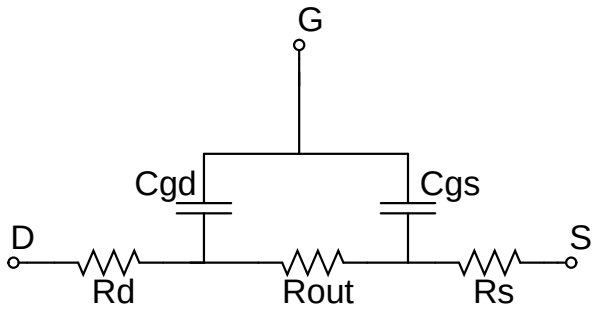


Figure 6.1: Quasi-static model of a MOSFET

segments in series. Additional short channel effects, resulting from segmentation,

are suppressed by adjusting the model parameters in the BSIM3v3 model file. The gate overlap capacitances are made zero in the middle segment(M_m), gate to drain overlap capacitance, C_{gdo} is made zero in the bottom segment(M_b) at the source and gate to source overlap capacitance,C_{gso} is made zero in the top segment(M_t) at the drain. The junction capacitances are made zero in all the three segments. Another transistor(M_s), biased in cutoff region, is placed in parallel to account for the junction capacitances. Thus, the bias dependence of junction capacitances will be taken care. The drain/source parasitic resistance, R_{ds} is distributed among all the three segments. The sheet resistances of drain and source diffusion of M_m are made zero. They are also made zero for source of M_t and the drain of M_b.

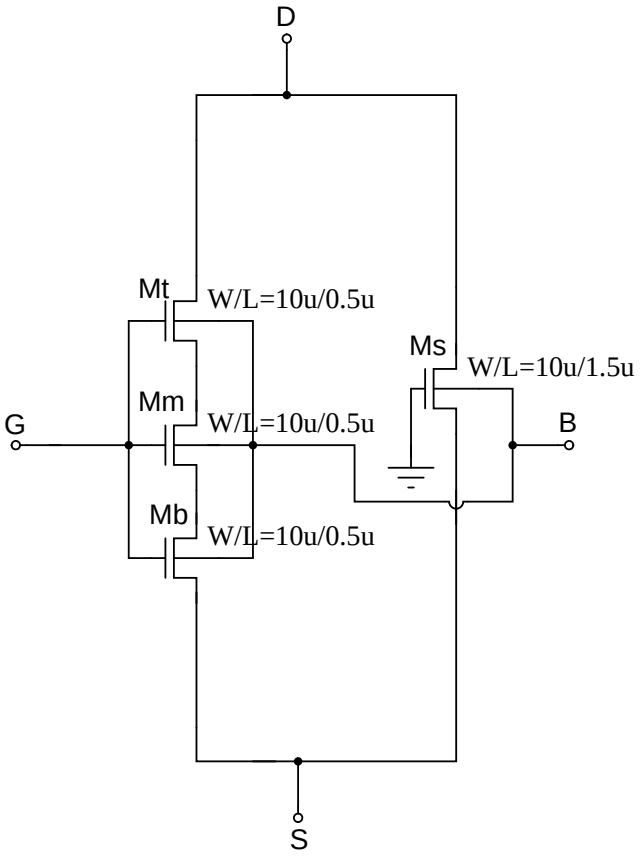


Figure 6.2: Seqmentation model of a MOSFET

6.2 BSIM3v3 quasi-static model

This section briefly discusses the BSIM3v3 model of the MOSFET, and the changes that are to made to the model parameters to fit for segmentation model. For a detailed discussion of the model, the reader is referred to the BSIM3v3 manual.

6.2.1 Threshold voltage

The standard threshold voltage of a MOSFET with long channel length/width and uniform substrate doping concentration is given by

$$V_{th} = V_{th0} + \gamma \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s} \right) \tag{6.1}$$

Equation 6.1 is valid only when the substrate doping concentration is constant and the channel length is long. Under these conditions, potential is uniform along the channel. But in reality, these two conditions are not always satisfied. Modifications have to be made when the substrate doping concentration is not uniform or and when the channel length is short,narrow,or both.

Threshold voltage tailoring results in vertical non-uniform doping. To take it into account, equation 6.1 is modified as:

$$V_{th} = V_{th0} + K1 \left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s} \right) - K_2 V_{bseff} \tag{6.2}$$

The doping concentration near the drain and the source is higher than that in the middle of the channel. This lateral non uniform doping will cause the threshold voltage to increase. The average channel doping can be calculated as follows:

$$N_{eff} = N_a(1 + \frac{2L_x}{L}\frac{N_{ds} - N_a}{N_a}) = N_a(1 + \frac{Nlx}{L}) \tag{6.3}$$

where L_x is the extension of drain or source into the channel. N_{ds} is the drain or source doping concentration and N_a is the substrate doping concentration. To

model lateral non uniform doping effect, equation 6.2 is modified as:

$$V_{th} = V_{th0} + K1\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) - K_2 V_{bseff} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}}\right)\sqrt{\Phi_s} \tag{6.4}$$

The short channel effects reduces the threshold voltage. To model these effects, equation 6.4 is modified as:

$$V_{th} = V_{th0} + K1\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right) - K_2 V_{bseff} + K1\left(\sqrt{1 + \frac{N_{lx}}{L_{eff}}}\right)\sqrt{\Phi_s} - \Delta V_{th} \tag{6.5}$$

where ΔV_{th} is the threshold voltage reduction due to the short channel effects. The various short channel effects include

1. narrow channel effect [1]

$$\Delta V_1 = \left(K_3 + K_{3b} V_{bseff}\right)\frac{T_{OX}}{W_{eff} + W_0}\Phi_s \tag{6.6}$$

2. DIBL effect

$$\Delta V_2 = \left(exp(-D_{sub}\frac{L_{eff}}{2l_{t0}}) + exp(-D_{sub}\frac{L_{eff}}{l_{t0}})\right)(E_{ta0} + E_{tab} V_{bseff}) V_{ds} \tag{6.7}$$

3. narrow width effect

$$\Delta V_3 = D_{VT0w}\left(exp(-D_{VT1w}\frac{W_{eff}L_{eff}}{2l_{tw}}) + 2exp(-D_{VT1w}\frac{W_{eff}L_{eff}}{l_{tw}})\right) \tag{6.8}$$

4. charge sharing effect

$$\Delta V_4 = D_{VT0}\left(exp(-D_{VT1}\frac{L_{eff}}{2l_t}) + 2exp(-D_{VT1}\frac{L_{eff}}{l_t})\right) \tag{6.9}$$

Taking all the above short channel effects into account, the threshold voltage reduction is given by:

$$\Delta V_{th} = \Delta V_1 + \Delta V_2 + \Delta V_3 + \Delta V_4 \tag{6.10}$$

[1] depletion charge increases due to fringing fields resulting in the reduction of V_{th}

l_t, l_{tw} in equations 6.8 and 6.9 are given by:

$$l_t = \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}}(1 + D_{vt2} V_{bseff}) \tag{6.11}$$

$$l_{tw} = \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}}(1 + D_{vt2w} V_{bseff}) \tag{6.12}$$

$$l_{t0} = \sqrt{\frac{\epsilon_{si} X_{dep}}{C_{ox}}} \tag{6.13}$$

$$X_{dep} = \sqrt{\frac{2\epsilon_{si}(\Phi_s - V_{bseff})}{qN_{ch}}} \tag{6.14}$$

Changes made to the V_{th} parameters

If the doping concentration is assumed to be constant through out the channel length, threshold voltage remains same through out the channel when V_{ds}=0 and V_{bs}=0. By the similar argument, the threshold voltage of the three segments should be same when V_{bs}=0 and V_{bs}=0.

The parameters D_{VT1w}, D_{VT1} and D_{sub} of the three segments, are increased by a factor of three and N_{lx} is reduced by a factor of three, so that there is no variation in V_{th} due to segmentation.

The effective channel length, L_{eff} is given by

$$L_{eff} = L_{drawn} - 2DLC \tag{6.15}$$

where, DLC is the long channel gate capacitance offset. The parameters DLC and LD[2] are reduced by a factor of three, so that L_{eff} is same for all the three transistor segments. The changes are tabulated in table 6.1.

6.2.2 Drain current equation

In strong inversion, the drain current is given by:

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + \frac{V_{ds}}{E_{sat} L}} \left(V_{gs} - V_{th} - A_{bulk} \frac{V_{ds}}{2} \right) V_{ds} \tag{6.16}$$

[2]lateral diffusion of drain and source into the channel

Table 6.1: Changes made to V_{th} parameters

Parameter	Value in QS Model	Value in Segmentation Model		
		M_t	M_m	M_b
D_{sub}	$5.000e-01$	$15.000e-01$	$15.000e-01$	$15.000e-01$
D_{VT1}	$1.039e+00$	$3.117e+00$	$3.117e+00$	$3.117e+00$
D_{VT1W}	$6.671e+04$	$20.013e+04$	$20.013e+04$	$20.013e+04$
N_{lx}	$1.888e-07$	$0.629e-07$	$0.629e-07$	$0.629e-07$
DLC	$3.000e-08$	$1.000e-08$	$1.000e-08$	$1.000e-08$
LD	$-5.005e-08$	$-1.668e-08$	$-1.668e-08$	$-1.668e-08$

where A_{bulk} is the bulk charge coefficient given by

$$A_{bulk} = A_{bulk0}\left(1+\left(\frac{CLC}{L_{eff}}\right)^{CLE}\right) \tag{6.17}$$

$$A_{bulk0} = \left(1+\frac{K_1}{2\sqrt{\Phi_s - V_{bs}}}\{\frac{A_0 L_{eff}}{L_{eff}+2\sqrt{X_j X_{dep}}}+\frac{B_0}{W_{eff}+B_1}\}\right) \tag{6.18}$$

In saturation region, we have to take $V_{ds} = V_{dsat}$. The drain current equation in linear region gets modified when we take the parasitic drain and source resistance, R_{ds}, into consideration.

$$I_{ds} = \frac{V_{ds}}{R_{total}} = \frac{V_{ds}}{R_{ds}+R_{ch}} \tag{6.19}$$

where R_{ch} is the channel resistance and R_{ds} is given by

$$R_{ds} = \frac{R_{dsw}[1+P_{rwg}V_{gseff}+P_{rwb}(\sqrt{\phi_s - V_{bseff}}-\sqrt{\phi_s})]}{(10^6 W_{eff})^{W_r}} \tag{6.20}$$

Considering the output resistance in the channel region, there are three physical mechanisms which affect the output resistance in the saturation region: channel length modulation(CLM), drain induced barrier lowering(DIBL), and the substrate current induced body effect. All three mechanisms affect the output resistance in the saturation region. The drain current depends very weekly on V_{ds} in saturation region. A Taylor series expansion can be used to expand the drain

current in saturation region.

$$I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{dsat}) + \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}}(V_{ds} - Vdsat) \quad (6.21)$$

$$\equiv I_{dsat}(1 + \frac{V_{ds} - V_{dsat}}{V_A}) \quad (6.22)$$

where,

$$I_{dsat} = I_{ds}(V_{gs}, V_{dsat}) = W v_{sat} C_{ox}(V_{gseff} - V_{th} - A_{bulk} V_{dsat}) \quad (6.23)$$

and

$$V_A = I_{dsat}(\frac{\partial I_{ds}}{\partial V_{ds}})^{-1} \quad (6.24)$$

The parameter V_A is called early voltage and is introduced for the analysis of the output resistance.

The early voltage due to DIBL effect is given by:

$$V_{ADIBL} = \frac{V_{gtseff} + 2v_t}{\theta_{rout}(1 + P_{DIBLCB} V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gtseff} + 2v_t}\right) \quad (6.25)$$

where,

$$\theta_{rout} = P_{diblc1} \left(exp(-D_{rout} \frac{L_{eff}}{2l_t}) + 2exp(-D_{rout} \frac{L_{eff}}{l_t})\right) + P_{diblc2} \quad (6.26)$$

The early voltage due to channel length modulation is given by

$$V_{ACLM} = \frac{1}{P_{clm}} \frac{A_{bulk} E_{sat} L + V_{gst}}{A_{bulk} E_{sat} l}(V_{ds} - V_{dsat}) \quad (6.27)$$

where l is proportional to junction depth, x_j.

The total early voltage is given by,

$$V_A = V_{Asat} + (\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBL}}) \quad (6.28)$$

where V_{Asat} is the early voltage when $V_{ds} = V_{dsat}$. It is introduced to obtain continuity between linear and saturation region.

Changes made to the parameters affecting I_d and r_o

The value of bulk charge coefficient, A_{bulk}, is 1 for long channel devices. As the device becomes shorter it's value increases. The parameter A_0 is increased so that the bulk charge coefficient is not affected by the segmentation. Also the output resistance, r_0 of the short channel devices reduces due to CLM and DIBL effects. The reduction in output impedance due to segmentation is overcome by increasing the parameter D_{rout}. The body effect coefficient of DIBL parameters, P_{diblcb} is reduced nearly by a factor 2.9 so as to reduce the additional body effect experienced by the middle and top segments. The output impedance reduces when body effect increases. The increase in body effect due to segmentation is overcome by reducing the value of P_{diblcb}. The changes are tabulated in table 6.2.

Table 6.2: Changes made to drain current parameters

Parameter	Value in QS Model	Value in Segmentation Model		
		M_t	M_m	M_b
D_{rout}	$5.000e-01$	$10.750e-01$	$10.750e-01$	$10.750e-01$
A_0	$2.541e+00$	$3.812e+00$	$3.812e+00$	$3.812e+00$
P_{diblcb}	$3.222e-01$	$1.111e-01$	$1.111e-01$	$1.111e-01$

6.2.3 Extrinsic parameters

The extrinsic parameters include the overlap capacitances, junction capacitances and the parasitic resistaces. The overlap capacitances are modelled by the parameters C_{gdo}, C_{gdl} for gate to drain and C_{sdo}, C_{sdl} for gate to source. The junction capacitances are modelled by parameters C_j, C_{jsw}. The junction capacitances are made zero in all the three segments. Another transistor, M_s of same size as the single transistor, is connected in parallel with the three segments to take care of junction capacitances. It is biased in cutoff region by connecting its gate to ground. The overlap capacitances of M_s are made zero and its other parameters remain same as the single transistor. Table 6.3, shows the changes made to extrinsic parameters. The parasitic drain/source resistance is distributed equally among

Table 6.3: Changes made to extrinsic parameters

Parameter	Value in QS Model	Value in Segmentation Model		
		M_t	M_m	M_b
C_{gdo}	$1.200e-10$	$1.200e-10$	$0.000e+00$	$0.000e+00$
C_{gdl}	$1.310e-10$	$1.310e-10$	$0.000e+00$	$0.000e+00$
C_{gso}	$1.200e-10$	$0.000e+00$	$0.000e+00$	$1.200e-10$
C_{gsl}	$1.310e-10$	$0.000e+00$	$0.000e+00$	$1.310e-10$
C_j	$9.400e-04$	$0.000e+00$	$0.000e+00$	$0.000E+00$
C_{jsw}	$2.500e-10$	$0.000e+00$	$0.000e+00$	$0.000E+00$
R_{dsw}	$3.449e+02$	$1.150e+02$	$1.150e+02$	$1.150e+02$
No of drain squares	NRD	NRD	0	0
No of source squares	NRS	0	0	NRS
Drain area	AD	AD	0	0
Source area	AS	0	0	AS
Drain perimeter	PD	PD	0	0
Source perimeter	PS	0	0	PS

all the three segments by reducing the parameter, R_{dsw} by a factor of three. The sheet resistance of the source/drain diffusion region is made zero by making the number of source/drain squares, NRS/NRD zero.

6.2.4 Noise parameters

This section discusses noise model parameters, and changes made to them to for segmentation model.

Thermal noise model

In QS model the default thermal noise model is spice2 model, i.e,

$$S_{thermal} = \frac{8kT}{3}(g_m + g_{mb} + g_{ds}) \tag{6.29}$$

In segmentation model the thermal noise model is changed to BSIM3v3 model. i.e,

$$S_{thermal} = \frac{4kT}{{L_{eff}}^2}|Q_{inv}| \tag{6.30}$$

where, Q_{inv} is the inversion layer charge.

Flicker noise model

In QS model the default flicker noise model is BSIM3v3 model. It has been changed to spice2 model in the segmentation model. The spice2 model for flicker noise is

$$S_{flicker} = \frac{K_f I_{ds}^{af}}{C_{ox}{L_{eff}}^2 f^{ef}} \tag{6.31}$$

where af is the frequency exponent, ef is flicker exponent and K_f is flicker noise parameter.

The NOIMOD flag has been changed accordingly, in segmentation model, to account for these changes.

Table 6.4: Changes made to NOIMOD flag

Parameter	Value in QS Model	Value in Segmentation Model		
		M_t	M_m	M_b
NOIMOD	3	4	4	4

6.3 Simulation results

Various simulations are run for both QS model and segmentation model with W=2.2u and L=0.6u. Simulation results should match at DC, which makes sure that the segmentation model is valid at low frequencies also. But, at higher frequencies the simulation results with both the models deviate considerably.

6.3.1 Drain current characteristics

The drain current characteristics are shown in the figure 6.3. The curves match with a maximum error of ±3.8%.

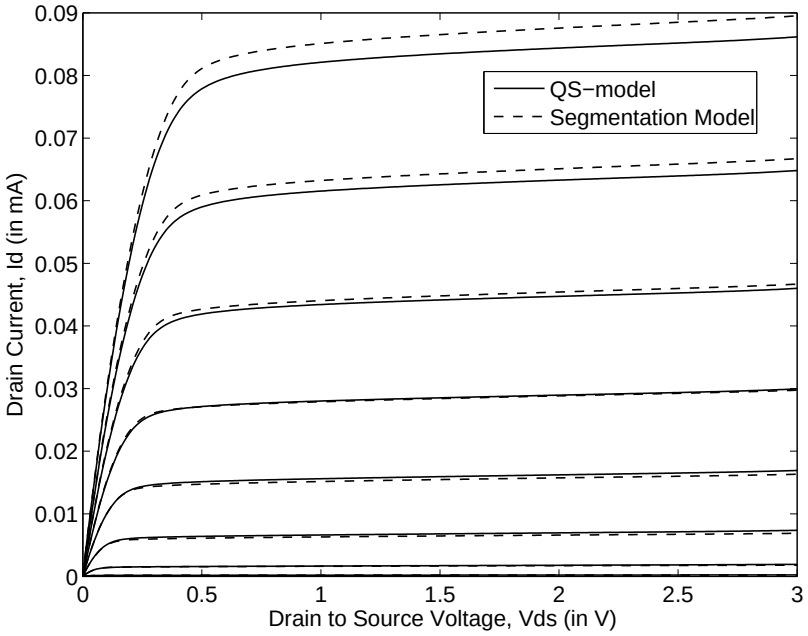


Figure 6.3: Id vs Vds curves for $V_{bs} = 0,\ W = 2.2u,\ L = 0.6u$

6.3.2 I-V characteristics for diode connection

The I-V characteristics of a diode connected MOSFET are plotted for both QS and segmentation models. The I-V curves are shown in figure 6.4. There is a maximum discrepancy of +6%.

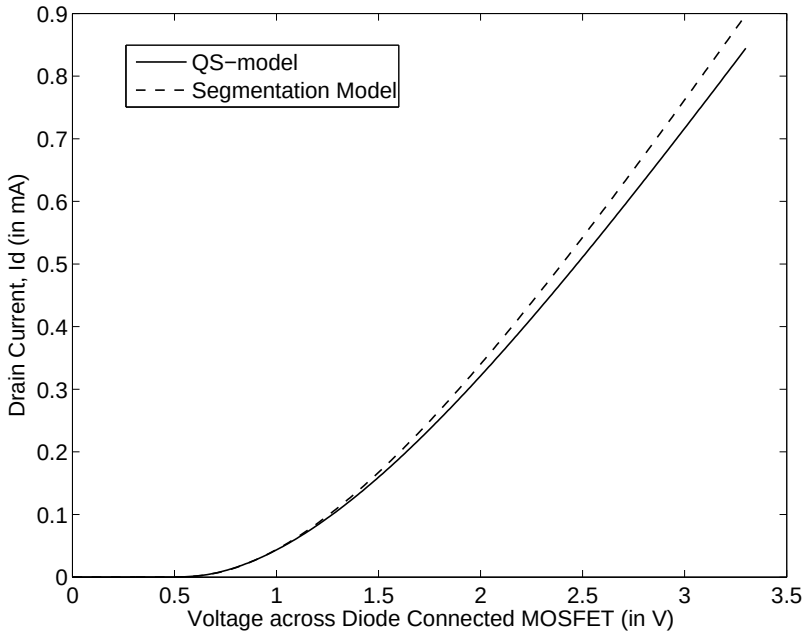


Figure 6.4: I-V curves for diode connection with $V_{bs} = 0, W = 2.2u, L = 0.6u$

6.3.3 g_m, g_{mb} and $g_m r_o$ Vs I_d Characteristics

The transconductance g_m and the intrinsic gain $g_m r_o$ are obtained as function of the drain current for both models. The results are shown in figure 6.5. At $33.6\mu A$, the maximum error in g_m is +4% and the maximum error in $g_m r_o$ is +7.8%. Figure 6.6 shows plot of g_{mb} Vs drain current At $I_d = 33.6\mu A$, the error in g_{mb} is +2.6%.

6.3.4 Input admittance at the gate

In QS model, the input admittance, being capacitive, is directly proportional to the frequency .

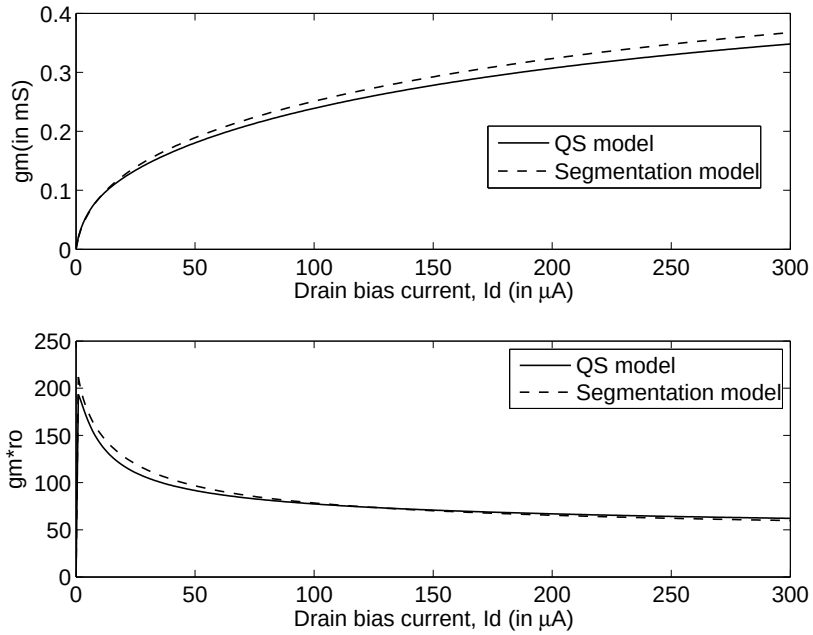


Figure 6.5: g_m and $g_m r_o$ Vs drain current for $V_{bs} = 0, W = 2.2u, L = 0.6u$

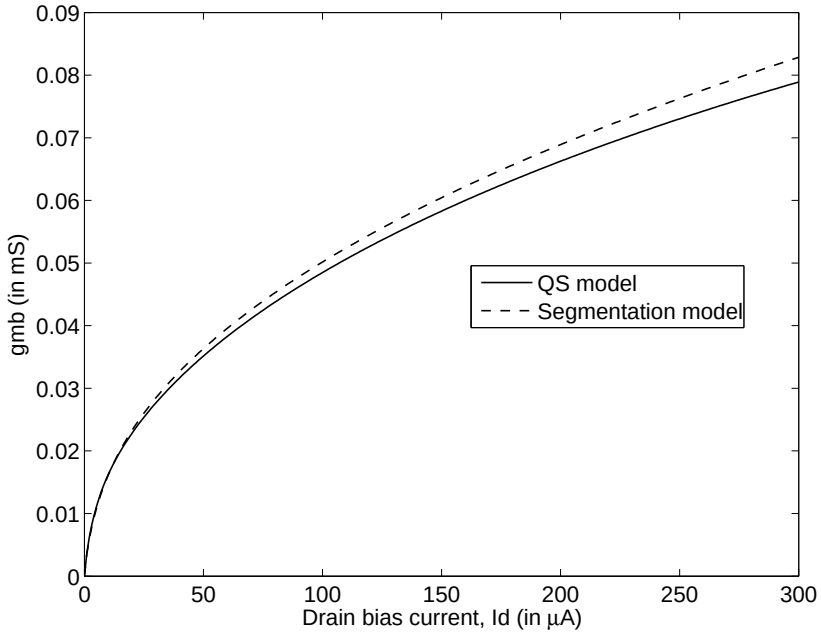


Figure 6.6: g_{mb} Vs drain current for $V_{bs} = 0, W = 2.2u, L = 0.6u$

In the segmentation model, the input admittance is not purely capacitive. The channel being a distributed RC network, the input impedance is a series combination of resistance and capacitance. Thus, the input admittance approaches equivalent conductance of the distributed RC network, as the frequency increases. The simulation results are shown in figure 6.7.

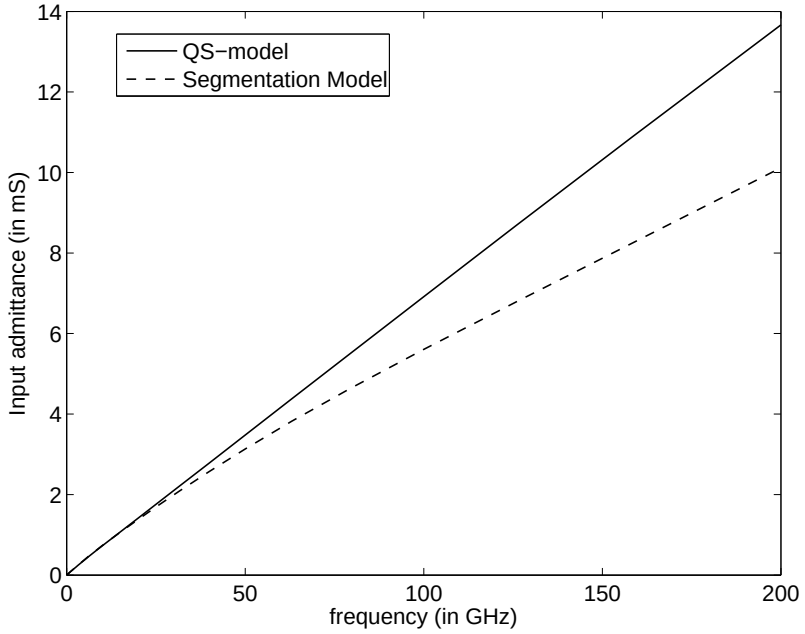


Figure 6.7: Input admittance Vs frequency

6.3.5 Noise

The drain noise current spectral density and the induced gate noise current spectral density are obtained for QS and the segmentation model, at a given drain current. The simulation results are shown in figure 6.8.

Drain current noise

The drain current noise should match for both the quasi static and the segmentation model. The error in drain current thermal noise spectral density is -3.84%.

Induced gate noise

The drain noise current will induce noise in the gate terminal through capacitive coupling between channel and the gate. In reality, the channel of a MOSFET is a distributed RC network and there is capacitive coupling between the channel and the gate. As the frequency increases, this coupling increases and hence the gate induced noise increases with frequency. As the number of segments increases, capacitive coupling to the channel increases and and the gate induced noise approaches the theoretical value.

The gate induced noise is given by

$$S_{ig} = 4kTg_g * \frac{4}{3} \tag{6.32}$$

where,

$$g_g = \frac{1}{5}\frac{\omega^2 {C_g}^2}{g_{ds}|_{V_{DS}=0V}} \tag{6.33}$$

The theoretical value of the gate induced noise, for W=2.2u and L=0.6u, is $1.106e-13\ \frac{A}{\sqrt{Hz}}$ at 1 GHz and it's value is $0.885e-13\ \frac{A}{\sqrt{Hz}}$ for the segmentation model.

In the quasi static model there is no coupling of the channel to the gate, as the channel is modelled as a lumped RC model. The small increase in gate induced noise at higher frequencies, in quasi static model, is attributed to the voltage drop across drain resistance which is coupled to the gate through parasitic capacitances.

Figure 6.8, shows the comparison of both drain current noise and gate induced noise for both Quasi-static model and Segmentation model.

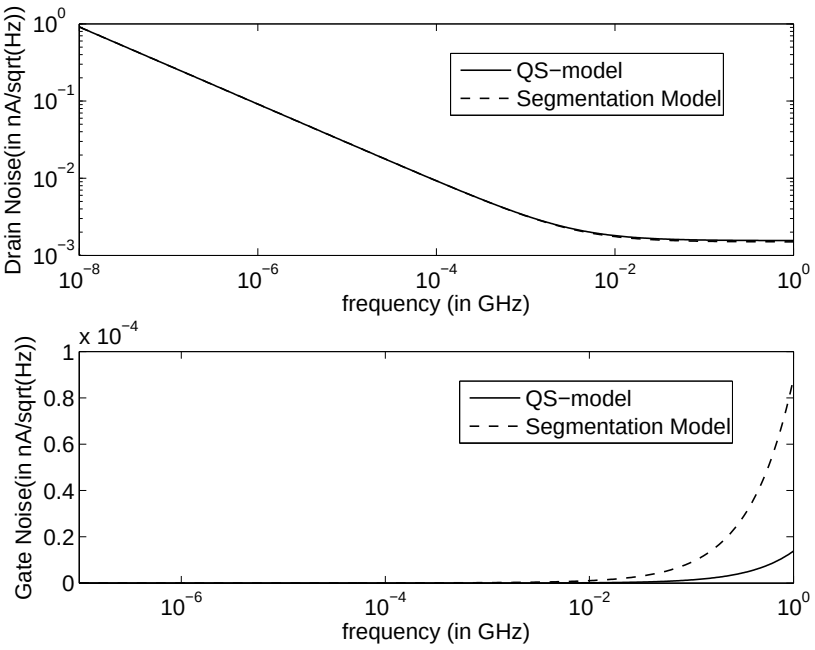


Figure 6.8: Drain noise current and Induced gate noise current Vs frequency

6.4 Response of Chebyshev filter

. The segmentation model is used to simulate 70-500MHz Programmable Gm-C Chebyshev filter. The netlist of the filter is taken from [1], and segmentation model is used for the input transistors corresponding of all transconductors. The macro-model of the filter is shown in figure 6.9. The filter is simulated with following

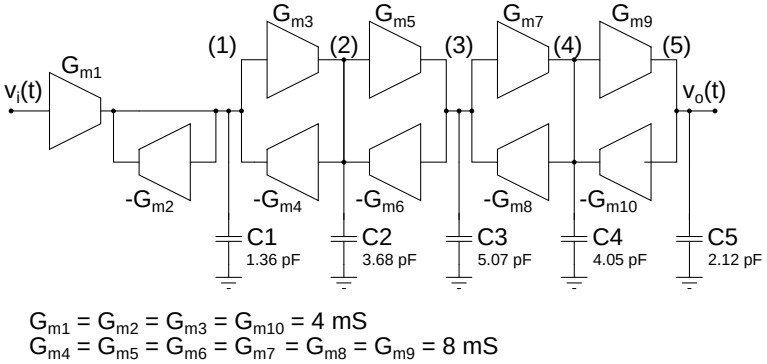


Figure 6.9: Macro model of the Chebyshev filter

three models:

1. Quasi-static model with xpart=1 i.e charge partitioning of 40/60.

2. Quasi-static model with xpart=0 i.e. charge partitioning of 0/100.
3. Segmentation Model

The transconductance of a MOSFET has a time constant, τ associated with it i.e, g_m is modelled as

$$\frac{g_m}{1+s\tau}$$

and the input impedance is a series combination of R and C. Both these NQS effects are taken care in the segmentation model.

In the quasi static model, with xpart=1, the time constant τ is assumed to be zero and the input impedance is assumed to be purely capacitive.

In the quasi static model, with xpart=0, the g_m of the transistor is modelled as

$$g_m\,(1-s\tau)$$

which is a valid assumption for low frequencies.

Output response

The Chebyshev filter is simulated with all the three models and it's normalized magnitude response is shown in figure 6.10. Time constant, associated with g_m, causes the $j\omega$ axis to shift towards left half plane as the frequency increases. A clear explanation of this frequency shift is given in [9].

There is more peaking in the magnitude response at higher frequencies with both segmentation model and QS model with xpart=0. The peaking in case of segmentation model is less than the peaking in QS model with xpart=0. The peak in case of first case is 1.46, while it is 1.38 in the second case. The bandwidth has increased with both segmentation model and QS model with xpart=0.

Figure 6.11 shows the normalized magnitude response in dB. The same filter is simulated for minimum possible bandwidth of 70MHz. The normalized magnitude response is shown in the figure 6.12. Peaking in the magnitude response is less in this case. The magnitude responses with QS model(xpart=0) and segmentation

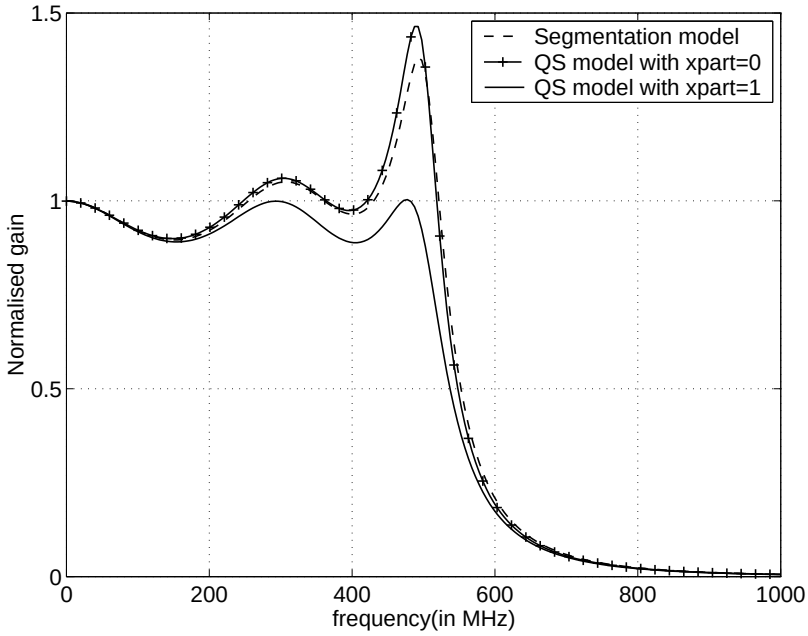


Figure 6.10: Normalized magnitude response of the Chebyshev filter for maximum bandwidth

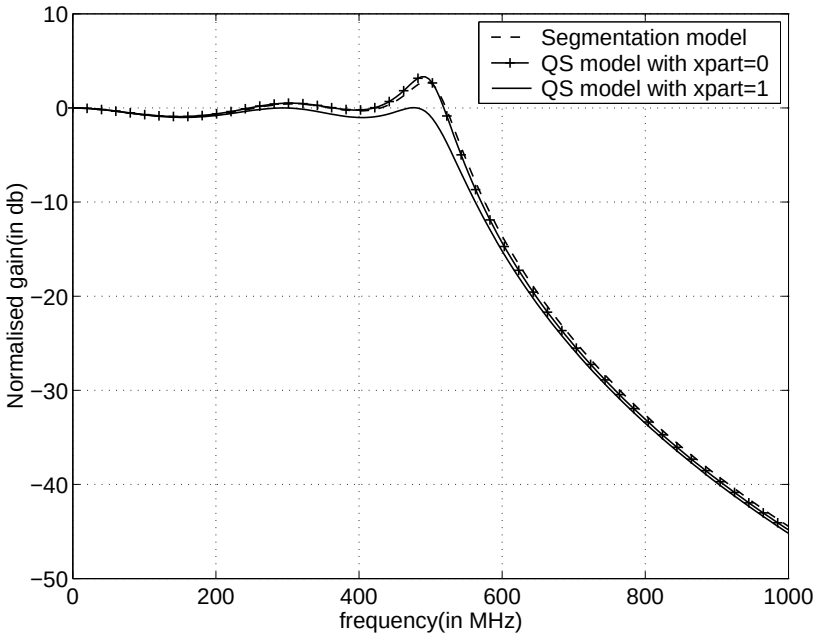


Figure 6.11: Normalized magnitude response(in dB) of the Chebyshev filter for maximum bandwidth

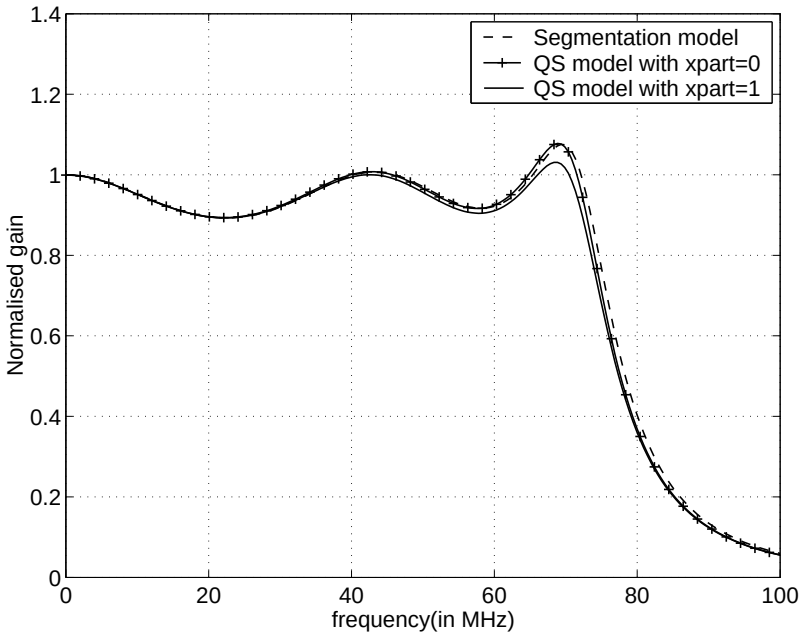


Figure 6.12: Normalized magnitude response of the Chebyshev filter for minimum bandwidth

model almost match with each other. This is because at low frequencies,

$$\frac{g_m}{1+s\tau} \simeq g_m(1-s\tau)$$

Figure 6.13 shows the magnitude response in dB.

Output noise

The output noise of the filter is shown in figure6.14. The error in output noise at low frequencies, with the segmentation model, is -3.9% and this is due to the errors in g_m, g_{mb} and r_o.

Figure 6.15 shows the normalized noise.

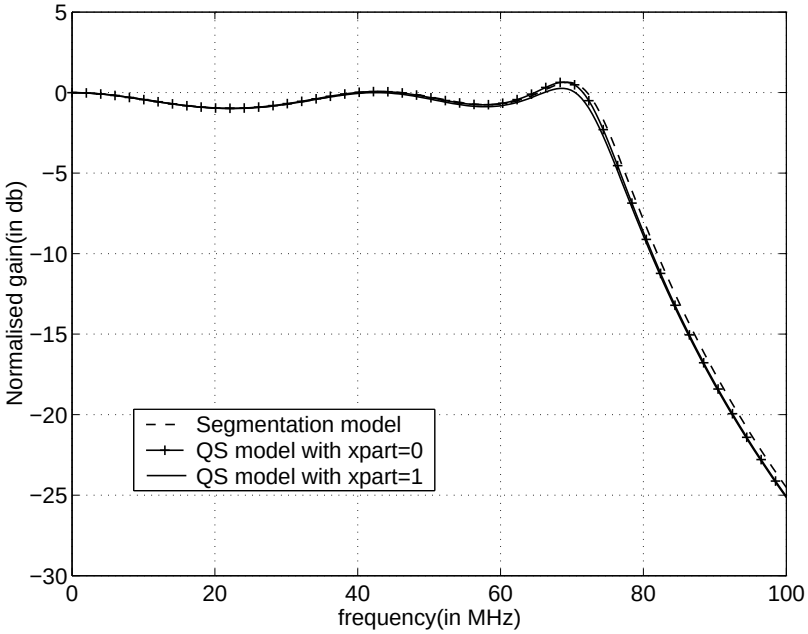


Figure 6.13: Normalized magnitude response(in dB) of the Chebyshev filter for minimum bandwidth

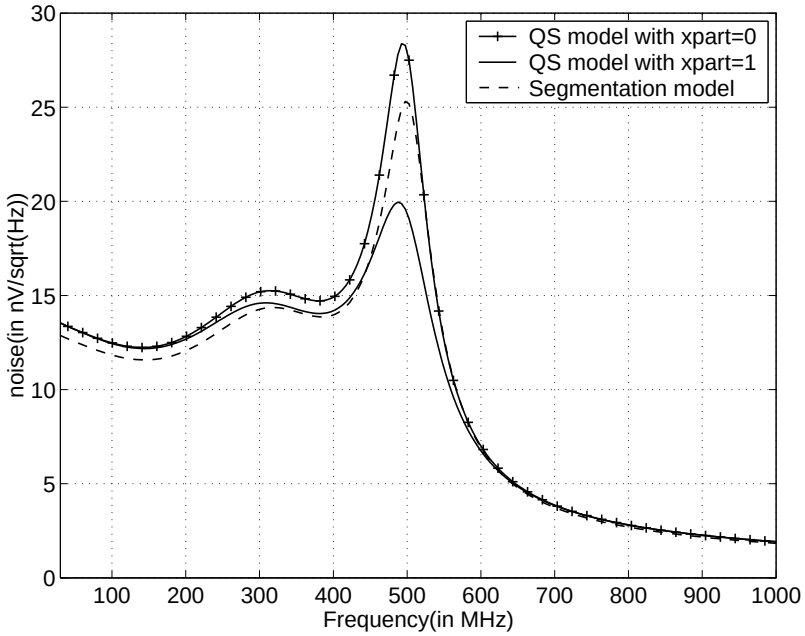


Figure 6.14: Output noise of the Chebyshev filter

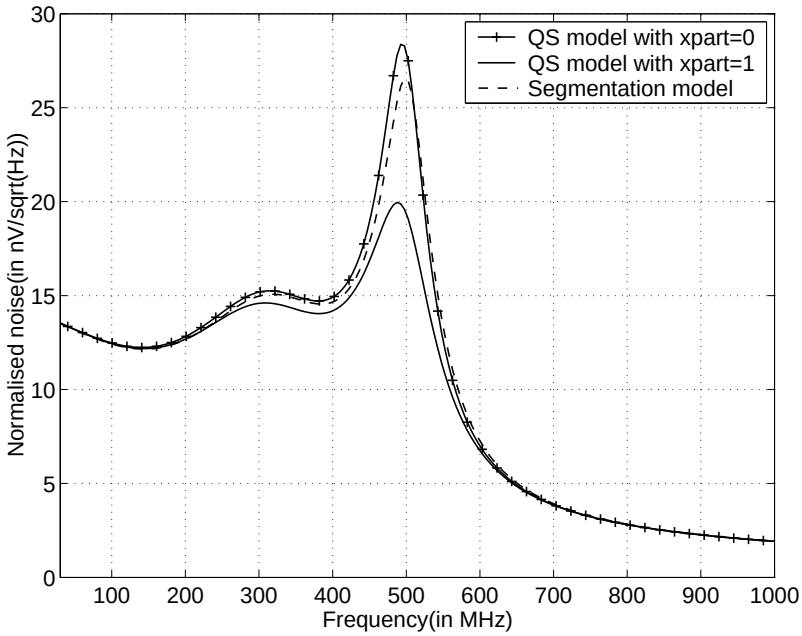


Figure 6.15: Normalized output noise of the Chebyshev filter

6.5 Conclusion

A segmentation model is developed using BSIM3v3 quasi-static model. The model is used to simulate high frequency Gm-C filter. The model predicts Non-quasi-static effects of MOSFET successfully. Simulation time increased considerably when segmentation model is used. A much careful modeling of segments will lead to better matching of segmentation model with QS model at DC.

APPENDIX A

Right half plane zero cancellation

The integrator, realized using OTA, will have a right half plane zero which reduces the phase margin of the system. To cancel the effect of right half plane zero, a compensating resistor R_z is introduced in series with the integrating capacitor.

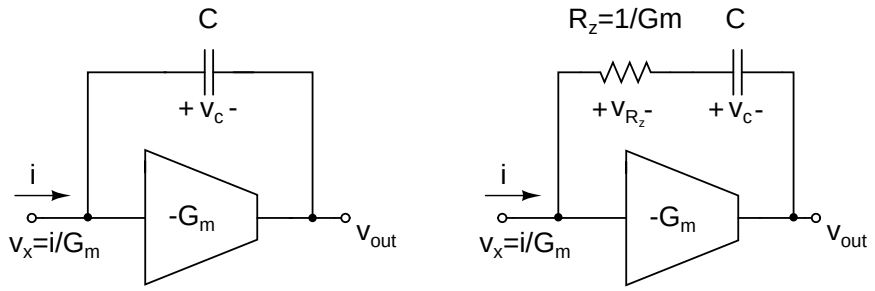


Figure A.1: OTA-C integrator with and without R_z

OTA-C integrator without R_z

$$\begin{aligned} v_{out} &= -v_c + v_x && \text{(A.1)} \\ &= -\frac{i}{sC} + \frac{i}{G_m} && \text{(A.2)} \\ &= i\left(\frac{1}{G_m} - \frac{1}{sC}\right) && \text{(A.3)} \end{aligned}$$

From, equation A.3, the right half plane zero is given by,

$$s = \frac{G_m}{C} \qquad \text{(A.4)}$$

OTA-C integrator with R_z compensation

$$
\begin{aligned}
v_{out} &= -v_c - v_{R_z} + v_x && \text{(A.5)} \\
&= -\frac{i}{sC} - \frac{i}{G_m} + \frac{i}{G_m} && \text{(A.6)} \\
&= -\frac{i}{sC} && \text{(A.7)}
\end{aligned}
$$

Thus, the right half plane zero can be eliminated if $R_z = \frac{1}{G_m}$. In reality, the cancelling won't be accurate, If $R_z > \frac{1}{G_m}$, the zero moves towards $-\infty$, and if $R_z < \frac{1}{G_m}$, the zero moves towards $+\infty$.

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