# 16 bit Calibrated Current Steering Audio Band Digital-to-Analog Converter

*A Project Report*

*submitted by*

**PAWAN AGARWAL**

*in partial fulfilment of the requirements*
*for the award of the dual degree of*

**BACHELOR OF TECHNOLOGY**
**and**
**MASTER OF TECHNOLOGY**


**DEPARTMENT OF ELECTRICAL ENGINEERING**
**INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.**

**MAY 2009**

# THESIS CERTIFICATE

This is to certify that the thesis titled 16 bit Calibrated Current Steering Audio Band Digital-to-Analog Converter, submitted by **Pawan Agarwal**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** and **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

**Dr. Nagendra Krishnapura**
Research Guide
Assistant Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai
Date: 30th April 2009

# ACKNOWLEDGEMENTS

First and foremost, my special gratitude is due to my brother Pradeep, for his sacrifice and loving support. I want to thank my parents, who loved me and taught me the value of hard work by their own example. To them, I dedicate this thesis.

I offer my sincerest gratitude to my supervisor, Dr Nagendra Krishnapura, who has supported me throughout the project with his patience and knowledge whilst allowing me the room to work in my own way. He always provided encouragement, sound advice, good teaching, good company, and lots of good ideas. I would have been lost without him.

Dr.Shanthi Pavan's profound knowledge and timely wit came as a boon. His valuable suggestions as final words during the course of work are greatly acknowledged. What I know today about the process of research, I learned from Dr. Nagendra and Dr.Shanti Pavan. I learned to believe in my future work and myself. Thank you Professors.

I would like to thank Saurabh Saxena and Shrey Ginoria for their critical appreciation. In many ways I have learnt much from and because of them. Manoj Kumar, without his support, IIT-JEE would not have been possible. Thank you, Manoj.

In my daily work, I have been blessed with a friendly and cheerful group of friends Shantanu, Lovneet, Kedar, Dhruv, Muthu, Siva, Kartikey, labmates and batchmates. Thanks a lot guys.

Finally, I would like to thank the members of *Pink Floyd* for showing me *The Dark Side of The Moon.*

# ABSTRACT

A 16 bit calibrated current steering audio band digital-to-analog converter is presented in this work. Oversampling sigma-delta architectures are preferred for such low-speed, high dynamic range applications because of their immunity to mismatch in the components used and because they contain predominantly digital circuitry. The matching required for the components can be orders of magnitude less when compared to current steering D/A converters. However, a recent concern has been with the use of delta sigma converters which have large out of band noise with class D switching amplifiers. Some of the out of band noise of the delta sigma D/A converters can be modulated by the switching frequency of the class D amplifier and fold into the audio band, thus deteriorating the signal to noise ratio. This has motivated research in traditional nyquist rate D/A converter architectures which do not have sharply rising out of band noise spectral density.

An additional benefit of the nyquist rate D/A converter is the reduced oversampling ratio. Digital circuitry running at the high oversampled rate dissipates large amount of power in delta sigma D/A converters. Digital circuitry in a nyquist rate D/A converter consumes less power because of reduced oversampling ratio.

Current steering architectures can be used for low-speed, high dynamic range and low out of band noise applications. In a modern VLSI fabrication process, the matching between two components can range from 0.1% to 1%, which is unacceptable for a converter of 16 bit resolution. However reducing mismatch in MOS devices for acceptable linearity requires very large device sizes. Therefore, a background calibration technique is employed to cancel out the effect of mismatch in the current source array.

The 16 bit D/A converter is segmented in 6+6+4 thermometer fashion to

achieve best performance in terms of DNL/INL with minimum complexity and area. The oversampling ratio can be programmed from 4X to 512X. The D/A converter is realized using a pMOS and an nMOS current source array in parallel followed by an I-V converter. Two different schemes of switching the p and n current sources which tradeoff distortion with idle channel noise are provided for. The I-V conversion is performed by a three stage class AB operational amplifier. This converter is implemented in 0.18 $\mu$m UMC CMOS technology, with a 1.8 V power supply. For simulations, the sampling frequency ($f_s$) is 6.144 MHz (OSR of 128X) and signal frequency $f_{in}$ is $\sim$1KHz. The D/A converter consumes $\sim$700 $\mu$W for the analog circuit and $\sim$410$\mu$W for the digital circuit. It occupies an area of 1138$\mu$m $\times$ 942$\mu$m.

Another part of this work is the design of a deserializer for convenient measurement of a high speed delta sigma A/D converter. Due to limitations of measurement instrumentation available, the data rate has to be brought down before it can be processed. The deserializer can split the input data stream of 1 GHz frequency into two data streams at 500 MHz frequency. The output of the deserializer is transmitted in LVDS standard. The deserializer is implemented in 0.18 $\mu m$ UMC CMOS technology, with a 1.8 V power supply. Total power consumed by the deserializer is $\sim$60 mW. The layout occupies an area of 372$\mu$m$\times$ 242$\mu$m.

# TABLE OF CONTENTS

# LIST OF FIGURES

# ABBREVIATIONS

| | |
|---|---|
| **DAC** | Digital to Analog Converter |
| **MSB** | Most Significant Bit |
| **USB** | Uppermost Significant Bit |
| **LSB** | Lowest Significant Bit |
| **OSR** | Over Sampling Ratio |
| **DNL** | Differential Non-Linearity |
| **INL** | Integral Non-Linearity |
| **SNR** | Signal to Noise Ratio |
| **SFDR** | Spurious Free Dynamic Range |
| **THD** | Total Harmonic Distortion |
| **DR** | Dynamic Range |
| **CML** | Current Mode Logic |
| **LVDS** | Low Voltage Differential Signaling |

# CHAPTER 1

# Introduction

A 16 bit current steering calibrated audio band D/A converter is presented in this thesis. The advantage of this type of converter is the absence of sharply rising out of band noise and low power consumption. The audio band extends from 20Hz to 22kHz. The Nyquist sampling rate is 48kHz.

Generally, oversampling sigma-delta architectures are used for this application. However, some of the out of band noise of the sigma-delta D/A converters can be modulated by the switching frequency of the class D amplifier and folds into the audio band. This has motivated to use a nyquist rate D/A converter, as it has a very low out of band noise spectral density.

A background calibration technique is implemented to minimize the effect of the current source transistor mismatch. The current steering DAC suffers from the flicker noise contribution of the MOS transistor current source. The calibration of the current cells affects the flicker and the thermal noise spectrum because of switching, which is explained in Chapter 3.

The current steering D/A converter consists of current sources which are switched between the output and the terminating voltage source, depending on the input signal. The DAC is implemented in a segmented thermometer coded design. The thermometer D/A converter is employed with pMOS and nMOS differential current steering architecture to get an optimum performance, which is explained in the Section. 4.2.2. Different types of current switching schemes are implemented to get the desired performance under different conditions. Furthermore, programmable OSR gives flexibility to accept the input which is sampled at various frequencies. The calibration clock is randomized to avoid harmonic tones at the calibration frequency.

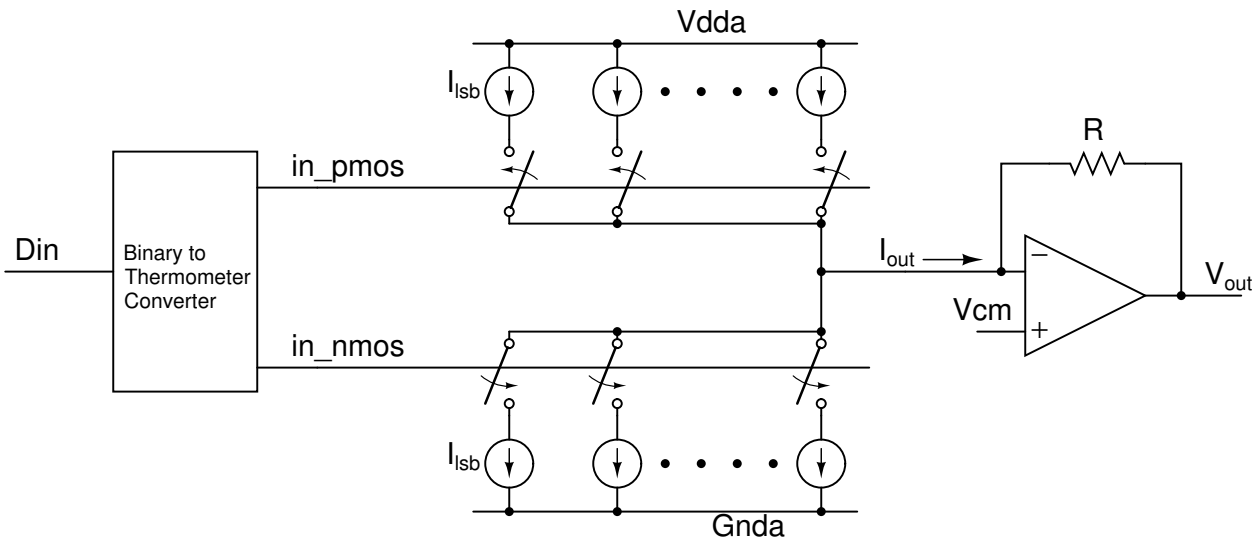


Figure 1.1: Current Steering D/A converter Architecture

The main aim of this design is to minimize the power and the out of band noise. Apart from this, the DAC must be monotonic. Here a programmable oversampling ratio varying from 4X to 512X is used. The total power consumption of the converter is ≈1.1 mW and the area is 1138$\mu$m × 942$\mu$m. The out of band non-harmonic tones are at ≈-120 dB. As the input code goes from 0 to $2^{16} - 1$, the output voltage swings from -0.75 V to +0.75 V. The full specification of the D/A converter is given in Chapter 2.

Apart from the above, a deserializer is also built to convert a high frequency input signal into two parallel streams of low frequency signals. This deserializer is not a part of the D/A converter described above. The deserializer is used with a high speed $\Delta\Sigma$ modulator. Deserializer presented here is tested with a signal of frequency 1 GHz which is converted to two signals at the frequency of 500 MHz. A LVDS trasmitter is then used to transmit the signal in standard LVDS format. The deserializer is implemented in 0.18 $\mu$m UMC CMOS technology, with a 1.8 V power supply. Total power consumed by the deserializer is ∼60 mW. The layout occupies an area of 372$\mu$m × 242$\mu$m.

The organization of the thesis is as follows:

**In Chapter 2** we present an overview of system design and architecture.

**In Chapter 3** we present noise analysis.

**In Chapter 4** we present the chosen DAC architecture and circuit diagrams.

**In Chapter 5** we present the calibration circuit, its issues and their solutions.

**In Chapter 6** simulation and layout results are presented.

**In Chapter 7** we present a deserializer.

**In Chapter 8** we present conclusion and future work.

# CHAPTER 2

# System Design and Specification

The Audio Band Digital-to-Analog converter has the specifications given in Table. 2.1:

## 2.1 Segmentation

The D/A converter can be implemented mainly in Binary weighted or Thermometer weighted current source or as a combination of both.

The advantage of a binary weighted DAC is that, no input decoding logic is required as the digital inputs directly control the switches. However, during the mid code transition(01111... to 10000..), the MSB current source needs to be matched to the sum of all other current sources within 0.5 LSB. Because of process variations and mismatch, this is very difficult to guarantee. Therefore, this architecture cannot be monotonic. Also at the mid code transition, all the switches switch simultaneously, which can give a highly non-linear large mid code glitch.

In a N-bit thermometer weighted DAC, there are $2^N$ unit current sources. In this case, a binary to thermometer code converter is used to decode the digital

Table 2.1: DAC Specifications

| | |
|---|---|
| Oversampling ratio | 4X to 512X |
| Dynamic Range | 100 dB(flat)/102dB(A-weighted) |
| Distortion | <-80 dB |
| Idle Channel Noise | $< 5\mu$V |
| Out of band tones | <-120 dB |
| Power | $< 1\ mW$ |

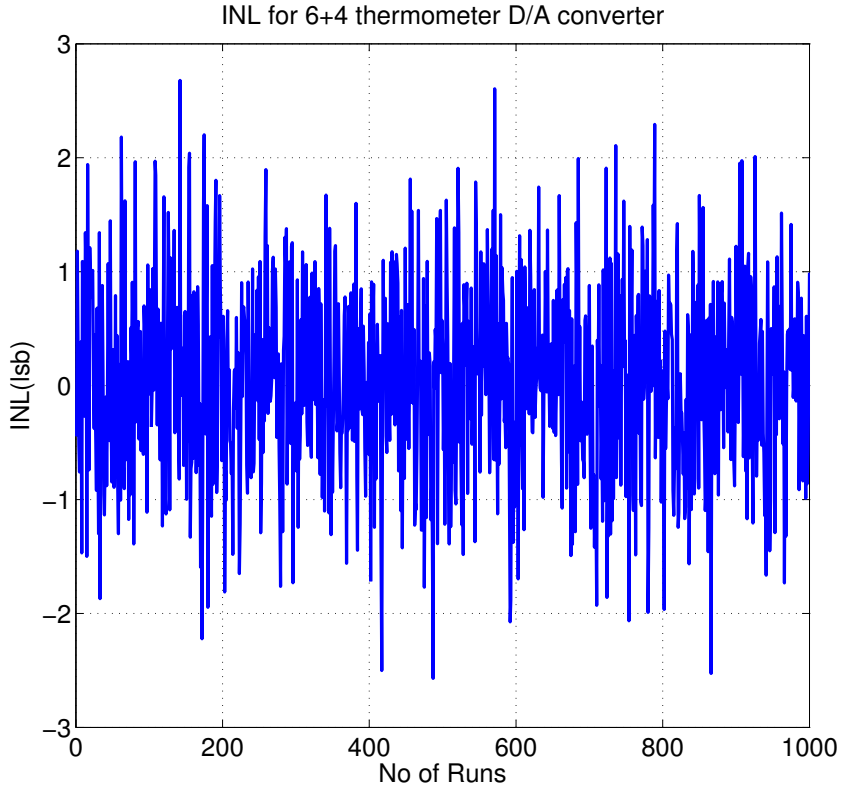


Figure 2.1: Maximum INL for each simulation of 6+4 fully thermometer DAC

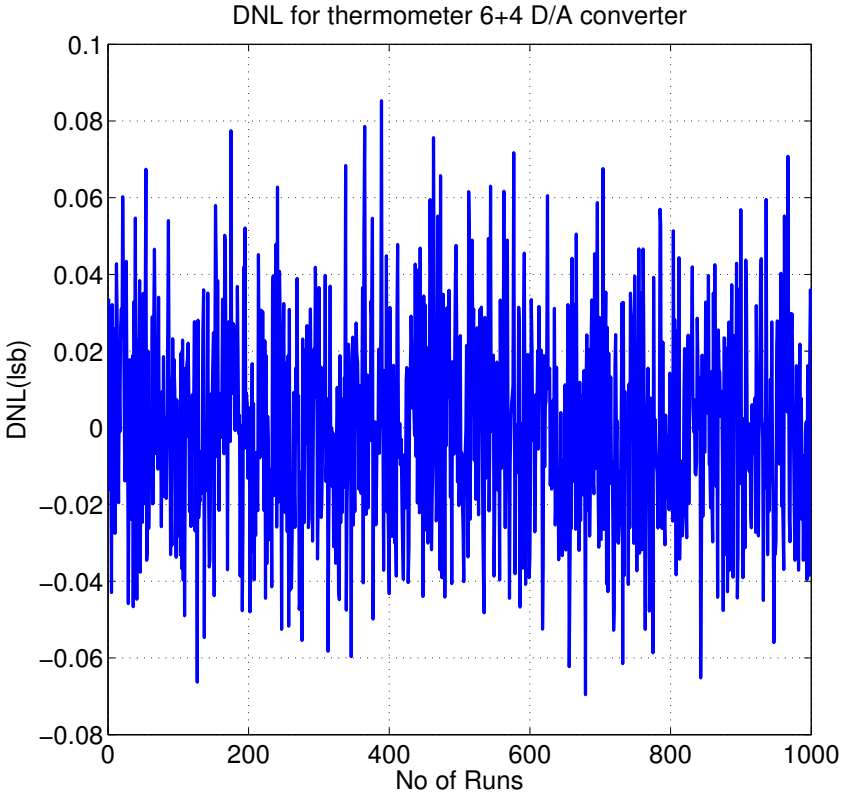


Figure 2.2: Maximum DNL for each simulation of 6+4 fully thermometer DAC

inputs. When the digital input increases by 1 LSB, one more current source is switched from the negative side to the positive side. In a thermometer DAC, analog output always increases as digital input increases. Hence, monotonicity is guaranteed using this architecture. Here, the magnitude of the glitch is directly proportional to the input amplitude step.

Since monotonicity is a very strict requirement, as implied by the above argument, the DAC needs to be implemented in thermometer fashion. Since $2^N$ current sources are practically infeasible to implement, the DAC needs to be segmented. The DAC is segmented as follows. First, we segment the 16 bit DAC in 6+10 to minimize complexity. The 10 bit DAC is further segmented in 6+4 as discussed in Ref. [1]. This is also implemented in thermometer weighted DAC to ensure complete monotonicity.

$$\frac{{\sigma_I}^2}{I^2} = \frac{4{A_{vt}}^2}{WL(V_{gs} - V_{th})^2} \tag{2.1}$$

The $\frac{\sigma_I}{I}$ for INL and DNL simulation is calculated using Eqn. 2.1, where the device sizes and MOS overdrive is chosen according to the noise and bias considerations explained in later chapters. The constant values are $A_{vtN} = 4.787mV * \mu m$ and $A_{vtP} = 4.6899mV * \mu m$, as given in Ref. [2]. The results of 1000 MATLAB simulations for INL and DNL of a 6+4 segmented thermometer DAC are shown in Fig. 2.1 and Fig. 2.2.

## 2.2 Architecture

The DAC was implemented as a 6+6+4 segmented architecture, as shown in Fig. 2.3. The switches and the nMOS current sources are not shown in the Fig. 2.3 for simplicity. To minimize the flicker noise and increase the matching, long devices has been chosen. The general calibration scheme is shown in Fig. 2.4. In the used calibration technique, we compare the current of the main cell to a reference cell and vary the gate voltage of MOS device using a calibration opamp, till its current

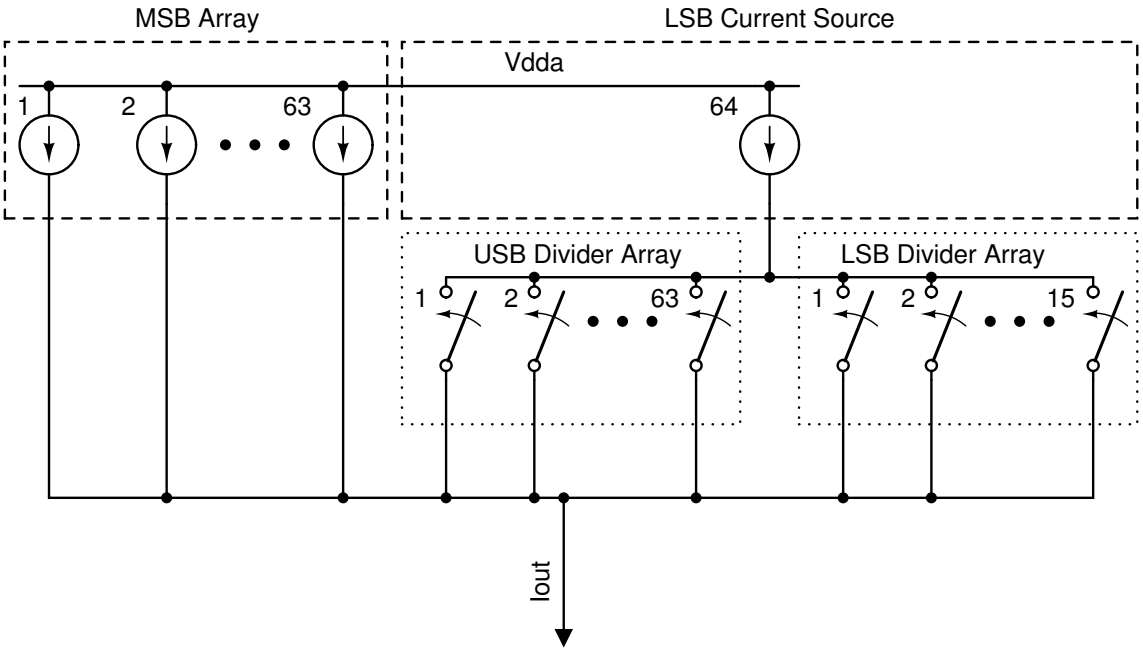


Figure 2.3: Block Diagram of 6+6+4 Segmented Architecture

is same as that of the reference current cell. A background calibration technique is used to maintain continuity in the output. When a particular cell is being calibrated, the input of this cell is fed to a dummy MSB cell which provides the same current. All the current cells and dummy cells are calibrated continuously to avoid distortion due to charge leakage through gate capacitance of the current source. A constant IR biasing technique is employed to avoid the output swing variation across the process corners. The full swing DAC current is $37.5\mu A$, which is converted using a I-V converter three stage op-amp (Ref. [3]) into 0.5Vrms. The $I_{msb}$ is 585.9375 nA and $I_{lsb}$ is 572.2 pA. Due to the very small current, extra care needs to be taken while calibrating, as the charge injection and leakage current can produce large changes in the cell current thereby generating distortion. Also, the calibration period should be sufficient to minimize distortion due to mismatch.

### 2.2.1 Differential Architecture

The current steering DAC can be implemented as only pMOS current sources, only nMOS current sources or as a combination of both. Assuming that DAC is

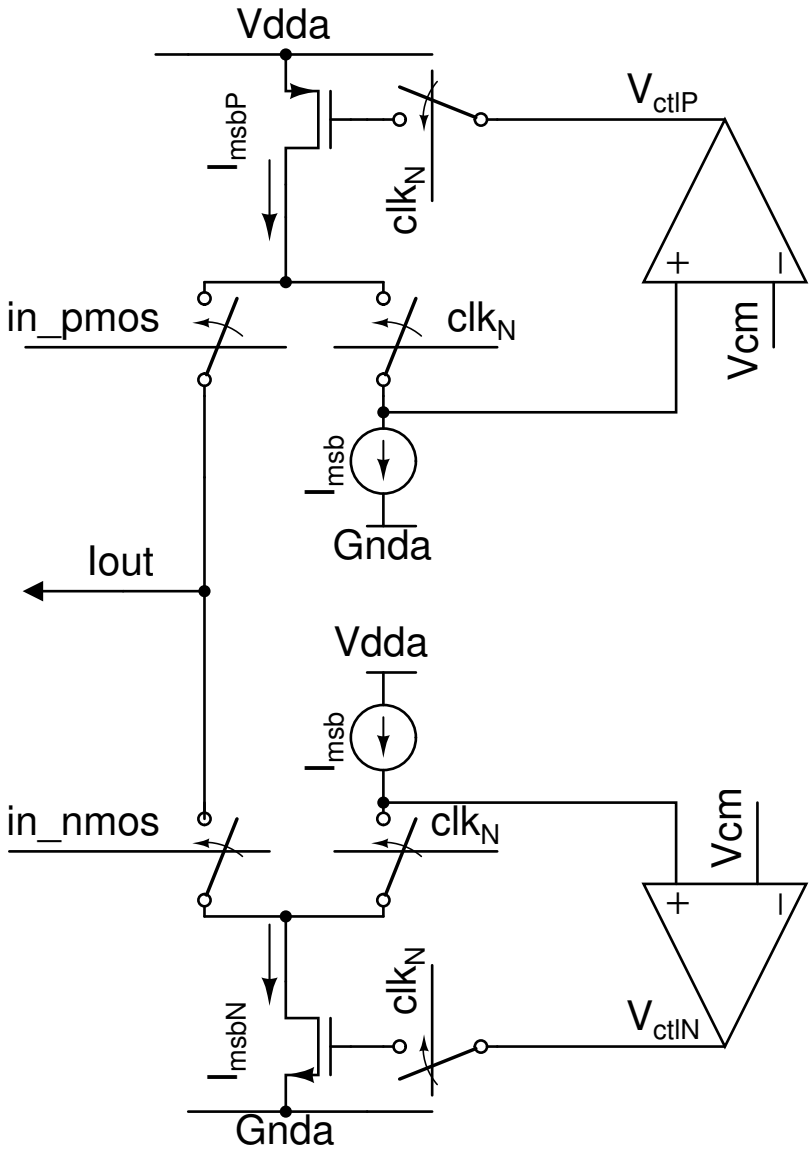


Figure 2.4: General calibration scheme

implemented as the pMOS current sources, for a given output swing of $\pm I_0$, the pMOS current cells should have a peak value of $2I_0$. A nMOS current source of value $I_0$ is used as shown in Fig. 2.5 for providing a constant current of value $-I_0$ at the output. When all the pMOS current sources are ON, the current at the output will be equal to $2I_0 - I_0 = +I_0$ and when all the pMOS current sources are OFF, the current at the output will be $-I_0$. In this case, the noise will be maximum when all the pMOS current sources are ON, the noise of the bias circuit will get multiplied by transconductance $g_m$ of nMOS and $2g_M$ of pMOS current sources assuming the same overdrive $V_{GST} = (V_{GS} - V_{TH})$. Additionally, the noise due to current sources will also be high ($\propto 2I_0 + I_0$).

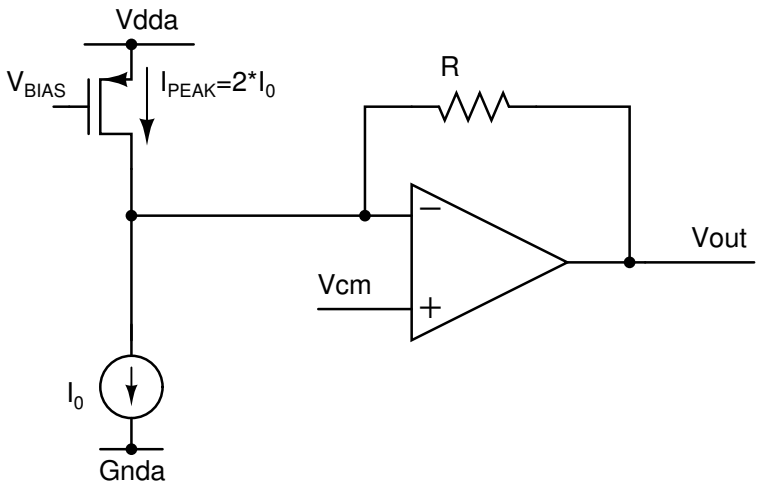


Figure 2.5: Single ended current steering DAC

In the case, when both the nMOS and the pMOS current sources are used, there will be maximum noise when the current sources are at their peak values. Since its a differential architecture, at the peak, only one type of the current sources will be ON. This means that the bias noise will get multiplied by the transconductance $g_m$ of either the pMOS current source or of the nMOS current source. This clearly shows an improvement by 3X in the noise. Also, it has smaller current consumption for the same output swing ($I_0$ compared to $2I_0 + I_0$ of single ended case). Hence, the differential architecture is used in the design.

# CHAPTER 3

# Noise analysis

## 3.1 Noise

The MOS transistor exhibits two types of noise, the thermal noise and the flicker noise. While the thermal noise is constant over the entire frequency spectrum, the flicker noise or $1/f$ noise has a power spectral density $PSD(f)$ inversely proportional to the frequency $f$ (-10dB/decade). Below the $1/f$ corner frequency $f_c$, the flicker noise dominates the thermal noise. $1/f$ corner frequencies, typically well above the audio band in newer CMOS processes, can be problematic. The noise can also get folded due to sampling of the noise on the gate capacitance of the MOS current source. Expression for flicker noise and the thermal noise in a MOSFET are given below along with the expression for resistor's thermal noise:

$$S_{MOSflicker}(f) \quad \alpha \quad \frac{1}{f} \tag{3.1}$$

$$S_{MOSthermal}(f) \quad = \quad \frac{8}{3}kTg_m\frac{\mathrm{V}^2}{\mathrm{Hz}} \tag{3.2}$$

$$S_{resistor}(f) \quad = \quad 4kTR\frac{\mathrm{V}^2}{\mathrm{Hz}} \tag{3.3}$$

Where, $S$ = noise power spectral density

$f$ = frequency

$k$ = Boltzmann constant

$T$ = absolute temperature

$g_m$ = device transconductance

## 3.2 Noise modeling

The total noise of the system ($I_{out}(n)$) gets affected mainly due to factors given below:

- Bias voltage noise getting converted to the current noise through $g_m$ of the current sources.
- Noise folding due to the switched biasing[4].
- Low pass filtering of the noise due to the calibration loop response.

### 3.2.1 Noise sources

The main noise contributors, as shown in Fig. 3.1 are:

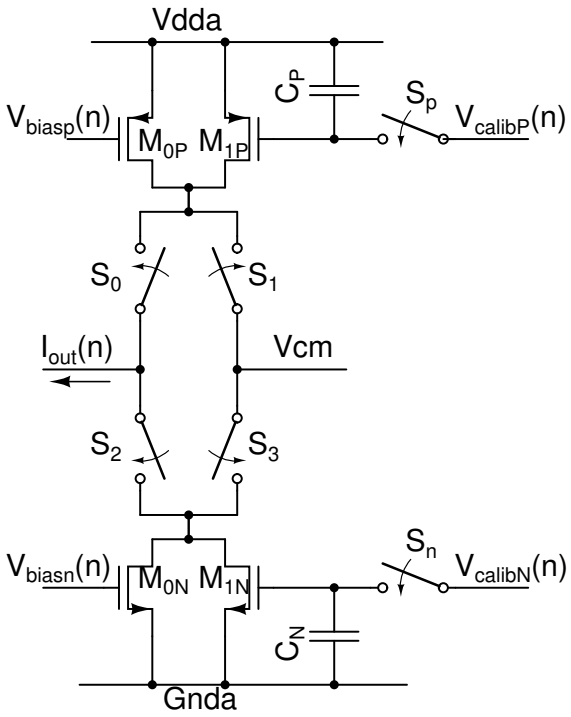


Figure 3.1: Noise sources

- The current sources $M_{0P}$, $M_1$, $M_{0N}$ and $M_{1N}$.
- The noise voltage of the bias generation circuit ($V_{biasP}(n)$, $V_{biasN}(n)$) getting converted to the noise current through the transconductance of $M_{0N}$, $M_{0P}$.

- The noise voltages of the the calibration opamp ($V_{calibP}(n)$, $V_{calibN}(n)$) getting sampled onto the capacitors $C_P$ and $C_N$, periodically through the switches $S_P$ and $S_N$. This noise then gets converted to the output noise current through the transconductance of $M_{1N}$ and $M_{1P}$. The switches are operated using the calibration clock.

Here, we have neglected the noise of switches and the power supply for calculation purposes.

### 3.2.2 Noise folding

Folding of the noise spectrum occurs at two points in the loop, shown in Fig. 3.1. First, it occurs at the switches $S_p$ and $S_n$. A noise model is shown in the Fig. 3.2, where the noise source $n_1(t)$ is getting multiplied by the $1/N$ duty cycle clock signal $P_1(t)$ (where N is the number of cells to be calibrated) because of the switching. This is similar to the situation where, the calibration opamp's noise $V_{calibP}(n)$ gets multiplied with the clock signal of switch $S_p$ and gets sampled onto the capacitor $C_P$. The picture is the same for nMOS and pMOS in terms of the noise response.

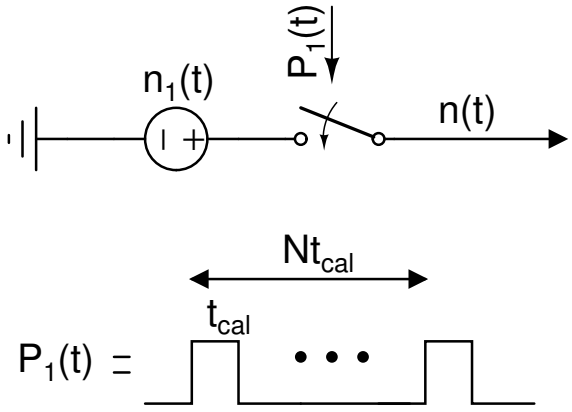


Figure 3.2: Noise model

$$
\begin{aligned}
n(t) &= n_1(t) \times p_1(t) && (3.4)\\
N(f) &= N_1(f) \otimes P_1(f) && (3.5)\\
n_1(t) &= n_{01}(t) + n_{02}(t) && (3.6)\\
n_{01}(t) &= \frac{8}{3} kT g_m && (3.7)\\
n_{02}(t) &= n_{opamp}(t) \times p_2(t) && (3.8)\\
p_1(t) &= [u(t) - u(t - t_1)] \otimes \Sigma\delta(t - nT) && (3.9)\\
P_1(f) &= \frac{1}{j2\pi f}(1 - e^{-j2\pi f t_1}) \times \Sigma\frac{1}{T}\delta(f - \frac{n}{T}) && (3.10)
\end{aligned}
$$

Here $n_1(t)$ is the noise of the current source, $n_{01}(t)$ is the noise of the current cell and $n_{02}(t)$ is the noise sampled onto the gate capacitance of the current source. $P_1(t)$ is the controlling signal at the switch $S_0$ and $P_2(t)$ is the controlling signal at the switch $S_P$. Similar equations can be formed for the nMOS case.

Multiplication in the time domain implies convolution of the noise and the clock signal in the frequency domain. Now, $n_{02}(t)$ gets converted to current noise through transconductance of $M_{0N}$ and $M_{0P}$ and then gets added to the noise of these MOS current sources. Finally this noise is multiplied with the input signal response at the switches $S_0$ and $S_2$ respectively.

The above model was implemented in MATLAB and simulations are done for the white noise, the flicker noise and both combined. The theoretical noise folding results are shown in Fig. 3.3. Periodic steady state analysis and periodic noise analysis is used for the simulations in cadence to study the behavior of folding. Fig. 3.4 shows the circuit noise when $P_1(t)$ is constantly ON (i.e. no calibration). Fig. 3.5 shows the modulated noise because of the clock signal applied to $P_1(t)$ with different frequencies.

Theoretically, when the calibration frequency is increased by 2X, the DC value of the thermal noise goes down by $\sim 3dB$. Also the area under the main lobe of the noise spectrum increases by less than 2X compared to the case when the cali-

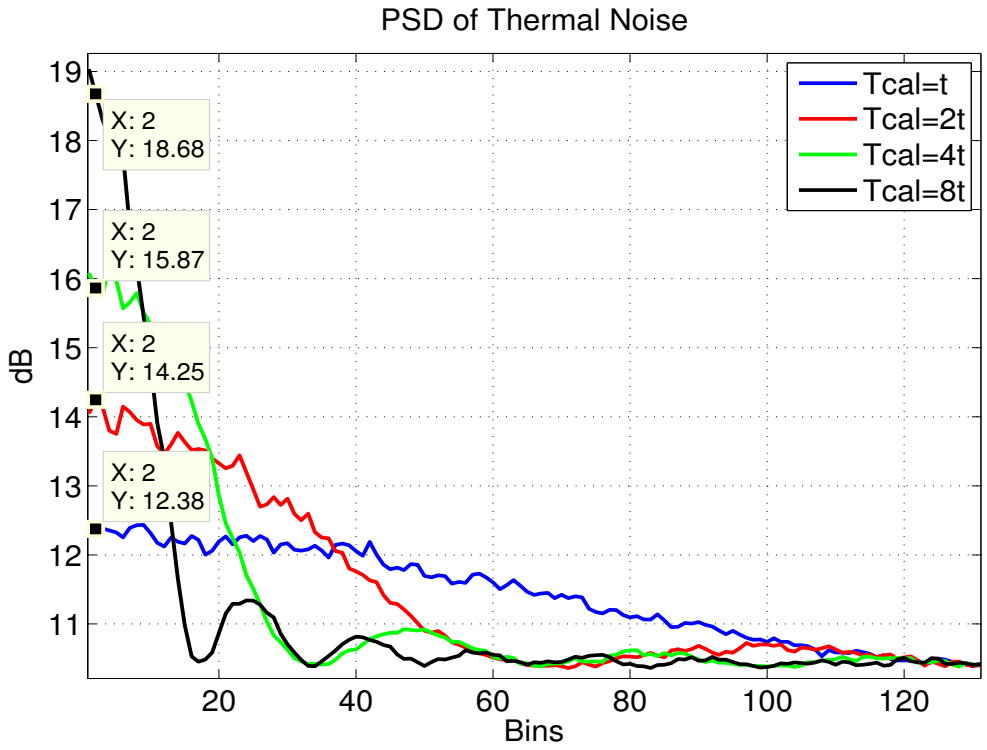


Figure 3.3: Ideal folding of thermal noise

bration frequency is 1X. In the actual simulation, when we increase the calibration frequency by 2X, the DC value is almost constant as shown in Fig. 3.5 and the total area under the lobes increases by $\sim 2X$. As the calibration frequency goes up, the differnce between the DC values goes down.

In case of the flicker noise, resetting of the noise at every calibration cycle causes the DC value to go down. MATLAB simulations show that for every 2X of calibration frequency, the noise spectral density goes down by $\sim 6dB$. The ideal effect of folding on the flicker noise is shown in Fig. 3.6. Actual simulations shows that, if we increase the calibration frequency by 2X, the DC value of the flicker noise goes down by $\sim 3dB$.

Effect of folding on the noise is seen strongly in the thermal noise compared to the flicker noise because at higher frequencies, the thermal noise is constant while the flicker noise goes down as $1/f$. Due to this reason, the thermal noise dominates the flicker noise strongly even in the audio band as shown in Fig. 3.7.

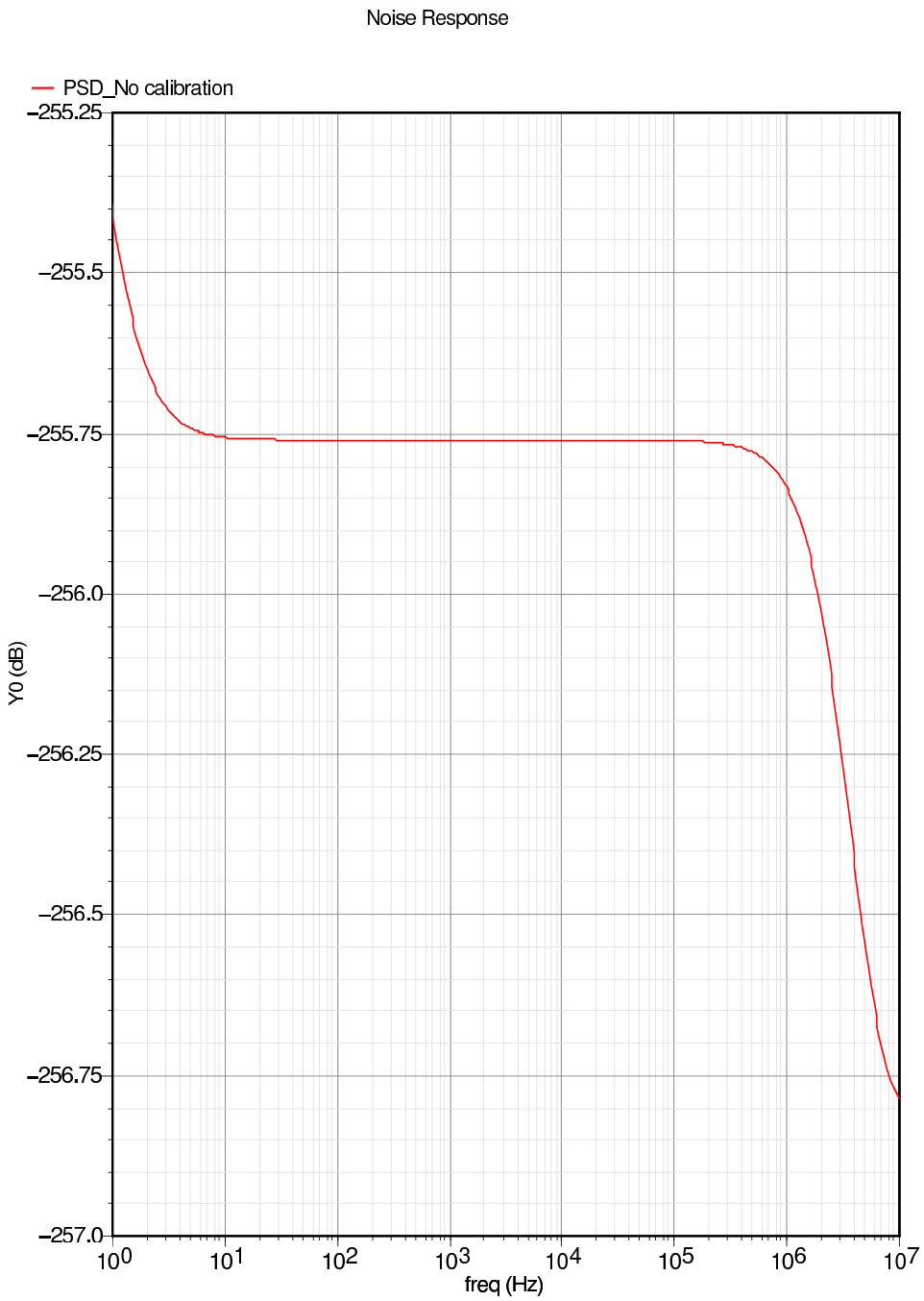


Figure 3.4: Output thermal noise without calibration

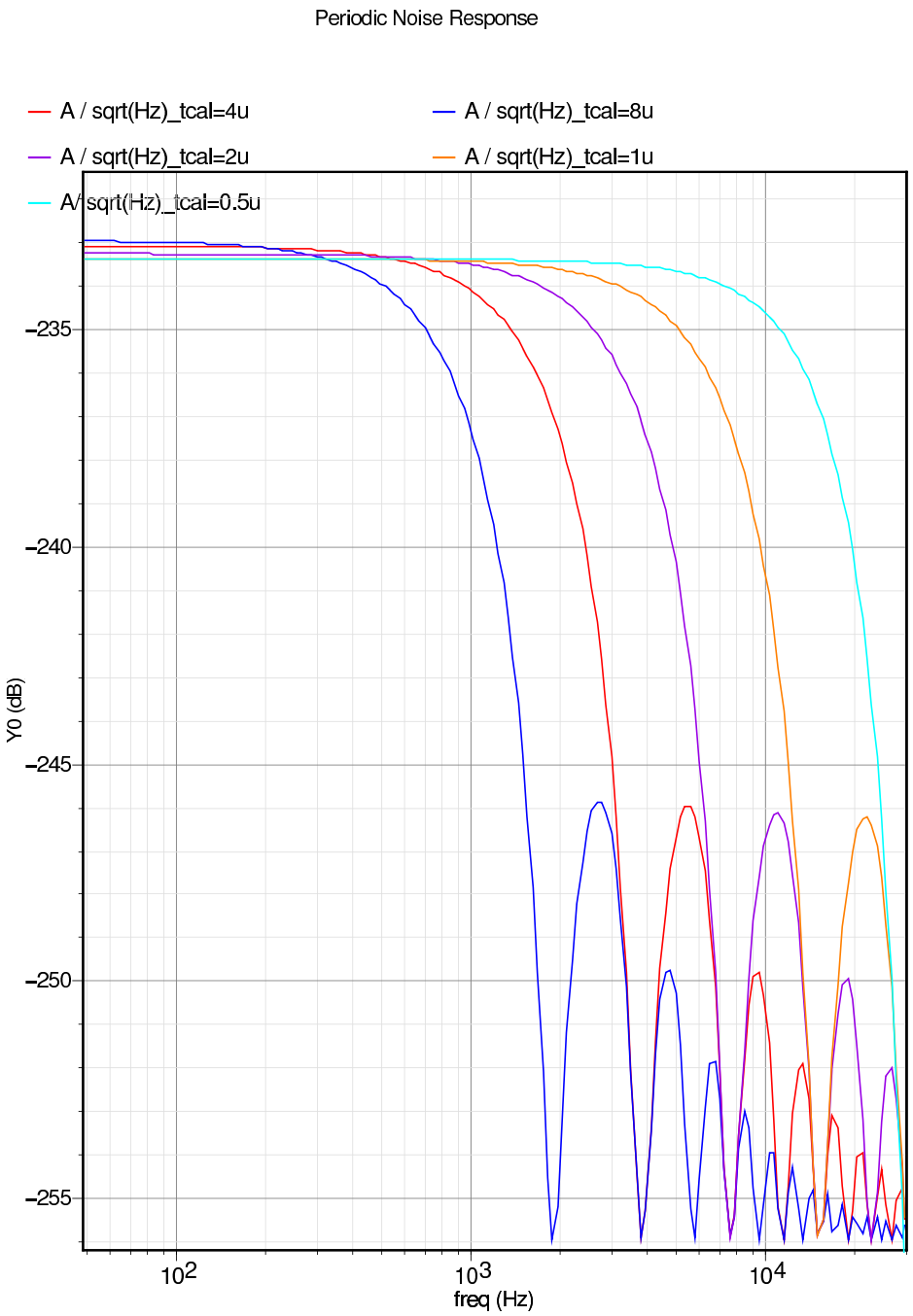


Figure 3.5: Output thermal noise with various calibration periods

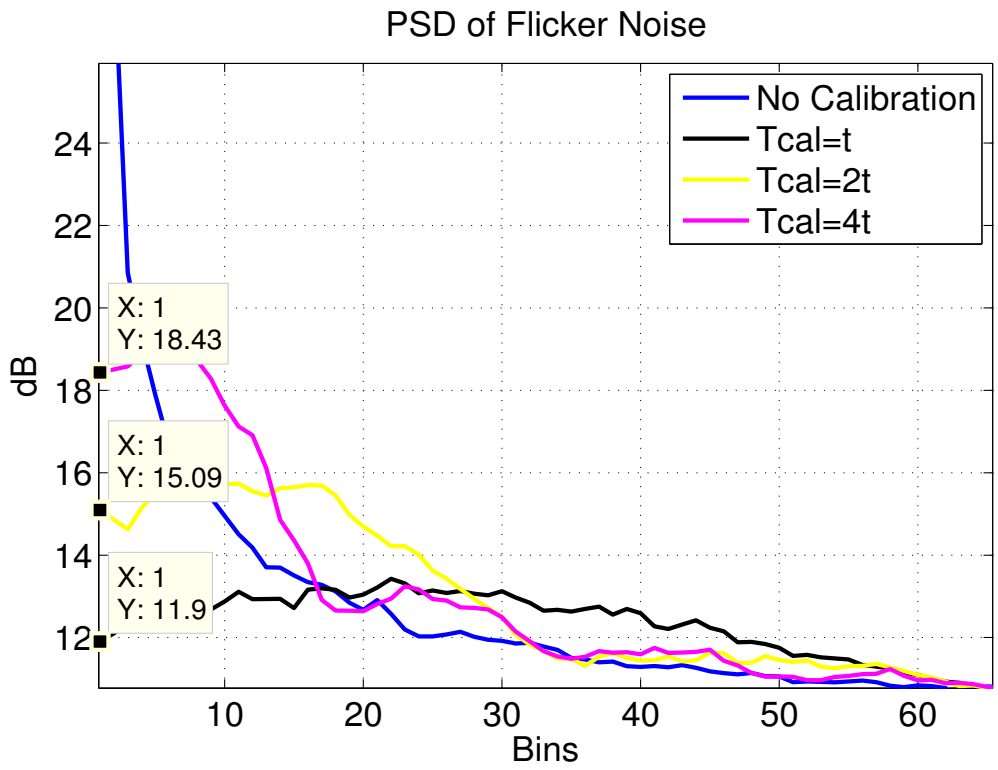


Figure 3.6: Folding of flicker noise due to calibration

Thus, even with the calibration, the total noise does not go down as expected due to the dominating nature of the flicker noise at low frequencies. In practice, the noise increases as we increase the calibration frequency. The flicker noise does not play a significant role, once it is calibrated, irrespective of the frequency.

The main lobe width of response of the total noise is $\frac{1}{Nt_{cal}}$, where $N$ is number of elements to be calibrated and $t_{cal}$ is the calibration period. From the above argument, it appears that if we increase the calibration frequency, the thermal noise will stop dominating and the total noise will go down. But then other factors (e.g. charge leakage etc) will start affecting the performance of the circuit. A proper choice has to be made in terms of the calibration period and the gate capacitance, to optimize the noise and the area.

The noise data for various calibration periods is given in Table. 3.1. The absolute noise values are taken and then normalized with respect to the no calibration case.

User: ee04b066 Date: Aug 22, 2008 Time: 5:09:38 PM IST

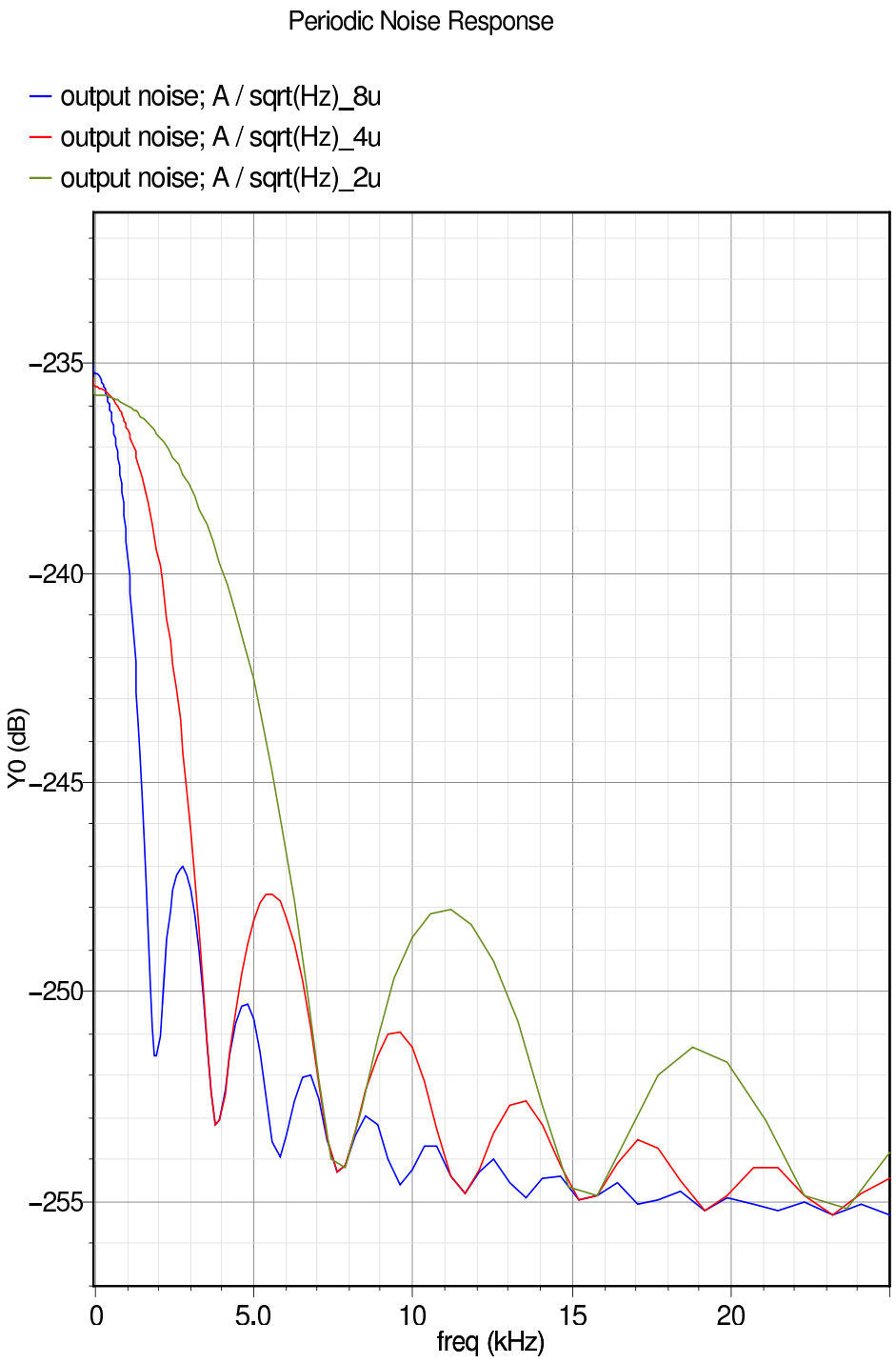


Figure 3.7: Total noise after calibration

Table 3.1: Noise values (normalized w.r.t. no calibration case) for various Calibration Periods

| $t_{cal}$ | Thermal noise | Flicker noise | Total noise |
|---|---|---|---|
| No calibration | 1 | 1 | 1 |
| $16\mu s$ | 3.42 | 1.52 | 3.03 |
| $8\mu s$ | 4.77 | 1.2 | 4.04 |
| $4\mu s$ | 12.05 | 1.1 | 9.82 |

### 3.2.3 Effect of calibration loop bandwidth on noise folding

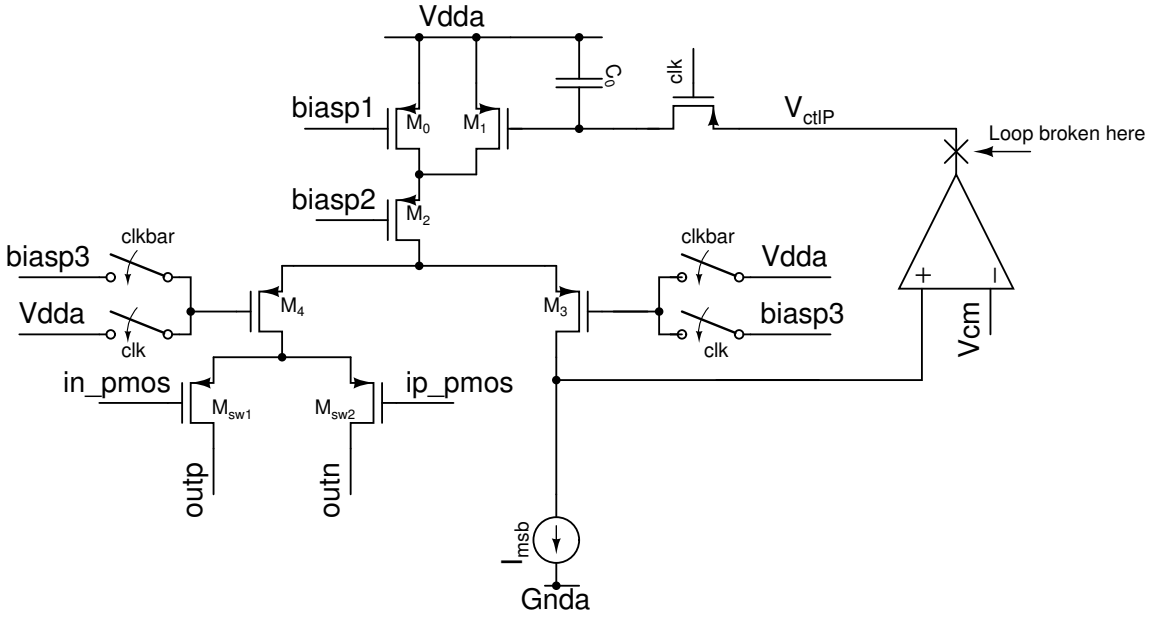


Figure 3.8: pMOS calibration loop Architecture

The amount of noise getting folded depends on the calibration loop (shown in Fig. 3.8) bandwidth. In Fig. 3.9, the squares represents the ideal loop response for different bandwidths and the blue line represents the white noise spectrum. The total noise getting folded back is equal to the area of the white noise under the ideal square loop response (product of the square box and the blue curve). As the loop bandwidth decreases (response changes from black square to red square), the noise getting filtered off due to the low pass response of the loop increases. So the noise getting folded back to the signal band decreases. Considering the above argument, the loop bandwidth has been kept to a minimum where it can calibrate

the cell in a given time without allowing any extra noise.

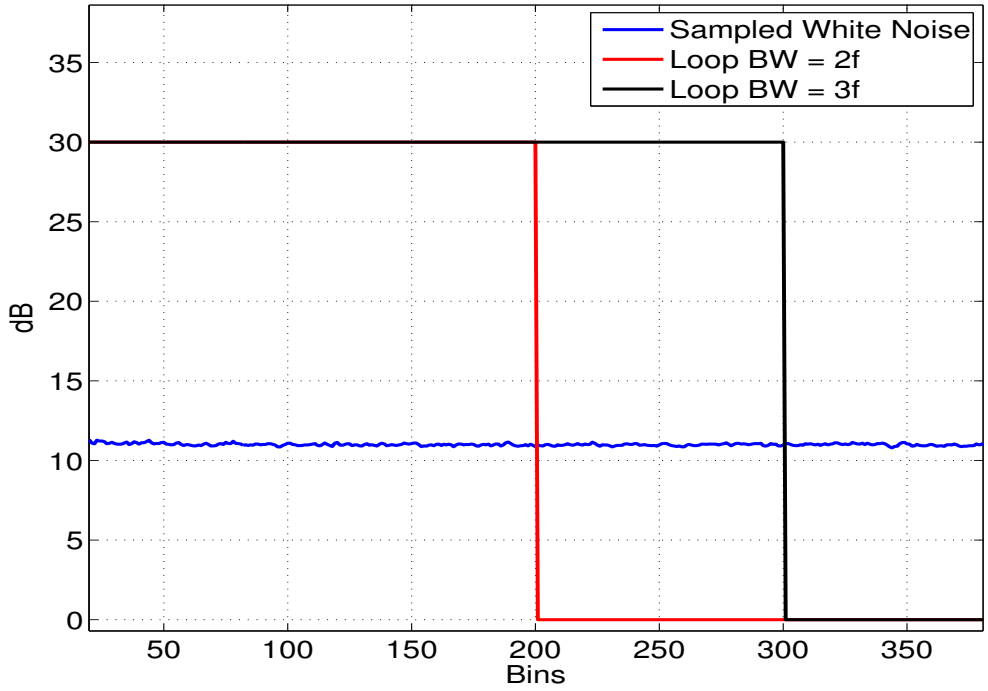


Figure 3.9: Calibration loop response and white noise

As given in the Fig. 3.10 , if we change the loop bandwidth from $10MHz$ to $124KHz$, the DC value of thermal noise (assuming flat frequency spectrum) should go down by $10log(\frac{10^7}{124*10^3}) = 19dB$. Because of sampling, the white noise spectrum is not flat throughout the spectrum as assumed and thus the actual gain is 17 dB. The effect of loop filtering on the flicker noise is shown in Fig. 3.11. As shown in Fig. 3.12 , the loop bandwidth is kept to 100KHz with a phase margin of 90 deg. For all simulations, the thermal noise is taken as bandlimited with bandwidth around 20 times that of the signal bandwidth.

### 3.2.4 Noise Optimization

Thermal noise of the bias circuit is the most dominant component of the total thermal noise because it gets multiplied by $g_m$ of N cells (where N is number of the current cell). So minimization of the total current in the bias circuit and the

User: ee04b066 Date: Sep 2, 2008 Time: 2:46:56 PM IST

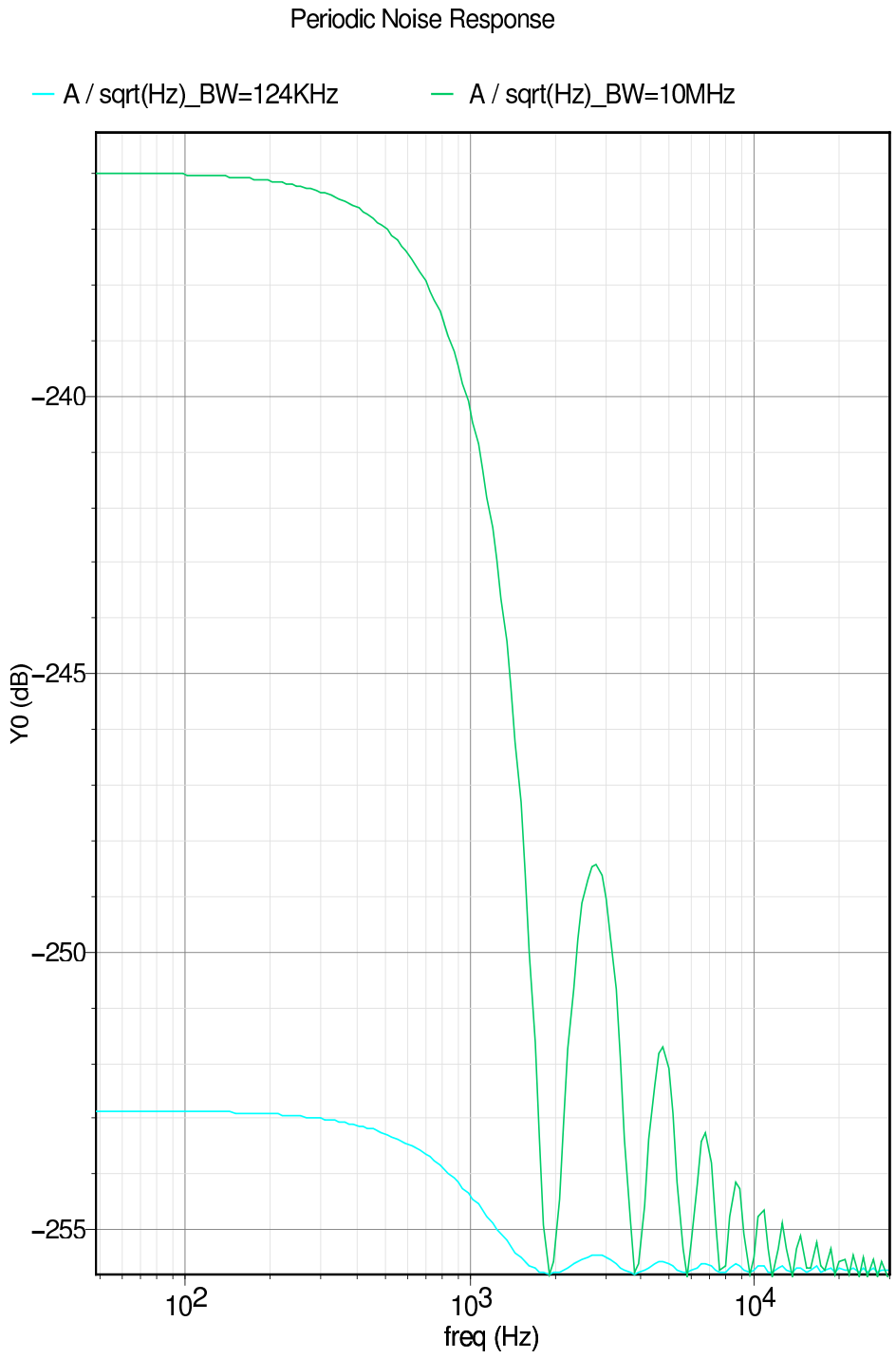


Figure 3.10: Effect of loop bandwidth on the thermal noise

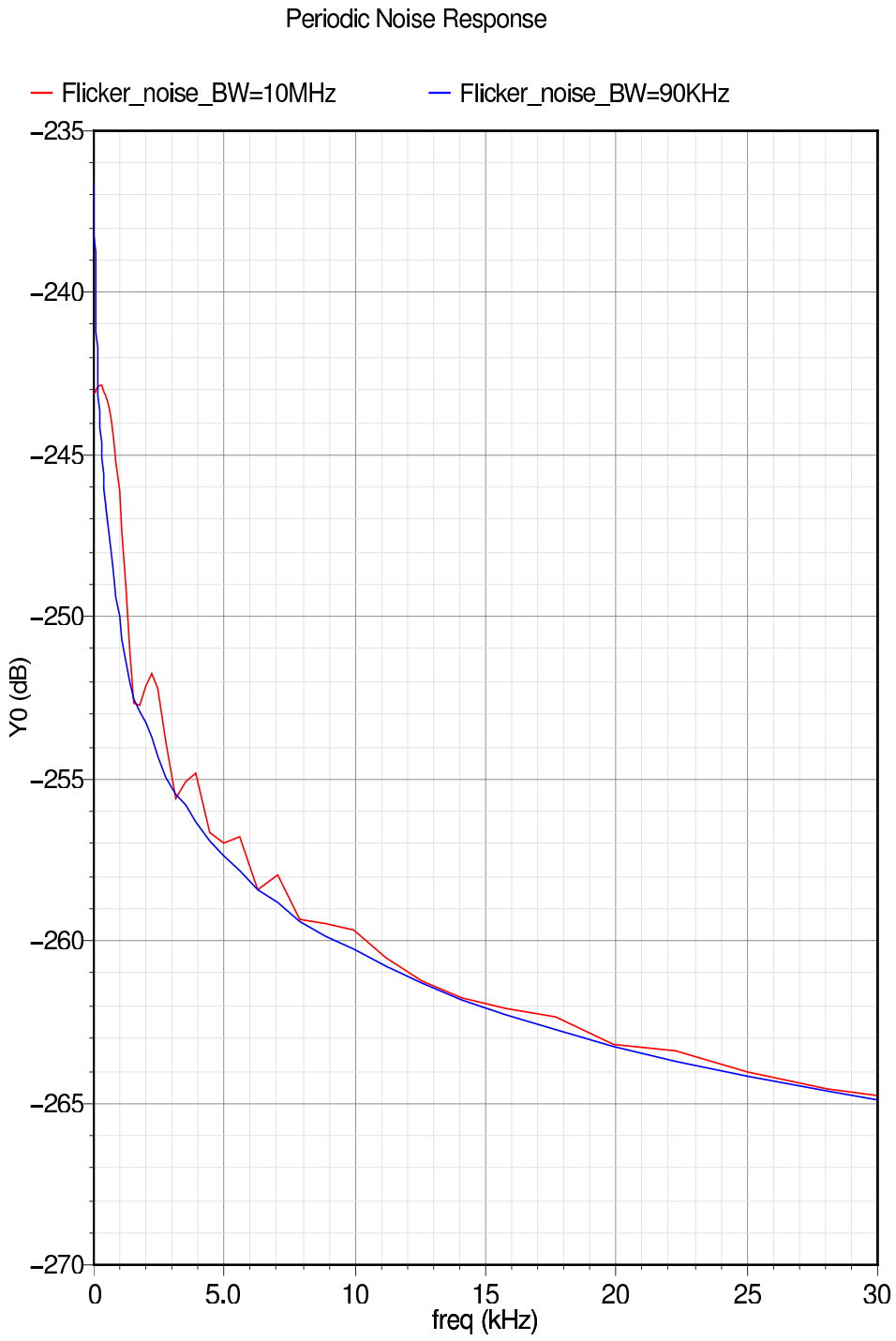


Figure 3.11: Effect of loop bandwidth on the flicker noise

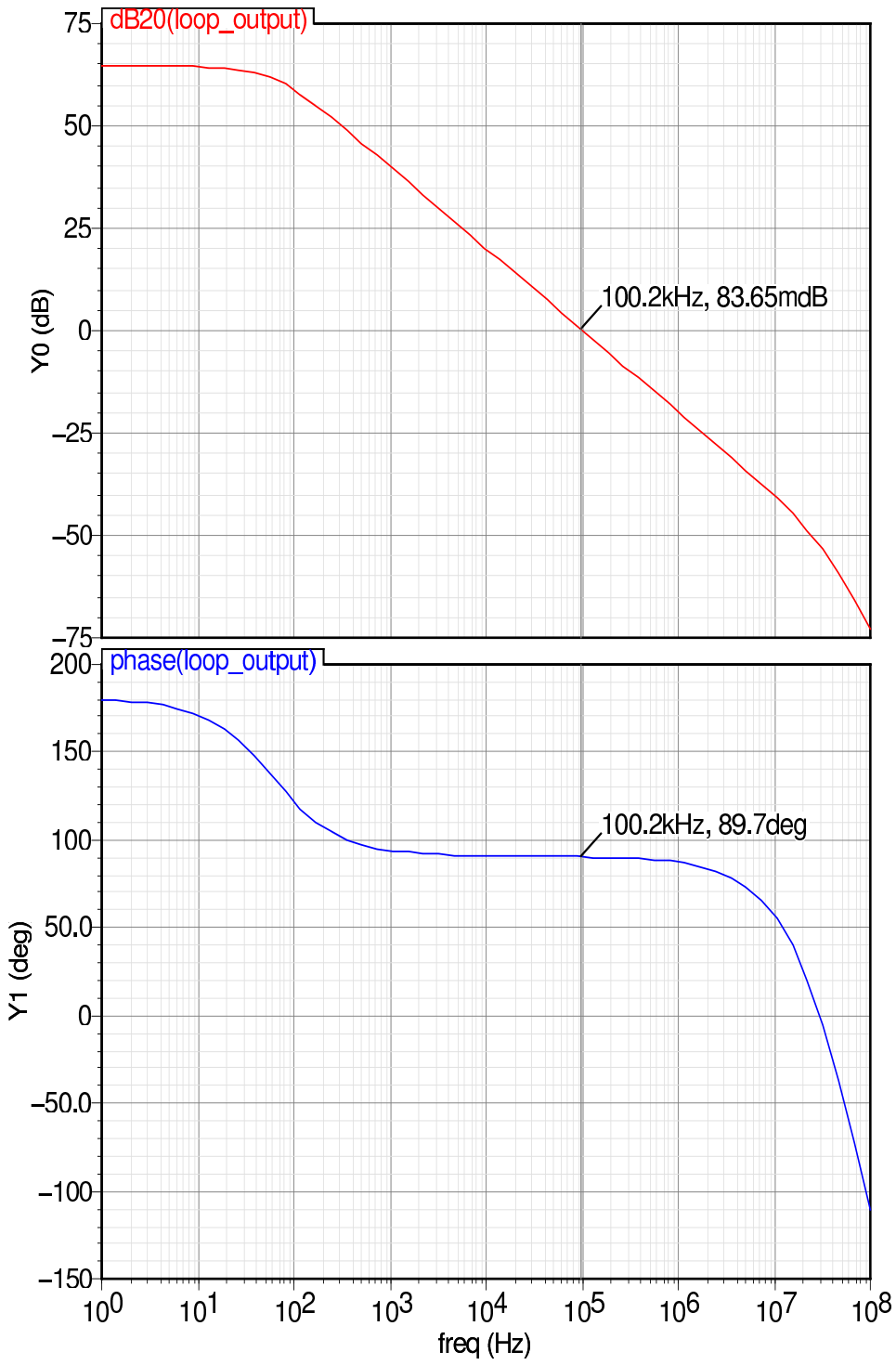


Figure 3.12: Loop gain of the calibration loop

DAC cell, with a specified total thermal noise value, is done here. Fig. 3.13 shows the main noise sources of the DAC current cell and the bias circuit.

Assuming that a noiseless reference current source is provided, the main contributors to the output noise are, $M_2$, $M_3$ and $M_4$ whose noise gets multiplied by the transconductance of N cells of the pMOS current source $M_1$ and the nMOS current source $M_0$. Then, the current noise will be converted to the noise voltage using the opamp and resistance R. The noise of R also depends on the current in the current cell as $2^{16} \times I_{lsb} \times R = 0.75V$.

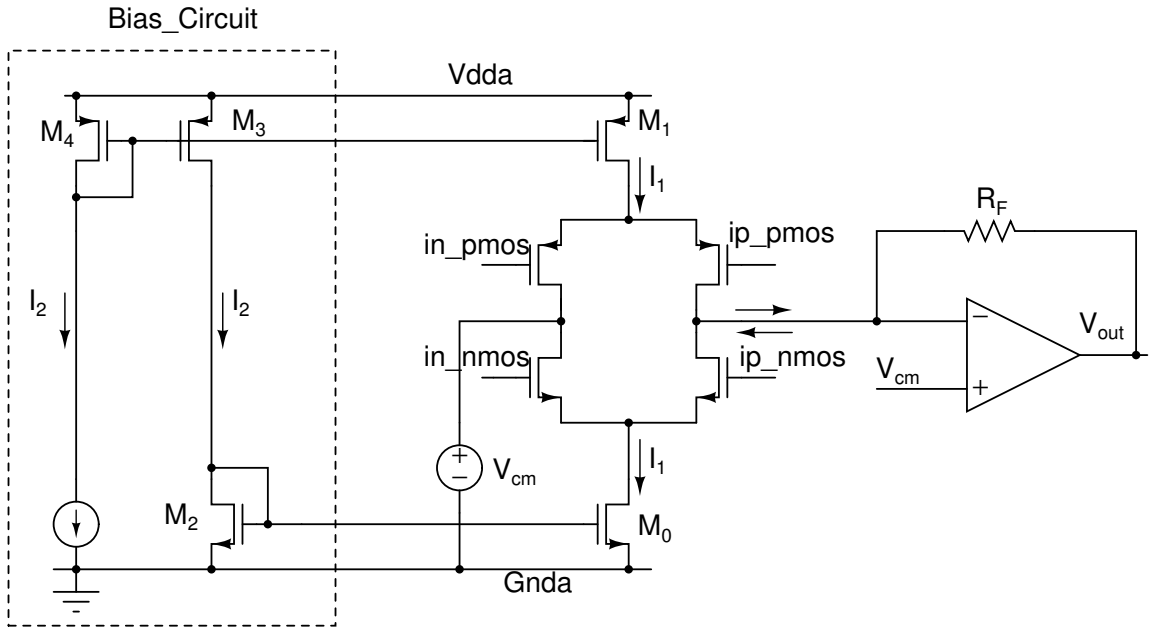


Figure 3.13: Generic DAC architecture

As seen in Fig. 3.13, the noise is maximum when all the nMOS current sources are ON, because at this instance, $M_2$ and $M_3$ are also contributing to the output noise. While in the case when only pMOS current sources are ON, the noise of $M_2$ and $M_3$ will not contribute to the output.

Assuming same $V_{GS} - V_{TH}$ for both pMOS and nMOS, the transconductance of the current source transistors are given by, $g_{m2} = g_{m3} = g_{m4} = g_{m0}\frac{I_2}{I_1}$.

The total thermal noise of the circuit at the output is given by Eqn. 3.11.

Using the condition for output swing given in Eqn. 3.12, we get Eqn. 3.13

$$S_{th} = 4kTR \times BW + \frac{8}{3}kTR^2[g_{m0} + (g_{m2} + g_{m3} + g_{m4})\frac{I_1}{I_2}^2] \times BW \quad (3.11)$$

$$S_{th} = 4kTR \times BW[1 + \frac{2}{3}R(g_{m0} + (g_{m2} + g_{m3} + g_{m4})\frac{I_1}{I_2}^2)]$$

$$IR = V_s \quad (3.12)$$

$$S_{th} \propto \frac{1}{I_1}[1 + \frac{4V_s}{3V_{GST}}(1 + 3\frac{I_1}{I_2})]$$

$$S_{th} \propto \frac{1}{I_1}(1 + 2.22\frac{I_1}{I_2}) \quad (3.13)$$

$$I_2 = \frac{2.22I_1}{(\frac{SI_1}{C} - 1)} \quad (3.14)$$

$$I_{total} = I_1 + 2I_2 \quad (3.15)$$

$$\frac{\partial I_{total}}{\partial I_1} = \frac{\partial(I_1 + 2I_2)}{\partial I_1}$$

$$I_2 = 1.05I_1 \quad (3.16)$$

Where, C is a constant. The optimization adjusts the value of $I_2$ to minimize the total current for a given noise specification. The solution to the optimization is given in Eqn. 3.16.

# CHAPTER 4

# DAC Architecture

The current steering D/A converter architecture is presented in this chapter. The architecture consists of pMOS and nMOS differential current sources. The differential current output is converted to a single ended voltage signal using an I-V converter.

## 4.1 MOSFET Operation

When used as a current source, a MOSFET can operate in the following modes (Ref. [5]):

**Subthreshold region::** Ideally when $V_{GS} < V_{TH}$, where $V_{TH}$ is the threshold voltage of the device, the transistor is turned off and there is no conduction between the drain and the source. Practically, there is a weak inversion current present called, the subthreshold leakage current given by Eqn. 4.1.

$$I_D = I_{D0} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \tag{4.1}$$

Where $I_{D0}$ is the current at $V_{GS} = V_{TH}$, the slope factor $n = 1 + \frac{C_D}{C_{OX'}}$, $C_D$ is the capacitance of the depletion layer and $C_{OX'}$ is the capacitance of the oxide layer.

**Triode mode or Linear region::** When $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$, the transistor is turned ON, the current flows between the drain and the source given by Eqn 4.2

$$I_D = \mu_n C_{OX} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \tag{4.2}$$

Where $\mu_n$ is the effective charge carrier mobility, $C_{OX}$ is the gate oxide capacitance per unit area, W is the gate width and L is the gate length.

**Saturation region::** When $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GS} - V_{TH})$, the transistor is in the strong inversion region. The current, including the effect of the channel length modulation, is given by Eqn. 4.3.

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{4.3}$$

Where $\lambda$ is the channel length modulation parameter.

Eqn. 4.3 shows minimum dependence on $V_{DS}$ as the value of $\lambda$ is very small($\approx$ 0.1), while in subthreshold, current is exponentially depended on $V_{GS}$ and slight mismatch can cause a large difference in the current. So we use a MOS device in saturation region with nearly identical $V_{DS}$ for current mirroring.

## 4.2 Analog Architecture

### 4.2.1 Cascode

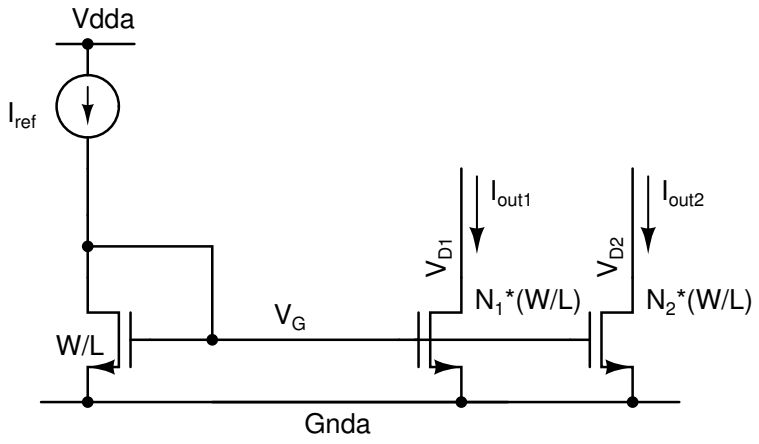


Figure 4.1: Current Mirror

A simple current mirror is shown in Fig. 4.1. Ideally, since all the three devices have same $V_{GS} - V_{TH}$ $(= V_{GST})$, they will have currents $I_{out1} = N_1 \times I_{ref}$ and

$I_{out2} = N_2 \times I_{ref}$ . But, because of the channel length modulation, the value of $I_{out1}$ and $I_{out2}$ will not be directly multiplied by their size ratio to the main current source $I_{ref}$.

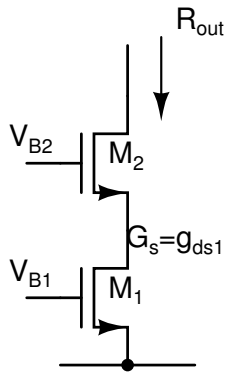


Figure 4.2: Cascoding of MOSFETs

Cascoding is used to solve the problem of different $V_{DS}$. When a MOS is cascoded with another MOS biased in the saturation region, its output impedance increases. There could be a difference between the output node voltage and the calibrating node voltage. So, when current is switched from the output node to the calibration node, because of the change in $V_{DS}$, the current source value will change. To solve this problem, the cascoding devices are sized in such a way that $V_{DS}$ of all the nMOS current mirrors are almost the same when the current is switched from output node to calibration node. Similar argument holds true for the pMOS current sources. Cascoded device structure is shown in Fig. 4.3.

$$\begin{aligned} R_{out} &= \frac{g_{m2}}{g_{ds2} \times g_{ds1}} + \frac{1}{g_{ds2}} + \frac{1}{g_{ds1}} \\ R_{out} &\approx \frac{g_{m2}}{g_{ds2} \times g_{ds1}} \end{aligned} \tag{4.4}$$

After cascoding, the increased input impedance $R_{out}$ also shields the current source $V_{DS}$ from the switching impulses and the clock feed through present at the switches. The third cascode is used to further increase its susceptibility from switching, which is also used as a switch.

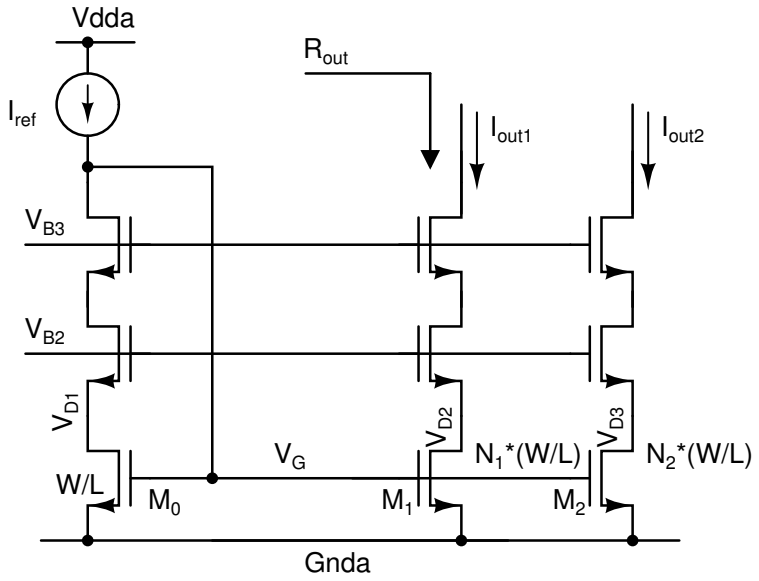


Figure 4.3: Cascoding of Current mirrors

Table 4.1: Device Sizes for the MSB cell

| Device | Size | Device | Size |
|---|---|---|---|
| $M_{0P}$ | $\frac{6*0.5\mu m}{10\mu m}$ | $M_{0N}$ | $\frac{3*0.25\mu m}{20\mu m}$ |
| $M_{1P}$ | $\frac{2*0.5\mu m}{10\mu m}$ | $M_{1N}$ | $\frac{0.25\mu m}{20\mu m}$ |
| $M_{2P}$ | $\frac{8*0.24\mu m}{0.18\mu m}$ | $M_{2N}$ | $\frac{4*1\mu m}{0.18\mu m}$ |
| $M_{30P}$, $M_{31P}$ | $\frac{4*0.24\mu m}{0.18\mu m}$ | $M_{30N}$, $M_{31N}$ | $\frac{2*1\mu m}{0.24\mu m}$ |
| $M_{40P}$, $M_{41P}$, $M_{42P}$, $M_{43P}$ | $\frac{2*0.24\mu m}{0.18\mu m}$ | $M_{40N}$, $M_{41N}$ , $M_{42N}$, $M_{43N}$ | $\frac{2*0.24\mu m}{0.24\mu m}$ |

### 4.2.2 MSB current cell

As discussed in Section 2.2.1, differential architecture is chosen for the D/A converter. The converter has a total of 63 MSB cells. The MSB current cell circuit diagram is shown in Fig. 4.4. The device sizes are given in the Table. 4.1. The capacitor value is 200fF.

BiascalP is the output of the calibrating op-amp used. In the normal working mode, clk signal is low keeping the switch $SW_0$ open. The current flows to one of the outputs accordingly, depending on the input signal.

When a cell is calibrating, its respective clk signal is high, keeping the switch $SW_0$ close. The current of the pMOS current source is diverted to the output node VcalP through various switches. Here this current is compared with a reference

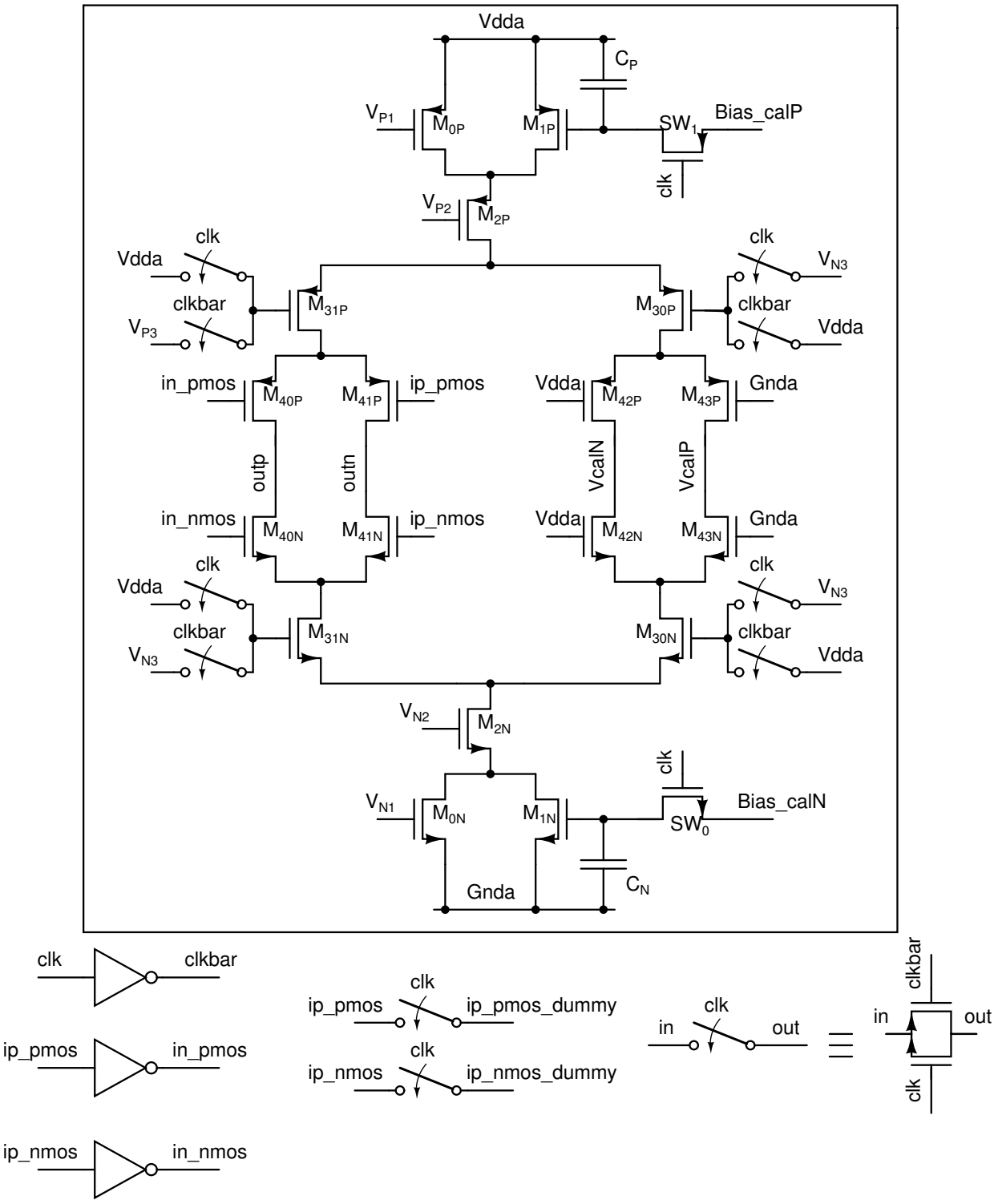


Figure 4.4: MSB current Cell

current source and an opamp is used in negative feedback loop to change the gate voltage of the device $M_{1P}$. During calibration, charge is stored in the capacitor $C_P$, which will maintain the gate voltage when the switch is open. The scheme described above is same for the nMOS current sources also.

A dummy MSB current cell is used to make sure of the continuous operation of the converter. The dummy MSB cell is shown in Fig. 4.5

Cells to be calibrated apart from MSB cells are a dummy cell, 2 LSB cells and a reference current cell. The sequence for calibration is, the reference cell gets calibrated in clk[0], LSB cells in clk[1] and clk[2] and the dummy cell in clk[3]. When any of the above cells are getting calibrated, dummy cell current is terminated using the logic shown in Fig. 4.5.

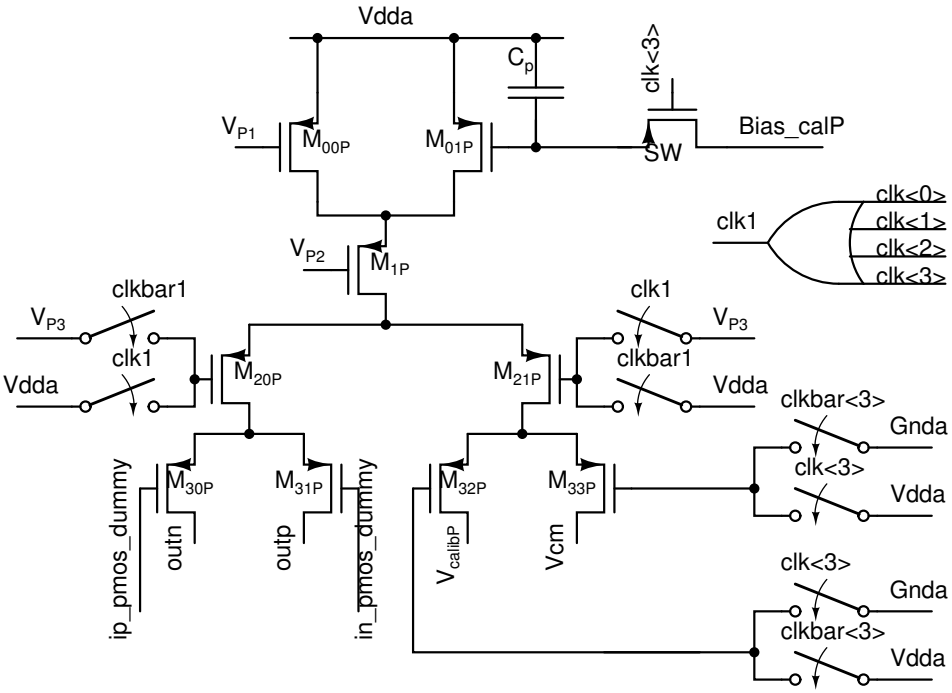


Figure 4.5: MSB dummy current cell

### 4.2.3 LSB current cell

The 10 bit LSB is further divided into 6 bit USB and 4 bit LSB (Ref. [1]). The circuit diagram for the LSB current cell is shown in Fig. 4.6. The remaining 10 bit DAC is implemented using the current divider (as shown in Fig. 4.7) , which is essentially an array of switches with appropriate sizes which divides the current and differential switches to route the current to the output or to the termination. Long transistors have been chosen for the current divider to ensure good matching among LSB divider, as the LSB current can not be calibrated in this case.

No separate dummy is used for the LSB cell to avoid the wiring complexity in layout. Unlike the MSB dummy cell, the dummy for LSB cell is incorporated within the cell. Again, the switching scheme is shown in the Fig. 4.6.

The switch array is made of 63 switches to account for 6 bit USB and 15 switches for the 4 bit LSB. One extra switch is used to terminate the remaining LSB current.

### 4.2.4 Bias Circuit

The bias circuit is shown in Fig. 4.8. Because of process variations, the value of the resistance used to convert the current into the voltage can vary, which results in different output swings at different process corners. At some corner, because of the large swing, signal can get clipped because of the opamp limitations thus giving a huge distortion. To avoid this situation, a constant IR biasing circuit is used. With process variations, the biasing resistor will also vary and give an appropriate current to maintain a constant output swing. The two resistors are placed next to each other in layout to improve matching.

The circuit also exhibits a stable operating point with all zero branch currents. To bring it to the desired operating point, a start-up circuit is used. Start-up circuit is shown in Fig. 4.8. As shown in the figure, if the bias $V_{bP1}$ is stuck to Vdda, when the circuit starts, $M_{S2P}$ will switch on and start pulling its drain

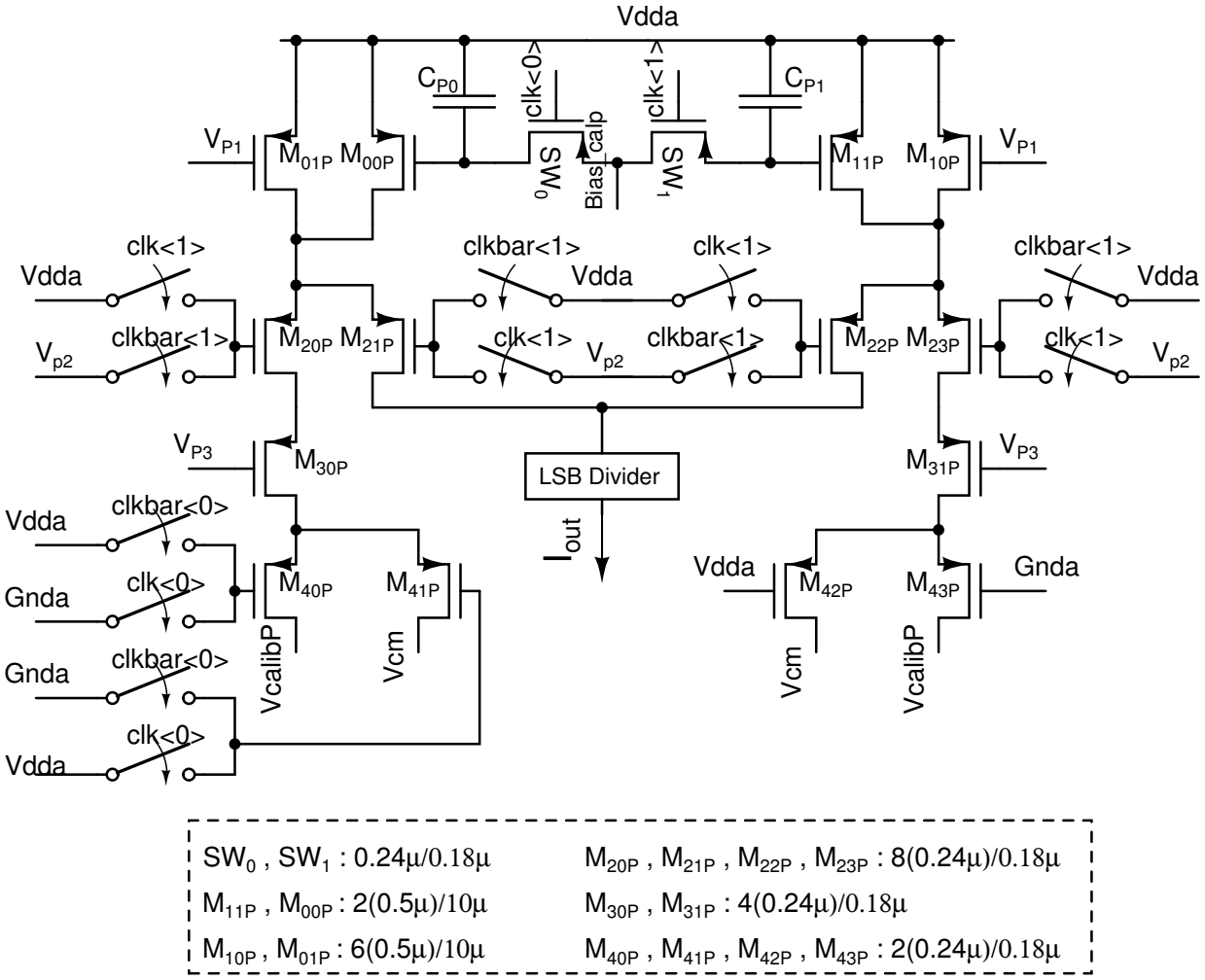


Figure 4.6: LSB current cell

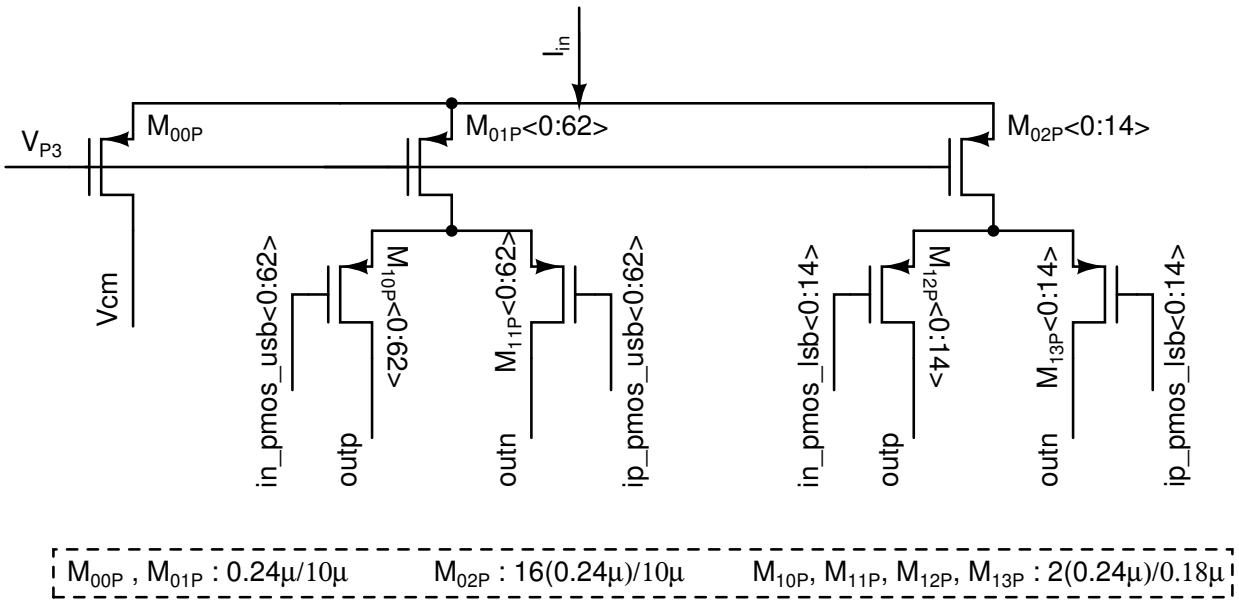


Figure 4.7: LSB divider cell

voltage down as $M_{S0P}$ is in cut off state. This will trigger the $M_{S1P}$ device, which will start pulling the current from node $V_{bP1}$ and switch on $M_{S0P}$. This negative feedback loop will bring it closer to the correct operating point and the actual bias circuit will fix its value correctly.

The bias circuit also suffers from the problem of switching feed through. Because of the coupling capacitance between the drain and the gate of MOSFET, the bias voltages experience switching glitches. As shown in Fig. 4.9, the effect of switching glitches are maximum on the third cascode bias, which are closer to the switching nodes compared to the main current source bias.

Voltage buffers can not be used here, to avoid the coupling between switching nodes and bias voltages because mismatch among buffers will also pose a big problem for calibration. Because of very small currents, maintaining the exact bias for the current sources using buffers is difficult. To avoid this situation, large on-chip bypass capacitors of value $\sim$40 pF are used to bypass the glitches to Vdda for pMOS and Gnda for nMOS accordingly. Apart from that, an another on-chip capacitor of value $\sim$150 pF is used to bypass glitches between Vdda and Gnda.

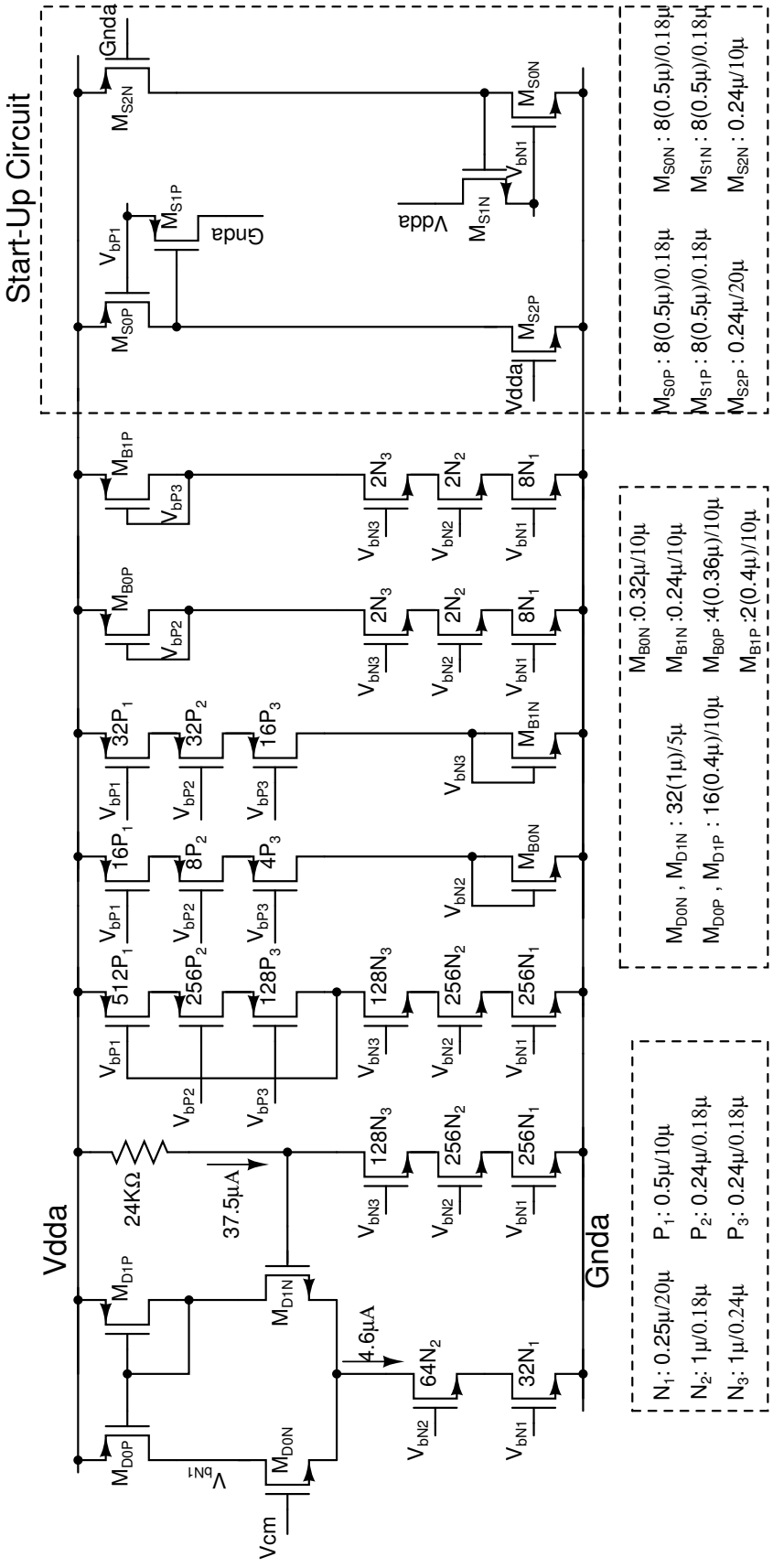


Figure 4.8: Bias circuit

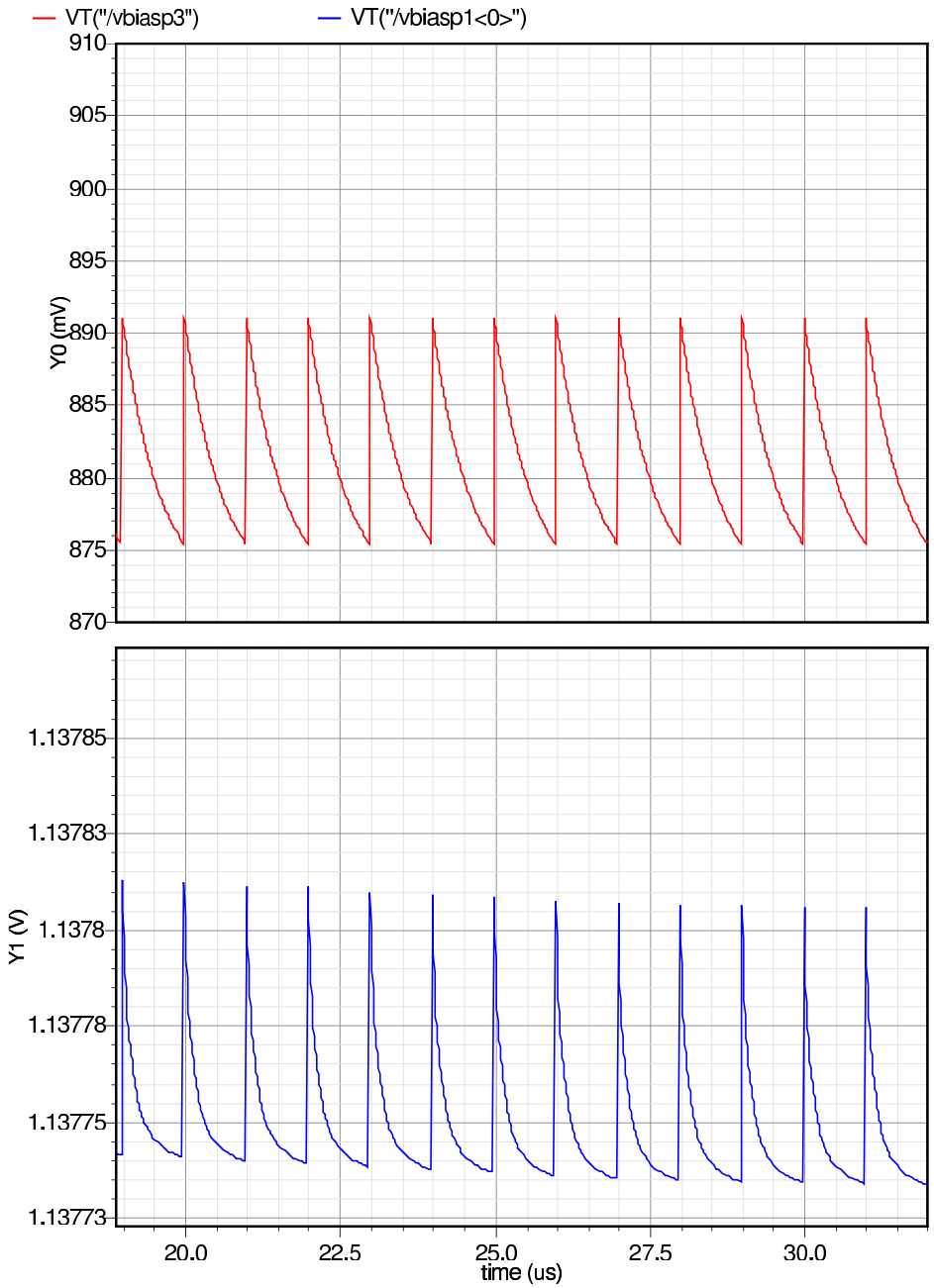


Figure 4.9: Switching Glitches on bias voltage of [TOP:the third cascode] [BOTTOM:the Current source]

### 4.2.5 Switching Schemes

The input thermometer coded data can be used in many combinations to switch the current sources and get the desired performance of a 16 bit DAC. Here, we have discussed two possibilities which are implemented in the converter design.

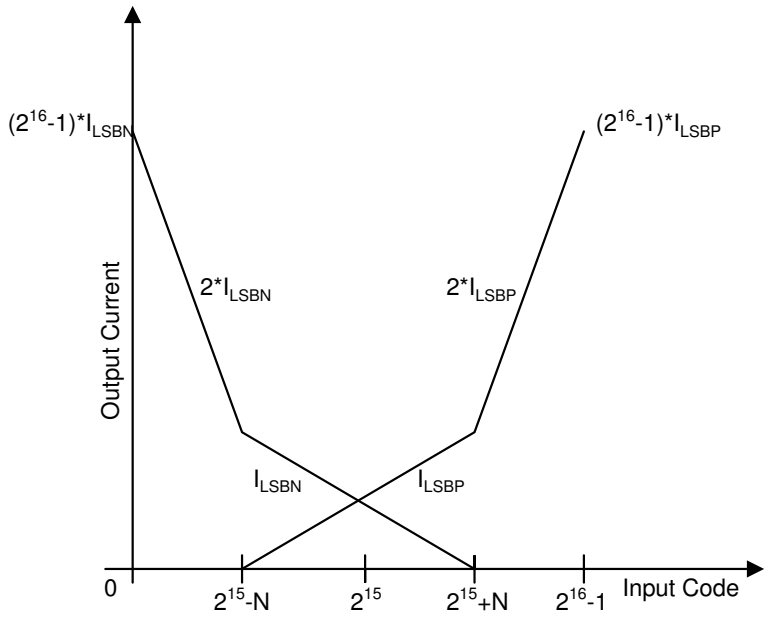


Figure 4.10: Input Code Switching Curve

In general, the switching of the input differential pair is done as shown in the Fig. 4.10. As Fig. 4.10 shows, when the input code is $< 2^{15} - N$, the pMOS sources are used to provide the -ve output voltage swing and when the input code is $> 2^{15} + N$, the nMOS current sources are used to provide the +ve output voltage swing. When the input code is in between $< 2^{15} - N$ and $> 2^{15} + N$, both pMOS and nMOS current sources are switches in a complementary way. If K is the input code, the value of the output current is calculated to simulate the behavior of the DAC with different switching schemes.

**When** $K < 2^{15} - N$

$$I_{out} = -I_{lsbN}(2^{16} - 1) + K(2I_{lsbN}) \tag{4.5}$$

**When** $(2^{15} - N) < K < (2^{15} + N)$

$$\begin{aligned} I_{out} &= -I_{lsbN}(2^{16} - 1) + (2^{15} - 1) \times 2I_{lsbN} \\ &+ (K - 2^{15} + N)(I_{lsbP} + I_{lsbN}) \end{aligned} \tag{4.6}$$

**When** $K > 2^{15} + N$

$$\begin{aligned} I_{out} &= -I_{lsbN}(2^{16} - 1) + (2^{15} - 1) \times 2I_{lsbN} \\ &+ 2N \times (I_{lsbP} + I_{lsbN}) + (K - 2^{15} - N) \times 2I_{lsbP} \end{aligned} \tag{4.7}$$

Based on the above equations, the slope of the DAC gain (normalized w.r.t. NMOS current source gain) is given by:

**When** $K < 2^{15} - N$

$$slope = 1 \tag{4.8}$$

**When** $(2^{15} - N) < K < (2^{15} + N)$

$$slope = 1 + [\frac{(K - 2^{15} + N)}{2N}]\frac{x}{I_{lsbN}} \tag{4.9}$$

**When** $K > 2^{15} + N$

$$slope = 1 + \frac{x}{I_{lsbN}} \tag{4.10}$$

Where $x = I_{lsbN} - I_{lsbP}$. Here N can be varied from 0 to $2^{15}$ depending on the system requirements. In our case we have used the extreme cases of N = 0 and N = $2^{15}$.

First possibility is the complementary switching scheme, when $N = 2^{15}$, in which pMOS and nMOS are switched in a complementary way. In this case, at mid-code, both the current sources provide equal currents which cancel out each

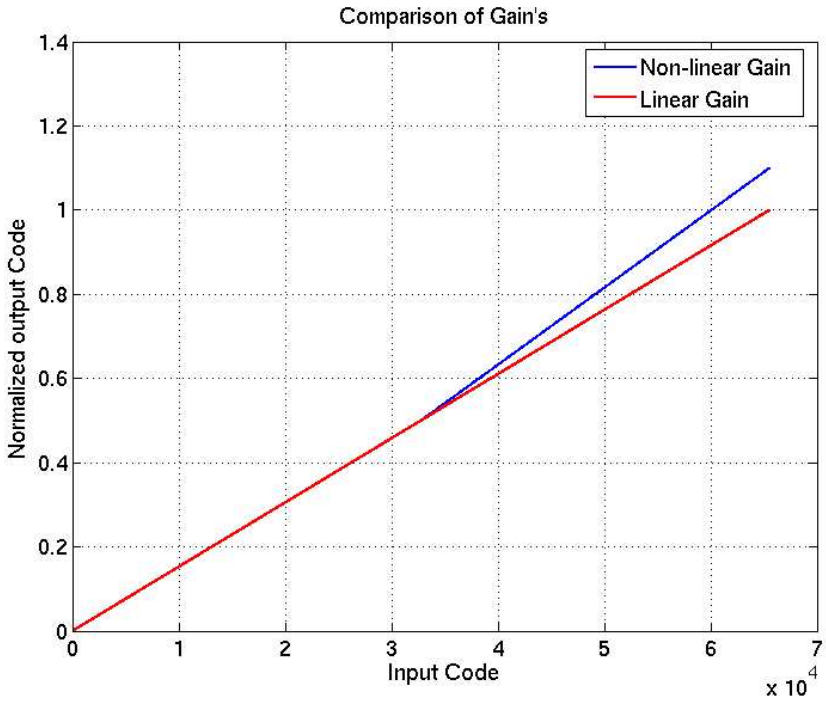


Figure 4.11: Gain curve due to different switching techniques

other. This configuration is good in terms of distortion because, the mismatch between the nMOS and the pMOS LSB currents will have no effect, as the sum of both the currents is constant for the entire input code range. But this has the problem of higher noise at the mid code. Although, there is no current flowing to the output at the mid-code, noise of the current sources will be present at the output.

In the second possibility, when $N = 0$, the pMOS gives the output swing below the common mode voltage and the nMOS gives the output swing above the common mode voltage. At the mid code, the current is zero at the output due to both the current sources. This is used when the system has very stringent idle channel noise specifications. Since both the pMOS and the nMOS current sources are disconnected from the I-V converter, the noise due to current source is ideally 0. But this switching scheme can give rise to a large distortion. If the value of the pMOS and the nMOS LSB currents are not same, the input code versus the output code curve is not smooth near the mid-code, as shown in Fig. 4.11 in blue line.

The DAC output FFT is shown in Fig. 4.12. We can see that in the case of modified switching (with $N = 0$), the distortion is more compared to the comlementary switching case (with $N = 2^{15}$). The second harmonic tone is at -104.1 dB in the case of modified switching while it is at -105.5 dB in the case of normal switching.

## 4.3 Digital Engine

The D/A converter is implemented in a thermometer fashion, while the data is supplied in a binary fashion. To make the data compatible to DAC architecture, a binary-to-thermometer code converter is used. The DAC also needs a calibration clock with a duty cycle of $1/N$, where N is the number of cells to be calibrated. Both the circuit architectures are explained in the following sections.

### 4.3.1 Binary to Thermometer Code Conversion

The technique for binary-to-thermometer conversion is adopted from Ref. [6]. N bits are converted to the thermometer code in (N-1) cascading stages. First, two LSB bits are converted to the thermometer code using an array of gates as shown in Fig. 4.13. Then the output of this decoder is fed to a second array of gates with another LSB input bit and so on. The circuit used for the conversion differs when, number of input bits are even (Fig. 4.14) and odd (Fig. 4.15).

As presented in Section. 4.2.5, two types of switching schemes (modified switching and normal switching) are implemented using an Algo. 1:

Where, **in** is the 16 bit binary input signal. Major chunk of the digital power is consumed by the binary to thermometer code converter because of its large size and fast switching. Driving the large wiring capacitance adds to the problem of power consumption. To reduce the power consumption, the circuit is divided in two parts:

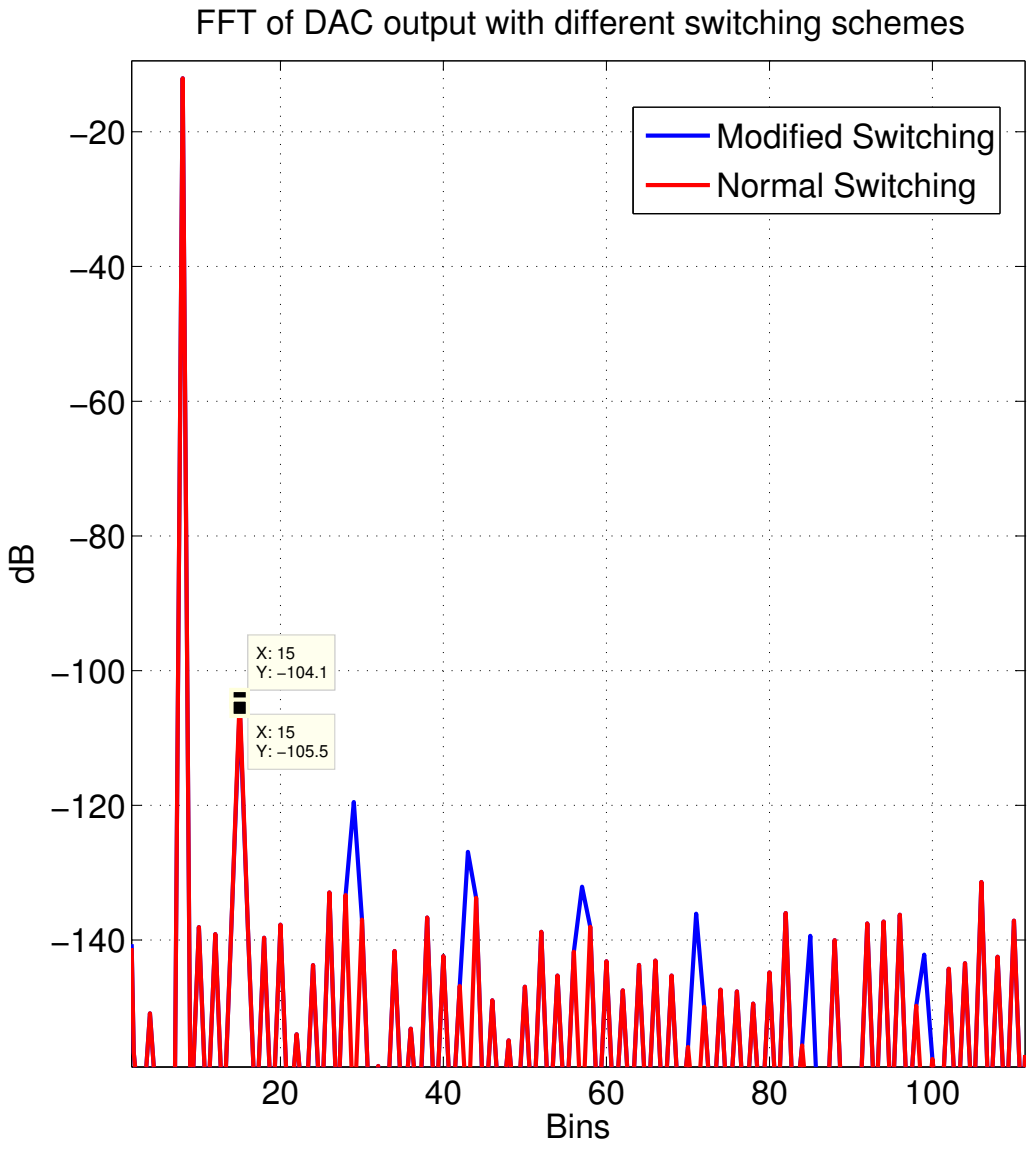


Figure 4.12: Distortion due to different switching techniques. 2nd harmonic at a) -104.1 dB for modified switching and b) -105.5 dB for complementary switching

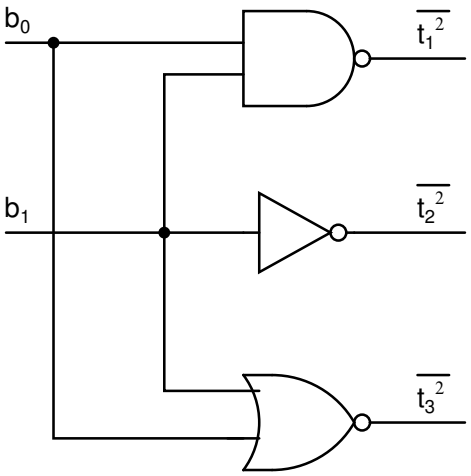


Figure 4.13: Binary to Thermometer converter for 2-bit input

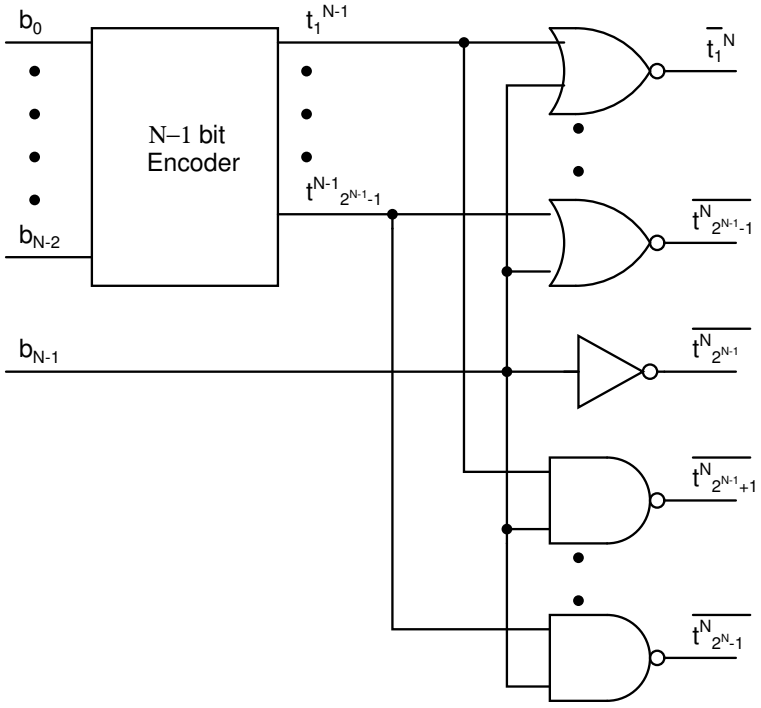


Figure 4.14: Binary to Thermometer converter for N-bit input where N is even

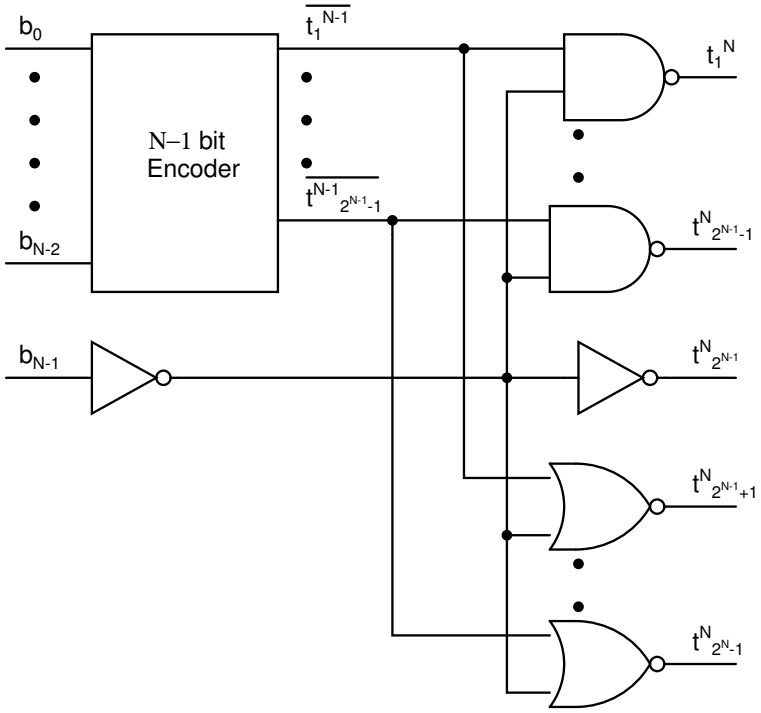


Figure 4.15: Binary to Thermometer converter for N-bit input where N is odd

**Algorithm 1** Switching Algorithm

```
if mode then
  if in(15) then
    Switch OFF all the nMOS current sources
    Use input to switch the pMOS current sources
  else
    Switch OFF all the pMOS current sources
    Use input to switch the nMOS current sources
  end if
else
  Do normal switching
end if
```

- Binary to thermometer converter for MSB.
- Binary to thermometer converter for USB + LSB.

After dividing the circuit, it is placed close to the MSB and the LSB arrays to minimize the wiring capacitance. Using this technique, with OSR of 128X, the power consumed by binary to thermometer converter is brought down from $\approx 1mW$ to $\approx 600\mu W$.

### 4.3.2 Clock Generator

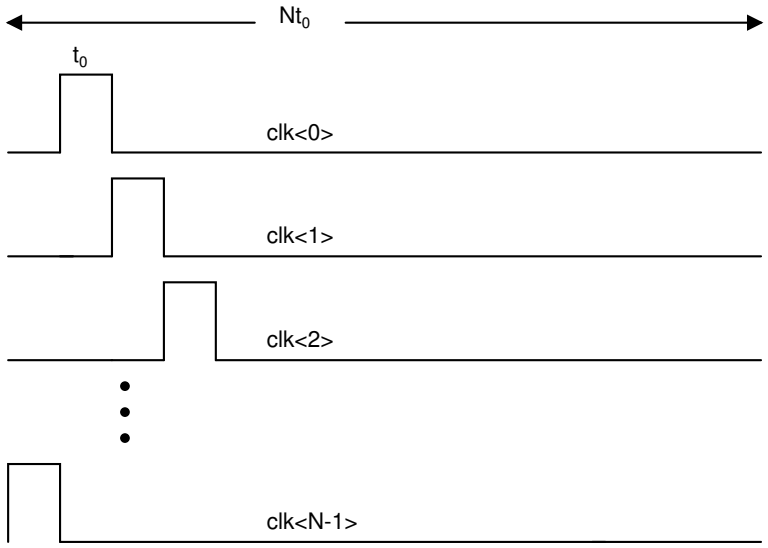


Figure 4.16: Different Calibration Clocks

To calibrate the current cells, we need N clock signals with $1/N$ duty cycle as shown in Fig. 4.16. The clock generator can be programmed for different calibration periods. To do so, the circuit takes a clock signal, which is used to sample the input data, and a 3 bit signal which determines the clock division ratio, as the inputs. Using this we can divide the input clock signal by a factor of $2^1$ to $2^8$. Circuit for the programmable clock divider is shown in Fig. 4.17. Most of the power consumed by the clock generator is used in the large buffers at the output. The power consumed by the clock generator is ~400 $\mu$W, when the input clock signal is at 128X OSR and a division ratio of 16 is used.

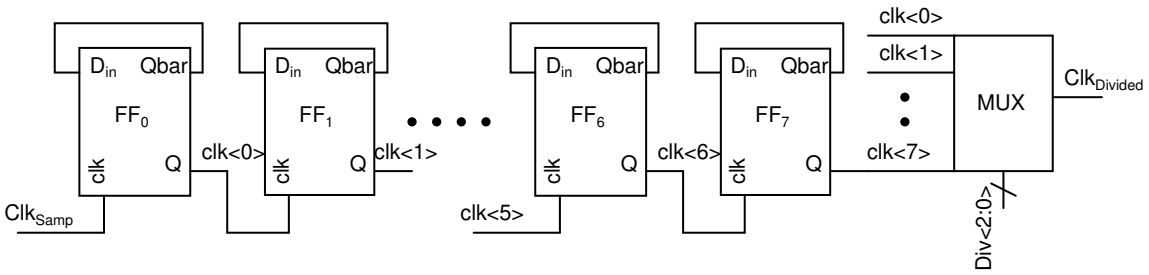


Figure 4.17: Programmable Clock Divider

Circuit for the calibration clock generator consists of N flip-flops connected in series with some combinational circuit to ensure that only one clock is high at a time. All the Flip-Flops are clocked using the divided clock signal. The circuit diagram used to generate the clock signals is shown in Fig. 4.18.

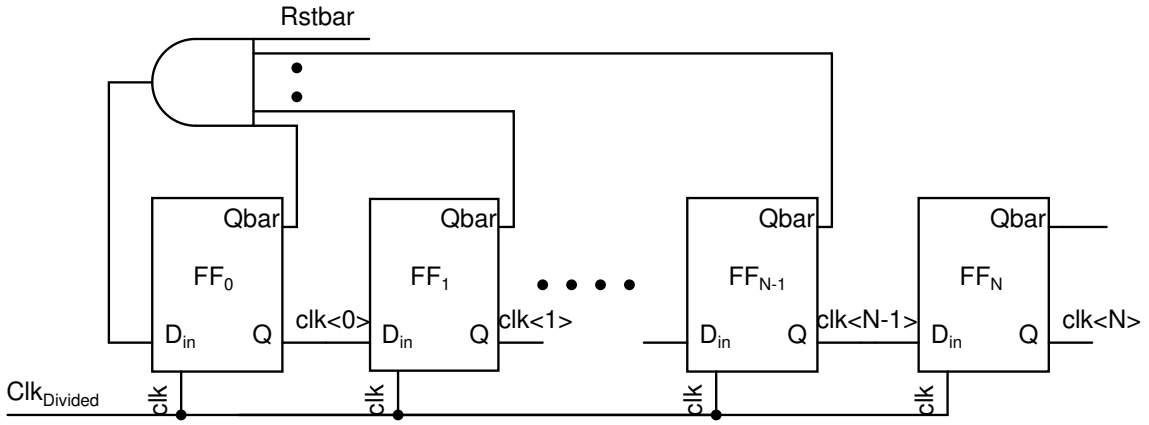


Figure 4.18: Calibration Clock Generator

The clock is pseudo randomized to avoid the harmonic tones because of the coupling between adjacent running wires. The algorithm used for randomizing the clocks is shown in Algo. 2:

Where **Clkdiv** is the clock signal generated using the programmable divider, **Clkin** is clock signals generated by the clock generator, **Clkout** is the randomized output, **Flag** is an internal signal used to randomize clocks and N is the number of cells to be calibrated (67 in this case). In this algorithm, when the **Flag** signal is low, the Clkin signals are connected directly to the Clkout signals (e.g. Clkin[0] is

**Algorithm 2** Algorithm for pseudo Randomization of Clocks

@posedge(Clkdiv)
**if** Reset **then**
  $Flag \leftarrow 0$
  $Count \leftarrow 0$
**else if** Count == N **then**
  $Count \leftarrow 0$
  $Flag \leftarrow Flagbar$
**else**
  $Count \leftarrow Count + 1$
**end if**
**if** Flag **then**
  $Clkout[0 : N-1] \leftarrow Clkin[0 : N-1]$
**else**
  $Clkout[0 : N-1] \leftarrow Clkin[N-1 : 0]$
**end if**

connected to Clkout[0] and so on) and when the **Flag** is high, the Clkin signals are reversed and then connected to Clkout (e.g. Clkin[0] is connected to Clkout[N-1], Clkin[1] is connected to Clkout[N-2] and so on). A decimal counter, counting upto N is used for randomizing the clocks. Thus, the output of the clock generator is periodic with period of 2N.

# CHAPTER 5

# Calibration Technique

As the MOSFETs are becoming smaller, during chip manufacturing, random process variations affects the transistor dimensions. This results in performance variations, threshold gradient, current factor gradient etc. However, to get acceptable matching, the device dimensions should be very large, as explained in Section 5.1. Hence, a calibration technique is presented in this chapter to minimize the effect of the threshold gradient $\Delta V_{TH}$.

## 5.1 Mismatch Analysis

In the current steering DAC, the $V_{TH}$ mismatch is very crucial because the current is $\propto V_{GST}$ overdrive. A small mismatch in $V_{TH}$ can cause large differences in the current, which can produce large distortion. The $V_{TH}$ mismatch has been modelled as:

$$\sigma_{V_{TH}} = \frac{A_{V_T}}{\sqrt{WL}} + C_0 \tag{5.1}$$

Where W, L are dimensions of the device, $A_{V_T} = 4.787\ mV\mu m$, $C_0$=0.5382 mV for nMOS, while $A_{V_T} = 4.899\ mV\mu$m and $C_0$=0.1894 mV for pMOS (Ref. [2]).

The current factor mismatch($\beta$) has been modelled as a random variable with standard derivation as

$$\sigma_{\frac{\Delta I}{I}} = \frac{A_\beta}{\sqrt{WL}} \tag{5.2}$$

Where $A_\beta = 1.598\%\mu m$ Ref. [2] and W, L are the device dimensions. Using the above equations, the standard deviation of mismatch between two devices is found to be:

$$\sigma_{V_{TH}}(nMOS) = 1.61mV$$
$$\sigma_{V_{TH}}(pMOS) = 0.964mV$$

Even with the threshold mismatch, the current in different devices can be same using current mirroring, if their overdrive ($V_{GS} - V_{TH}$) is same. Which means that, the threshold mismatch can be nullified by changing the gate voltages of the current sources accordingly. This is realized using a calibration technique presented in this chapter.

## 5.2 Calibration

### 5.2.1 Idea

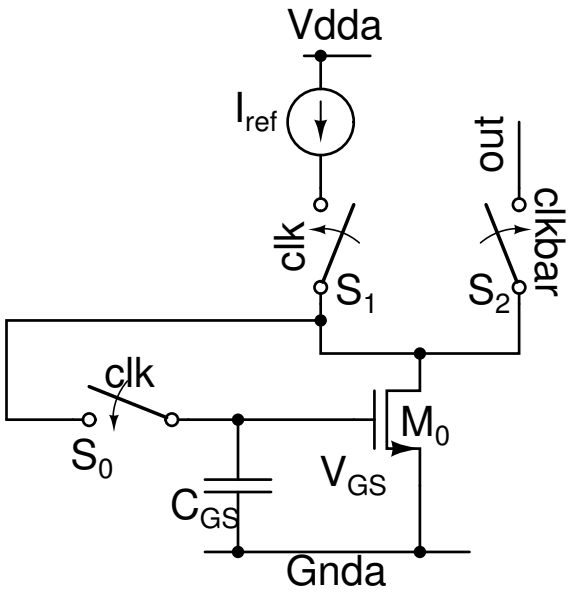


Figure 5.1: Calibration Principle

The calibration principle presented in this section was proposed in Ref [7]. Basic calibration circuit is shown in Fig. 5.1. When the switches $S_0$ and $S_1$ are closed, the reference current $I_{ref}$ flows into the transistor $M_0$, which is connected

in diode configuration. Because of the presence of negative feedback loop around the nMOS, charge is stored in the gate capacitance $C_{GS}$, maintaining the gate voltage at $V_{GS}$. When $S_2$ gets closed and the other switches get open, the charge is preserved on $C_{gs}$ and $I_{ref}$ current flows into $M_0$ from the output.

### 5.2.2 Imperfections

In practice, the calibration circuit suffers mainly because of two issues, charge injection and charge leakage. This affects the current flowing through the transistors, by changing its gate voltage $V_{GS}$. Both, the cause and the solution proposed in Ref. [7] are presented in this Section.

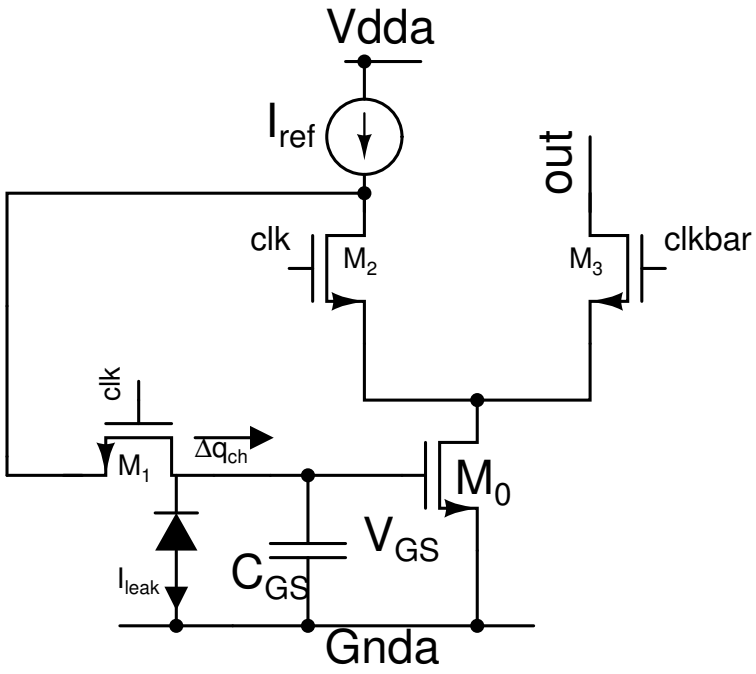


Figure 5.2: Calibration circuit issues

#### Charge Injection

A real calibration circuit is shown in Fig. 5.2. Here, all the switches are implemented using the nMOS device and $C_{gs}$ is the gate-source capacitance of $M_0$. When the switch $M_1$ is turned OFF, its channel charge is partly dumped on to

the gate capacitance of $M_0$ and hence, the charge on $C_{gs}$ decreases by an amount $\Delta q_{ch}$. The charge change implies a sudden change in $V_{GS}$ of $M_0$ given by Eqn. 5.3:

$$\Delta V_{GS,q} = \frac{\Delta q_{ch}}{C_{gs}} \tag{5.3}$$

The change in the gate voltage of $M_0$ affect the drain current $I_{DS}$. The change in the output current is given by Eqn. 5.4

$$I_{DS,q} = I_{ref} - g_m \frac{\Delta q_{ch}}{C_{gs}} \tag{5.4}$$

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \tag{5.5}$$

$$C_{gs} = \frac{2}{3} W L C_{ox} \tag{5.6}$$

Where $\mu$ = electron mobility and $C_{ox}$ = oxide capacitance per $\mu m^2$.

The difference between the current sources are of higher importance than the actual value of the current, as the former will give large distortion in the output. Hence, the difference in $\Delta q_{ch}$ due to the switches mismatch also affects the output spectrum. The switch mismatches are determined by the switch sizes. However, the switch sizes must be kept minimal to minimize $I_{leak}$. From Eqn. 5.4, it is noticed that if we increase the value of $C_{GS}$, effect of the switches mismatch and the charge injection will reduce.

### Charge Leakage

Another factor which governs the current of the MOS transistor is leakage of the charge stored in the gate capacitance. Although, switch $M_1$ is switched off, the reverse-biased diode between its source and the substrate is still present. The leakage current $I_{leak}$ of this diode decreases the charge on $C_{gs}$ continuously. The voltage on $C_{gs}$ as a function of time is given by Eqn. 5.7

$$V_{GS,leak}(t) = V_{GS}(0) - \frac{I_{leak}}{C_{gs}}t \tag{5.7}$$

$$I_{DS,leak}(t) = g_m V_{GS,leak}(t) = I_{ref} - g_m \frac{I_{leak}}{C_{gs}}t \tag{5.8}$$

So the combined effect of the charge injection and the charge leakage problem on $I_{DS}$ is given by Eqn. 5.9

$$I_{DS} = I_{ref} - g_m \frac{I_{leak}}{C_{gs}}t - g_m \frac{\Delta q_{ch}}{C_{gs}} \tag{5.9}$$

Using Eqn. 5.5 and Eqn. 5.6 and substituting the values in Eqn. 5.9 we get Eqn. 5.10.

$$I_{DS}(t) = I_{ref} - \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}}\frac{1}{L}\sqrt{\frac{I_{DS}(t)}{WL}}[\Delta q + I_{leak}t] \tag{5.10}$$

From Eqn. 5.9, its apparent that increasing the value of gate capacitance $C_{gs}$ or decreasing the $g_m$ or both will improve the circuit performance. Increasing the transistor length will serve two purposes, minimizing the flicker noise and increasing the gate capacitance. A separate MOS capacitor is also added to the gate of the current sources to further improve the performance. For the nMOS current source, the capacitor is realized using the nMOS device with drain, source and bulk connected to Gnda and gate connected to the gate of the current source. Similarly for the pMOS current source, a pMOS device with drain, source and bulk connected to Vdda and gate connected to the gate of the current source is used.

### 5.2.3 Modified Calibration Circuit

Increasing the size of the gate capacitance $C_{gs}$ beyond a value is not feasible in terms of area. A MOS capacitor is added to the gate of the current source to

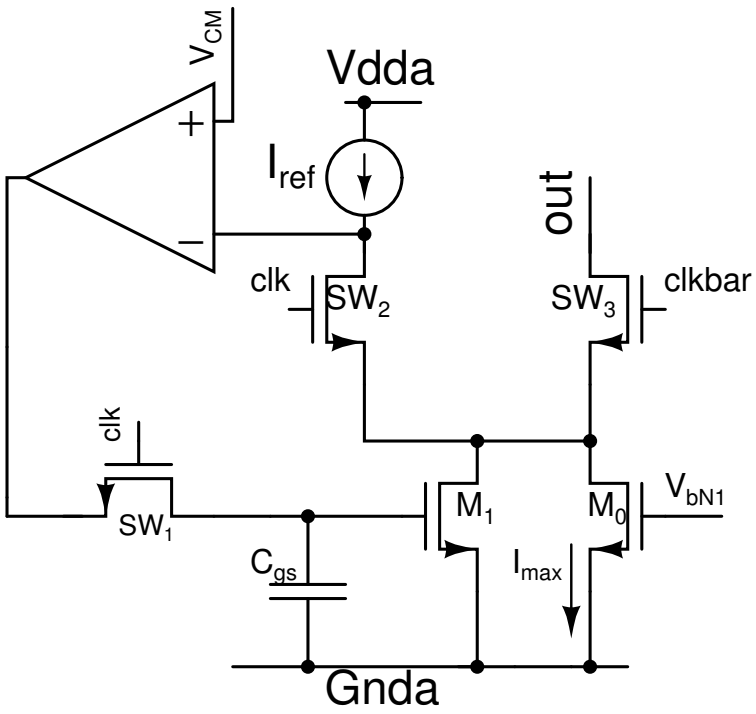


Figure 5.3: Modified Calibration Circuit

increase $C_{gs}$ to 200fF.

Transconductance of the current source also plays an important role, as it reflects the effect of change in the gate voltage. $g_m$ should be minimized as much as possible. Apart from minimizing $g_m$, the $g_m$ is divided into two parts for the calibration as shown in Fig. 5.3. Here $M_0$ carries about 75% of the reference current. This decreases the value of current in $M_1$ to about 25%, which implies that the transconductance of $M_1$ is decreased by a factor of $\sqrt{4}$. Furthermore, its size is also decreased by 4 times, reducing value of $g_m$ by factor of 4 overall. An opamp is used to increase the gain of the calibration loop to calibrate it correctly.

The value of current in the main current source has been decided by the matching requirements. Given the standard deviation of the threshold mismatch and $g_m$ of device $M_1$, we can know the maximum amount of the current mismatch possible in the circuit. The current in $M_1$ should be more than the maximum mismatch current to calibrate properly. The circuit has been designed to calibrate for more than $6\sigma_{V_{TH}}$ mismatch.

The main current source $M_0$ is implemented using simple current mirrors with cascode devices, as its current can vary due to mismatch.

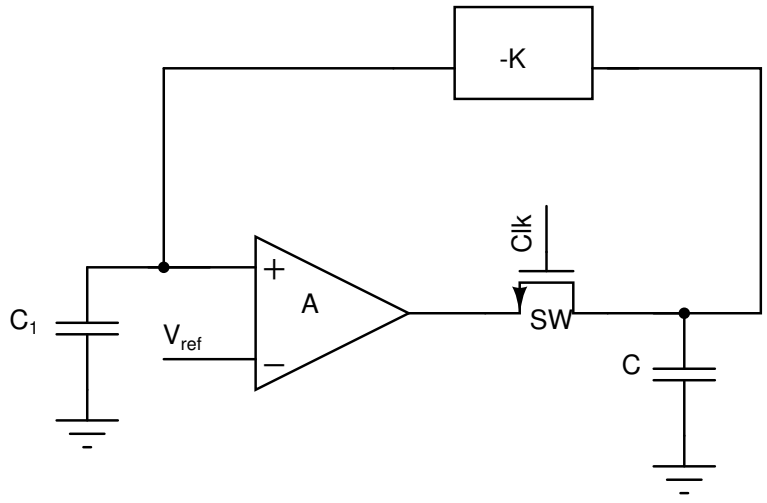


Figure 5.4: Loop Model

The model for the calibration loop is shown in Fig. 5.4. Here, gain block K represents the current source with cascodes. The dominant pole of this loop is because of the capacitance $C_1$, which is mainly because of wiring. With normal single stage opamp, it is found that the phase margin is not enough for stability. The output of the calibration opamp is shown in Fig. 5.5, when a step is applied to the gate bias of the current source.

So, the next choice is either to compensate or to use a diode connected load. Simple diode connected load based opamp is used to avoid complexity due to the compensation scheme. In this case, loop gain is of more importance than the gain of the opamp. The loop bandwidth is reduced to minimize noise folding as disscused in Section. 3.2.3. The modified loop response is shown in Fig. 3.12, with loop BW=100KHz and phase margin=90 degrees. The circuit diagram for both, the pMOS and the nMOS calibration opamp's are shown in Fig.5.6 and Fig. 5.7.

Fig. 5.8 shows the output current of a current cell over a period of time with calibration process. The current changes suddenly after the calibration is done because of the charge injection. Because of the charge leakage, the value of the current varies with time. The calibration period chosen for simulation is 5$\mu$s.

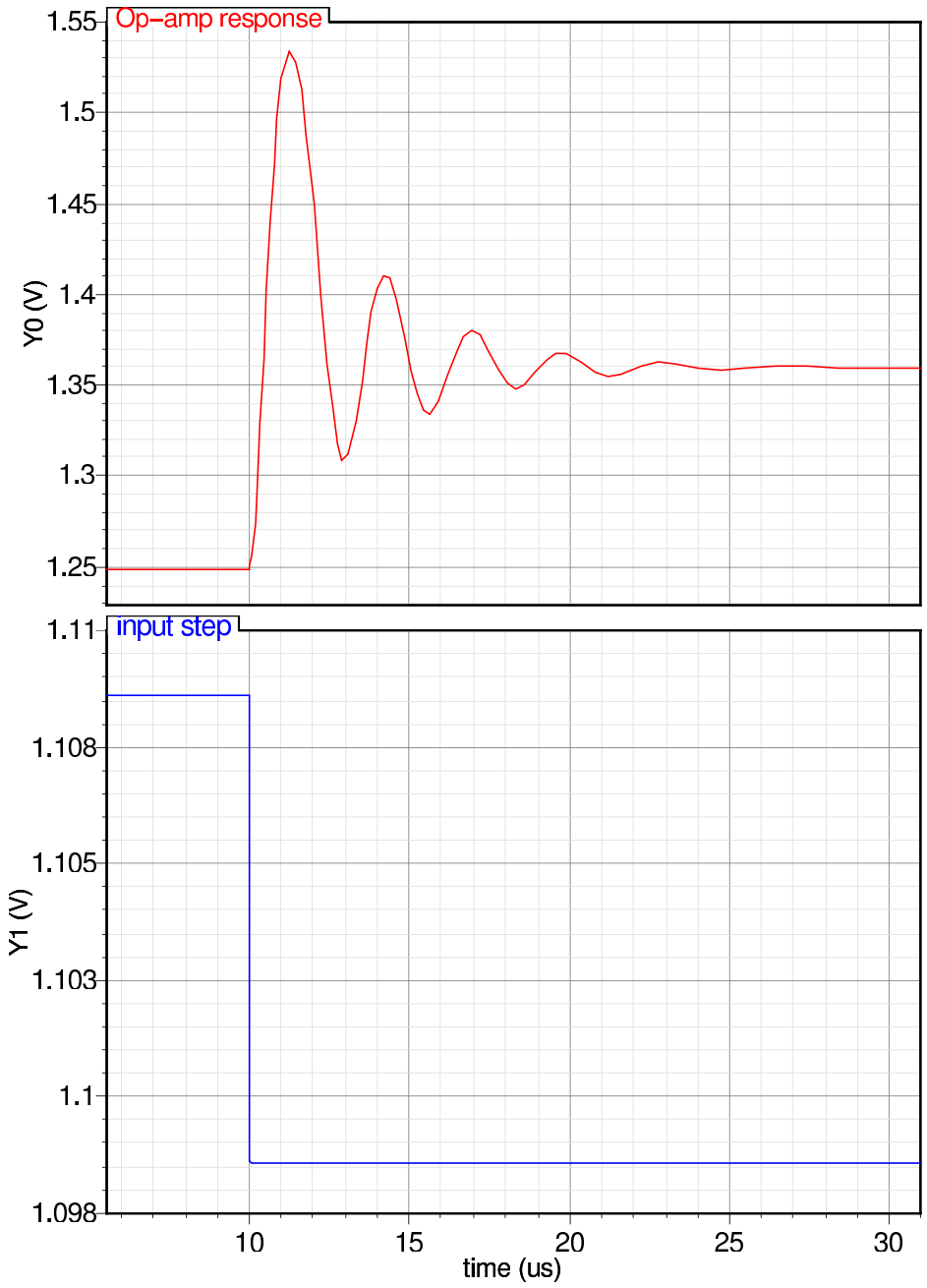


Figure 5.5: Ringing of calibration loop with a single stage opamp with a current mirror load

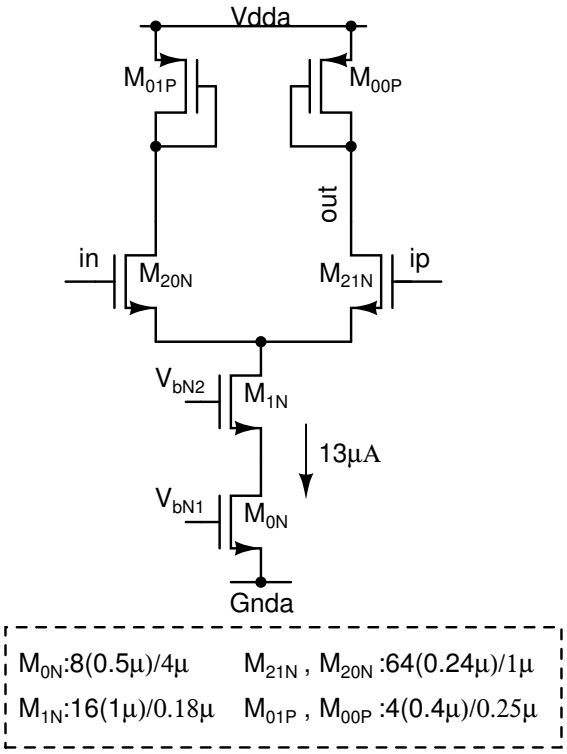


Figure 5.6: Calibration op-amp for PMOS current source

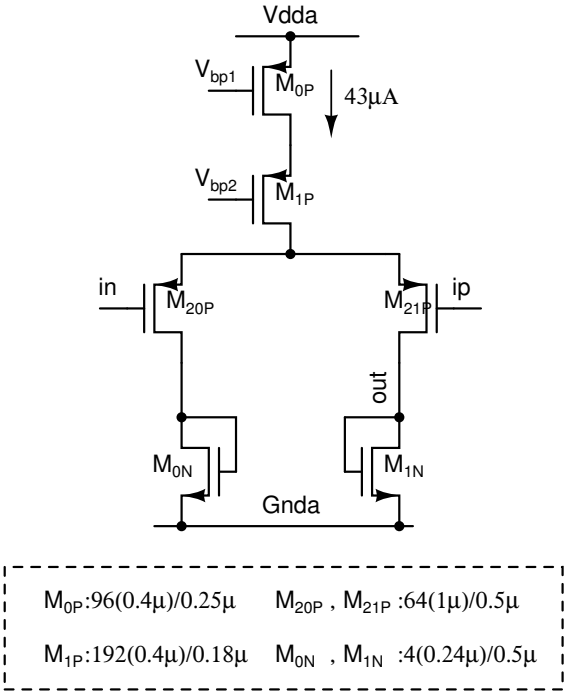


Figure 5.7: Calibration op-amp for NMOS current source

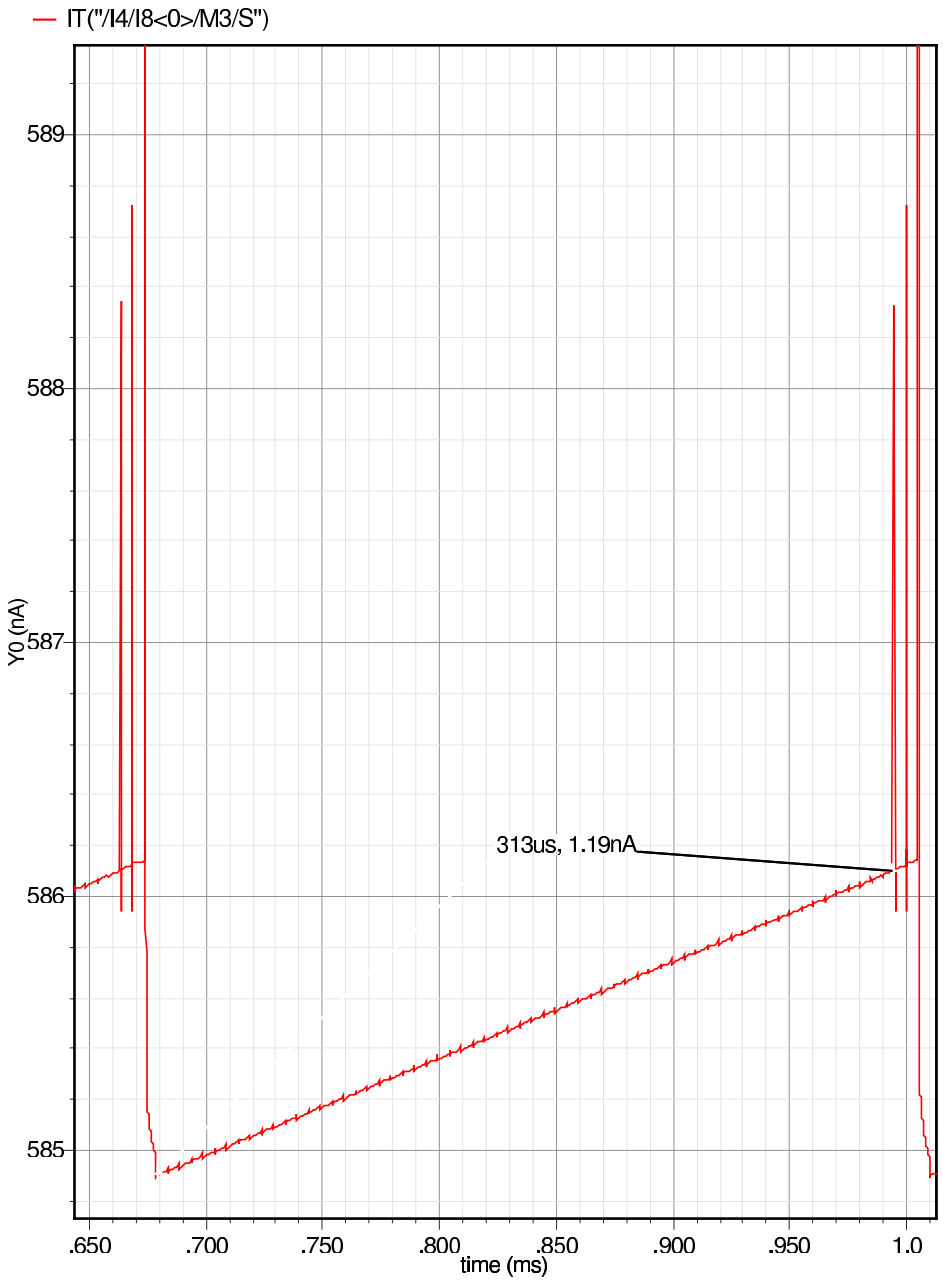


Figure 5.8: Leakage and Charge injection effect

# CHAPTER 6

## Simulation and Layout Results

The DAC presented here is fabricated in 0.18$\mu$m UMC CMOS technology with a power supply of 1.8 V. A low pass filter with a cut-off frequency of 20KHz is used to filter the output of the DAC before taking the FFT. The simulation results are presented in this chapter.

The calibration loop response with the final chosen parameters (bandwidth etc.) is shown in Fig. 3.12. The DAC is simulated for various process corners and the respective current settling is shown in Fig. 6.1.

For all simulations, a Gaussian distribution is assumed for the mismatch. A mismatch is introduced to the gate voltage of the current sources using a Gaussian random voltage generator with standard deviation of $\sigma V_{TH}$. To measure the effect of the calibration, the D/A converter is also simulated without calibration and result is shown in Fig. 6.2. The output spectrum with the calibration period of 15$\mu$s is shown in Fig. 6.3. The SFDR values for above two cases are given in Table. 6.1. An improvement of $\sim$34 dB in SFDR is noticed with the calibration.

The final D/A converter simulation results are shown in Table. 6.2. Here $f_s$ is 6.144 MHz and the input signal frequency is $\sim$1 KHz. The output signal levels for dynamic range and THD are 1mV and 0.5Vrms. The power breakdown for different parts of the chip is shown in Table. 6.3. The noise contributed by different sections of the chip is given in Table. 6.4.

Table 6.1: SFDR values with different Calibration Periods

| Calibration Period | SFDR |
|---|---|
| No Calibration | 66 dB |
| 10$\mu$s | 87.2 dB |
| 15$\mu$s | 90.4 dB |

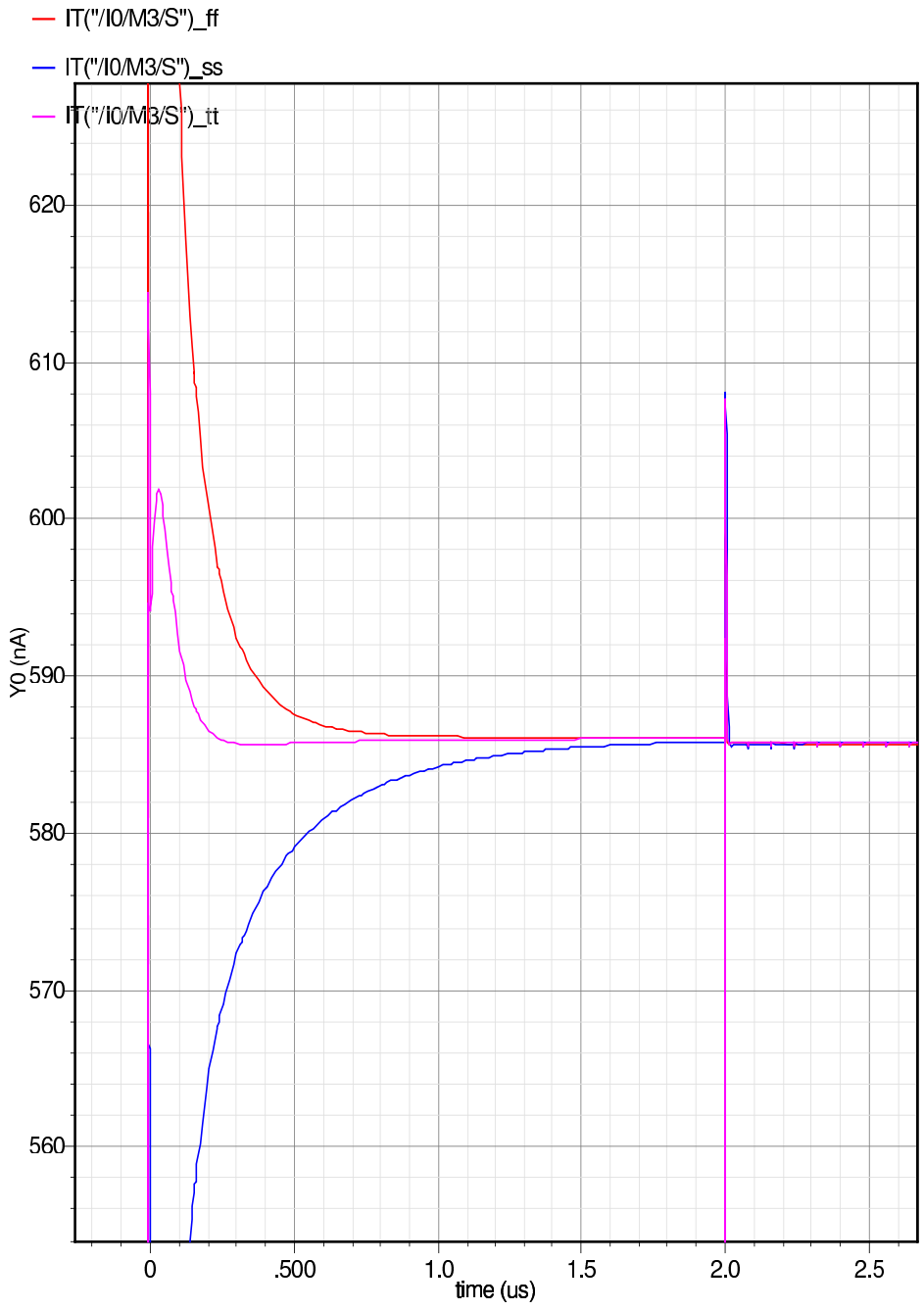


Figure 6.1: Current Settling

Table 6.2: Simulated performance summary of the 16 bit calibrated current steering D/A converter

| | |
|---|---|
| Process Technology | 0.18 $\mu$m UMC CMOS |
| Supply Voltage | 1.8V |
| Full scale output | 1.5Vpp Single-Ended |
| Load ($R_L, C_L$) | 1K$\Omega$ , 100pF |
| Idle Channel Noise (Complementary) | 5.2$\mu$V |
| Idle Channel Noise (One Sided) | 3.7$\mu$V |
| THD (Complementary) | -87 dB |
| THD (One Sided) | -85.1 dB |
| Dynamic Range (Complementary) | 99.6 dB |
| Dynamic Range (Complementary + A-weighted) | 104 dB |
| Dynamic Range (One Sided) | 103 dB |
| Dynamic Range (One Sided + A-weighted) | 107 dB |
| Calibration Rate | Programmable from $f_s/2$ to $f_s/256$ |
| Total Power Consumption | $\sim$1.1mW |
| Chip Area | 1131$\mu$m$\times$ 948$\mu$m |

Table 6.3: Power Consumption in different parts of Chip

| Circuit | Power Consumption |
|---|---|
| Current Steering DAC | 68$\mu$W |
| Calibration Opamps | 100$\mu$W |
| I-V converter Opamp | 360$\mu$W |
| Bias Circuit | 178$\mu$W |
| Digital (@ 6.144MHz) | $\sim$410$\mu$W |

The calibration period chosen for all the results provided in this chapter is 15$\mu$s (mentioned otherwise). For testing purposes, the input to calibration clock generator is taken seperately. This is used to change the calibration period to any extend by changing the input signal and division ratio. Out of band non-harmonic tones are found to be at $\sim$112 dB. When the DAC is simulated at OSR of 128, the total power consumed is $\sim$1.5mW, where $\sim$750$\mu$W is used in digital circuitry and remaining in analog circuitry.

The layout is shown in Fig. 6.4. Layout in the pin package is shown in Fig. 6.5. The layout area can be further reduced by optimizing the MSB current cell area.

Table 6.4: Noise contribution by different parts of the Chip

| Circuit | Contribution (%) |
|---|---|
| Current Steering DAC | $\sim 20\%$ |
| I-V converter Opamp | $\sim 4\%$ |
| Bias Circuit | $\sim 69\%$ |
| Resistor ($R_F$) | $\sim 7\%$ |

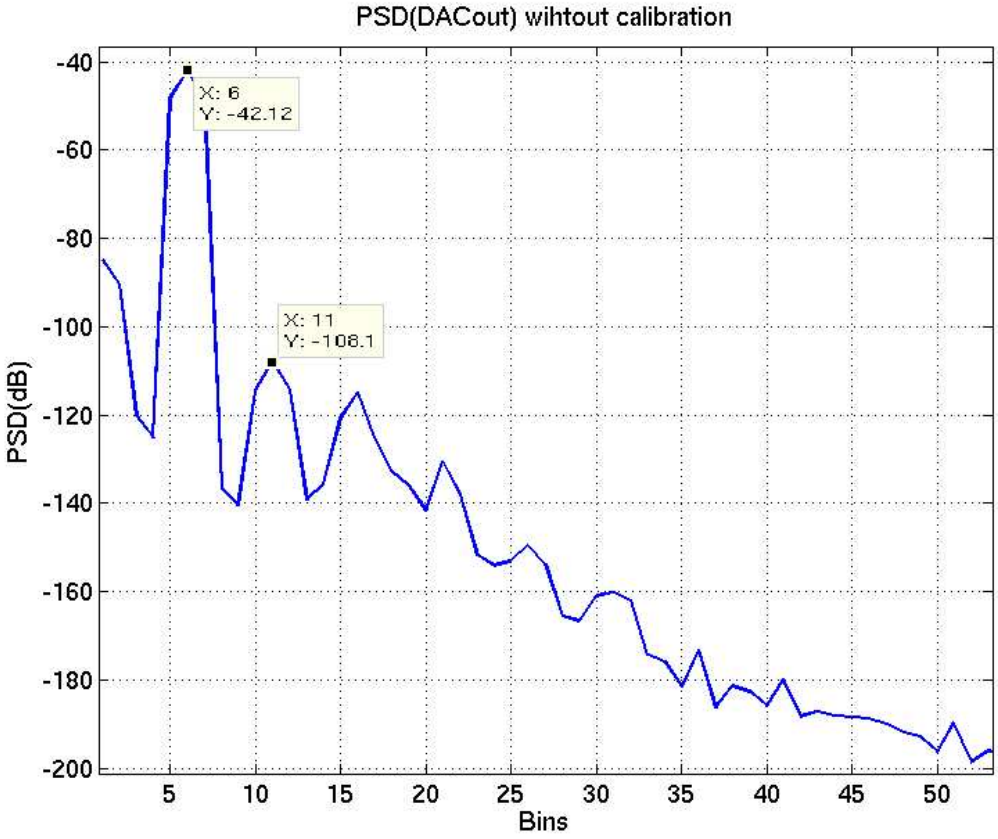


Figure 6.2: DAC output without Calibration

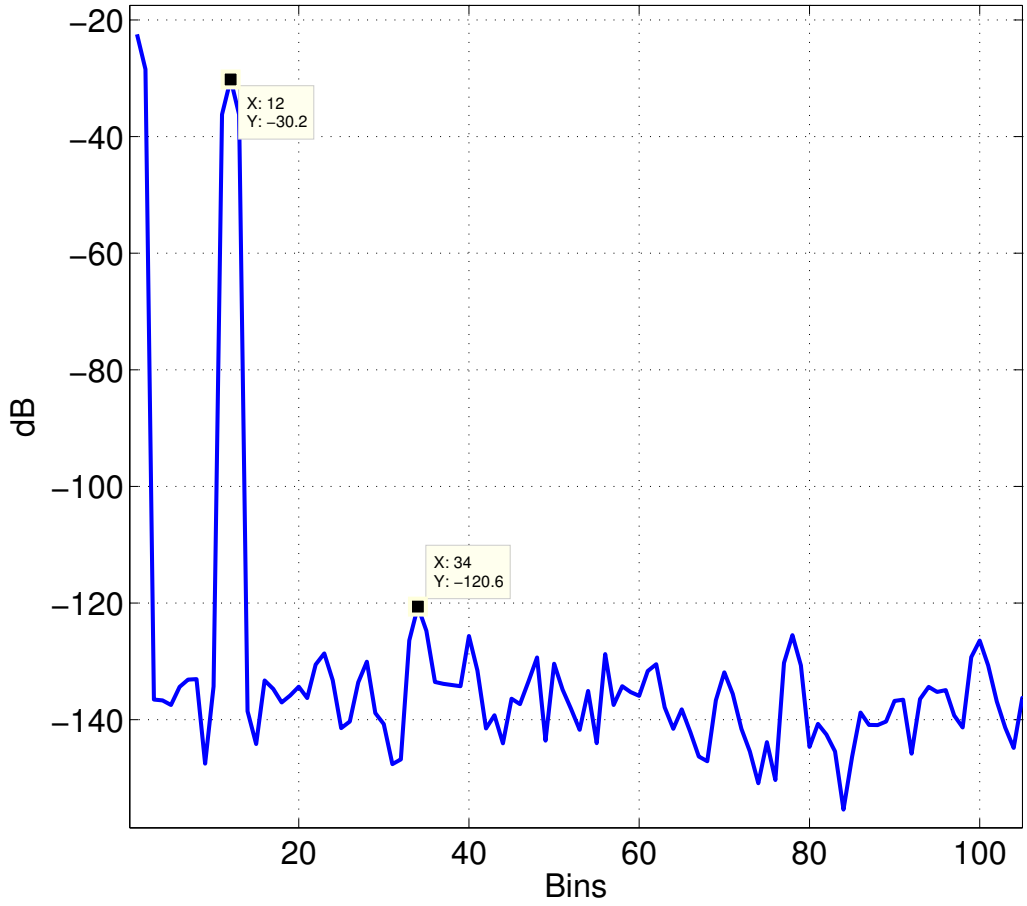


Figure 6.3: DAC output with Calibration

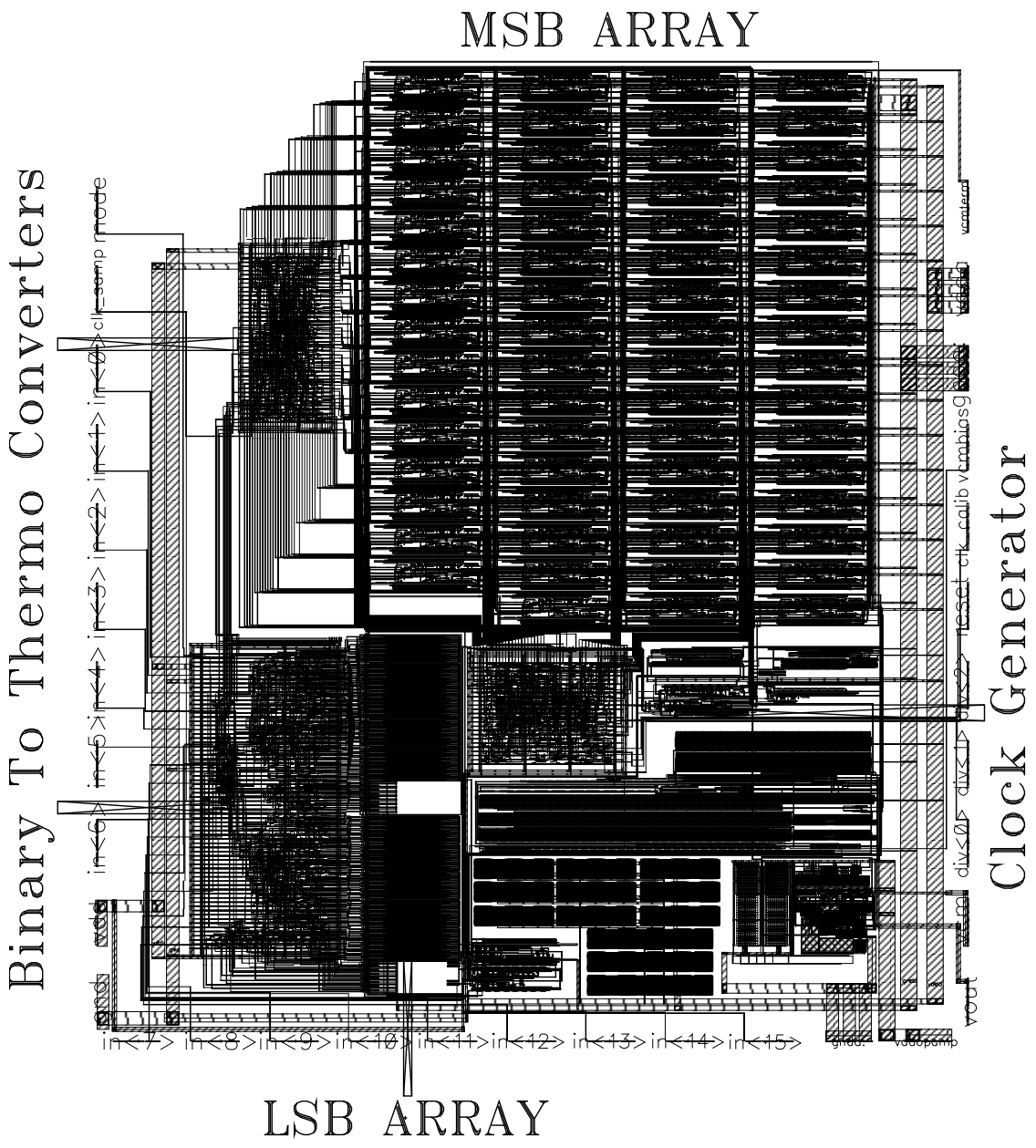


Figure 6.4: Layout of D/A Converter

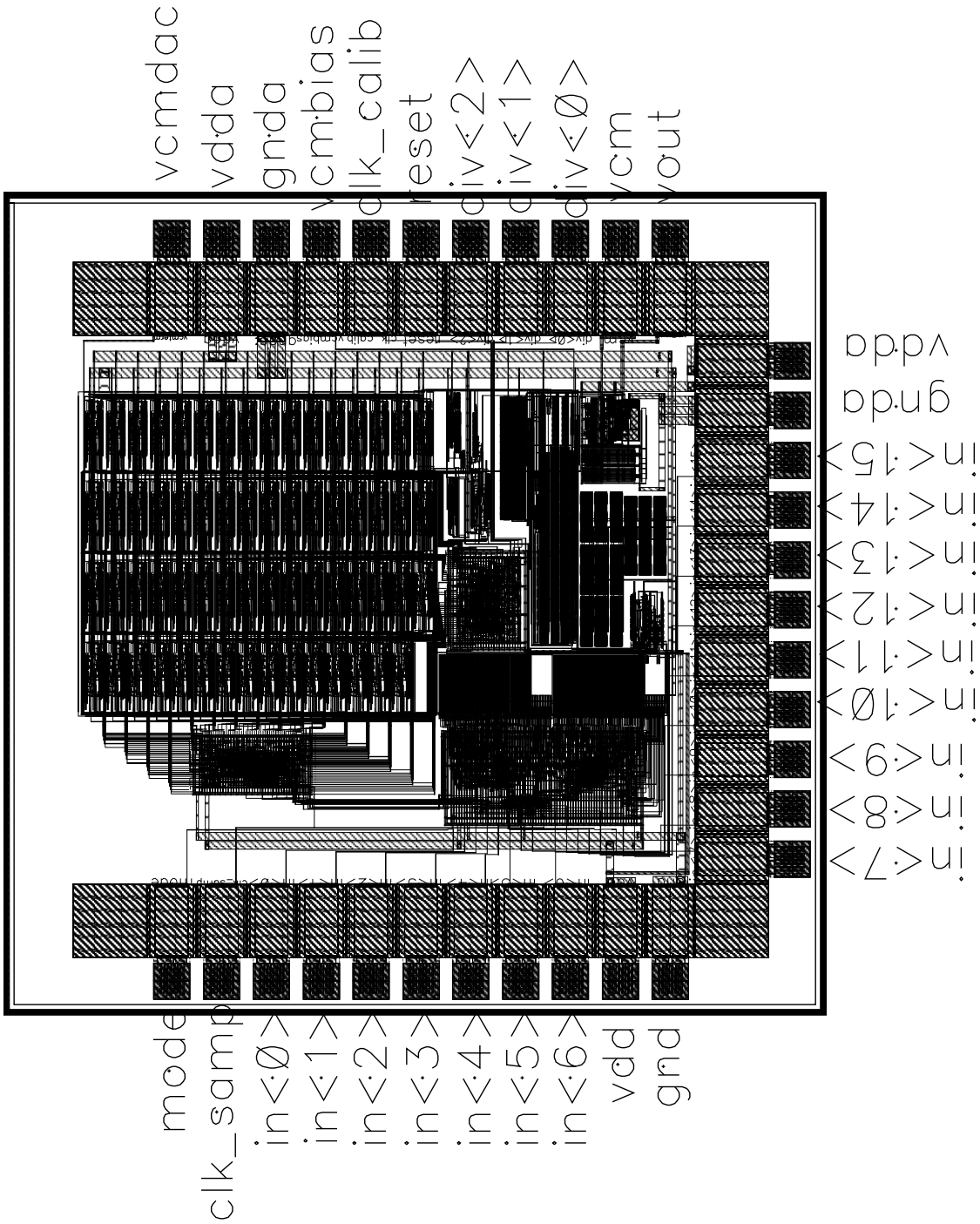


Figure 6.5: D/A Converter with pin Package

# CHAPTER 7

## Deserializer for a High Speed $\Delta\Sigma$ Modulator

The work presented in this chapter is not a part of the audio band D/A converter. Deserializer is used to convert a high frequency signal to several lower frequency signals for the testing or interfacing with other peripherals. The deserializer presented here is used to convert a input stream at 1GHz into two output streams at 500MHz.

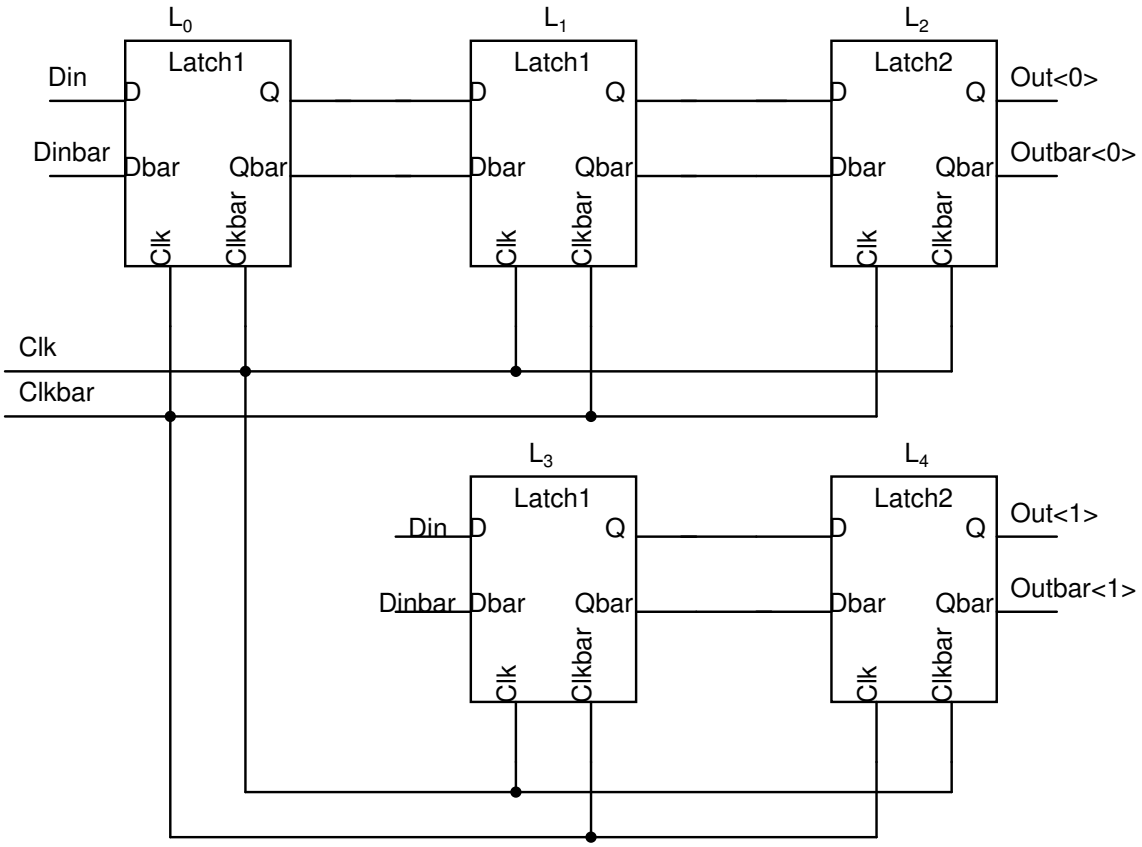


Figure 7.1: Block Diagram of a 1-to-2 Deserializer

The basic block diagram is shown in Fig. 7.1. Here, a data stream Din is taken as input and passed through a series of latches, clocked appropriately by a clock

at 500MHz, generated from the original data synchronized clock using a simple Flip-Flop based clock divider. Transparent latches are used in the circuit.

At the negative edge of the clock, the input data is latched into latch $L_0$. At the following positive clock edge, the data is latched into latch $L_3$ and the data of latch $L_0$ is transferred to latch $L_1$. At the following negative clock edge, the data of latch $L_1$ is sampled into latch $L_2$ and data of latch $L_3$ is sampled into latch $L_4$, while simultaneously, the input data sample is stored at the output of the latch $L_0$, thus completing the cycle. After this, at every negative edge of the clock, the input data is sampled at the output through the two paths at half the speed.

Because of the swing issues, two types of latches with different swings are used. The final stage latches have more swing than the earlier ones to make the interface working in all the process corners. The latches are shown in Fig. 7.2 and Fig. 7.3.

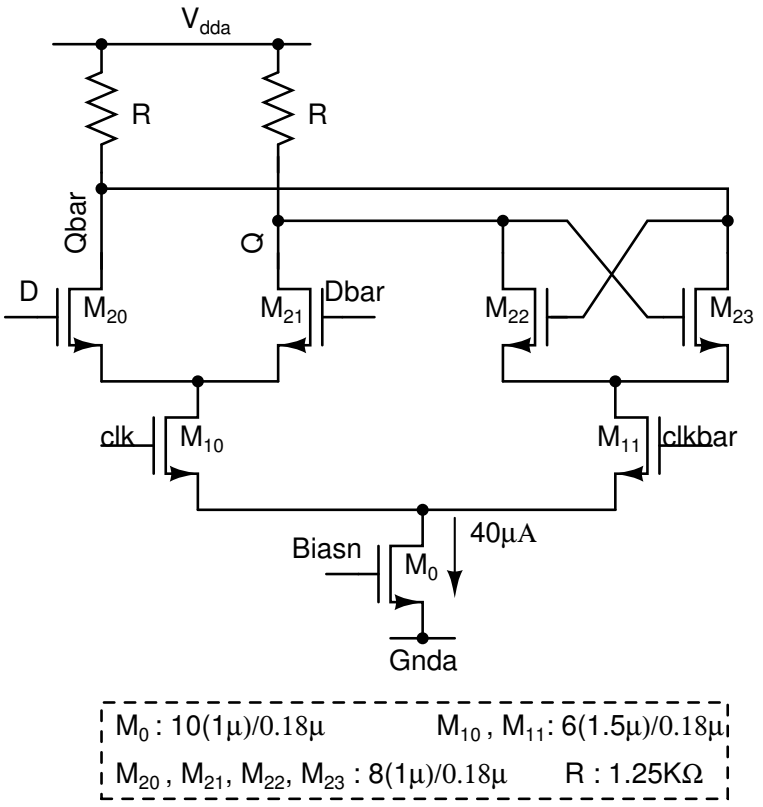


Figure 7.2: Latch 1

The output of the deserializer should be in LVDS standard. A CML to CMOS converter is used. The output of this converter is fed to the LVDS driver as

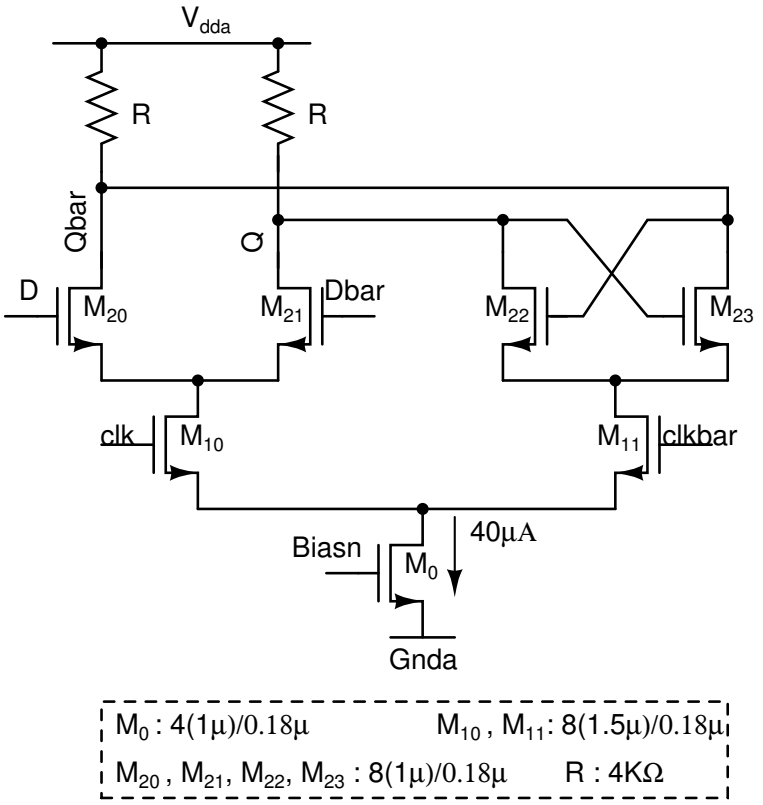


Figure 7.3: Latch 2

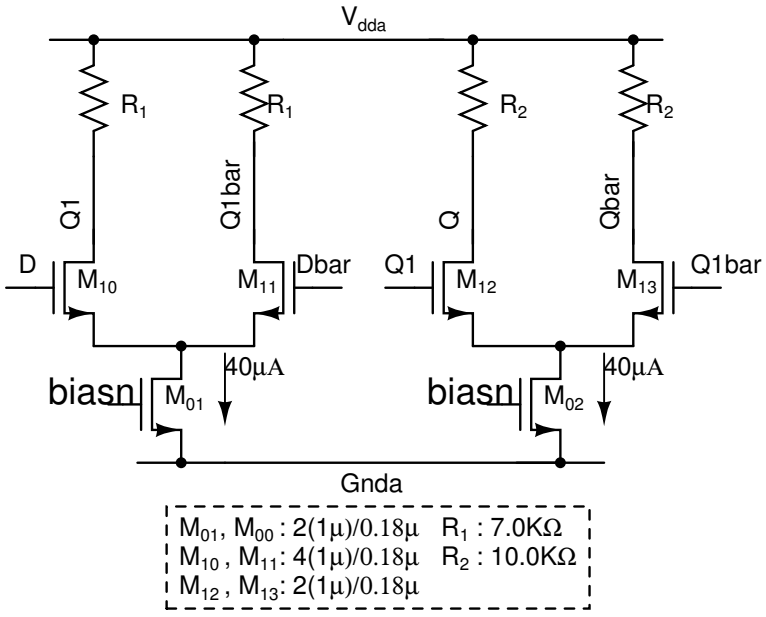


Figure 7.4: CML Buffer

presented in Ref. [8]. A CML to CMOS converter is shown in Fig. 7.5. The LVDS driver is shown in Fig. 7.6

Here the input is first buffered to avoid loading and to maintain the rise/fall time properly. The Buffer is shown in Fig. 7.4. Since the output of the CML varies from $V_{dda}$ to $(V_{dda} - IR)$, an inverter with the transition voltage close to Vdda is used. It will convert the CML signal into a CMOS signal. To further avoid loading, a chain of inverters with appropriate sizes are used.

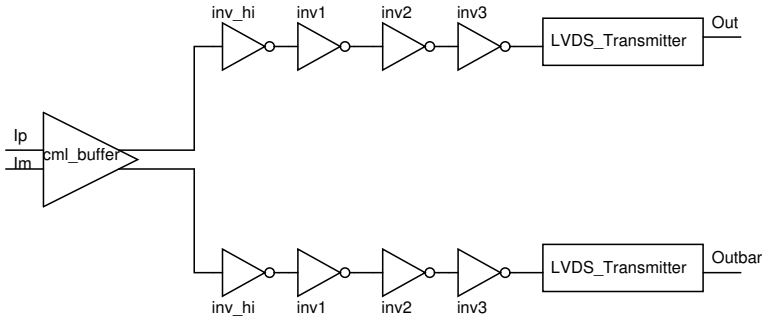


Figure 7.5: CML to CMOS converter

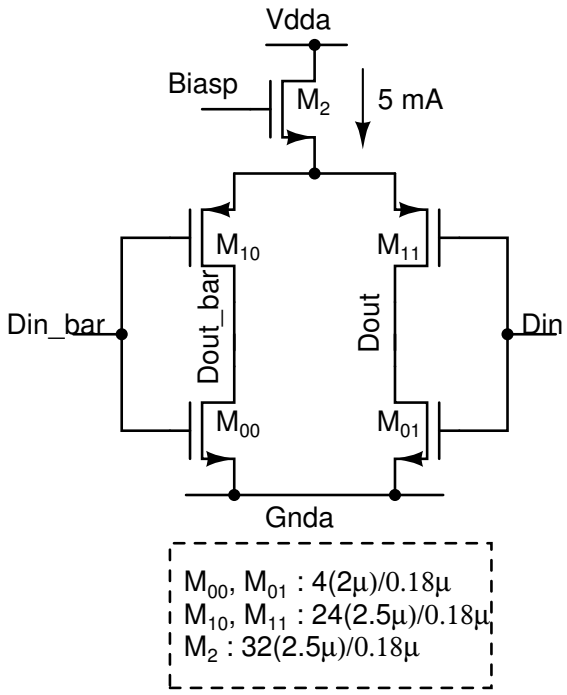


Figure 7.6: LVDS Transmitter

The eye diagram of the output clock and the data stream for the process corner (fnsp, rmax, $T = 70°C$) is shown in Fig. 7.7. The positive edge of the clock comes

after the data is settled properly. The deserializer presented in this chapter is implemented in 0.18 $\mu$m UMC CMOS technology with 1.8V power supply. The power consumed by the circuit is ∼60 mW. The total layout area of deserializer is 372$\mu$m × 242$\mu$m. The layout is shown in Fig. 7.8.

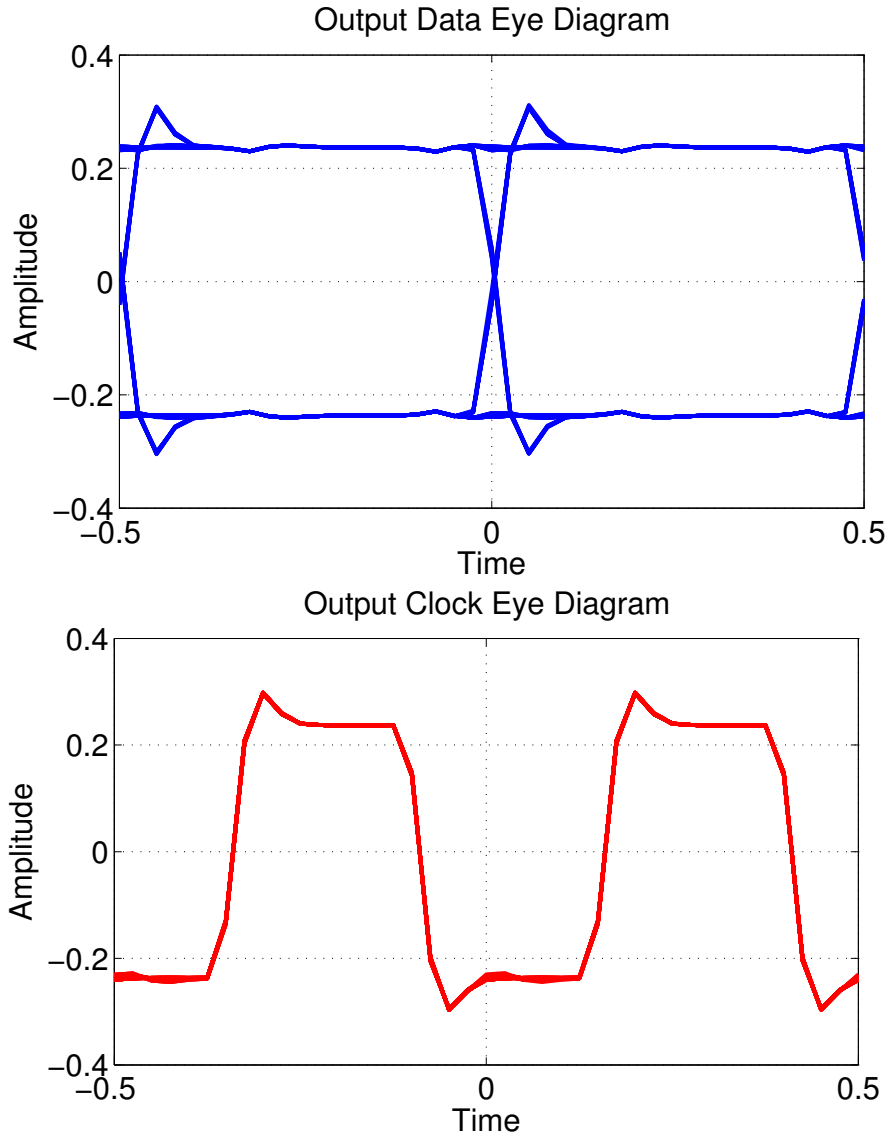


Figure 7.7: Eye Diagram of a) Output Data b) Data Synchronized Clock

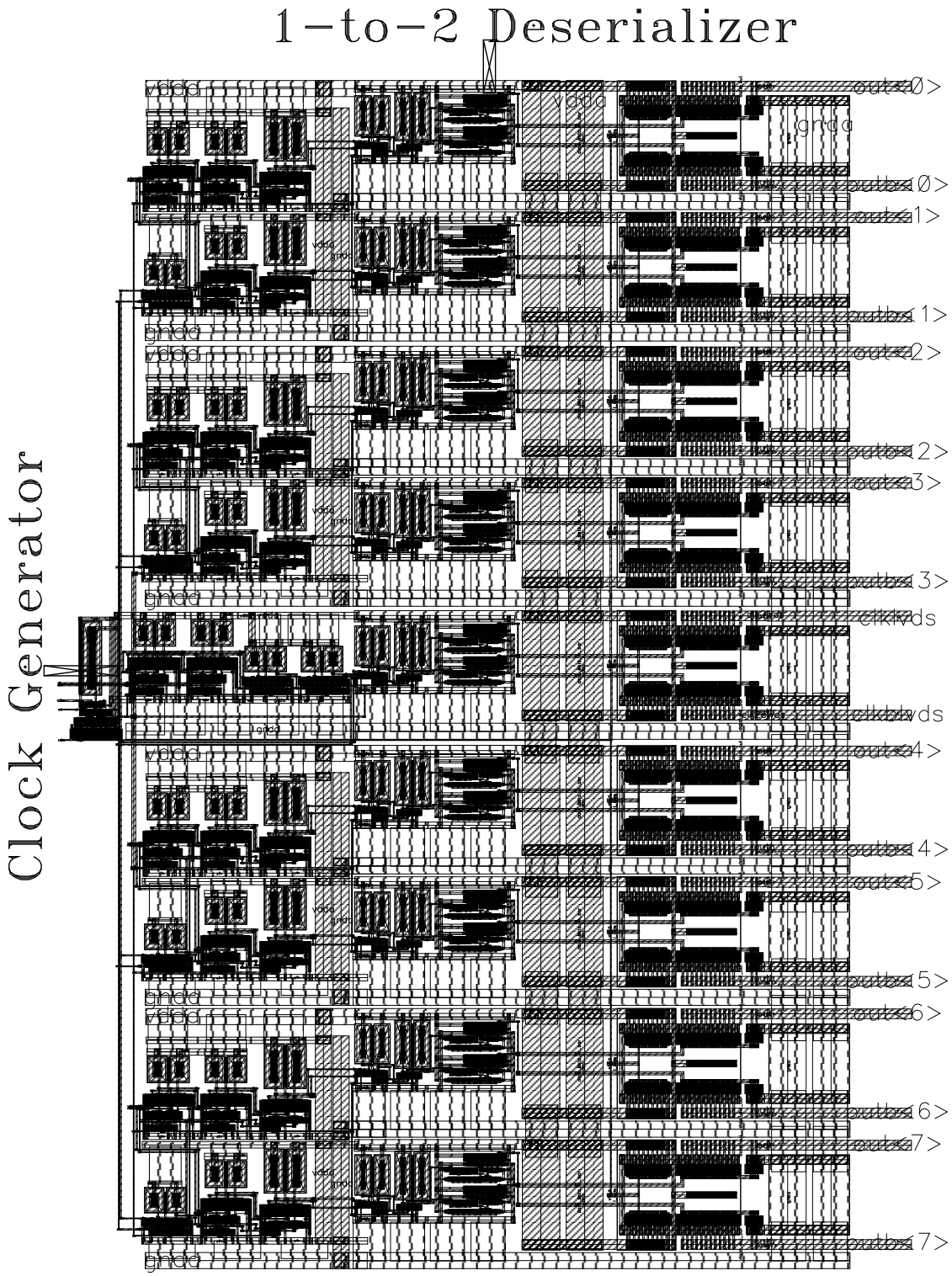


Figure 7.8: Layout of a 4-to-8 Deserializer

# CHAPTER 8

# Conclusions and Future Work

## 8.1 Conclusions

The 16-bit current steering calibrated digital to analog converter presented here is optimized for noise, power and the out of band non-harmonic tones. The main focus was on minimizing power while keeping the noise within specifications. It is found that the calibration parameters should be chosen very carefully as there is a huge trade off between the noise/area and the distortion. The calibration increases the noise and reduces the distortion. The flicker noise is not the main cause of concern in the calibrated audio DAC because of the noise folding. The thermal noise folding makes it a dominant part of the total noise.

Here, the 16 bit binary input is taken serially and converted to the thermometer code. The peak output current swing of the converter is $\pm 37.5$ $\mu$A. A 20K$\Omega$ resistor is used, in the negative feedback configuration, to convert I to V using an operational amplifier, with the gain of 100 dB and bandwidth of 10MHz, for an output swing of $\pm 0.5$ Vrms.

The digital circuitry is the most power hungry part of the D/A converter. It has been designed to work at the OSR varying from 4X to 512X. The power consumed by the digital circuit can be reduced by splitting the digital block. But this can cause the problem of complexity in layout. Apart from that, because of the large wiring capacitance, large power is consumed in the output drivers. It is expected to consume less power when used at the low OSR values because of reduced switching. But, the reduction in power will not be proportional to frequency because of the large number of drivers present. When the OSR is reduced from 128 to 16, the power goes down from 410$\mu$W to 61$\mu$W.

Large on-chip bypass capacitors and metal shielding between the analog and digital signal wires are used to bypass the switching feed through in the gate bias voltage of the current source. A random clock is used to avoid on-board coupling between adjacent wires. Digital and Analog part of the converter are powered using separate supplies, as the digital supply will have large switching glitches in the power supply, which can affect the performance of the DAC.

## 8.2 Future Work

The D/A converter exceeds the idle channel noise and THD specification when switched in one-sided switching mode. So, the current of the first stage of the I-V converter can be reduced to reduce the power consumption. This will increase the noise contribution by I-V converter. Since, in idle channel case, noise of the I-V converter is dominant, it can be increased by more than twice while still meeting the given noise specification.

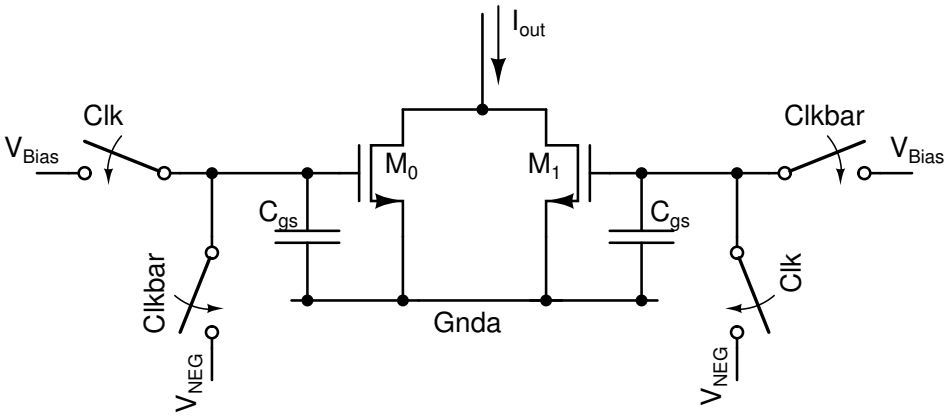


Figure 8.1: Switched Biasing Circuit

Large device lengths were chosen to minimize the flicker noise due to the current sources. It was observed during the designing of the converter, that the flicker noise is not the dominating factor of the total noise. This implies that the length of the devices can be reduced and the DAC can be made for the same noise specification. This may give a reduction in area.

Apart from that, a switched biasing technique can also be implemented as described in Ref. [4]. The basic switched source technique circuit, as shown in Fig. 8.1, is fabricated in 0.18$\mu$ m UMC CMOS technology.

Also, due to the single ended output requirement, half the current is plainly terminated. A better scheme can be used where instead of termination, both half of the currents can be used to convert to a single ended output.

# APPENDIX A

# APPENDIX

## A.1 Dynamic Range

Since most of the audio applications are not used at full volume all the time, the true measure of noise in audio system is when there is no input signal present. For calculation purpose, we give an input signal 60 dB below the full scale. The dynamic range is given by:

$$DR = SNR + 60dB \tag{A.1}$$

In our case, the full scale amplitude at the output is $0.5Vrms$.

## A.2 A-weighted Filter

A-weighted filter is used to shape the noise, to measure the SNR according to the human ear sensitivity towards signals at various frequency [9]. Its transfer function is given below:

$$R_A(f) = \frac{12200^2 * f^4}{(f^2 + 20.6^2)\sqrt{(f^2 + 107.7^2)(f^2 + 737.9^2)}(f^2 + 12200^2)} \tag{A.2}$$

$$A = 2.0 + 20log_{10}(R_A(f)) \tag{A.3}$$

The filter response is shown in the figureA.1:

Where f is defined till 20KHz. To find the A-weighted dynamic range, noise is multiplied with filter's response and then DR is calculated.

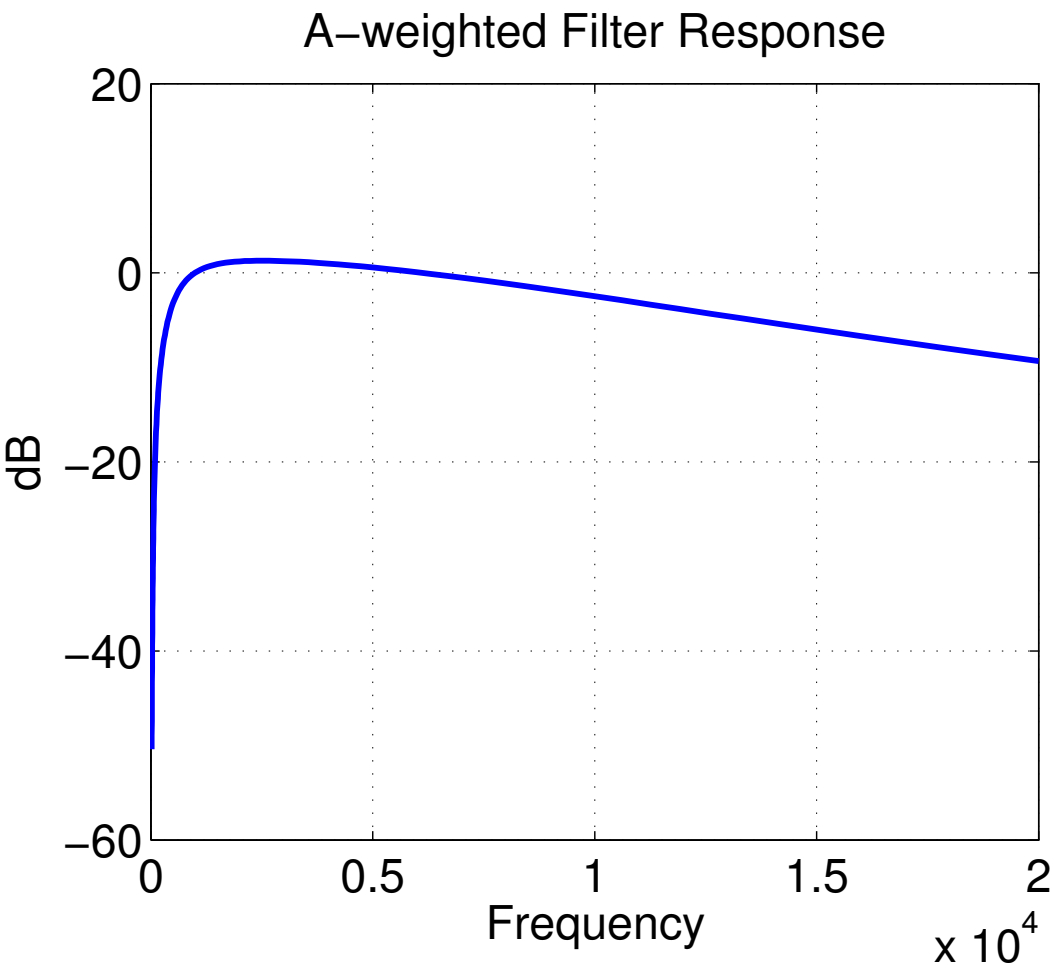


Figure A.1: A-weighted Filter Response

# REFERENCES


[1] Chi-Hung Lin and Klaas Bult. "A 10-b 500-MSample/s CMOS DAC in 0.6 $mm^2$", *IEEE Journal of Solid-State Circuits*, Vol.33, Page(s):1948 - 1958, No.12, December 1998

[2] UMC180, ver9.1 Documents.

[3] Sandeep Monangi, "16 bit Audio Band Digital-to-Analog Converter", *M.Tech Dissertation*, IIT Madras, 2009.

[4] Eric A. M. Klumperink, Sander L. J. Gierkink, Arnoud P. van der wel and Bram Nauta. "Reducing MOSFET $1/f$ Noise and Power Consumption by Switched Biasing", *IEEE Journal of Solid-State Circuits*, Vol.35, Page(s):994 - 1001, No.7, July 2000

[5] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill Edition, 2002, ISBN 0-07-052903-5

[6] K. Ola Andersson, Niklas U. Andersson, Mark Vesterbacka and J. Jacob Wikner. "A 14-bit Dual Current Steering DAC", *IEEE Journal of Solid-State Circuits*, Vol.35, Page(s):994 - 1001, No.7, July 2000

[7] D. Wouter J. Groenveld, Hans J. Schouwenaars, Henk A. H. Termeer and Cornelis A. A. Bastiaansen. "A Self-Calibration Technique for monolithic High-Resolution D/A Converters", *IEEE Journal of Solid-State Circuits*, Vol.24, Page(s):1517 - 1522, No.6, December 1989

[8] Reddy Karthikeyan, "Analysis of Clock Jitter in Continuous Time $\Delta\Sigma$ Modulators", *M.S. Dissertation*, IIT Madras, 2007.

[9] http://en.wikipedia.org/wiki/A-weighting

[10] M. Gustavsson, J. J. Wikner and N. Tan. "CMOS Data Converters for Communications", *Kluver Aademic Publishers*, Boston, MA, USA, 2000, ISBN 0-7923-7780-X