Testing and Characterization of IEEE 802.15.4 based given ZigBee transceiver

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Testing and Characterization of IEEE 802.15.4 based given ZigBee transceiver**, submitted by **Divya kesharwani**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Courses on Analog IC design and VLSI Broadband Communication circuits by Dr. Nagendra Krishnapura were the best classes I have undertaken. His courses helped me in understanding of IC design concepts and kept my desire to learn analog alive.I wish to emulate his consistency and dedication to work.At this point I would also like to thank Dr. Shanthi Pavan, who first introduced me to the world of Analog Design.I thank both the professors for developing my concepts in Analog VLSI.I also thank the entire EE department for making my stay at IIT Madras an enduring one.

I thank Vallabhaneni.M for helping me continuously during the course of my work and also for the technical discussions i had with him.Many thanks to him for designing the PCB board for the testing.The layout is given in chapter 6

Thanks to Debashish Behera and Asif Basha for all the discussions we had in lab.Thanks to every one who helped me in any way for successful completion of the project.Finally I dedicate this thesis to my parents and my family.

ABSTRACT

The project involves the understanding and documentation of specifications of previously designed ZigBee transceiver chip (here after referred as *'the chip'*) and later to test the performance of the chip.The thesis gives an insight of what is there inside the chip without going in to detailed technical aspects of what made it to be there inside the chip.

To begin with, a compatible microstrip antenna was fabricated and was tested for the specifications which gave the impedance bandwidth of 175MHz and resonates at 2.5GHz range meeting the ZigBee standard.Later a PCB board, to mount the chip and other off-chip components needed to test the chip, was designed and fabricated.The memory register of the chip was programmed using Spartan3 FPGA board, the code for which was written in Verilog.Eight chips were tested for Frequency Synthesizer's functioning.One out of eight chip worked with linear VCO characterization,phase noise of -132dBc/Hz @ 3.5MHz from carrier and spurs of -48dBc @ 5MHz.The power amplifier was tested and the maximum power obtained was around -19.44dBm when expected is 0dBm for ZigBee standard.The results in details for every chip is presented here in.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Abbreviations

VSWR Voltage Standing Wave Ratio

FPGA Field Programmable Gate Arrays

NEGCOMA Non-radiating Edge Gap Coupled Microstrip Antenna

PCB Printed Circuit Board

RxTx Receiver and Transmitter chain

Table 1: List of Instruments used

Device	Manufacturer	Model;specs
Spartan3 FPGA Board	Xilinx + Digilient	XE3S200
Digital Storage Oscilloscope	GW Instex	GDS-840C;250MHz;25GS/s
ES4 Series Signal Generator	Agilient	E4422B;250KHz-4GHz
DC power supply	GW Instex	GPS 4303;4CH
Spectrum Analyzer	HP	8592A;50KHz-22GHz
Logic Analyzer	Agilient	1682AD
PNA series Vector Network Analyzer	Agilient	E8362B;10MHz-20GHz
ECal Module	Agilient	N4691-60001;10MHz-26.5gHz
multimeter	CIE	8050

CHAPTER 1

Introduction

1.1 Motivation

IEEE 802.15.4 (ZigBee)is an IEEE standard for low cost, low power, low data rate, and short range wireless personal area networks with a high density of nodes and simple protocol.The 2.4-GHz band assigned by IEEE 802.15.4 is highly attractive, since this unlicensed band is commonly available throughout the world. Applications of this low data rate standard include those for industrial and commercial uses, home automation, PC peripherals, consumer electronics, and personal health care appliances, as well as for toys and games that should be able to run for six months to two years on just button cells or batteries.

The purpose of this work is to test the previously designed ZigBee protocol based RF chip and characterize the Receiver and Transmitter chain and the local oscillator.The design was the contribution of previous students at IIT Madras toward the ZigBee transceiver design project and final testing of the design is an integral part of completion of the ZigBee Project.

The Documentation and characterization of the chip is also a motivation of this project.The project deals with hardware testing of the chip where the board for

testing was designed and two iteration were done to reach the results which are listed in this work.

1.2 Organization

Chapter 2 deals with the basic concepts of antenna design and characterizes a compatible antenna for the test process.

Chapter 3 deals with the description of the designed chip and pin description.

Chapter 4 deals with the programing of digital interface of the chip.

Chapter 5 deals with the Frequency Synthesizer architecture,testing and results.

Chapter 6 deals with issues related to board design and layouts are presented.

Chapter 7 concludes the report by drawing the inferences and presenting the summary and future work.

CHAPTER 2

Antenna Fabrication and Testing

The antenna is usually the last element considered when designing an RF equipment.But remember, a chain is as weak as its weakest element.As the part of the transmission chain is a wireless link, the transmit and receive antenna are directly involved to achieve the desired overall performance.

2.1 Definitions

Definition 1 :An antenna is a conductive element with converts electrical energy in to an electromagnetic field (transmit) or converts an electromagnetic field in to electrical energy (receive) .It bears the property of reversibility.Its characteristics are center frequency, bandwidth, polarization, gain, radiation pattern and impedance.

Definition 2: Coaxial feed: Here the metal conductor connects the radiating patch and excites it.The construction is simple and its easy to obtain the impedance matching.Figure 2.2 shows a coaxial feed to a patch antenna.

Definition 3: Patch or microstrip antenna is used at higher frequencies as it has advantage of real omni directional pattern,but it gives sharp bandwidth.Mostly microstrip antenna operates in TM10 mode.

Definition 4:Radiating Edge:In a patch antenna the vertical components of the

electric field at the two edges along the width cancel one another in the broadside direction whereas the horizontal components combine in the broadside direction. Therefore, the edges along the width are termed as the radiating edges.The fields along the length cancel completely in the broadside direction, and hence the edges along the length are known as nonradiating edges.

2.2 Motivation for NEGCOMA antenna

The ZigBee 802.15.4 standard offers 2.4GHz band that is commonly available.As there are challenges like reduced power consumption, flicker noise and DC offset, it is essential to use a suitable and compatible antenna for testing.An application specific micro strip antenna (also known as patch antenna) was fabricated and tested by

1. Coaxial feeding form the radiating plane.

2. Coaxial feeding form the ground plane.

Why NEGCOMA was chosen: Of the verious Mircostrip antenna that were analysed in the simulation results in [3], REGCOMA (radiation edge gap-coupled micro strip antenna), NEGCOMA (non radiating edges gap-coupled microstrip antenna) and Differential NEGCOMA were well suited for ZigBee band but the first one being too bulky and third one being to complex were ruled out and we chose NEGCOMA to fabricate for testing.The parasitic patched along the non-radiating edge

in NEGCOMA helps in achieving the required bandwidth due to dual tuning effect [3]

2.3 Performance Measures

As mentioned in section 2.1, an antenna can be characterized by various parameters.For the present purpose of testing the chip out main concern was to meet the required *bandwidth* of antenna.The antenna bandwidth is explained below.

2.3.1 Standing Wave Ratio(SWR):

The proper matching of the antenna to the feed point implies that both impedance are identical.This condition ensures that all the energy delivered by the feed point is converted in an electromagnetic field.In case of mismatch,the reflected wave and original travelling wave sets standing wave in the transmission line.The maximum value of envelop to the minimum value of the envelop is termed as Voltage Standing Wave Ratio ($VSWR$).It determines the amount of energy which is not converted by antenna into an energy but is returned to the transmitter (return loss).The antenna can radiate(wanted) or burn the energy(unwanted).

VSWR and reflection coefficient Γ are related by:

$$\text{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{2.1}$$

and Return loss is related to reflection coefficient Γ as:

$$\text{Return loss} = -20 \log |\Gamma| \tag{2.2}$$

The accepted criterion for good matching is VSWR ≤ 2.

One possible way is to keep the *Return loss* in the range.Form the equation 2.1 , $|\ \Gamma\ |$ is found to be $\frac{1}{3}$ and thus the Return loss should be less than $\approx$ 10dB. The range of frequencies this condition is satisfied is called *Bandwidth.*

Since the designed antenna is a single port system it has only S_{11} parameter which is a measure of its return losses or matching and can be used to determines the bandwidth.We used the log-magnitude plot of S_{11} to see the minimum return loss and then smith chart to find the corresponding impedance of the feed point.The bandwidth is expected to be greater than 80 MHz (16*5MHz) to assimilate 16 channels (each of 5MHz) and the impedance of around 50 Ω as the transmitter and receiver feed points are designed to be 50 Ω termination.
Using the Vector Network Analyzer (VNA) we found the plot of antenna's S_{11} parameter.The VNA offers an impedance of 50 Ω.

2.4 Test setup

We calibrated the VNA sweep for frequency range of 2 GHz to 3 GHz and also the reference standard of Omni-directional antenna using the Electronic calibration module mentioned in list of instruments used table 1. with respect to which the

performance of our antenna will be measured.Tightening the SMA connector well and placing the antenna at proper orientation such that it is away form any metal object is essential for better and accurate measure of the result.

Figure 2.1: Antenna Test Setup.

2.5 Substrate specification and simulation results

2.5.1 Substrate

The substrate used in the final antenna implementation was made of copper cladded glass fiber substrate (FR4 Substrate) as the simulation was done with this substrate and acceptable results were obtained.In the simulation process return loss, VSWR and impedance variation versus frequency were studied.

The table 2.1 gives the substrate specification of the antenna fabricated.

Table 2.1: Substrate Specification

Parameter	Name	FR4
ε_r	Relative Permittivity	4.4 S/m
μ_r	Relative permeability	1 S/m
h	Substrate thickness	1.6mm
T	Metal Thickness	35 μm
σ	Conductivity	4.37e7 S/m

2.5.2 Simulation results and Antenna Configuration

The simulation for the NEGCOMA antenna with the dimensions as shown in the figure 2.2 gave two resonant frequencies at 2.47GHz and 2.41GHz (three in reality).The impedance bandwidth of 103.2MHz was obtained form 2395.8GHz to 2498GHz which is suitable for ZigBee band.The two parasitic patches along the non-radiating edge increases the impedance bandwidth.

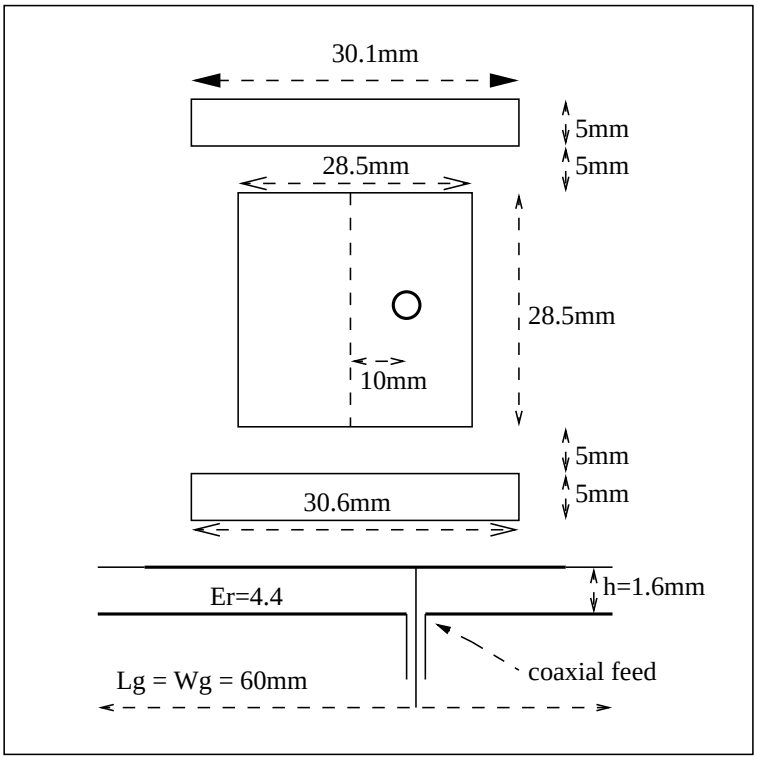

Figure 2.2: Dimensions of NEGCOMA.

2.6 Test Results and Comparison

The antennas were tested with coaxial feed from both side.Using the test setup shown in section 2.4 , *Bandwidth* and feed point *impedance* were obtained.

2.6.1 Coaxial feed from ground plane

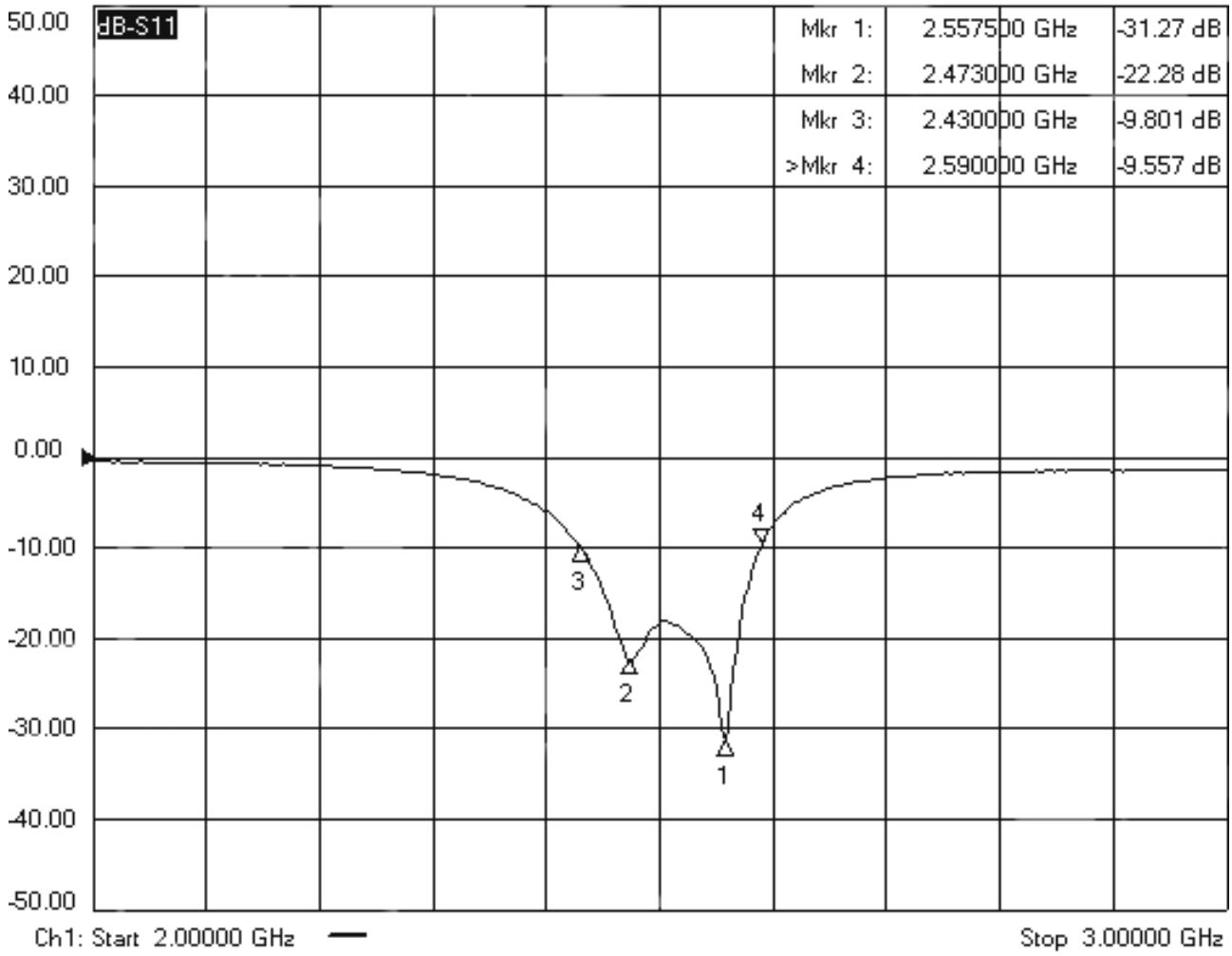

Figure 2.3: Log S_{11} Vs Frequency for bottom feed.

1. Log S11 plot with frequency (refer figure 2.3): The resonance is seen at two points as expected.First at 2.5575GHz and second at 2.4730GHz with the

minimum return loss(Marker 1 and 2 in figure).Marker 3 and 4 are the points of 10 dB crossing which determines the bandwidth.The obtained bandwidth is 160MHz which is good and acceptable for the ZigBee band.

2. Smith chart (refer figure 2.4) : It is clear form the smith chart that marker 1 and Marker 2, where antenna resonates, has impedance very close to 50 Ω as expected.This would ensure better matching at the feeding points and results in minimum return losses.

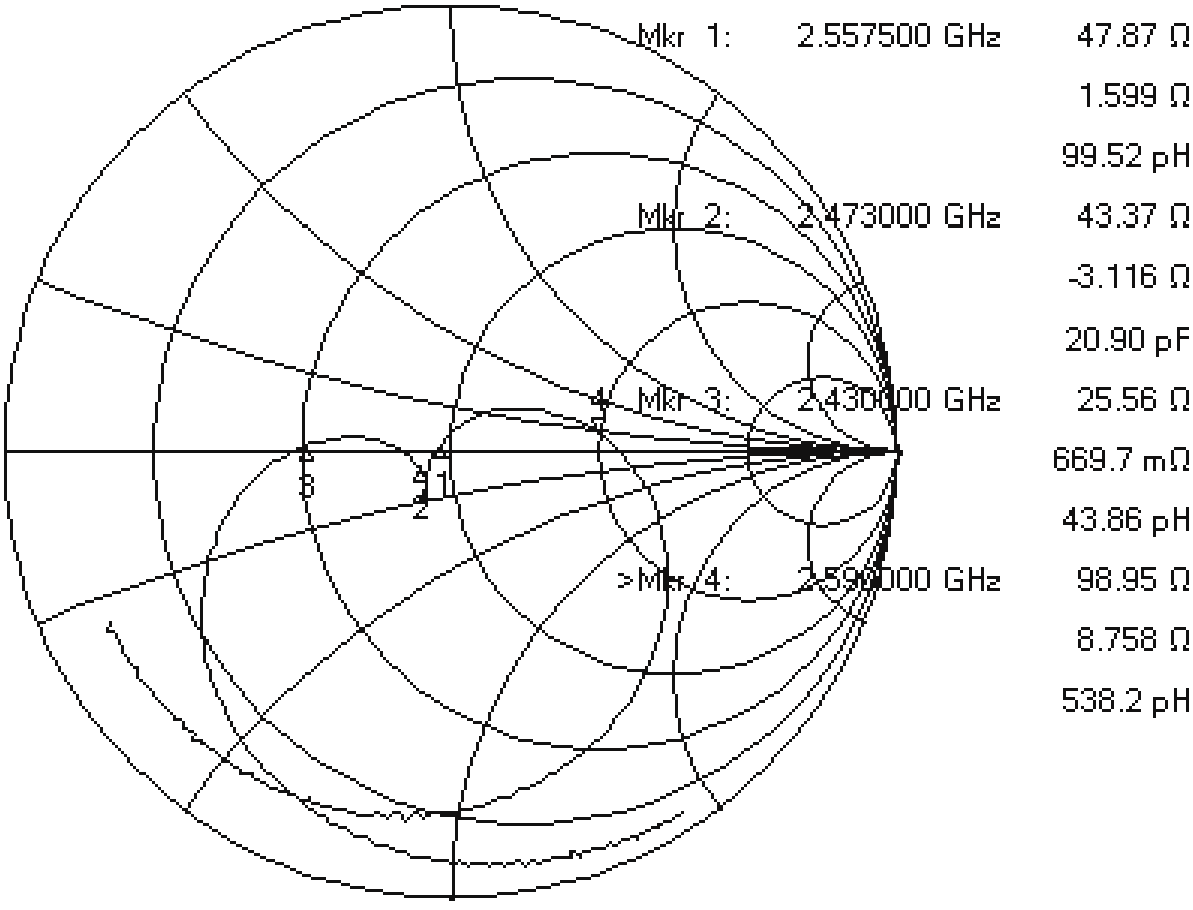

Figure 2.4: Feed point Impedance at various frequencies for bottom feed.

2.6.2 Coaxial feed from radiating plane

1. Log S11 plot with frequency (refer figure 2.5): The resonance is seen at two points as expected.First at 2.5575GHz and second at 2.4730GHz with the minimum return loss(Marker 1 and 2 in figure).Marker 3 and 4 are the points of 10 dB crossing which determines the bandwidth.The obtained bandwidth is 175MHz which is good and acceptable for the ZigBee band.

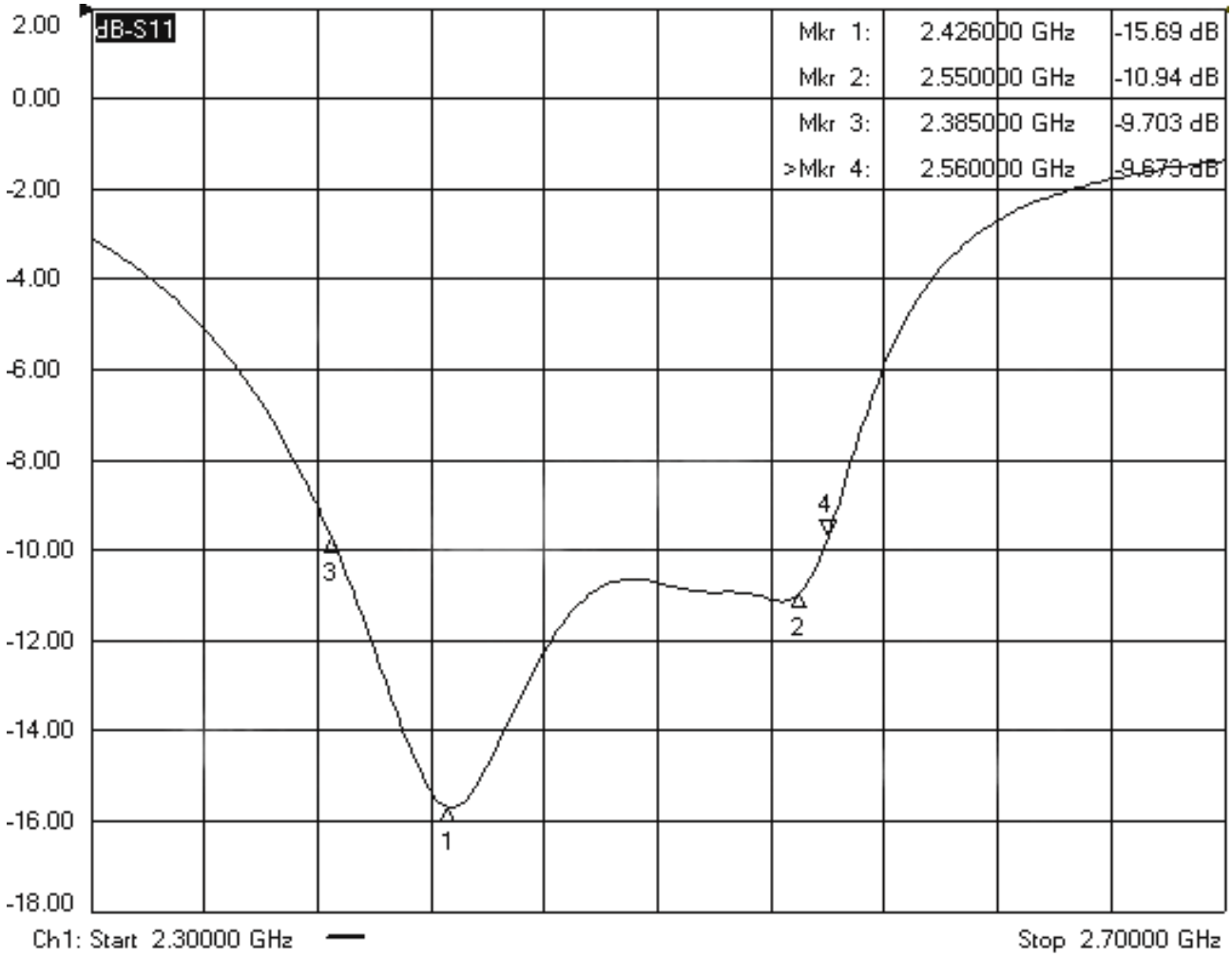

Figure 2.5: Log S_{11} Vs Frequency for top feed.

2. Smith chart (refer figure 2.6) : It is clear form the smith chart that marker 1 and Marker 2 where antenna resonates has impedance very close to 50Ω as

expected.This would ensure better matching at the feeding points and results in minimum return losses.The value of marker 1 is 2.426GHz with 42.702 Ω and 6.6111 Ω with PH=433.89.

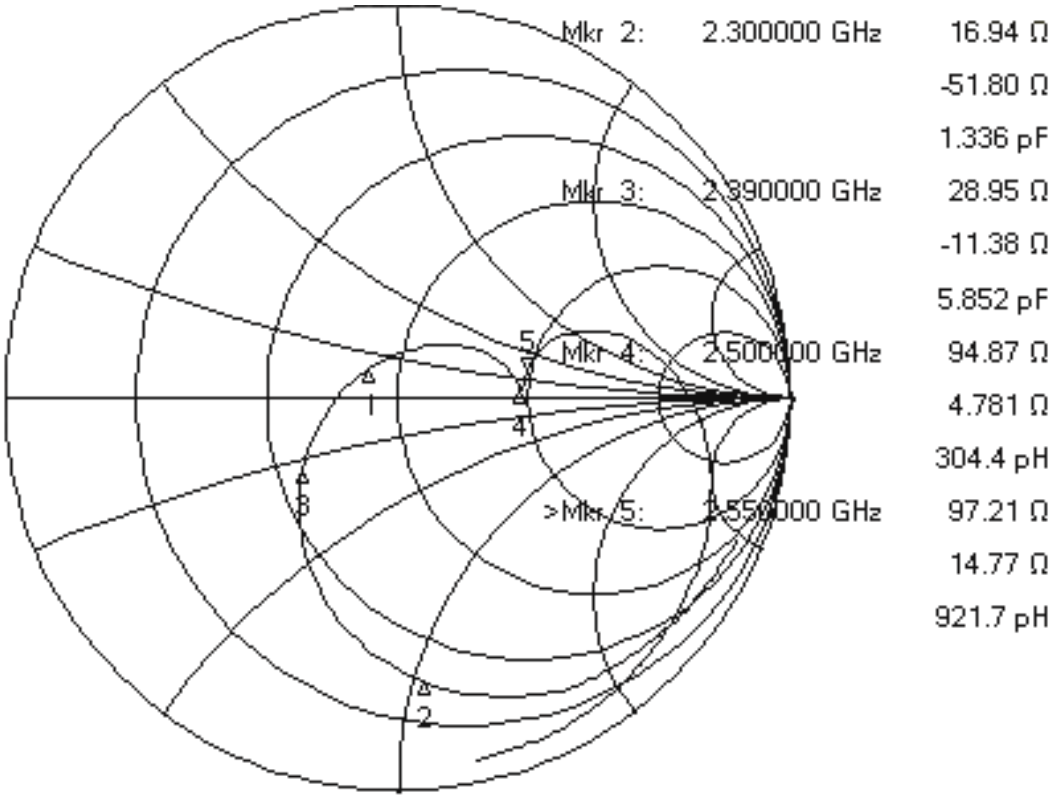

Figure 2.6: Feed point Impedance at various frequencies for top feed.

CHAPTER 3

Pin arrangement and top level functional description

ZigBee transceiver chip uses Zero-IF architecture for the reasons of low power consumption,low cost and high level of integration and linearity.At the same time it eliminates passive IF filters as no image rejection filter is needed and RF Spectrum is translated to the base band in the first down conversion.However it does have some disadvantages like dc-offset, even order distortion, flicker noise, I/Q mismatch and LO leakage.In the transmitter chain, the base band signal after a digital-to-analog converter (DAC) is filtered and amplified by the LPF and PA respectively. After that, the analog base band signal is upconverted to the RF signal directly .
Superheterodyne and low IF architecture are other two architecture used in modern handsets but they require off-chip components and are also complicated.Thus they consume more power.Due to these reasons Zero architecture was chosen in the design.Figure 3.1 shows the block level diagram of signal path in Zero IF architecture.

3.1 Pin Arrangement

The figure 3.2 gives the pin arrangement in the transceiver chip.

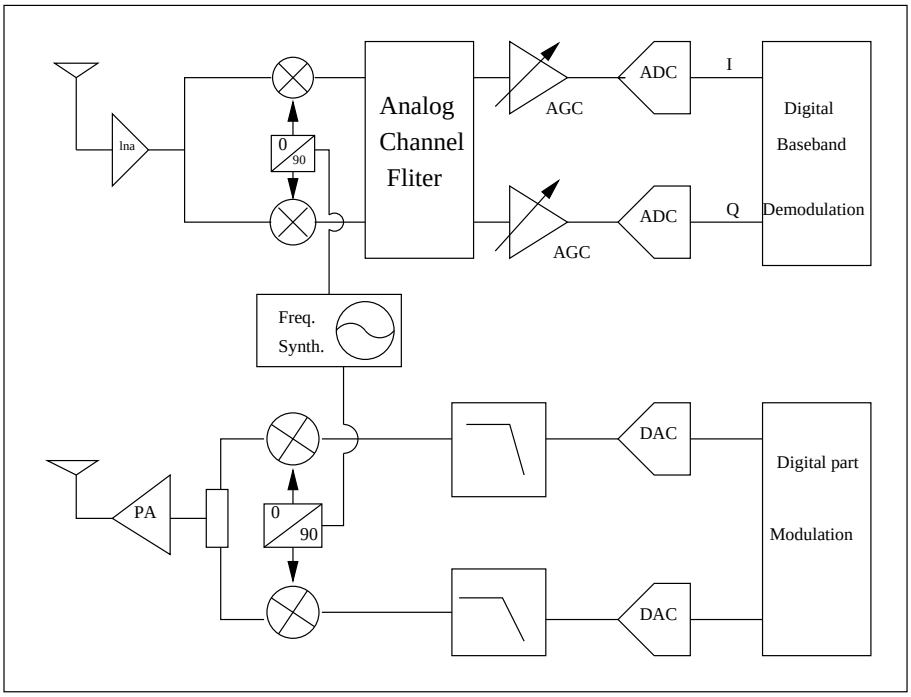

Figure 3.1: Block diagram of the ZERO-IF transceiver

3.2 Top level functional description

Block level functional description for each part in the chip is mentioned in brief below,for details of design please see references.:

3.2.1 Rx chain-Part1:

Low Noise Amplifier(LNA), Down Conversion Mixer and a programmable low pass Filter with their bias arrangement.

1. *LNA*: To amplify the weak incoming signal and prevent the adjacent interferes, LNA is used as first block of receiver chain.In the chip,the differential LNA is implemented to work in two gain mode with the gain switching of $14dB$. The high gain mode offers $15dB$ gain to the incoming signal when it is at low power

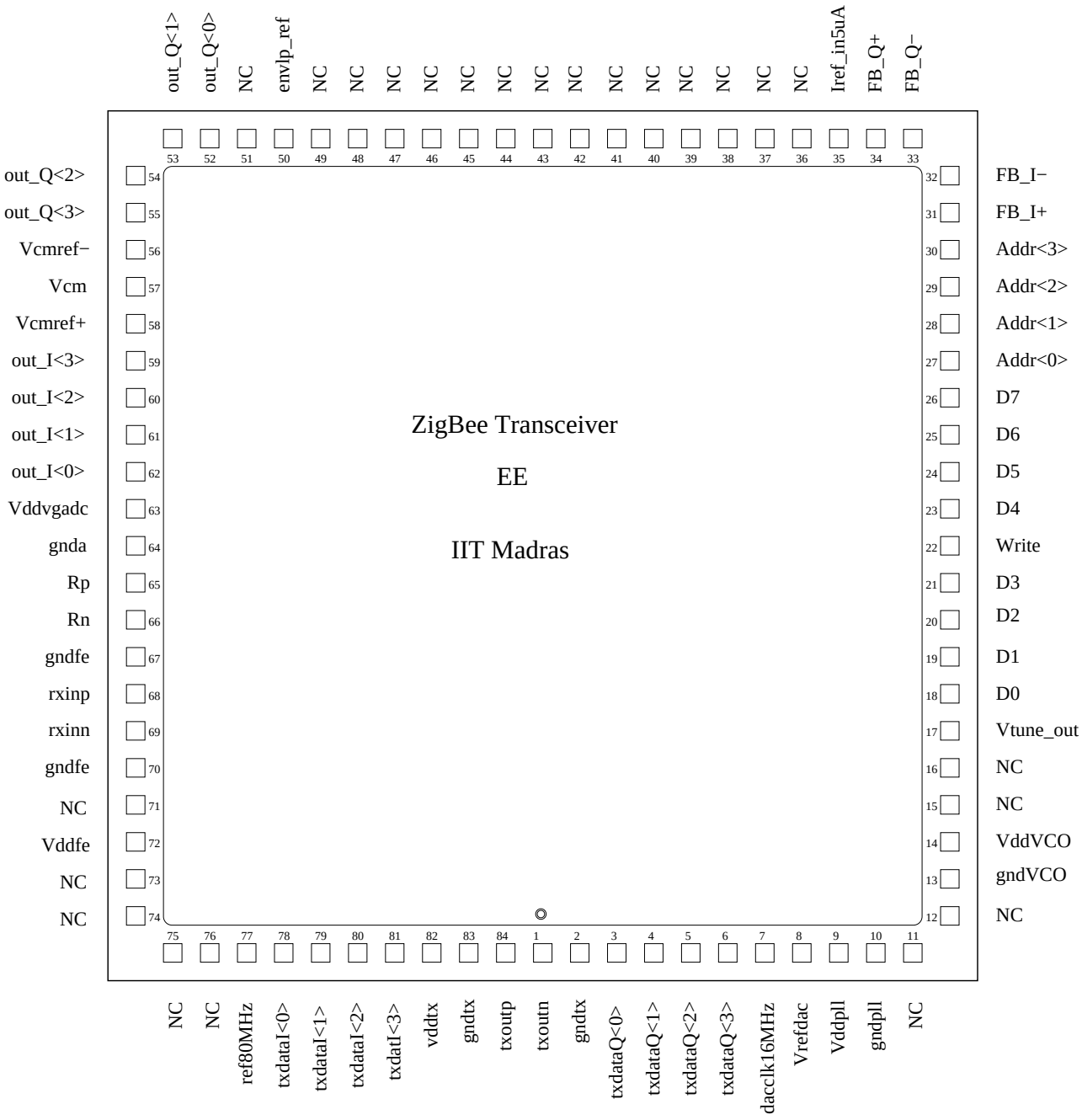

Figure 3.2: Pin Arrangement

level ($-85dbm$ to $-60dbm$) and just 1dB gain when the incoming signal has higher power level ($-60dbm$ to $-20dbm$).The resistive termination ,matching network and balun is to be provided off chip.

2. *Down Conversion mixer*: Active gilbert mixer is used for down conversion owing to its linearity of operation.The noise due to its mixer is minimized by larger length transistor, greater overdrive voltage and by using PMOS switches.The mixer feed a low pass filter.The output of the filter is buffered and is available as a *test pin* in the chip.

3. *Low pass Filter*:LPF suppress the higher frequency component and determines the BER and noise of the system.In the chip,a butter worth filter with single buffer and three pole section is used.The filter is digitally programmable to outwit the effect of component sensitivity over process and temperature.Filter bandwidth is $1.5MHz$ and DC gain of unity.The filter output is brought out of the chip as *test pin* to analyze the analog baseband signal.

3.2.2 Rx chain-Part2:

Automatic gain control(AGC),and Analog-to-digital converters(ADC).

1. *AGC*: The automatic gain control is made to provide a variable gain to incoming signal to make it swing for full range of ADC, with it drives.By varying the active load resistors form 12.45 Ω to 160 Ω the variable gain form 13.5dB to 65dB has been achieved.The third stage of AGC also have gain switching of 14dB .The loop filter used in the feedback path has DC gain of 16 and

3-db bandwidth of $1.8kHz$.The peak detector reference voltage is set to 1.5V *(which is set off chip)* so as the amplitude of the output from VGA is 3Vpp (full scale range of ADC).

2. *ADC*: Analog-to-Digital converter:Four bit ADC is used with Vpp output of 3V is used.The clock used is of 16MHz.

3.2.3 Frequency Synthesizer

Phase locked loop functioning as Frequency Synthesizer.

1. *Frequency Synthesizer*:LC oscillator based frequency synthesizer is used in the chip with output frequency range form 2.400GHz to 2.480GHz achieved by integer N divider with divider ratio form 480 to 496 and reference frequency of $5MHz$ (frequency input to the chip is $80MHz$ and it is divided by 16 to give reference frequency for PLL.). The VCO follows the divide by two circuit which gives the output frequency and is fed to the divider chin.A type three PLL with tri-state phase frequency detector is used and loop filter's pole zero placement is done to meet the stability.The unity gain frequency of the loop in PLL is $35KHz$ and settling time is $110us$.

3.2.4 Tx Chain

The transmitter chain consisting of Digital-to-analog converter(DAC), Low pass filter, mixer and Power Amplifier.

1. *DAC*:The 4 bit DAC with oversampling of 8 times is used in the chip.The sampling frequency is $16MHz$.A second order low pass butter worth filter follows the DAC and has cut-off frequency of $1.5MHz$.This follow the upconversion mixer made form active gilbert cell.

2. *Power Amplifier*:The power amplifier placed at the end on the transmit chain has 8 possible gain settings that is programmable form the embedded memory in the chip.The class AB power amplifier is used in the design.

3.2.5 Supporting circuits

Memory registers, Bias current generator, and Clock generation circuit.

1. *Memory register*:The memory registers is a digital interface of the chip and is used to program the chip for various modes of operations in Rx,Tx chain and the frequency synthesizer.The memory has 8 bit input data lines ($Data < 0 : 7 >$), 4 bit address lines ($Addr < 0 : 3 >$) and one write enable.Out of possible sixteen registers (4^2) only 4 are used in the chip.

2. *Clock and Bias generation*:From of the input clock of $80MHz$ the ADC and DAC clock of $16MHz$ and the PLL reference clock of $5MHz$ is generated.Current biasing arrangement is used to bias the entire transceiver chip.Required current and bias voltages are generated using the cascode mirrors arrangement form a 5μA input current reference and 1.8V supply for various blocks.Most of the biasing voltages and current needed is generated in form this circuit.

CHAPTER 4

Embedded Memory and its Programming

The first section of the chapter describes memory register used in the chip.

4.1 Embedded Memory Block

As described in chapter 3, various blocks in the chip are programmed using a digital interface to the outside world.Figure 4.1 shows the block diagram of the Embedded Memory in the chip.It is a 4 bit address bus memory with 16 registers, each with 8 bit data bus.A one bit positive logic write enable pin performs the write operation.The table 4.1 describes the input-output pins of the embedded memory.It is driven by 1.8V supply.

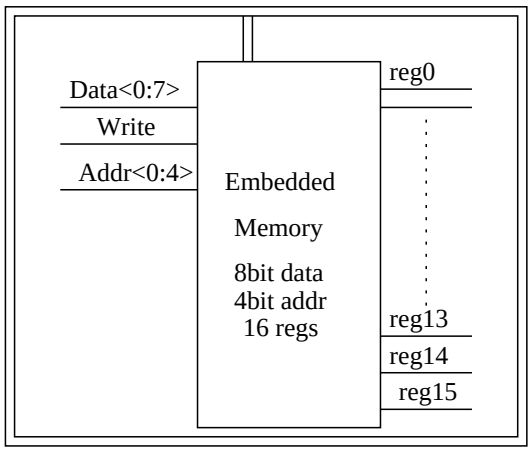

Figure 4.1: The block diagram of the memory cell.

Table 4.1: Input/Output ports in Embedded memory

Signal	Direction	Description
Data<0:7>	Input (logical high)	8 bit data bus for writing data to registers.
Addr<0:3>	Input (logical high)	4 bit address bus to enable the register.
Write	Input (logical high)	1 bit write enable to perform write operation.
$reg14 < 0:7 >$	Output(logical high)	8 bit register to control receiver modes.
$reg13 < 0:7 >$	Output(logical high)	8 bit register to control VCO modes.
$reg12 < 0:7 >$	Output(logical high)	8 bit register to program divider modulus.
$reg11 < 0:7 >$	Output(logical high)	8 bit register to control Transmitter modes.
reg10-reg0	Output(logical high)	Not Used in the chip.
reg15	Output(logical high)	Not Used in the chip.
$reg_{bar}0-15$	Output(logical high)	Not Used in the chip.

Functioning :The writing and reading to and form the embedded memory involves the Address, Data and write pins.When a given register is to be written, its address is put in the address bus and corresponding data in the data bus.A high in the write pin will write the data in the desired location.The read operation is asynchronous and once a register is written it can be read instantaneously.

4.1.1 Registers Used

Of all the 16 registers in the memory only 4 are used in the chip and are described as under:

1. *Register Address 11*: Controls different modes of Transmitter chain.Can be accessed by the address 1011.The table 4.2 details its bits functions.

2. *Register Address 12*: Controls the Frequency Synthesizer modulus.Can be accessed by the address 1100.The table 4.3 details the its functions.

Table 4.2: Register 11 bit description

bit	control pins	Control Function
$0-3$	Txpower$< 0:3 >$	the strength of PA.All zero: Maximum power output.
4	TxPd	the Up conversion mixer.High on this activates it.
$5-7$	Txdummy$< 5:7 >$	Not used in the chip.

Table 4.3: Register 12 bit description

bit	control pins	Control Function
$0-4$	modulus$< 0:4 >$	Program the modulus(form 0 to 31).
$5-7$	plldummy	Not used in the chip.

3. *Register Address 13*:Controls different modes of VCO in Frequency synthesizer.Can be accessed by the address 1101.The table 4.4 details its bits functions.

Table 4.4: Register 13 bit description

bit	control pins	Control Function
0	vcofreq$< 0 >$	adds a parallel capacitor to VCO varactror.
$1-2$	vcofreq$< 1:2 >$	Not used in the chip.
3	Vtune_{ctl}	enable control voltage monitor
4	vcoibias$< 0 >$	for high VCO current 120μA else 100μA.
5	vcoibias$< 1 >$	for high buffer1$current$60μA else 80μA.
6	vcoibias$< 2 >$	for high buffer2$current$60μA else 80μA.
7	vcodummy	Not used in the chip

4. *Register Address 14*:Control the different modes of Receiver chain.Can be accessed by the address 1110.The table 4.5 details its functions.

Table 4.5: Register 14 bit description

bit	control pins	Control Function
$0-2$	rxbw$<0:2>$	Rx filter Bandwidth.
3	rxgain	$14dB$ Gain switching of LNA
4	rxpd	the down conversion mixer.A high activates it
$5-7$	rxdummy	Not used in the chip

4.2 Programming the registers

We used the FPGA Spartan 3 series board to program the Memory.Figure 4.3 shows the test setup for the testing of chip with verilog code and Xilinx ISE software the memory was programmed.Figure 4.4 shows the module generated by the ISE projest nevigator for data writing in registers.It has a main clock (mclk) of $50MHz$ as input available in FPGA board itself,an asynchronous reset button (rst) to clear the registers and the input dacclk ($16MHz$) taken form the chip to pass the data to chip.The data bus,address bus ,write clock and signal data I/Q components are the outputs.The figure 4.2 shows the waveforms that was observed in Logic analyzer.Here the data gets stabilized well before the positive edge of the write clock (wclk) and ensures that correct writing to the register.The address and the corresponding data changes as required.

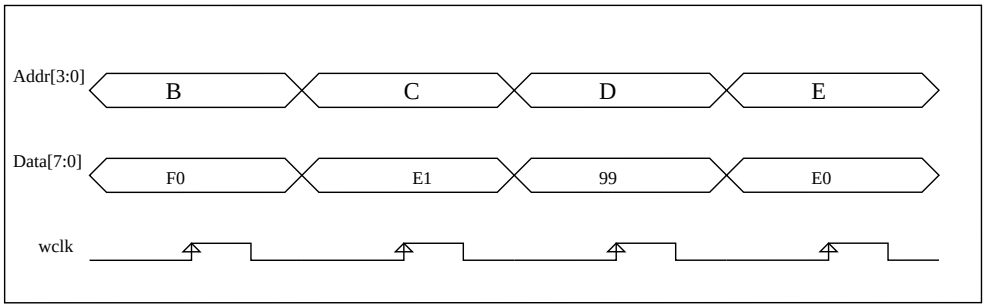

Figure 4.2: Writing operation to memory block.

NOTE: The spartan 3 FPGA series gives the output of 3.3V pp but the chip and the memory registers is designed for 1.8V pp compatibility.To overcome this problem we used a potential divider circuit at each output of the FPGA board before writing the data to registers.

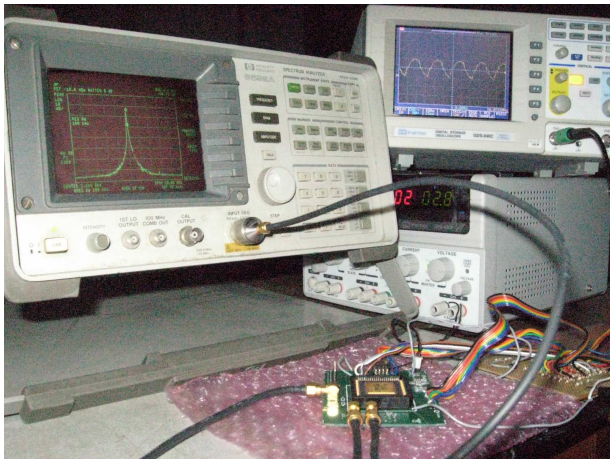

Figure 4.3: Test setup for testing.

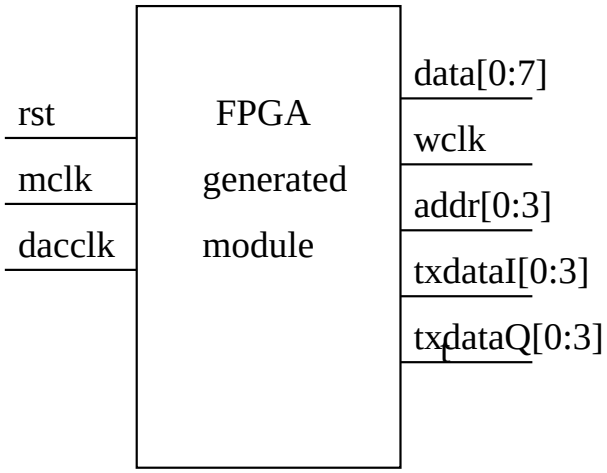

Figure 4.4: Module generated by Xilinx ISE software.

CHAPTER 5

Frequency Synthesizer Testing and Characterization.

The frequency synthesizer, which performs the main role of career generation for the down-conversion/ up-conversion, is a key building block in radio front-ends. Despite not being directly involved in the signal path, the performance of the synthesizer affects the overall performance of the transceiver.

This chapter is divided in three section.First section gives the overview of the architecture of PLL used in the chip and architectural properties of building blocks.The second section tabulates the specification set by ZigBee standard and that obtained in simulation .The third and last section deals with the hardware testing and results obtained with various chips that were tested in different settings and these results are compared with the needed specifications in section 2 and the conclusion is drawn.

5.1 Architecture and Architectural Properties.

This section is divided is three parts.(1) RF system of the voltage controlled oscillator and the CML divide-by-2.(2) Digital system consisting divider chain.(3) Analog system like phase/ frequency detector and loop filter.

1. *VCO*: LC based oscillator is employed to function as Voltage Controlled Oscillator.The capacitor in the LC tank is a varactor and varies with control voltage.Thus with the change is control voltage the frequency of oscillation can be varied to give the required frequency.This forms the basic principal of VCO and the control voltage versus output frequency relation characterizes the VCO.The tuning range of VCO is defined form this characterization and the K_{vco} is obtained form the slope of the curve so obtained.

   For this application the VCO should be tunable form 4800GHz to 4960GHz,ie a minimum tuning range of 160MHz (as it runs twice the output frequency).

2. *PFD and Loop Filter*: A nand-based tri-state Phase/Frequency Detector (PFD) is used to perform the role of phase/ frequency detection in the synthesizer.The PFD compares the divider output with the reference and generates UP and DN signals, which represent the difference in phase/ frequency of the two inputs.

   The charge pump converts these signals in to current information.The RC branch converts this current to voltage and is fed to VCO.This RC loop filter plays important role in loop stabilization, settling time and unity gain frequency.

3. *Divider chain*: The divider chain following the first divider is programmable from 481 to 496 (16 channels with center frequencies from 2.405 GHz to 2.480GHz with spacing of 5MHz).The divider used is prescaler based pulse-swallow architecture shown in figure 5.1.The reference clock of 5MHz is used and an integer-N PLL based synthesizer is designed as the output frequency

is intrgral multiple of input frequency.

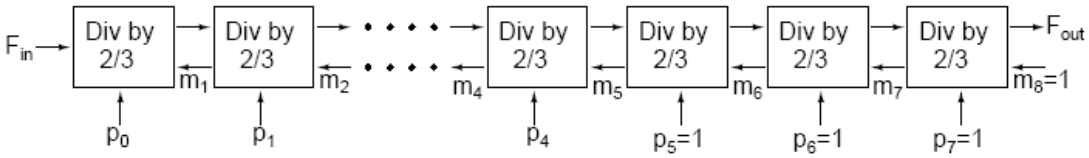

Figure 5.1: Block Diagram of Divider chain

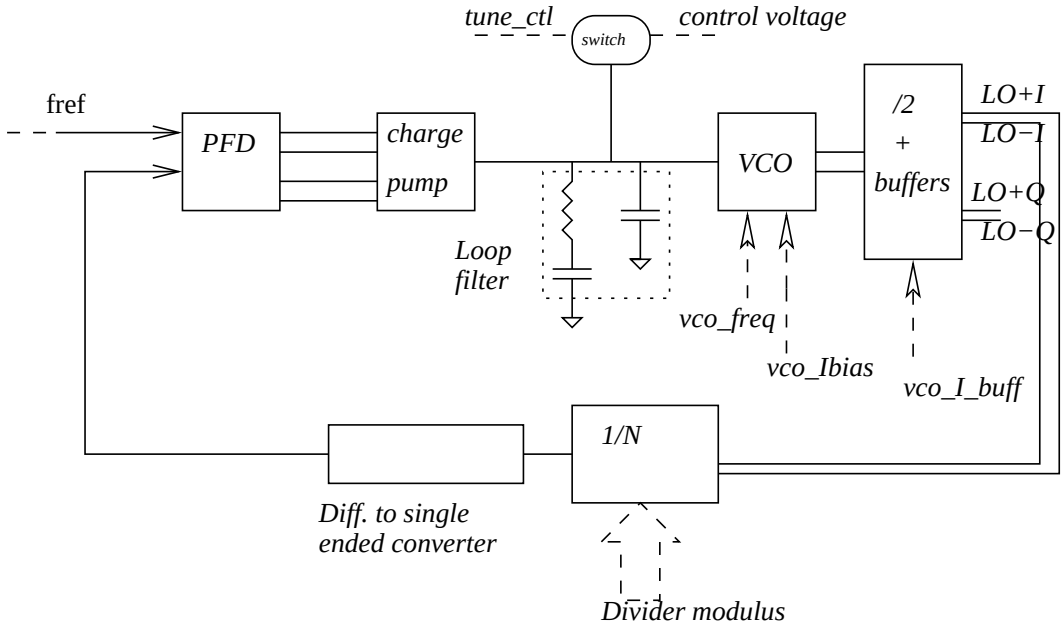

Figure 5.2: Block diagram of the Frequency Synthesizer

5.2 ZigBee Specification for PLL

This section tabulates the specification of frequency synthesizer.In the table 5.1 two column gives the specification that were needed by the ZigBee standard and that the frequency synthesizer was designed for.These specifications are then tested in third section.

Table 5.1: PLL Specification

performance metric	Value:ZigBee standard	Value:Simulation
Frequency Synthesis	2405-2480 MHz in steps of 5MHz	2405-2480MHz in steps of 5MHz
Phase Noise	-92dBc/Hz@3.5MHz	-117dBc/Hz@3.5MHz
Settling Accuracy	40ppm(100KHz of 2.5GHz)	40ppm(100KHz of 2.5GHz)
Spurs@5MHz	-20dBc	-39dBc
Spurs@10MHz	-50dBc	-50dBc
Settling time	196μs	110μs

5.3 Test Results and Comparison

This section gives the detailed results that were obtained during the project for testing the frequency synthesizer.The specification that are listed in previous section are observed and, where ever possible, supporting graphs and tables are presented.

We tested 8 chips (numbered form 1 to 8) of which only one worked as per expectation.The testing was done in two iteration.The PCB board was designed twice and are numbered as Board 1 and Board 2. The First one did not have the socket for mounting the chip and so the chip was hard soldered.The second one was designed with chip mounting socket to facilitate the quick replacing of chip.First two chips (1 and 2) in the first board and chips 3 to 8 were tested on second board.The Results, Mistakes and Graphs (where ever possible) are listed below.

This section is further divider in tho parts as Board 1 and Board 2

5.3.1 Board 1

Mistakes in this board:

- We mistakenly mapped the VddVCO supply to wrong pin in the chip.
- The bias value of V_{cm-Ref} was also mapped to the wrong pin in the chip.

Chips that were tested:

- *Chip* 1: Due to the above errors we could not see any spectrum and were suspecting the chip.The output that we could see was the 16MHz clock that is generated for DAC and ADC reference.
- *Chip* 2: This was also hard soldered in the first board.For this we went step by step and discovered the errors listed above.The PCB traces that were wrongly mapped were cut manually and correct mapping was done.

  We could see the spectrum at 2.405GHz for divider modulus of $N = 481$ and reference frequency of 5MHz.Also the spectrum shifted with the shift in reference frequency and increase in 'N'.The spectrum was shown to the Guide.

5.3.2 Board 2

The table 5.2 below gives details of testing with this board and table

Nature of failure:A default spectrum was observed and that was not shifting with reference frequency or divier modulus 'N'.With increase in frequency a sudden jump in control voltage from 52mV to 1.75mV was observes for all the failing chip.No

Table 5.2: Chips tested on Board 2

Chips Tested	No.3-No.8
Worked	No.4
Failed	rest all

Table 5.3: DC electrical Value of pins

Signal pins	DC value
txoutn,txoutp	1.8V
Vrefdac	0.9V
envlp$_{ref}$	1.5V
Vcmref-	0.15V
Vcm	0.9
Vcmref+	1.65V

gradual increment in V_{ctl} with f_{ref} was observed.The table 5.4 below shows the value for one of the chip.

Table 5.4: Fault in Chip No.7

Feed Frequency	Output Freq.	V$_{ctl}$
82.5MHz	2.411GHz	50mV
92.6MHz	2.566GHz	1.8V

Thus the tuning range came out to be 100MHz or less that is far below the required value.More over the all showed sudden jumps in frequency as against the gradual increase with frequency.

We suspected the divider chain to be not working and increased the input supply to 2V and tested all the chips.But the performance with the faulty chip remained the same.

Chip no.4

The Chip number 4 worked very close to the expected results.Below are the measurements and plots that were taken for the performance of chip 4.The setting of the register values and the instrument setting are tabulated below.

Table 5.5: Setting of Spectrum Analyzer for all the measurements

Resolution BW	100k
Video BW	10k
Attenuation	0dB
span	varied as per need
Ref level	-10dBm

NOTE The Spectrum Analyzer has the offest of -6dBm in the power level representation.

Table 5.6: Register settings for Chip no. 4

Reg. 11	F0	Pout of PA maximum ; Tx mixer on
Reg. 12		Varied form 481-496
Reg. 13	99	extra cap.;Vctl moniter on;VCO current 100 μA
Reg.14	E0	Rx cahin disabled

1. The results of chip 4, for supply 1.8V and Input $F_{ref} = 80MHz$ (F_{ref} to PLL is $5MHz$), is as under (Table 5.7):

   Here the frequency increment with each increment in divider modulus is 5MHz as expected.But the frequency obtained for each divider ratio setting is 1 channel away form the expected result.The possible sourse of error could be the free sunning frequency of VCO is not as designed or since the transfer function form the input to the output if PLL is a low pass transfer function and the

Table 5.7: Control voltage and Output frequency with 'N' for V_{supply}=1.8V and f_{ref} 80MHz

N (divier modulus)	V_{ctl} (mV)	F_{out} (GHz)
481	52.1	2.3996
482	145	2.4050
483	207	2.4098
484	262	2.4145
485	306	2.4197
486	347	2.4247
487	385	2.4297
488	422	2.4347
489	453	2.4398
490	483	2.4448
491	514	2.4498
492	544	2.4548
493	572	2.4599
494	603	2.4649
495	630	2.4699
496	658	2.4749

input frequency is only $5MHz$ the phase noise in the signal generator can be cause the error in output frequency.For this setting the VCO is characterized in figure 5.7.

2. The results of chip 4, for supply 2V (Increased supply) and Input $F_{ref} = 80MHz$ (F_{ref} to PLL is $5MHz$), is as under (Table 5.8):

   Here, with 2 V supply, the frequency increment with each increment in divider modulus is 5MHz as expected.But the frequency obtained for each divider ratio setting is 2 channel away form the expected result.The possible sourse of error could be same as said above.Here the control voltage measurement was not possible as it became very sensitive to the probe and as the probe was placed on the control voltage monitor the pll loses the lock and spectumm

Table 5.8: Control voltage and Output frequency with 'N' for V_{supply}=2V and f_{ref} 80MHz

N (divier modulus)	F_{out} (GHz)
481	2.4067
482	2.4067
483	2.4101
484	2.4151
485	2.4201
486	2.4251
487	2.4298
488	2.4348
489	2.4398
490	2.4448
491	2.4501
492	2.4558
493	2.4601
494	2.4651
495	2.4702
496	2.4752

gets distorted.This proves the sensitivity of reference voltage.

3. The results of chip 4, for supply 1.8V and Input $F_{ref} = 80.36MHz$ (F_{ref} to PLL is $5.023MHz$,Increased), is as under (Table 5.9):

   Here, with 1.8V supply and increased reference frequency of $80.36MHz$, the frequency increment with each increment in divider modulus is 5MHz as expected.But the frequency obtained for each divider ratio setting is 1 channel away form the expected result and the possible sourse of error could be same as said above.Figure 5.7 shows the charactrzation of VCO for control voltage versus output frequency.

Table 5.9: Control voltage and Output frequency with 'N' for V_{supply}=1.8V and f_{ref} 80.36MHz

N (divier modulus)	V_{ctl} (mV)	F_{out} (GHz)
481	216	2.4116
482	271	2.4166
483	317	2.4214
484	356	2.4264
485	392	2.4309
486	427	2.4359
487	460	2.4410
488	492	2.4460
489	521	2.4511
490	550	2.4561
491	580	2.4611
492	608	2.4661
493	637	2.4711
494	665	2.4760
495	696	2.4810
496	724	2.4860

5.4 Performance Evaluation and Comparison

The frequency synthesizer was tested for all the value of divider modulus and other settings.The table 5.10 below list the noise performance seen in the spectrum of frequency synthesizer.The plots of spectrum obtained in spetrum analyzer is also shown.

Comparing the results obtained with that listed in table 5.1 we see that the frequency synthesizer meets most of the specification of the standard.

Figure 5.6 shows the zoomed picture of spectrum where spurs at 5MHz offset for the center is seen which is the evidence of locking of the pll.The settling of control voltage was also observed (where ever possible) on the oscilliscope, and it was seen to be quite settled with peak-to-peak variation of just 38mV-40mV.

Table 5.10: Synthesizer performance:Fref=80MHz,chip 4, N = 480,V_{supply} = 1.8V

performance metric	Test Results
Frequency Synthesis	2405-2480 MHz in steps of 5MHz form section 5.3.2
Phase Noise	-132dBc/Hz@3.5MHz
Settling Accuracy	not achieved, Slip of one channel
Spurs@5MHz	-48dBc
Spurs@10MHz	-56dBc
Settling time	could not measure

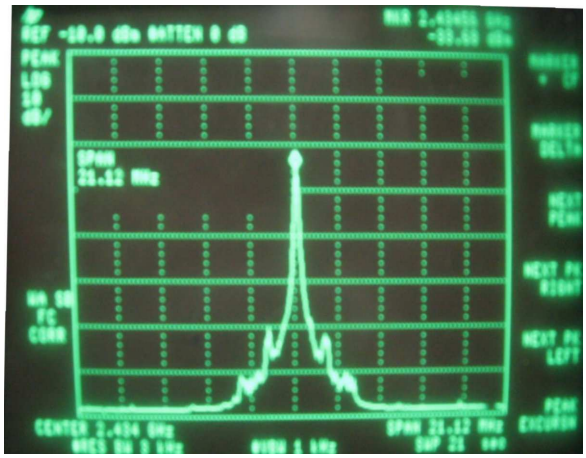

Figure 5.3: Spectrum:Fref=80MHz, Vdd=1.8V

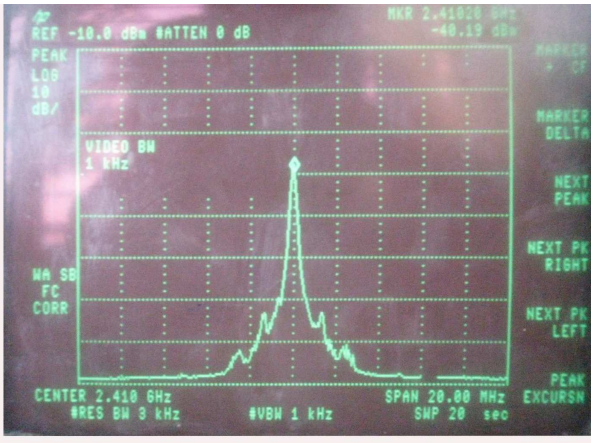

Figure 5.4: Spectrum:Fref=80MHz, Vdd=2V

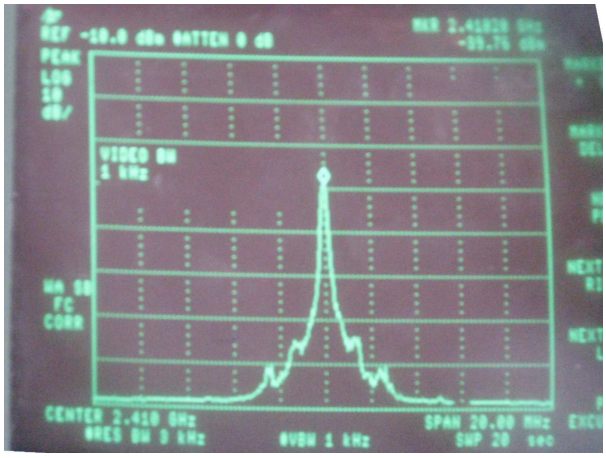

Figure 5.5: Spectrum:Fref=80.36MHz, Vdd=1.8V

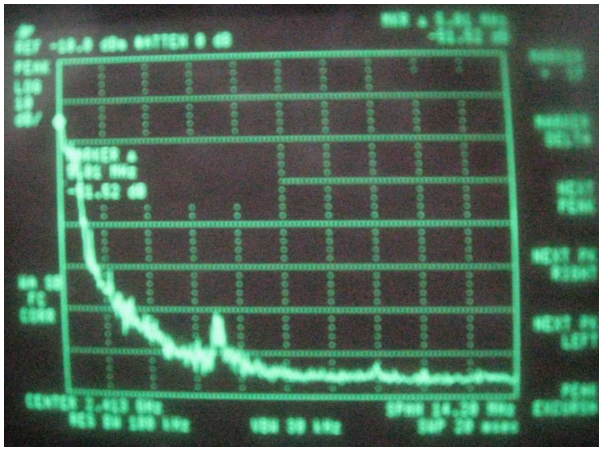

Figure 5.6: Phase noise spur visible at 5Mhz

Spectrum figures 5.3 , 5.4, 5.5 also shows the settled frequency synthesizer for different suppy voltages as the output spectrum seen is a typical spectrum of a frequency synthesizer.

Form the plot 5.7 a linear relation of the form in equation 5.1 is seen between output frequency and control voltage.Also the consistency in VCO functioning can be concluded as the graphs obtained for two different input frequencies track each other very closely.The table 5.11 gives specifications of VCO obtained from the figure 5.7

$$f_{out} = f_o + K_{vco} * V_{ctl} \tag{5.1}$$

Table 5.11: VCO specifications

K_{vco}	$\approx 164MHz/V$
f_o	4.72GHz
Tuning range	90MHz (2.40GHz - 2.49GHz)

5.5 Power Amplifier

This section presents the results obtained by the variation of output power for the power amplifier for a single divider modulus.That is by increasing the bit $0-3$ of register 11 in the memory the power output of PA can be varied and with this the output power of the spectrum in measures.This experiment ensures the functioning to PA.

1. The table 5.12 below gives the setting of Control Registers.

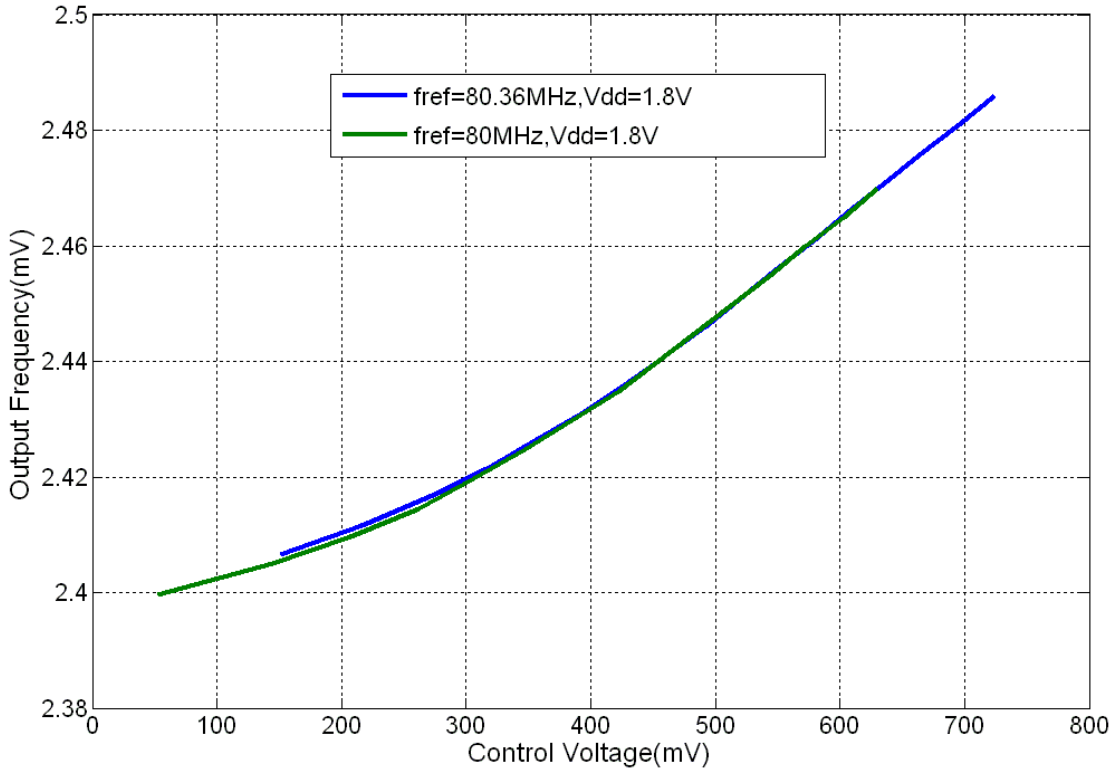

Figure 5.7: VCO Characterization.

Table 5.12: Register settings for Output Power test for chip 4

Supply voltage	1.8V	normal supply
Input F_{ref}	80.0MHz	Fref to PLL is $5MHz$
Reg. 11		PA strength varied; Tx mixer on
Reg. 12	N=494	set for a single frequency
Reg. 13	99	extra cap;Vctl moniter on;VCO current 120 μA
Reg.14	E0	Rx cahin disabled

Possible 16 combination for bits 0-3 of register 11 the power amplifier output has 16 different values.The maximum output is when all the 4 bits are down and minimum output is when all the 4 bits are up.The table 5.13 below gives the strength of output spectrum for settings in above table.

Table 5.13: Output Power with variation in strength of PA for 1.8V and N=494

bit values[MSB-LSB]	potput power (dBm)
0000	-19.44
0001	-20.11
0010	-20.65
0011	-21.37
0100	-21.92
0101	-22.8
0110	-23.88
0111	-24.58
1000	-25.6
1001	-26.9
1010	-28.6
1011	-30.25
1100	-32.29
1101	-35
1110	-41
1111	-52

2. The table 5.14 below gives the setting of Control Registers.

Table 5.14: Register settings for Output Power test for chip 4

Supply voltage	2V	increased supply
Input F_{ref}	80.0MHz	Fref to PLL is $5MHz$
Reg. 11		PA strength varied; Tx mixer on
Reg. 12	N=494	set for a single frequency
Reg. 13	99	extra cap.;Vctl moniter on;VCO current 120 μA
Reg.14	E0	Rx cahin disabled

Possible 16 combination for bits 0-3 of register 11 the power amplifier output has 16 different values.The maximum output is when all the 4 bits are down

and minimum output is when all the 4 bits are up.The table 5.15 below gives the strength of output spectrum for settings in above table.

Table 5.15: Output Power with variation in strength of PA for 2V and N=494

bit values[MSB-LSB]	output power (dBm)
0000	-19.66
0001	-20.2
0010	-20.92
0011	-21.56
0100	-21.22
0101	-23.07
0110	-23.82
0111	-26.00
1000	-26.00
1001	-27.26
1010	-28.82
1011	-30.52
1100	-32.70
1101	-35.76
1110	-41.63
1111	-53.60

Here, form table 5.13 and 5.15 the output power increases with increasing strength of power amplifier.The increase/decrease is more when the MSB is switched and is less when LSB is switched, which commensurate with the design of PA.Also the two case taken above, one for 1.8V and other for 2V, there is increase in output power for eash power level of PA for the case of 2V supply which is again as expected as the rail voltage has been increased.

CHAPTER 6

PCB board design, Schematic and layout

This chapter discusses, in brief, the design of PCB boards for mounting of chip, the issues related to PCB design,the schematic and layout.

6.1 Design of PCB

OrCAD software is used to design the PCB board.The design is made on copper plated FR-4 substrate.During hte chip testing and characterization phase, two PCB's were manufactured.PCB1 was not desighed for a socket mount of chip and PCB2 had a socket to mount the chip.Some issues of PCB design are presented below.

1. Power Supply Routing

   The power supply routing is an issue in RF boards as the system performance of the synthesizer is affected by corruption in power lines.The control voltage of the VCO is very sensitive to outside world and also to the power supply variation.

   The supply lines are susceptible to high frequency noise.Before entering the chip, the noise is filtered using the parallel bank of surface mount capacitors.Also a constant voltage reference generator is used to generate 1.8V supply.

2. Grounding Scheme

   The PCB should have proper grounding scheme.The proper selection of placement of external components and appropriate routing of traces the floating islands can be reduced and single ground plane can be formed.The ground plane minimizes the parasitic impedance in RF signal paths.

3. Reference Clocks

   The reference clock of 80MHz is obtained form the signal generator,instead of a dedicated crystal.The more the accurate the clock is, netter the performance of synthesizer.Since the PLL loop is low pass, most of the jitter in the reference gets transmitted to output without any attenuation.So for application purposes the dedicated crystal is a must.For the purpose of testing the signal generator would suffice.The reference is matched to 50 Ω

4. Biasing

   The power supply is regulated using TPS7301QD chip.This is not a adjustable supply regulator but an adjustable supply regulator would be handy to use for testing at 1.8V and 2V.The bias current of 5μA is needed to the chip.As we didn't have the current reference generator we used register to accomplish this job.The value of register was adjusted to get the current very close to 5μA.The accuracy of this current source is essential as all the bias current is the chip is derived ftom this current reference.

5. Off chip components

   The off chip components that were used are SMA connector, SMD capaci-

tors and resistors, power regulator and 10nH inductor to bias output pins of transmitter,100KΩ resistance for bias current, 2kΩ external resistor for constant g_m bias circuit.

6. PCB trace coupling

   The reference provided for VCO is usually a strong signal.The PCB 2 that we designed suffered form the coupling problem.It was observed that the control voltage was picking the DAC clock frequency of 16MHz which is generated form the reference frequency internally.The reason that we found was the nearly placed traces of the two signal.We manually disconnected the trace and managed to isolate the control voltage form the dac clock.

6.2 Schematic of the board designed

Figures 6.1, 6.2, 6.3 shows the schematic of the board that was desiged.This schematic is divides in two parts, one is power supply block and other is RxTx block that house the chip.

6.3 Layout

Figures 6.4 and 6.5 are the layout of the printed antenna and the PCB board that was designed for the testing.

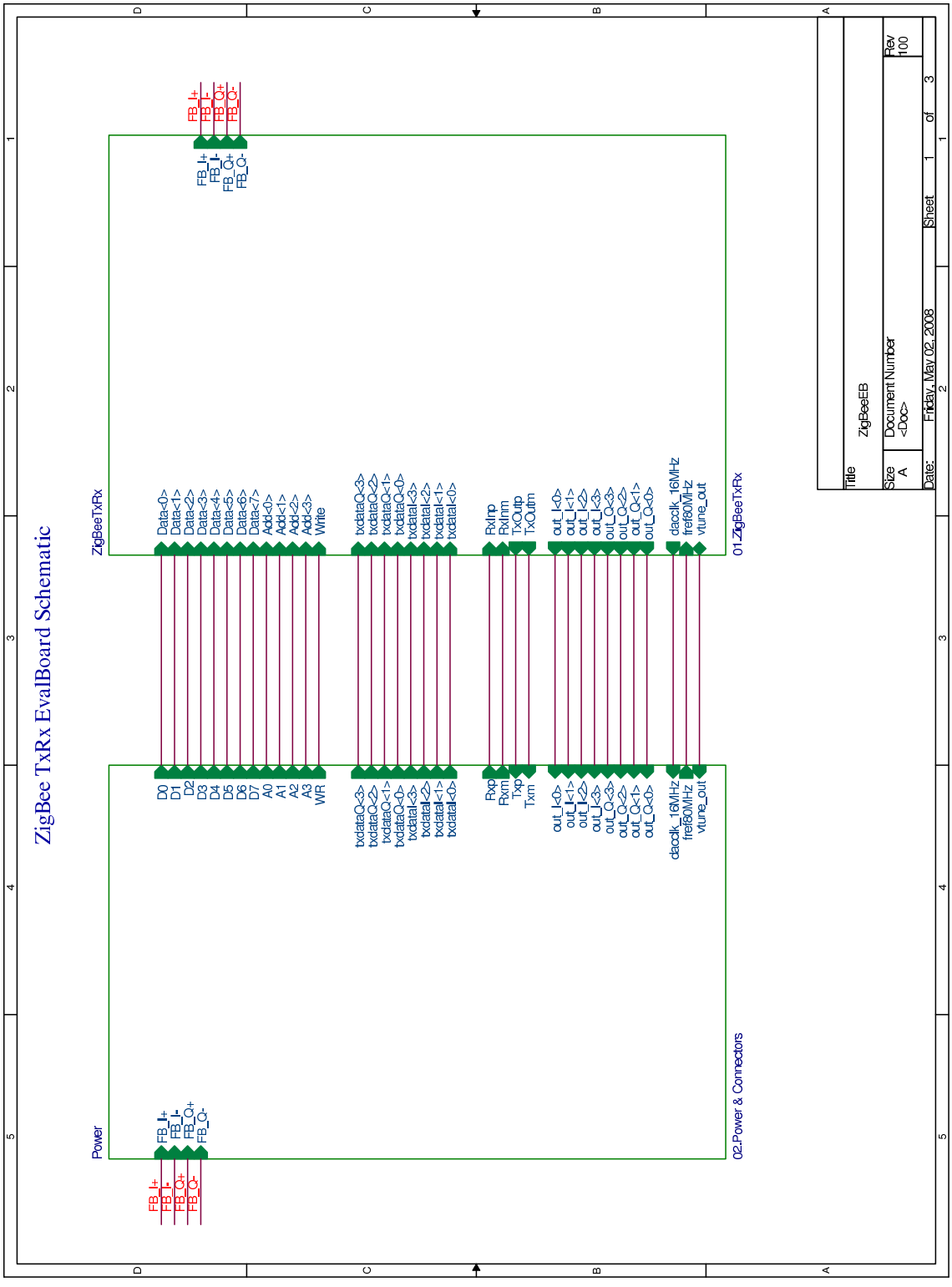

Figure 6.1: Top level schematic

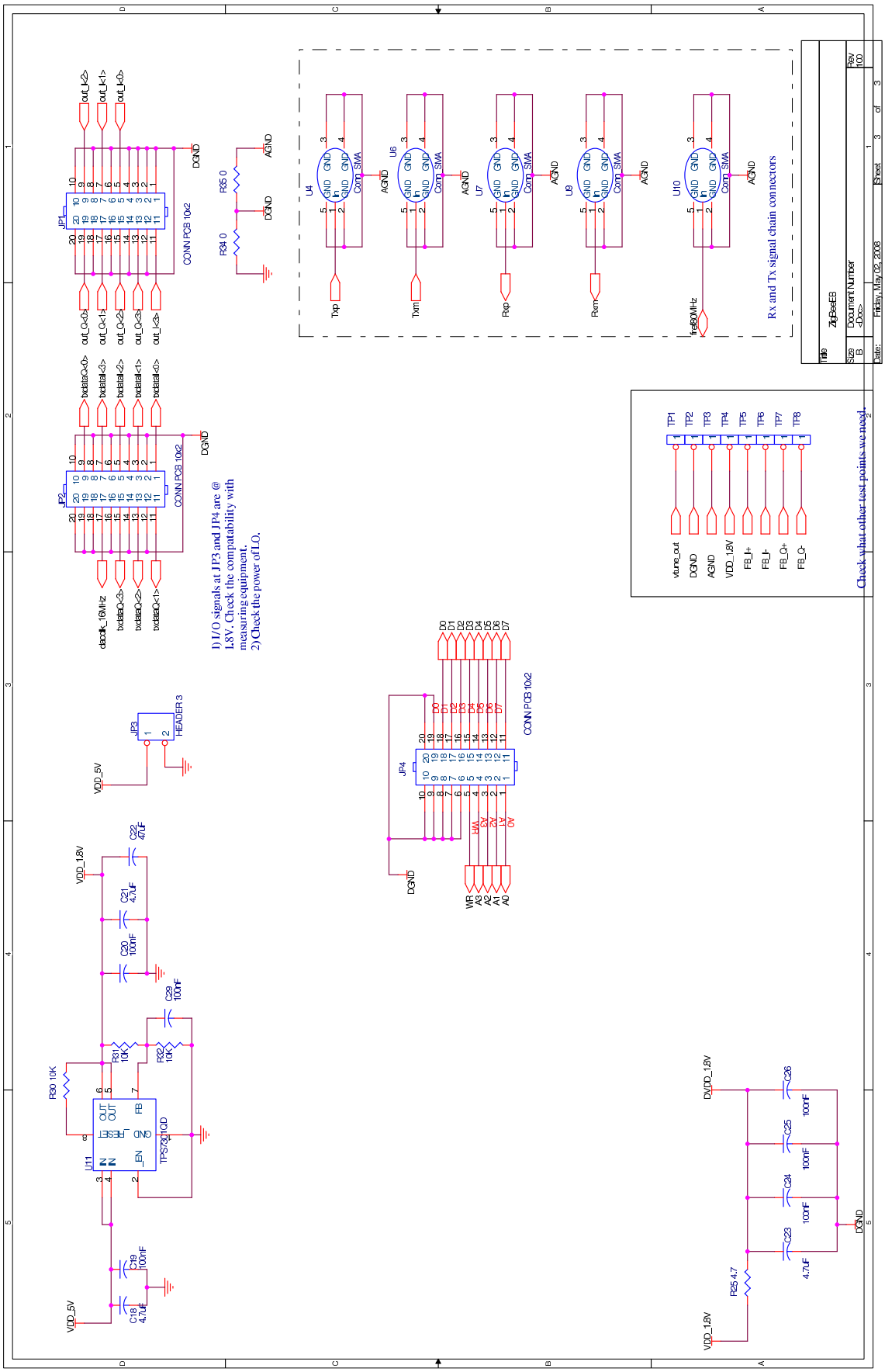

Figure 6.2: Power supply lock

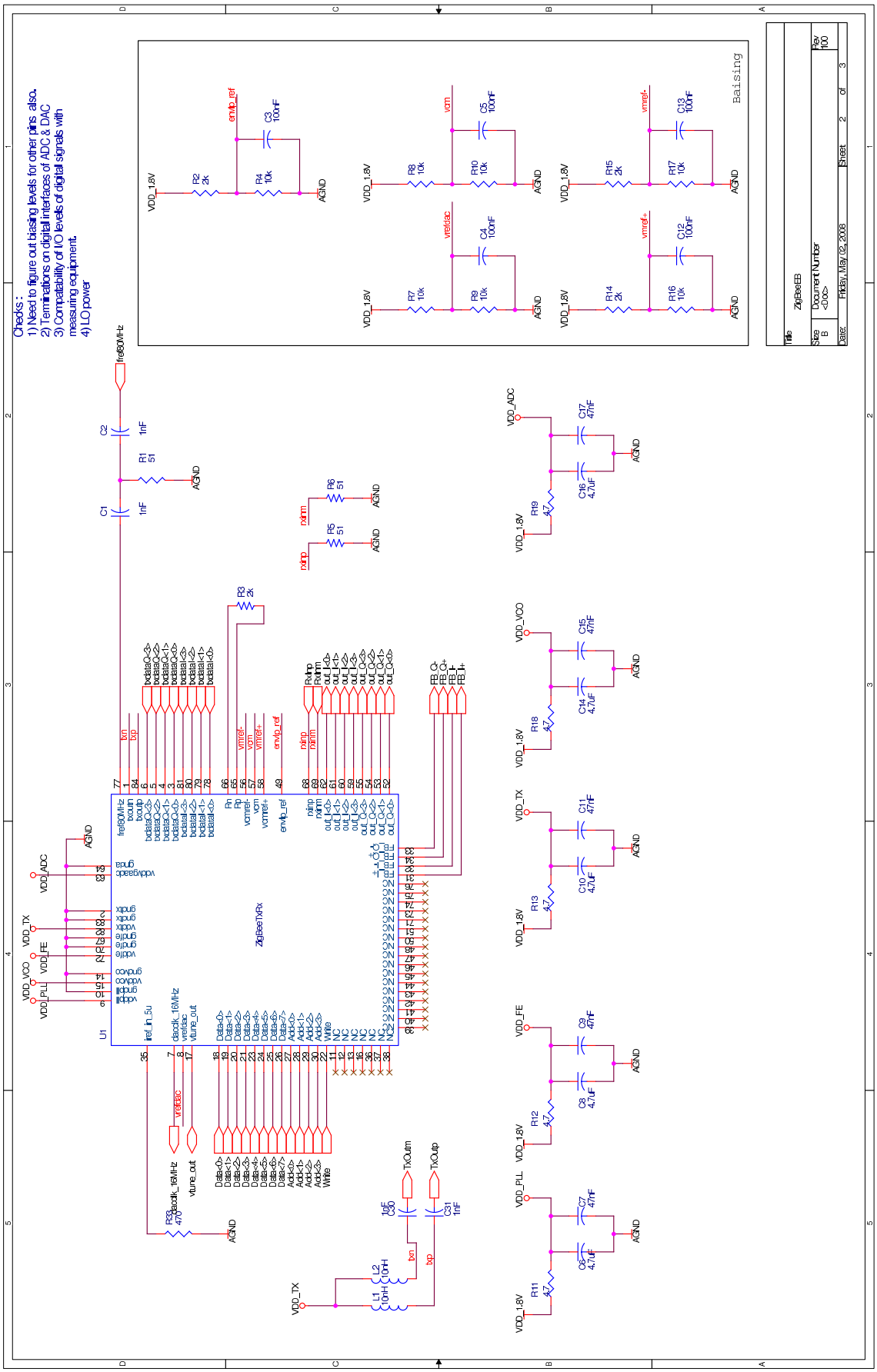

Figure 6.3: RxTx block

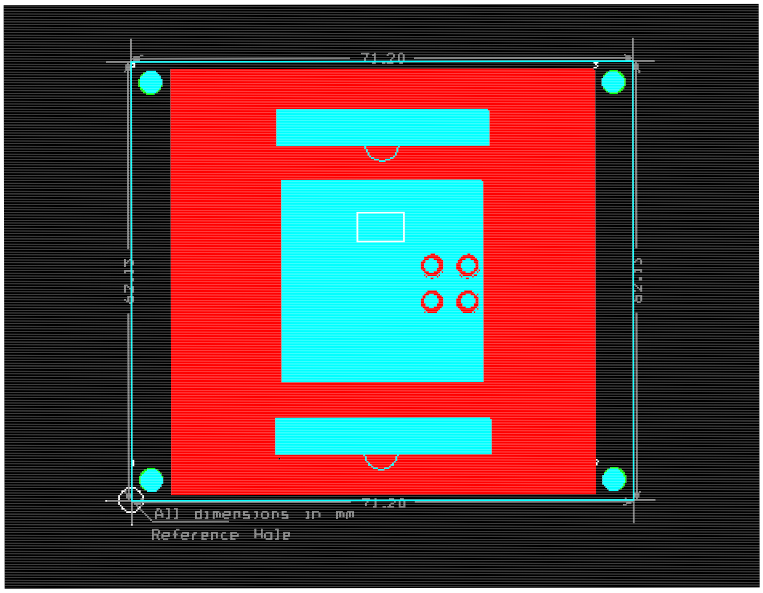

Figure 6.4: Layout of Antenna

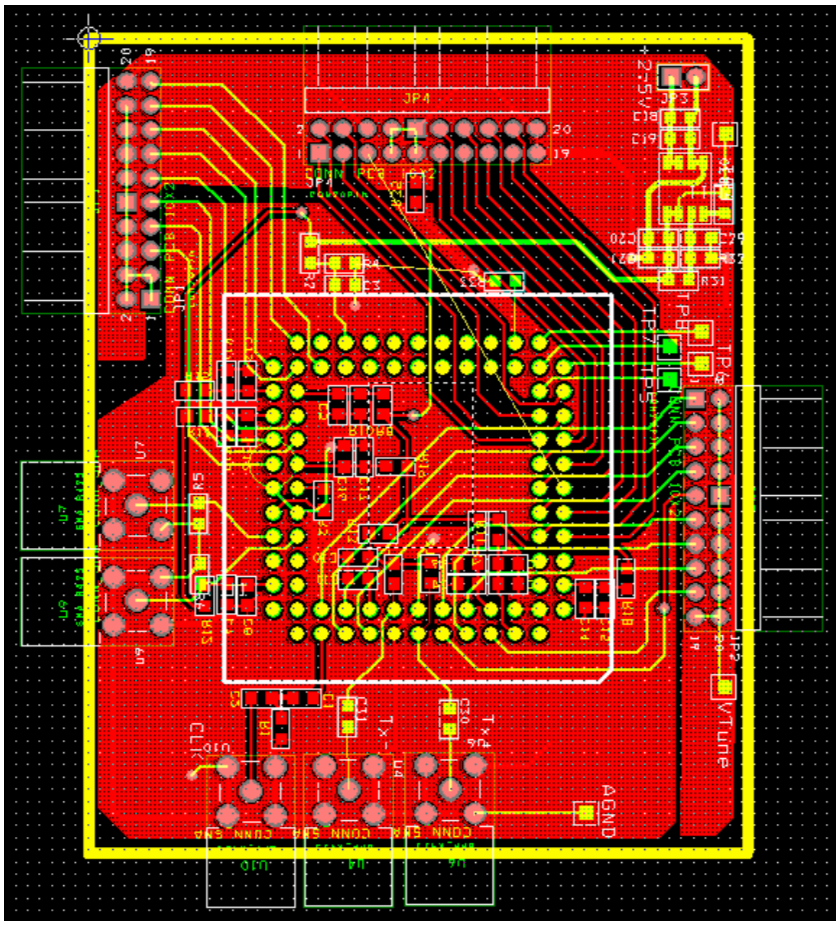

Figure 6.5: Layout of board

CHAPTER 7

Conclusion

The project was intended to test the entire chip but due to lack of time and unavailability of appropriate components we could just characterize only the frequency synthesizer which it self took longer than expected time.

The results of frequency synthesizer listed in chapter 5 shows that most of of the specification of the standard were met.The functioning of frequency synthesizer with increase in divider modulus was linear with $k_{VCO} \approx 164$ MHz/V, phase noise of -132dBc/Hz@3.5MHz offset and tuning range of 90MHz, but an unexpected shift of 1 modulus was observed.The reason could be the phase noise of the input reference form the function generator,as was mentioned in chapter 6 or the fabrication itself which could have shifted the free running frequency of VCO.Other specifications like phase noise and spurs were met easily as per the ZigBee standard.The frequency synthesizer still has scope of improvement in terms of lacking performance to make it fully compatible for the IEEE 802.15.4 standard.

With the change in I/Q components of input data to the transmitter chain the increase in output spectrum power was seen confirming the mixer functioning.

With the increase in Power amplifier power the output power was seen to be increasing confirming the proper functioning of PA.

The fabricated antenna gave the expected result with respect to matching of approx 50 Ω and bandwidth more that 80MHz which is needed as per ZigBee standard.

7.1 Future Work

There are certain avenues for improvements in the testing procedures.The board was not made easy to switch between 1.8V and 2V, so the further testing could be done with this facility.At the same time the PCB design did not have all the test points that could be tested/probed so this too has little scope of improvement.The unavailability of modern RF testing equipments in the lab. caused little hindrance to the work.Instruments like real time oscilloscope and SeaSolver software by NI Inc. for RF transmitter testing would have eased the process.

The next phase of testing could be to finish the receiver and transmitter chain testing with the improvements suggested above.

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